Yassin Abulnaga

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Education

The University of British Columbia — Vancouver, BC

Bachelor of Applied Science in Electrical Engineering — *Aug. 2023 – May 2027*

- *Relevant Coursework:* Embedded Systems and Signal Processing (ELEC 291, A+), Computing Systems I (CPEN 211), Circuit Analysis I (ELEC 201, A), Computation in Engineering (APSC 160, A+), Data Structures & Algorithms (CPSC 259, A-)

Experience

Electrical Engineering Intern — May 2025 – September 2025

Kimko Electromechanical — *Dubai, UAE*

- Design and draft electrical circuits for power, lighting, and emergency systems using AutoCAD for residential and commercial developments.
- Assist in planning and laying out low-voltage electrical distribution systems, including socket outlets, lighting layouts, and backup systems (UPS, generators).
- Update and maintain single-line diagrams, panel schedules, and schematic drawings to reflect site changes and design revisions.
- Supervise on-site installation of conduits, cable trays, distribution boards (DBs), and switchgear in compliance with DEWA regulations.

Relevant Projects

Coin Retrieval Robot | *STM32, PIC32, UART, C* — Feb. 2025 – Apr. 2025

- Engineered an autonomous coin collection robot with wireless manual override using a PIC32-based controller.
- Integrated IR sensors, servo-driven electromagnet, and Colpitts oscillator for metallic object detection.
- Designed and implemented UART-based wireless communication (JDY-40) with PS2 joystick remote and LCD status output.
- Applied interrupt-driven FSM logic and PWM motor control to coordinate autonomous navigation and retrieval.

Oven Reflow Controller | *8051 Assembly, N76E003, Python* — Dec. 2024 – Jan. 2025

- Developed an embedded reflow soldering controller using a finite state machine architecture.
- Programmed thermal feedback control, LCD display, and keypad input in 8051 assembly on N76E003 MCU.
- Implemented a Python-based UART interface for real-time temperature visualization and state debugging.
- Integrated real-world sensors (thermocouple, OP07 op-amp) and actuators (solid-state relay) in a closed-loop control system.

16-bit RISC Central Processing Unit | *SystemVerilog, Quartus II, ModelSim* — Sept. 2024 – Nov. 2024

- Designed and implemented a single-cycle 16-bit RISC CPU using RTL design principles in SystemVerilog.
- Created a custom data path supporting instruction fetch, decode, and execution from RAM.
- Integrated ALU, shifter, and control logic using modular design methodology.
- Simulated CPU using ModelSim and tested key logic blocks, including timing behavior and signal correctness.

Technical Skills

Hardware Design: SystemVerilog, Verilog, FSM, RTL design, synthesis, Quartus II, ModelSim, ASIC design principles

Scripting & Programming: Python, C, C++, Assembly (8051/ARM), Git, MATLAB, LaTeX

EDA & Tools: Quartus II, ModelSim, AutoCAD, Jupyter, VSCode

Embedded Systems: STM32, PIC32, N76E003, UART, PWM, LCD, sensor-actuator integration

Testing & Debugging: Oscilloscope, Multimeter, Linux/Unix environments, system-level validation

Areas of Interest: ASIC Design, RTL Verification, Memory Circuit Design, Embedded Systems