# Yassin Abulnaga

+1 (236) 268-5455 | yabulnag@gmail.com | 3615 W 17 Ave, Vancouver | LinkedIn | GitHub

## Education

**The University of British Columbia** Vancouver, BC

*Bachelor of Applied Science in Electrical Engineering* *Aug. 2023 – May 2027*

- *Relevant Coursework:* Embedded Systems and Signal Processing (ELEC 291, A+), Computing Systems I (CPEN 211), Digital Systems Design (CPEN 311), Computation in Engineering (APSC 160, A+), Data Structures & Algorithms (CPSC 259, A-)

## Experience

**Electrical Engineering Intern** May 2025 – Sept 2025

*Kimko Electromechanical* *Dubai, UAE*

- Designed and drafted **40+ electrical circuit layouts** (power, lighting, SLDs) using AutoCAD for residential and commercial projects.
- Assisted in planning and laying out **low-voltage distribution systems** (socket outlets, lighting, UPS, generators), ensuring compliance with DEWA standards.
- Updated and maintained **20+ single-line diagrams, panel schedules, and schematics**, reducing revision turnaround time by **15%**.
- Supervised on-site installation of conduits, cable trays, DBs, and switchgear in compliance with DEWA regulations.

## Relevant Projects

**16-bit RISC Central Processing Unit** | *SystemVerilog, Quartus II, ModelSim* Sept. 2024 – Nov. 2024

- Designed and implemented a single-cycle **16-bit RISC CPU** in **SystemVerilog** with integrated **ALU**, shifter, register file, and control logic.
- Built a custom **datapath** supporting **20+ instructions** with instruction fetch, decode, and execution from **RAM**.
- Verified functionality using **ModelSim testbenches** and **15+ FPGA hardware tests** on **DE1-SoC**.
- Performed **timing analysis**, achieving stable execution at **50 MHz** and validating **memory-mapped I/O** programs.

**FPGA Multi-Core RC4 Cracking Circuit** | *SystemVerilog, ModelSim* Sept. 2025 – Present

- Implementing a hardware-accelerated **brute-force RC4** cracker with **10 parallel decryption cores** to search a **24-bit** keyspace.
- Building **FSM-based** control, ModelSim testbenches, and **FPGA bring-up** flows to debug timing, logic, and throughput.

**Coin Retrieval Robot** | *STM32, PIC32, UART, C* Feb. 2025 – Apr. 2025

- Programmed **firmware in C** on STM32/PIC32 to integrate sensors, motor drivers, and wireless override.
- Applied **interrupt-driven FSMs** and **PWM control**, enabling consistent retrieval with **90%+ accuracy** in 50+ tests.
- Implemented **UART wireless comms** with PS2 joystick remote and LCD debug output for low-latency control.

## Technical Skills

**Hardware & RTL Design:** SystemVerilog, FSMs, RTL design, memory-mapped I/O, timing analysis, Quartus II, ModelSim

**Embedded Systems & Firmware:** C/C++, Assembly (8051/ARM), STM32, PIC32, N76E003, UART/$I^2C$, PWM

**Verification & Debug:** ModelSim testbenches, FPGA prototyping, hardware bring-up, oscilloscope, logic analyzer, Linux/Unix environments

**Scripting & Tools:** Python, MATLAB, Git, Bash, AutoCAD, Jupyter, VSCode

**Areas of Interest:** ASIC/FPGA Design, RTL Verification, Physical Design, Memory Systems, Embedded Firmware