A)

11 seconds -> 10^6 instructions
1 second -> 10^6/11 = 90909.1 instructions

Each instruction takes 5 cycle in average
So
Work Frequency = 90909.1 * 5 = 454545.45 tick/s
= 0.45 MHz

B)

The bus transmits 64 bits per second, that is 8 bytes per second.
It runs at 300 MHz → 300 x 10^6 ticks/s

The bus transmits
8*300 * 10^6 = 2.4 x 10^9 bytes / s

Or 1 Mbyte is 1024 ^2 = 1048576 Byte

The bus transmits
2.4 x 10^9 / 1048576 = 2288.82 MBytes / s.

C)

It is pipelined so the Cycle will be the length of the longest stage:
550 ps

D)

It is not pipelined, the cycle will be the sum of all the stages :
300 + 400 + 300 + 550 + 100 = 1650 ps

E)

CPU runs at 2.5 GHz → number of clocks per second is :
2.5 * 10^9 ticks / s

F)

2 ns → 1 cycle
1 s → x cycles

X = 1/(2*^10^9) = 5 * 10^8 cycles.

G)

CPU runs at 2 GHz → 2 x 10^9 ticks/s
Executing an instruction takes 10 ticks on average

Number of instructions executed per second is :

2 x 10 ^9 / 10 = 2 x 10 ^8 instructions.

H)

4 stage-pipeline, each stage takes 2ns

// ins : instructions

In 8ns :	+ 8ns	+ 8ns
1 ins	2 ins	3 ins
3/4 ins	1+3/4 ins	2+3/4 ins
2/4 ins	1+2/4 ins	2+2/4 ins
1/4 ins	1+1/4 ins	2+1/4 ins

We can see the pattern
So the number of cycles in 1s is :

1s / 2 (ns/cycle) = 500 000 000 cycles

→ number of instructions in first line:

500 000 000 / 4 = 125 000 000 ins

So the number of instructions in total is :

125 000 000 + (125 000 000 -1) * 3 + 3/4 + 2/4 + 1/4
= 499999999.5 ins

So the pipelined CPU will have completed 499 999 999 instructions / s