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Title

R3: BOOST CONVERTER – SCHEMATIC AND PCB DESIGN

Course Name

EE-365 Power Electronics

Keywords

Boost Converter, Altium Designer, Schematic Design, PCB Design

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OVERVIEW

In the third part, the project course deals with the schematic and PCB design of the Boost converter according to the specifications assigned to your group. Furthermore, the selection of all the necessary components will be made and used to fill out the provided schematic and PCB layout template in Altium.

The list of available SMD capacitors, SMD resistors and THT trimmers that can be used for your design is provided in the Appendix section. The use of additional components not listed in the Appendix is allowed for some specific elements, but it needs to be properly motivated and authorized. See the Appendix section for further information.

To provide your answers and explanations, use the framed boxes below each question.
Follow the nomenclature given in this report to set the proper designators for the circuit components.
In case multiple units are employed to realize the same circuit component, append additional frame boxes in the answers, and add numbers to the corresponding designators (e.g., in case of multiple parallel input capacitors, denote them as $C_{in,1}$, $C_{in,2}$, ect...).

Populate the schematic diagram while proceeding from Q1 to Q19. Complete and review the schematic diagram in Q20 and finally proceed to the design of the PCB. Some hints are provided along the text to facilitate the design process.

As a first step, create the ALTIUM schematic diagram and start placing the MOSFET, the Schottky Diode, the input and output terminal connectors and the template model of the inductor.

CONTROLLER CONFIGURATION

For the converter control, the controller UC3843AN from Texas Instruments will be used. A diagram of the corresponding IC is given in Figure 1b. A more detailed block diagram of the selected controller can be found in the application note *UCx84xA Current-Mode PWM Controller datasheet (Rev. G)*.

This section is aimed at specifying the preliminary settings for the desired IC configuration.

ALTIUM Schematic Hints:
Place the UC3843AN controller in your ALTIUM schematic. Choose the DIP8 socket footprint.

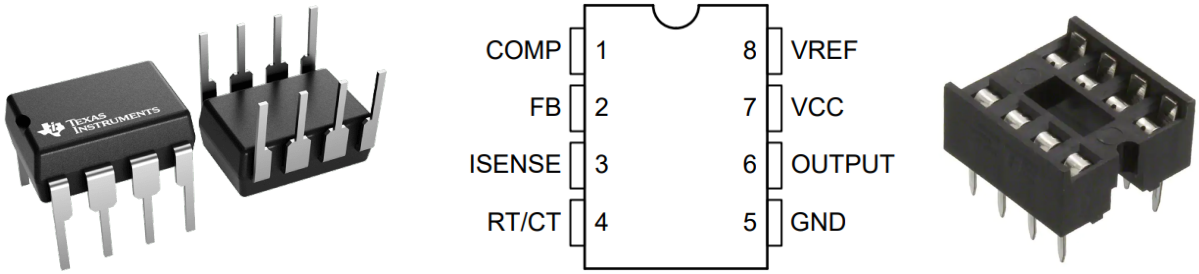

Figure 1 a) UC3843AN IC b) Pinout of UC3843AN IC c) DIP8 Socket

Q1: OSCILLATOR FREQUENCY SETTINGS

The working frequency of the IC is chosen with a timing resistor and a timing capacitor to be connected to the RT/CT pin of the IC. Using the graph provided in the application note *UCx84xA Current-Mode PWM Controller datasheet (Rev. G)* (Section 7.3.5), select a resistance R_T and a capacitance C_T needed to achieve the required switching frequency. Note that, for the UC3843AN IC, the switching frequency is equal to the oscillator frequency.

ALTIUM Schematic Hints:
Connect the timing resistor between the VREF and RT/CT pin, and the timing capacitor between the RT/CT and GND pin. Use the designators R_T and C_T. Consider adding a trimmer to allow for possible adjustments.

ALTIUM PCB Hints:
For best performances, keep the timing capacitor lead to the device GND as short and direct as possible.

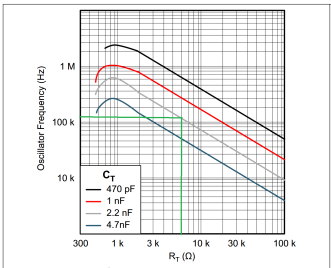

Figure 7-4. Oscillator Frequency vs Timing Resistance

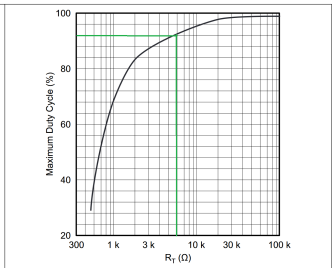

Figure 7-5. Maximum Duty Cycle vs Timing Resistance

It is recomended in the datasheets that we use a timing resistor of a velue that varies between 5kΩ and a 100kΩ. Therefore, to correspond to such a resistor with our switching frequency, we chose a timing capacitor of 2.2nF which gives us a timing resistor of around 6kΩ.
From the formula of the datasheet: $R_T = \frac{1.72}{C_T \cdot f_{sw}}$ we find that R_t is equal to 6.25kΩ.

R_T = 6.25 kΩ	Code: KIT-RMCF1206FT-04	Package: 1206/3216	
C_T = 2.2 nF	Code: C1206C222K5GEC7210	Package: 1206/3216	/ 5 pt.

Q2: REFERENCE VOLTAGE CAPACITOR

The pin VREF of the UC3843AN IC provides a stable 5 V reference for both the internal circuitry and the external components. A bypass capacitor is required to provide reference stability and to prevent noise problems with high-speed switching transients. Following the UC3843AN datasheet, select a proper ceramic capacitor.

ALTIUM Schematic Hints:
Connect the bypass capacitor between the VREF and GND pin. Use the designator C_{VREF}.

ALTIUM PCB Hints:
For best performances, use a short lead path.

Based on datasheet recommendation we chose 1 µF
Datasheet extract:
"This reference is also used for internal comparators and needs a high frequency bypass capacitor of 1 µF. "

C_{VREF} = 1 µF	Code: C1206C105K3RACTU	Package: 1206/3216	/ 2 pt.

AUXILIARY CIRCUIT FOR THE CONTROLLER

The UC3843AN IC gets power from the VCC pin. This power supply is provided by the output voltage of the boost converter. This section is aimed at the design of the supply circuit for this device.

Q3: AUXILIARY CAPACITOR

Considering the Turn-ON and Turn-OFF thresholds of the device, and the operating supply current that can be absorbed by the VCC pin (see the UC3843AN datasheet), compute the required capacitance C_{VCC} to guarantee the controller operation for at least 1 ms.

For this calculation, assume that the VCC current is the sum of a quiescent current contribution and an average output current related to the MOSFET gate control. The quiescent current is the maximum operating supply current given in the document *UCx84xA Current-Mode PWM Controller datasheet (Rev. G)* (Section 6.5). Knowing the switching frequency and the MOSFET gate charge (Qg), average output current can be calculated as $I_{OUT} = Q_g f_{SW}$. C_{VCC} should be large enough to hold VCC above the undervoltage lockout (UVLO) threshold.

Then, select a proper capacitor.

ALTIUM Schematic Hints:
Connect the capacitor between the VCC and GND pins. Use the designator C_{VCC}. To improve robustness against noise related problems, add also a ceramic bypass capacitor between VCC and GND, and use the designator $C_{VCC,bp}$.

$$
\begin{aligned}
I_q &\approx 0.017\,\text{A} \\
Q_g &\approx 1.7 \times 10^{-8}\,\text{C} \\
I_{avg} &= Q_g \cdot f_{sw} \\
&\approx 1.7 \times 10^{-8}\,\text{C} \cdot 125\,000\,\text{Hz} \\
&\approx 0.002\,125\,\text{A} \\
I_{tot} &= I_{avg} + I_q \\
&\approx 0.002\,125\,\text{A} + 0.017\,\text{A} \\
&\approx 0.019\,125\,\text{A} \\
I_{tot,safety} &\approx 0.025\,\text{A} \\
t &\approx 0.001\,\text{s} \\
Cvcc \cdot (V_{cc} - V_{min}) &= I_{tot,safety} \cdot t \\
C_{vcc} &= \frac{t \cdot I_{tot,safety}}{V_{cc} - V_{min}} \\
&\approx \frac{0.001\,\text{s} \cdot 0.025\,\text{A}}{15\,\text{V} - 7\,\text{V}} \\
&\approx 3.125 \times 10^{-6}\,\text{F} \\
C_{gate} &\approx 1 \times 10^{-9}\,\text{F} \\
C_{vcc,bp} &= C_{gate} \cdot 10 \\
&\approx 1 \times 10^{-9}\,\text{F} \cdot 10 \\
&\approx 1 \times 10^{-8}\,\text{F}
\end{aligned}
$$

Because of derating (–60 % due to bias voltage), we need a bigger capacity for C_{vcc} and the only capacitor that performs suffeciently under deriating has a nominal capacitance of 10 µF.
($C_{VCC,bp}$ has a derating of 1 %, which is within the acceptable limits.)
It will have a derated capacitance of 4 µF

C_{VCC} = 10µF	Code: C1206C106K4PACTU	Package: 1206/3216	
$C_{VCC,bp}$ = 10nF	Code: C1206S103J5RACAUTO	Package: 1206/3216	/ 6 pt.

Q4: AUXILIARY ZENER DIODE

Select a Zener diode to protect the IC power stage below the maximum supply voltage of the UC3843AN.

ALTIUM Schematic Hints:
Connect the Zener diode between VCC and GND. Respect the correct polarity. Use the designator Z_{VCC}.

Chose 15V in accordance to IC Vcc specifications.

$V_{Z_{vcc}}$ = 15V	Code: HPZR-C11-QX	Package: SOD-123W-2	/ 4 pt.

Q5: LIMITING RESISTOR

The input voltage of the auxiliary supply is equal to the output voltage of the boost converter. However, the voltage at the VCC pin is limited by the Zener diode chosen in Q4 and much lower than the output voltage. For this reason, a series resistance has to be added to the auxiliary supply circuit in a way to limit the current flowing into the Zener diode within the bounds given in its datasheet.

Considering the parameters and operational limits of the Zener diode chosen in Q4, select a proper limiting resistor R_{aux}. Then, compute its steady-state voltage drop and power losses during the normal functioning of the controller. To guarantee a safety margin, select a resistor package with a power rating at least 20% higher than the computed value of the power losses.

ALTIUM Schematic Hints:
Connect the limiting resistor between the Zener diode and the output of the boost converter. Use the designator R_{aux}.

$$
\begin{aligned}
V_{out} &= 48\,\text{V} \\
P_{zener} &= 1\,\text{W} \\
I_{max,zener} &= \frac{P_{zener}}{V_{cc}} \\
&\approx \frac{1\,\text{W}}{15\,\text{V}} \\
&\approx 0.066\,666\,7\,\text{A} \\
I_{zener,sec} &\approx 0.02\,\text{A} \\
R_{aux} &= \frac{V_{out} - V_{cc}}{I_{tot,safety} + I_{zener,sec}} \\
&\approx \frac{48\,\text{V} - 15\,\text{V}}{0.025\,\text{A} + 0.02\,\text{A}} \\
&\approx 733.333\,\Omega \\
V_{raux} &= R_{aux} \cdot \left(I_{zener,sec} + I_{tot,safety}\right) \\
&\approx 733.333\,\Omega \cdot (0.02\,\text{A} + 0.025\,\text{A}) \\
&\approx 33\,\text{V} \\
P_{raux} &= R_{aux} \cdot \left(I_{tot,safety} + I_{zener,sec}\right)^2 \\
&\approx 733.333\,\Omega \cdot (0.025\,\text{A} + 0.02\,\text{A})^2 \\
&\approx 1.485\,\text{W} \\
P_{raux,safety} &= P_{raux} \cdot 1.2 \\
&\approx 1.485\,\text{W} \cdot 1.2 \\
&\approx 1.782\,\text{W}
\end{aligned}
$$

For power considerations, we will choose 2 resistances in parallel:

$$
\begin{aligned}
R_{parallel,1} &\approx 3300\,\Omega \\
R_{parallel,2} &\approx 1000\,\Omega \\
R_{parallel} &= \frac{R_{parallel,1} \cdot R_{parallel,2}}{R_{parallel,1} + R_{parallel,2}} \\
&\approx \frac{3300\,\Omega \cdot 1000\,\Omega}{3300\,\Omega + 1000\,\Omega} \\
&\approx 767.442\,\Omega \\
P_{raux,parallel,max} &= \frac{\left(\left(I_{tot,safety} + I_{zener,sec}\right) \cdot R_{parallel}\right)^2}{R_{parallel,2}} \\
&\approx \frac{((0.025\,\text{A} + 0.02\,\text{A}) \cdot 767.442\,\Omega)^2}{1000\,\Omega} \\
&\approx 1.192\,66\,\text{W}
\end{aligned}
$$

R_{aux} = 1//3.3kΩ	Code: KIT-RMCF1206FT-04	Package: 2512/6332	
$\Delta V_{R_{aux}}$ = 33V	$P_{R_{aux}}$ = 2W		/ 5 pt.

GATE DRIVER

The PWM controller IC has an internal ground-referenced gate driver, which can be used to directly control the MOSFET through the OUTPUT pin. The peak current that can be absorbed or supplied at the OUTPUT pin is limited in the range ± 1 A. For additional information, refer to the application note *UCx84xA Current-Mode PWM Controller datasheet (Rev. G)* (Section 7.2).

This section is aimed at defining the parameters of the external gate driver circuitry.

Q6: CHOICE OF THE GATE RESISTOR

The gate resistor defines dynamics of the MOSFET switching. A smaller resistance value results in higher turn-ON and turn-OFF speed and into lower switching losses, but requires a higher peak current to operate.

Considering the typical internal gate resistance $R_{G,int}$ of the selected MOSFET (chosen in Part 1), compute the minimum value of the external gate resistance $R_{G,min}$ to be added to the circuit in order to limit the peak current of the OUTPUT pin to its feasible range (i.e., 1 A).

Then, select a resistor whose resistance value is higher than $R_{G,min}$. If required, you can add additional resistor and diode to generate different turn-ON and turn-OFF resistance.

ALTIUM Schematic Hints:
Connect the resistor between the OUTPUT pin and the Gate terminal of the chosen MOSFET. Use the designator R_G.

ALTIUM PCB Hints:
If possible, keep a short path for the gate driver output.

$$I_{G,max} = 1\ \text{A}$$
$$R_{G,ming} = \frac{v_c c}{I_{G,max}} = 15$$
$$R_{G,chosen} = 50\ \Omega$$

Because we operate at a relatively low frequency, we decided to have a lower gate current since the increase in switching losses are minor and in this way we are less likely to destroy the IC.

$R_{G,min} = 15\Omega$	$R_G = 50\Omega$	Code: KIT-RMCF1206FT-02	Package: 1206/3216	/ 4 pt.

Q7: POWER LOSSES OF THE GATE RESISTOR

Estimate the average turn-on and turn-off currents $I_{avg,ON}$ and $I_{avg,OFF}$ through the gate resistor, using the total gate charge Q_g available in the MOSFET data sheet. Thereby, approximate that all of Q_g is injected and extracted within time intervals $t_D(ON)+t_R$, and $t_D(OFF)+t_F$, which are also available in the data sheet.

Calculate the average power through the external gate resistor R_G, assuming pulses of average currents $I_{avg,ON}$ and $I_{avg,OFF}$ during the above mentioned time intervals. Verify that the resistor chosen in Q6 can tolerate this power dissipation. In case this requirement is not satisfied, choose a different resistor in Q6.

NB: Note that, for this approximate calculation, the currents $I_{avg,ON}$ and $I_{avg,OFF}$ may result to be higher than the previously imposed 1 A limit. This results in a more conservative margin for the power losses verification.

$$t_{d,on} \approx 2.45 \times 10^{-8}\,\text{s}$$
$$t_{d,off} \approx 3.2 \times 10^{-8}\,\text{s}$$
$$t_r \approx 3.35 \times 10^{-8}\,\text{s}$$
$$t_f \approx 1.4 \times 10^{-8}\,\text{s}$$
$$I_{on} = \frac{Q_g}{t_{d,on} + t_r} \approx \frac{1.7 \times 10^{-8}\,\text{C}}{2.45 \times 10^{-8}\,\text{s} + 3.35 \times 10^{-8}\,\text{s}} \approx 0.293\,103\,\text{A}$$
$$I_{off} = \frac{Q_g}{t_{d,off} + t_f} \approx \frac{1.7 \times 10^{-8}\,\text{C}}{3.2 \times 10^{-8}\,\text{s} + 1.4 \times 10^{-8}\,\text{s}} \approx 0.369\,565\,\text{A}$$
$$P_{rg} = R_{gate} \cdot f_{sw} \cdot \left(I_{on}^2 \cdot \left(t_r + t_{d,on}\right) + I_{off}^2 \cdot \left(t_r + t_{d,off}\right)\right)$$
$$\approx 50\,\Omega \cdot 125\,000\,\text{Hz} \cdot \left(0.293\,103\,\text{A}^2 \cdot \left(3.35 \times 10^{-8}\,\text{s} + 2.45 \times 10^{-8}\,\text{s}\right) + 0.369\,565\,\text{A}^2 \cdot 3.35 \times 10^{-8}\,\text{s} + 3.2 \times 10^{-8}\,\text{s}\right)$$
$$\approx 0.087\,054\,\text{W}$$

$I_{avg,ON}$ = 293mA	$I_{avg,OFF}$ = 367mA	P_{R_G} = 87 mW	/ 6 pt.

CURRENT MEASUREMENT

The UC3843AN circuit implements a peak-current control on the transistor current I_{sw}. In order to measure it, a current sensing network is used. The current sensing network is composed of a shunt resistor and of a low-pass RC filter. The output signal is provided to the ISENSE pin of the UC3843AN IC.

This section is aimed at designing the current measurement network.

Q8: CURRENT SENSING SHUNT RESISTOR

Calculate the shunt resistance for current measurements R_{CS}, such that the corresponding voltage under the maximum peak current of the MOSFET is less than 60% of the maximum ISENSE pin voltage (see the UC3843AN datasheet). Calculate the shunt resistor power losses in the worst-case operating conditions. Choose a resistor of adequate power rating.

ALTIUM Schematic Hints:
Connect the resistor between the Source terminal of the MOSFET and GND. Use the designator R_{CS}. Choose a resistor with a low tolerance (e.g., ≤ 1%) and a low dependence on the temperature.

ALTIUM PCB Hints:
If possible, use a short lead path.

$$
\begin{aligned}
V_{isense,max} &= 1\,\text{V} \\
I_{sw,max} &\approx 3.5\,\text{A} \\
R_{cs,max} &= \frac{0.6 \cdot V_{isense,max}}{I_{sw,max}} \\
&\approx \frac{0.6 \cdot 1\,\text{V}}{3.5\,\text{A}} \\
&\approx 0.171\,429\,\Omega \\
P_{R,cs} &= R_{cs} \cdot I_{sw,max}^2 \\
&\approx 0.15\,\Omega \cdot 3.5\,\text{A}^2 \\
&\approx 1.8375\,\text{W}
\end{aligned}
$$

R_{CS} = 150mΩ	$P_{R_{CS}}$ = 1.8W	Code:CSRN2512FKR150	Package: 2512/6332	/ 5 pt.

Q9: CURRENT MEASUREMENT FILTERING

Due to the switching behaviour of the converter, the measured current may include undesired spikes. For this reason, a low-pass filter is used. The filter should be fast enough to follow the dynamics of the input current (i.e., around f_{sw}), but low enough to neutralize the undesired spikes effects (i.e., at higher frequencies).

Choose a standard capacitance C_{CSF} and compute the corresponding resistance R_{CSF} in a way to obtain a 3dB cut-off frequency $f_{-3dB} = 25\,f_{sw}$.

Then, verify that the impedance of the RC filter at f_{sw} is sufficiently higher than R_{CS}, in order to not alter the power circuit.

Include in your answer Bode plot of the designed filter.

ALTIUM Schematic Hints:
Connect the filtering resistor between the sensing terminal of R_{CS} (i.e., connected to the Source terminal of the MOSFET) and the ISENSE pin of the UC3843AN IC. Connect the capacitor between the ISENSE pin and the GND pin of the UC3843AN IC. Use the designators R_{CSF} and C_{CSF}.

ALTIUM PCB Hints:
If possible, connect the filtering components far from the power path. Do not use a direct connection between the resistor and the MOSFET source, but rather connect it to the corresponding terminal of R_{CS}.

$$
\begin{aligned}
f_{cutoff} &= 25 \cdot f_{sw} \\
&\approx 25 \cdot 125\,000\,\text{Hz} \\
&\approx 3.125 \times 10^6\,\text{Hz} \\
R_f &\approx 5000\,\Omega \\
C_f &= \frac{1}{2 \cdot \pi \cdot f_{cutoff} \cdot R_f} \\
&\approx \frac{1}{2 \cdot 3.141\,59 \cdot 3.125 \times 10^6\,\text{Hz} \cdot 5000\,\Omega} \\
&\approx 1.018\,59 \times 10^{-11}\,\text{F} \\
C_f &\approx 10.1859\,\text{pF}
\end{aligned}
$$

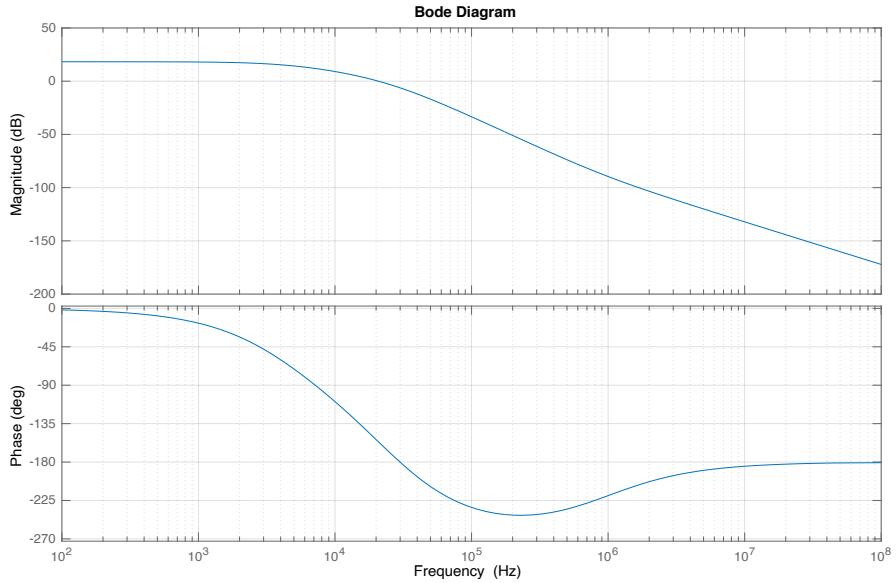

Figure 2 Bode diagram of the transfer function of the current sensing filter.

R_{CSF} = 5 kΩ	Code: KIT-RMCF1206FT-04	Package: 1206/3216
C_{CSF} = 10 pF	Code: C1206C100J1GAC	Package: 1206/3216

/ 6 pt.

SLOPE COMPENSATION

The peak current control has an inherent sub-harmonic oscillation phenomenon when the duty cycle exceeds 50%, which is documented in *Practical Feedback Loop Analysis for Current-Mode Boost Converter* (Section 2).

A common solution to this problem is adding a slope compensation on the reference current signal delivered at the COMP pin. Slope compensation is introduced by injecting a portion of the oscillator waveform to the actual sensed current. The two signals are summed together at the current sense input (CS) connection at the filter capacitor. This can be done by designing a RC ramp generator using the internal oscillator frequency available at the RT/CT pin of the UC3843AN controller. To minimize loading on the oscillator, the timing capacitor waveform is buffered with a small transistor whose collector is connected to the VREF pin. For additional information, refer to the application note *UCx84xA Current-Mode PWM Controller datasheet (Rev. G)* (Section 7.3.5).

Q10: SLOPE COMPENSATION DESIGN

Compute the optimal compensation slope S_e.

Hints:
For peak current mode control, any tendency toward sub-harmonic oscillation is damped within one switching cycle, by adding a compensating ramp equal to the down-slope of the inductor current at the maximum duty cycle. The compensation ramp should be scaled by the current-sense gain. For additional information, refer to the application note *Understanding and Applying Current-Mode Control Theory*.

$$
\begin{aligned}
S_n &= \frac{V_{in,min}}{L} \\
&\approx \frac{15.75\,\text{V}}{0.000\,23\,\text{H}} \\
&\approx 68\,478.3\,\text{A}\,\text{s}^{-1} \\
S_f &= \frac{V_{out} - V_{in,min}}{L} \\
&\approx \frac{48\,\text{V} - 15.75\,\text{V}}{0.000\,23\,\text{H}} \\
&\approx 140\,217\,\text{A}\,\text{s}^{-1} \\
S_{e,min} &= \frac{S_f - S_n}{2} \cdot R_{cs} \\
&\approx \frac{140\,217\,\text{A}\,\text{s}^{-1} - 68\,478.3\,\text{A}\,\text{s}^{-1}}{2} \cdot 0.15\,\Omega \\
&\approx 5380.43\,\text{V}\,\text{s}^{-1} \\
S_e &= 50\,000\,\text{V}\,\text{s}^{-1}
\end{aligned}
$$

We chose Se bigger to reduce peak oscillations.

$S_e =$ 50 000 A s^{-1}	/ 4 pt.

Q11: SLOPE COMPENSATION IMPLEMENTATION

Once the ideal value of the external ramp slope S_e has been computed, it needs to be generated. The RT/CT pin of UC3843AN provides a sawtooth wavefrom. The amplitude and frequency of this sawtooth waveform can be found in the datasheet, and the slope of this sawtooth waveform can be obtained accordingly.

The ramp generated at the ISENSE pin is scaled by the voltage divider R_{RAMP} and R_{CSF}.

Select the resistor R_{RAMP}.

ALTIUM Schematic Hints:
KSP2222ABU is selected as the NPN transistor to buffer the timing capacitor voltage. Connect the resistor between the Emitter terminal of the NPN transistor and ISENSE pin. Use the designator R_{RAMP}. Consider adding a trimmer to allow for possible adjustments. Choose an NPN transistor with a high bandwidth.

ALTIUM PCB Hints:
If possible, use a short lead path.

$$
\begin{aligned}
V_{rt,ct} &\approx 1.7\,\text{V} \\
S_{ic} &= V_{rt,ct} \cdot f_{sw} \cdot 2 \\
&\approx 1.7\,\text{V} \cdot 125\,000\,\text{Hz} \cdot 2 \\
&\approx 425\,000\,\text{V}\,\text{s}^{-1} \\
R_{ramp} &= R_{csf} \cdot \left(\frac{S_{ic}}{S_e} + 1 \right) \\
&\approx 5000\,\Omega \cdot \left(\frac{425\,000\,\text{V}\,\text{s}^{-1}}{50\,000\,\text{V}\,\text{s}^{-1}} + 1 \right) \\
&\approx 47\,500\,\Omega
\end{aligned}
$$

$R_{RAMP} =$ 47.5 kΩ	Code: KIT-RMCF1206FT-05	Package: 1206/3216	/ 6 pt.

COMPENSATION NETWORK DESIGN

The output voltage of the boost converter is measured through FB pin with a voltage divider. The closed-loop feedback control of the output voltage is achieved with a Type II compensation network.

Refer to the circuit scheme shown in *Practical Feedback Loop Analysis for Current-Mode Boost Converter* (Figure 8).

Premise:
For the design of the feedback compensation network, the boost converter can be modeled as a controllable dynamic system. In this framework, the voltage V_{COMP} (applied between the COMP and GND pins of the UC3843AN IC) is the control input signal, while the output voltage U_{out} is the output signal of the dynamic system. This means that this equivalent dynamic model intrinsically considers both the converter power operation and the Peak-Current Mode Control of the UC3843AN. All the other operating conditions (e.g., output power, input voltage) are treated as internal parameters of the dynamical system.

The design process is here divided in:
1. a preliminary identification of the current-controlled converter model, based on the operating conditions and on already selected components;
2. a design of an ideal Type II controller, based on the sole analysis of the transfer functions of the converter and of the controller;
3. a design of the Type II controller implementation, aimed at choosing the components of the real compensation network;
4. a verification of the overall system correct functioning, considering both the small-signal stability requirements and the large-signal operating ranges requirements.

To make the design and verification easier, the following auxiliary files are provided:
- the MATLAB script *Boost_Small_Signal_P1.m*, for the analysis of the current-controlled converter;
- the MATLAB script *Boost_Small_Signal_P2.m*, for the design of the ideal Type II controller transfer function;
- the PLECS model *Boost_PLECS.plecs*, for the time-domain simulation of the overall controlled system.

Q12: CONTROL-TO-OUTPUT TRANSFER FUNCTION

For a given steady-state operating point, the small-signal control-to-output transfer function can be identified in a way to link small perturbations of V_{COMP} to small perturbations of U_{OUT}.

According to the application note *Understanding and Applying Current-Mode Control Theory*, the small-signal control-to-output transfer function of a current-mode Boost converter is:

$$\tilde{H}(s) = G_0 \cdot \frac{\left(1 + \frac{s}{\omega_Z}\right) \cdot \left(1 - \frac{s}{\omega_R}\right)}{\left(1 + \frac{s}{\omega_P}\right) \cdot \left(1 + \frac{s}{Q_P \cdot \omega_n} + \frac{s^2}{\omega_n^2}\right)}$$

Referring to the application note *Understanding and Applying Current-Mode Control Theory*, compute the following quantities for the converter nominal operating point:
1. the static gain G_0;
2. the frequency $f_P = \omega_P/2\pi$ of the dominant pole;
3. the frequency $f_n = \omega_n/2\pi$ of the switching-related pole;
4. the frequency $f_Z = \omega_Z/2\pi$ of the output capacitor related zero;
5. the frequency $f_R = \omega_R/2\pi$ of the right half-plane zero.

Verify your results with the MATLAB script *Boost_Small_Signal_P1.m*.

Hints:
In the application note *Understanding and Applying Current-Mode Control Theory*, the output voltage of the error amplifier V_{COMP} is connected to the PWM comparator directly. However, according to the application note *UCx84xA Current-Mode PWM Controller datasheet (Rev. G)* (Figure 7-1), V_{COMP} is attenuated by an R/2R voltage divider in UC3843AN IC. This attenuation should be considered when calculating G_0.

$$
\begin{aligned}
A_{CS} &= \left(\frac{R}{R + 2 \cdot R}\right) \\
&\approx \left(\frac{1\,\Omega}{1\,\Omega + 2 \cdot 1\,\Omega}\right) \\
&\approx 0.333\,333 \\
S_n &= \frac{V_{in}}{L} \cdot R_{cs} \\
&\approx \frac{21\,\mathrm{V}}{0.000\,23\,\mathrm{H}} \cdot 0.15\,\Omega \\
&\approx 13\,695.7\,\mathrm{A\,s^{-1}} \\
Q_p &= \frac{\frac{1}{\pi} \cdot 1}{1 + \frac{S_e}{S_n} \cdot D_{off} - 0.5} \\
&\approx \frac{\frac{1}{3.141\,59} \cdot 1}{1 + \frac{50\,000\,\mathrm{V\,s^{-1}}}{13\,695.7\,\mathrm{A\,s^{-1}}} \cdot 0.4375 - 0.5} \\
&\approx 0.207\,406 \\
K_m &= \frac{1}{\frac{0.5 - D \cdot R_{cs}}{f_{sw} \cdot L} + \frac{S_e}{f_{sw} \cdot V_{out}}} \\
&\approx \frac{1}{\frac{0.5 - 0.5625 \cdot 0.15\,\Omega}{125\,000\,\mathrm{Hz} \cdot 0.000\,23\,\mathrm{H}} + \frac{50\,000\,\mathrm{V\,s^{-1}}}{125\,000\,\mathrm{Hz} \cdot 48\,\mathrm{V}}} \\
&\approx 124.887 \\
K_d &= 2 + \frac{R_{load} \cdot D_{off}^2}{R_{cs}} \cdot \frac{1}{K_m} + \frac{0.5 \cdot R_{cs} \cdot D}{f_{sw} \cdot L} \\
&\approx 2 + \frac{46.08\,\Omega \cdot 0.4375^2}{0.15\,\Omega} \cdot \frac{1}{124.887} + \frac{0.5 \cdot 0.15\,\Omega \cdot 0.5625}{125\,000\,\mathrm{Hz} \cdot 0.000\,23\,\mathrm{H}} \\
&\approx 2.557\,11
\end{aligned}
$$

$$G_0 = \frac{R_{load} \cdot D_{off}}{A_{CS} \cdot R_{cs} \cdot K_d}$$
$$\approx \frac{46.08\,\Omega \cdot 0.4375}{0.333\,333 \cdot 0.15\,\Omega \cdot 2.557\,11}$$
$$\approx 157.678$$

$$w_P = \frac{K_d}{R_{load} \cdot C_{out}}$$
$$\approx \frac{2.557\,11}{46.08\,\Omega \cdot 3.23 \times 10^{-6}\,\mathrm{F}}$$
$$\approx 17\,180.4\,\mathrm{rad\,s^{-1}}$$

$$w_n = 2 \cdot \pi \cdot \frac{f_{sw}}{2}$$
$$\approx 2 \cdot 3.141\,59 \cdot \frac{125\,000\,\mathrm{Hz}}{2}$$
$$\approx 392\,699\,\mathrm{rad\,s^{-1}}$$

$$w_Z = \frac{1}{R_{ESR} \cdot C_{out}}$$
$$\approx \frac{1}{15\,\Omega \cdot 3.23 \times 10^{-6}\,\mathrm{F}}$$
$$\approx 20\,639.8\,\mathrm{rad\,s^{-1}}$$

$$w_R = \frac{D_{off}^2 \cdot R_{load}}{L}$$
$$\approx \frac{0.4375^2 \cdot 46.08\,\Omega}{0.000\,23\,\mathrm{H}}$$
$$\approx 38\,347.8\,\mathrm{rad\,s^{-1}}$$

$$H_{open} = \frac{G_0 \cdot \left(1 + \frac{s}{w_R}\right) \cdot \left(1 - \frac{s}{w_Z}\right)}{\left(1 + \frac{s}{w_P}\right) \cdot \left(1 + \frac{s}{w_n \cdot Q_p} + \frac{s}{w_n}^2\right)}$$

$G_0 =$ 157.7	$f_P =$ 2.7 kHz	$f_n =$ 62.5 kHz
$f_Z =$ 3.3 kHz	$f_R =$ 6.1 kHz	

/ 6 pt.

Q13: CONTROL-TO-OUTPUT BODE DIAGRAM

Using the MATLAB Script *Boost_Small_Signal_P1.m*, draw the Bode diagram of the Control-to-Output transfer function $\tilde{H}(s)$ for multiple operating conditions of the Boost.

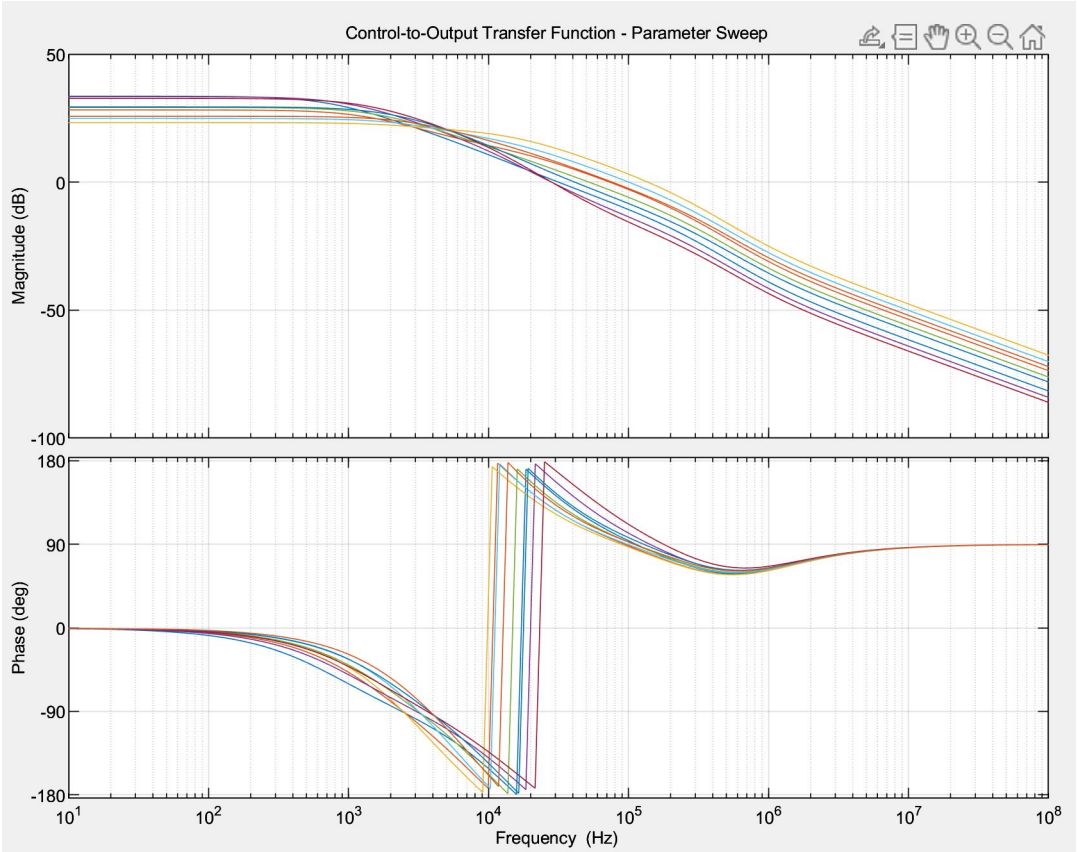

Figure 3 Bode diagram of the control-to-output transfer function in different operating conditions.

/ 3 pt.

Q14: TYPE II CONTROLLER TRANSFER FUNCTION DESIGN

To control the converter, a Type II compensation network is used.

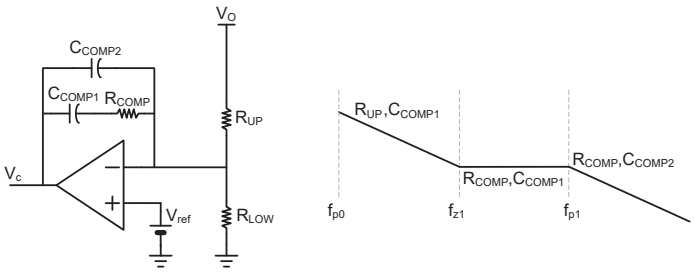

Figure 4 Type II Compensator with Gain Curve

The transfer function of an ideal Type II compensation network is:

$$\tilde{C}_{TypeII}(s) = G_{comp} \cdot \frac{1 + \frac{s}{2\pi f_{z,comp}}}{s(1 + \frac{s}{2\pi f_{p,comp}})}$$

The static gain, zero and pole of the compensation network are define by the components:

$$G_{comp} = \frac{1}{R_{UP} C_{COMP1}}$$

$$f_{z,comp} = \frac{1}{2\pi R_{COMP} C_{COMP1}}$$

$$f_{p,comp} = \frac{1}{2\pi R_{COMP} C_{COMP2}}$$

This transfer function must be designed to achieve a desired crossover frequency f_c and to guarantee the controller robustness. The integral action guarantees a zero steady-state error, while a zero and a pole should be carefully placed to compensate for the dynamical behavior of $\tilde{H}(s)$. In general, the higher the crossover frequency, the faster is the system to respond to input changes and to react to disturbances. However, too high crossover frequency may weaken the closed loop control robustness and lead to instability.

Considering the Control-to-Output transfer function $\tilde{H}(s)$ derived in Q12, and with the help of the application note *Practical Feedback Loop Analysis for Current-Mode Boost Converter* (Section 4), select:

1. the desired crossover frequency f_c;
2. the frequency $f_{z,comp}$ of the transfer function zero;
3. the frequency $f_{p,comp}$ of the transfer function pole;
4. the controller gain G_{comp} to achieve the desired crossover frequency.

Design Hints:

The crossover frequency should be less than about one-tenth the switching frequency and less than about one-fifth the right half-plane zero frequency f_R. Generally speaking, lower values can improve the stability of the system, but may weaken the dynamic performances during transients.

The compensation zero $f_{z,comp}$ is placed at one-fifth the selected crossover frequency f_c.

The compensation pole $f_{p,comp}$ is placed coincident with the output capacitor related zero f_Z or the right half-plane zero frequency f_R, which is lower.

The controller gain G_{comp} is determined by unity gain condition at the desired crossover frequency: $\left|\tilde{C}_{TypeII}(\omega_c)\right| \cdot \left|\tilde{H}(\omega_c)\right| = 1$

First estimation of parametrs:

$$\begin{aligned} f_c &= \frac{f_{sw}}{10} \\ &\approx \frac{125\,000\ \text{Hz}}{10} \\ &\approx 12\,500\ \text{Hz} \end{aligned}$$

$$\begin{aligned} f_{z,comp} &= \frac{f_c}{5} \\ &\approx \frac{12\,500\ \text{Hz}}{5} \\ &\approx 2500\ \text{Hz} \end{aligned}$$

$$\begin{aligned} f_{p,comp} &= f_{z,comp} \\ &\approx 2500\ \text{Hz} \\ &\approx 2500\ \text{Hz} \end{aligned}$$

Because the system is not stable with these values, we have chose to reduce the crossover frequency:

$$
\begin{aligned}
f_c &= 2000\,\text{Hz} \\
f_{z,comp} &= \frac{f_c}{5} \\
&\approx \frac{2000\,\text{Hz}}{5} \\
&\approx 400\,\text{Hz} \\
f_{p,comp} &= f_{z,comp} \\
&\approx 400\,\text{Hz} \\
&\approx 400\,\text{Hz} \\
H_{open}(s = 2\pi f_c) &= \frac{G_0 \cdot \left(1 + \frac{s}{w_Z}\right) \cdot \left(1 - \frac{s}{w_R}\right)}{\left(1 + \frac{s}{w_P}\right) \cdot \left(1 + \frac{s}{w_n} \cdot \frac{1}{Q_p} + \frac{s}{w_n}^2\right)} \\
&\approx \frac{157.678 \cdot \left(1 + \frac{12566.370614359172j}{6.191\,95 \times 10^6\,\text{rad s}^{-1}}\right) \cdot \left(1 - \frac{12566.370614359172j}{38\,347.8\,\text{rad s}^{-1}}\right)}{\left(1 + \frac{12566.370614359172j}{17\,180.4\,\text{rad s}^{-1}}\right) \cdot \left(1 + \frac{12566.370614359172j}{392\,699\,\text{rad s}^{-1}} \cdot \frac{1}{0.207\,406} + \frac{12566.370614359172j}{392\,699\,\text{rad s}^{-1}}^2\right)} \\
&\approx (60.170978596924186 - 118.04194852636614j) \\
C_{II}(s = 2\pi f_c) &= \frac{\left(1 + \frac{s}{2 \cdot \pi \cdot f_{z,comp}}\right)}{s} \cdot \frac{1}{\left(1 + \frac{s}{2 \cdot \pi \cdot f_{p,comp}}\right)} \\
&= \frac{1}{s} \\
&\approx -7.957747154594768e - 05j \\
G_{comp} &= \frac{1}{|H_{open}(s = 2\pi f_c)| \cdot |C_{II}(s = 2\pi f_c)|} \\
&\approx \frac{1}{|(60.170978596924186 - 118.04194852636614j)| \cdot |-7.957747154594768e - 05j|} \\
&\approx 94.8454
\end{aligned}
$$

$f_c =$ 2 kHz	$f_{z,comp} =$ 400 Hz	$f_{p,comp} =$ 400 Hz	$G_{comp} =$ 94.9	/ 8 pt.

Q15: IDEAL TYPE II CONTROLLER TRANSFER FUNCTION VERIFICATION

Using the MATLAB Script *Boost_Small_Signal_P2.m*, draw the Bode diagram of the Open-Loop System $\tilde{L}_{ideal}(s) = \tilde{H}(s) \cdot \tilde{C}_{TypeII}(s)$ and of the Closed-Loop System $\tilde{F}_{ideal}(s) = \tilde{L}_{ideal}(s)/(1 + \tilde{L}_{ideal}(s))$ in multiple operating conditions of the converter.

Verify that in the nominal operating point the crossover frequency f_c matches the desired crossover frequency chosen in Q14.

Verify that in all operating conditions the system is stable and that the phase margin of the transfer function is higher than 30°. In case this condition is not verified, repeat the procedure in Q14 (e.g., by choosing different values for f_c, f_z, f_p and G_{comp}).

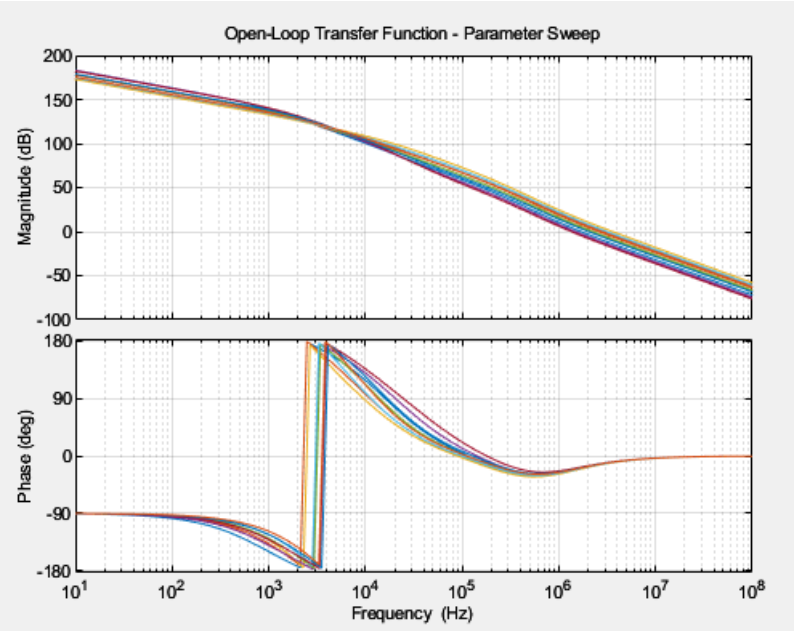

Figure 5 Bode diagram of the ideal open-loop transfer function in different operating conditions.

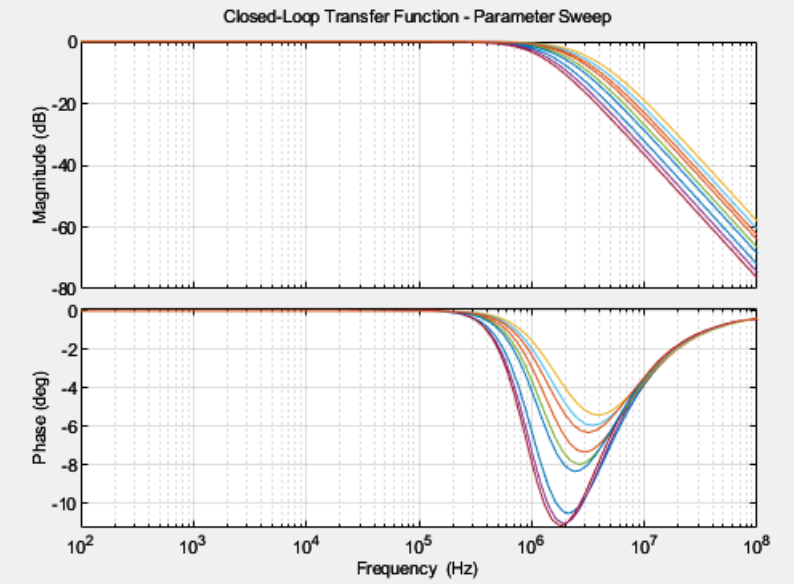

Figure 6 Bode diagram of the ideal closed-loop transfer function in different operating conditions.

/ 5 pt.

Q16: VOLTAGE FEEDBACK DIVIDER

Calculate voltage feedback divider resistors (R_{UP} and R_{LOW} in Figure 4) and the corresponding power losses. Feedback is compared to the internal 2.5 V reference, as can be seen in Figure 7-2 of the application note *UCx84xA Current-Mode PWM Controller datasheet (Rev. G)*.

For the rated voltage Vout, the voltage feedback should match the internal reference. Select the closest standard resistance values and with power ratings higher than calculated dissipations. Select a resistance high enough to keep the current through the divider in 1 mA range.

ALTIUM Schematic Hints:
Use the designators R_{UP} and R_{LOW}. Connect the R_{UP} resistor between the positive output terminal and the FB pin, and the R_{LOW} resistor between the FB pin and the output ground. To allow for some small adjustments in the real circuit, consider adding a trimmer in series to R_{LOW}.

Initial calculations for order of magnitude:
(estimate large Resistance (R_{up}) based on slightly higher target current.)

$$V_{ref} \approx 2.5\,\text{V}$$
$$I_{target} \approx 0.001\,\text{A}$$
$$R_{up} = \frac{V_{out}}{I_{target} \cdot 1.1} \approx \frac{48\,\text{V}}{0.001\,\text{A} \cdot 1.1} \approx 43\,636.4\,\Omega$$
$$R_{low} = \frac{R_{up}}{\left(\frac{V_{out}}{V_{ref}} - 1\right)} \approx \frac{43\,636.4\,\Omega}{\left(\frac{48\,\text{V}}{2.5\,\text{V}} - 1\right)} \approx 2397.6\,\Omega$$
$$I_{ref} = \frac{V_{out}}{R_{up} + R_{low}} \approx \frac{48\,\text{V}}{43\,636.4\,\Omega + 2397.6\,\Omega} \approx 0.001\,042\,71\,\text{A}$$

From these calculations we choose the following actual resistors:

$$R_{up} \approx 43\,700\,\Omega$$
$$R_{low} \approx 2400\,\Omega$$
$$I_{ref} = \frac{V_{out}}{R_{up} + R_{low}} \approx \frac{48\,\text{V}}{43\,700\,\Omega + 2400\,\Omega} \approx 0.001\,041\,21\,\text{A}$$
$$V_{ref} = I_{ref} \cdot R_{low} \approx 0.001\,041\,21\,\text{A} \cdot 2400\,\Omega \approx 2.498\,92\,\text{V}$$

R_{UP} = 43.7 kΩ	Code: KIT-RMCF1206FT-05	Package: 1206/3216		
R_{LOW} = 2.4 kΩ	Code: KIT-RMCF1206FT-04	Package: 1206/3216		/ 5 pt.

Q17: COMPENSATION NETWORK IMPLEMENTATION

Based on the calculation result of Q14 and Q16, calculate the values of the compensation resistor R_{COMP}, capacitor C_{COMP1} and C_{COMP2}.

ALTIUM Schematic Hints:
The compensation network, consisting of a parallel connection of C_{COMP2} and the series connection of R_{COMP} and C_{COMP1}, is connected between the pins COMP and FB.

$$
\begin{aligned}
C_{comp,1} &= \frac{1}{R_{up} \cdot G_{comp}} \\
&\approx \frac{1}{43\,700\,\Omega \cdot 94.8454} \\
&\approx 2.412\,69 \times 10^{-7}\ \mathrm{F} \\
R_{comp} &= \frac{1}{2 \cdot \pi \cdot f_{z,comp} \cdot C_{comp,1}} \\
&\approx \frac{1}{2 \cdot 3.141\,59 \cdot 400\,\mathrm{Hz} \cdot 2.412\,69 \times 10^{-7}\ \mathrm{F}} \\
&\approx 1649.14\,\Omega \\
C_{comp} &= \frac{1}{2 \cdot \pi \cdot f_{p,comp} \cdot R_{comp}} \\
&\approx \frac{1}{2 \cdot 3.141\,59 \cdot 400\,\mathrm{Hz} \cdot 1649.14\,\Omega} \\
&\approx 2.412\,69 \times 10^{-7}\ \mathrm{F}
\end{aligned}
$$

R_{COMP} =	16.5 kΩ	Code:	KIT-RMCF1206FT-04	Package:	1206/3216
C_{COMP1} =	0.22 µF	Code:	C1206C224K5RACTU	Package:	1206/3216
C_{COMP2} =	0.22 µF	Code:	C1206C224K5RACTU	Package:	1206/3216

/ 6 pt.

Q18: PLECS VERIFICATION

Using the PLECS model *Boost_PLECS.plecs*, verify the correct functioning of the designed compensation network in multiple operating conditions. Insert the picture of the Output Voltage Scope results.

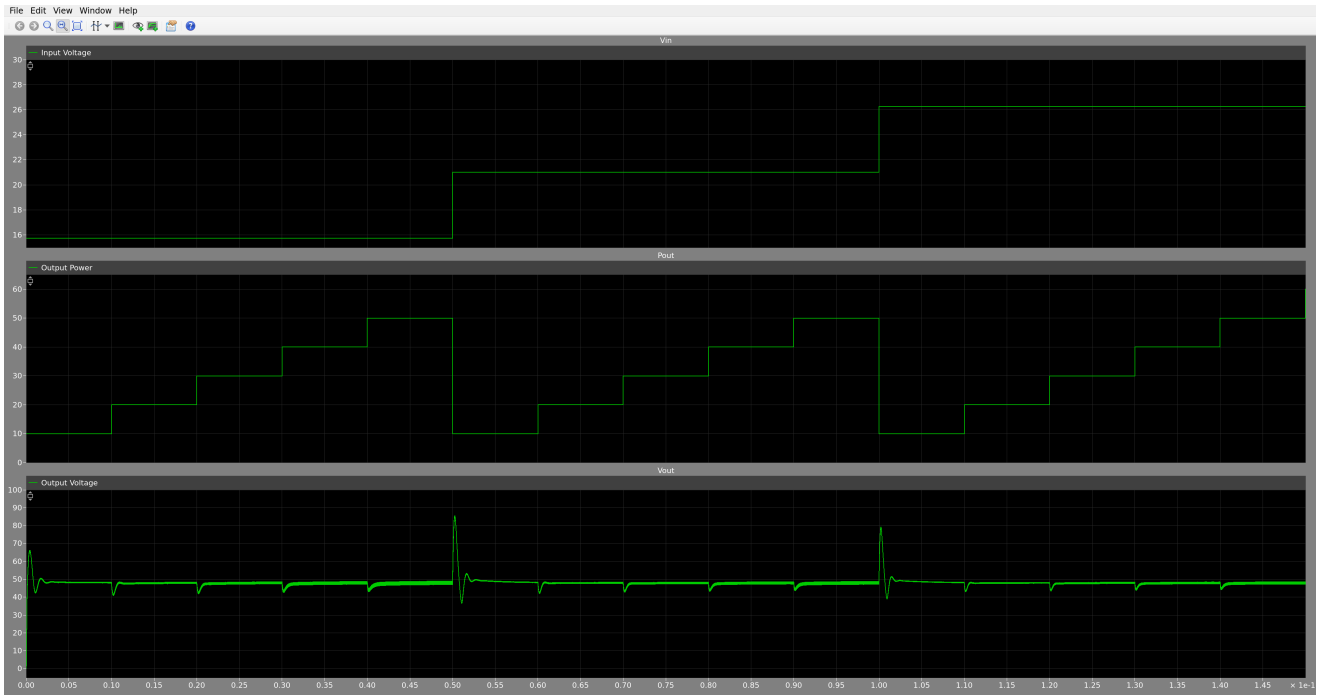

Figure 7 Simulation results obtained in PLECS.

Average output voltage of 47.97 V (target: 48 V)
Switching frequency of 123.6 kHz (target: 125 kHz)
Max simulated MOSFET voltage 85.5 V (Max rating 100 V)

Consequences: Reduce R_t and then fine-tune with variable series resistance (*VR*3 in Schematic)

NOTE: Mosfet voltage spikes to 97 V when removing load while operating at 50 W (aka, 100 % guarantee to destroy converter if load is removed under operation!!!)

/ 6 pt.

SCHEMATIC AND PCB

This section is aimed at the finalization of the ALTIUM schematic diagram and at the design of the Altium PCB.

Q19: DISCHARGE RESISTORS

Calculate the maximum resistances $R_{in,max}$ and $R_{out,max}$ that will discharge the selected input and output capacitor within 1 minute (from the initial voltage to less than 1%).

Then, select the resistances to use in the real circuit from standard available values. Furthermore, calculate power losses in the input and output resistors during normal operation (for the input discharge resistor consider the maximum voltage $U_{in,max}$). Select resistors with power ratings at least two times higher than the calculated loss values.

ALTIUM Schematic Hints:
Connect the discharge resistors in parallel to the input and output capacitors. Use the designators R_{in} and R_{out}.

$$t_{discharge} = 60\,\text{s} \tag{1}$$
$$C_{in} \approx 0.0066\,\text{F} \tag{2}$$
$$R_{in,max} = 0 - \frac{t_{discharge}}{C_{in} \cdot \ln 0.01} \tag{3}$$
$$\approx 0 - \frac{60\,\text{s}}{0.0066\,\text{F} \cdot \ln 0.01} \tag{4}$$
$$\approx 1974.07\,\Omega \tag{5}$$
$$R_{out,max} = 0 - \frac{t_{discharge}}{C_{out} \cdot \ln 0.01} \tag{6}$$
$$\approx 0 - \frac{60\,\text{s}}{3.23 \times 10^{-6}\,\text{F} \cdot \ln 0.01} \tag{7}$$
$$\approx 4.033\,69 \times 10^{6}\,\Omega \tag{8}$$
$$P_{rin} = \frac{V_{in}^2}{R_{in}} \tag{9}$$
$$\approx \frac{21\,\text{V}^2}{1780\,\Omega} \tag{10}$$
$$\approx 0.247\,753\,\text{W} \tag{11}$$
$$P_{rout} = \frac{V_{out}^2}{R_{out}} \tag{12}$$
$$\approx \frac{48\,\text{V}^2}{3.6 \times 10^{6}\,\Omega} \tag{13}$$
$$\approx 0.000\,64\,\text{W} \tag{14}$$

$R_{in,max}$ =< 1, 9kΩ	R_{in} = 1, 78kΩ	$P_{R,in}$ = 247mW	Code: KIT-RMCF1206FT-04	Package: 1206	
$R_{out,max}$ =< 4MΩ	R_{out} = 3, 6MΩ	$P_{R,out}$ = 623µW	Code: RMCF1206JT3M60	Package:1206	/ 6 pt.

Q20: SCHEMATIC LAYOUT

Follow the instructions given below to finalize the ALTIUM schematic diagram with the missing components.

- *Test Points*
  Test-Points will be used for measurement and debugging purposes. The provided Test-Point model has two connection terminals, which must be respectively connected to the desired signal and to the corresponding ground. Place Test-Points to measure the following signals:
  - the voltage on all the pins of the UC3843AN controller (COMP, FB, CS, VREF, VCC, GATE, RT/CT), referred to the Input GND;
  - the voltage on the current sensing resistor R_{CS}, referred to the Input GND;
  - the voltage on the MOSFET drain terminal, referred to the Input GND;
- *Heatsinks*
  Place the heatsinks for the MOSFET and for the Schottky Diode. Choose the correct footprint, coherently with the models chosen in Part 1. Leave their mounting connections terminals floating.

- *Decoupling Capacitors*
  To improve the design against noise, place decoupling capacitors around the most sensitive pins of the controller. Refer to the UC3843AN controller datasheet for info.

- *Mounting Holes*
  To provide mechanical stability to the circuit, place 4 mounting holes in your design, and leave them floating.

Once all the previous steps have been completed, validate the schematic in ALTIUM Designer. Include here the final schematic of your Boost converter design.

A dummy figure is given below, exchange it with the one you obtained in ALTIUM.
Delete this before writing anything.

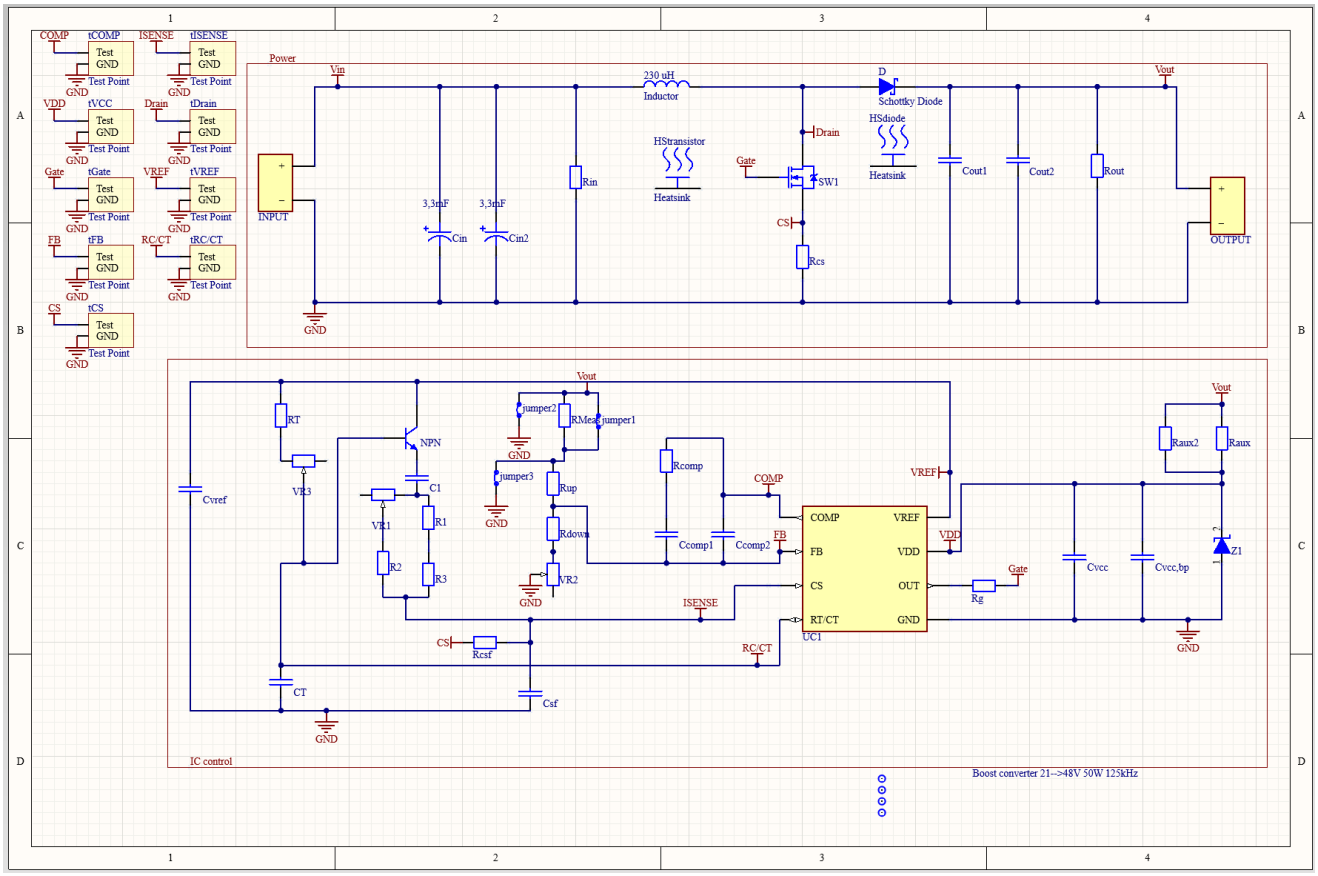

Figure 8 Schematic of the designed Boost converter.

/ 10 pt.

Q21: MINIMAL COPPER WIDTH FOR CURRENT-CARRYING TRACKS

Prior to routing your PCB, determine the minimal copper width needed for the current-carrying tracks. The copper thickness is fixed to 35 µm, whereas the current density is limited to 35 A/mm^2, to limit the copper temperature rise to roughly 10 °C. Based on these two

information and the rated current, calculate your current-carrying track width and proceed with it for power stage.

$$
\begin{aligned}
J_{max} &= 35\,\mathrm{A\,mm^{-2}} \\
I_{power} &\approx 3.5\,\mathrm{A} \\
t_{Cu} &\approx 0.035\,\mathrm{mm} \\
I_{aux} &\approx 0.05\,\mathrm{A} \\
W_{power} &= \frac{I_{power}}{t_{Cu} \cdot J_{max}} \\
&\approx \frac{3.5\,\mathrm{A}}{0.035\,\mathrm{mm} \cdot 35\,\mathrm{A\,mm^{-2}}} \\
&\approx 2.857\,14\,\mathrm{mm} \\
W_{aux} &= \frac{I_{aux}}{t_{Cu} \cdot J_{max}} \\
&\approx \frac{0.05\,\mathrm{A}}{0.035\,\mathrm{mm} \cdot 35\,\mathrm{A\,mm^{-2}}} \\
&\approx 0.040\,816\,3\,\mathrm{mm}
\end{aligned}
$$

We can see that for the auxilary power supply, we can use the standard signal trace width of 0.5 mm

$d_{Cu} = 2.9\mathrm{mm}$ / 2 pt.

Q22: BILL OF MATERIAL

With the help of the ALTIUM Report Manager, generate the bill of materials (BOM) needed to build your converter and include it below. This report-type document provides a list of all the required components for design realization.

In case your design requires the use of additional components not listed in the Appendix section, highlight them and be sure to provide the following information in tabular form:

- Manufacturer Part Number;
- Supplier Part Number (e.g., Digikey, Mouser, etc...);
- Supplier Link;
- Quantity (n.b., check that the needed quantity is available in stock, and that it is possible to order the exact amount needed);
- Unit Price (in CHF);
- Total Price (in CHF).

Refer, if possible, to a single supplier for all your additional required components. The Appendix provides some constraints for the additional components that can be allowed in your design.

Comment	Description	Designator	Footprint	LibRef	Quantity
Inductor	Inductor	230 uH	ETD29/16/10	Inductor	1
	Single Terminal Socket	B1, B2, B3, B4	Hole	Hole	4
Capacitor (SMD)	Capacitor (non polarized)	C1, Ccomp1, Ccomp2, Csf, CT, Cvcc, Cvcc,bp, Cvref	SM/1206	Capacitor (SMD)	8
3,3mF	Capacitor - Radial Packaging - Polarized	Cin, Cin2	radial_18mm	Capacitor (Radial - Polarized)	2
3,23 uF	Capacitor (non polarized)	Cout1, Cout2	SM/2220	Capacitor (SMD)	2
Schottky Diode	Schottky Diode	D	TO-220AC	Schottky Diode	1
Heatsink	HEATSINK TO-218,TO-220,TO-247	HSdiode, HStransistor	Heatsink FA-T220	Heatsink	2
2Pos 5.08mm	Connector 2 Pos 5.08mm Pitch1017503	INPUT, OUTPUT	Connector_2Pos_5.08mm	Power Connector	2
Jumper		jumper1, jumper2, jumper3	jumper	Jumper	3
NPN	NPN Bipolar Transistor	NPN	TO-92 Straight Lead	NPN	1
Resistor (SMD)	Resistor (Surface Mounted)	R1, R2, R3, Rcomp, Rcsf, Rdown, RMeas, Rout, RT, Rup	SM/1206	Resistor (SMD)	10
Resistor (SMD)	Resistor (Surface Mounted)	Raux, Raux2, Rcs	SM/2512	Resistor (SMD)	3
50 Ohm	Resistor (Surface Mounted)	Rg	SM/1206	Resistor (SMD)	1
10kohm	Resistor (Surface Mounted)	Rin	SM/1206	Resistor (SMD)	1
MOSFET	N-Channel Power MOSFET	SW1	TO-220AB	NMOS-2	1
Test Point		tCOMP, tCS, tDrain, tFB, tGate, tISENSE, tRC/CT, tVCC, tVREF	TESTPOINT HDR1X2	Test Point	9
UC3843AN	Texas Instruments UC3843AN PWM Controller	UC1	DIP8 Socket	UC3843AN	1
Variable Resistor	Variable Resistor	VR1, VR2, VR3	TRIMMER CT-6EP	Variable Resistor	3
D Zener	Zener Diode	Z1	DO-7	Zener	1

/ 5 pt.

Q23: PCB LAYOUT

Before manufacturing the PCB of the designed converter, it is necessary to check that the connections and component placings were done correctly. For this purpose, route your PCB, following the guidelines given below.

For this course, the PCB prototype is limited to **two layers**. It is not allowed to exceed the maximum size set by the provided template.

For best performances, partition the PCB by physically grouping components:

- Power circuitry (MOSFET, diodes, coupled inductor, input and output capacitors, input and output terminals, etc...);
- Control circuitry (UC3843AN controller, etc...).

Set a minimum insulation distance of 0.2 mm (8 mils) between the PCB traces.

Use a minimum width of 0.5 mm (20 mils) for the signal tracks. Respect the minimum width computed in Q21 for the power tracks. Consider using a primary-side GND plate and a secondary-side GND plate, and be sure to keep them isolated from one another.

Auto-routing is not allowed. Route in the following order:

- Power stage (MOSFET, diode, coupled inductor...) to have the minimum physical loop on the board, as this loop will be the source of interference.
- Auxiliary measurement and control circuits.

You can use vias to connect tracks on the two sides of the PCB. Avoid using vias in main current path, or use bigger vias, or vias in parallel to increase current carrying capability (in such a case, the inner diameter must be higher than vias used for signal paths).

Place the mounting holes in the opposite sides of the board, in a way to ensure a good mechanical stability.
Verify that the heatsinks are properly aligned to the MOSFET and Schottky Diode.

Annotate the PCB silkscreen with all the required information (e.g., connector polarities, components identifiers, etc...).

Run a design rule check in ALTIUM Designer, and correct all the errors.

Include below a 2D and 3D view of the top and bottom layers of your final PCB layout.

Dummy figures are given below, exchange them with the ones you obtained in ALTIUM.
Delete this before writing anything.

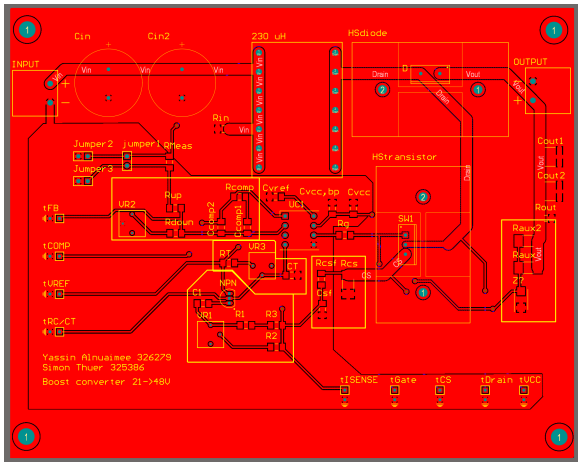

Figure 9 PCB top view in 2D mode.

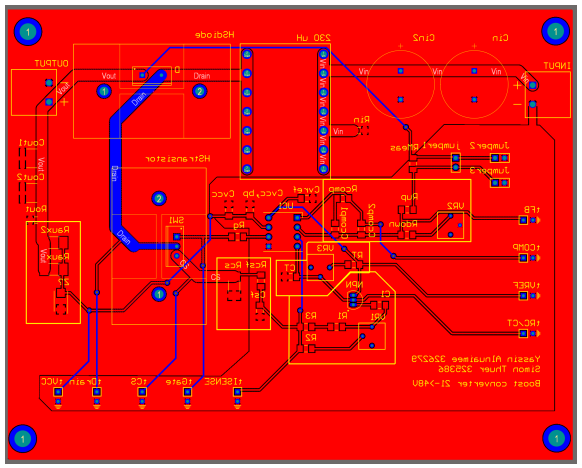

Figure 10 PCB bottom view in 2D mode.

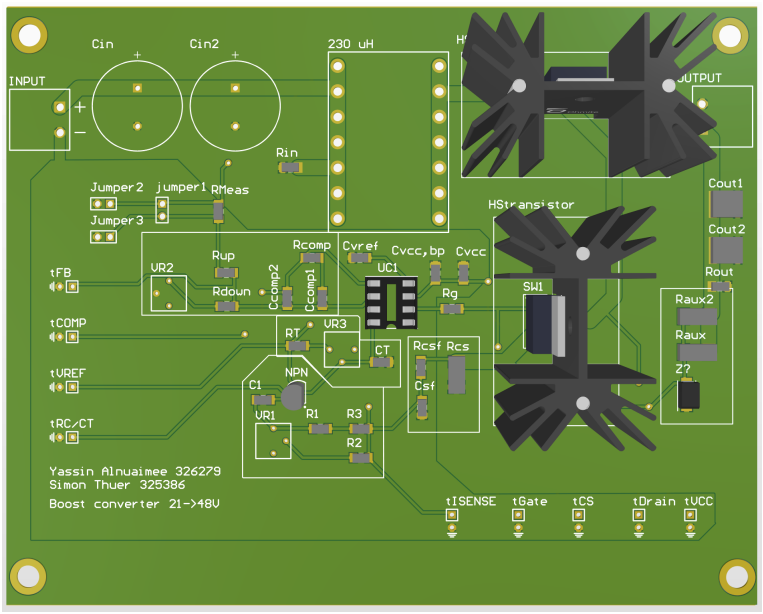

Figure 11 PCB top view in 3D mode.

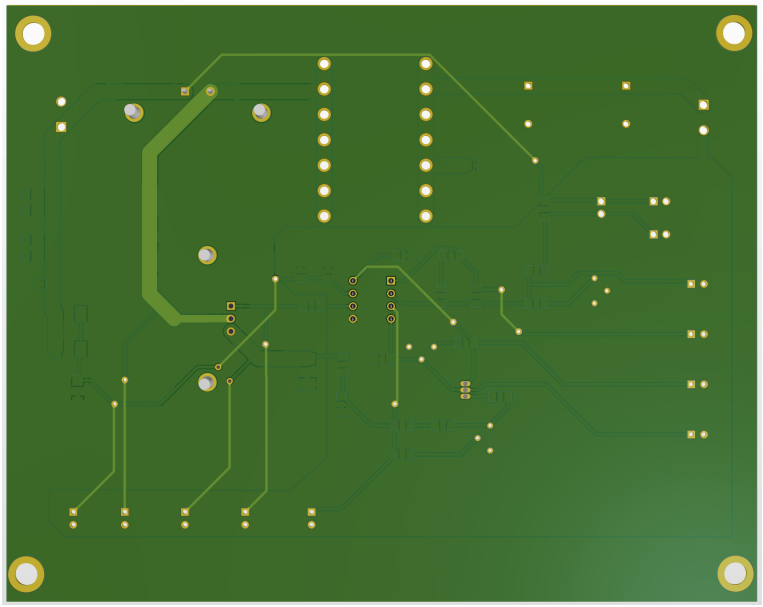

Figure 12 PCB bottom view in 3D mode.

/ 10 pt.

Total: / 125 pt.

LOSS TOOL FROM REPORT 1

This question is reported here due to the frequent non-convergence of the model used in the MATLAB Loss Tool during the fulfilment of Report 1. If you choose to not do it, the grade for the associated question in Report 1 (Q20) will remain unchanged, otherwise the grade of Report 1 will be updated.

Q24: LOSS TOOL

Considering the output of the provided loss tool in MATLAB, acquire losses for multiple values of U_{in} and P_{out}. Add an additional operating point at half of the rated power; i.e., $P_{out} = 25\,\text{W}$ (the loss tool has this operating point by default). From these results, identify the nominal operating point and compare it with your results; comment deviations in case they appear. Additionally, give a brief explanation for why there are more or less losses for different operating conditions. As input for the loss tool, data from the previous calculations has to be provided. Read the comments in the code carefully to obtain valid results.

We've already done it in report 1

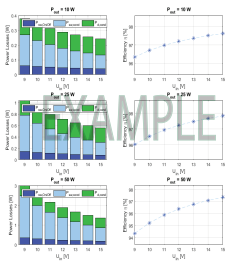

Figure 13 Semiconductor power losses and efficiencies achieved for different operating points.

/ 7 pt.

APPENDIX

This section contains the list of available components that can be used in your design, and some specification requirements for additional components.

LIST OF AVAILABLE SMD CAPACITORS

The list of available SMD Ceramic Capacitors is given in Table 2. Refer to these values for your design.
For information about the power ratings of different SMD ceramic capacitors, refer to Table 1.

Table 1 Power ratings of different SMD ceramic capacitors packages, empirically determined considering a temperature rise of 25 °C rise above the ambient temperature (Source: Johanson Dielectrics).

Package (Imperial/Metric)	1206/3216	1210/3225	1812/4532	2512/6332
Power Rating	80 mW	200 mW	400 mW	900 mW

Table 2 List of available SMD Ceramic Capacitors

Manufacturer	Part Number	Package (Imperial/Metric)	Capacitance		Tolerance (%)	Rated Voltage (V)
KEMET	C1206C100J2GACTU	1206/3216	10	pF	±5	200
KEMET	C1206C220F2GACTU	1206/3216	22	pF	±1	200
KEMET	C1206C330F2GACTU	1206/3216	33	pF	±1	200
KEMET	C1206C470F2GACTU	1206/3216	47	pF	±1	200
KEMET	C1206C101J1GACTU	1206/3216	100	pF	±5	100
KEMET	C1206C221J1GACTU	1206/3216	220	pF	±5	100
KEMET	C1206C471J1GACTU	1206/3216	470	pF	±5	100
KEMET	C1206C102J1GACTU	1206/3216	1000	pF	±5	100
KEMET	C1206C222K1GACTU	1206/3216	2200	pF	±10	100
KEMET	C1206C472K5GACTU	1206/3216	4700	pF	±10	50
KEMET	C1206C222K2RACTU	1206/3216	2200	pF	±10	200
KEMET	C1206C104K5RACTU	1206/3216	0.1	µF	±10	50
KEMET	C1206C154K5RACTU	1206/3216	0.15	µF	±10	50
KEMET	C1206C224K5RACTU	1206/3216	0.22	µF	±10	50
KEMET	C1206C334K5RACTU	1206/3216	0.33	µF	±10	50
KEMET	C1206C474K3RACTU	1206/3216	0.47	µF	±10	25
KEMET	C1206C105K3RACTU	1206/3216	1	µF	±10	25
KEMET	C1206C225K5RACTU	1206/3216	2.2	µF	±10	50
KEMET	C1206C106K4RACTU	1206/3216	10	µF	±10	16
KEMET	C1206C225K4PACTU	1206/3216	2.2	µF	±10	16
KEMET	C1206C335K3PACTU	1206/3216	3.3	µF	±10	25
KEMET	C1206C475K3PACTU	1206/3216	4.7	µF	±10	25
KEMET	C1206C106K4PACTU	1206/3216	10	µF	±10	16
KEMET	C1206C153K5RAC7800	1206/3216	15	nF	±10	50
KEMET	C1206S103J5RACAUTO	1206/3216	10	nF	±5	50
YAGEO	CC1206KRX7RYBB472	1206/3216	4.7	nF	±10	250
Samsung EM	CL31B102KDCNNNC	1206/3216	1.0	nF	±10	200
Würth El.	885342208003	1206/3216	10	nF	±10	250

Manufacturer	Part Number	Package (Imperial/Metric)	Capacitance		Tolerance (%)	Rated Voltage (V)
KEMET	C1206C100J1GAC	1206/3216	10	pF	±5	100
KEMET	C1206C120J5GACTU	1206/3216	12	pF	±5	50
KEMET	C1206C150J5GAC7800	1206/3216	15	pF	±5	50
KEMET	C1206C180J5GAC	1206/3216	18	pF	±5	50
KEMET	C1206C220J5GAC7800	1206/3216	22	pF	±5	50
KEMET	C1206C270J5GACTU	1206/3216	27	pF	±5	50
KEMET	C1206C330J5GAC7800	1206/3216	33	pF	±5	50
KEMET	C1206C390J5GACTU	1206/3216	39	pF	±5	50
KEMET	C1206C470J5GAC7800	1206/3216	47	pF	±5	50
KEMET	C1206C560J5GACTU	1206/3216	56	pF	±5	50
KEMET	C1206C680K5GACTU	1206/3216	68	pF	±10	50
KEMET	C1206C820J1GACTU	1206/3216	82	pF	±5	100
KEMET	C1206C101J1GAC7210	1206/3216	100	pF	±5	100
KEMET	C1206C121K5GACTU	1206/3216	120	pF	±10	50
KEMET	C1206C151J5GAC7800	1206/3216	150	pF	±5	50
KEMET	C1206C181J5GACTU	1206/3216	180	pF	±5	50
KEMET	C1206C221J5GACTU	1206/3216	220	pF	±5	50
KEMET	C1206C271K5GACTU	1206/3216	270	pF	±10	50
KEMET	C1206C331J5GAC7800	1206/3216	330	pF	±5	50
KEMET	C1206C391J5GACTU	1206/3216	390	pF	±5	50
KEMET	C1206C471J5GAC	1206/3216	470	pF	±5	50
KEMET	C1206C561J5GACTU	1206/3216	560	pF	±5	50
KEMET	C1206C681J5GACTU	1206/3216	680	pF	±5	50
KEMET	C1206C821J5GAC7800	1206/3216	820	pF	±5	50
KEMET	C1206C102J5GAC7800	1206/3216	1	nF	±5	50
KEMET	C1206C122J1GACTU	1206/3216	1.2	nF	±5	100
KEMET	C1206C152K5GACTU	1206/3216	1.5	nF	±10	50
KEMET	C1206C182J5GACTU	1206/3216	1.8	nF	±5	50
KEMET	C1206C222K5GEC7210	1206/3216	2.2	nF	±10	50
KEMET	C1206C272J5GACTU	1206/3216	2.7	nF	±5	50
KEMET	C1206C332J5GACTU	1206/3216	3.3	nF	±5	50
KEMET	C1206C392JAGACAUTO	1206/3216	3.9	nF	±5	250
KEMET	C1206C472J5GECTU	1206/3216	4.7	nF	±5	50
KEMET	C1206C562JCGACAUTO	1206/3216	5.6	nF	±5	500
KEMET	C1206C682JCGACAUTO	1206/3216	6.8	nF	±5	500
KEMET	C1206C822JBGACTU	1206/3216	8.2	nF	±5	630
KEMET	C1206S103J5RACAUTO	1206/3216	10	nF	±5	50
KEMET	C1206C123J5RACTU	1206/3216	12	nF	±5	50
KEMET	C1206C153J5RACTU	1206/3216	15	nF	±5	50
KEMET	C1206C183J5RACTU	1206/3216	18	nF	±5	50
KEMET	C1206C223J5RACAUTO	1206/3216	22	nF	±5	50
KEMET	C1206C273J5RACTU	1206/3216	27	nF	±5	50
KEMET	C1206C333J2RECTU	1206/3216	33	nF	±5	200
KEMET	C1206C393JARACTU	1206/3216	39	nF	±5	250
KEMET	C1206X473JARECTU	1206/3216	47	nF	±5	250
KEMET	C1206C473J1RECAUTO	1206/3216	47	nF	±5	100
KEMET	C1206C563K5RACTU	1206/3216	56	nF	±10	50
KEMET	C1206C683J1RECAUTO	1206/3216	68	nF	±5	100
KEMET	C1206C823J5RACTU	1206/3216	82	nF	±5	50

LIST OF AVAILABLE SMD RESISTORS

The SMD Resistors can be chosen from Table 3. This table includes both SMD resistor kits and individual resistor values.
For the resistance codes of the Stackpole Electronics Kits it is possible to refer to Fig.14.

Table 3 List of available SMD Resistors (Individual and Kits).

Manufacturer	Part Number	Package (Imperial/Metric)	Resistance Value(s) (Single or Kit)		Tolerance (%)	Rated Power (W)
Stackpole Electronics	KIT-RMCF1206FT-02	1206/3216	E96 values from 10 Ω to 97.6 Ω		±1	0.25
Stackpole Electronics	KIT-RMCF1206FT-03	1206/3216	E96 values from 100 Ω to 976 Ω		±1	0.25
Stackpole Electronics	KIT-RMCF1206FT-04	1206/3216	E96 values from 1 kΩ to 9.76 kΩ		±1	0.25
Stackpole Electronics	KIT-RMCF1206FT-05	1206/3216	E96 values from 10 kΩ to 97.6 kΩ		±1	0.25
Stackpole Electronics	RMCF1206FT10R0	1206/3216	10	Ω	±1	0.25
Vishay Dale	CRCW120620R0FKEA	1206/3216	20	Ω	±1	0.25
YAGEO	SR2512JK-7W1KL	2512/6332	1	kΩ	±5	2
YAGEO	SR2512FK-7W2KL	2512/6332	2	kΩ	±1	2
TE Connectivity	CRGP2512F3K3	2512/6332	3.3	kΩ	±1	2
TE Connectivity	CRGP2512F10K	2512/6332	10	kΩ	±1	2
Stackpole Electronics	CSM2512FT50L0	2512/6332	50	mΩ	±1	2
Stackpole Electronics	CSRN2512FKR100	2512/6332	100	mΩ	±1	2
Stackpole Electronics	CSRN2512FKR150	2512/6332	150	mΩ	±1	2
Stackpole Electronics	CSRN2512FKR200	2512/6332	200	mΩ	±1	2

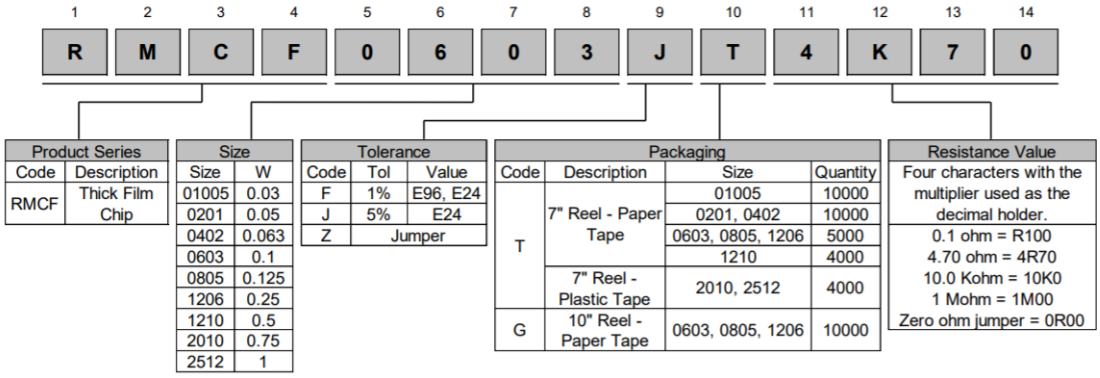

Figure 14 Resistor Code for Stackpole Electronics Kits.

LIST OF AVAILABLE TRIMMERS

The trimmers can be chosen from Table 4. They can be used in combination with the R_{RT} resistor and with the R_{FBU} resistor to allow for some small adjustments.

All trimmers are Through-hole and have the same footprint.
Be sure to connect the correct terminals when using the trimmers in your design.

Table 4 List of available trimmers.

Manufacturer	Part Number	Nominal Resistance	Tolerance (%)	Rated Power (W)
Nidec Copal Electronics	CT6EP102	1 kΩ	±10	0.5
Nidec Copal Electronics	CT6EP502	5 kΩ	±10	0.5

RULES FOR ADDITIONAL COMPONENTS

The use of additional components not listed in the appendix is allowed, but it needs to be properly motivated and authorized.

Only the following components can be authorized:

- Input and Output capacitors;
- Diodes (auxiliary circuit and Zener diodes);
- Auxiliary circuit Limiting Resistor;
- Gate Resistor.

Note also that:

- Additional **SMD** components are limited to the package **1206 or bigger**;
- All **diodes** are limited only to **through-hole** technology.

To this purpose, the group is asked to provide in Q22 the following information in tabular form:

- Manufacturer Part Number;
- Supplier Part Number (e.g., Digikey, Mouser, etc...);
- Supplier Link;
- Quantity (n.b., check that the needed quantity is available in stock, and that it is possible to order the exact amount needed);
- Unit Price (in CHF);
- Total Price (in CHF).

Refer, if possible, to a single supplier for all your additional required components.