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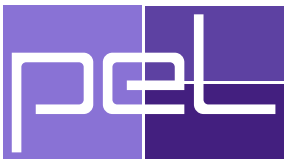	*Author(s) Name(s)* Yassin Alnuaimee 326279 Simon Thür 325386	*Function* BSc Student(s)
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Title

R4: BOOST CONVERTER - ASSEMBLING AND TESTING

Course Name

EE-365 Power Electronics

Keywords

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COMPENSATION NETWORK DESIGN

The output voltage of the boost converter is measured through FB pin with a voltage divider. The closed-loop feedback control of the output voltage is achieved with a Type II compensation network.

Refer to the circuit scheme shown in *Practical Feedback Loop Analysis for Current-Mode Boost Converter* (Figure 8).

Premise:
For the design of the feedback compensation network, the boost converter can be modeled as a controllable dynamic system. In this framework, the voltage V_{COMP} (applied between the COMP and GND pins of the UC3843AN IC) is the control input signal, while the output voltage U_{out} is the output signal of the dynamic system. This means that this equivalent dynamic model intrinsically considers both the converter power operation and the Peak-Current Mode Control of the UC3843AN. All the other operating conditions (e.g., output power, input voltage) are treated as internal parameters of the dynamical system.

The design process is here divided in:

1. a preliminary identification of the current-controlled converter model, based on the operating conditions and on already selected components;
2. a design of an ideal Type II controller, based on the sole analysis of the transfer functions of the converter and of the controller;
3. a design of the Type II controller implementation, aimed at choosing the components of the real compensation network;
4. a verification of the overall system correct functioning, considering both the small-signal stability requirements and the large-signal operating ranges requirements.

To make the design and verification easier, the following auxiliary files are provided:

- the MATLAB script *Boost_Small_Signal_P1.m*, for the analysis of the current-controlled converter;
- the MATLAB script *Boost_Small_Signal_P2.m*, for the design of the ideal Type II controller transfer function;
- the PLECS model *Boost_PLECS.plecs*, for the time-domain simulation of the overall controlled system.

Q1: CONTROL-TO-OUTPUT TRANSFER FUNCTION

For a given steady-state operating point, the small-signal control-to-output transfer function can be identified in a way to link small perturbations of V_{COMP} to small perturbations of U_{OUT}.

According to the application note *Understanding and Applying Current-Mode Control Theory*, the small-signal control-to-output transfer function of a current-mode Boost converter is:

$$\tilde{H}(s) = G_0 \cdot \frac{\left(1 + \frac{s}{\omega_Z}\right) \cdot \left(1 - \frac{s}{\omega_R}\right)}{\left(1 + \frac{s}{\omega_P}\right) \cdot \left(1 + \frac{s}{Q_P \cdot \omega_n} + \frac{s^2}{\omega_n^2}\right)}$$

Referring to the application note *Understanding and Applying Current-Mode Control Theory*, compute the following quantities for the converter nominal operating point:

1. the static gain G_0;
2. the frequency $f_P = \omega_P/2\pi$ of the dominant pole;
3. the frequency $f_n = \omega_n/2\pi$ of the switching-related pole;
4. the frequency $f_Z = \omega_Z/2\pi$ of the output capacitor related zero;
5. the frequency $f_R = \omega_R/2\pi$ of the right half-plane zero.

Verify your results with the MATLAB script *Boost_Small_Signal_P1.m*.

Hints:
In the application note *Understanding and Applying Current-Mode Control Theory*, the output voltage of the error amplifier V_{COMP} is connected to the PWM comparator directly. However, according to the application note *UCx84xA Current-Mode PWM Controller datasheet (Rev. G)* (Figure 7-1), V_{COMP} is attenuated by an R/2R voltage divider in UC3843AN IC. This attenuation should be considered when calculating G_0.

$$
\begin{aligned}
A_{CS} &= \left(\frac{R}{R + 2 \cdot R}\right) \\
&\approx \left(\frac{1\,\Omega}{1\,\Omega + 2 \cdot 1\,\Omega}\right) \\
&\approx 0.333\,333 \\
S_n &= \frac{V_{in}}{L} \cdot R_{cs} \\
&\approx \frac{21\,\mathrm{V}}{0.000\,23\,\mathrm{H}} \cdot 0.15\,\Omega \\
&\approx 13\,695.7\,\mathrm{A\,s^{-1}} \\
Q_p &= \frac{\frac{1}{\pi} \cdot 1}{1 + \frac{S_e}{S_n} \cdot D_{off} - 0.5} \\
&\approx \frac{\frac{1}{3.141\,59} \cdot 1}{1 + \frac{50\,000\,\mathrm{V\,s^{-1}}}{13\,695.7\,\mathrm{A\,s^{-1}}} \cdot 0.4375 - 0.5} \\
&\approx 0.207\,406 \\
K_m &= \frac{1}{\frac{0.5 - D \cdot R_{cs}}{f_{sw} \cdot L} + \frac{S_e}{f_{sw} \cdot V_{out}}} \\
&\approx \frac{1}{\frac{0.5 - 0.5625 \cdot 0.15\,\Omega}{125\,000\,\mathrm{Hz} \cdot 0.000\,23\,\mathrm{H}} + \frac{50\,000\,\mathrm{V\,s^{-1}}}{125\,000\,\mathrm{Hz} \cdot 48\,\mathrm{V}}} \\
&\approx 124.887 \\
K_d &= 2 + \frac{R_{load} \cdot D_{off}^2}{R_{cs}} \cdot \frac{1}{K_m} + \frac{0.5 \cdot R_{cs} \cdot D}{f_{sw} \cdot L} \\
&\approx 2 + \frac{46.08\,\Omega \cdot 0.4375^2}{0.15\,\Omega} \cdot \frac{1}{124.887} + \frac{0.5 \cdot 0.15\,\Omega \cdot 0.5625}{125\,000\,\mathrm{Hz} \cdot 0.000\,23\,\mathrm{H}} \\
&\approx 2.557\,11
\end{aligned}
$$

$$G_0 = \frac{R_{load} \cdot D_{off}}{A_{CS} \cdot R_{cs} \cdot K_d}$$
$$\approx \frac{46.08\,\Omega \cdot 0.4375}{0.333\,333 \cdot 0.15\,\Omega \cdot 2.557\,11}$$
$$\approx 157.678$$

$$w_P = \frac{K_d}{R_{load} \cdot C_{out}}$$
$$\approx \frac{2.557\,11}{46.08\,\Omega \cdot 3.23 \times 10^{-6}\,\mathrm{F}}$$
$$\approx 17\,180.4\,\mathrm{rad\,s^{-1}}$$

$$w_n = 2 \cdot \pi \cdot \frac{f_{sw}}{2}$$
$$\approx 2 \cdot 3.141\,59 \cdot \frac{125\,000\,\mathrm{Hz}}{2}$$
$$\approx 392\,699\,\mathrm{rad\,s^{-1}}$$

$$w_Z = \frac{1}{R_{ESR} \cdot C_{out}}$$
$$\approx \frac{1}{15\,\Omega \cdot 3.23 \times 10^{-6}\,\mathrm{F}}$$
$$\approx 20\,639.8\,\mathrm{rad\,s^{-1}}$$

$$w_R = \frac{D_{off}^2 \cdot R_{load}}{L}$$
$$\approx \frac{0.4375^2 \cdot 46.08\,\Omega}{0.000\,23\,\mathrm{H}}$$
$$\approx 38\,347.8\,\mathrm{rad\,s^{-1}}$$

$$H_{open} = \frac{G_0 \cdot \left(1 + \frac{s}{w_R}\right) \cdot \left(1 - \frac{s}{w_Z}\right)}{\left(1 + \frac{s}{w_P}\right) \cdot \left(1 + \frac{s}{w_n \cdot Q_p} + \frac{s}{w_n}^2\right)}$$

$G_0 =$ 157.7	$f_P =$ 2.7 kHz	$f_n =$ 62.5 kHz
$f_Z =$ 3.3 kHz	$f_R =$ 6.1 kHz	

/ 6 pt.

Q2: CONTROL-TO-OUTPUT BODE DIAGRAM

Using the MATLAB Script *Boost_Small_Signal_P1.m*, draw the Bode diagram of the Control-to-Output transfer function $\tilde{H}(s)$ for multiple operating conditions of the Boost.

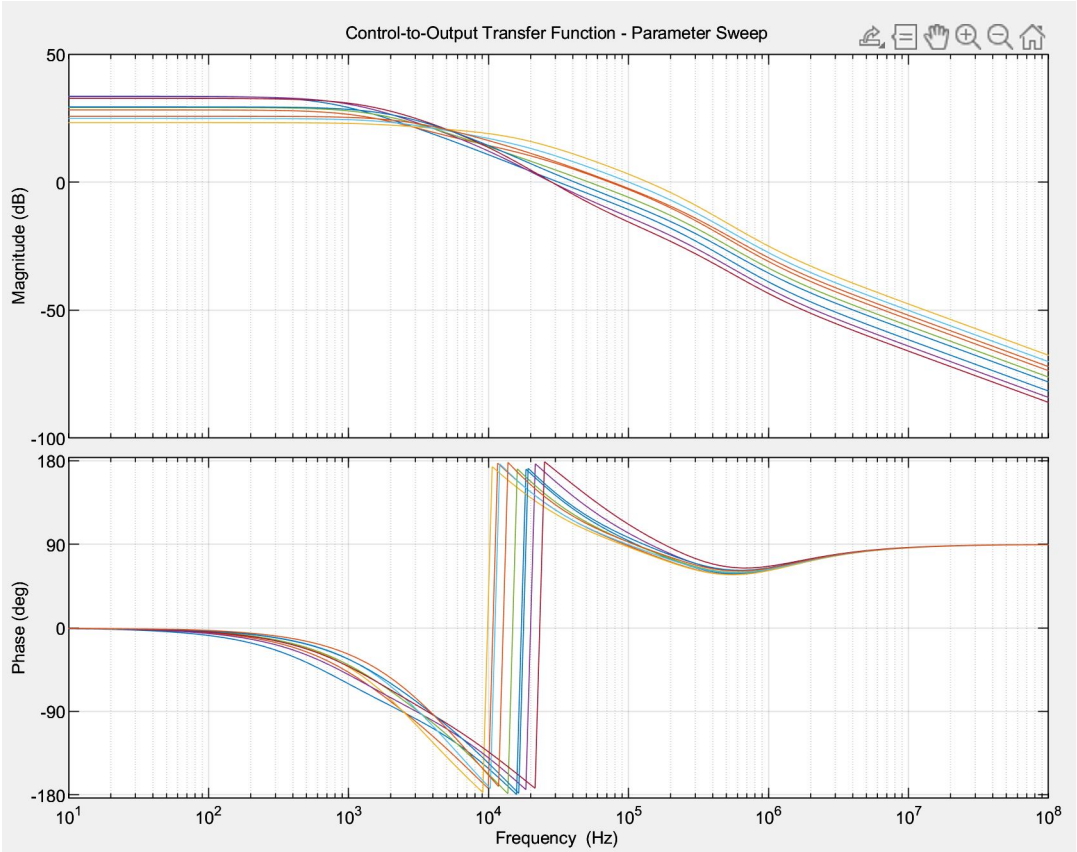

Figure 1 Bode diagram of the control-to-output transfer function in different operating conditions.

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Q3: TYPE II CONTROLLER TRANSFER FUNCTION DESIGN

To control the converter, a Type II compensation network is used.

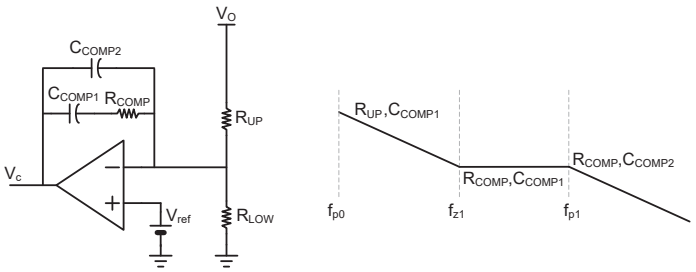


Figure 2 Type II Compensator with Gain Curve

The transfer function of an ideal Type II compensation network is:

$$\tilde{C}_{TypeII}(s) = G_{comp} \cdot \frac{1 + \frac{s}{2\pi f_{z,comp}}}{s(1 + \frac{s}{2\pi f_{p,comp}})}$$

The static gain, zero and pole of the compensation network are define by the components:

$$G_{comp} = \frac{1}{R_{UP} C_{COMP1}}$$

$$f_{z,comp} = \frac{1}{2\pi R_{COMP} C_{COMP1}}$$

$$f_{p,comp} = \frac{1}{2\pi R_{COMP} C_{COMP2}}$$

This transfer function must be designed to achieve a desired crossover frequency f_c and to guarantee the controller robustness. The integral action guarantees a zero steady-state error, while a zero and a pole should be carefully placed to compensate for the dynamical behavior of $\tilde{H}(s)$. In general, the higher the crossover frequency, the faster is the system to respond to input changes and to react to disturbances. However, too high crossover frequency may weaken the closed loop control robustness and lead to instability.

Considering the Control-to-Output transfer function $\tilde{H}(s)$ derived in Q1, and with the help of the application note *Practical Feedback Loop Analysis for Current-Mode Boost Converter* (Section 4), select:

1. the desired crossover frequency f_c;
2. the frequency $f_{z,comp}$ of the transfer function zero;
3. the frequency $f_{p,comp}$ of the transfer function pole;
4. the controller gain G_{comp} to achieve the desired crossover frequency.

Design Hints:

The crossover frequency should be less than about one-tenth the switching frequency and less than about one-fifth the right half-plane zero frequency f_R. Generally speaking, lower values can improve the stability of the system, but may weaken the dynamic performances during transients.

The compensation zero $f_{z,comp}$ is placed at one-fifth the selected crossover frequency f_c.

The compensation pole $f_{p,comp}$ is placed coincident with the output capacitor related zero f_Z or the right half-plane zero frequency f_R, which is lower.

The controller gain G_{comp} is determined by unity gain condition at the desired crossover frequency: $\left|\tilde{C}_{TypeII}(\omega_c)\right| \cdot \left|\tilde{H}(\omega_c)\right| = 1$

First estimation of parametrs:

$$\begin{aligned} f_c &= \frac{f_{sw}}{10} \\ &\approx \frac{125\,000\ \text{Hz}}{10} \\ &\approx 12\,500\ \text{Hz} \end{aligned}$$

$$\begin{aligned} f_{z,comp} &= \frac{f_c}{5} \\ &\approx \frac{12\,500\ \text{Hz}}{5} \\ &\approx 2500\ \text{Hz} \end{aligned}$$

$$\begin{aligned} f_{p,comp} &= f_{z,comp} \\ &\approx 2500\ \text{Hz} \\ &\approx 2500\ \text{Hz} \end{aligned}$$

Because the system is not stable with these values, we have chose to reduce the crossover frequency:

$$
\begin{aligned}
f_c &= 2000\,\text{Hz} \\
f_{z,comp} &= \frac{f_c}{5} \\
&\approx \frac{2000\,\text{Hz}}{5} \\
&\approx 400\,\text{Hz} \\
f_{p,comp} &= f_{z,comp} \\
&\approx 400\,\text{Hz} \\
&\approx 400\,\text{Hz} \\
H_{open}(s = 2\pi f_c) &= \frac{G_0 \cdot \left(1 + \frac{s}{w_Z}\right) \cdot \left(1 - \frac{s}{w_R}\right)}{\left(1 + \frac{s}{w_P}\right) \cdot \left(1 + \frac{s}{w_n} \cdot \frac{1}{Q_p} + \frac{s}{w_n}^2\right)} \\
&\approx \frac{157.678 \cdot \left(1 + \frac{12566.370614359172j}{6.191\,95 \times 10^6\,\text{rad s}^{-1}}\right) \cdot \left(1 - \frac{12566.370614359172j}{38\,347.8\,\text{rad s}^{-1}}\right)}{\left(1 + \frac{12566.370614359172j}{17\,180.4\,\text{rad s}^{-1}}\right) \cdot \left(1 + \frac{12566.370614359172j}{392\,699\,\text{rad s}^{-1}} \cdot \frac{1}{0.207\,406} + \frac{12566.370614359172j}{392\,699\,\text{rad s}^{-1}}^2\right)} \\
&\approx (60.170978596924186 - 118.04194852636614j) \\
C_{II}(s = 2\pi f_c) &= \frac{\left(1 + \frac{s}{2 \cdot \pi \cdot f_{z,comp}}\right)}{s} \cdot \frac{1}{\left(1 + \frac{s}{2 \cdot \pi \cdot f_{p,comp}}\right)} \\
&= \frac{1}{s} \\
&\approx -7.957747154594768e - 05j \\
G_{comp} &= \frac{1}{|H_{open}(s = 2\pi f_c)| \cdot |C_{II}(s = 2\pi f_c)|} \\
&\approx \frac{1}{|(60.170978596924186 - 118.04194852636614j)| \cdot |-7.957747154594768e - 05j|} \\
&\approx 94.8454
\end{aligned}
$$

$f_c =$ 2 kHz	$f_{z,comp} =$ 400 Hz	$f_{p,comp} =$ 400 Hz	$G_{comp} =$ 94.9	/ 8 pt.

Q4: IDEAL TYPE II CONTROLLER TRANSFER FUNCTION VERIFICATION

Using the MATLAB Script *Boost_Small_Signal_P2.m*, draw the Bode diagram of the Open-Loop System $\tilde{L}_{ideal}(s) = \tilde{H}(s) \cdot \tilde{C}_{TypeII}(s)$ and of the Closed-Loop System $\tilde{F}_{ideal}(s) = \tilde{L}_{ideal}(s)/(1 + \tilde{L}_{ideal}(s))$ in multiple operating conditions of the converter.

Verify that in the nominal operating point the crossover frequency f_c matches the desired crossover frequency chosen in Q3.

Verify that in all operating conditions the system is stable and that the phase margin of the transfer function is higher than 30°. In case this condition is not verified, repeat the procedure in Q3 (e.g., by choosing different values for f_c, f_z, f_p and G_{comp}).

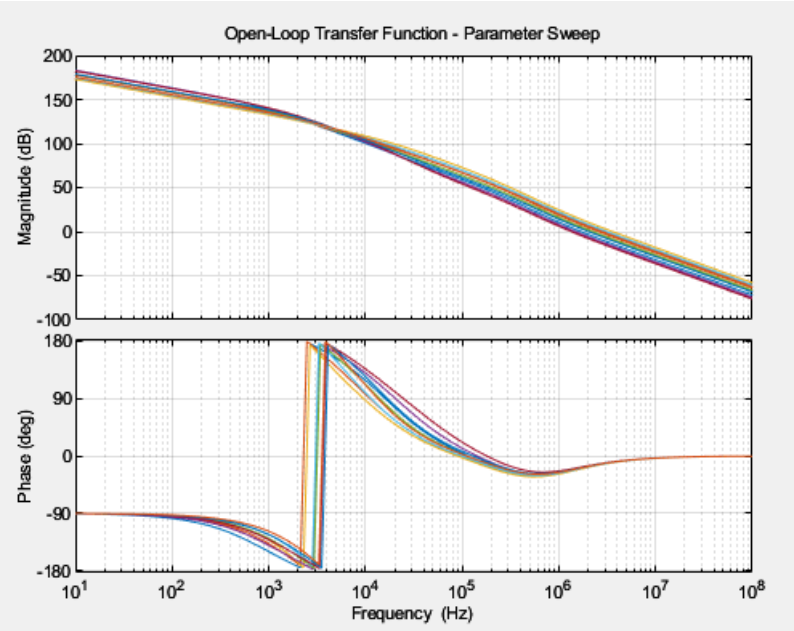


Figure 3 Bode diagram of the ideal open-loop transfer function in different operating conditions.

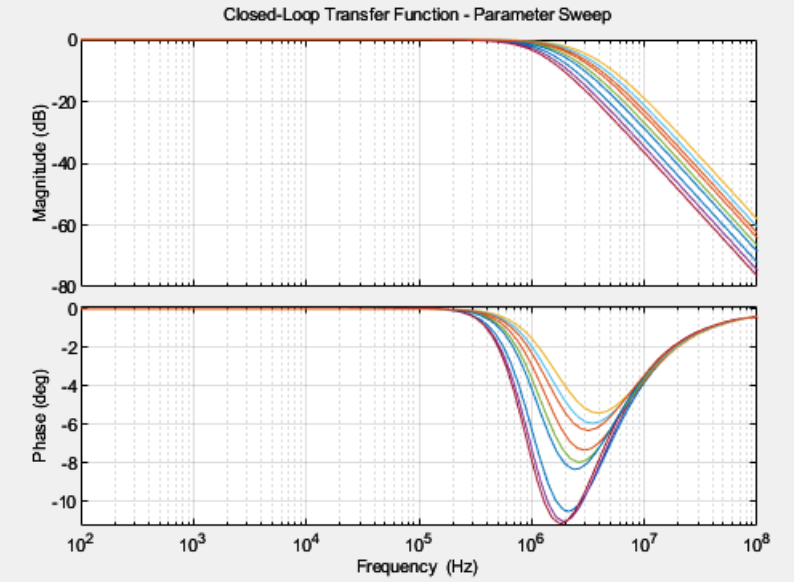


Figure 4 Bode diagram of the ideal closed-loop transfer function in different operating conditions.

/ 5 pt.

Q5: VOLTAGE FEEDBACK DIVIDER

Calculate voltage feedback divider resistors (R_{UP} and R_{LOW} in Figure 2) and the corresponding power losses. Feedback is compared to the internal 2.5 V reference, as can be seen in Figure 7-2 of the application note *UCx84xA Current-Mode PWM Controller datasheet (Rev. G)*.

For the rated voltage Vout, the voltage feedback should match the internal reference. Select the closest standard resistance values and with power ratings higher than calculated dissipations. Select a resistance high enough to keep the current through the divider in 1 mA range.

ALTIUM Schematic Hints:
Use the designators R_{UP} and R_{LOW}. Connect the R_{UP} resistor between the positive output terminal and the FB pin, and the R_{LOW} resistor between the FB pin and the output ground. To allow for some small adjustments in the real circuit, consider adding a trimmer in series to R_{LOW}.

Initial calculations for order of magnitude:
(estimate large Resistance (R_{up}) based on slightly higher target current.)

$$V_{ref} \approx 2.5\,\text{V}$$
$$I_{target} \approx 0.001\,\text{A}$$
$$R_{up} = \frac{V_{out}}{I_{target} \cdot 1.1} \approx \frac{48\,\text{V}}{0.001\,\text{A} \cdot 1.1} \approx 43\,636.4\,\Omega$$
$$R_{low} = \frac{R_{up}}{\left(\frac{V_{out}}{V_{ref}} - 1\right)} \approx \frac{43\,636.4\,\Omega}{\left(\frac{48\,\text{V}}{2.5\,\text{V}} - 1\right)} \approx 2397.6\,\Omega$$
$$I_{ref} = \frac{V_{out}}{R_{up} + R_{low}} \approx \frac{48\,\text{V}}{43\,636.4\,\Omega + 2397.6\,\Omega} \approx 0.001\,042\,71\,\text{A}$$

From these calculations we choose the following actual resistors:

$$R_{up} \approx 43\,700\,\Omega$$
$$R_{low} \approx 2400\,\Omega$$
$$I_{ref} = \frac{V_{out}}{R_{up} + R_{low}} \approx \frac{48\,\text{V}}{43\,700\,\Omega + 2400\,\Omega} \approx 0.001\,041\,21\,\text{A}$$
$$V_{ref} = I_{ref} \cdot R_{low} \approx 0.001\,041\,21\,\text{A} \cdot 2400\,\Omega \approx 2.498\,92\,\text{V}$$

R_{UP} = 43.7 kΩ	Code: KIT-RMCF1206FT-05	Package: 1206/3216		
R_{LOW} = 2.4 kΩ	Code: KIT-RMCF1206FT-04	Package: 1206/3216		/ 5 pt.

Q6: COMPENSATION NETWORK IMPLEMENTATION

Based on the calculation result of Q3 and Q5, calculate the values of the compensation resistor R_{COMP}, capacitor C_{COMP1} and C_{COMP2}.

ALTIUM Schematic Hints:
The compensation network, consisting of a parallel connection of C_{COMP2} and the series connection of R_{COMP} and C_{COMP1}, is connected between the pins COMP and FB.

$$
\begin{aligned}
C_{comp,1} &= \frac{1}{R_{up} \cdot G_{comp}} \\
&\approx \frac{1}{43\,700\,\Omega \cdot 94.8454} \\
&\approx 2.412\,69 \times 10^{-7}\ \mathrm{F} \\
R_{comp} &= \frac{1}{2 \cdot \pi \cdot f_{z,comp} \cdot C_{comp,1}} \\
&\approx \frac{1}{2 \cdot 3.141\,59 \cdot 400\,\mathrm{Hz} \cdot 2.412\,69 \times 10^{-7}\ \mathrm{F}} \\
&\approx 1649.14\,\Omega \\
C_{comp} &= \frac{1}{2 \cdot \pi \cdot f_{p,comp} \cdot R_{comp}} \\
&\approx \frac{1}{2 \cdot 3.141\,59 \cdot 400\,\mathrm{Hz} \cdot 1649.14\,\Omega} \\
&\approx 2.412\,69 \times 10^{-7}\ \mathrm{F}
\end{aligned}
$$

R_{COMP} =	16.5 kΩ	Code:	KIT-RMCF1206FT-04	Package:	1206/3216
C_{COMP1} =	0.22 µF	Code:	C1206C224K5RACTU	Package:	1206/3216
C_{COMP2} =	0.22 µF	Code:	C1206C224K5RACTU	Package:	1206/3216

/ 6 pt.

Q7: PLECS VERIFICATION

Using the PLECS model *Boost_PLECS.plecs*, verify the correct functioning of the designed compensation network in multiple operating conditions. Insert the picture of the Output Voltage Scope results.

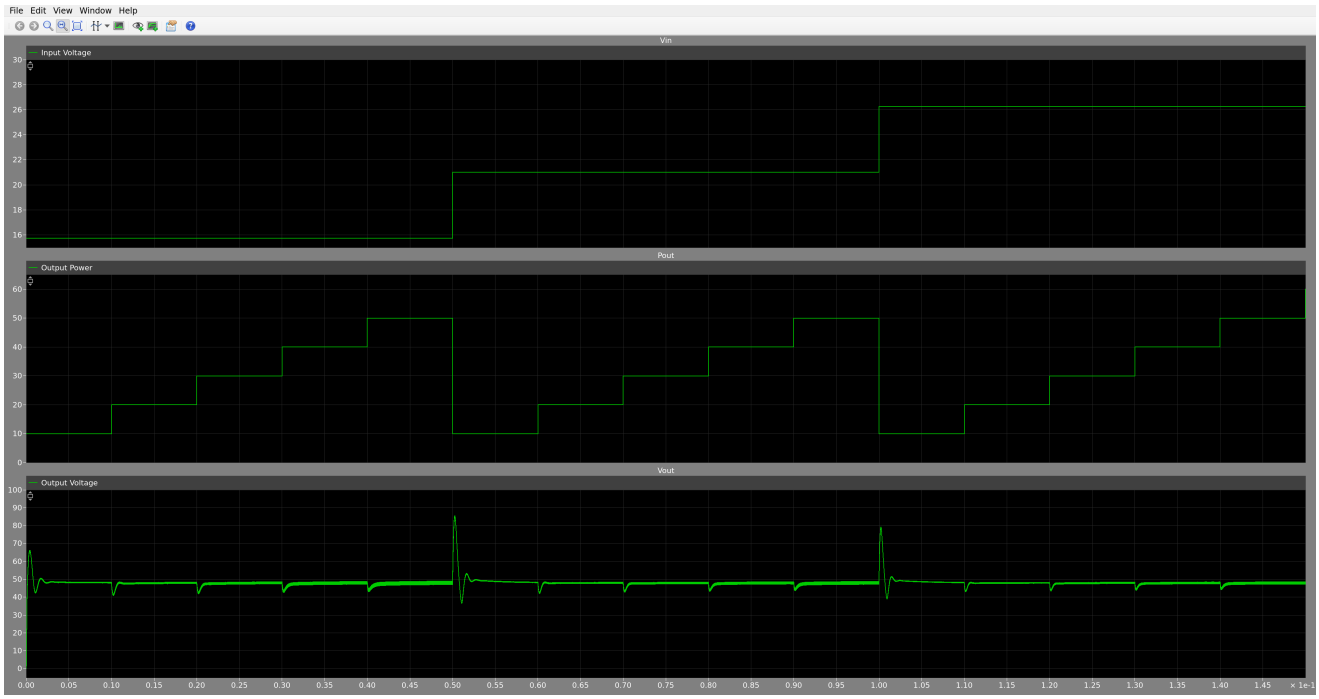


Figure 5 Simulation results obtained in PLECS.

Average output voltage of 47.97 V (target: 48 V)
Switching frequency of 123.6 kHz (target: 125 kHz)
Max simulated MOSFET voltage 85.5 V (Max rating 100 V)

Consequences: Reduce R_t and then fine-tune with variable series resistance (*VR*3 in Schematic)

NOTE: Mosfet voltage spikes to 97 V when removing load while operating at 50 W (aka, 100 % guarantee to destroy converter if load is removed under operation!!!)

/ 6 pt.

OVERVIEW OF ASSEMBLING AND TESTING PART

The last part of the project course deals with the assembling and testing of the designed boost converter.

To facilitate the debugging, the assembling, and testing are here divided into different steps, aimed at individually verifying the correct behavior of each part of the converter.

During the testing, the following instrumentation will be used:

- *Elektro-Automatik EA-PSI 5200-10A* DC power supplies (or equivalent power supplies),
- *BK Precision 8542B* Active Load,
- *Rigol DS1074Z* Oscilloscope,
- *Newtons4th Ltd PPA5530* Power Analyzer,
- *Omicron Lab Bode 100* Multifunctional Test Set,
- *FLIR E60* Thermal Camera.

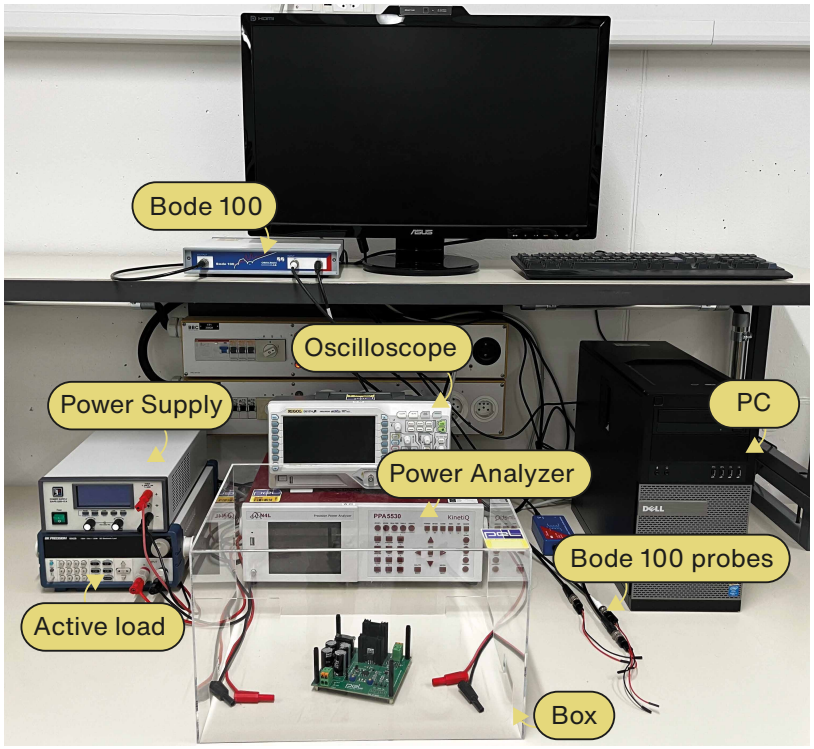


Figure 6 Complete test setup

PRELIMINARY ASSEMBLING AND TESTING

SOLDERING OF SMD COMPONENTS

Place the thermal paste and all the SMD components. Put the board in the oven and select the proper temperature profile, which can be found in the technical specifications of the thermal paste. Check the continuity with a multimeter and look for unintentional short circuits.

SOLDERING OF BOOST INDUCTOR AND DIODE

Solder the boost inductor. Solder Diode, place the heatsinks and connect them. Check the continuity with a multimeter and look for unintentional short circuits.

SOLDERING OF CONNECTORS, SOCKETS, JUMPERS, AND TEST POINTS

Solder the Input and Output Power Connectors, the Sockets of the UC3843AN device, the Jumpers, and all the Test-Points. Check the continuity with a multimeter and look for unintentional short circuits.

SOLDERING OF VARIABLE RESISTORS

If selected in the boost design, solder the Through-Hole variable resistors (i.e., Trimmers). Before soldering, measure with a multimeter what is the actual resistance between the terminals, and adjust it to be close to the rated value of the design.
Check the continuity with a multimeter and look for unintentional short circuits.

Q8: ZENER DIODE AND IC VOLTAGE SUPPLY

Use the power supply to provide your nominal voltage to the input connector pin, while the output load is disconnected. Verify if the Zener Diode is clamping the voltage as expected to supply the UC3843AN pin. Be careful to respect the correct polarity. With the oscilloscope, measure the voltage at the Vcc pin of UC3843AN.
Hints:
Set the power supply to have an OCP of 1 A.

on the oscilloscope, the values are higher than in reality. That's why, we used a multimeter and found $Vin = 21V$ and $V_{zener} = 15,55V$. Therefore, the zener is clamping the voltage as expected

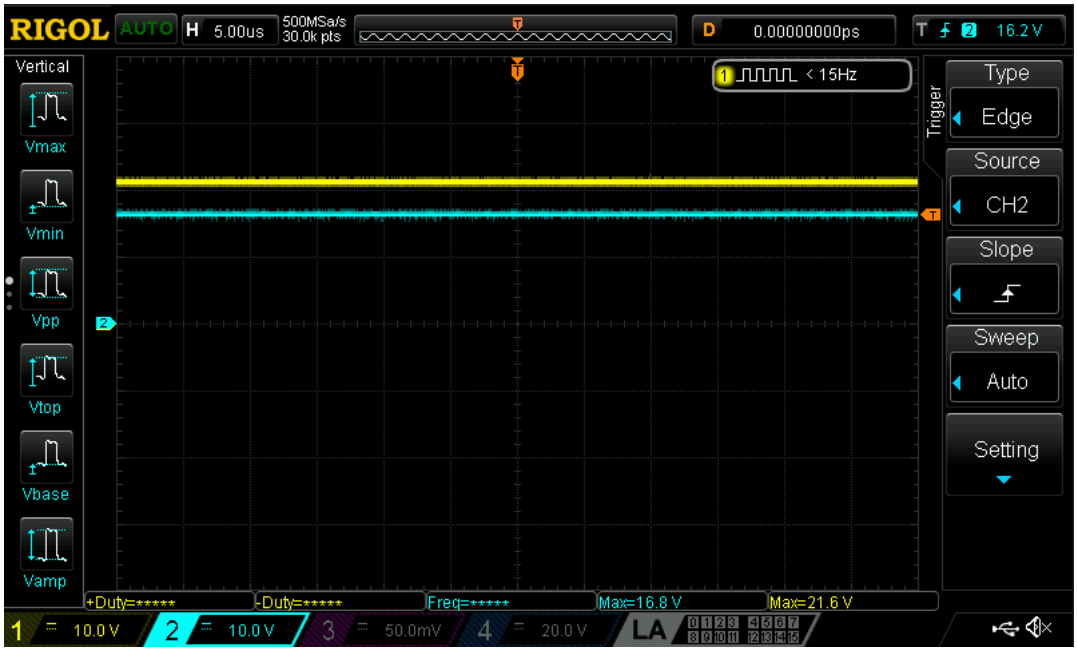


Figure 7 Input and Zener voltage

$V_{in} = 21V$	$V_{d,zener} = 15,55V$	/ 1 pt.

Q9: REFERENCE VOLTAGE OF UC3843AN

Place the UC3843AN controller in its socket. Connect the supply to the UC3843AN and verify if the voltage reference is 5 V. With the oscilloscope, measure the voltage at the Vref pin of UC3843AN.

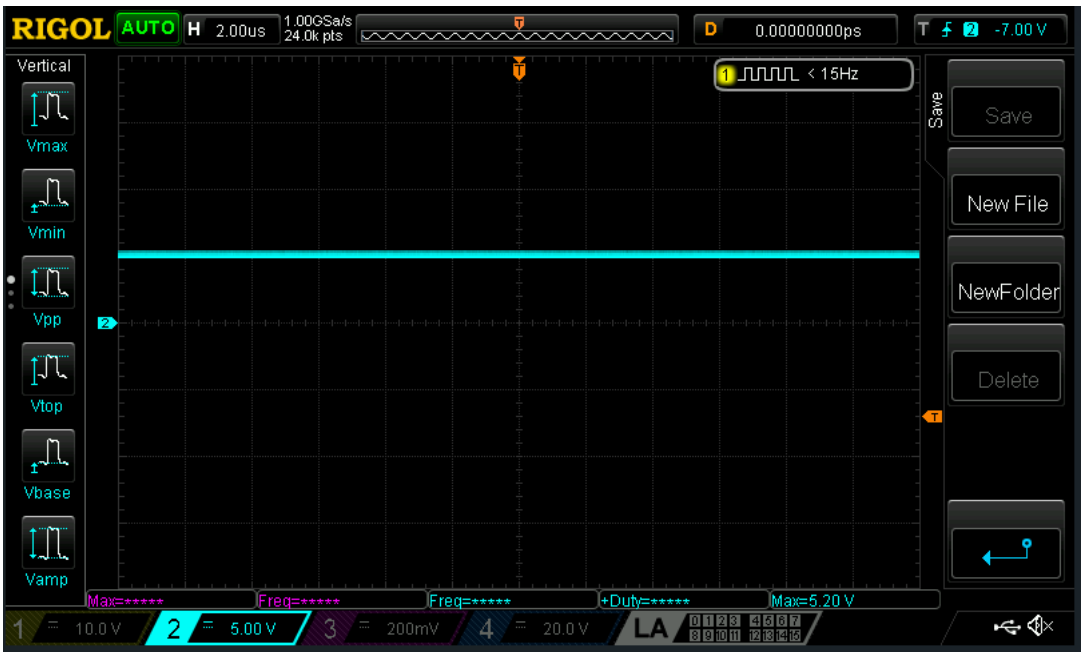


Figure 8 Oscilloscope capture of Vref

As becomes clear from this picture, our V_{ref} is at a very stable 5 V as expected.

$V_{ref} = 5V$	/ 1 pt.

Q10: FREQUENCY VERIFICATION

With the oscilloscope, measure the oscillator voltage at the RT/CT pin and the switching signal at the OUT pin by properly connecting to the corresponding test points.

Check the oscillator frequency f_{osc} at the RT/CT pin, the switching frequency f_{sw} at the OUT pin, and the maximum duty cycle D_{max} at the OUT pin, and compare them with the design specifications.

Include an oscilloscope capture of your results. Add the measurement of the frequencies and duty cycle through the oscilloscope "Measure" options.

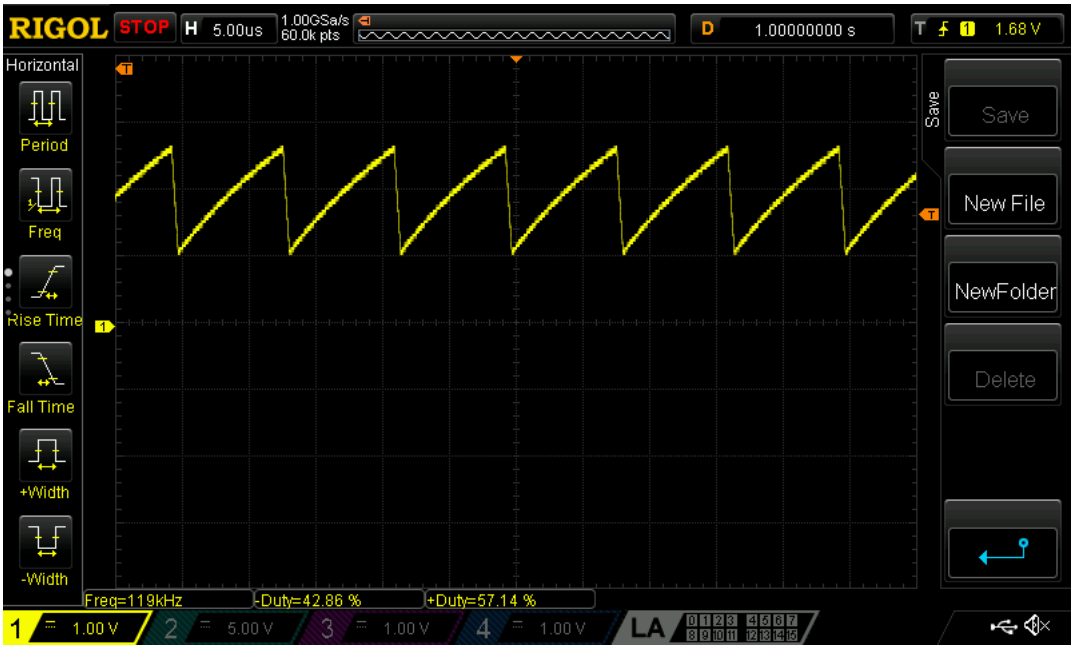


Figure 9 oscillator frequency measured at the Rt/Ct pin of the controller

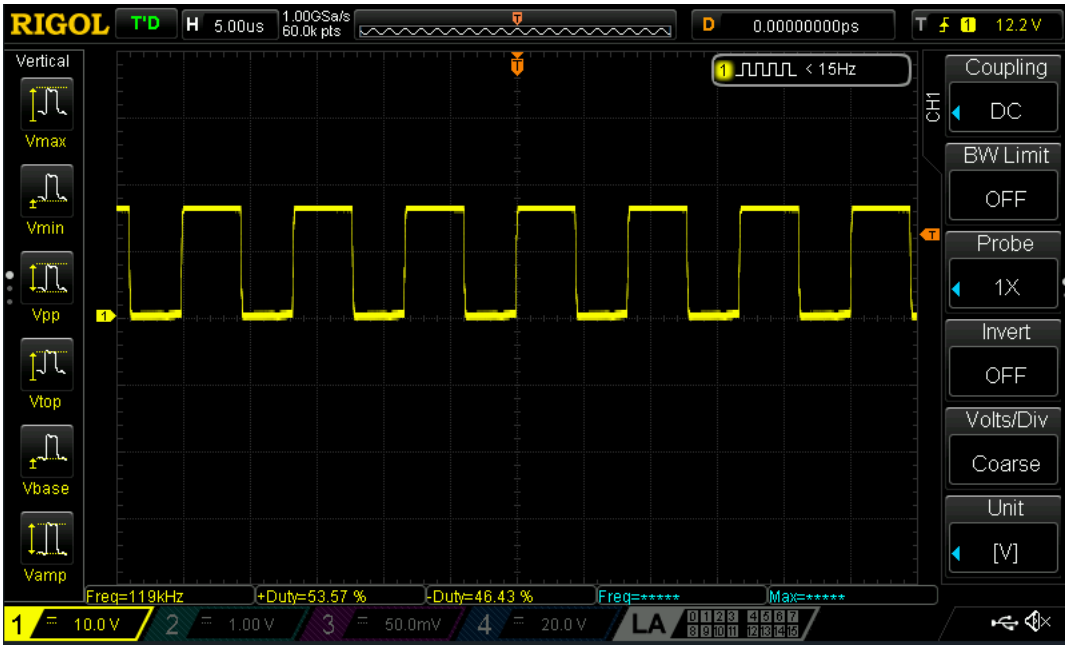


Figure 10 switching frequency measured at the output of the controller

We have a target switching frequency of 125 kHz. As you can see, we are very close to the target frequency with out 119 kHz and a maximum duty cycle of 0,54.

$f_{osc} = 119kHz$	$f_{sw} = 119kHz$	$D_{max} = 0,54$	/ 4 pt.

Q11: INPUT CAPACITOR VOLTAGE WITHSTANDING AND DISCHARGE TIME VERIFICATION

Use the power supply to provide your maximum input voltage to the boost input terminals, and check the voltage withstand capabilities of the input capacitor(s).

Set the power supply output to "OFF" and measure the discharge time of the input voltage until approx 1% of the initial value. Compare the results with the design choice done in R3 and motivate the obtained results.

As you can observe in the following figure, we need approximately 30s to discharge the input capacitor

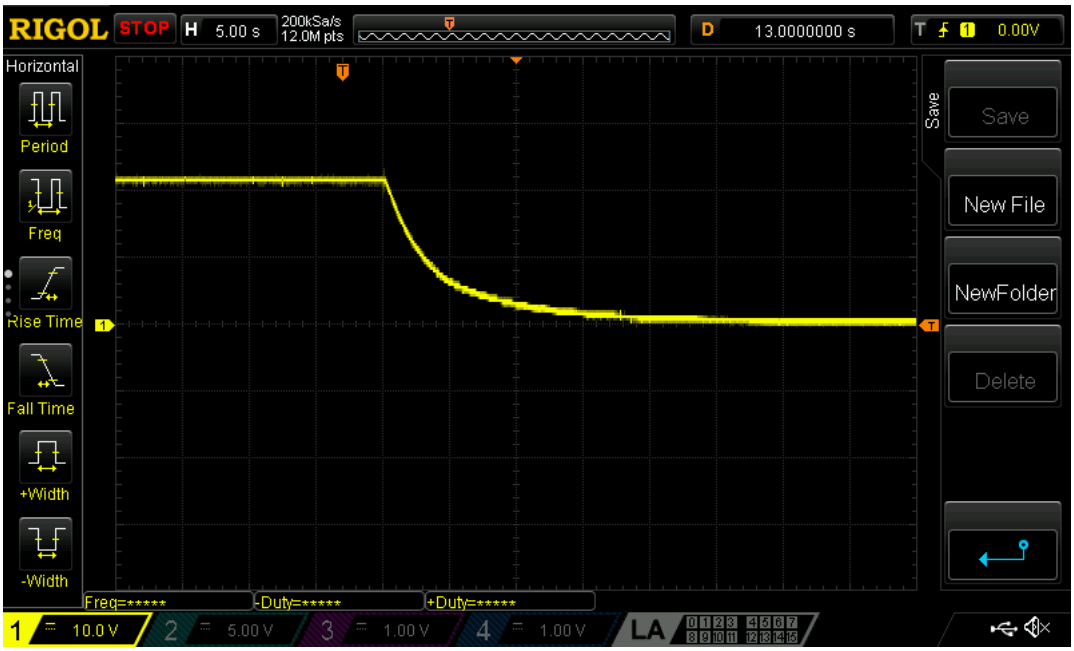


Figure 11 output capacitors discharge

$\Delta T_{in,disch.} = 30s$	/ 3 pt.

Q12: OUTPUT CAPACITOR VOLTAGE WITHSTANDING AND DISCHARGE TIME VERIFICATION

Use the power supply to provide your rated output voltage to the boost input terminals, and check the voltage withstand capabilities of the output capacitor(s).

Set the power supply output to "OFF" and measure the discharge time of the output voltage from U_{out} to around 1% of the rated output voltage. Compare the results with the design choice done in R3 and motivate the obtained results.

As you can observe in the following figure, we need approximately 40s to discharge the input capacitor

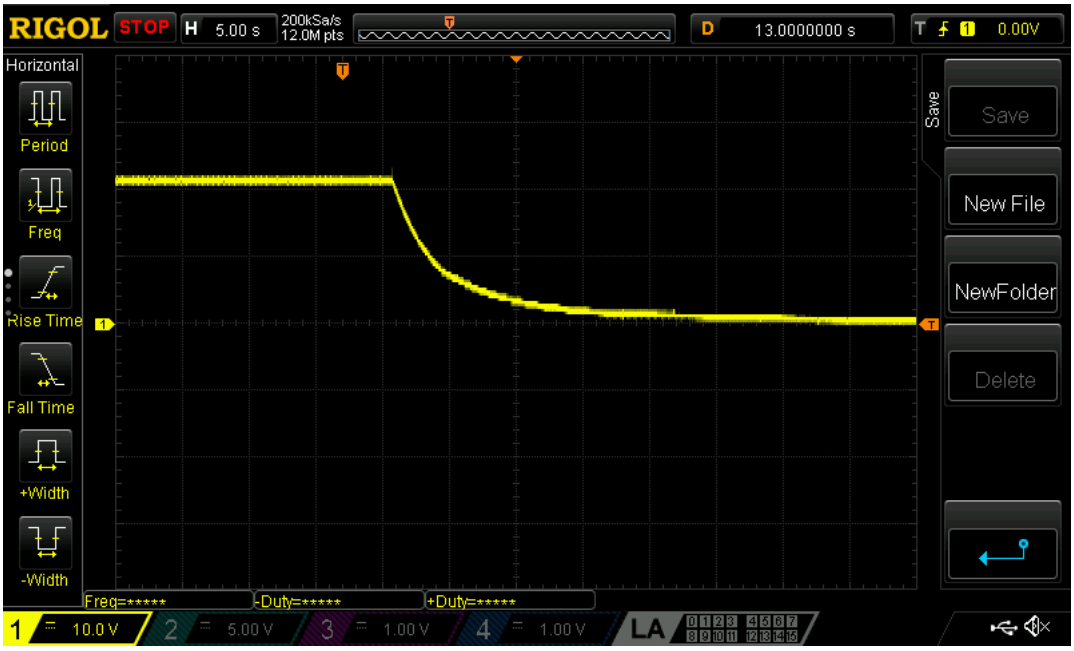


Figure 12 Oscilloscope capture

$\Delta T_{out,disch.} = 40s$	/ 3 pt.

Q13: OUTPUT VOLTAGE DIVIDER VERIFICATION

While using the power supply to provide the rated output voltage U_{out} to the boost output terminals, measure the voltage across the resistor R_{FBB} (i.e., the voltage that is applied at the Feedback pin of the UC3843AN) through the corresponding test point, and verify that it is close enough to the internal reference voltage of 2.495 V.

Compare the experimental result with the theoretical result of R3, and motivate the comparison.

the voltage acroos the resistor R_{FB} is very close to the internal reference voltage. It's at $2.48V$

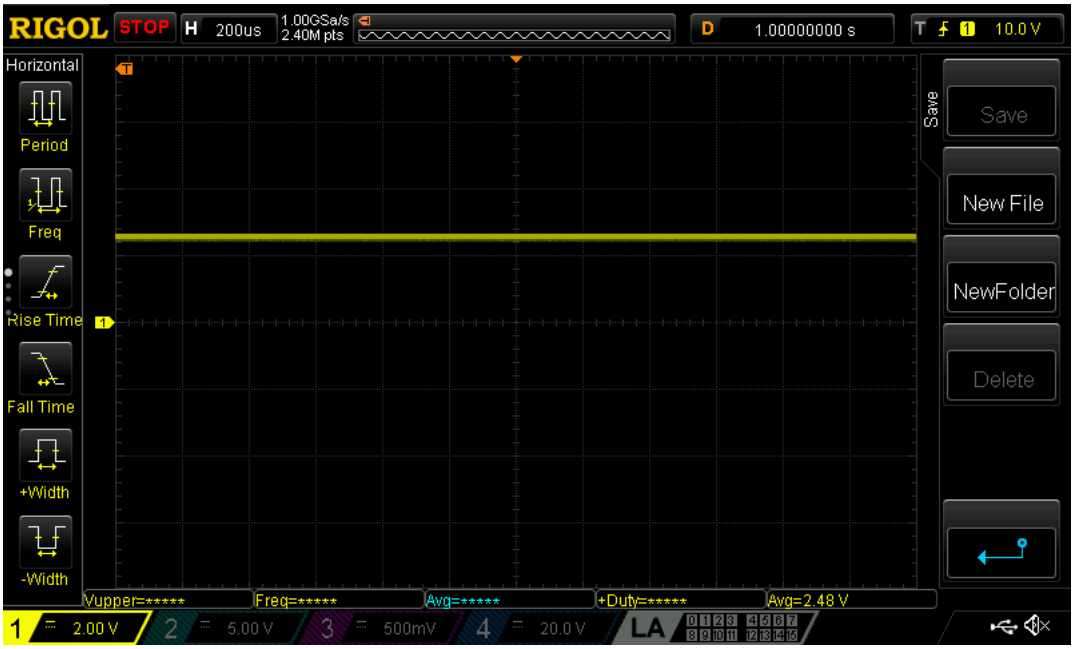


Figure 13 Oscilloscope capture of FB voltage

$V_{FB} = 2,48V$	/ 3 pt.

TESTING OF THE OUTPUT VOLTAGE CONTROL LOOP

SOLDERING OF MOSFET

Solder the MOSFET. Place the heatsinks and connect them to the switching devices. Check the continuity with a multimeter and look for unintentional short circuits.

Q14: VERIFICATION OF THE OUTPUT VOLTAGE CONTROL

This test is aimed to verify the correct functioning of the output voltage control of the UC3843AN.
With an oscilloscope verify if the output voltage is regulated.
Set the oscilloscope to measure the following variables:

- the Switching signal at the OUT pin of the UC3843AN,
- the Voltage on the R_{shunt} resistor (it identifies the real MOSFET current),
- the Isense pin of the UC3843AN (it identifies the filtered MOSFET current),
- the Output Voltage U_{out}.

With the following graph, we can measure the peak current as $\frac{V_{CS}}{R_{CS}} = \frac{62}{150} = 0.41V$.

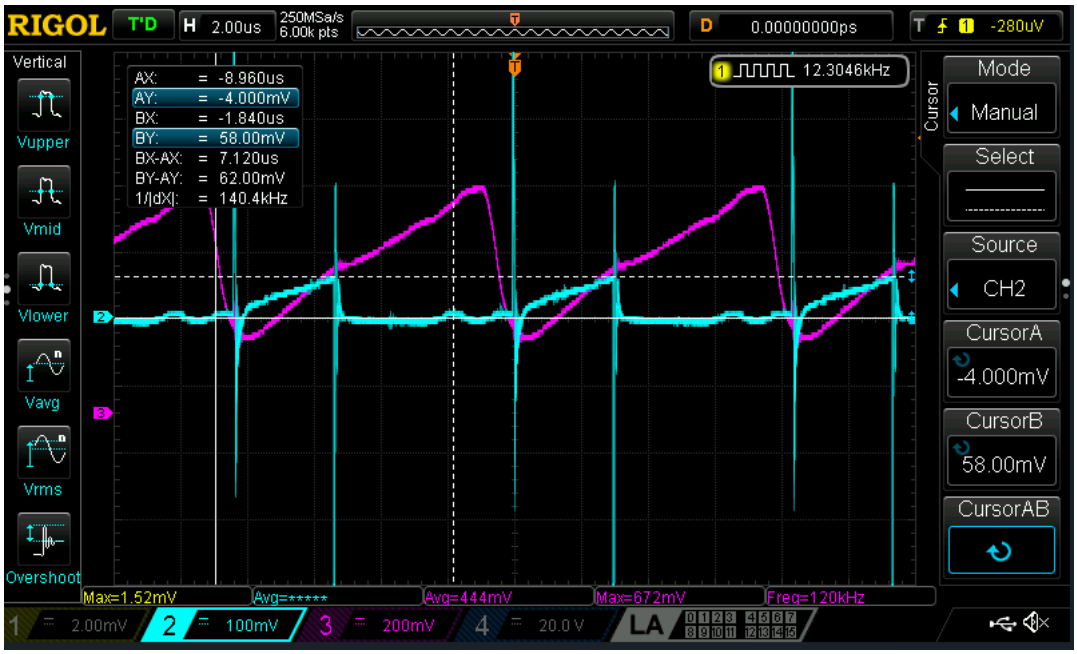


Figure 14 Isense in blue and CS in purple

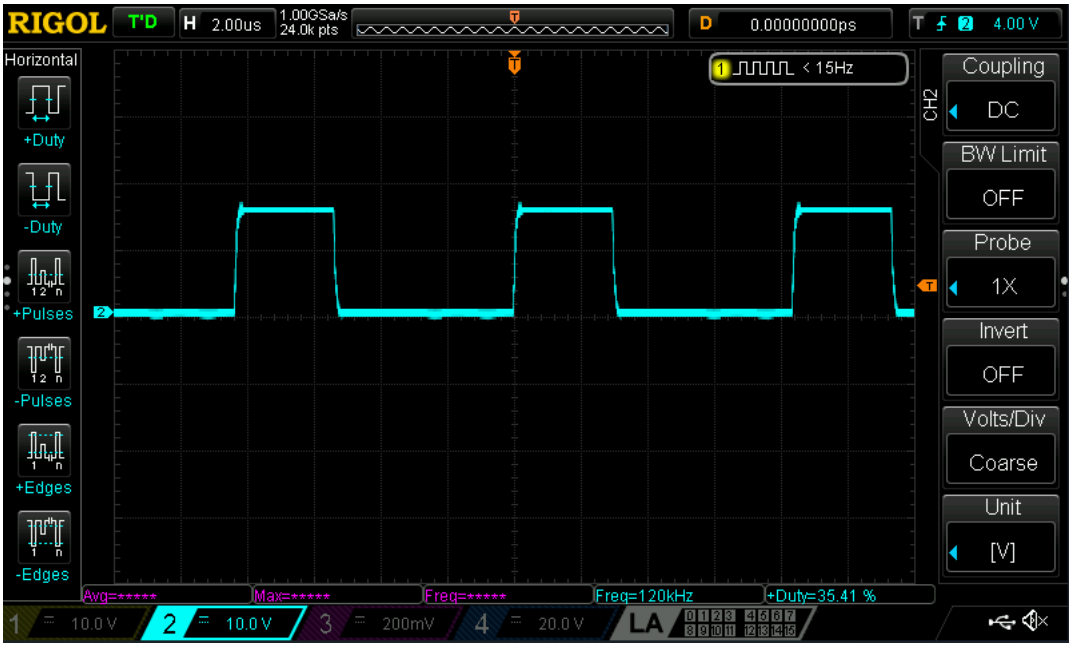


Figure 15 Output of the controller

Here we can observe that our Duty cycle is 0.35.
In the following graph, it says that we are at $50V$ output voltage when in reality we measured it as $48V$ with the multimeter

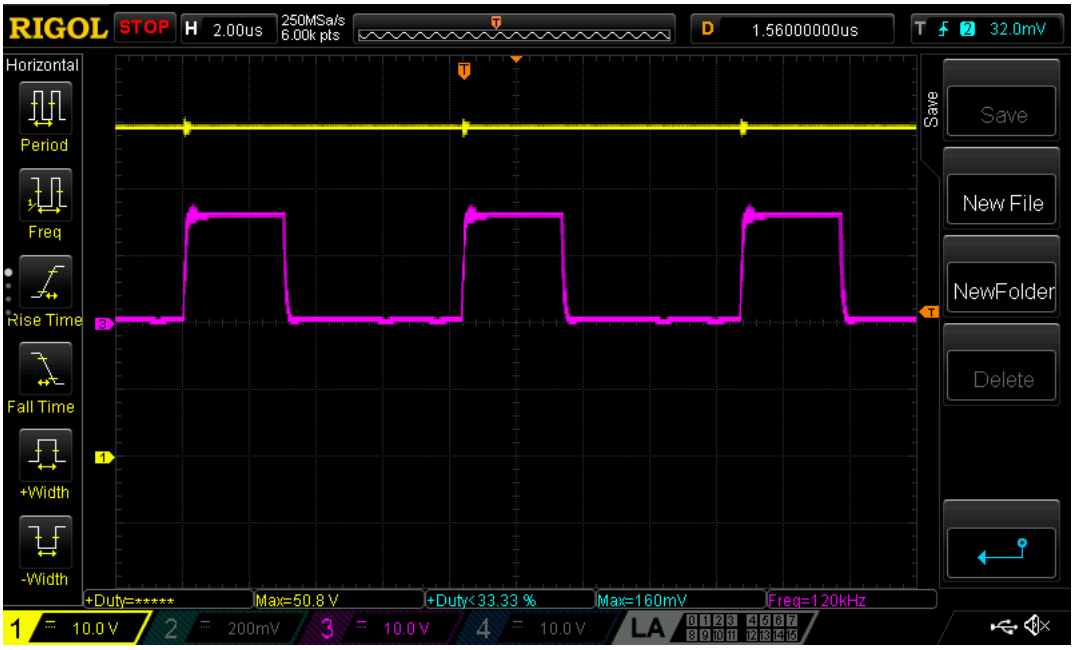


Figure 16 Output of the controller and main output voltage

Figure 17 Voltage from drain to source measured by putting a pin on drain and an other to CS

$D = 0,35$	$I_{peak} = 0,4A$	$V_{DS,max} = 50V$	/ 10 pt.

TESTING OF THE PEAK CURRENT CONTROL

This test is aimed to verify the correct functioning of the peak current control of the UC3843AN. At this stage, the current will be controlled in a closed loop with the load.

Connect the output terminals to the active load. Set the active load to CC "Controlled Current", and set a small current (e.g. $I_{load} = 0.2$ A.) Connect the oscilloscope to measure the following variables:

- the Switching signal at the OUT pin of the UC3843AN,
- the Voltage on the R_{shunt} resistor (it identifies the real MOSFET current),
- the Isense pin of the UC3843AN (it identifies the filtered MOSFET current),

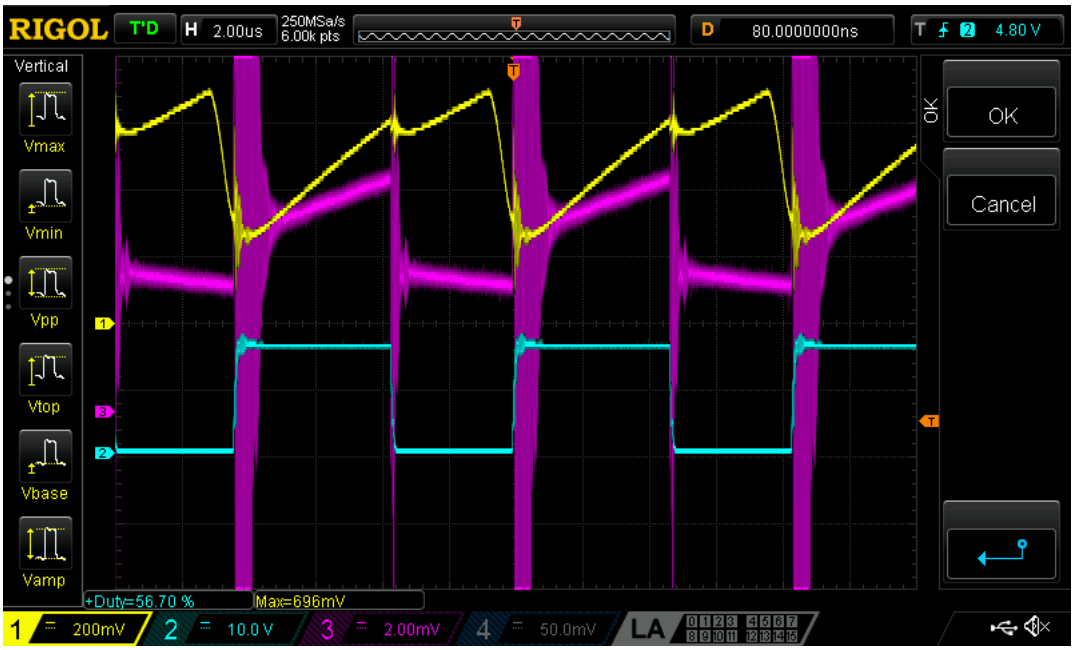


Figure 18 Oscilloscope capture example

We can see in the above image, that the ISENSE voltage is a lot less noisy than the voltage over the shunt. We can also clearly see that added slope coming from the Rt/Ct par of the current sensing circuit.

$D = 0.56$	$I_{peak} = 1A$	$U_{out} = 47,97V$	/ 10 pt.

Q15: VERIFICATION AT HALF AND NOMINAL POWER

Connect the input and output terminals of the boost converter to the supply source and active load, respectively. Set the active load to CC and increase the load to first 25 W, and later to 50 W.
Check the output voltage U_{out}, and verify that it is correctly stabilized at its rated desired value.

Include an oscilloscope capture of your results. By using the oscilloscope "Measure" options, including the following information:

- Duty cycle of the switching signal,
- Peak value of the voltage across R_{shunt} (from which it is possible to compute the peak primary current),
- Peak value Isense pin (which takes into account the effects of the filtering),
- Average value of the output voltage.

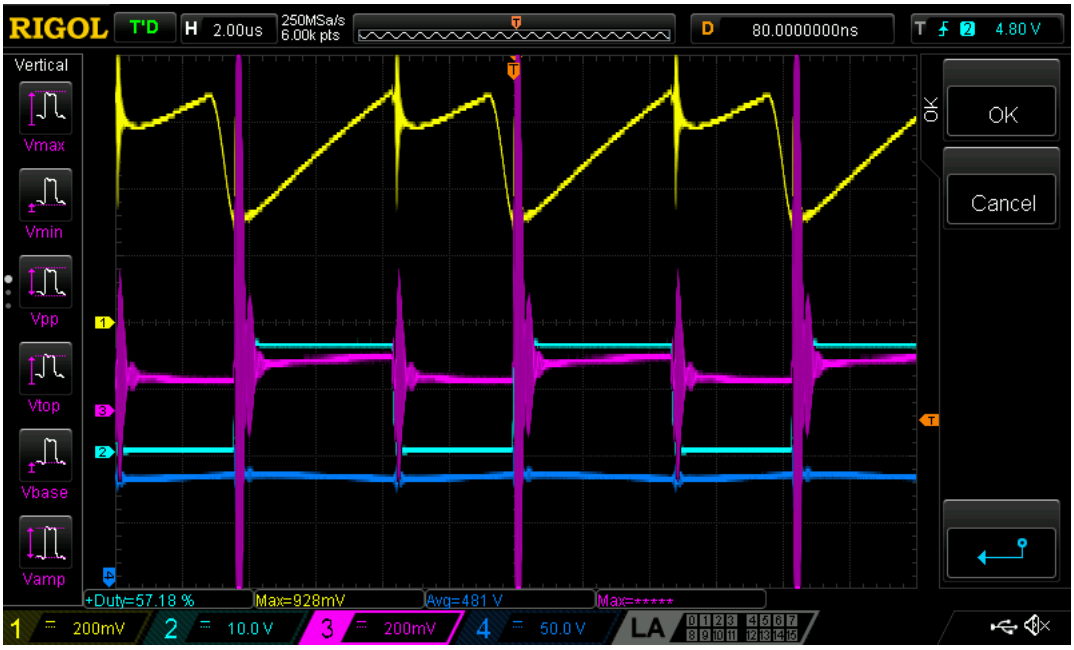


Figure 19 Oscilloscope capture halfpower

Figure 20 Oscilloscope capture fullpower

With these two images we can see that boost converter remains stable when connected to a load. We can also see the effect of the load on the duty cycle and the slope compensation.

$D = 0,57$	$I_{peak} = 3,3A$	$U_{out} = 47.94V$	/ 10 pt.

Q16: VERIFICATION AT DIFFERENT INPUT VOLTAGES

Verify the correct functioning of the converter at your minimum input and maximum input voltage.

Check the output voltage U_{out}, and verify that it is correctly stabilized at its rated desired value.

Again, include an oscilloscope capture of your results.

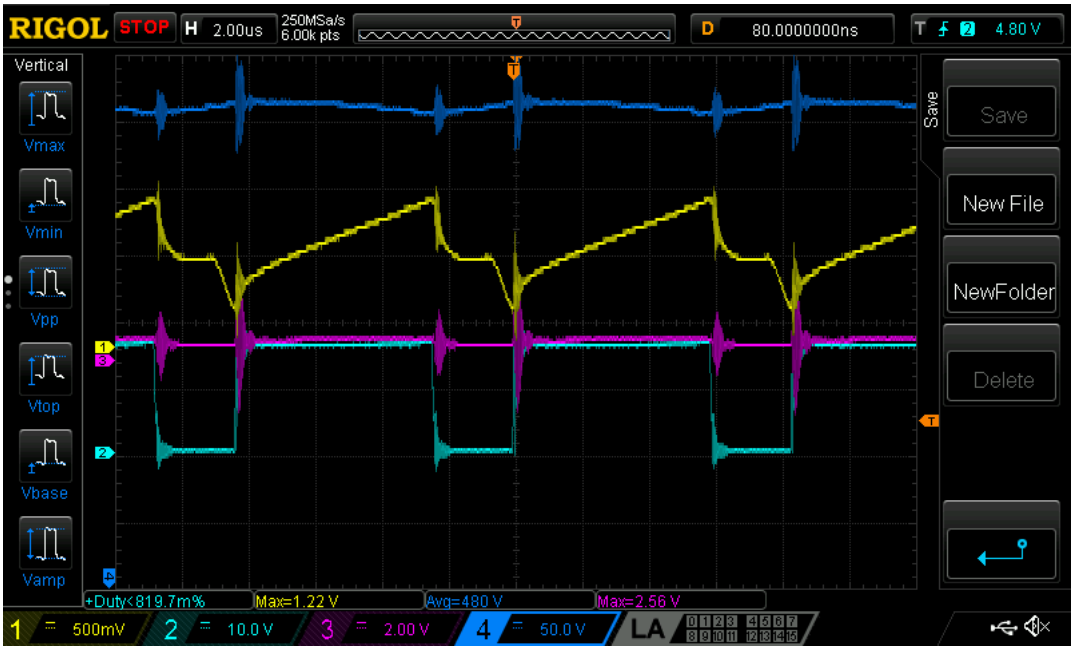


Figure 21 Oscilloscope capture Vin min

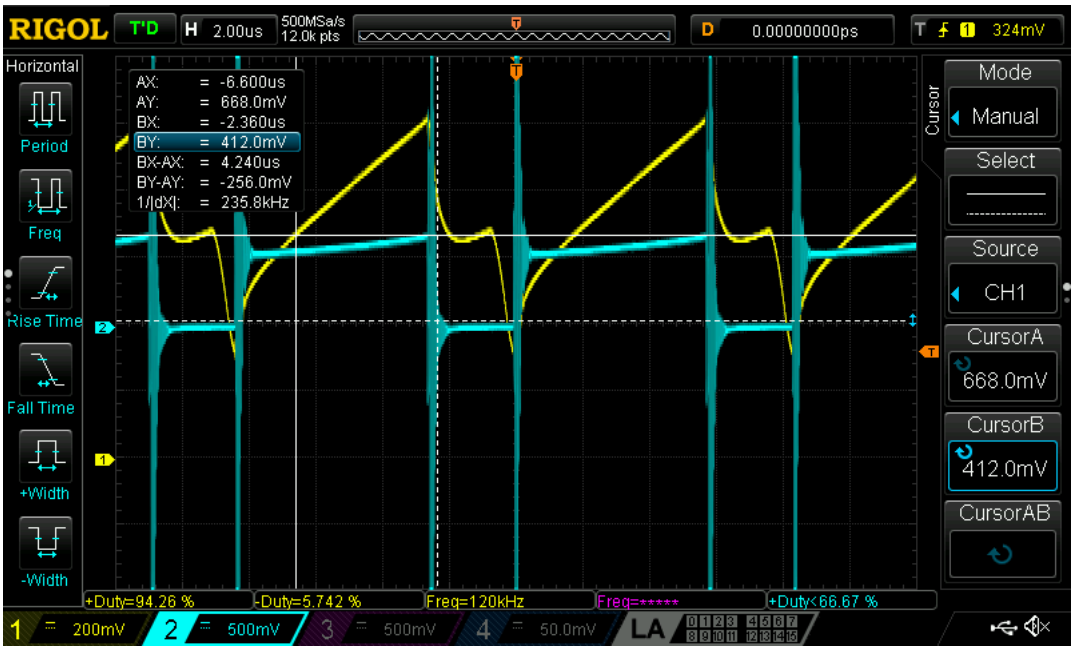


Figure 22 current measurment at Vin min

current can measured as $\frac{V_{CS}}{R_{CS}} = \frac{668}{150} = 4.45A$.

Figure 23 Oscilloscope capture Vin max

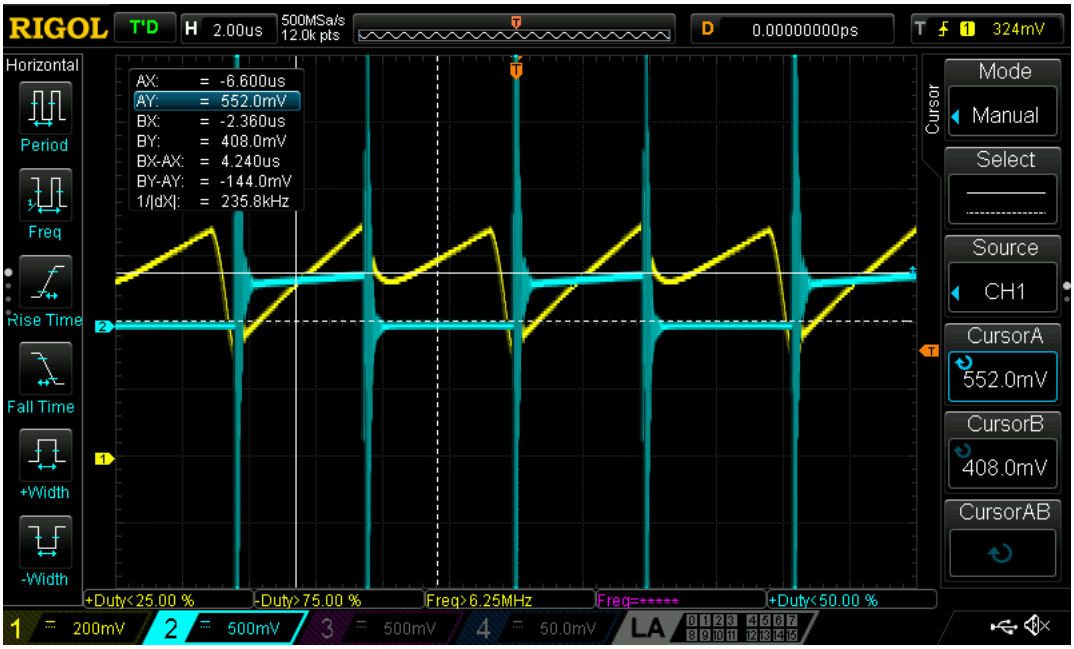


Figure 24 current measurment at Vin max

current can measured as $\frac{V_{CS}}{R_{CS}} = \frac{552}{150} = 3,68A.$

We can see that our system is stable in the input voltage range of 15.75-26.25 V. We can also observe a change in the duty cycle (note that the oscilloscope measure of the duty cycle for Vin min does not reflect the actual duty cycle)

$D(@U_{in,min}) = 0,69$	$I_{peak}(@U_{in,min}) =$ 4.45 A	$U_{out}(@U_{in,min}) = 47,96V$	
$D(@U_{in,max}) =$ 0.46	$I_{peak}(@U_{in,max}) =$ 3.68 A	$U_{out}(@U_{in,max}) = 47,94V$	/ 10 pt.

Q17: VERIFICATION OF OUTPUT VOLTAGE RIPPLE

Verify output voltage ripple. Again, include an oscilloscope capture of your results.

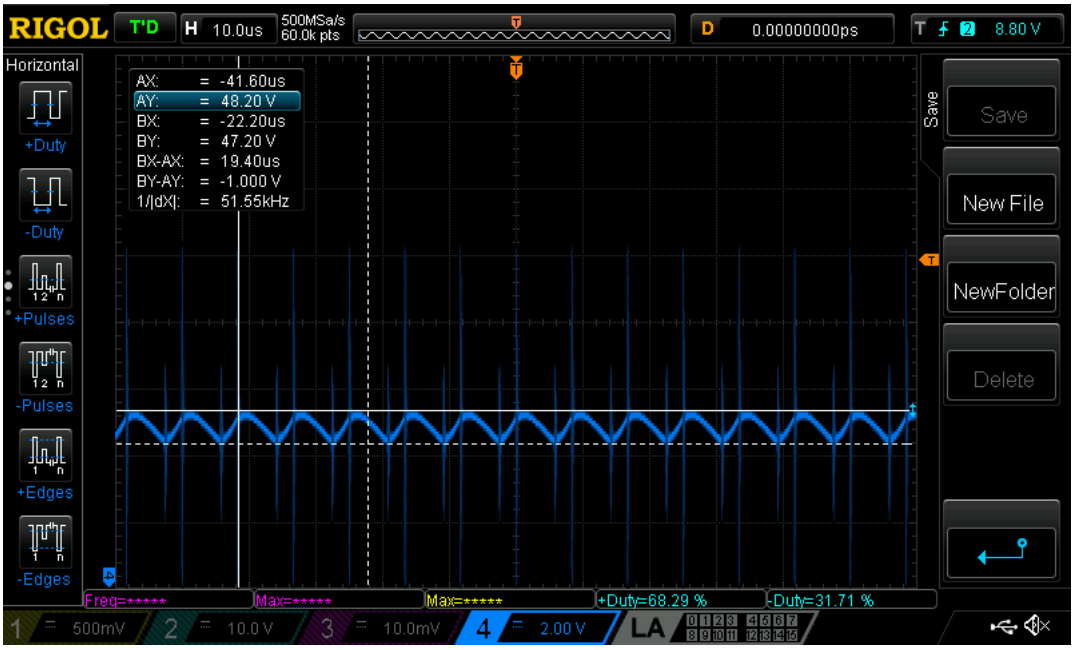


Figure 25 Oscilloscope capture output ripple Vin min

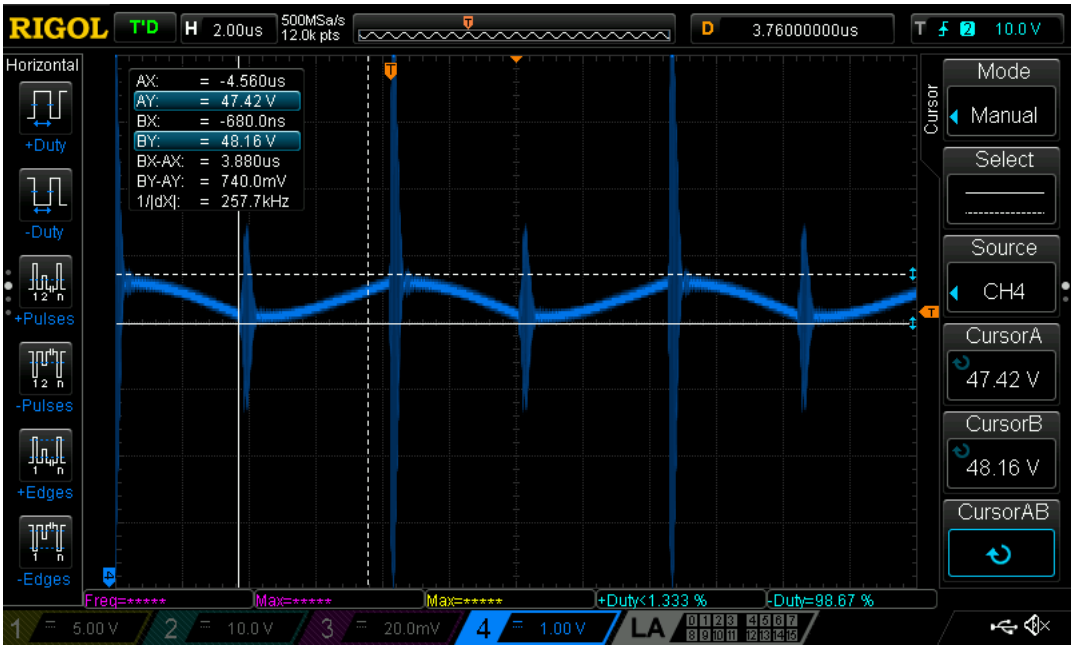


Figure 26 Oscilloscope capture output ripple Vin max

The accepted peak-to-peak output voltage ripple is 2.4 V, and we are clearly below that with a peak to peak ripple of 1 V.

$D(@U_{in,min}) = 0,69$	$I_{peak}(@U_{in,min}) = 4,45A$	$\Delta U_{out}(@U_{in,min}) = 0,7V$	
$D(@U_{in,max}) = 0,46$	$I_{peak}(@U_{in,max}) = 3,68A$	$\Delta U_{out}(@U_{in,max}) = 1V$	/ 10 pt.

LOOP STABILITY MEASUREMENT

The stability and robustness of the voltage control can be tested with the Omicron Lab Bode 100 multifunctional test set. This test is based on the injection of a small perturbation between the real output voltage terminal and the output voltage measurement used for the closed-loop voltage control, and on the measurement of the corresponding effects on the control loop.
Useful information can be found in the information note *Loop Gain Measurement - The Voltage Injection Method using the Bode 100 and the B-WIT 100.pdf* and in the *Bode 100 User Manual*.

Disable the primary-side power supply and the output-side active load.

Disconnect the jumper on the injection resistance R_{inj} and connect its terminals to the output of the B-WIT 100 Wideband Injection Transformer. Connect the input of the B-WIT 100 Wideband Injection transformer to the Bode 100 Output BNC.

Connect the Channel 1 Input of the Bode 100 between the terminal of the jumper connected to R_{FBU} (i.e., the terminal used for the output voltage measurement) and the secondary-side GND. Connect the Channel 2 Input of the Bode 100 between the terminal of the jumper connected to the positive secondary-side output terminal (i.e., the terminal corresponding to the real output voltage) and the secondary-side GND.

Connect the Bode 100 to the PC, turn it on and open the program *Bode Analyzer Suite*. Select the "Gain/Phase" measurement mode. Check in the "Hardware Setup" page that both Input 1 and Input 2 of the Bode 100 are set in "High Impedance" mode. Set the injection frequency sweep from 100 Hz to 1 MHz and the Source Level to -20 dBm.

Q18: LOOP STABILITY IN THE NOMINAL OPERATING POINT

Set the active load in CR "resistive mode" and choose the resistance in a way to absorb the nominal power $P_{out} = 50\,\text{W}$ when the converter voltage U_{out} is at its nominal value.

Enable the active load and the primary-side power supply, and set the input voltage to $U_{in} = 50\,\text{V}$.

In the Bode Analyzer Suite, enable the continuous injection of the perturbation voltage, and monitor the results. In case the results are too noisy, increase the Source Level value. In case the "Receiver Overload" message is displayed, change the "Attenuator Levels" of the receivers.

Export the results and process them offline. Draw the bode plot of the measured Loop Gain and check the crossover frequency f_{bw}, the phase margin φ_m, and the gain margin G_m.

Compare the results with the theoretical values computed in R2.

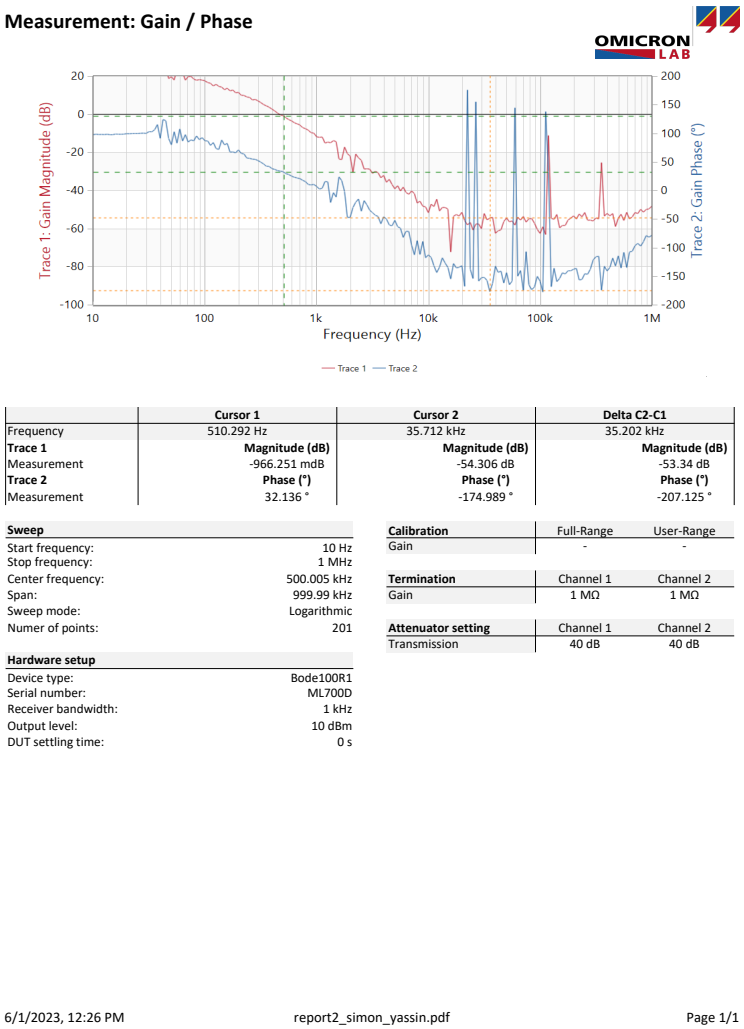


Figure 27 OMICRON output pdf

The gain margin is calculated as $-32 + 180 = 148^{\circ}$.
Note that our crossover frequency is lower than what we calculated, because we sometimes stability issues and so decided to experimentally lower the crossover frequency in the hardware. This has resulted in an incredibly stable system as can be seen by both gain and phase margins. Moreover, as indicated by the TA, we cannot find the the gain margin as the phase does not reach -180°.

$f_{bw} =$ 510 Hz	$\varphi_m =$ 148°	$G_m =$ *NAN*	/ 6 pt.

EFFICIENCY MEASUREMENTS

Once the converter's functioning has been verified, it is possible to evaluate its energetic performance.

Turn on the power analyzer. Set the coupling to "dc" and add the measurement of the efficiency as "phase/next phase". Set the display in "three-phase mode". The boost output variables and the energetic efficiency can be read from the "Phase 1" column, while the boost input variables can be read from the "Phase 2" column of the display. Discard the reading displayed in the "Phase 3" column.

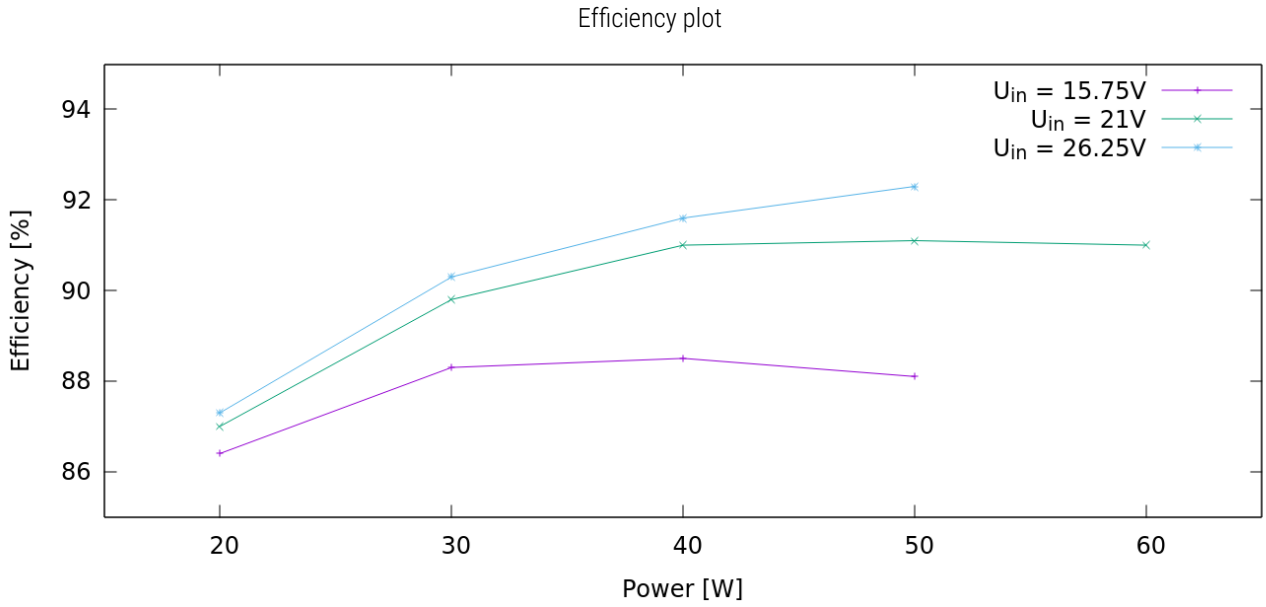
Q19: EFFICIENCY PLOT

Turn on the primary-side power supply and the secondary-side active load. Fill the table below with the efficiency measurements in the listed operating conditions. Then, include an Efficiency plot of your results.

Table 1 Efficiency Measurements.

U_{in} (↓) P_{out} (→)	20 W	30 W	40 W	50 W
15.75 V	86,4%	88,3%	88,5%	88,1%
21 V	87%	89,8%	91%	91,1%
26.25 V	87,3%	90,3%	91,6%	92,3%

at 60W we are at 91% efficieny



We can see clearly that the efficiency is better with higher input voltage. We can also see that for each input voltage, there is an optimum load for hightes efficiency. In our case for nominal input voltage, the ideal load is the specified 50 W.

/ 6 pt.

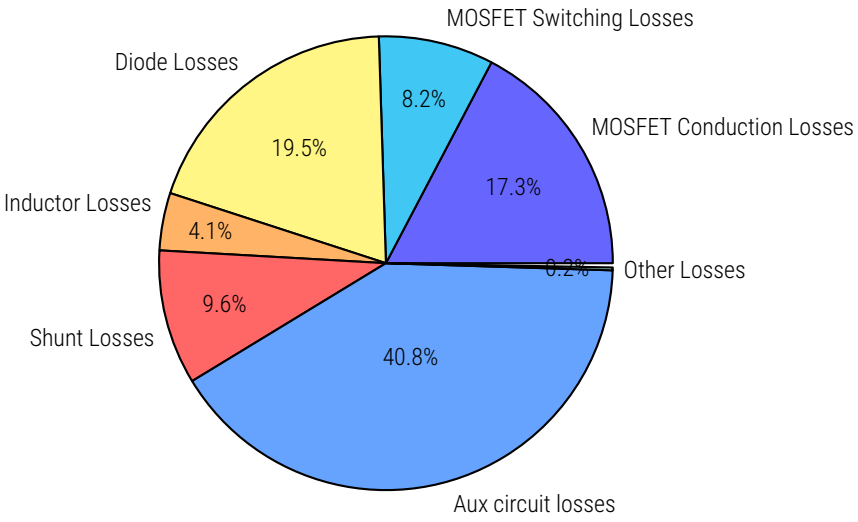
Q20: ANALYSIS OF THE POWER LOSSES

Considering the converter nominal operating point (i.e., with $U_{in} = 50$ V and $P_{out} = 50$ V), compute the power losses and estimate the different contributions. Explain how each different contribution has been estimated from the available measurements.
Fill in the table below and the corresponding pie chart.

Then, suggest a possible way to modify the design in a way to reduce the losses and improve the efficiency of the converter.

Table 2 Power Losses Contributions.

Total Power Losses	4.88 W	100%
MOSFET Conduction Losses	0.85 W	17.3%
MOSFET Switching Losses	0.4 W	8.2%
Diode Losses	0.95 W	19.5%
Inductor Losses	0.2 W	4.1%
Shunt Losses	0.47 W	9.6%
Auxiliary Circuit Losses	2 W	40.8%
Other Losses	0.01 W	0.2%



As we can see, the auxillary power supply consumes the most unnecessited power. An easy way to drastically reduce the power would be not to burn all the voltage over R_{aux} but maybe use the input voltage and a traco-power buck converter to power the IC. Another way to reduce power losses would be to decrease the R_{gate} so that there are less switching losses.

/ 6 pt.

THERMAL MEASUREMENTS

The last step of the testing is to verify the thermal capabilities of the converter.

Q21: THERMAL MEASUREMENT AT THE NOMINAL OPERATING POINT

Set up the converter to work at its nominal operating point. Let the boost converter operate for 10 min.

Measure with the thermal camera the temperature of the components on the PCB comprising your converter. Include the captured thermal image in your answer, and identify the component(s) with the highest temperature(s) and explain why exactly is this the case.

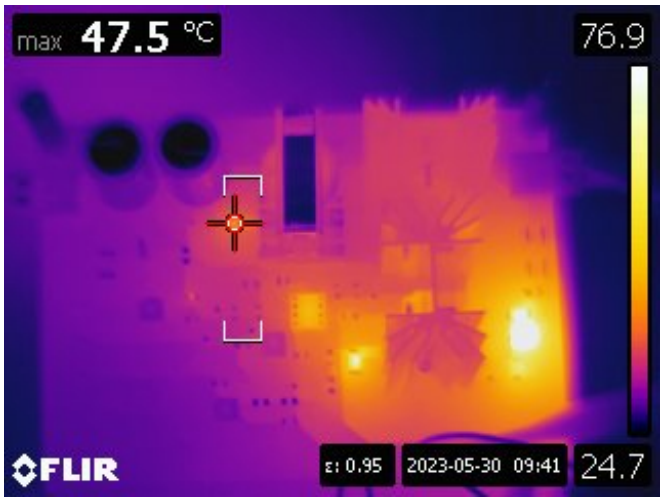


Figure 28 thermal image of boost converter measurement

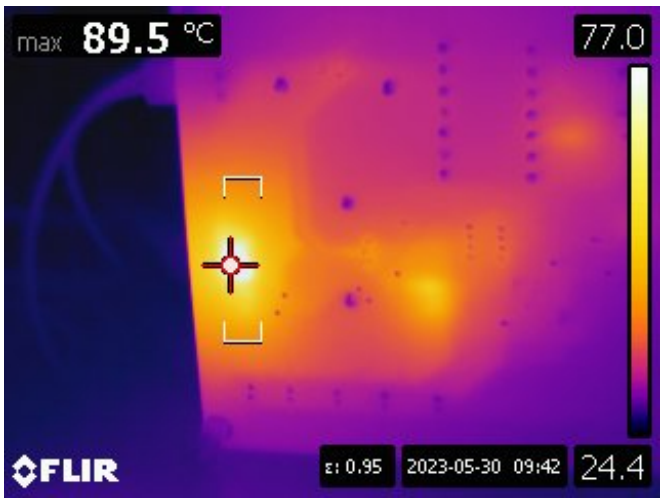


Figure 29 backward thermal image of boost converter measurement

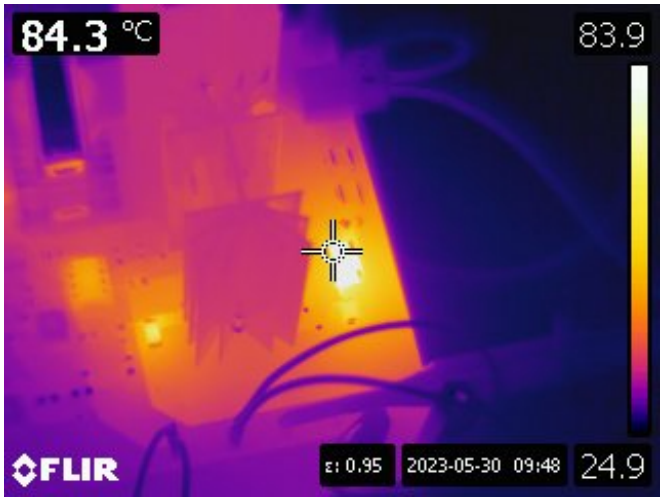


Figure 30 thermal image of boost converter measurement

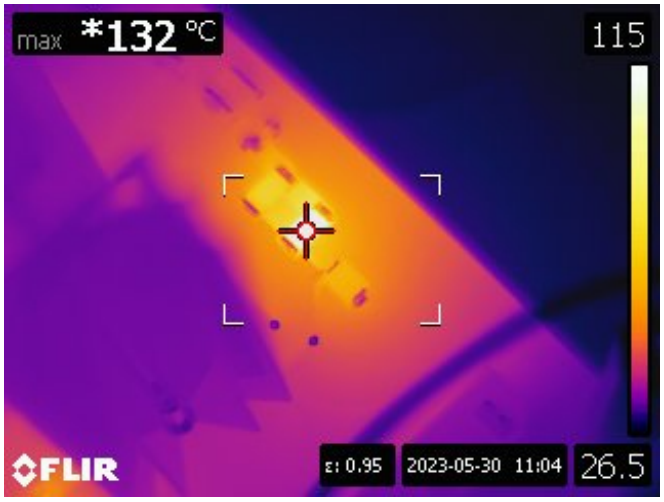


Figure 31 thermal image of boost converter measurement

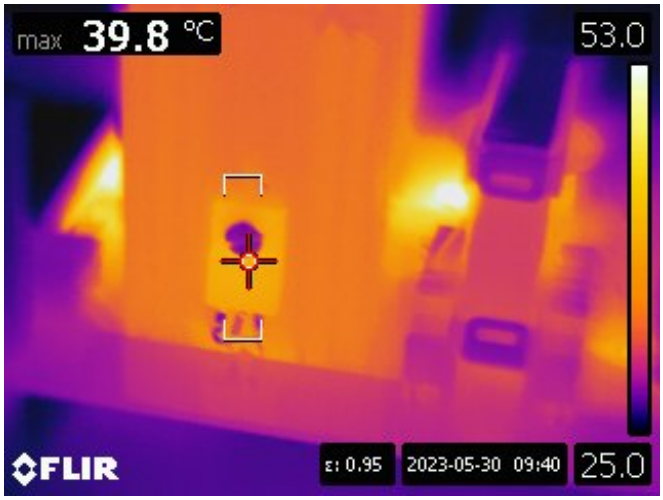


Figure 32 thermal image mosfet

What we can see clearly is that the auxillary power is the hottest. This corresponds to what we found in the losses analysis as it is not the most efficient way of powering the IC.
On the flip side, our semiconductor devices are very cool, both the MOS-FET and diode measuring at less than 50 °C.

T_{max} = 130°C	/ 7 pt.