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Title

INTERLEAVING OPERATION OF DC-DC BUCK CONVERTERS

Course Name

EE-409(c) Lab in electrical energy systems

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THEORY

Understanding certain concept that is of key relevance for the objectives of the project. Each project is therefore dealing with well-defined topic.

In the realm of power electronics, DC-DC buck converters are instrumental in efficiently stepping down voltage levels while concurrently increasing current output. These converters operate on the principle of switching control. Using a transistor to periodically connect and disconnect the input voltage, with the output voltage being determined by the duty cycle of this switching.

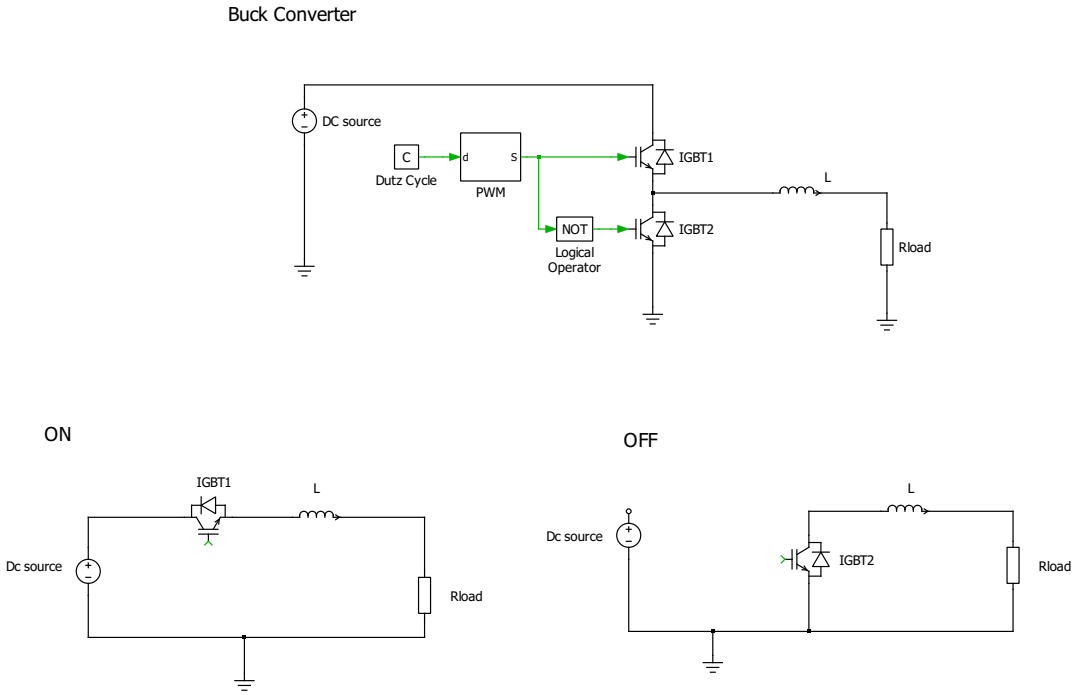


Figure 1 Schematic of buck converter showing the integral circuit and comparison when the transistor is on and off

Applying kirchoff's laws and assuming power conservation, we get that:

$$\frac{V_{out}}{V_{in}} = D \qquad \frac{I_{out}}{I_{in}} = \frac{1}{D} \qquad 0 \leq D \leq 1 \tag{1}$$

Therefore, by storing energy in an inductor and smoothing out the resultant voltage and current ripples with capacitors, buck converters provide a stable and regulated DC output.

The innovation of interleaving multiple buck converters has further enhanced their performance and applicability. Indeed, Interleaving, the process of operating different converters (phases) in parallel so that their switching does not occur simultaneously, as shown in 2, offers significant advantages. The interleaving strategy adopted is that all phases have the same switching frequency and duty cycle but have phase shift between them equal to $\frac{2\pi}{n}$ with n being the number of phases interleaved.

It facilitates load current sharing and reduces both input and output current ripples, which translates to smaller, more cost-effective components, and minimizes electromagnetic interference. Indeed, as shown in 3b, the individual ripple of each phase current cancels one another out to give out a smaller overall current ripple.
Moreover, as it can be noticed in 3a, a higher phase count can reduce the amount of current the input capacitors have to handle by 50% or more depending on the duty cycle [1]. Furthermore, with n being the number of phases, it can be observed in 3c that the maximum ripple of a n-phase buck converter, is equal to the maximum ripple of a single phase converter divided by n, the ripple frequency is equal to the single phase frequency multiplied by n and zero ripple occur at duty cycles equal to $\frac{1}{n}, \frac{2}{n}, \frac{3}{n} \ldots \frac{n-1}{n}$ [2] [3].

$$\begin{cases} max\,(n\_phase\,\Delta I) & = \frac{max(1\_phase\,\Delta I)}{n} \\ n\_phase\,f_{\Delta I} & = n \cdot 1\_phase\,f_{\Delta I} \end{cases} \tag{2}$$

This distributed approach to power conversion not only enhances efficiency by curbing resistive losses but also improves thermal management—dispersing heat more evenly and thus bolstering the reliability and longevity of the system. Furthermore, in high-power

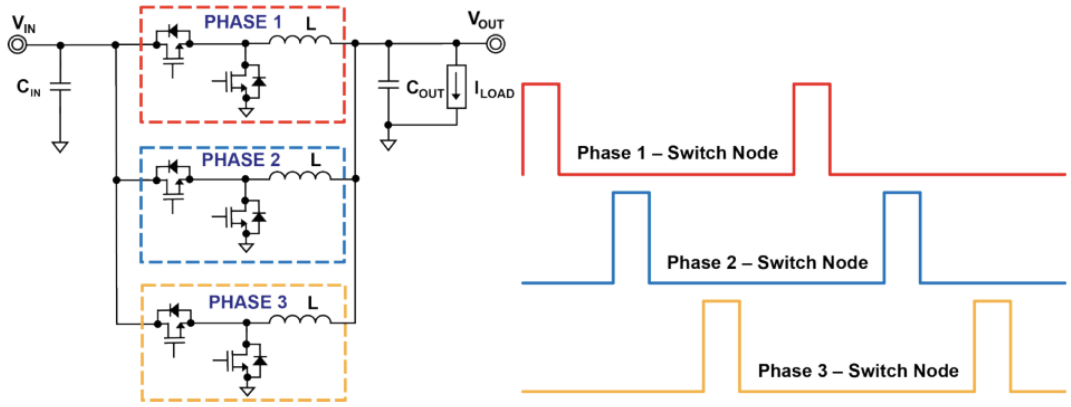
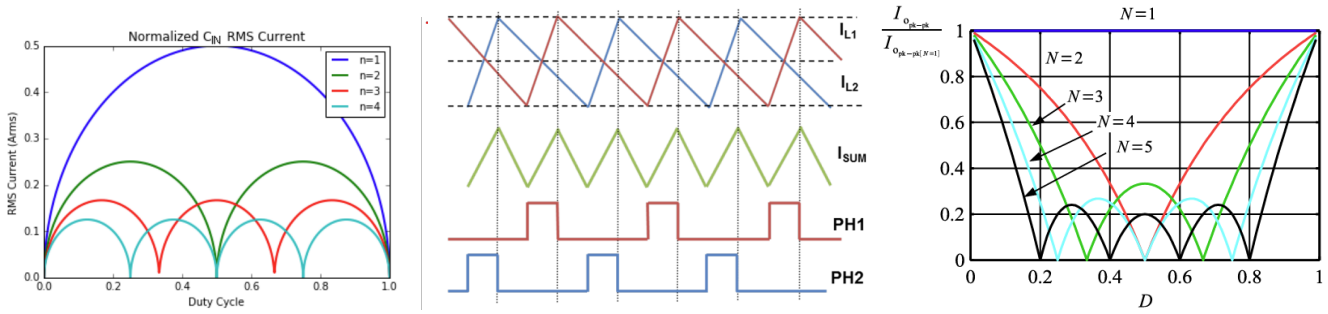


Figure 2 Example of multiphase buck converter



(a) (b) (c)

Figure 3 (a) Normalized Input Capacitance RMS Current (b) Inductor Ripple Current Waveforms (c) Normalized Output Capacitance Ripple

applications, interleaved buck converters can achieve higher power outputs without necessitating disproportionately large components, while also delivering superior dynamic response to load fluctuations. These compelling benefits make interleaved buck converters a pivotal solution in sophisticated power management scenarios where efficiency and compactness are paramount.

OFFLINE SIMULATIONS

Developing model (hardware and software) and verifying theoretical concepts through offline simulations. PLECS software from PLEXIM is used for this.

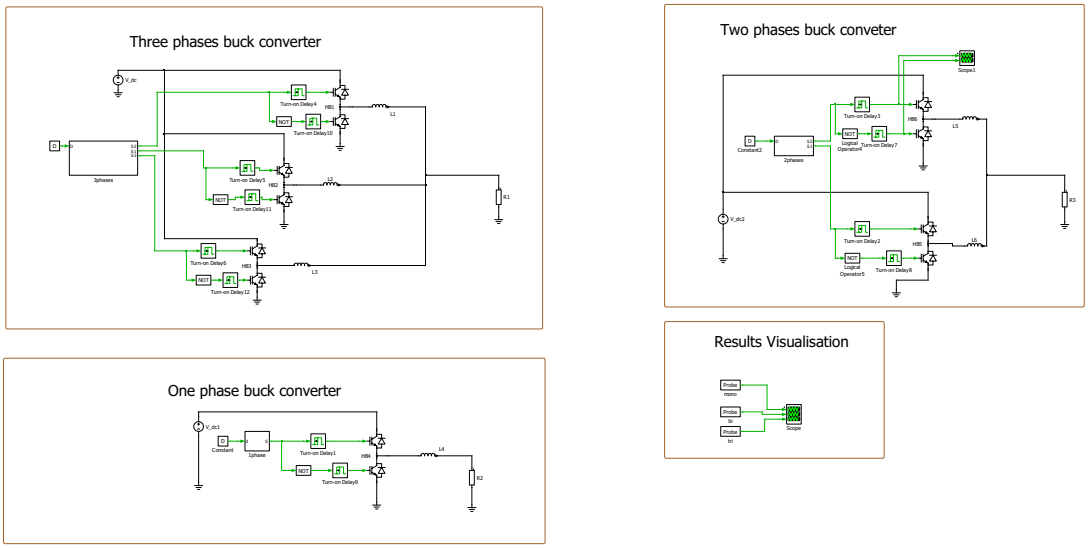


Figure 4 Model for the PLECS offline simulations of 1,2 and 3 interleaved Buck converters

To implement and develop a complete model for the PLECS offline simulation, we created three different circuits of Buck converters: 1, 2 and 3 interleaved Buck converters. The different values of the parameters of the buck converter correspond to the real values of the PETS (e.g., switching frequency of 5kHz, DC source of 630V, inductors of 28mH, 50Ω load …). The IGBTs of the converters are turned on and off using Pulse Width Modulation. This PWM is created by comparing a duty cycle with a triangular wave as shown below in the figure.

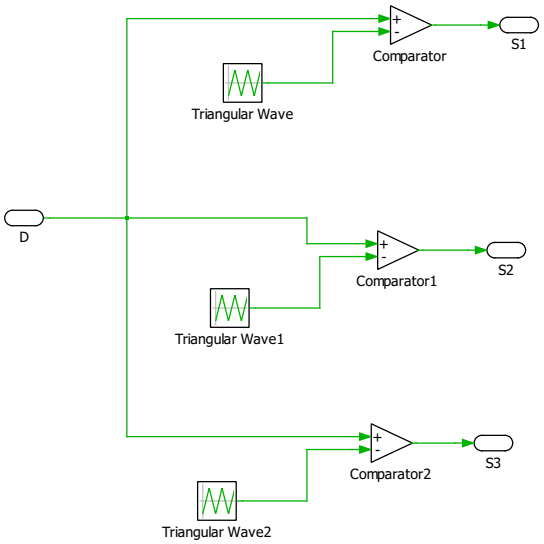


Figure 5 Schematic of PWM creation

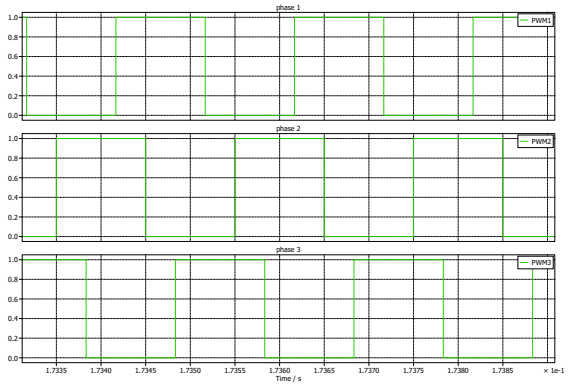


Figure 6 Waveforms of the PWMs for the three phase interleaving Buck with D=0,5

Running the simulation gives us the following results:

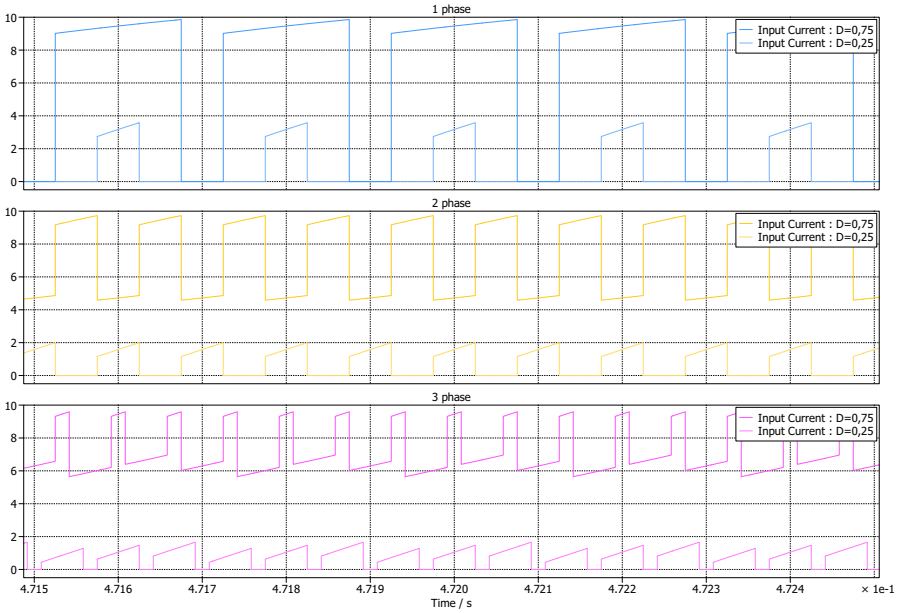


Figure 7 Input current of buck converters

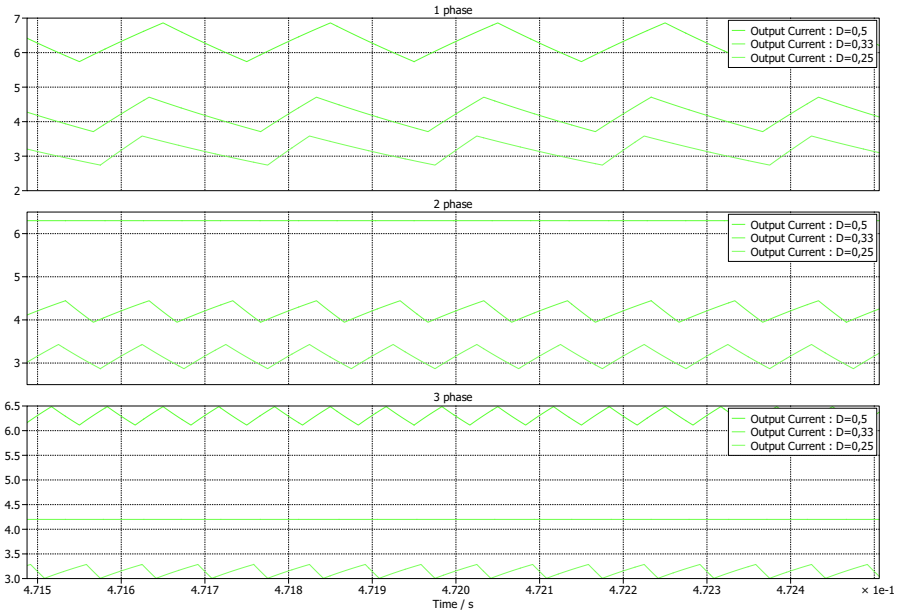


Figure 8 Output current of buck converters

D	1 phase		2 phase		3 phase	
	Output ripple	Input I_RMS	Output ripple	Input I_RMS	Output ripple	Input I_RMS
0.05	0.21	0.14	0.21	0.11	0.19	0.09
0.15	0.57	0.73	0.47	0.52	0.37	0.44
0.25	0.85	1.58	0.56	1.12	0.28	0.93
0.33	1	2.44	0.49	1.72	0	1.44
0.5	1.12	4.51	0	3.16	0.37	3.35
0.66	1	6.9	0.49	5.97	0	5.61
0.75	0.85	8.22	0.56	7.51	0.28	7.2
0.85	0.57	9.98	0.47	9.46	0.37	9.24
0.95	0.21	11.65	0.21	11.51	0.19	11.45

Table 1 Results from the offline simulations

From these results, it can be seen that we are indeed in phase with the theory. When plotting the output currents ripples 9, the resulting waveforms are very similar to the ones shown in 3.

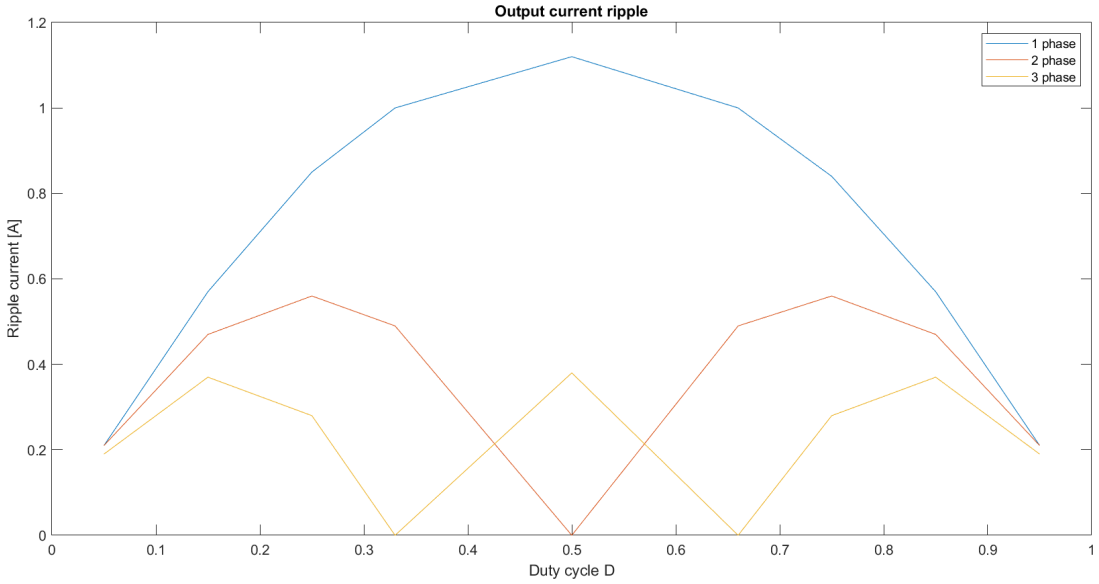


Figure 9 Output currents ripples from offline simulation

Therefore, interleaving buck converters by adding other phases in parallel reduces indeed the output current ripple as low to zero for certain operating conditions. Moreover, as it can be observed in 9 and 1, the maximum ripple is indeed divided by the number of phases interleaved (1.12 to 0.56 to 0.37) as stated in 2.
However, these results come from a circuit that is too idealistic. Indeed, in reality, our PWM signals are not as perfect as in 6. Dead time has to be taken into consideration as switching devices naturally have a delay when turning on and off. Thus, a delay of 2 µs (10^{-2} times the switching period) has been added to the turning on and off of the transistors so that no two transistors are on at the same time, which would cause a short circuit.

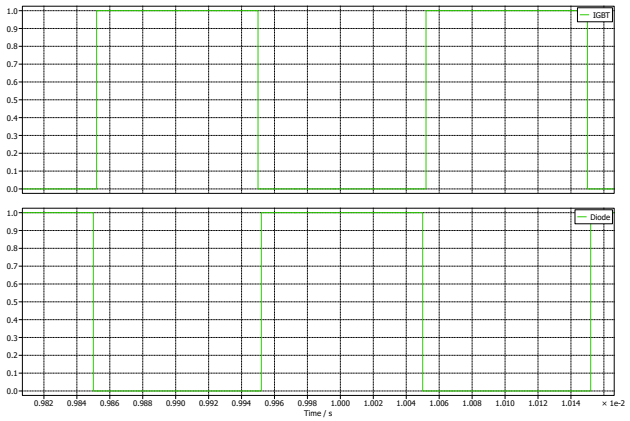


Figure 10 PWM waveforms with dead time delay

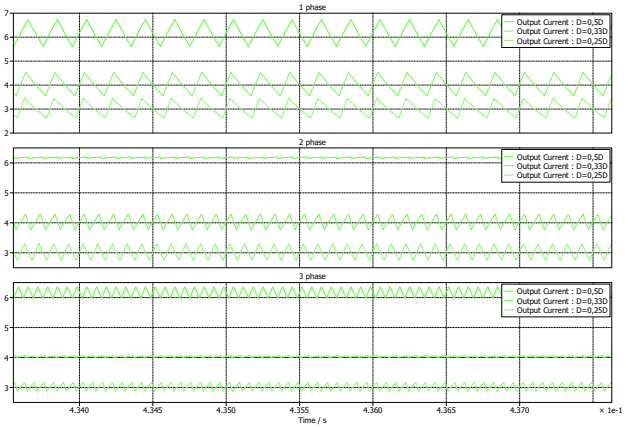


Figure 11 Output Currents with dead time delay

Hence, when adding dead time delay, the more realistic waveforms of PWM look like 10 and very small ripples are observed in the current outputs 11 where there was no ripple at all previously 8. In fact, the results from 2 and 3 express the change in output current ripple and it can be observed that the RMS value of output current is smaller as the converter is on less time.

D	1 phase		2 phase		3 phase	
	without delay	with delay	without delay	with delay	without delay	with delay
0.05	0.21	0.17	0.21	0.17	0.19	0.16
0.15	0.57	0.54	0.47	0.45	0.37	0.36
0.25	0.85	0.82	0.56	0.56	0.28	0.30
0.33	1.00	0.98	0.49	0.52	0.00	0.06
0.50	1.12	1.12	0.00	0.04	0.37	0.37
0.66	1.00	1.02	0.49	0.47	0.00	0.07
0.75	0.85	0.86	0.56	0.56	0.28	0.26
0.85	0.57	0.60	0.47	0.49	0.37	0.37
0.95	0.21	0.25	0.21	0.24	0.19	0.22

Table 2 Output current ripple with and without delay

D	I_RMS without delay	I_RMS with delay
0.05	0.63	0.51
0.15	1.90	1.77
0.25	3.16	3.03
0.33	4.21	4.04
0.50	6.30	6.18
0.66	8.40	8.20
0.75	9.45	9.33
0.85	10.71	10.59
0.95	11.97	11.84

Table 3 RMS utput current value with and without delay

Aditionally, to evaluate the purity of our output signal, we use the Total Harmonic Distortion (THD) which is defined as the ratio of the RMS value of all harmonics to the RMS value of the fundamental component times 100%.

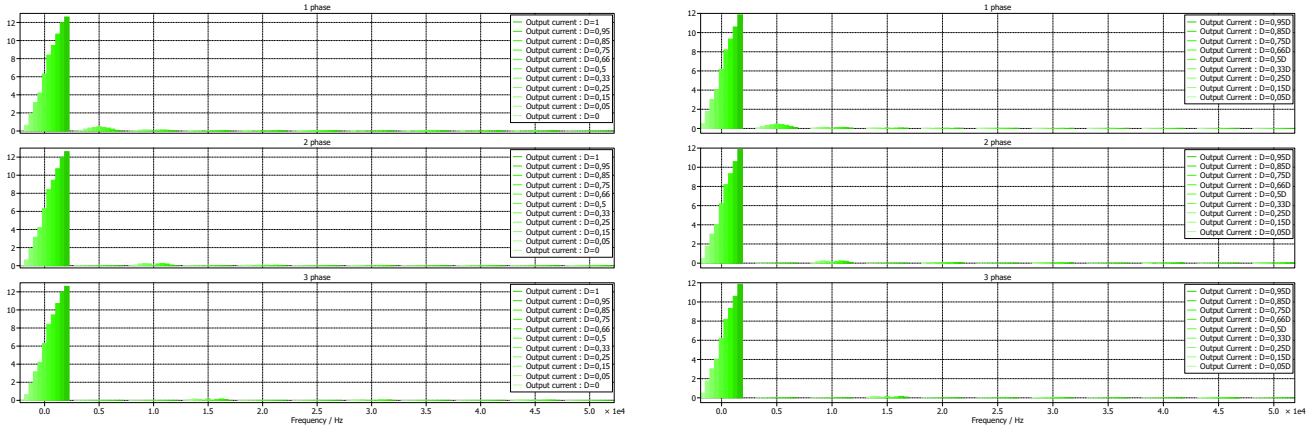
$$THD = \frac{\sqrt{\sum_{n=2}^{\infty} V_n^2}}{V_1} \cdot 100\% \tag{3}$$

where V_n is the amplitude of the nth harmonic and V_1 is the amplitude of the fundamental frequency.

Plotting the Fourier spectrum of output currents gives the results in12. The THDs in 4 are calculated using 12.

D	1 phase		2 phase		3 phase	
	without delay	with delay	without delay	with delay	without delay	with delay
0.05	13.82	13.95	13.08	13.34	12.35	12.73
0.15	12.38	12.52	10.19	10.48	8.00	8.44
0.25	10.92	11.06	7.28	7.57	3.63	4.07
0.33	9.70	9.90	4.85	5.24	0.00	0.56
0.5	7.28	7.42	0.00	0.28	2.42	2.46
0.66	4.85	5.09	2.43	2.35	0.00	0.34
0.75	3.64	3.78	2.43	2.45	1.21	1.12
0.85	2.18	2.33	1.80	1.88	1.41	1.44
0.95	0.73	0.87	0.69	0.82	0.65	0.76

Table 4 Output current THD in percentage (%) with and without delay



(a) (b)

Figure 12 (a) Fourier spectrum of output currents (b) Fourier spectrum of output currents with dead time delay

As a result, it can be noticed that adding phases lowers the THD percentage of the output currents. This means that adding phases helps reducing the distortion (ripples) of the output currents. Furthermore, it can be observed that dead time increases the THD as it increases the output currents ripple. Nevertheless, the duty cycles with which it would be expected to have no ripple at all such as $D = 0.5$ for the two-phase buck and $D = \frac{1}{3}$ or $D = \frac{2}{3}$ for the three-phase buck express very low THD values. Finally, it is worth noticing that THD values decrease the more the duty cycle at which the converter operates increases.

REAL-TIME HIL SIMULATIONS

This step requires programming of the Digital Signal Processor (DSP) from Texas Instruments in order to deploy relevant control algorithms on it. Model of the system to be controlled is developed on the RT-Box from PLEXIM, and typically will be provided already on the RT-Box. In this way complete control algorithm can be verified in a safe manner. Programming of the DSP will be done using the Code Generation option from PLECS, avoiding need for prior knowledge in C-coding.

After successfully programming the digital signal processor from Texas Instruments and modeling the system on the RT-BOX, the following results can be observed 13 14 15 16. Indeed, the results are very similar to the ones from the offline simulation with dead time delay 11. The ripple of the output currents does indeed decrease the more phases are interleaved as it can be seen in 5. Moreover, operating points where the ripple is very close to zero can be noticed in 14 and 15.

Furthermore, it can indeed be observed that THD decreases the more phases are interleaved 6. Moreover, as a consequence of what was said previously, operating points where the THD is very close to 0 percent can be noticed. It is noteworthy that the ripples and THD values of the output current differ from the offline simulations as the used load is not the same.

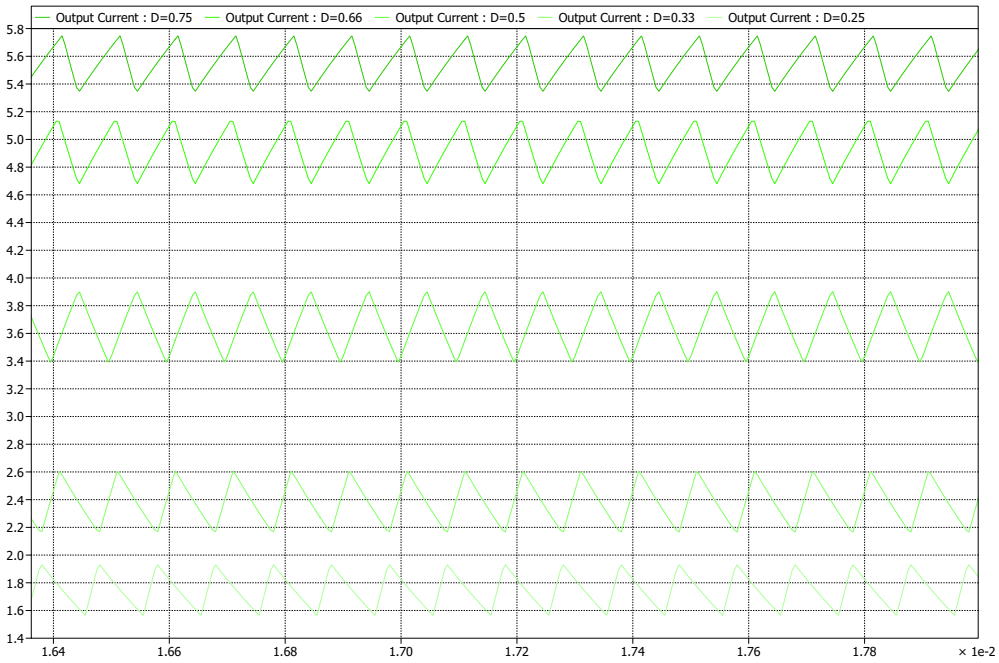


Figure 13 1 phase Buck converter output currents

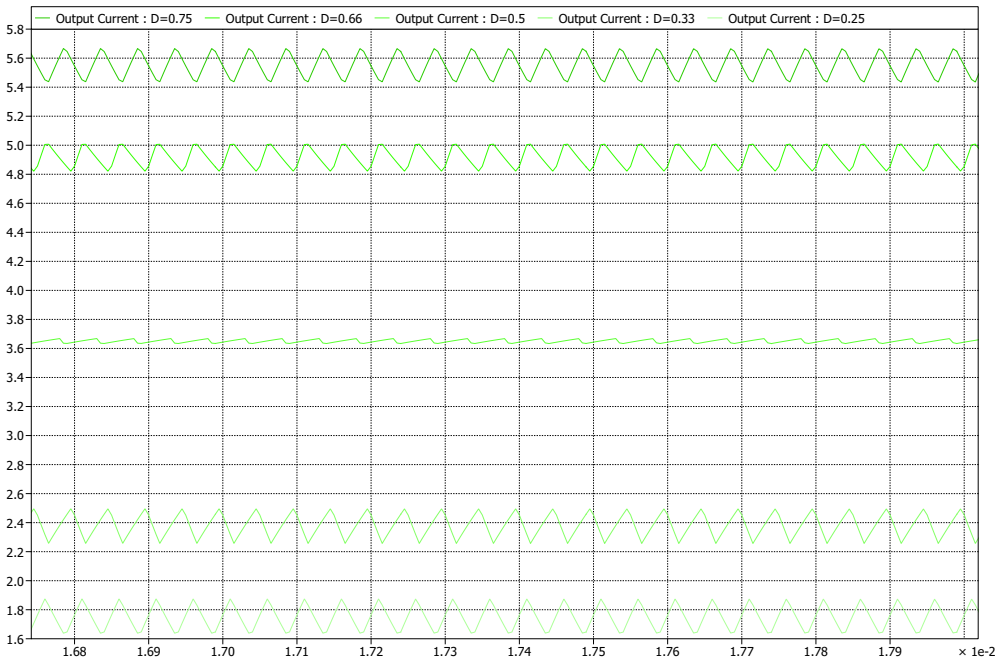


Figure 14 2 phase Buck converter output currents

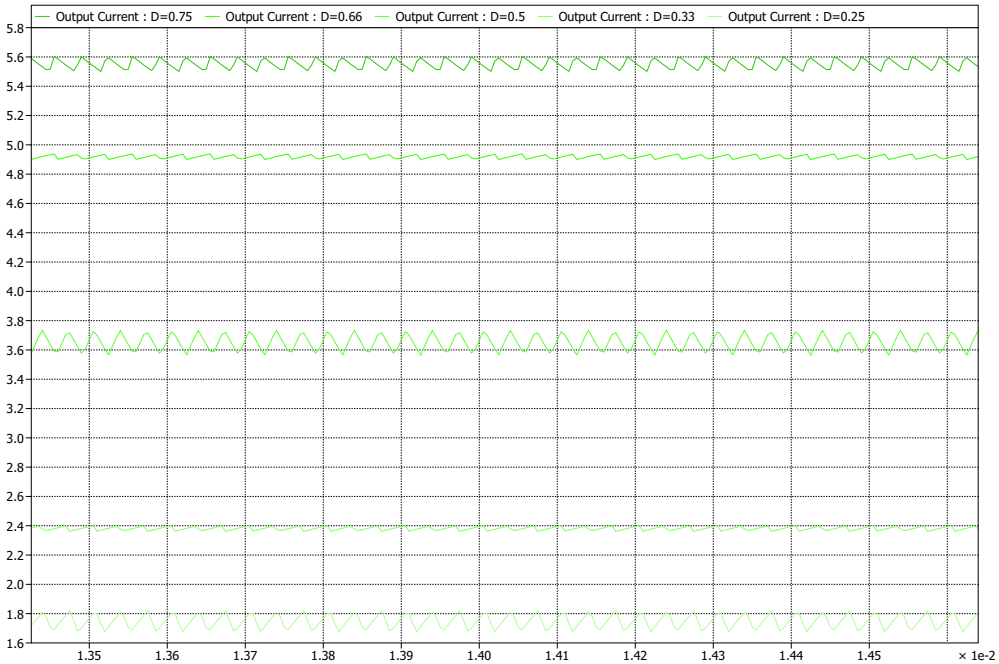


Figure 15 3 phase Buck converter output currents

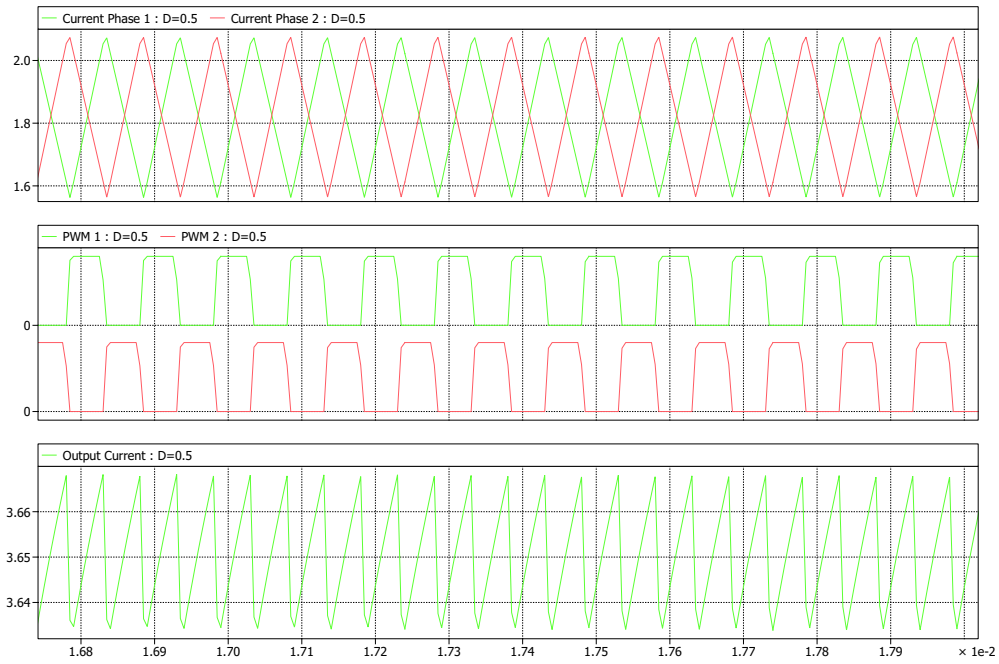


Figure 16 RT-HIL 2 phase Buck converter output current and PWMs at D=0.5

D	1 phase	2 phase	3 phase
0.25	0.37	0.25	0.14
0.33	0.45	0.24	0.04
0.50	0.53	0.04	0.17
0.66	0.48	0.20	0.04
0.75	0.42	0.23	0.10

Table 5 RT-HIL output currents ripples

D	1 phase	2 phase	3 phase
0.25	8.69	5.96	3.22
0.33	7.76	4.15	0.59
0.50	5.87	0.42	1.81
0.66	3.97	1.75	0.28
0.75	3.04	1.86	0.71

Table 6 RT-HIL output currents THD in percentage (%)

EXPERIMENTAL VALIDATION

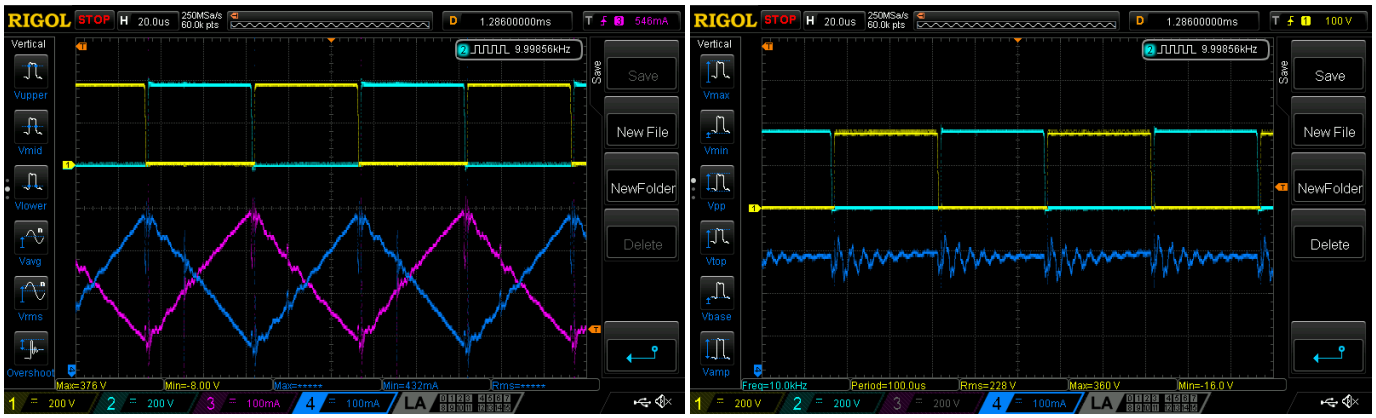
With control software developed in the previous step, experimental verification can be performed, using the same software, on the Power Electronics Teaching Setup (PETS).

In this part, the same DSP code is used to validate the results experimentally on the Power Electronics Teaching Setup (PETS). the results were gathered from an oscilloscope using current and voltage probes 17. The data was then processed using MATLAB giving the results in 18 and 19.

From these results, it can indeed be seen that the theory and previous simulations are validated. As expected, the results are very close to the ones from the RT-HIL simulations. Indeed, it can be observed that the output currents ripple is reduced the more phases are interleaved and that there are operating points where the ripple is approximately zero 7.

Moreover, the THD percentages calculated using the formula 3 and the single-sided Amplitude Spectrum using the fast Fourier transform in MATLAB 19 are also in accordance with the results from Real-Time HIL Simulations. Indeed, the THD percentage decreases the more phases are interleaved and that there are operating points where the THD is very close to 0 percent 8.

It is noteworthy that the current ripples are lower than the ones from the Real-Time HIL Simulations and that the THD values are higher for the single-phase buck but lower for the other two.



(a) PWM and phases currents

(b) PWM and output current

Figure 17 Oscilloscope waveforms of 2 phase interleaved buck converter at D=0.5

D	1 phase	2 phase	3 phase
0.25	0.26	0.16	0.13
0.33	0.30	0.16	0.08
0.50	0.34	0.11	0.11
0.66	0.33	0.16	0.09
0.75	0.30	0.18	0.08

Table 7 Experimental output currents ripples

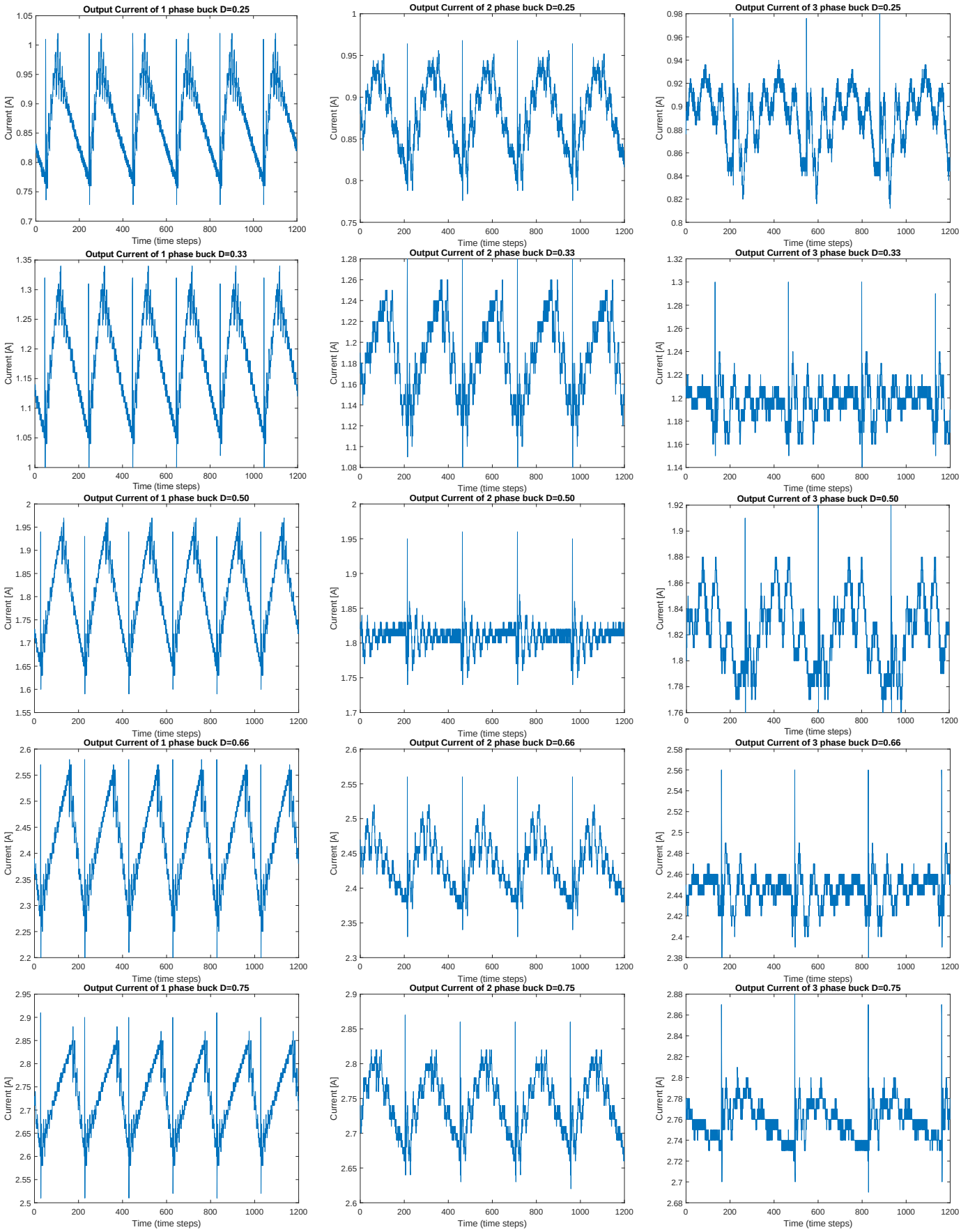


Figure 18 Experimental output Currents

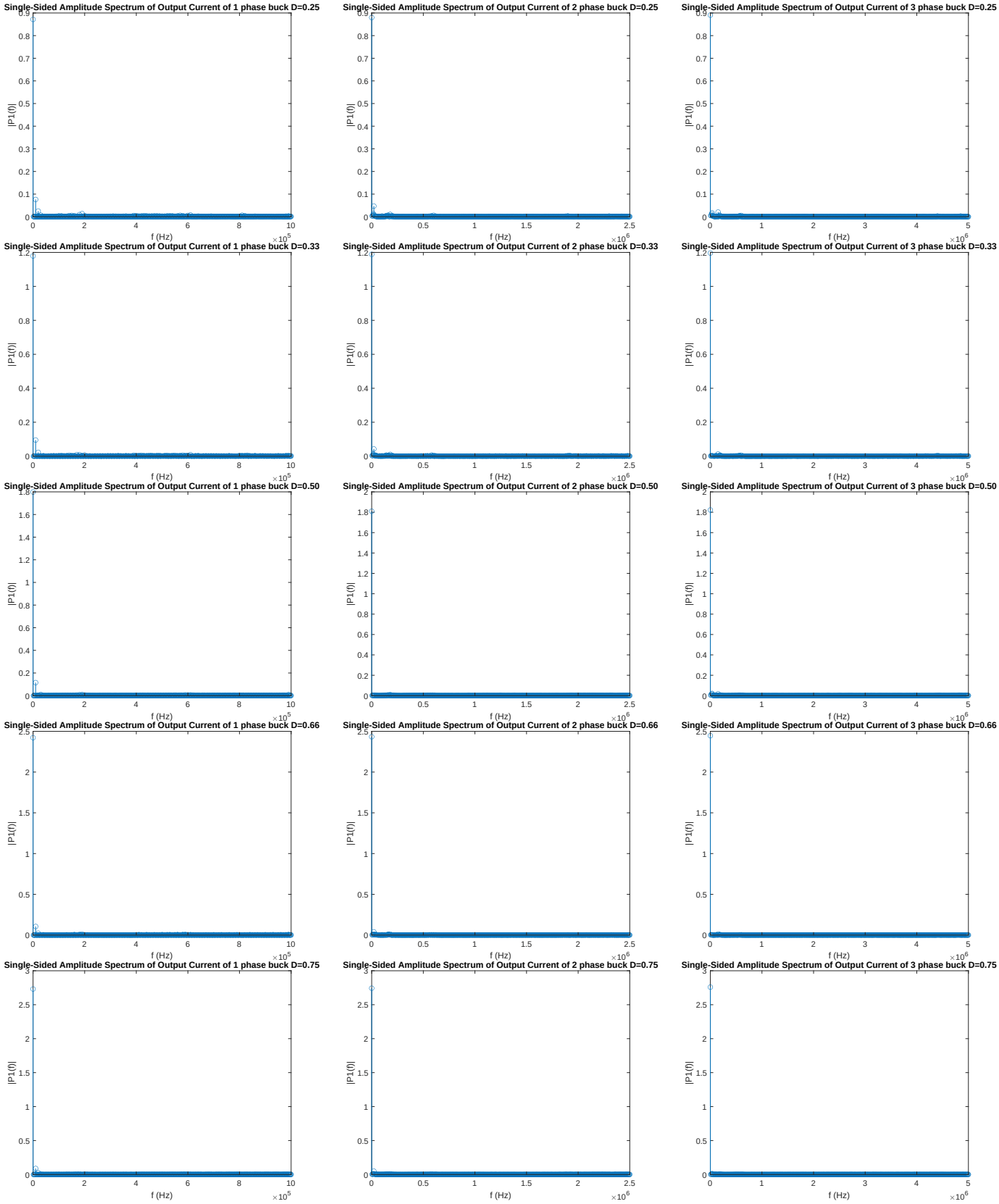


Figure 19 Experimental Single-Sided Amplitude Spectrum of Output currents

D	1 phase	2 phase	3 phase
0.25	9.28	5.40	2.23
0.33	8.31	3.63	0.40
0.50	6.42	0.32	1.34
0.66	4.46	1.65	0.24
0.75	3.41	1.82	0.56

Table 8 Experimental output currents THD in percentage (%)

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