Traffic Light Controller

-Using Verilog

For a Four way Junction

Overview & Key Features:

- The Verilog Traffic Light Controller is designed to manage the traffic lights at an intersection between a main road and a side road. The controller operates based on the presence of vehicles or pedestrians on the side road, detected by a sensor, and predefined timing parameters for green, yellow, and red light durations.

Key Features:

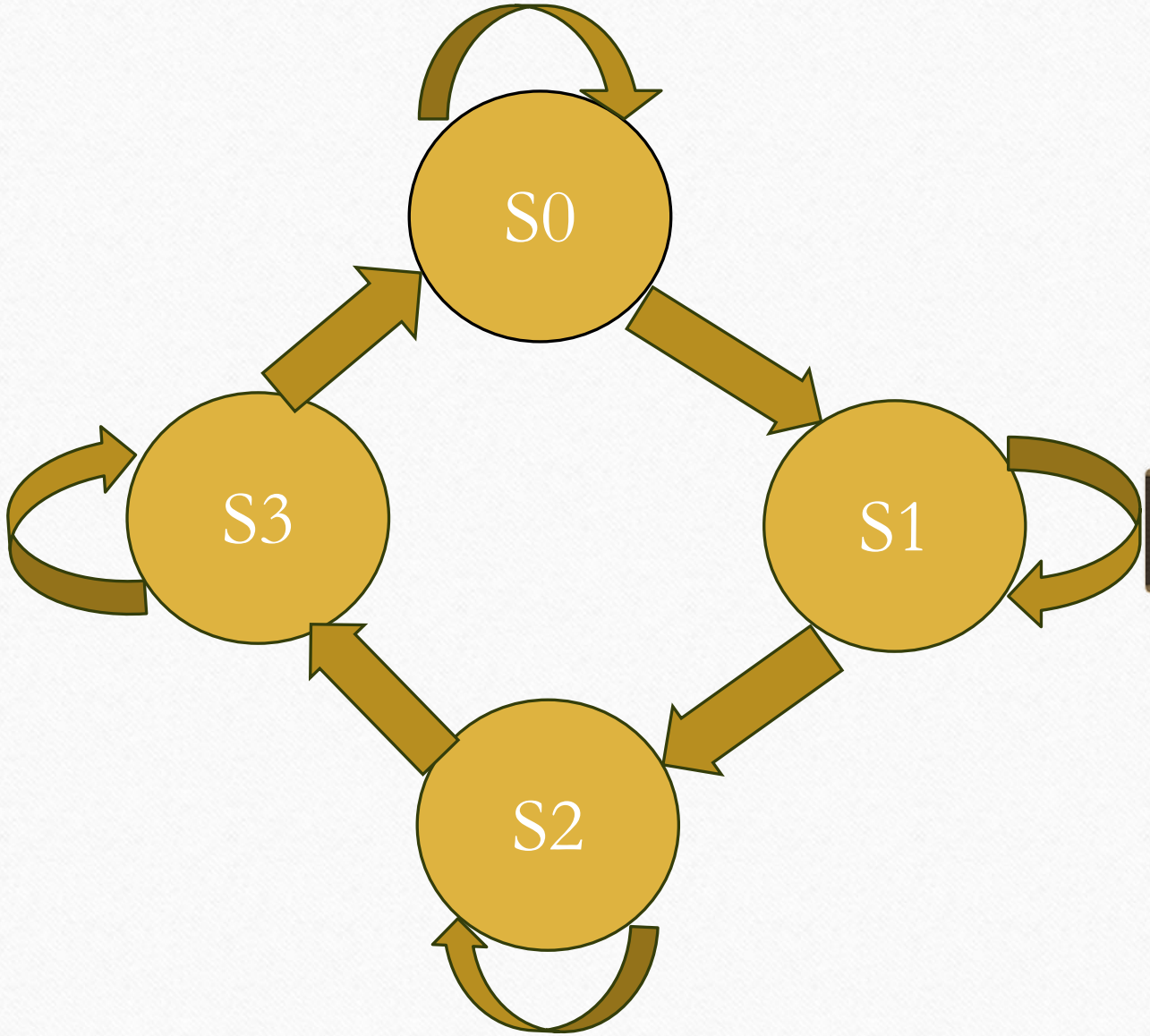
- **Sensor Input**: Detects vehicles or pedestrians on the side road.
- **State Machine**: Uses a finite state machine (FSM) to control the traffic lights.
- **Timing Parameters**: Configurable durations for green, yellow, and red lights.
- **Output Signals**: Controls the traffic lights for both the main road and the side road.

States:

S0: Main road is green, side road is red.
S1: Main road is yellow, side road is red.
S2: Main road is red, side road is green.
S3: Main road is red, side road is yellow.

Timing Parameters:

- **TL (Time for Main Road Green Light)**: Duration for which the main road light remains green.(10 secs)
- **TS (Time for Side Road Green Light)**: Duration for which the side road light remains green.(6 secs)
- **TY (Time for Yellow Light)**: Duration for which the yellow light remains on both roads.(4 secs)



State Transition Logic &Output Logic:

State Transitions:

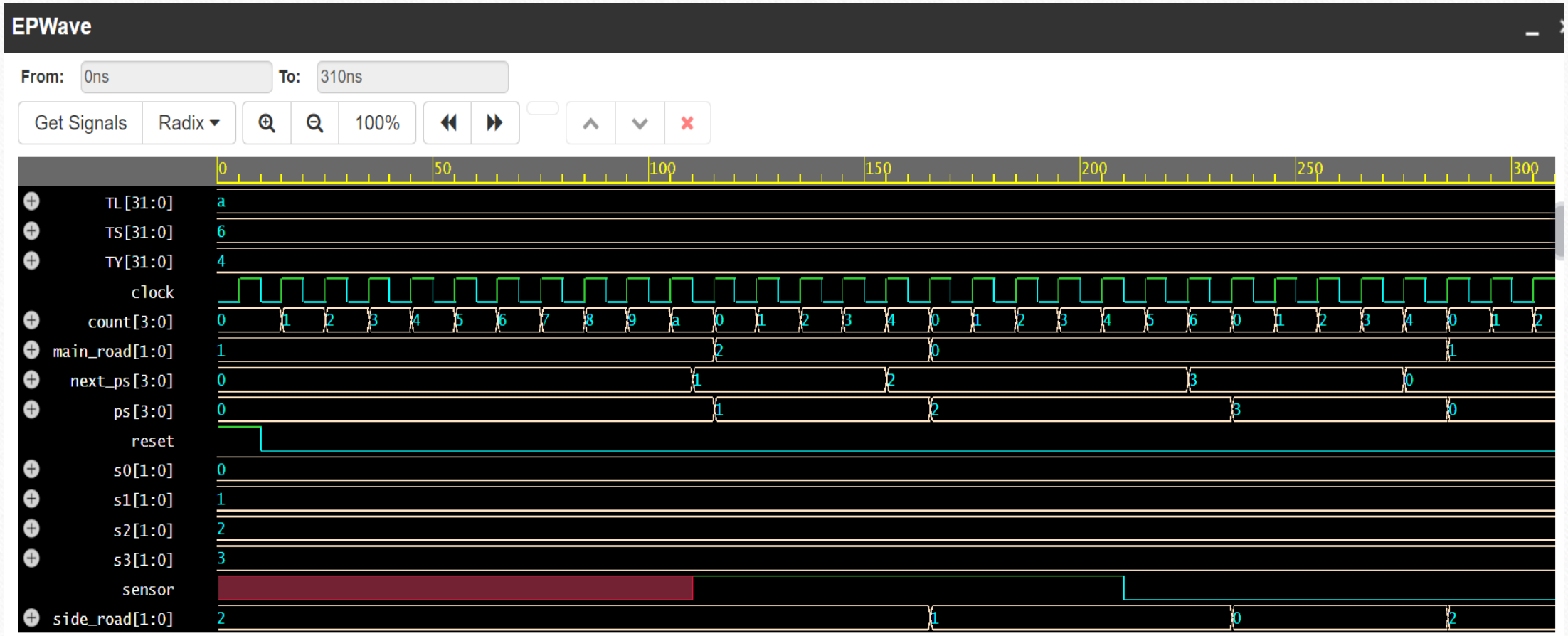
•Transition from s0 to s1 when the main road green light duration (TL) expires and a vehicle is detected on the side road.
•Transition from s1 to s2 after the main road yellow light duration (TY) expires.
•Transition from s2 to s3 after the side road green light duration (TS) expires.
•Transition from s3 to s0 after the side road yellow light duration (TY) expires.

- **Output Logic:**

The output logic determines the state of the traffic lights on the main road and side road based on the current state of the FSM. The traffic lights are controlled using 2-bit signals:
main_road and *side_road* use 2-bit signals to represent the light colors:

  - 00: Red
  - 01: Green
  - 10: Yellow

Simulation Result:



Conclusion & Tools Used:

- The Verilog Traffic Light Controller project demonstrates a practical application of finite state machines (FSM) to manage traffic lights at an intersection. By leveraging sensor inputs and configurable timing parameters, the controller efficiently directs traffic flow between a main road and a side road.
- Tools Used:
  - Vivado Software,
  - EDA Play Ground.