SASTRA DEEMED UNIVERSITY

Course code: ECE316 **Course Name: Digital VLSI Design**

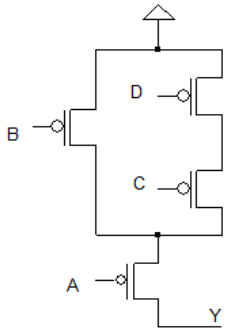
CIA III - June 2022

Answer Key

PART A

1.Saturation region

2.



3. $1/\alpha^3$

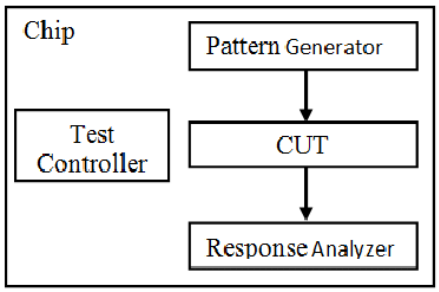
4. Latch up is a condition in which the parasitic components give rise to the establishment of low resistance conducting paths between VDS and VSS with disastrous results.
Remedies are [i] an Increase in substrate doping levels with a consequent drop in the value of Rs[ii]Reducing Rp by control of fabrication parameters and by ensuring low contact resistance to Vss [iii]Introduction of Guard Rings

5. Lambda rule specify the layout constraints such as minimum feature sizes and minimum allowable feature separations are stated in terms of a single parameter (λ) and thus allow linear, proportional scaling of all geometrical constraints.

6. controllability-ability to apply test patterns to the inputs of a subcircuit via the primary input of the circuit; observability-observe the response of a subcircuit via primary outputs

7. Bridging faults occur when a short develops between two unconnected signal lines of a logic gate.

8.

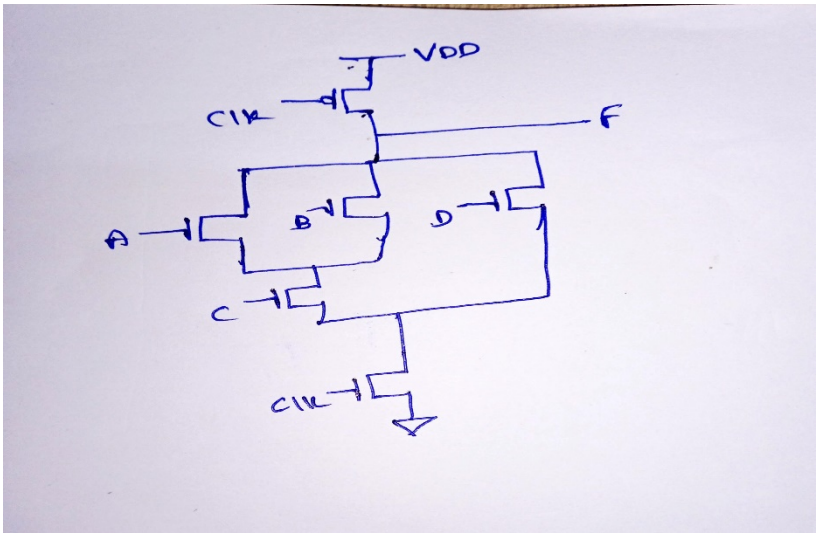


9.Flexibility, Decreased latency, Parallelism, Energy Efficiency etc.

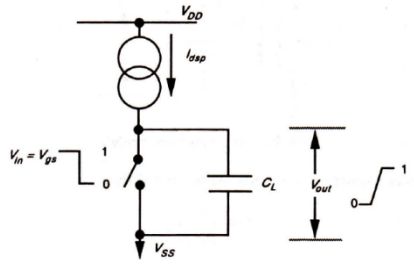
10. JTAG (Joint Test Action Group) is an industry standard for verifying designs and testing printed circuit boards after manufacture. JTAG implements standards for on-chip instrumentation in electronic design automation (EDA) as a complementary tool to digital simulation.

Part B

11.a



11.b.



$$\tau_r = \frac{2V_{DD}C_L}{\beta_p(V_{DD} - |V_{tp}|)^2}$$

with $|V_{tp}| = 0.2V_{DD}$, then

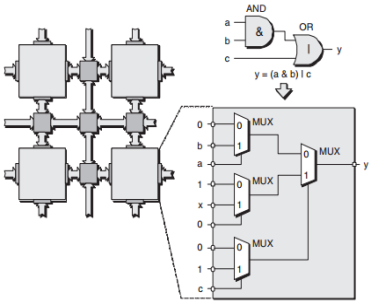
$$\tau_r \doteq \frac{3C_L}{\beta_p V_{DD}}$$

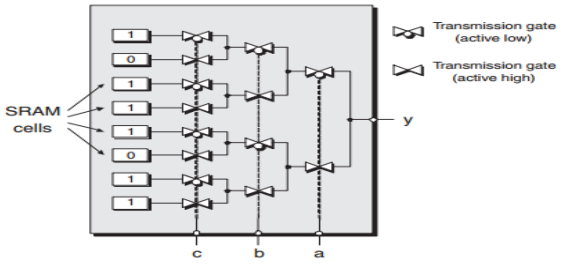
12. Pattern is 0011 / x1'x2'x3 x4

13. MUX-based approach, consider one way in which the 3-input function $y = (a \,\&\, b) \mid c$ could be implemented using a block containing only multiplexers

LUT based approach: A group of input signals is used as an index (pointer) to a lookup table. The contents of this table are arranged such that the cell pointed to by each input combination contains the desired value.

Any one example like y = (a. b) + c





Part C

14.a. The hot electron (or short channel) effect is described in as occurring when a high voltage Is applied across the source and drain of a device, the electric field is high, and the electrons are accelerated in the channel.

b. The test generation process consists of three steps:

Step 1. Select a pdcf for the given fault.

Step 2. Drive the D (or D') from the output of the gate under test to an output of the circuit

by successively intersecting the current test cube with the propagation D-cubes of successive gates. A test cube represents the signal values at various lines in the circuit during each step of the test generation process. The intersection of a test cube with the propagation D-cube of a successor gate results in a test cube.

Step 3. Justify the internal line values by driving back toward the inputs of the circuit, assigning input values to the gates so that a consistent set of circuit input values may be obtained.

c. Read Only Memory (ROM) refers to memory in a digital system that has only read capabilities. Can be used to perform logic operations.

Random Access Memory (RAM) refers to memory in a digital system that has both read and write capabilities. Mostly it's a high-speed temporary storage memory.

Static RAM (SRAM) is able to store its information as long as power is applied, and it does not lose the data during a read cycle (early memory was mostly SRAM)

Dynamic RAM (DRAM) uses a capacitor to temporarily store data which must be refreshed periodically to prevent information loss, and the data is lost in most DRAMs during the read

cycle

SRAM takes approximately four times the silicon area of DRAM with the same technology.