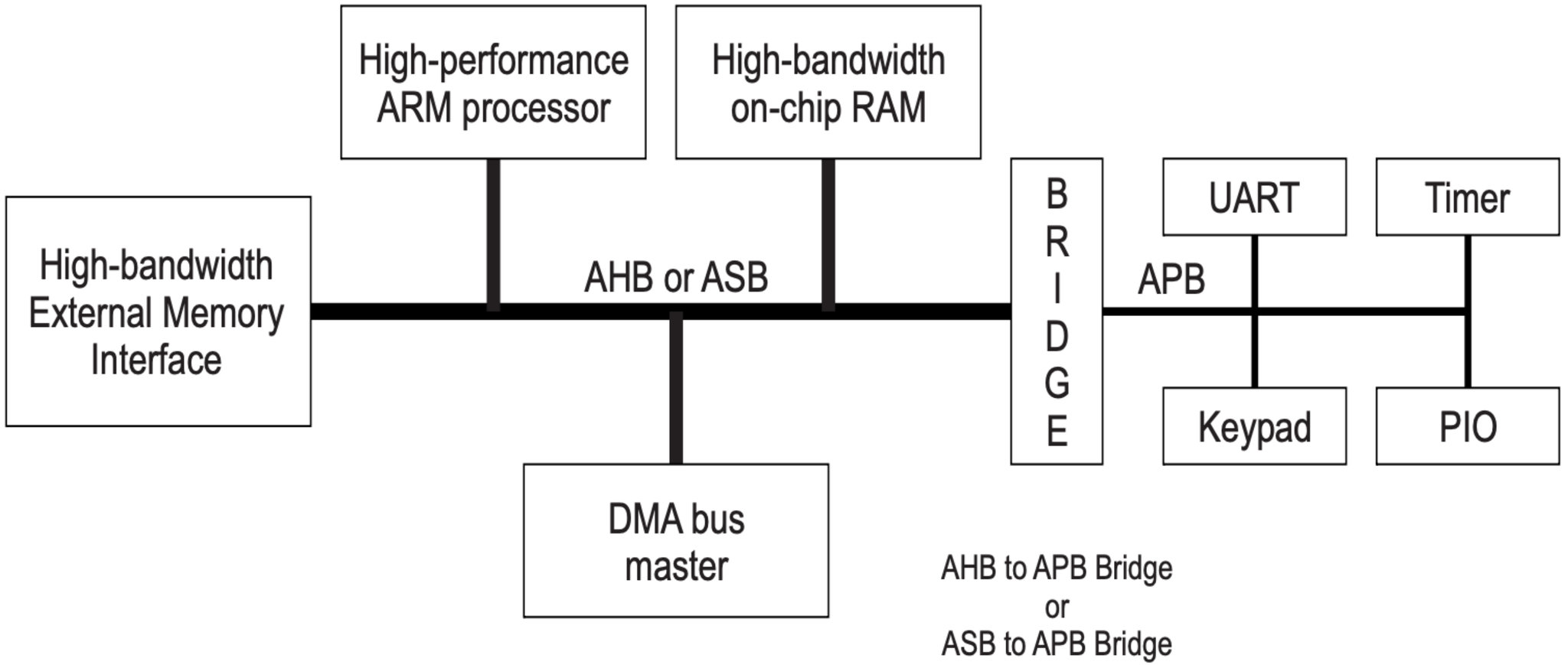
AMBA PROTOCOLS

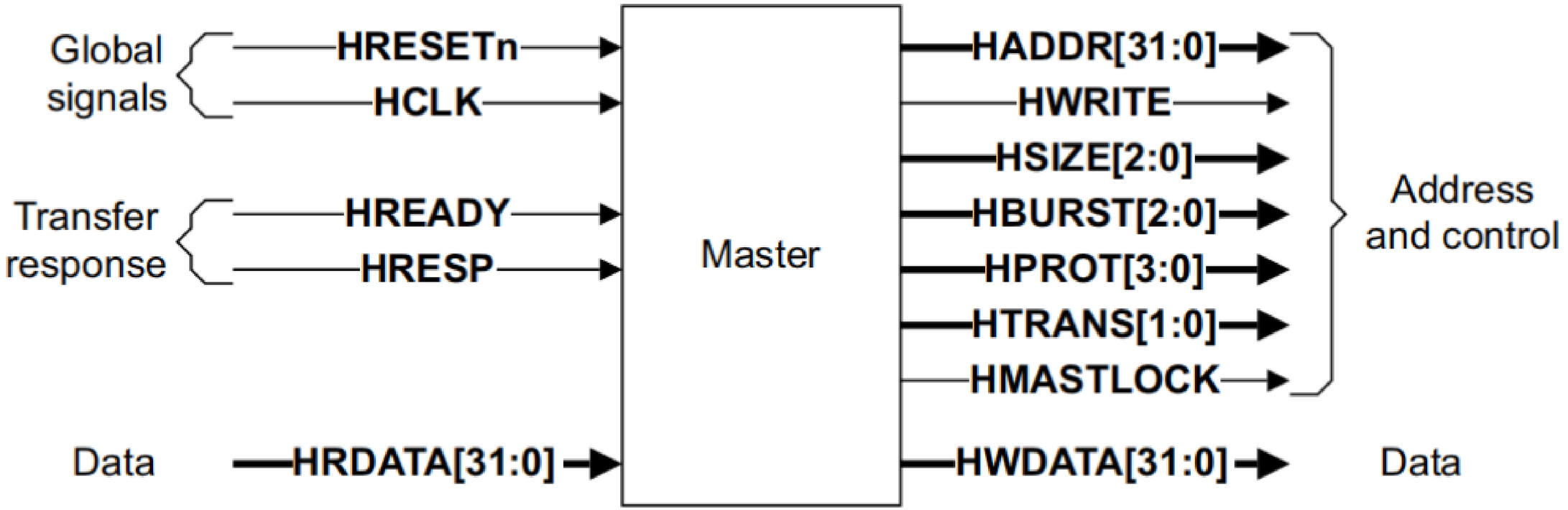
AHB to APB Bridge

AHB TO APB BRIDGE

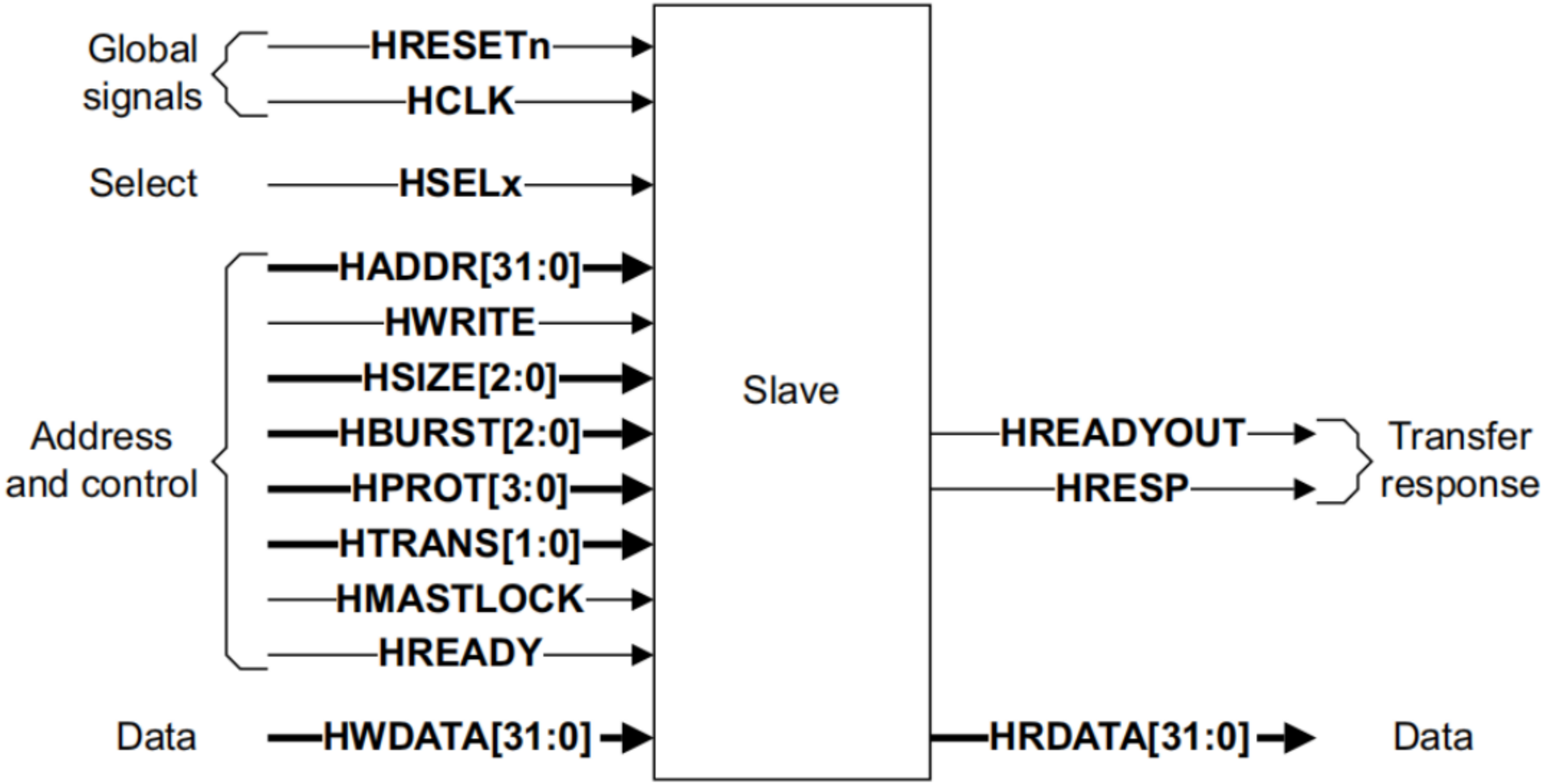


AHB to APB Bridge
or
ASB to APB Bridge

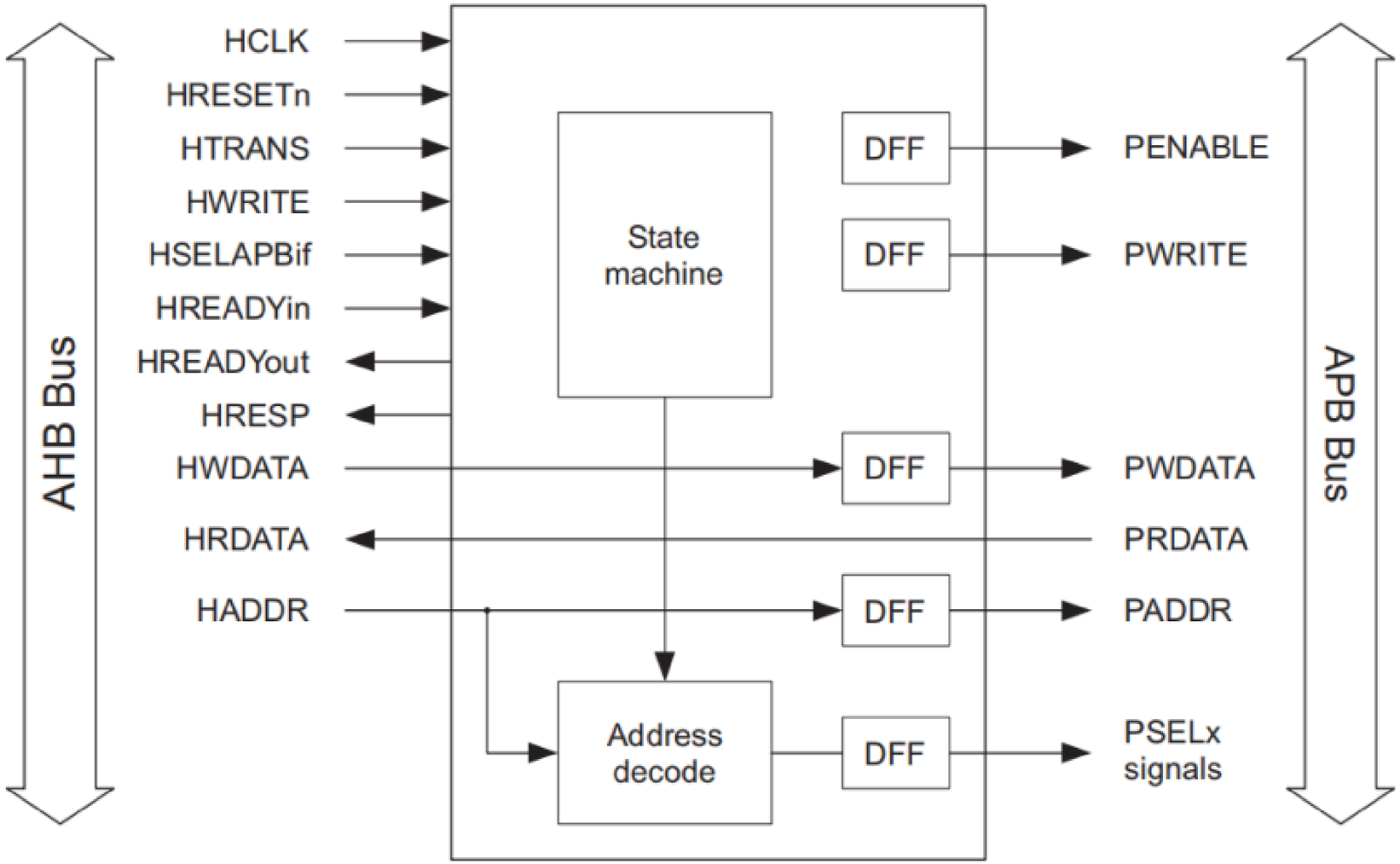
AHB MASTER INTERFACE



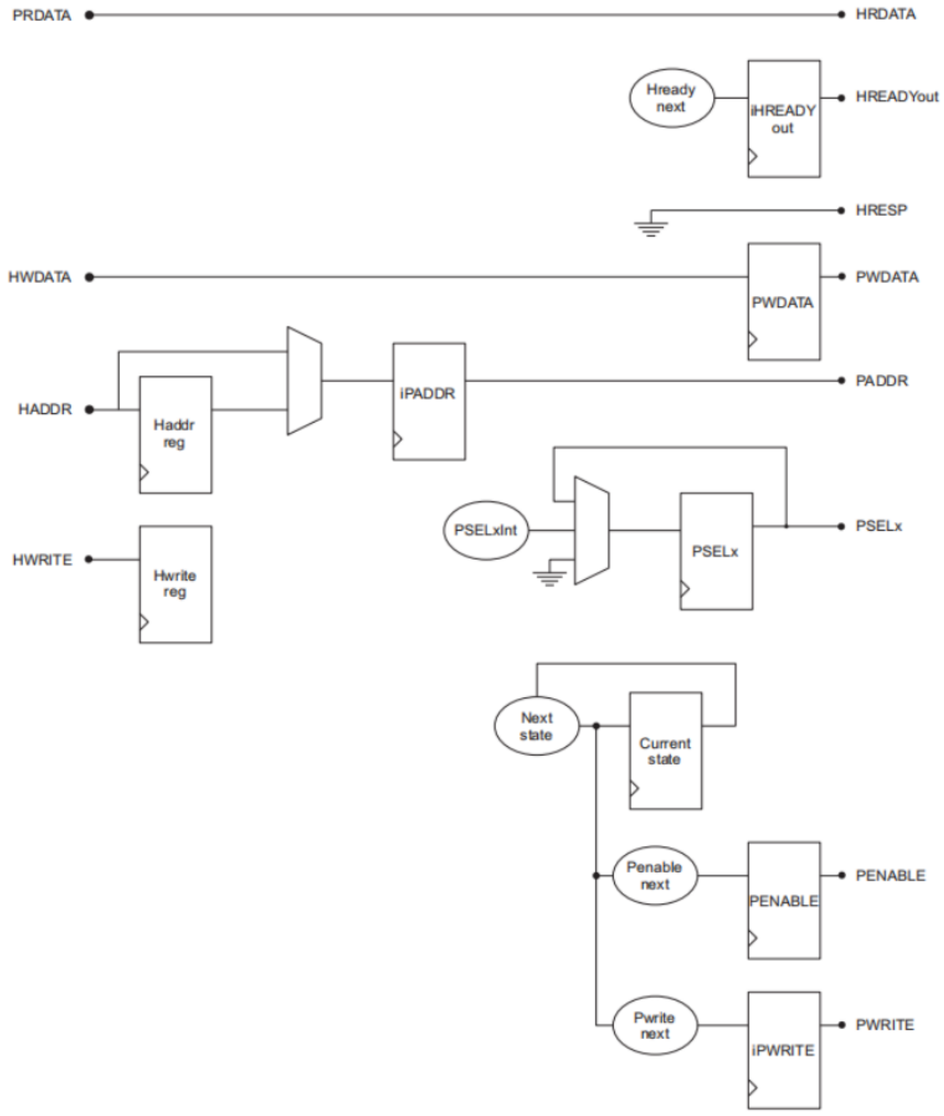
AHB SLAVE INTERFACE



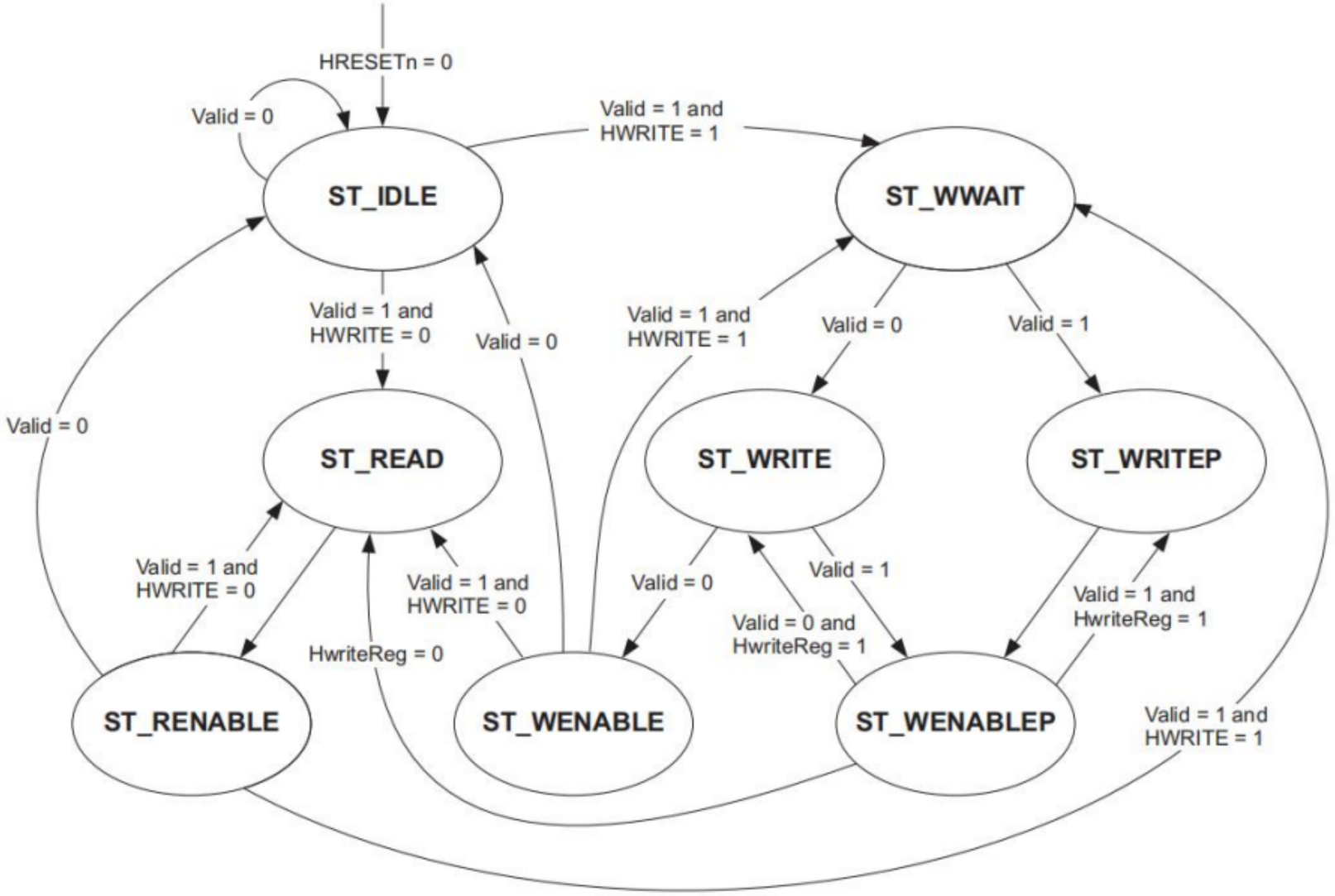
ARCHITECTURE



BRIDGE MODULE



AHB TO APB TRANSFER STATE MACHINE



ST_IDLE :-

During this state the APB buses and PWRITE are driven with the last values they had and PSEL and PENABLE lines are driven LOW.

The ST_IDLE state is entered from:

• reset, when the system is initialized

• ST_RENABLE, ST_WENABLE, or ST_IDLE, when there are no peripheral transfers to perform.

The next state is:

• ST_READ, for a read transfer, when the AHB contains a valid APB read transfer

• ST_WWAIT, for a write transfer, when the AHB contains a valid APB write transfer.

ST_READ :-

During this state the address is decoded and driven onto PADDR, the relevant PSEL line is driven HIGH, and PWRITE is driven LOW.

A wait state is always inserted to ensure that the data phase of the current AHB transfer does not complete until the APB read data has been driven onto HRDATA.

The ST_READ state is entered from ST_IDLE, ST_RENABLE, ST_WENABLE, or ST_WENABLEP during a valid read transfer. The next state will always be ST_RENABLE.

ST_WWAIT

This state is needed due to the pipelined structure of AHB transfers, to allow the AHB side of the write transfer to complete so that the write data becomes available on HWDATA. The APB write transfer is then started in the next clock cycle. The ST_WWAIT state is entered from ST_IDLE, ST_RENABLE, or ST_WENABLE, during a valid write transfer. The next state will always be ST_WRITE

ST_WRITE :-

During this state the address is decoded and driven onto PADDR, the relevant PSEL line is driven HIGH, and PWRITE is driven HIGH. A wait state is not inserted, as a single write transfer can complete without affecting the AHB. The ST_WRITE state is entered from:

- ST_WWAIT, when there are no further peripheral transfers to perform
- ST_WENABLEP, when the currently pending peripheral transfer is a write, and there are no further transfers to perform. The next state is:
- ST_WENABLE, when there are no further peripheral transfers to perform
- ST_WENABLEP, when there is one further peripheral write transfer to perform.

ST_WRITEP :-

During this state the address is decoded and driven onto PADDR, the relevant PSEL line is driven HIGH, and PWRITE is driven HIGH. A wait state is always inserted, as there must only ever be one pending transfer between the currently performed APB transfer and the currently driven AHB transfer. The ST_WRITEP state is entered from:

- ST_WWAIT, when there is a further peripheral transfer to perform.
- ST_WENABLEP, when the currently pending peripheral transfer is a write, and there is a further transfer to perform. The next state will always be ST_WENABLEP.

ST_RENABLE :-

During this state the PENABLE output is driven HIGH, enabling the current APB transfer. All other APB outputs remain the same as the previous cycle. The ST_RENABLE state is always entered from ST_READ.

- ST_READ, when there is a further peripheral read transfer to perform.
- ST_WWAIT, when there is a further peripheral write transfer to perform.
- ST_IDLE, when there are no further peripheral transfers to perform.

ST_WENABLE :-

During this state the PENABLE output is driven HIGH, enabling the current APB transfer. All other APB outputs remain the same as the previous cycle. The ST_WENABLE state is always entered from ST_WRITE.

The next state is:

- ST_READ, when there is a further peripheral read transfer to perform.
- ST_WWAIT, when there is a further peripheral write transfer to perform.
- ST_IDLE, when there are no further peripheral transfers to perform.

ST_WENABLEP :-

A wait state is inserted if the pending transfer is a read because, when a read follows a write, an extra wait state must be inserted to allow the write transfer to complete on the APB before the read is started. The ST_WENABLEP state is entered from:

- ST_WRITE, when the currently driven AHB transfer is a peripheral transfer.
- ST_WRITEP, when there is a pending peripheral transfer following the current write.

The next state is:

- ST_READ, when the pending transfer is a read.
- ST_WRITE, when the pending transfer is a write, and there are no further transfers to perform.
- ST_WRITEP, when the pending transfer is a write.

BRIDGE FUNCTIONAL DESCRIPTION

APB output signal generation :

The generation of all APB output signals is based on the status of the transfer state machine:

• PWDATA is a registered version of the HWDATA input, which is only enabled during a write transfer. As the bridge is the only bus master on the APB, then it can drive PWDATA continuously.

• PENABLE is only set HIGH during one of three enable states, in the last cycle of an APB transfer. A register is used to generate this output from the next state of the transfer state machine.

BRIDGE FUNCTIONAL DESCRIPTION

APB output signal generation :

• PSELx outputs are decoded from the current transfer address. They are only valid during the read, write and enable states, and are all driven LOW at all other times so that no peripherals are selected when no transfers are being performed.

•PADDR is a registered version of the currently selected address input (HADDR or the address register) and only changes when the read and write states are entered at the start of the APB transfer.

• PWRITE is set HIGH during a write transfer, and only changes when a new APB transfer is started. A register is used to generate this output from the next state of the transfer state machine.

BRIDGE FUNCTIONAL DESCRIPTION

APB output signal generation :

• The APBen signal is used as an enable on the PSEL, PWRITE and PADDR output registers, ensuring that these signals only change when a new APB transfer is started, when the next state is ST_READ, ST_WRITE, or ST_WRITEP.

BRIDGE FUNCTIONAL DESCRIPTION

AHB output signal generation :

HRDATA is directly driven with the current value of PRDATA. APB slaves only drive read data during the enable phase of the APB transfer, with PRDATA set LOW at all other times, so bus clash is avoided on HRDATA (assuming OR bus connections for both the AHB and APB read data buses).

• HREADYout is driven with a registered signal to improve the output timing. Wait states are inserted by the APB bridge during the ST_READ and ST_WRITEP states, and during the ST_WENABLEP state when the next transfer to be performed is a read.

• HRESP is continuously held LOW, as the APB bridge does not generate SPLIT, RETRY or ERROR responses.

AHB TO APB SCHEMATIC