Power control (PWR) RM0456

The table below shows the power modes overview.

Table 99. Low-power mode summary

Mode name	Entry	Wake-up source ⁽¹⁾	Wake-up system clock	Effect on clocks	Voltage regulators
Sleep (Sleep-now or Sleep-on-exit)	WFI or Return from ISR	Any interrupt except OTG_FS, USB, and UCPD in range 4 – OTG_HS in range 3 and 4	Same as before entering Sleep mode	CPU clock OFF No effect on other clocks or analog clock sources	Range 1, 2, 3, 4
	WFE	Wake-up event			
Stop 0	LPMS = 000 + SLEEPDEEP bit + WFI or Return from ISR or WFE	Any EXTI line (configured in the EXTI registers) Specific peripherals events/interrupts (2)	HSI16 when STOPWUCK = 1 in RCC_CFGR1 MSIS with the frequency before entering the Stop mode, limited to 24 MHz, when STOPWUCK = 0	All clocks OFF except LSI and LSE MSIK, MSIS, or HSI16 can be enabled temporarily when requested by an autonomous peripheral, or forced to be kept enabled.	Range 1, 2, 3, 4
Stop 1	LPMS = 001 + SLEEPDEEP bit + WFI or Return from ISR or WFE				
Stop 2	LPMS = 010 + SLEEPDEEP bit + WFI or Return from ISR or WFE				Low-power regulator (SMPS or LDO)
Stop 3	LPMS = 011 + SLEEPDEEP bit + WFI or Return from ISR or WFE	WKUP pin edge, RTC/TAMP events/interrupts ⁽²⁾ , external reset in NRST pin, IWDG reset		All clocks OFF except LSI and LSE	
Standby with SRAM2_ 8 Kbytes	LPMS = 10x+ RRS1 = 1 + SLEEPDEEP bit + WFI or Return from ISR or WFE		MSIS from 1 MHz up to 4 MHz		
Standby with SRAM2_Full	LPMS = 10x+ RRS1 = RRS2 = 1+ SLEEPDEEP bit + WFI or Return from ISR or WFE				
Standby	LPMS = 10x + RRS1 = RRS2 = 0 + SLEEPDEEP bit + WFI or Return from ISR or WFE				OFF
Shutdown	LPMS = 11x + SLEEPDEEP bit + WFI or Return from ISR or WFE	WKUP pin edge, RTC/TAMP events/interrupts (2), external reset in NRST pin	MSIS 4 MHz	All clocks off except LSE	OFF

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