jb8855

Midterm 1, October 1st 2024

Maximum time: 140 minutes : **5:00 PM - 7:20 PM**

- Midterm 1 Format: Closed Book, Up to 10 'Cheat Sheets' using both sides allowed
- No Communications with anyone permitted using any device. Use of a Laptop/Mobile device etc. during the Exam is not allowed.
- Please place your mobile device/iPad/Tablet/Laptop in your backpack before you begin working on the Exam.
- You may use a laptop/mobile only after you complete the Exam: to take pictures of each page of your Examination Blue Book and upload the PDF of these pages to Brightspace
- Use of calculators are allowed.
- The Midterm I hard copy will be released in Class at 5 PM and not online. Please read instructions below on uploading your completed Midterm I solutions with all work shown in steps – to get any credit
- Instructor/CAs available in classroom if you have questions on the Midterm, during the Exam
- You will be provided an Examination Blue Book. Please bring with you a Pen/Pencil & Eraser
- Please write down your solutions in the Examination Blue Book, single-sided with (i) your name, netID, Course number printed on the cover sheet (ii) Page Number and Problem number identified clearly on each sheet. Please use a separate sheet for each Problem/Problem part
- Please stop working on your Midterm at 7:20 PM – you have 10 minutes to scan/take pictures of each sheet and upload them as completed PDF assignment on NYU Brightspace by 7:30 PM – you may use any of several smartphone apps to integrate your scans/pictures of sheets into a PDF file.
- Please be sure to check you have all pictures of pages you use in the Examination Blue Book - in the same order as they appear in the Examination notebook
- Portal will close at 7:30 PM sharp not allowing upload of your Midterm after this time
- This Midterm has 5 problems, most with multiple parts. Please attempt all of them. Please show all work. Please write legibly

1. Assume three processors P1, P2 and P3 have average CPIs of 1,2 & 3 for a given benchmark. Their architects have a common CMOS heat removal efficiency-imposed limitation on maximum clock frequency of 5GHz.

(a) What ratio should the number of instructions of the benchmark in P1, P2 and P3 be to execute the benchmark at maximum clock frequency of 5GHz with the same execution time?

(b) If the compilers of P2 and P3 were crafted by extraordinarily expert engineers such that the ratio of the number of instructions of the benchmark were 1.5: 1.25: 1 then what minimum clock frequency should each of them have to execute the benchmark in the same time? Assume you are no longer restricted by the heat removal constraint of 5GHz

1.5 : 1.25 :

2. Write a sequence of `RISC V` instructions that would

(a) accomplish swapping the most significant 16 of 32 bits with the least significant 16 of the 32 bit register `x10`

(b) Write a sequence of `RISC V` instructions that would determine the sum of a consecutive sequence of integers from `m` to `n` where `m<n` and both `m` and `n` are divisible by `4`.

3. *Write down the RISC V code for the following tasks:*

Assume Base address of arrays `A, B, C` are in registers `x5, x6, x7`

Assume variables `f, g, i` are in registers `x8, x9, x10`

Implement in RISC V these line of code in C:

(i) `f = g - A[B[C[128]]]`

(ii) `f = g - A[C[16] + B[32]]`

(iii) `A[i] = 4B[8i-81] + 4C[32i+32]`

4. One possible performance enhancement is to do a shift and add instead of an actual multiplication. [Since 9×6, for example, can be written $(2\times2\times2+1)\times6$, we can calculate 9×6 by shifting the bit string representing 6 to the left three times and then adding 6 to that result]. Show the best way to calculate $0x2E_{hex} \times 0x3D_{hex}$ using shifts and adds/subtracts. Assume both inputs are 8-bit unsigned integers.

5. A processor from Fasto Technologies (FT) has 32 registers, uses 16-bit immediates and has 142 instructions in its ISA. In a given program,

- 20 % of the instructions take 1 input register and have 1 output register.,
- 30 % have 2 input registers and 1 output register,
- 25 % have 1 input register, 1 output register and take an immediate input as well,
- The remaining 25 % have one immediate input and 1 output register.

(1) For each of the 4 types of instructions , how many bits are required? *Assume that the ISA requires that all instructions be a multiple of 8 bits in length.*

(2) How much less memory does the program take up if variable-length instruction set encoding is used as opposed to fixed-length encoding?