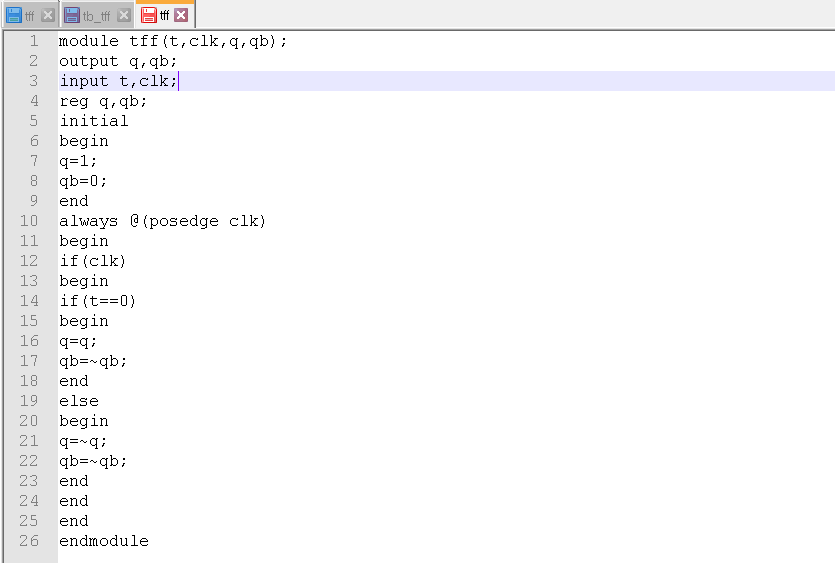
## LAB EVALUATION-2

Yaswanth Ram Ponnada

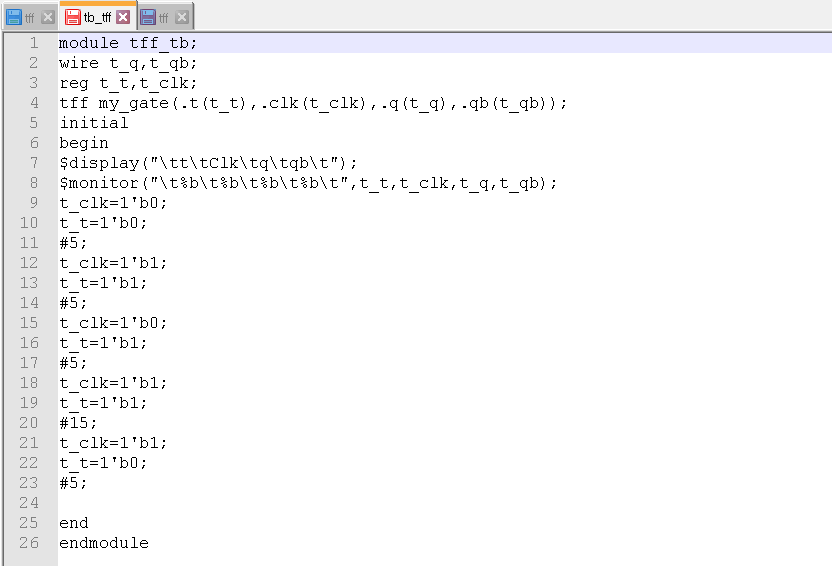
CB.EN.U4CSE18243

1) T flip flop

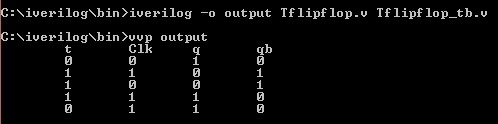
Design:



Test bench:

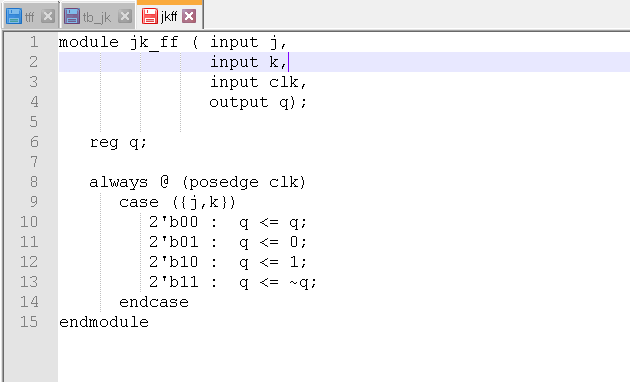


Output:

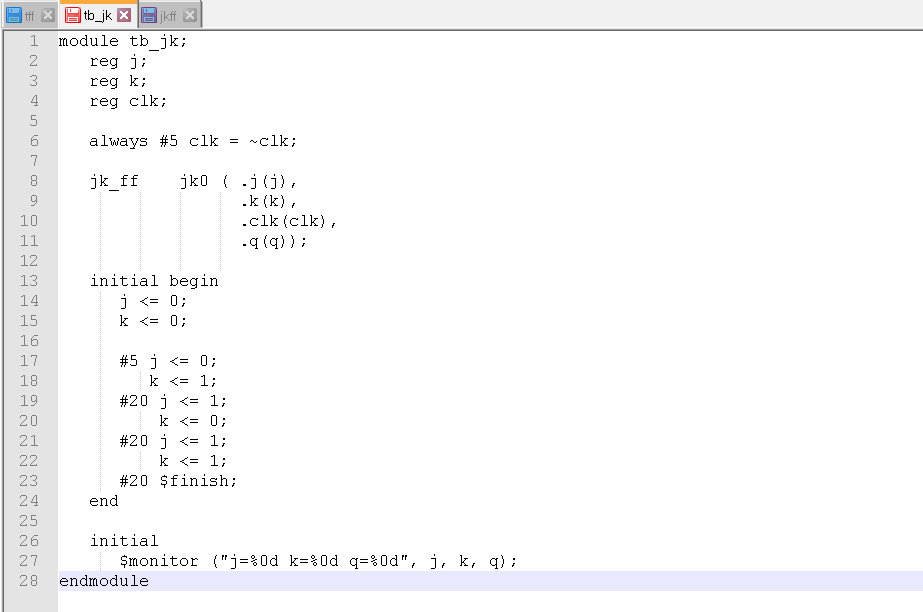


2) JK flip flop

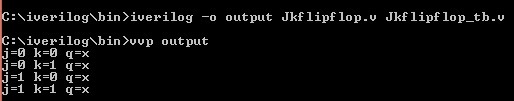
Design:



Test bench:

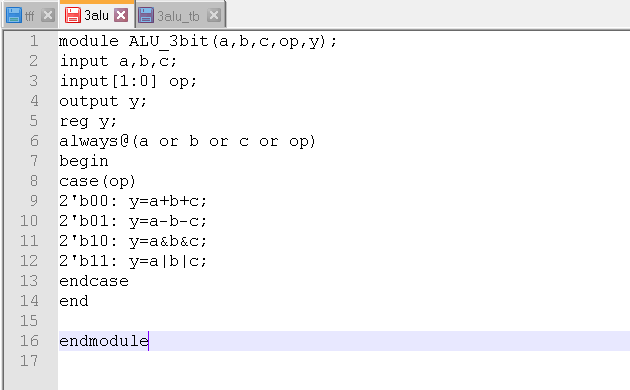


Output:



3) 3-bit ALU with addition, subtraction, AND & OR

Design:



Testbench:

module ALU\_3bit\_tb;

reg t\_a,t\_b,t\_c;

reg [1:0] t\_op;

wire t\_y;

ALU\_3bit my\_alu(.op(t\_op),.a(t\_a),.b(t\_b),.c(t\_c),.y(t\_y));

initial

begin

$monitor(" a:%b b:%b c:%b | y:%b",t\_a,t\_b,t\_c,t\_y);

$display("Add");

t\_a=0;

t\_b=0;

t\_c=0;

t\_op=2'b00;

#20

t\_a=0;

t\_b=0;

t\_c=1;

t\_op=2'b00;

#20

t\_a=0;

t\_b=1;

t\_c=0;

t\_op=2'b00;

#20

t\_a=0;

t\_b=1;

t\_c=1;

t\_op=2'b00;

#20

t\_a=1;

t\_b=0;

t\_c=0;

t\_op=2'b00;

#20

t\_a=1;

t\_b=0;

t\_c=1;

t\_op=2'b00;

#20

t\_a=1;

t\_b=1;

t\_c=0;

t\_op=2'b00;

#20

t\_a=1;

t\_b=1;

t\_c=1;

t\_op=2'b00;

#20

$display("subtract");

#20

t\_a=0;

t\_b=0;

t\_c=0;

t\_op=2'b01;

#20

t\_a=0;

t\_b=0;

t\_c=1;

t\_op=2'b01;

#20

t\_a=0;

t\_b=1;

t\_c=0;

t\_op=2'b01;

#20

t\_a=0;

t\_b=1;

t\_c=1;

t\_op=2'b01;

#20

t\_a=1;

t\_b=0;

t\_c=0;

t\_op=2'b01;

#20

t\_a=1;

t\_b=0;

t\_c=1;

t\_op=2'b01;

#20

t\_a=1;

t\_b=1;

t\_c=0;

t\_op=2'b01;

#20

t\_a=1;

t\_b=1;

t\_c=1;

t\_op=2'b01;

#20

$display("AND");

#20

t\_a=0;

t\_b=0;

t\_c=0;

t\_op=2'b10;

#20

t\_a=0;

t\_b=0;

t\_c=1;

t\_op=2'b10;

#20

t\_a=0;

t\_b=1;

t\_c=0;

t\_op=2'b10;

#20

t\_a=0;

t\_b=1;

t\_c=1;

t\_op=2'b10;

#20

t\_a=1;

t\_b=0;

t\_c=0;

t\_op=2'b10;

#20

t\_a=1;

t\_b=0;

t\_c=1;

t\_op=2'b10;

#20

t\_a=1;

t\_b=1;

t\_c=0;

t\_op=2'b10;

#20

t\_a=1;

t\_b=1;

t\_c=1;

t\_op=2'b10;

#20

$display("OR");

#20

t\_a=0;

t\_b=0;

t\_c=0;

t\_op=2'b11;

#20

t\_a=0;

t\_b=0;

t\_c=1;

t\_op=2'b11;

#20

t\_a=0;

t\_b=1;

t\_c=0;

t\_op=2'b11;

#20

t\_a=0;

t\_b=1;

t\_c=1;

t\_op=2'b11;

#20

t\_a=1;

t\_b=0;

t\_c=0;

t\_op=2'b11;

#20

t\_a=1;

t\_b=0;

t\_c=1;

t\_op=2'b11;

#20

t\_a=1;

t\_b=1;

t\_c=0;

t\_op=2'b11;

#20

t\_a=1;

t\_b=1;

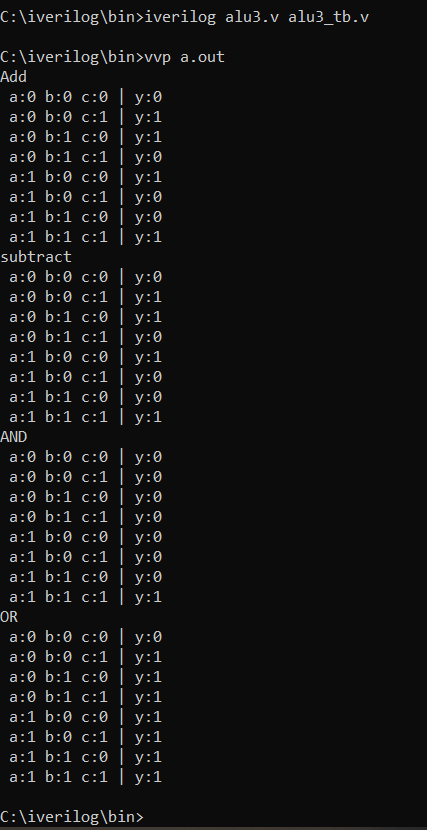
t\_c=1;

t\_op=2'b11;

end

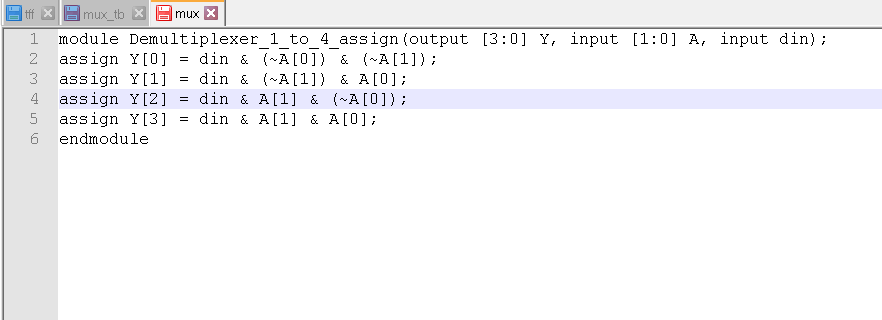
endmodule

Output:

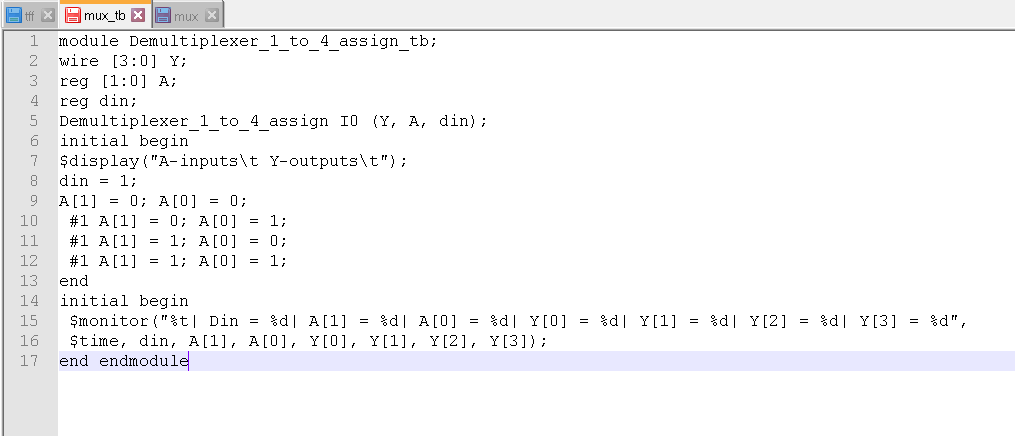


4) 1\*4 demux:

Design:



Testbench:



Output:

