Yatharth Agarwal

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A Hardware Engineer with 2+ years of experience in PCB Design, VLSI, and Embedded Systems. With excellent communication, collaborative skills, and proficiency in multiple CAD tools, I am looking to leverage my experience in developing innovative, high-performance architectures and contribute towards enabling the next generation of low-power edge computing systems.

Education

MS in Electrical & Computer Engineering (Thesis) *May 2025*

Purdue University - West Lafayette | CGPA 3.75/4.00

Advanced VLSI Design, Computer Architecture, Digital System Design Automation, MOS VLSI Design, IC Fab Lab

BTech in Electronics & Communication Engineering *May 2023*

Manipal Institute of Technology | CGPA 8.94/10.0

(Honor's courses) Analog & RF VLSI, CMOS Mixed Signal Design, Semiconductor Process Tech.

Work Experience

Graduate Research Assistant *October 2023 - Present*

Embedded System Laboratory *West Lafayette, IN*

- Engineering an integrated secure platform for device Authentication, Firmware verification, and runtime monitoring of Unmanned Aerial Vehicles, contributing to enhanced hardware security as a part of SRC JUMP2.0 center Cognisense.
- Designed PCBs with PCIe and Gigabit Ethernet, ensuring signal integrity and EMI resilience in space-constrained environments.
- Researched and devised a novel Processing in Pixel and Compute in Memory architecture in Cadence Virtuoso, achieving 40x improvement in power consumption and minimal area overhead in binarized neural networks using HW/SW co-design techniques.

Hardware Engineering Intern *January 2023 - June 2023*

Cisco *Bengaluru, India*

- Conducted DFM & DFA analysis on PCBs with 36 layers, back-drilling, and VIPPO techniques, fine-tuned for high data rates of up to 10Gbps, improving router design efficiency and manufacturability.
- Applied Agile product development methodology and proposed value engineering strategies to reduce BOM costs by 4%.

Technical Head *May 2021 - July 2022*

Project Manas *Manipal, India*

- Supervised and led a team of 50+ undergraduates to develop End-to-End detailed Technical Architecture for Unmanned Aerial vehicles capable of autonomous navigation and perception.
- Prototyped and fabricated power distribution system PCBs for high-power propulsion (300A) and low-voltage control electronics.

Project Experience

8T SRAM Compute in Memory Macro *August 2023 - November 2023*

- Designed a 4kb Compute-in-Memory macro using Cadence Virtuoso utilizing 8TSRAM thin cell layout, streamlined for area, latency, and power, resulting in an 85x improvement in energy consumption over baseline systems.
- Studied circuits and device technologies to mitigate PVT variations and enhanced read/write schemes for submicron semiconductor processes involving FinFets.

VSDSquadron - RISCV Bring up and system development *March 2023 - Present*

- Produced PCBs and firmware for four RISC-V-based development boards, collaborating with OEMs to minimize the bill of materials, resulting in 1,000+ units sold and promoting accessible education.
- Organized and led free workshops for 500+ B. Tech students covering RISC-V design, physical design, and embedded systems using VSDSquadron, resulting in increased student engagement and over 85% positive feedback on technical content.

RISCV32I Core - RTL2GDSII *January 2023 - March 2023*

- Implemented RTL for a RISCV32I core with SPI and UART interface on the Artix7 FPGA.
- Performed step-by-step modeling and conducted the Physical design flow for generating a GDSII based on SKY130 PDK and OpenLANE.

Physical Verification SKY130 & OpenROAD 7nm Contest *March 2023 - April 2023*

- Gained an understanding of Physical Verification & various DRC/LVS violations and related mitigation strategies utilizing Netgen and Xschem.
- Created DRC verification scripts for ASAP7 PDK and won the outstanding contribution award for enhancing OpenROAD Flow Scripts Physical design tool.

Technical Skills

VLSI Design | Cadence (RTL-to-GDSII flow certified) | Virtuoso | Innovus | Tcl | Xshem | OpenLANE | Yosys

PCB Design | Altium | Eagle | KiCad | DFM analysis | DFA analysis

Embedded Systems | Atmel Studio | STM32 Cube IDE | RISC-V ISA | ARM | make scripting | Linux