DRC and LVS Checks for ASAP7

Yatharth Agarwal
ECE Dept.
MIT Manipal
Manipal, India
yatharthrpi@gmail.com

Abstract – Design Rule Checking (DRC) and Layout Versus Schematic (LVS) are two essential steps in the chip design process that help ensure the functionality and reliability of the final product. This paper discusses the implementation of DRC and LVS for ASAP7 PDK in the OpenROAD Flow and optimising the Tech Lef file for the PDK.

I. INTRODUCTION

OpenROAD is an integrated chip physical design tool that takes a design from RTL to GDSII. OpenRoad Flow Scripts is a flow controller that supports the ASAP7 PDK for various designs. It was discovered that DRC and LVS are currently not supported for the PDK, potentially leading to undetected errors in the design and ultimately affecting the reliability and functionality of the final product.

II. DRC

The ASAP7 Design Rule Manual[1] defines the various rules for each layer and the specifications to be considered during the layout. Klayout is a tool that uses a *.lydrc* file to crosscheck with the described rules and report the corresponding violations. Modifying the *asap7.lydrc* by laurent2c[2] for ORFS and running DRC on the *GCD* design, it is observed that there exist over 300 violations that can be categorised into various categories described in *table 1*.

DRC Category	Count	DRC Category	Count
NSELECT.W.1	9	NSELECT.W.2	10
PSELECT.W.1	10	PSELECT.W.2	11
M1.S.2	1	M1.S.3	2
V1.S.4	1	V1.S.5	2
V2.M3.AUX.2	106	**Total**	**350**

Table 1

III. ASAP7 TECH LEF

LEF is a standard format used to describe the physical layout of integrated circuits. The tech LEF file is specific to a particular process technology. It contains information about the layers, pins, power and ground connections, and other physical attributes of the layers in the library.
By analysing[3] the *asap7_tech_1x_201209.lef* file, it is observed that there are missing enclosure[4] rules along with incomplete and inaccurate definitions for the metal and via layers resulting in most DRC issues listed in *table 1*. Modifying the tech LEF allows the DRC errors to be resolved by meeting the design rules.

IV. LVS

LVS compares the physical layout of a chip design against the schematic to ensure that they match. It checks for errors like missing connections, shorts, and other discrepancies between the physical layout and the schematic. The LVS checks for Klayout are defined in the *.lylvs* file. Currently, there are no available *.lylvs* files for ASAP7. Using existing files for sky130hd PDK along with the KLayout documentation[5], the required file can be written for ASAP7 PDK.

V. REFERENCES

[1] ASAP7 PDK Design Rule Manual
https://github.com/The-OpenROAD-Project/asap7/blob/master/asap7PDK_r1p7/docs/asap7_drm_201207a.pdf

[2] laurentc2, ASAP7_for_KLayout
github.com/laurentc2/ASAP7_for_KLayout

[3] Cadence LEF/DEF Language Reference
https://www.ispd.cc/contests/18/lefdefref.pdf

[4] ORFS Discussions ASAP7 DRC #854
https://github.com/The-OpenROAD-Project/OpenROAD-flow-scripts/discussions/854

[5] Klayout Layout vs. Schematic
https://www.klayout.de/doc/manual/lvs.html