

Yatin Gilhotra

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September 20, 1996

yatingilhotra.github.io

Education

B. Tech. in Electronics & Communication Engg.

Delhi Technological University
(formerly Delhi College of Engineering)

August 2014 - May 2018

81.54% Aggregate

Awarded **First Class with Distinction**

Shastri Research Student Fellow

Class 12th CBSE (AISSCE)

PKR Jain Sr. Sec. Public School, Ambala

March 2014

96.6% Aggregate

Maths

Physics

Chemistry

English

Rank: 1/300

Awarded: **Student of the Year**

Experience

Analog and Mixed Signal Circuit Design Engineer

High Speed SerDes Design Group, Synopsys Inc.

August 2018 - Present

Bangalore, India

- 112Gb/s TX for 400GBASE-Ethernet:** NRZ and PAM-4, 5-tap FFE, DAC based Transmitter designed on 7nm FinFET. Improved significantly on power and area efficiency. Developed robust design for Jitter, SNDR, ENOB, and Output Swing across PVT, and Mismatch variations.
- 10-1.6Gb/s Multi Protocol RX:** Designed 1-Tap Speculative, 5 Tap DFE, Samplers, Offset-Cancellation Loop, Current Steering DAC, Clock Tree, High Speed TSPC Flops, and Deserializer for 1.6-10Gb/s Multi-Protocol RX on TSMC 40nm.
 - Enhanced Samplers to achieve low sensitivity, and designed for low kickback, and random noise, with minimal trade-off in power.
 - Designed a low offset Common-Mode Feedback Loop, for precise Common Mode matching between input and reference branches of samplers. Extensive analysis done for high stability margins, good PSRR, and rms-noise of the loop.
 - Designed a low power, high precision Current Steering DAC with less than 1-LSB INL, with programmable range(1x-4x).
 - Implemented a skew calibration scheme for precise on-chip clock-data alignment. Designed clock tree for low DJ, RJ, and Phase Mismatch.
 - Devised and implemented from scratch, a single Deserializer solution compliant with all the targeted communication protocols.
- 12-0.25Gb/s Loopback Test, HDMI2.1 TX:** Designed and Developed a configurable 0.25-12Gb/s Delay Locked Loop based Near End, Horizontal Eye Loopback-Test for HDMI2.1 TX production testing, on TSMC-28nm.
- Responsibilities:** General responsibilities include participating, and critiquing in periodic design reviews. Reporting, and working closely with CAD teams in solving Custom Compiler, HSPICE, and FineSim(Design Tools) bugs. Conducting regular update meetings and design reviews with customers.

Research Intern

Polystim Neurotechnologies Lab, Polytechnique Montreal | Mentor: Prof. Mohamad Sawan

June 2017 - August 2017

Montreal, Canada

- Project:** Design of an adaptive thresholding Smoothed-TEO based action-potential detector based on Qn-estimator of scale.
 - Improved the spike detection algorithm from taking $O(N^2)$ time and $O(N^2)$ space to warranting $O(N \log N)$ time and $O(N)$ space.
 - Ran rigorous simulations on golden-truth data generated from the real extra-cellular neural recordings from hippocampus of a monkey.
 - Qn-STE0 algorithm outperforms many state-of-the-art spike detection algorithms, in all binary hypothesis metrics including Accuracy, Sensitivity, and Specificity.

Junior Research Fellow

VLSI Design Tools and Technology Laboratory, IIT-Delhi | Mentor: Assoc. Prof. Shouribrata Chatterjee

August 2016 - January 2017

New Delhi, India

- Bandgap References:** Designed a 0.5V, sub-picowatt 2-Transistor BGR, and a 1.2V high precision Brokaw's BGR in SCL's 180nm technology.
- Op-Amp:** Designed a 1V, 60dB, 600MHz UGB, two stage, miller compensated Op-Amp in UMC 65nm CMOS.

Texas Instruments University Program

Centre for Electronic Design and Technology, Netaji Subhas Institute of Technology

December 2015 - January 2016

New Delhi, India

- Developed a remotely controllable **Smart Irrigation System** by linking IOT-enabled Beaglebone with Whatsapp. Built sensors for soil temperature, and moisture sensing, facilitating the irrigation decisions.

Publications

Joshi R., Raghuvanshi A., **Gilhotra Y.**, Sharma S., Sharma S., Dalmia P., Pandey N.

An FPGA Based Floating Point Gauss-Seidel Iterative Solver

 In: 14th IEEE INDICON, December 2017, IIT Roorkee

Oruganti S., **Gilhotra Y.**, Pandey N., Pandey R.

OTRA Based Piece-Wise Linear VTC Generators and their application in High-Frequency Sinusoid Generation

 Advances in Electrical and Electronic Engineering, Vol. 15, No. 5, 2017

Oruganti S., **Gilhotra Y.**, Pandey N., Pandey R.

New Topologies for OTRA Based Programmable Precision Half-Wave and Full-Wave Rectifiers

 In: 2nd IEEE International Conference on Recent Developments in Control, Automation & Power Engineering, Oct. 2017, Noida

Other Academic Projects

Design of ULP, UL-Gm OTA for Subhertz Applications using Dynamic Subthreshold Operation


Mentor: Prof. Rajeshwari Pandey

 January 2018 - May 2018

 Delhi Technological University

- Studied the analog properties of a DTMOS transistor in sub-threshold region, and implemented the findings for low power analog design.
- Achieved nominally **25%** power reduction compared to regular CMOS, with minimal trade-offs in dynamic range in designing 0.5V, 0.3Hz first order filters for biomedical applications.










Technical Skills

Cadence Virtuoso ADE-L & XL Custom Compiler SAE Design Vision Verilog VHDL MATLAB C/C++ Python
Web Development Jekyll  OrCAD PSpice

Relevant Coursework

Analog Electronics Digital Electronics Network Analysis and Synthesis Probability and Stochastic Processes
Signals and Systems Analog Integrated Circuits Digital System Design Electromagnetic Theory Computer Architecture
Digital Signal Processing Microprocessors and Interfacing VLSI Design Control Systems Embedded Systems
Optical Communication CMOS Integrated Circuits Wireless Communication Micro and Nano Fabrication

Other Notable Positions and Achievements

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Teaching Assistant
CMOS Integrated Circuits Lab: Gave lectures on op-amp design, and tutorials for performing simulations using Cadence Virtuoso™
(2018) | 
Micro and Nano Fabrication (MEMSx)
Online course by EPFLx on edX
Result: 95%
(2017) |
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Captain, DTU Boys Badminton
Silver Medal at Aahvaan 18', a national level intercollegiate sports meet Gold Medal at Arena 17', interdepartmental tournament, DTU
(2017-18) | 
All India JEE Mains Examination
All India Rank: 3113/1.2M+
(2014) |
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Research Assistant
Digital System Architecture and Design Group, DTU:
Conducted research on iterative solvers, and helped develop a novel, low latency Gauss-Jacobi solver.
(2017) | 
Excellence Award
By Smt. Smriti Irani , Minister of Human Resource Development, India for being in top 0.001% students in the country All India Rank: 955/1M+
(2014) |
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Shastri Research Student Fellowship
Awarded by Shastri Indo-Canadian Institute, Ministry of HRD, India Selected among India's 12 most promising undergraduates for India's research exchange program with Canada
(2016-2017) | 
Certificate of Merit by CBSE, in Instrumental Music (The Sitar)
Awarded to only 27 candidates in India, for exhibiting superior knowledge in Instrumental Music
(2014) |
| | 
Silver Medal
at SOF International Mathematics Olympiad
(2013) |