Nika Mansouri Ghiasi

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EDUCATION

B.Sc. in Electrical Engineering, Electronics Field September 2011 – (Expected July 2016)

School of Electrical and Computer Engineering, University of Tehran, Tehran, Iran
Total GPA: 17.56/20 – **Last three semesters GPA:** 19.24/20 (Department Average GPA: 14.64)

High School Diploma in Physics and Mathematics September 2007 – June 2011

National Organization for Development of Exceptional Talents, Mazandaran, Iran
Total GPA: 19.77 **- Ranked 1st**

AREAS OF INTERESTS

- Computer Architecture and CAD
- VLSI Design
- Digital Design in Bio-Medical Applications
- Architecture for High Performance Computing

RESEARCH EXPERIENCE

Visiting Researcher August 2015 – December 2015
Texas Tech University, Data-Intensive Scalable Computing Laboratory Lab (DISCL)
Under the supervision of Professor Yong Chen

- Team member of Goblin-Core64 (GC64) project: Purpose-Built Chip Multitasking System and Software Architecture for Data Intensive Computing
- **Implementation leader** of memory request coalescing for hybrid memory cube devices in the project.
- Utilization of RISC-V Rocket Chip generator on Zynq Xilinx FPGA platform

Bachelor Project July 2015 – Present
University of Tehran, Low Power High Performance Nano Systems Lab
Under The supervision of Professor Ali Afzali-Kusha and Professor Mehdi Kamal

- Finding critical paths in digital circuits in the presence of process variations.

Summer Intern July 2014 – September 2014
Polytechnic University of Turin, Test Group
Under The supervision of Professor Paolo Prinetto and Professor Zain Navabi

- Design and Synthesis of a hardware camera lens distortion core using Xilinx Vivado **High Level Synthesis** tool.
- Analysis of the state-of-the-art camera lens distortion algorithms, focusing on hardware architectures able to

Minor Undergraduate Research Work February 2015 – July 2015
University of Tehran, Silicon Intelligence and VLSI Signal Processing Lab

- Study of hardware design for MIMO Lattice Reduction algorithm, focus on optimizing divisor and CORDIC units

HONORS AND AWARDS

- Grant for visiting research position in Texas Tech University (2015)
- M. Sc. Admission from ECE Department, from University of Tehran, **Exempted from M. Sc. National entrance exam as an exceptional talent** (2015)
- Grant for research intern in Polytechnic University of Turin (2014)
- Awarded University of Tehran **Fellowship** for B.Sc. (2011 – Present)
- **Ranked as top 0.1% among more than 280,000 students** in National Universities Entrance Exam (2011)
- Semifinalist at **Mathematics, Chemistry**, and **Literature** National Olympiads held by Young Scholars Club (2010)
- Accepted as a member of National Organization for Development of Exceptional Talents (NODET) (2007)

PUBLICATIONS

-X. Wang, **N. Mansourighiasi**, J. Leidel, Y. Chen, *"Dynamic Memory Coalescing for Hybrid Memory Cube Devices",* to be submitted to The 25th International ACM Symposium on High-Performance Parallel and Distributed Computing (HPDC-2016) Kyoto, Japan - May 31 to June 4, 2016 **(final draft is ready)**

-Sayed Rasool Faraji, Aliazam Abbasfar, and Samad Sheikhaei, **Nika Mansourighiasi** "Efficient Lattice Reduction Algorithm with Fixed Complexity for MIMO Detection" (to be submitted)

PROFESIONAL ACTIVITIES

Running a booth in IEEE/ACM Super-Computing 2015 in Austin, TX, November (**SC15**) to demo GC64: first UC Berkeley's RISC-V extension for supercomputing applications.

WORK EXPERIENCE

University of Tehran, CAD Research Group — July 2013 – September 2013
Under the supervision of Professor Zain Navabi

- Design and implementation of an extension board for Spartan-3 Xilinx FPGA

RELEVANT COURSE PROJECTS

- Modeling hardware of FIR filter using GEZEL and System C
- **Coprocessor and Custom Instruction** design for a MIPS processor on Nios II soft core on ALTERA DE-2 boards
- Design of low power memory architecture in **sub-threshold and near-threshold** rejoins
- **Fabricated Micron Technology MOSFET in Thin Film Lab** of University of Tehran
- **Profiling** of a digital design and finding circuit bottlenecks using Nios II IDE
- Implementing different **adder units and adder trees** such as Kogge-Stone and comparing their speed and area
- Analyzing the effects of **process and environmental variations** on digital designs using Monte Carlo simulation
- Finding maximum power of digital designs by **input reordering**
- **Gate-sizing** of logic circuits to find the minimum logic efforts of the circuit paths
- Design of **pipeline, single and multi-cycle MIPS** like processor using Verilog
- Design and implementation of digital signal generator, digital oscilloscope, and digital phase difference measurer and VGA controller on ALTERA DE-0 FPGA boards
- **Amplifier design** with specified frequency response, power, and stability
- **Box man game** using C
- implementation of signal generator with AVR microprocessors controlled by resistive touch and GLCD
- **Layout Design** of a four-bit ripple adder using L-Edit tool
- Design, simulation, and comparison of Standard CMOS with **other logic families** (Domino, Pseudo-NMOS, etc.)
- Design and implementation of a **line follower robot**

LANGUAGE

English: Fluent - **TOEFL iBT: 113/120**_R:29/30 L:29/30 S:27/30 W:28/30
- **GRE**: Quantitative Reasoning: **170/170** Verbal reasoning 149/170 Writing: 3.5/6

Farsi: Native
Arabic: Elementary

RELEVANT COURSES

VLSI (20/20)
Digital Electronics (20/20)
Computer Architecture (18.7/20 – second best grade)
HW/SW Co-design of Embedded Systems (19.7/20)
Introduction to Biomedical Engineering (19.2/20)
Digital Logic Design Lab (20/20)
Introduction to Computing and Programing (18.5/20)
Linear Control Systems (17/20)
Electronic III (16.2/20 – third best grade)

TEACHING ASSISTANTSHIP EXPERIENCE

- Robot Design with FPGA class for the UT student branch of IEEE Iran Section
- Computer Architecture (Professor Saeed Safari)
- Digital Logic Design (Professor Zain Navabi)
- Introduction for Computing Systems and Programming (Professor Hadi Moradi)
- Electronics I (Professor Mohammad-Reza Kolahdouz)
- Numerical Calculations (Professor Hossein Mahmoudi Darian)
- Probability and Statistics for Engineering (Professor Massoud Rabiee)

SKILLS

HDLs: Verilog, Chisel, GEZEL, System C
Programing: C/C++, Assembly
EDA Tools: ModelSim, Quartus II, HSPICE, MATLAB, Simulink, Tanner Tools (L-Edit, S-Edit), Proteus
Others: CodeVisionAVR, PSPICE, Multisim, Altera SOPC Builder, and NIOS II IDE
Operating Systems: Linux, Windows

OTHER INTERESTS

Philosophy: Modern, Sociological, Philosophy of Science
Literature: Ancient poems, World novels
Sports: Swimming, Walking

REFERENCES

Available upon request.