Bahareh Mostafazadeh Davani

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Research Interests

- **Computer Architecture**
- System on Chip (SoC) Design
- Very Large-Scale Integration (VLSI) circuit design
- Signal Processing
- Field Programmable Gate Array Architectures

Education

- **Sharif University of Technology**, Tehran, Iran (2010 - [expected]2014)

  - B.Sc. student in Computer Engineering, Department of Computer Engineering

  - Current GPA : 16.82/20 , last year GPA:17.57/20

  - Currently in the 7^{th} term
  Major courses: Fundamentals of Programming - C++ (17/20), Advanced Programming (17.4/20), Signals and Systems(19.1/20), Computer Architecture(19.5/20), Electrical Circuits(18.5/20), Digital Electronics(17.3), Microprocessors(18.8)

- **Farzanegan High School**, Tehran, Iran, (2007 - 2010)
  Affiliated with the National Organization for the Development of Exceptional Talents (NODET)
  High School Diploma GPA: 19.23 out of 20

- **Farzanegan High School**, Shiraz , Iran, (2006 - 2007)
  Affiliated with the National Organization for the Development of Exceptional Talents (NODET)

Honors

- Ranked 286^{th} in National Universities Entrance Competition(Aug. 2010)
  among 300,000+ candidates.

- Ranked among 30 students chosen Nation wide upon two levels of examination in Iranian National Olympiad in Informatics. (2007)

- Member of The **National Organization for Development of Exceptional Talents** (2003 2010)
  NODET student selection exam is held every year nationwide for students starting middle and high school. The organization is responsible for a number of schools across the country and training the top students on a more advanced level on every field of study.

Research Experience

- **Research Assistant at EASY Lab** (June 2013-present)
  Advisor: Dr.Maziar Goudarzi
  I assist in a project which is intended to be expanded for multicore processors on FPGA as well, but currently we are analyzing the power consumption of a simple processor (OpenRisc). The ultimate goal is to devise and assess innovative system-level techniques for power/performance optimization in multiprocessors in field-programmable system-on-chip (FPSoC) devices.

- **Summer Internship at Asr Gooyesh Pardaz Co.** (Summer 2013)
  Advisor: Dr.Hossein Sameti
  Main projects were research on a Grapheme to Phoneme conversion toolkit, and also a Recurrent Neural Network Language Model.

Teaching Experience

- **Teaching Assistant for Signals and Systems Course** (Fall 2013)
  Instructor: Dr.Hamid Rabiee
- **Teaching Assistant for Fundumentals of Electrical and Electronical Circuits Course** (Fall 2013)
  Instructor: Dr.Mehdi Jalili
- **Teaching Assistant for Computer Architecture Course** (Spring 2013)
  Instructor: Dr.Maziar Goudarzi
- **Teaching Assistant for Signals and Systems Course** (Spring 2013)
  Instructor: Dr.Hossein Sameti
- **Teaching Assistant for Electrical Circuits Course** (Spring 2013)
  Instructor: Dr.Mehdi Jalili

Test Scores

- **TOEFL: 112/120(Internet-Based Test)**
  Reading(27/30), Listening(30/30), Speaking(28/30), Writing(27/30)
- **GRE General Test(Paper-Based)**: Verbal (152/170 Percentile: 53) , Quantitative (166/170 Percentile: 93) , Analytical Writing (4.0/6.0 Percentile: 54)

Notable Course Projects

- **Developing Static Random Access Memory**
  Digital Electronics Course Project, Developed using HSPICE.
- **Design and Implementation of a Pipeline CPU**
  Computer Architecture Course Project. A pipeline CPU with MIPS instruction set, implemented using Altera Quartus.
- **Design and Implementation of an Engineering Calculator**
  Computer Structure & Language Course Project, implemented with MIPS assembly language.
- **Implementation of a Multi-threaded Game**
  Advanced Programming Course Project, developed in C++ Language.

Skills

- Programming:
  - *Software:* C++, C, MATLAB, Python
  - *Hardware:* Assembly(MIPS, Intel 8085,8086), Verilog HDL
- CAD Tools: Altera Quartus, Modelsim, Proteus, Altium Designer , HSpice , Cadence
- Operating Systems : Windows , Linux
- Languages: Persian (Native), English (Fluent), Arabic(Familiar), Spanish(Learning)

Activities

- **Chief of Executive Committee** , **1st National Digital System Design Conest**, Tehran, Iran. (October 2013 at Sharif University of Technology.)
  This is a nationwide contest, held in two separate sections: **FPGA Contest** and **Hardware-Software Co-design**. Former is a two player game, in which contestants must implement their agent on an FPGA board and compete with other teams.
  In the Co-design section, given a source code, they are to design the most efficient hardware-software system on an FPGA board of their choice , with costs taken to consideration.
  I was in charge of testing and developing the game for FPGA contest, and also managing the executive committee.
- Elected Member, **Student Scientific Chapter(SSC)** , 2011-2013, Computer Engineering Dept. SSC is the student committee concerned with directing the department extra-curriculum activities.
- **Chief of Staff**, 15th **Asia Regional ICPC/ACM**, 2013, Tehran, Iran. One of the three Chiefs of Staff, responsible for managing executive tasks of the contest and coordinating other staffs .
- **Chief of Staff**, 14th **Asia Regional ICPC/ACM**, 2012, Tehran, Iran.
- **Technical Staff**, 13th **Asia Regional ICPC/ACM**, 2011, Tehran, Iran. Member of technical committee, Responsible for resolving technical and scientifical problems during the contest.