Sahand Salamat

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Education

Fall 2012 - Spring 2017 (expected) **Bachelor of Science (B.Sc.) in Electrical Engineering**, *ECE Department, University of Tehran, Tehran*, Iran.
Specialized in Digital Systems

- *GPA:* $18.24/20$ *(2014-present),* $16.53/20$ *(overall)*

2008 - 2012 **High School Diploma**, *Allameh Helli High School under the supervision of National Organization for Development of Exceptional Talents (NODET), Hamedan*, Iran.

- *GPA :* $19.63/20$

Research Interests

- Embedded system design
- Low-power design
- High-performance and parallel computing
- Digital system verification
- Machine learning and big data
- Approximate computing
- High-level synthesis
- Computer architecture

Honors and Certificates

- Ranked 320th among 300,000 students in Physics and Mathematics National Universities Entrance Exam for Undergraduate Studies (Konkur)
- Qualified for the Final Stage of the National Physics Olympiad for two years
- *Certificate of Training* for attending workshop on teaching assistant training offered by University of Tehran

Research Experience

Fall 2015 - Present **Research assistant**, *in Design, Verification & Debugging of Embedded Systems (DVDES) LAB, under the supervision of Dr. B. Alizadeh* , ECE Department, University of Tehran,Iran.

Summer 2015 - Fall 2015 **Intern**, *in Design, Verification & Debugging of Embedded Systems (DVDES) LAB, under the supervision of Dr. B. Alizadeh*, ECE Department, University of Tehran,Iran.

Summer 2014 - Fall 2014 **Intern**, *Thin Film Layer (TFL) LAB, under the supervision of Dr. Z. Sanaee* , ECE Department, University of Tehran,Iran.

Publications

- **S. Salamat**, M. Ahmadi, B. Alizadeh, M. Fujita "Systematic Approximate Logic Optimization Using Don't Care Conditions" in International Symposium on Quality Electronic Design (ISQED), 2017.
- **S. Salamat**, M. R. Azarbad, B. Alizadeh, "Improve High Level Synthesis for Multi-Dimensional Nested Loops Using Reshaping and Vectorization Methods for Multi-Level Non-Rectangular Nested Loop" in Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2017. *-(submitted)*
- M. Ahmadi,**S. Salamat**, B. Alizadeh "A Dynamic Timing Error Avoidance Technique Using Approximation Logic Synthesis in High Performance Designs" in Transactions on Circuits and Systems I (TCAS I), 2017. *-(submitted)*

Projects

Notable Projects

On going **Early Prediction of Timing Critical Instructions in Pipeline Processor**.
Implemented a timing violation predictor to improve the performance of time borrowing technique in CPUs (an improvement on a publication with the same name), under the Supervision of Dr. Z. Navabi

2015 **Hardware Implementation of Trax Game**.
Implemented the Trax game on FPGA DE2i-150 board, using Chisel language under Genetic Algorithm for ICFPT 2015

2015 **Software Implementation of Trax Game**.
Implemented the Trax game in Java under both Genetic Algorithm and Minimax Algorithm with alpha-beta pruning

2014 **Anodic Aluminium Oxide Nano Structure**.
Fabricated an Anodic Aluminium Oxide Nanostructure (hexagonally arranged holes with 100 nm diameter) at Thin Film Laboratory, under the Supervision of Dr. Z. Sanaee

2014 **Multi-core Execution**.
Implemented an NoC-based multi-core system on FPGA using Leon3 processor

Course Projects

FPGA-based embedded system design — Implemented FIR filter on FPGA using both Verilog-HDL and Nios II core, and added acceleration through costume instruction and costume hardware

FPGA-based embedded system design — Ran real-time μC-OS on FPGA using Nios II core, and implemented an air-hockey game on OS

Pattern Recognition — Designed and implemented different classifiers such as Bayes classifier, K-NN and linear classifier using MATLAB

Microprocessor — Built a temperature controller circuit using AT-Mega32. *Nominated for the annual student best project award at University of Tehran*

Data structure & algorithms — Solved an HLS scheduling-binding problem using ILP, by C++ as well as MATLAB ILP solver

Linear control system — Modeled, simulated, and controlled a DC motor on SystemC-AMS

VLSI design — Designed, optimized, and simulated various logic circuits under design and process variations using HSPICE

Electronic system level design — Designed and implemented a FIR filter on FPGA using Matlab Simulink and the proprietary System Generator developed by Xilinx Co.

Computer architecture — Designed and implemented MIPS 5-stage pipeline processor, with dynamic branch prediction and two level cache, on FPGA

Core-based embedded systems design — Implemented matrix operators and calculations using GPU programming (CUDA)

Teaching Experiences

Teaching Assistant

Fall 2016 — FPGA-based embedded system design, Instructor Dr. B. Alizadeh

Fall 2016 — Data Structure and Algorithm in Electrical Engineering, Instructor Dr. M. Kamal

Spring 2016 — Microprocessor, Instructor Dr. O. Fatemi

Spring 2016, Fall 2015 — Digital Logic Design, Instructor Prof. Z. Navabi

Spring 2016, Fall 2015 — Computer Architecture, Instructor Dr. S. Safari

Spring 2015, Fall 2014 — Digital Logic Design Lab, Instructor Prof. Z. Navabi

Fall 2015 — Digital Electronics, Instructor Dr. M. Kamal

Fall 2014 — Electronic Circuit I, Instructor Dr. Z. Sanaee

spring 2014 Introduction to Computing Systems and Programming, Instructors DR. H. Moradi and Dr. M. R. Hashemi

Voluntary Experiences

2015 - 2016 Active member (executive committee) of IEEE student branch at University of Tehran

Summer 2015 Instructed hardware design and implementation on FPGAs, under the supervision of Prof. Z. Navabi

Summer 2015 Instructed hardware design and implementation using discrete logic elements (74 series), under the supervision of Prof. Z. Navabi

Fall 2014 Involved in setting up and operation of *Hobby Lab*, under the supervision of Prof. Z. Navabi

Computer skills

Programming C, C++, Verilog HDL, HSPICE (expert),

Languages & APIs Java, Chisel, SystemC, SystemC-AMS, SystemVerilog, CUDA (advanced),

VHDL, C#, assembly, visual basic (familiar)

Development Tools Modelsim, Quartus, Catapult HLS tool (expert),

Matlab/Simulink, CodeVision AVR, Proteus, Altium Designer, ISE , Vivado, Vivado HLS , Eclipse, LaTeX, Microsoft Office (advanced),

AutoCad, Pspice, Multisim (familiar)

Operating Systems Windows, Linux

Major Course Grades

- Digital Logic Design: 19.3/20
- Computer Architecture: 19.7/20
- Electronic System Level Design: 18.8/20
- Data Structures and Algorithms: 18.57/20
- Digital System Verification: 20/20
- VLSI: 19.19/20
- Digital Logic Design Lab 17.5/20
- Object Oriented Simulation 18.7/20
- Internship 20/20
- FPGA-based Embedded System Design 19.7/20
- Core-based Embedded System Design 18.7/20
- Digital Electronics 18.35/20

Major course GPA: 19.06

Language Skills

Persian (Native)
English (Excellent)
- TOEFL iBT: 100 (Reading: 27, Listening: 26, Speaking: 22, Writing: 25)
- GRE: 318 (Quantitative Reasoning:170, Verbal Reasoning:148, Analytical Writing:3.5)

Arabic (Basic)

Hobbies

Reading(novel & poem), TV series, Music, Mountaineering, Swimming

References

- My Personal Page
- Dr. Bijan Alizadeh Assistant Professor
- Dr. Mehdi Kamal Assistant Professor
- Dr. Zeinab Sanaee Assistant Professor
- Dr. Omid Fatemi Assistant Professor
- DVDES Lab Webpage
- Dr. Zainalabedin Navabi Professor
- Dr. Saeed Safari Assistant Professor
- Dr. Hadi Moradi Associate Professor
- Dr. Mahmoud Reza Hashemi Assistant Professor