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Imprecise 4-2 compressor design used in image processing applications

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Abstract: Approximate computing can be used in the error-tolerant applications since it can provide meaningful results with lower power consumption. In this study, the authors proposed a novel imprecise 4-2 compressor which is used in the multipliers of image processing applications. Besides the output values, they also consider the pattern distribution to resynthesise the 4-2 compressor in imprecise style. Compared to the precise compressor, the proposed imprecise 4-2 compressor can reduce power consumption and delay by 56 and 39%. Compared to the precise multiplier, the simulation results show that the multiplier which uses the proposed imprecise 4-2 compressor can achieve 33 and 30% improvement in power consumption and delay, respectively. In addition, the image quality of their design is good for human perception because peak signal-to-noise ratio PSNR values are more than 33 and mean structural similarity values are more than 0.99. Even compared to the related imprecise works, their design has a better error rate to improve the quality of images while maintains both the high power efficiency and low circuit complexity.

1 Introduction

Multiplier is an energy-hungry element and generally used in basic arithmetic operation for common DSP applications [1]. Typically, the steps of multiplication can be categorised as follows: In the first step, the multiplicand and the multiplier are multiplied to generate partial products. The second step is the partial products reduction. The third step is the final addition with carry propagation. In the tree multiplier, the three steps can be implemented with corresponding subcircuits [2–5], for example, (i) the Booth encoders and decoders generate a reduced number of partial products; (ii) a carry save structured accumulator makes a further reduction of the partial products matrix; (iii) a fast carry propagation adder [6] computes the final binary result.

Especially, the second step plays a significant role in area cost, overall delay, and power consumption [2–5]. Compressors are the important elements which can count the number of 1s in the inputs. Thus, for high-performance column compression multiplier, the 3-2 compressors [full adders (FAs)] and the 4-2 compressors are widely used to reduce the partial products matrix in the second step [2–5, 7].

A large number of arithmetic applications are implemented using precise and deterministic algorithms. However, some applications such as signal/image processing, communication, and multimedia can tolerate errors and produce results which are good enough for human perception [8–10]. Since approximate or less-than-optimal results are sufficient, these error-tolerant applications allow computing systems to trade quality for energy, area, and performance [10–14].

To enhance energy efficiency, various imprecise (or approximate) 4-2 compressors were proposed to design the multipliers. In [10], two 4-2 compressors (Design 1 and Design 2) were proposed to reduce power and delay with acceptable accuracy. Design 2 [10] is one of the state-of-the-art imprecise 4-2 compressor in recent days [14]. In [11], the authors modified the existing approximate 4-2 compressor and proposed a simple error recovery module. The authors in [12] analysed the error probability and the average error to design the approximate compressors without XOR gates. In [13], the dual-quality reconfigurable 4-2 compressors (DQ4:2C_4) can switch between the exact and approximate modes during the run time. For large size multiplier, the authors in [14] proposed approximate 15-4 compressors which are composed of approximate 5-3 compressors. Fixed-width multipliers with various error correction techniques are other approximation techniques to achieve high energy efficiency with the compromising accuracy [9].

In this paper, we observe the truth table of precise 4-2 compressor in image processing to implement the proposed imprecise 4-2 compressor. According to the pattern distribution and value difference of image outputs, we resynthesise the 4-2 compressor in imprecise style. The proposed imprecise 4-2 compressor can reduce the hardware complexity and improve peak signal-to-noise ratio (PSNR). Simulation results are provided at the gate level, such as gate count, power consumption, latency, and error rate. The proposed design provides good image quality with high energy efficiency. For further simulation, the multiplier with the proposed design is used in image processing application. Compared to the previous imprecise 4-2 compressor (Design 1 [10]), the results show that the multiplier with the proposed imprecise 4-2 compressor can improve PSNR about 50% on average. All mean structural similarities (MSSIMs) of the proposed design can achieve above 0.99. The multiplier with the proposed imprecise 4-2 compressor also has the lower normalised mean error distance (NED) and the lowest power-delay product (PDP)-mean relative error distance (MRED) product that prove that the superiority of the proposed design.

The remaining part of this paper is organised as follows. Section 2 introduces the precise and imprecise 4-2 compressors. Section 3 presents the proposed imprecise 4-2 compressor in detail. Sections 4 and 5 provide the simulation results and image processing application using the proposed design, respectively. Section 6 offers a brief conclusion of this paper.

2 Related work

2.1 Precise 4-2 compressors

A traditional precise 4-2 compressor has five inputs and three outputs [15, 16] and the symbol of the precise 4-2 compressor is shown in Fig. 1*a*. All inputs (X_1, X_2, X_3, X_4, and C_i) and the output *Sum* have the same weight. The remaining outputs (*Carry* and C_o) are weighted one binary bit order higher. The carry in (C_i) receives the carry out (C_o) of the previous stage. The basic equation of the 4-2 compressor can be written as follows:

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$$X_1 + X_2 + X_3 + X_4 + C_{\mathrm{i}} = Sum + 2 \cdot (Carry + C_{\mathrm{o}}) \quad (1)$$

The conventional implementation of the precise 4-2 compressor is composed of two FAs as shown in Fig. 1*b*. In [3], the precise 4-2 compressor which is based on XOR–XNOR gates has been proposed. The circuitry of the precise 4-2 compressor is shown in Fig. 2. An XOR–XNOR gate can generate the output signals of XOR and XNOR simultaneously. The critical path of this design is shorter than the critical path of Fig. 1*b*. In order to reduce the power and delay of precise 4-2 compressor [3], the authors in [4] replaced two XOR gates with transmission gate-based multiplexer (TG-based MUX only used in intermediate stage) and CMOS multiplexer (MUX).

2.2 Imprecise 4-2 compressors

The imprecise 4-2 compressors have been proposed in [10] for decreasing the circuit complexity and reducing the power consumption. The circuitry of Design 1 [10] is shown in Fig. 3. In Design 1 [10], the output signal *Carry* is the same value as the input C_{i}, and the circuitry which produces the output signals *Sum* and C_{o} are modified to reduce the cost. The circuitry of Design 2 [10] is shown in Fig. 4. In Design 2 [10], C_{i} and C_{o} are completely removed because C_{i} is always zero in the first stage. Thus, there are only four inputs and two outputs. By eliminating C_{i} and C_{o}, Design 2 [10] reduces effectively in terms of area cost, power, and delay. Based on the compressors proposed in [10], several tree structure multipliers have been proposed in [10, 17]. These imprecise multipliers use Dadda's [18] scheme and provide significant performance improvement compared to other imprecise multipliers.

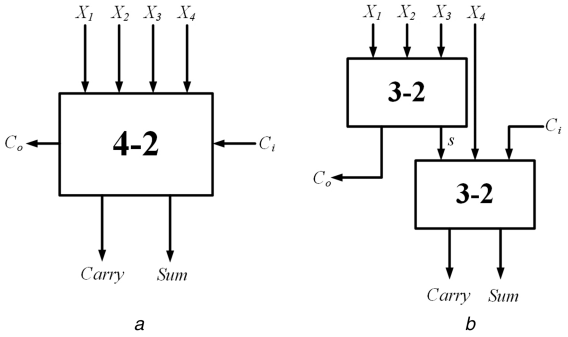

Fig. 1 *The traditional precise 4-2 compressor*
(a) Symbol of 4-2 compressor, ***(b)*** Conventional 4-2 compressor implemented with 3-2 compressors (FAs)

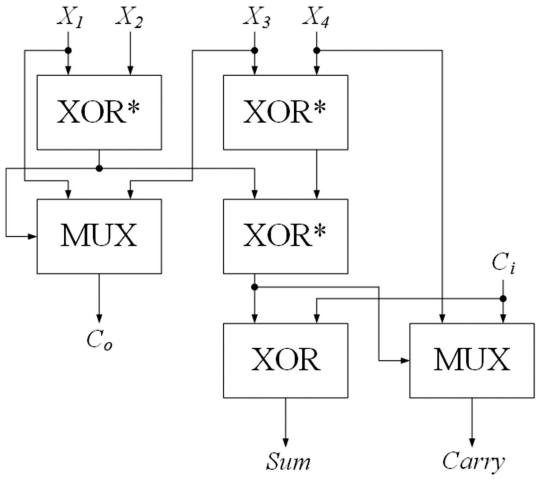

Fig. 2 *Precise 4-2 compressor of [3]*

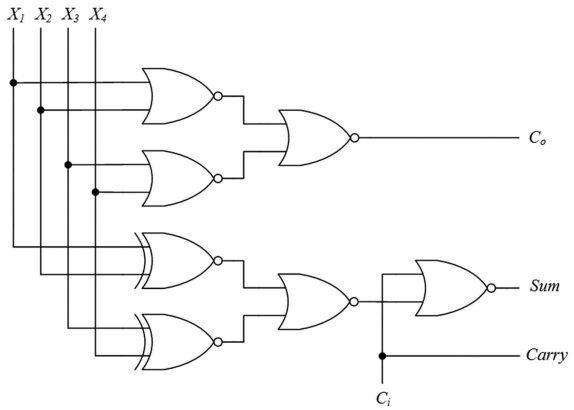

Fig. 3 *Design 1 of [10]*

Researchers in [11] investigated the truth table of the existing approximate 4-2 compressor and modified the truth table to make the *difference* value (the difference between the outputs of the approximate and precise 4-2 compressor) is 0 or −1. In this way, the error can be compensated by the simple error recovery module. The approximate 4-2 compressor [11] can be constructed by two XOR gates, one OR gate, and an AND–OR complex compound gate. In [12], the researchers analysed the error probability and the average error in a systematic way to design the approximate 4-2 compressor. The approximate 4-2 compressor [12] can be implemented by using two AND and two OR gates (without XOR gates) that can reduce the hardware complexity effectively.

Researchers in [13] proposed four approximate 4-2 compressors, which can switch between the exact and approximate modes during the run time to reduce power consumption. The compressors consist of an approximate (four inputs and two outputs) and supplementary parts. In the approximate mode, each compressor has its accuracy and (dual-quality 4:2 compressor Structure 4) DQ4:2C_4 has the lowest error rate.

Table 1 summarises the features of previous designs. Compared to the precise 4-2 compressor [3], Design 1 [10] traded the accuracy for the lower cost and critical path. The error rate is defined as the probability of incorrect outputs and the equation can be written as

$$Error\ rate = \frac{\text{Number of incorrect outputs}}{\text{Number of total outputs}} \quad (2)$$

Note that Design 2 [10], approximate 4-2 compressors [11, 12], and DQ4:2C_4 [13] have only four inputs (X_1, X_2, X_3, and X_4) and two outputs (*Carry* and *Sum*). As shown in Table 1, of course, the approximate compressors have lesser cost and shorter delay compared to the precise compressor. The error rate of approximate 4-2 compressor [11] is 25%. However, compared to other imprecise designs, the cost and the critical path of approximate 4-2 compressor [11] are higher and longer because of the AND–OR complex compound gate. Approximate 4-2 compressor [12] has the least cost and the shortest critical path but it has the highest error rate. Note that the outputs of approximate 4-2 compressor [12] have the same weight. However, if the outputs of approximate 4-2 compressor [12] are different weights, the error of this compressor is 56.25%. The costs of Design 2 [10] and DQ4:2C_4 [13] are almost the same. Just consider the approximate part of DQ4:2C_4 [13], compared to Design 2 [10], although the costs of both designs are almost the same, the error rate and the critical path of Design 2 [10] are lower and shorter, respectively. In this paper, the proposed design is compared to the precise 4-2 compressor [3], Design 1 [10], Design 2 [10], approximate 4-2 compressors [11, 12], and DQ4:2C_4 [13] to prove the effectiveness of our design.

3 Proposed imprecise 4-2 compressor

3.1 Error rate and the PSNR

The imprecise 4-2 compressor has been generally used to speed up the reduction of the partial products. However, if an imprecise 4-2 compressor is composed of two imprecise FAs (approximation 1 of [19]), it may result in a worse error rate (53%) [10]. The equation of error rate is defined as (2). In [10], the performance of the

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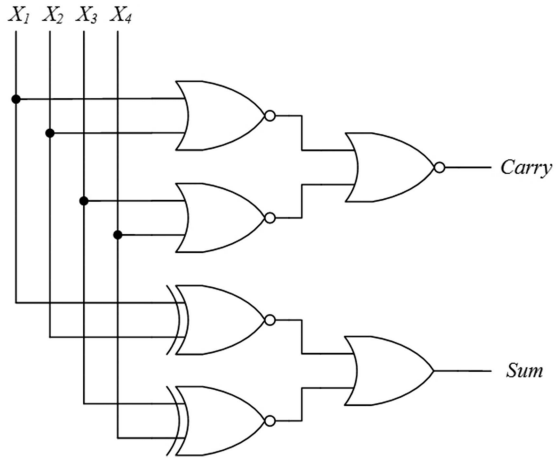

Fig. 4 *Design 2 of [10]*

Table 1 Comparisons for 4-2 compressors

Design	Cost	Critical path	Error rate
precise 4-2 compressor [3]	four XOR, two MUX	three XOR	(0/32) 0%
Design 1 [10]	two XNOR, five NOR	one XNOR + two NOR	(12/32) 37.5%
Design 2 [10]	one OR, two XNOR, three NOR	one XNOR + one OR	(4/16) 25%
approximate 4-2 compressor [11]	two XOR, one OR, one AND–OR complex compound gate	AND–OR complex compound gate	(4/16) 25%
approximate 4-2 compressor [12]	two AND, two OR (three-input OR gate)	one AND + one OR (three-input OR gate)	(9/16) 56.25%
DQ4:2C$_4$[13]	two XNOR, four NAND (approximate) three NOT, two XOR, six NAND, three tri-state buffer, two gating PMOS (supplementary)	one XNOR + one NAND + one tri-state buffer (approximate)	(5/16) 31.25%

imprecise circuit is better than the performance of the precise circuit, but the error rate problem still exists. To improve the error rate and the PSNR of the imprecise 4-2 compressor, we investigate the truth table of the precise 4-2 compressor and propose a novel imprecise 4-2 compressor design. Table 2 shows the truth table of the precise 4-2 compressor.

Note that the PSNR is not directly determined by the error rate. For example, the high error rate does not mean that the PSNR must be worse since the outputs which affect the image quality may still be correct. In contrast, the low error rate does not mean that the PSNR must be better since these incorrect outputs may really affect the image quality. To achieve better PSNR with the lower error rate, we analyse the Gaussian blurred output data to design the proposed imprecise 4-2 compressor for image processing application. As shown in Table 3, the highly probable outputs of benchmarks (six benchmarks as shown in Fig. 5) are '000' and '001' ($C_o = 0$, $Carry = 0$, $Sum = 0$ or 1). That is, the italic values in Table 2 have a great effect on the image quality. Therefore, these output patterns must be correct in the proposed design to improve the image quality.

3.2 Proposed imprecise 4-2 compressor

Table 2 also shows the truth table of Design 1 [10] and the proposed imprecise 4-2 compressor. The *difference* is the output value of the imprecise 4-2 compressor minus the output value of the precise 4-2 compressor. The equation of *difference* can be defined as

$$\begin{aligned} difference = {} & [Sum + 2 \cdot (Carry + C_o)]_{\text{imprecise}} \\ & - [Sum + 2 \cdot (Carry + C_o)]_{\text{precise}} \end{aligned} \tag{3}$$

For example, in Table 2, the inputs of precise 4-2 compressor are '00000' ($X_1 = 0$, $X_2 = 0$, $X_3 = 0$, $X_4 = 0$, $C_i = 0$), then, the outputs are '000' ($C_o = 0$, $Carry = 0$, $Sum = 0$); the outputs of Design 1 [10] are '001' and the outputs of the proposed design are '000' with the same input. Therefore, the *difference* values are 1 and 0, respectively. However, the substantial *difference* that is greater than +1 or less than −1 may not be acceptable in some applications. As mentioned before, outputs C_o and *Carry* have a higher weight than *Sum*. Thus, the *difference* value can be compensated by modifying the value of *Sum* to make the *difference* is between −1 to +1.

For example, if the outputs of imprecise 4-2 compressor and precise 4-2 compressor are '000' and '010', respectively, the *difference* is −2. By modifying the *Sum* of the imprecise 4-2 compressor from 0 to 1 ('001'), the *difference* will become −1. Note that if the outputs of the imprecise 4-2 compressor and precise 4-2 compressor are '011' and '101', respectively, the *difference* is 0 since C_o and *Carry* have the same weight as shown in (3). The proposed imprecise 4-2 compressor is also designed by modifying C_o, *Carry*, and *Sum* to make the *difference* is between −1 to +1, then, improves the image quality with low error rate.

In Table 2, the proposed imprecise 4-2 compressor has a lower error rate and the outputs '000' and '001' are always correct (the italic values). We modify C_o, *Carry*, and *Sum* which are bold italic values in Table 2 to design the proposed imprecise 4-2 compressor. For instance, consider the case of inputs '01001' (precise outputs '010'); we modify *Carry* first and the temporary imprecise outputs will be '000', but the *difference* is −2. Then, we modify *Sum* and the imprecise outputs will be '001' to compensate the *difference* from −2 to −1. As shown in Table 2, the error rate of the proposed design is 25% because there are 8 incorrect outputs of 32 outputs. This is less than the error rate of using two connected imprecise FAs (approximation 1 of [19]: about 53%) and the Design 1 [10] (37.5%). The circuitry of the proposed design can be implemented by Table 2. Fig. 6 shows the gate level implementation of the proposed design. Equations (4)–(6) are the logic expressions for the outputs of the proposed imprecise 4-2 compressor

$$C_0 = X_1 \cdot X_2 \tag{4}$$

$$Carry = \overline{\overline{(X_3 \cdot X_4)} \cdot \overline{(X_3 \oplus X_4) \cdot C_i}} \tag{5}$$

$$Sum = \overline{((X_3 \oplus X_4) \odot C_i) \cdot (X_1 \odot X_2)} \tag{6}$$

According to Fig. 6, the critical path of the proposed design is along the path from input X_i(X_3 or X_4) to the output *Sum* (1 XOR + 1 XNOR + 1 NAND gates). Clearly, the propagation delay of the proposed design is less than the optimised design of precise 4-2 compressor [3] (three XOR gates as summarised in Table 1). Moreover, the total number of gates in our design is significantly less than this precise compressor.

3.3 Implementations of multiplier

As shown in Fig. 7, the proposed imprecise 4-2 compressor can be used in the unsigned 8×8 array multiplier. In this paper, seven kinds of multipliers are investigated for detail analyses. Multipliers 1–3 adopt the array multiplier in Fig. 7 with different implementations of compressors. As mentioned before, Design 2 [10], approximate 4-2 compressors [11, 12], and DQ4:2C$_4$ [13] have only four inputs and two outputs. Thus, the structure of Multipliers 4–7 is different from the structure of Multipliers 1–3. Also the structure of Multipliers 4–7 needs one less FA but three more 4-input 4-2 compressors.

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- *Multiplier 1 (M1):* Precise 4-2 compressor [3] is used for all 4-2 compressors in Fig. 7.
- *Multiplier 2 (M2):* In Fig. 7, Design 1 [10] is used for the compressors in the n least significant columns; the remaining $n-1$ most significant columns use the precise 4-2 compressors [3].
- *Multiplier 3 (M3):* In Fig. 7, the proposed design is used for the compressors in the n least significant columns; the remaining $n-1$ most significant columns use the precise 4-2 compressors [3].
- *Multiplier 4 (M4):* Design 2 [10] is used for the compressors in the n least significant columns; the remaining $n-1$ most significant columns use the precise 4-2 compressors [3].
- *Multiplier 5 (M5):* DQ4:2C$_4$ [13] is used for the compressors in the n least significant columns; the remaining $n-1$ most significant columns use the precise 4-2 compressors [3].
- *Multiplier 6 (M6):* Approximate 4-2 compressor [11] is used for the compressors in the n least significant columns; the remaining $n-1$ most significant columns use the precise 4-2 compressors [3].
- *Multiplier 7 (M7):* Approximate 4-2 compressor [12] is used for the compressors in the n least significant columns; the remaining $n-1$ most significant columns use the precise 4-2 compressors [3].

Each multiplier has its features for different purposes. M1 provides exact computations, but consumes a lot of power. M2–M7 adopt the hybrid scheme which is composed of precise and imprecise 4-2 compressors to improve PSNR and image quality.

Table 2 Truth table of precise design, Design 1 [10], and the proposed imprecise 4-2 compressor

Inputs					Precise outputs			Design 1 [10] outputs				Proposed design outputs			
X_1	X_2	X_3	X_4	C_i	C_o	*Carry*	*Sum*	C_o	*Carry*	*Sum*	*difference*	C_o	*Carry*	*Sum*	*difference*
0	0	0	0	0	*0*	*0*	*0*	0	0	**1**	1	*0*	*0*	*0*	0
0	0	0	0	1	*0*	*0*	*1*	0	**1**	**0**	1	*0*	*0*	*1*	0
0	0	0	1	0	*0*	*0*	*1*	0	0	1	0	*0*	*0*	*1*	0
0	0	0	1	1	0	1	0	0	1	0	0	0	1	0	0
0	0	1	0	0	*0*	*0*	*1*	0	0	1	0	*0*	*0*	*1*	0
0	0	1	0	1	0	1	0	0	1	0	0	0	1	0	0
0	0	1	1	0	0	1	0	0	**0**	**1**	−1	0	1	0	0
0	0	1	1	1	0	1	1	0	1	**0**	−1	0	1	1	0
0	1	0	0	0	*0*	*0*	*1*	0	0	1	0	*0*	*0*	*1*	0
0	1	0	0	1	0	1	0	0	1	0	0	0	***0***	***1***	−1
0	1	0	1	0	0	1	0	**1**	**0**	0	0	0	***0***	***1***	−1
0	1	0	1	1	0	1	1	**1**	1	**0**	1	0	1	1	0
0	1	1	0	0	1	0	0	1	0	0	0	***0***	0	***1***	−1
0	1	1	0	1	1	0	1	1	**1**	**0**	1	***0***	***1***	1	0
0	1	1	1	0	1	0	1	1	0	1	0	***0***	***1***	1	0
0	1	1	1	1	1	1	0	1	1	0	0	***0***	1	***1***	−1
1	0	0	0	0	*0*	*0*	*1*	0	0	1	0	*0*	*0*	*1*	0
1	0	0	0	1	0	1	0	0	1	0	0	0	***0***	***1***	−1
1	0	0	1	0	0	1	0	**1**	**0**	0	0	0	***0***	***1***	−1
1	0	0	1	1	0	1	1	**1**	1	**0**	1	0	1	1	0
1	0	1	0	0	1	0	0	1	0	0	0	***0***	0	***1***	−1
1	0	1	0	1	1	0	1	1	**1**	**0**	1	***0***	***1***	1	0
1	0	1	1	0	1	0	1	1	0	1	0	***0***	***1***	1	0
1	0	1	1	1	1	1	0	1	1	0	0	***0***	1	***1***	−1
1	1	0	0	0	1	0	0	0	0	**1**	−1	1	0	0	0
1	1	0	0	1	1	0	1	**0**	**1**	**0**	−1	1	0	1	0
1	1	0	1	0	1	0	1	1	0	1	0	1	0	1	0
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1	1	1	0	1	1	1	0	1	1	0	0	1	1	0	0
1	1	1	1	0	1	1	0	1	**0**	**1**	−1	1	1	0	0
1	1	1	1	1	1	1	1	1	1	**0**	−1	1	1	1	0
error rate						(0/32) 0%			(12/32) 37.5%				(8/32) 25%		

Table 3 Number of Gaussian blurred output patterns for test images

C_o	*Carry*	*Sum*	Mandrill counts	Lena counts	Airplane counts	Sailboat counts	Peppers counts	House counts
0	*0*	*0*	*95,086,510*	*95,773,990*	*93,680,114*	*94,603,848*	*95,560,046*	*96,488,255*
0	*0*	*1*	*29,213,694*	*29,108,069*	*29,805,878*	*29,352,412*	*29,069,815*	*28,529,878*
0	1	0	5,282,945	5,012,409	5,301,149	5,632,650	5,350,348	4,692,963
0	1	1	104,605	88,138	30,104	51,225	49,014	46,750
1	0	0	2,620,809	2,601,042	3,443,601	2,804,037	2,632,336	3,053,789
1	0	1	2,725,411	2,516,886	2,909,260	2,705,193	2,466,866	2,344,746
1	1	0	439,226	376,920	310,423	332,036	351,112	323,415
1	1	1	10,400	6146	3071	2199	4063	3804

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For instance, if $n = 8$, the compressors of the eight least significant columns (P_0–P_7) are implemented with imprecise 4-2 compressors, and the compressors of the seven most significant columns (P_8–P_{14}) are implemented with the precise 4-2 compressors. Note that the hybrid scheme may not improve the error rate, but it will make the outputs more precise.

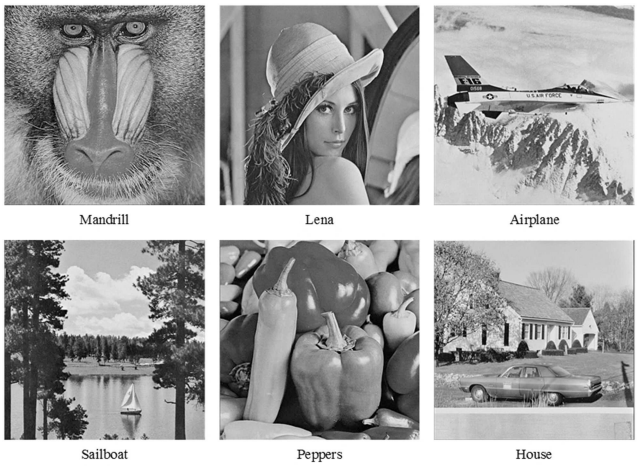

Fig. 5 *Six sample images: Mandrill, Lena, Airplane, Sailboat, Peppers, and House*

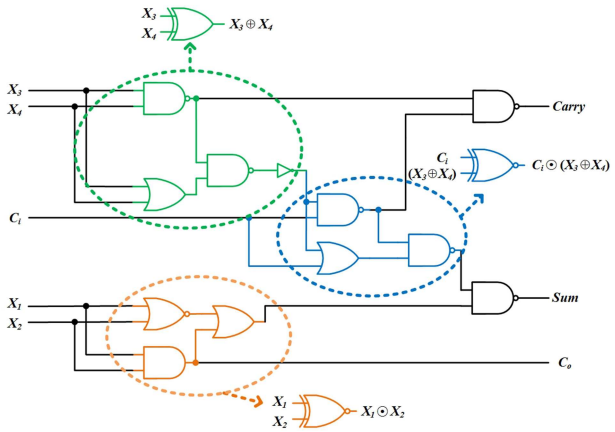

Fig. 6 *Proposed imprecise 4-2 compressor*

4 Simulation results

In this section, we use Taiwan Semiconductor Manufacturing Company 90 nm 1P9M CMOS technique to implement the traditional precise 4-2 compressor, Design 1 [10], Design 2 [10], approximate 4-2 compressors [11, 12], DQ4:2C_4 [13], and the proposed imprecise 4-2 compressor. The supply voltage is 1.0 V, the temperature is 25°C, and the results were simulated from the HSPICE. To avoid the weak drivability of outputs, all circuits are composed of CMOS logic gates for a fair comparison. Therefore, XOR, XNOR gates, and MUX are constructed by CMOS logic gates; XOR and XNOR gates can be constructed by two INV, two AND, and one OR gates; MUX can be constructed by two INV, two AND, and one OR gates. The FA adopts the 28T CMOS mirror adder. In Section 4.1, we provide comparisons among these 4-2 compressors (each size of 4-2 compressor is one-bit unit). In Section 4.2, we provide comparisons among M1–M5.

4.1 Comparisons of 4-2 compressors

Table 3 shows the number of output patterns in the array multiplier for the Gaussian blurred images. The italic values represent the highly probable outputs in all output patterns. According to these patterns, we propose a novel imprecise 4-2 compressor and use the proposed design in the 8×8 unsigned multipliers for further simulations.

Table 4 provides the comparisons among the precise 4-2 compressor of [3], Design 1 [10], Design 2 [10], approximate 4-2 compressors [11, 12], DQ4:2C_4 [13], and the proposed imprecise 4-2 compressor in terms of power, delay, cost, and error rate. Obviously, in terms of power, delay, and cost, the imprecise 4-2 compressors are much better than the precise 4-2 compressor. The critical path of precise 4-2 compressor [3] is along the path from input X_i to the output *Sum* (three XOR gates). The critical path of Design 1 [10] is through one XNOR and two NOR gates; the critical path of the proposed design is through one XOR, one XNOR, and one NAND gates; the critical path of Design 2 [10] is

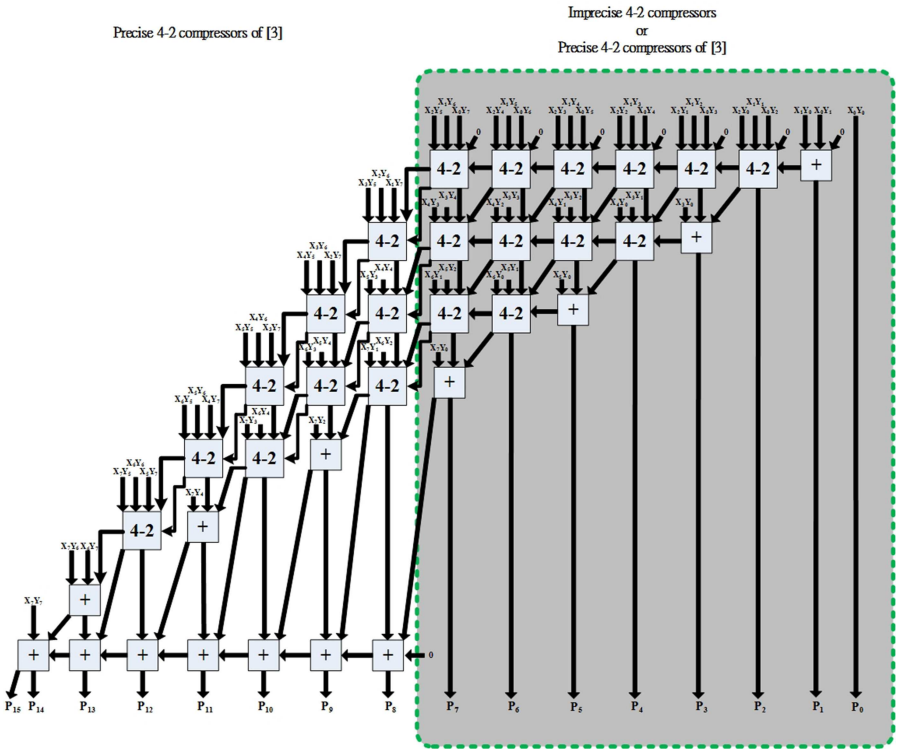

Fig. 7 *Unsigned 8 × 8 array multiplier*

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through one XNOR and one NOR gates; the critical path of DQ4:2C_4 [13] is through one XNOR, one NAND, and one tri-state buffer. The critical path of approximate 4-2 compressor [11] is the AND–OR complex compound gate and the critical path of approximate 4-2 compressor [12] is one AND and one OR gates.

To design the approximate compressor under the constraint of a low error rate, approximate 4-2 compressor [11] is composed of one OR, two XOR, and one AND–OR complex compound gate. Approximate 4-2 compressor [11] has the longest delay and consumes more power than other imprecise designs because of the high circuit cost, even though it has a lower error rate. Clearly, approximate 4-2 compressor [12] has the least delay and the least power consumption, but its error rate is the worst. The delay of DQ4:2C_4 [13] is relatively long because the tri-state buffers make the delay longer. The power consumption of DQ4:2C_4 [13] is relatively high since the supplementary part still contributes static power consumption even power-gated. Compared with the precise 4-2 compressor, the proposed imprecise 4-2 compressor can achieve about 56 and 39% improvement in terms of power consumption and delay, respectively. As mentioned before, compared with precise circuits, imprecise circuits can operate at lower power consumption and higher performance with meaningful results for human.

In terms of the cost, the costs of imprecise compressors are less than the cost of the precise 4-2 compressor [3]. The precise 4-2 compressor [3] can be composed of 2 MUX and 4 XOR gates (28 logic gates total of 128 transistors). Fig. 3 shows the circuitry of Design 1 [10] and Fig. 6 shows the proposed design in detail. To implement Design 1 [10], it needs 9 logic gates total of 44 transistors. To implement the proposed design, it needs 12 logic gates total of 54 transistors as shown in Fig. 6. The XNOR gate can be constructed by two NAND and one OR gates; the XOR gate can be constructed by one INV, two NAND, and one OR gates. In this way, the cost of XNOR and XOR gates can be reduced [20]. Fig. 4 shows the circuitry of Design 2 [10] (8 logic gates total of 42 transistors). It needs 2 XOR, 1 OR, and the AND–OR complex compound gate (17 logic gates total of 92 transistors) to construct approximate 4-2 compressor [11]. The cost of approximate 4-2 compressor [12] is the least (4 logic gates total of 28 transistors). DQ4:2C_4 [13] is composed of approximate and supplementary parts. The approximate part needs 14 gates (60 transistors) and the supplementary part needs 20 gates (100 transistors).

In terms of the error rate, the error rate of the proposed design is the same as the error rate of Design 2 [10] and approximate 4-2 compressor [11]. The error rates of Design 1 [10], approximate 4-2 compressor [12], and DQ4:2C_4 [13] are more than 30%; of course the error rate of the precise 4-2 compressor [3] is 0%. As summarised in Table 4, the proposed 4-2 compressor has moderate power consumption, delay, and cost with a lower error rate. We expect that the proposed imprecise design will perform better image quality for image applications since the proposed design guarantees the outputs '000' and '001' are always correct. The detail analyses of image processing are described in Section 5.

Table 4 Power, delay, cost, and error rate comparisons for 4-2 compressors

Design	Power, μW	Delay, ps	Transistors/ gates	Error rate
precise 4-2 compressor [3]	*1.51*	*212.20*	*128/28*	*(0/32) 0%*
Design 1 [10]	*0.33*	*95.29*	*44/9*	*(12/32) 37.5%*
proposed design	*0.67*	*129.90*	*54/12*	*(8/32) 25%*
Design 2 [10]	0.28	89.34	42/8	(4/16) 25%
DQ4:2C_4[13]	0.54	133.20	60/14 (approximate) 100/20 (supplementary)	(5/16) 31.25%
approximate 4-2 compressor [11]	0.76	145.90	92/17	(4/16) 25%
approximate 4-2 compressor [12]	0.17	80.60	28/4	(9/16) 56.25%

italic values distinguish the structure of Multipliers 1-3 from the structure of Multipliers 4-7.

4.2 Comparisons of 8 × 8 multipliers

For the further simulations, the comparisons of the previously described seven multipliers (M1–M7) are provided in this subsection. Table 5 provides the comparisons among these multipliers. As shown in Table 5, obviously, M1 is almost the worst in each comparison because its circuitry is more complex. As expected, the cost of M1 is more than the others except for M5 which has compressors constructed by supplementary and approximate parts. In terms of the power consumption and delay, M1 is the worst and the others are better than M1; the power consumption and delay of M2 and M3 are less than M4–M7 since the structures of M4–M7 need three more compressors which results in higher power consumption and longer delay. Even though the supplementary parts of M5 are gated, it still contributes some static power consumption as mentioned before.

In terms of the energy-delay product (EDP), the EDP of M1 is the worst since the huge power consumption and longest delay of M1. Since the AND–OR complex compound gate contributes the longer delay and larger power consumption, the EDP of M6 is the worst except M1. The EDP of M2, M3, M4 and M7 are less than the others. In terms of the error rate, there are 65,536 cases (256 multiplicands and 256 multipliers). The error rate of M2 is the worst. Except for M1 and M6, the error rate of M3 (with the proposed imprecise 4-2 compressor) is the lowest. Even though the error rates of M2–M7 are high, these multipliers still can be used in

Table 5 Power, delay, EDP, cost, error rate, MED, MRED, NED, and PDP-MRED product comparisons for 8 × 8 multipliers

Designs		Power, μW	Delay, ns	EDP, ns × *fJ*	Cost (gates)	Error rate, % (65,536 cases)	MED	MRED	NED	PDP (*fJ*) × MRED
precise multiplier	*multiplier 1 (M1) (precise [3])*	*15.09*	*0.892*	*12.01*	*652 + 14FA*	*0 (0/65,536)*	*0*	*0*	*0*	
imprecise multiplier	*multiplier 2 (M2) (design 1 [10])*	*9.83*	*0.576*	*3.26*	*424 + 14FA*	*98.95 (64,846/65,536)*	*212.59*	*0.1302*	*0.0033*	*5.67 × 0.1302 = 0.738*
	multiplier 3 (M3) (proposed)	*10.09*	*0.625*	*3.94*	*460 + 14FA*	*69.84 (45,770/65,536)*	*115.41*	*0.0159*	*0.0018*	*6.31 × 0.0159 = 0.100*
	multiplier 4 (M4) (design 2 [10])	9.96	0.650	4.21	436 + 13FA	98.07 (64,273/65,536)	140.80	0.1095	0.0022	6.47 × 0.1095 = 0.708
	multiplier 5 (M5) (DQ4:2C_4 [13])	11.33	0.735	6.12	826 + 13FA	72.87 (47,757/65,536)	143.91	0.0205	0.0022	8.33 × 0.0205 = 0.171
	multiplier 6 (M6) (4-2 design [11])	12.99	0.880	10.06	571 + 13FA	42.43 (27,810/65,536)	49.05	0.0092	0.0008	10.06 × 0.0092 = 0.107
	multiplier 7 (M7) (4-2 design [12])	9.42	0.578	3.15	376 + 13FA	93.76 (61,446/65,536)	329.66	0.1142	0.0051	5.44 × 0.1142 = 0.621

italic values distinguish the structure of Multipliers 1-3 from the structure of Multipliers 4-7.

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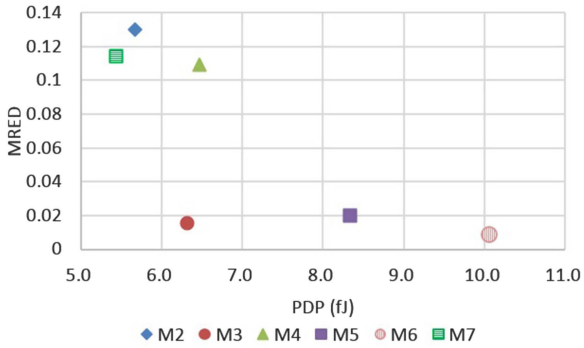

Fig. 8 *MRED and PDP of the imprecise multipliers*

Table 6 PSNR and MSSIM values of multiplier 2–7 for image sharpening

	Multiplier 2 (M2) (design 1 [10])		*Multiplier 3 (M3) (proposed)*		Multiplier 4 (M4) (design 2 [10])		Multiplier 5 (M5) (DQ4:2C4 [13])		Multiplier 6 (M6) (4-2 design [11])		Multiplier 7 (M7) (4-2 design [12])	
	PSNR, db	MSSIM	PSNR, db	MSSIM	PSNR, db	MSSIM	PSNR, dB	MSSIM	PSNR, dB	MSSIM	PSNR, dB	MSSIM
MANDRILL	24.46	0.9814	36.75	0.9968	28.05	0.9889	37.20	0.9968	41.09	0.9977	17.75	0.9251
Lena	24.11	0.9568	37.28	0.9920	27.42	0.9732	37.74	0.9919	41.52	0.9934	17.77	0.8444
Airplane	23.46	0.9715	33.93	0.9916	27.06	0.9831	34.23	0.9912	43.76	0.9950	17.43	0.9224
Sailboat	24.42	0.9585	36.30	0.9935	27.87	0.9770	36.58	0.9933	41.22	0.9952	17.54	0.8309
Peppers	24.12	0.9217	36.89	0.9918	27.40	0.9422	37.34	0.9913	41.86	0.9934	17.82	0.8265
House	23.79	0.9730	35.98	0.9944	26.87	0.9829	36.12	0.9942	43.02	0.9963	17.84	0.9243
average PSNR & MSSIM	24.06	0.9605	36.19	0.9934	27.45	0.9746	36.54	0.9931	42.08	0.9952	17.69	0.8789

italic values distinguish the structure of Multipliers 1-3 from the structure of Multipliers 4-7.

image processing since these hybrid schemes can make the outputs more precise. In the next section, the error metrics and the detail analyses of M2–M7 for image processing are described.

5 Error metrics and application: image processing

5.1 Error metrics

This section presents error metrics to evaluate the reliability of multipliers (M1–M7). The output quality of imprecise multipliers can be determined by the error distance (ED). The mean ED (MED) is the mean value of the EDs and the MRED is based on the calculation of EDs divided by the exact outputs. The MED and the MRED are defined as [13, 21]

$$\mathrm{MED} = \frac{1}{2^{2n}} \sum_{i=1}^{2^{2n}} |\mathrm{ED}_i| \tag{7}$$

$$\mathrm{MRED} = \frac{1}{2^{2n}} \sum_{i=1}^{2^{2n}} \frac{|\mathrm{ED}_i|}{S_i} \tag{8}$$

The ED_i is the difference between the precise output and the imprecise output. The S_i is the exact output of ith input. To compare the imprecise multipliers almost independent of their sizes, the NED is defined as [13, 21]

$$\mathrm{NED} = \frac{\mathrm{MED}}{D} = \frac{\mathrm{MED}}{\left(2^n - 1\right)^2} = \frac{1}{\left(2^n - 1\right)^2} \sum_{i=1}^{2^{2n}} \frac{|\mathrm{ED}_i|}{2^{2n}} \tag{9}$$

D is the maximum error value of an imprecise multiplier. Table 5 provides the MED, MRED, and NED of each multiplier. M1 is the precise multiplier, thus, the MED, MRED, and NED are 0. As shown in Table 5, the multiplier with the proposed compressor (M3) has the lowest MED, MRED, and NED except for M6. Moreover, M6 has the larger EDP than M3. Compared to M4 (constructed by Design 2 [10] which has the same error rate as the proposed 4-2 compressor), M3 also has the lowest MED, MRED, and NED that show the superiority of the proposed imprecise 4-2 compressor.

To investigate the energy efficiency and accuracies of the multipliers, we consider the PDP and MRED to evaluate M2–M7 as in [22, 23]. Fig. 8 shows MRED and PDP of M2–M7. As shown in Fig. 8, M3 has the lower MRED and moderate PDP. M2 and M7 have the lower PDPs but their MREDs are worse. M4 has the moderate PDP but has relatively poor MRED. M5 has high accuracy but high PDP. M6 has the best MRED, however, M6 has the largest PDP. Table 5 provides the PDP-MRED products of each multiplier. As shown in Table 5, M3 has the smaller PDP with high accuracy, thus, M3 has the smallest PDP-MRED product. Fig. 8 and PDP-MRED products in Table 5 show the superiority of the proposed imprecise 4-2 compressor compared with the other designs.

5.2 Image processing

This section presents an image processing application which using the 8×8 unsigned multipliers (M2–M7). For a solid result, the image sharpening algorithm [24] is used to evaluate the impact of the PSNR by implementing in Matlab. The PSNR is based on the mean square error (MSE) to estimate the image quality. The MSE and PSNR are defined as

$$\mathrm{MSE} = \frac{1}{mn} \sum_{i=0}^{m-1} \sum_{j=0}^{n-1} [I(i,j) - K(i,j)]^2 \tag{10}$$

$$\mathrm{PSNR} = 10 \cdot \log_{10}\left(\frac{\mathrm{MAX}_\mathrm{I}^2}{\mathrm{MSE}}\right) \tag{11}$$

m and n are the image dimensions. $I(i, j)$ and $K(i, j)$ represent the accurate and approximate values of each pixel, respectively. MAX_I is the maximum possible pixel value in the image. For instance, if a pixel value is represented by eight bits, then, its maximum value is 255.

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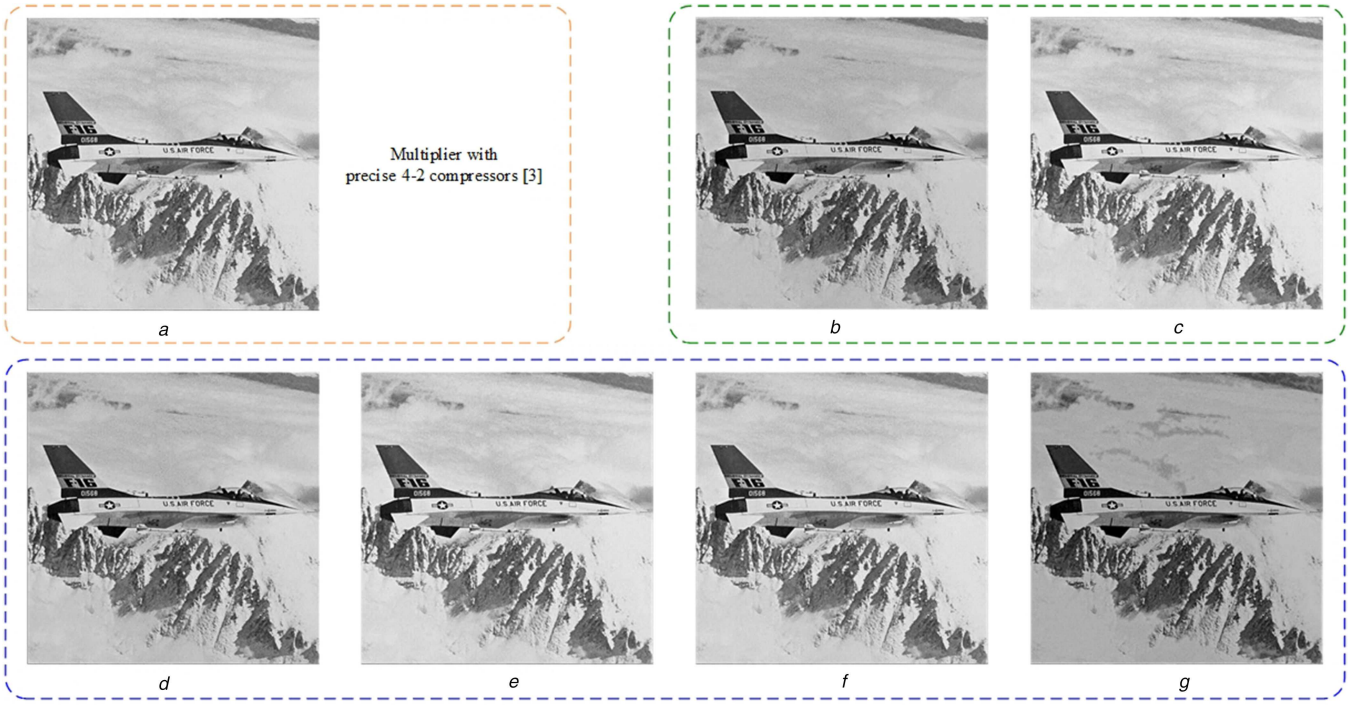

Fig. 9 *Sharpened Airplane images with the following multipliers*
(a) M1 (precise) (M1 (Precise [3])), ***(b)*** M2 (23.46 dB) (M2 (Design 1 [10])), ***(c)*** M3 (33.93 dB) (M3 (Proposed design)), ***(d)*** M4 (27.06 dB) (M4 (Design 2 [10])), ***(e)*** M5 (34.23 dB) (M5 (DQ4:2C4 [13])), ***(f)*** M6 (43.76 dB) (M6 (Approximate 4-2 compressor [11])), ***(g)*** M7 (17.43 dB) (M7 (Approximate 4-2 compressor [12]))

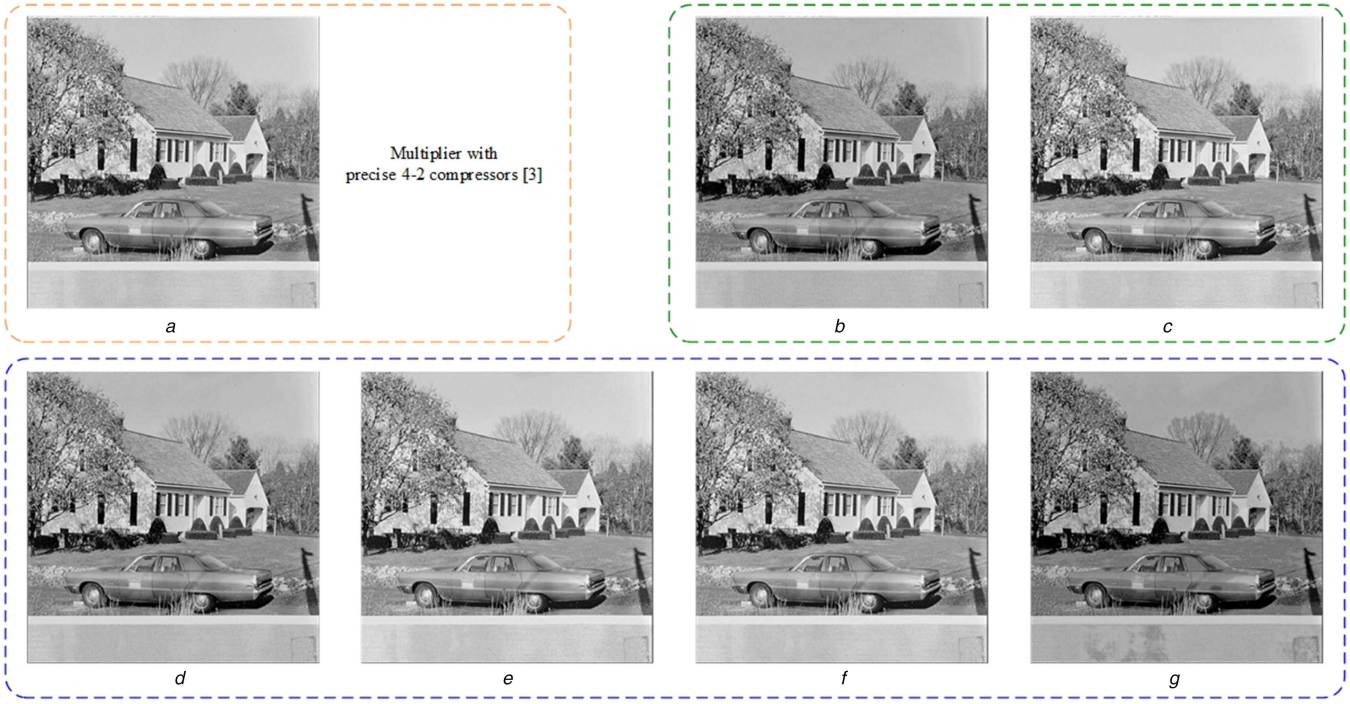

Fig. 10 *Sharpened House images with the following multipliers*
(a) M1 (precise) (M1 (Precise [3])), ***(b)*** M2 (23.79 dB) (M2 (Design 1 [10])), ***(c)*** M3 (35.98 dB) (M3 (Proposed design)), ***(d)*** M4 (26.87 dB) (M4 (Design 2 [10])), ***(e)*** M5 (36.12 dB) (M5 (DQ4:2C$_4$ [13])), ***(f)*** M6 (43.02 dB) (M6 (Approximate 4-2 compressor [11])), ***(g)*** M7 (17.84 dB) (M7 (Approximate 4-2 compressor [12]))

We adopt a Gaussian smoothing-based image sharpening filter and the sharpening algorithm of [24] performs as

$$S(x, y) = 2I(x, y) - R(x, y) \tag{12}$$

I is the original image, R is the Gaussian blurred image, and $S$is the sharpened image. First, Gaussian smoothing is performed on the original image I, and this can be done by convolving I with the following matrix $\boldsymbol{G}$:

$$\boldsymbol{G} = \begin{bmatrix} 1 & 4 & 7 & 4 & 1 \\ 4 & 16 & 26 & 16 & 4 \\ 7 & 26 & 41 & 26 & 7 \\ 4 & 16 & 26 & 16 & 4 \\ 1 & 4 & 7 & 4 & 1 \end{bmatrix} \tag{13}$$

The Gaussian blurred image R can be obtained by (14) as defined as follows:

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$$R(x,y)=\frac{1}{273}\sum_{i=-2}^{2}\sum_{j=-2}^{2}\boldsymbol{G}(i+3,j+3)I(x-i,y-j) \quad (14)$$

Finally, the sharpened image S is obtained by using (12).

We also provided the MSSIM to measure the structural similarity of the precise and imprecise images. The MSSIM can be obtained as follows:

$$\begin{aligned}\mathrm{SSIM}(I,R)&=[l(I,R)]^{\alpha}[c(I,R)]^{\beta}[s(I,R)]^{\gamma}\\&=\frac{(2\mu_I\mu_R+c_1)(2\sigma_{IR}+c_2)}{\left(\mu_I^2+\mu_R^2+c_1\right)\left(\sigma_I^2+\sigma_R^2+c_2\right)}\end{aligned} \quad (15)$$

$$\mathrm{MSSIM}(I,R)=\frac{1}{M}\sum_{j=1}^{M}\mathrm{SSIM}(I_j,R_j) \quad (16)$$

The structural similarity of an image is composed of luminance measurement $l(I, R)$, contrast comparison $c(I, R)$ and structure comparison $s(I, R)$. The details of the parameters are explained in [25, 26].

Six sample images (Mandrill, Lena, Airplane, Sailboat, Peppers, and House as shown in Fig. 5) are selected for the sharpening algorithm with M1–M7. Although M3 consumes more power than M2 (2.64%), M4 (1.31%), and M7 (7.11%), we expect that M3 has better image quality. Table 6 shows the PSNR and MSSIM comparisons among multipliers in image sharpening. Compared with M2, M3 can achieve 50.42% PSNR and 3.43% MSSIM improvement on average. Compared with M4 (M7), M3 can achieve 31.84% (104.58%) PSNR and 1.93% (13.03%) MSSIM improvement in average. For all multipliers, in terms of PSNR and MSSIM, M3, M5, and M6 have higher PSNRs and MSSIMs, M6 especially. Since M6 has the lowest MRED, M6 has a higher PSNR and MSSIM. However, the proposed design M3 has less power consumption and delay with high image quality than M5 and M6. Even if the error rate of DQ4:2C_4 [13] is higher, the image quality of M5 is better than the image quality of M4 because some error outputs of Design 2 [10] directly affect the image quality but the error outputs of DQ4:2C_4 [13] do not.

We tested six sample images and chose two of them (Airplane and House) to describe. Figs. 9 and 10 show the sharpened results for the two sample images. In Figs. 9*b* and *g*, the colour of clouds becomes grey and some noises appear on the clouds. In Fig. 9*d*, the details of clouds are absent. In Figs. 10*b*, *d* and *g*, there are some spots and noises on the background, especially the sky and the ground. As shown in Figs. 9 and 10, the image qualities of M3, M5, and M6 are similar to M1.

6 Conclusion

This paper presents a novel imprecise 4-2 compressor to improve energy-quality efficiency of image processing applications. By analysing the features of precise 4-2 compressor outputs the proposed imprecise 4-2 compressor can improve the quality of images and error rate. Compared to the precise 4-2 compressor, the proposed imprecise 4-2 compressor can reduce power consumption and delay by 56 and 39%, respectively. Compared to the precise multiplier, the multiplier which uses the proposed imprecise design can save 33% power consumption and achieve 30% improvement in delay. Multiplier M3 which adopts the proposed imprecise 4-2 compressor can achieve PSNR and MSSIM above 33 and 0.99 in average, respectively. In addition, multiplier M3 has the smallest PDP-MRED product that shows the proposed design can improve the accuracy and maintain both the high power efficiency and low circuit complexity.

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