Reset (Start Signal)	Top Module States	Adder States	Cycles	Result
0	ldle	Idle	-	No Result
1	ldle	Idle	-	No Result
0	shift_and_compress	Idle	1	No Result
0	shift_and_compress	Idle	2	No Result
0	shift_and_compress	Idle	3	No Result
0	shift_and_compress	Idle	4	No Result
0	shift_and_compress	Idle	5	No Result
1	ldle	Idle	-	No Result
0	shift_and_compress	Add	1	No Result
0	shift_and_compress	Add	2	No Result
0	shift_and_compress	Add	3	No Result
0	shift_and_compress	Add	4	No Result
0	shift_and_compress	Add	5	No Result
1	ldle	Idle	-	First Result
0	shift_and_compress	Add	1	First Result
0	shift_and_compress	Add	2	First Result
0	shift_and_compress	Add	3	First Result
0	shift_and_compress	Add	4	First Result
0	shift_and_compress	Add	5	Wrong Result
0	ldle	Idle	-	Second Result
0	ldle	Add	1	Second Result
0	ldle	Add	2	Second Result
0	ldle	Add	3	Second Result
0	ldle	Add	4	Second Result
0	ldle	Add	5	Wrong Result
0	ldle	Idle	-	Third Result
0	ldle	Idle	-	Third Result
0	ldle	Idle	-	Third Result
0	ldle	Idle	-	Third Result
0	ldle	Idle	-	Third Result
0	ldle	Idle	-	Third Result
0	ldle	Idle	-	Third Result