Arab Academy for Science, Technology & Maritime Transport

College of Engineering & Technology

Computer Engineering Department

Project Report

Course Title: Computer Architecture

Course Code: CC311

Semester: Spring 2021

Lecturer Name: Dr/ Ahmed AbouElfarag

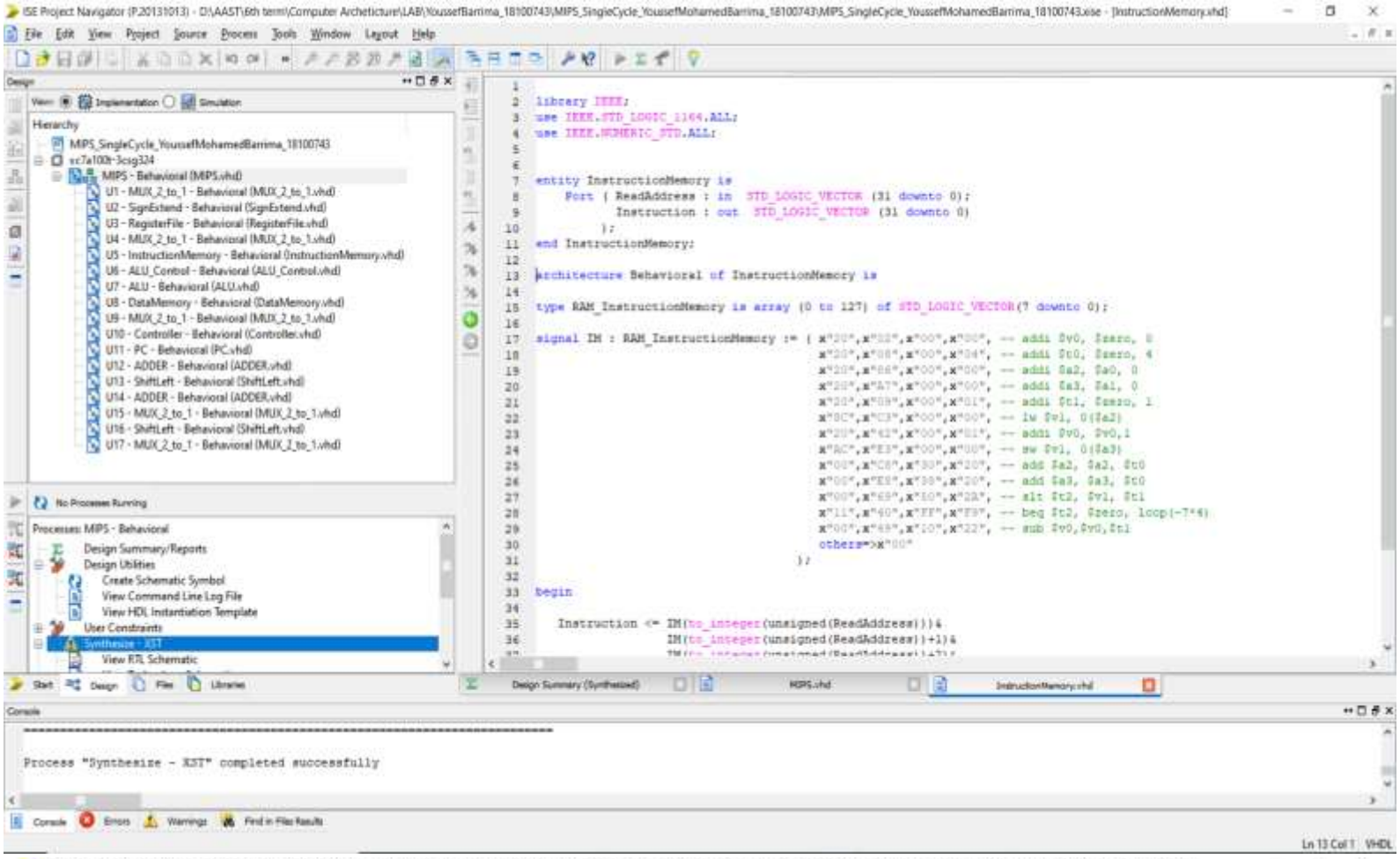
Single Cycle MIPS Processor Using VHDL

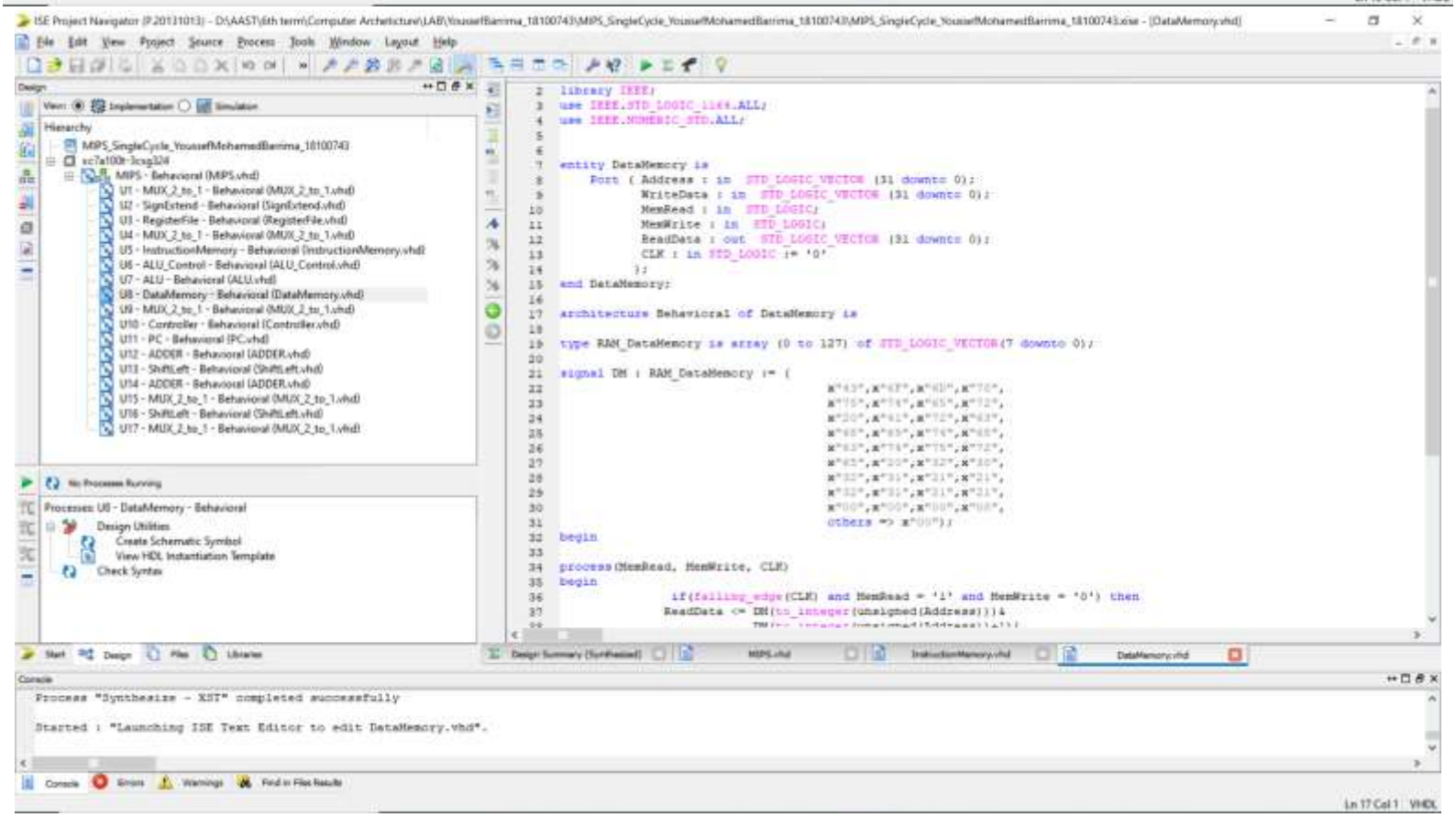
Subscribed and Presented by:

Student Name: Youssef Mohamed Alaa Elsaied Barrima

Registration #: 18100743

Department: Computer Engineering


ISE Project Navigator (P.20131013) - D:\AAST\6th term\Computer Archeticture\LAB\YousefBarnima_18100743\MIPS_SingleCycle_YousefMohamedBarnima_18100743\MIPS_SingleCycle_YousefMohamedBarnima_18100743.ise - [InstructionMemory.vhd]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
MIPS_SingleCycle_YousefMohamedBarnima_18100743
xc7a100t-3csg324
MIPS - Behavioral (MIPS.vhd)
U1 - MUX_2_to_1 - Behavioral (MUX_2_to_1.vhd)
U2 - SignExtend - Behavioral (SignExtend.vhd)
U3 - RegisterFile - Behavioral (RegisterFile.vhd)
U4 - MUX_2_to_1 - Behavioral (MUX_2_to_1.vhd)
U5 - InstructionMemory - Behavioral (InstructionMemory.vhd)
U6 - ALU_Control - Behavioral (ALU_Control.vhd)
U7 - ALU - Behavioral (ALU.vhd)
U8 - DataMemory - Behavioral (DataMemory.vhd)
U9 - MUX_2_to_1 - Behavioral (MUX_2_to_1.vhd)
U10 - Controller - Behavioral (Controller.vhd)
U11 - PC - Behavioral (PC.vhd)
U12 - ADDER - Behavioral (ADDER.vhd)
U13 - ShiftLeft - Behavioral (ShiftLeft.vhd)
U14 - ADDER - Behavioral (ADDER.vhd)
U15 - MUX_2_to_1 - Behavioral (MUX_2_to_1.vhd)
U16 - ShiftLeft - Behavioral (ShiftLeft.vhd)
U17 - MUX_2_to_1 - Behavioral (MUX_2_to_1.vhd)
No Processes Running
Processes: MIPS - Behavioral
Design Summary/Reports
Design Utilities
Create Schematic Symbol
View Command Line Log File
View HDL Instantiation Template
User Constraints
Synthesize - XST
View RTL Schematic
Start Design Files Libraries
Design Summary (Synthesized) MIPS.vhd InstructionMemory.vhd
1 library IEEE;
2 use IEEE.STD_LOGIC_1164.ALL;
3 use IEEE.NUMERIC_STD.ALL;
4
5
6 entity InstructionMemory is
7 Port (ReadAddress : in STD_LOGIC_VECTOR (31 downto 0);
8 Instruction : out STD_LOGIC_VECTOR (31 downto 0)
9);
10 end InstructionMemory;
11
12 architecture Behavioral of InstructionMemory is
13
14 type RAM_InstructionMemory is array (0 to 127) of STD_LOGIC_VECTOR(7 downto 0);
15
16 signal IM : RAM_InstructionMemory := (x"20",x"02",x"00",x"00", -- addi $v0, $zero, 0
17 x"20",x"08",x"00",x"04", -- addi $t0, $zero, 4
18 x"20",x"86",x"00",x"00", -- addi $a2, $a0, 0
19 x"20",x"A7",x"00",x"00", -- addi $a3, $a1, 0
20 x"20",x"09",x"00",x"01", -- addi $t1, $zero, 1
21 x"8C",x"C3",x"00",x"00", -- lw $v1, 0($a2)
22 x"20",x"42",x"00",x"01", -- addi $v0, $v0,1
23 x"AC",x"E3",x"00",x"00", -- sw $v1, 0($a3)
24 x"00",x"C8",x"30",x"20", -- add $a2, $a2, $t0
25 x"00",x"E8",x"38",x"20", -- add $a3, $a3, $t0
26 x"00",x"48",x"10",x"2A", -- slt $t2, $v1, $t1
27 x"11",x"40",x"FF",x"F9", -- beq $t2, $zero, loop(-7*4)
28 x"00",x"49",x"10",x"22", -- sub $v0,$v0,$t1
29 others=>x"00"
30);
31
32 begin
33
34 Instruction <= IM(to_integer(unsigned(ReadAddress)))&
35 IM(to_integer(unsigned(ReadAddress))+1)&
Console
Process "Synthesize - XST" completed successfully
Console Errors Warnings Find in Files Results
Ln 13 Col 1 VHDL


ISE Project Navigator (P.20131013) - D:\AAST\6th term\Computer Archeticture\LAB\YousefBarnima_18100743\MIPS_SingleCycle_YousefMohamedBarnima_18100743\MIPS_SingleCycle_YousefMohamedBarnima_18100743.ise - [DataMemory.vhd]
File Edit View Project Source Process Tools Window Layout Help
Design
View: Implementation Simulation
Hierarchy
MIPS_SingleCycle_YousefMohamedBarnima_18100743
xc7a100t-3csg324
MIPS - Behavioral (MIPS.vhd)
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U4 - MUX_2_to_1 - Behavioral (MUX_2_to_1.vhd)
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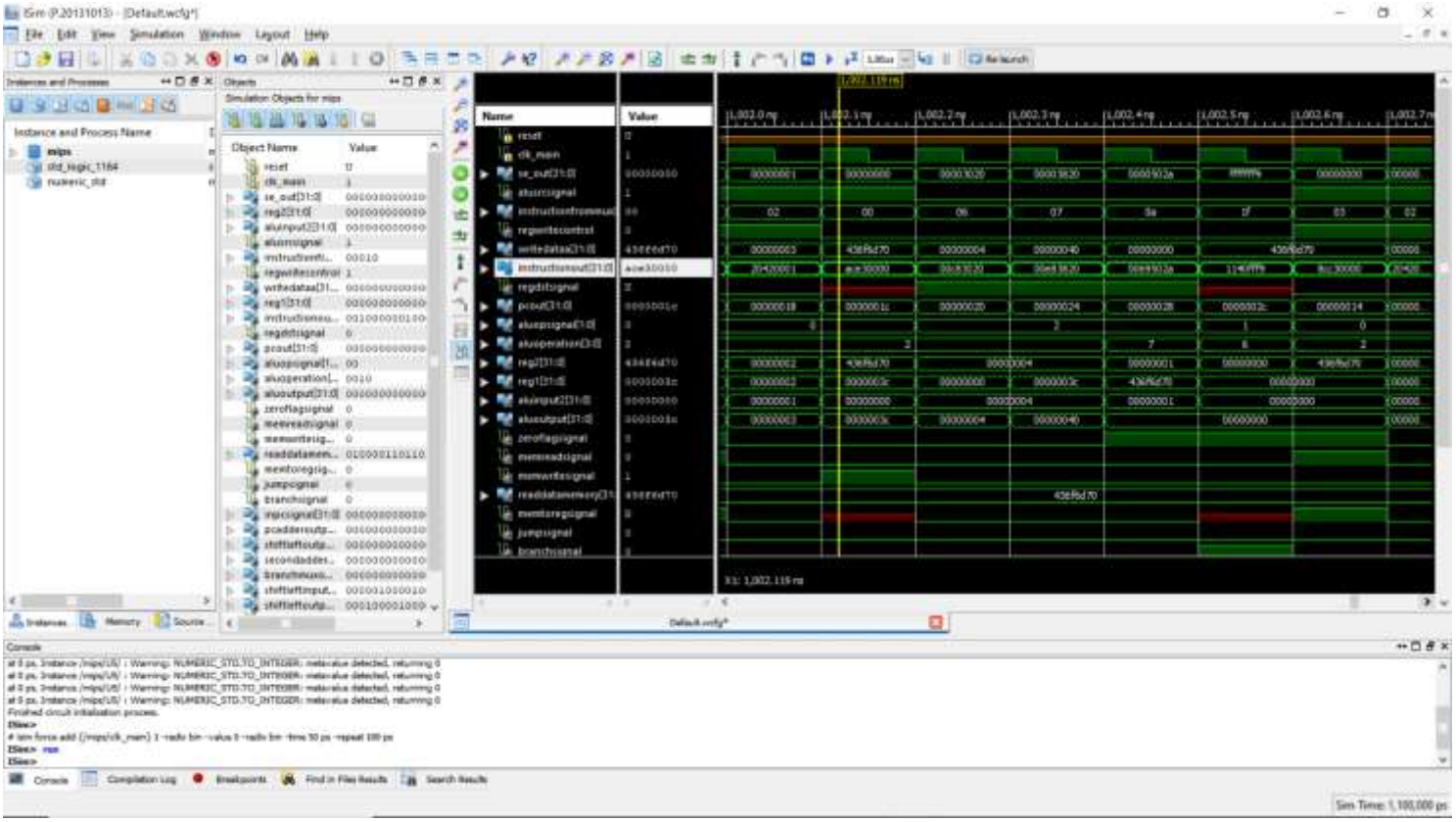
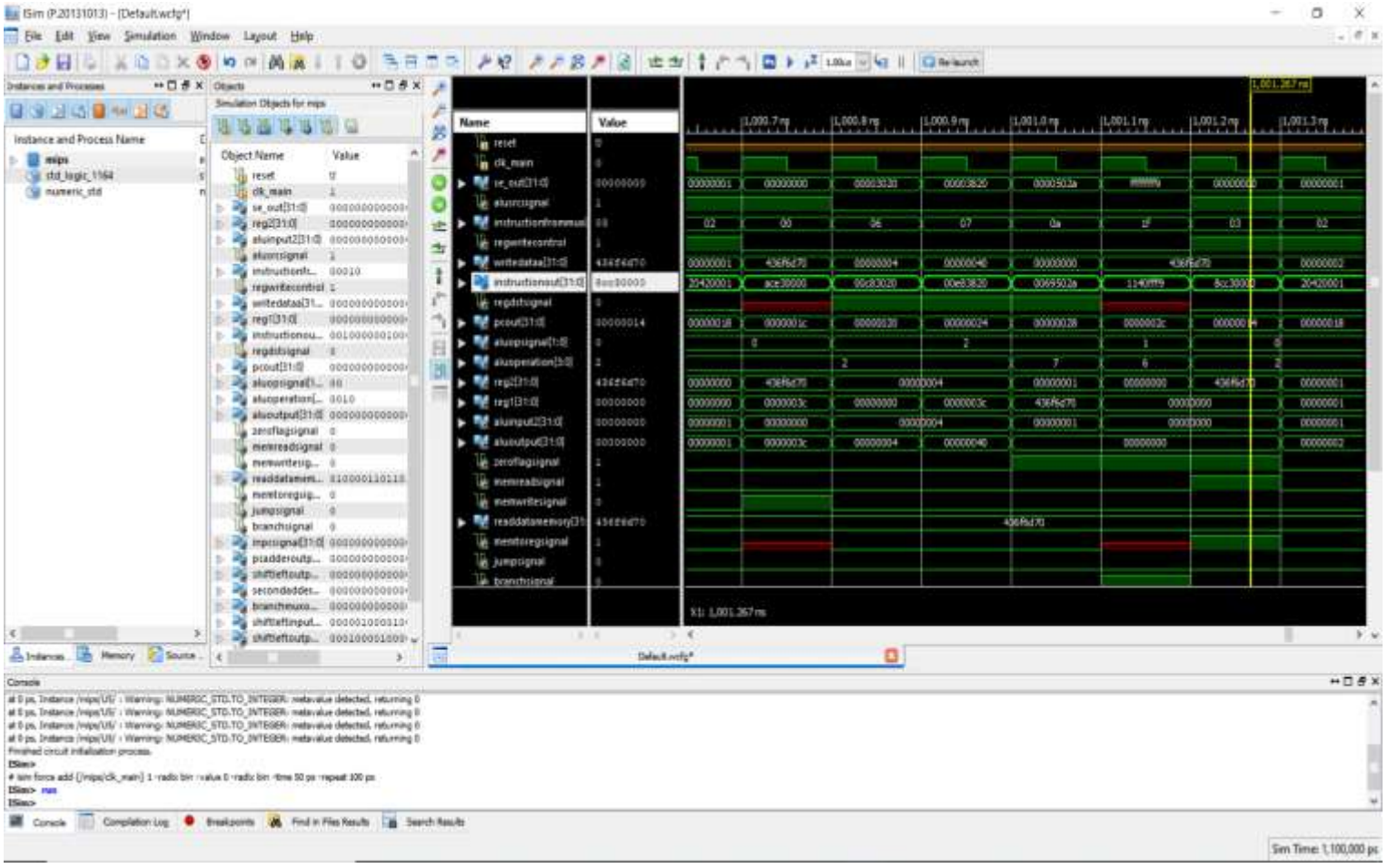
U14 - ADDER - Behavioral (ADDER.vhd)
U15 - MUX_2_to_1 - Behavioral (MUX_2_to_1.vhd)
U16 - ShiftLeft - Behavioral (ShiftLeft.vhd)
U17 - MUX_2_to_1 - Behavioral (MUX_2_to_1.vhd)
No Processes Running
Processes: U8 - DataMemory - Behavioral
Design Utilities
Create Schematic Symbol
View HDL Instantiation Template
Check Syntax
Start Design Files Libraries
Design Summary (Synthesized) MIPS.vhd InstructionMemory.vhd DataMemory.vhd
2 library IEEE;
3 use IEEE.STD_LOGIC_1164.ALL;
4 use IEEE.NUMERIC_STD.ALL;
5
6
7 entity DataMemory is
8 Port (Address : in STD_LOGIC_VECTOR (31 downto 0);
9 WriteData : in STD_LOGIC_VECTOR (31 downto 0);
10 MemRead : in STD_LOGIC;
11 MemWrite : in STD_LOGIC;
12 ReadData : out STD_LOGIC_VECTOR (31 downto 0);
13 CLK : in STD_LOGIC := '0'
14);
15 end DataMemory;
16
17 architecture Behavioral of DataMemory is
18
19 type RAM_DataMemory is array (0 to 127) of STD_LOGIC_VECTOR(7 downto 0);
20
21 signal DM : RAM_DataMemory := (
22 x"43",x"6F",x"6D",x"70",
23 x"75",x"74",x"65",x"72",
24 x"20",x"41",x"72",x"63",
25 x"68",x"65",x"74",x"65",
26 x"63",x"74",x"75",x"72",
27 x"65",x"20",x"32",x"30",
28 x"32",x"31",x"21",x"21",
29 x"32",x"31",x"31",x"21",
30 x"00",x"00",x"00",x"00",
31 others => x"00");
32 begin
33
34 process(MemRead, MemWrite, CLK)
35 begin
36 if(falling_edge(CLK) and MemRead = '1' and MemWrite = '0') then
37 ReadData <= DM(to_integer(unsigned(Address)))&
Console
Process "Synthesize - XST" completed successfully
Started : "Launching ISE Text Editor to edit DataMemory.vhd".
Console Errors Warnings Find in Files Results
Ln 17 Col 1 VHDL


ISim (P.20131013) - [Default.wcfg*]
File Edit View Simulation Window Layout Help
Instance and Process Name
mips
std_logic_1164
numeric_std
Object Name
Value
Simulation Objects for mips
Name
Value
reset
clk_main
Default.wcfg*
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,100,000 ps


ISim (P.20131013) - [Default.wcfg*]
File Edit View Simulation Window Layout Help
Instance and Process Name
mips
std_logic_1164
numeric_std
Object Name
Value
Simulation Objects for mips
Name
Value
reset
clk_main
Default.wcfg*
Console
Compilation Log
Breakpoints
Find in Files Results
Search Results
Sim Time: 1,100,000 ps