



XAPP383 (v1.1) August 1, 2003

Single Error Correction and Double Error Detection (SECDED) with CoolRunner-II™ CPLDs

Summary

This application note describes the implementation of a single error correction, double error detection (SECDED) design with a CoolRunner-II™ CPLD. CoolRunner-II devices are the latest CPLD from Xilinx that offer both low power and high-speed performance. A complete VHDL design is available with this application note, see [VHDL Code, page 4](#).

This design is a model of the Hamming code developed by R. Hamming (see [References, page 4](#) for more information). SECDED for N bits of data requires K parity bits to be stored with the data where:

$$N \leq 2^K - 1 - K$$

If the bits are numbered in sequence, those bit positions that represent powers of two are dedicated to parity bits. [Table 1](#) illustrates how the 16-bit data word and parity bits are stored in memory.

Table 1: Hamming Code Data and Parity Bits

Bit Position	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
Bit Number	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Data/Parity Bit	P5	D ₁₅	D ₁₄	D ₁₃	D ₁₂	D ₁₁	P4	D ₁₀	D9	D8	D7	D6	D5	D4	P3	D3	D2	D1	P2	D0	P1	P0

The parity bits P0-P4 are created for single error detection and correction and are created as follows:

$$\begin{aligned}
 P0 &= D15 \oplus D13 \oplus D11 \oplus D10 \oplus D8 \oplus D6 \oplus D4 \oplus D3 \oplus D1 \oplus D0 \\
 P1 &= D13 \oplus D12 \oplus D10 \oplus D9 \oplus D6 \oplus D5 \oplus D3 \oplus D2 \oplus D0 \\
 P2 &= D15 \oplus D14 \oplus D10 \oplus D9 \oplus D8 \oplus D7 \oplus D3 \oplus D2 \oplus D1 \\
 P3 &= D10 \oplus D9 \oplus D8 \oplus D7 \oplus D6 \oplus D5 \oplus D4 \\
 P4 &= D15 \oplus D14 \oplus D13 \oplus D12 \oplus D11
 \end{aligned}$$

One additional parity bit, P5, detects double errors that are not correctable. This extra parity bit is an overall parity bit and is comprised by XOR-ing all the data bits, D15-D0 and parity bits, P0-P4.

The syndrome is created upon a memory read and provides the ability to correct single bit errors. The syndrome is created by XOR-ing the parity bits read out of memory with the newly created set of parity bits from the data stored in memory. The value of the syndrome will indicate the bit position in error (if a single error has occurred). **Table 2** illustrates the value of the syndrome and the overall parity bit in detecting both single and double errors.

Table 2: Error Detection

Syndrome	Overall Parity (P5)	Error Type	Notes
0	0	No Error	
/=0	1	Single Error	Correctable. Syndrome holds incorrect bit position.
/=0	0	Double Error	Not correctable.
0	1	Parity Error	Overall parity, P5 is in error and can be corrected.

SECDED Design

Figure 1 illustrates the block level design of the SECDED for the CoolRunner-II CPLD. The left side of the diagram illustrates the processor interface. This interface consists of the 16-bit processor data bus, u_data[15:0], the read/write control signal, rw_n, and the error flag signal, error_out[1:0]. The right hand side describes the memory component interface, consisting of the memory data bus, mem_data[21:0].

The rw_n control signal from the processor switches the CPLD between read and write cycles. The rw_n signal will be equal to "1" for a processor read cycle and equal to "0" for a processor write cycle.

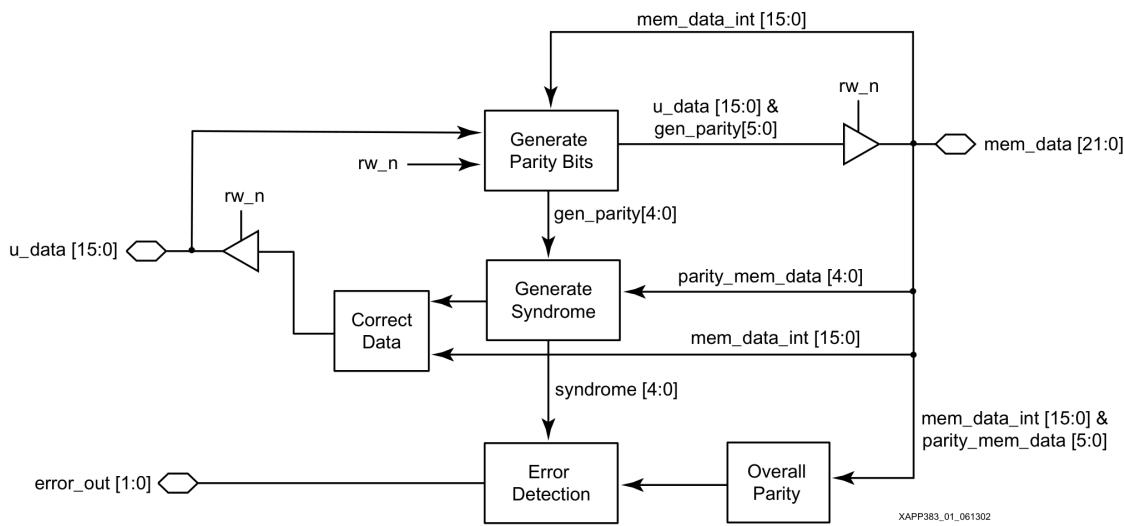


Figure 1: SECDED Block Diagram

The "Generate Parity Bits" block creates the parity bits to store with the processor data ($u_data[15:0]$) during a write cycle. In a read cycle, this block is also responsible for creating one of the inputs in generating the syndrome; this block creates the parity bits with the data word stored in memory.

The "Error Detection" block generates the $error_out[1:0]$ flag based on the syndrome and the overall parity created from the data in memory. The $error_out$ flag decodes to the states shown in Table 3.

Table 3: Error Detection Flags

error_out[1:0]	Description
00	No error has occurred.
01	Single error has been detected. Syndrome holds value of erroneous bit.
10	Double error has been detected. Not correctable
11	Parity error has occurred. Correctable.

The design illustrated here only describes the data path logic between the processor and memory device. This design can be expanded to include the control logic for interfacing with both the processor and memory device(s).

Review Week ⚡ 9

2022 - 11 - 21

CYCLIC CODES

Review Week 09

2022-11-21

Cyclic codes (with a worked example in \mathbb{F}_2^7)

Reminder - Def:

A cyclic code is $C \subseteq \mathbb{F}_q^n$ such that

- * C is linear;
- * $\forall c = (c_0, c_1, \dots, c_{n-1}) \in C$,
- $s(c) = (c_{n-1}, c_0, c_1, \dots, c_{n-2}) \in C$

Correspondence vectors \leftrightarrow polynomials:

$$\underline{C} = (c_0, c_1, \dots, \underline{c_{n-1}})$$

\downarrow maybe 0

$$\begin{aligned} C(x) &= c_0 + c_1 x + \dots \\ &\quad + \underline{c_{n-1}} x^{n-1} \\ &\in \mathbb{F}_q[x] \end{aligned}$$

Main result about cyclic codes: E. Prange, 1957

C cyclic $\Rightarrow \exists!$ generator polynomial of C ,
 $g(x) \in C$ such that $g(x)$ is monic

(leading coeff 1)

and

$$C = \{ u(x) \underline{g(x)} \mid u(x) \in \mathbb{F}_q[x], \deg u(x) g(x) < n \}$$

Important: $g(x)$ is a divisor of $x^n - 1 \in \mathbb{F}_q[x]$
 so $x^n - 1 = g(x) h(x)$ in $\mathbb{F}_q[x]$.

The generator polynomial of a cyclic C
 is the monic polynomial of C
 code

of the lowest degree in C .

EX

$$E_3 = \{ 000, 110, 101, 011 \}$$

code polynomials

$$\begin{aligned} (1+x)(1+x) &= \\ &= 1 + x^2 \end{aligned}$$

$$\begin{aligned} &\text{S} \quad \text{S} \quad \text{S} \quad \text{S} \\ &\downarrow \quad \downarrow \quad \downarrow \quad \downarrow \\ &0 \quad 1+x \quad 1+0x+x^2 \quad x+x^2 \\ &\cancel{\times} \quad \boxed{\begin{array}{l} \text{deg}=1 \\ g(x) \end{array}} \quad \boxed{\begin{array}{l} \text{deg}=2 \\ 1+x^2 \end{array}} \quad \begin{array}{l} \text{deg}=2 \\ \text{if } (a+b)^2 = a^2 + b^2 \end{array} \end{aligned}$$

If C is cyclic with generator polynomial $g(x)$,
easy to detect errors when C is used
for transmitting information:

$$\begin{array}{l} \text{received vector } y \in \mathbb{F}_q^n \Leftrightarrow y(x) \in \mathbb{F}_q[x] \\ \boxed{y(x) \in C} \Leftrightarrow \left\{ \begin{array}{l} \text{the remainder when } y(x) \\ \text{is divided by } g(x) \text{ is } 0. \end{array} \right. \end{array}$$

SKILL Divide $y(x)$ by $g(x)$ in $\mathbb{F}_q[x]$
with remainder

⌚ $y(x) = g(x) Q(x) + R(x)$
includes $R=0 \Rightarrow \deg R < \deg g$

IMPORTANT Long division over \mathbb{F}_q
 $q=2, 3, 5, 7$ (ii)?

Constructing cyclic codes: Factorise $x^n - 1$ over \mathbb{F}_q into irreducible monic factors. Possible $g(x)$ are obtained by multiplying some of those factors.

Ex. Classify all cyclic codes $C \subseteq \mathbb{F}_2^7$.

$$x^7 - 1$$

$$x^7 - 1 = (x-1)(x^6 + x^5 + x^4 + x^3 + x^2 + x + 1)$$

IMPORTANT

$g(x)$ is always a factor of the polynomial $x^n - 1$ in $\mathbb{F}_q[x]$

All possible cyclic codes in \mathbb{F}_q^n



$$x^n - 1 = P_1(x) P_2(x) \cdots P_s(x)$$

and

↑ monic irreducible

$g(x)$ is a product of several of the $P_1(x), \dots, P_s(x)$

$$g(x) = g_0 + g_1 x + \cdots + g_{n-k} x^{n-k}$$

$$x^n - 1 = g(x) h(x)$$

check polynomial

$$h(x) = h_0 + h_1 x + \cdots + h_k x^k$$

$$G = \left[\begin{array}{cccccc|c|c} g_0 & g_1 & \cdots & g_{n-k} & 0 & \cdots & 0 \\ 0 & g_0 & g_1 & \cdots & g_{n-k} & 0 & \cdots & 0 \\ \vdots & & & & & & & \\ g_0 & g_1 & \cdots & \cdots & \cdots & g_{n-k} & & \end{array} \right] \quad \left. \begin{array}{l} k \text{ rows} \\ g_{n-k} = 1 \end{array} \right\}$$

$$\dim C = n - \deg g(x)$$

$$H = \left[\begin{array}{cccccc|c} h_k & h_{k-1} & \cdots & h_0 & 0 & 0 & \cdots & 0 \\ 0 & h_k & \cdots & \cdots & h_0 & 0 & \cdots & 0 \\ \vdots & & & & & & & \\ h_k & \cdots & \cdots & h_0 & & & & \end{array} \right] \quad \left. \begin{array}{l} n-k \text{ rows} \end{array} \right\}$$

$$x^7 - 1 = (x-1)(x^6 + x^5 + x^4 + x^3 + x^2 + x + 1)$$

$$\boxed{(x+1)}$$

$$\boxed{\mathbb{F}_2}$$

$g(x) \subset C$?

$$\boxed{g(x) = 1+x}$$

$$h(x) = x^6 + \cdots + x + 1$$

$$H = [1 \ 1 \ 1 \ 1 \ 1 \ 1 \ 1]$$

$$\boxed{k = n - \deg g = 6}$$

$$\boxed{n-k=1}$$

$$C = \left\{ \underline{v} \in \mathbb{F}_2^7 : v_1 + v_2 + \dots + v_7 = 0 \right\}$$

$\approx E_7$