# Low-k Interconnect Stack with multi-layer Air Gap and Tri-Metal-Insulator-Metal Capacitors for 14nm High Volume Manufacturing

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**Abstract**

We describe here Intel's 14nm high-performance logic technology interconnects and back end stack featuring 13 metal layers and a tri-metal laminated metal-insulator-metal (MIM) capacitor. For the first time on a logic product in high volume, multiple layers (M4 and M6) incorporate an air gap integration scheme to deliver up to 17% RC benefit. Pitch Division patterning is introduced to deliver high yield capable interconnect layers with a minimum pitch of 52nm.

**Introduction**

This manuscript is an overview of Intel's 14nm back end interconnect process. The full integrated 14nm process was described in [1]. The Back End (BE) stack features 13 metal layers (Fig. 1) and has been scaled from the previous generation Intel technology interconnect stacks [2,3] on a traditional trajectory to provide density scaling in line with Moore's Law.

In this process, a pitch division scheme is utilized to deliver interconnect pitches less than 80nm. A minimum pitch of 52nm is achieved at M2, delivering 65% scaling reduction from Intel's 22nm process [2]. For resistance and capacitance performance improvements, ultra-low k (ULK) carbon doped oxide (CDO) dielectrics and scaled reduced k etch stops (ES) are used. For improved performance, Air Gaps (AG) are introduced at layers with the greatest need for performance. All layers with pitches tighter than 240nm employ a Self Aligned Via (SAV) process with sacrificial hard mask [4]. Layers with a looser pitch use a via-first process.

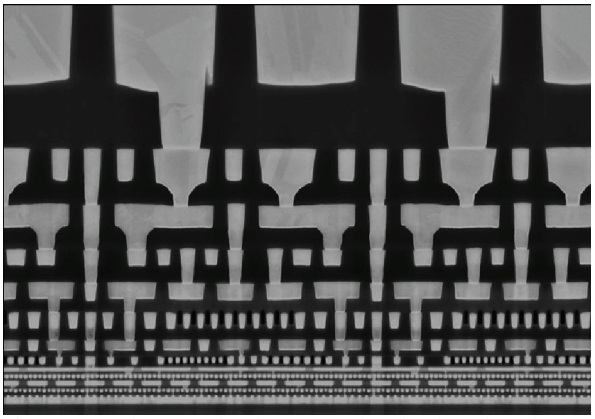

Figure 1: Metal 0 – Metal 11 in cross section showing Via and Trench profiles.

In this process, a thick oxide BE metal layer is introduced at M11 using an SiO2 dielectric. As in previous Intel interconnect stacks [2,3], a thick top metal layer is achieved with a plate-through-resist process and thick polymer dielectric in the Far Back End (FBE), which combines with M11 to simultaneously provide superior power distribution capability and excellent thermomechanical stress reduction incurred during flip chip packaging. The MIM capacitor is laminated within the passivation layer above the BE interconnect stack, between M11 and the thick top metal layer.

**Process Discussion**

The BE interconnect stack details, including pitch and metal thicknesses for each layer, are shown in Table 1. This represents the 14nm process used for high performance CPU products, low power SOC 14nm products will run a stack with more 52nm pitch layers for improved density. The BE layers (M0-M11) all utilize a dual damascene process, where M0-M8 employ ULK dielectrics [2] and M1-M8 are patterned with an SAV process flow [3]. ES thicknesses have been aggressively scaled down to 8nm for reduced capacitance. Mid-layer aspect ratios have also been increased to improve RC performance.

Aspect ratios of the lower layers (M0-M3) are optimized to below a factor of 2 to provide maximum

Table 1. Pitch, thickness and metal aspect ratio for the BE stack. (ULK: Ultra Low k; LK: Low k)

| Metal | Process | Dielectric | Pitch (nm) | Layer Thx (nm) | Metal Thx (nm) | AR |
|---|---|---|---|---|---|---|
| 0 | PD SAV | LK CDO | 56 | 70 | 40 | 1.4 |
| 1 | PD SAV | ULK CDO | 70 | 81 | 42 | 1.2 |
| 2 | PD SAV | ULK CDO | 52 | 73 | 40 | 1.5 |
| 3 | PD SAV | ULK CDO | 56 | 76 | 37 | 1.3 |
| 4 | SAV | Air Gap | 80 | 145 | 75 | 1.9 |
| 5 | SAV | ULK CDO | 100 | 210 | 110 | 2.2 |
| 6 | SAV | Air Gap | 160 | 310 | 180 | 2.3 |
| 7 | SAV | ULK CDO | 160 | 380 | 200 | 2.5 |
| 8 | SAV | ULK CDO | 160 | 400 | 200 | 2.5 |
| 9 | Via First | LK CDO | 252 | 540 | 260 | 2.1 |
| 10 | Via First | LK CDO | 252 | 675 | 375 | 3.0 |
| 11 | Via First | SiO2 | 1080 | 1770 | 1080 | 2.0 |
| 12 | Plate Up | polymer | 14000 | ~ | 6000 | 1.3 |

density with high yield. Mid- and upper-layers are optimized to a factor of 2 or greater for RC performance.

Each metal layer is targeted to achieve minimum resistance while still delivering sufficient current density for performance demands without sacrificing reliability requirements. Barriers have been thinned without loss of coverage continuity, and new electroplating chemistries have been introduced to provide good metal fill.

A dual patterning pitch division scheme is used for M0-M3 trench formation. This scheme involves first patterning a grating structure on which a spacer-based pitch reduction method is applied. Once the reduced pitch pattern is achieved, it is followed by a second patterning step to define orthogonal "plugs" that provide precision control of trench terminations and end-to-end spacing. The enhanced fidelity of this dual exposure technique offers new design rules that can be leveraged by designers to create increasingly dense designs.

M4 and above use single pass lithography for trench definition, where M4-M8 use an SAV-based process flow and M9-M11 use a via-first damascene flow.

The MIM is embedded above the top BE metal layer between M11 and the thick top metal layer. The MIM consists of a lamination of three, patterned TiN electrodes that are each separated by a Hf-based high k dielectric film (Fig.2). The thick top metal layer of the FBE is once again patterned with a cost-effective plate-through-resist process that provides for a highly controlled thick metallization pattern that can be used for precision power bussing designs with very low voltage droop. This layer is passivated with a SiN film before a spin-on, photo-definable dielectric and stress buffering film is deposited to prepare for the C4 bumping process.

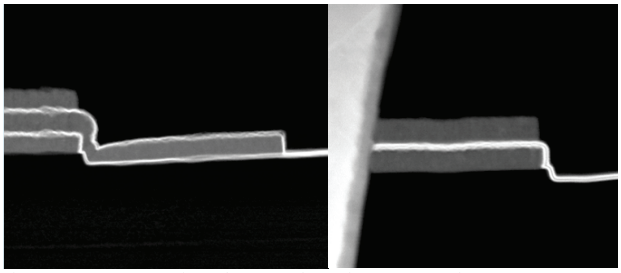

Figure 2. MIM capacitor shows 3 electodes connected to a center electrode tap (left). The right image shows the top and bottom electrode making connection to a top via.

## Air Gap

Intel has integrated an Air Gap dielectric into both M4 and M6 to provide critical performance benefit to the layers most heavily impacted by die footprint scaling. Fig. 3 shows both AG layers in cross section. This is the first ever multi-layer air gap process produced on a logic product in high volume.

The AG process utilizes a single loose pitch lithography masking layer to add or exclude the airgap on desired layout elements. This masking approach allows selective application of the dielectric reduction benefit of AG in tight pitched routing locations, while excluding it from certain layout locations such as around vias.

The AG is defined by lithographically masking regions where the AG is not desired. Carefully optimized etches and cleans are subsequently employed to remove the dielectric from between the metal trenches in these unmasked locations. Following dielectric removal, the Cu interconnects are capped with a thin (12nm at M4 and 16nm at M6) conformal SiC liner film. The subsequent layer dielectric deposition process is carefully optimized to pinch off above these gapped regions and additional processing delivers a planarized surface for the next patterning layer sequence.

AG cleans chemistries were specifically developed to avoid corrosion of the Cu and the barrier materials and avoid the risk of marginal reliability performance. All AG metals passed a battery of rigorous reliability stress testing

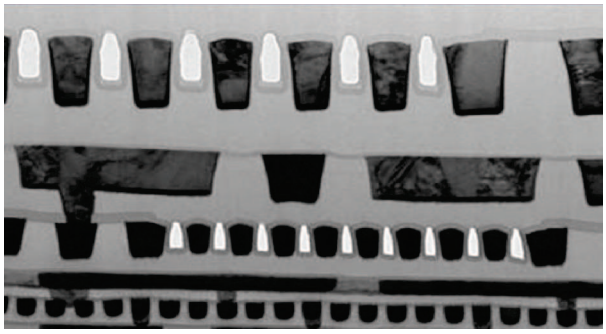

Figure 3. TEM showing Air gap at Metal 4 and Metal 6.

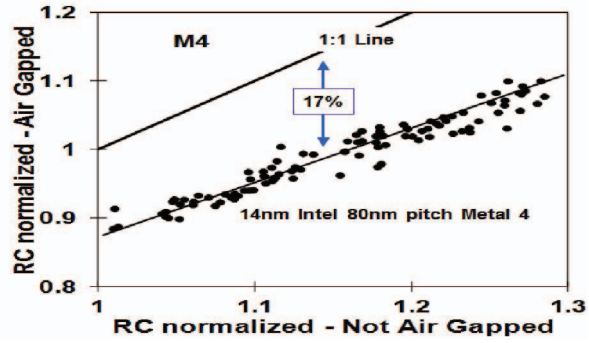


Figure 4. Air Gap vs non Air Gap interconnects demonstrates from 14% to 17% RC benefit.

to meet technology requirements. The Intel AG process demonstrates 14% to 17% RC improvement over non-AG interconnects, as measured on the same wafers as shown in Fig. 4.

## Results

The 14nm Intel process delivers up to 13% improved RC performance as compared to the 22nm matched metal pitch layers (Fig. 5). This benefit is delivered through the use of ULK films, increased aspect ratio trenches, reduced ES thickness and AG application. The dielectric films were optimized for performance and patterning. The etch and clean processes and chemistries were engineered to maintain the film dielectric constant while not degrading mechanical strength nor eroding trench and via profiles. As pitches continue to scale downward, the capability of the films to survive patterning with integrity has become the dominant concern for achieving high yield in a high volume manufacturing process.

The scaled ES films were optimized to simultaneously meet reliability and electrical performance goals. The minimum pitch (M2) R and C performance are shown in Fig. 6. This data is taken from 52nm pitch finger capacitors with 50% dense plates above and below to provide layer-to-layer and interlayer capacitance.

Despite incorporating more low modulus ULK dielectric layers than Intel's 22nm process, this process has

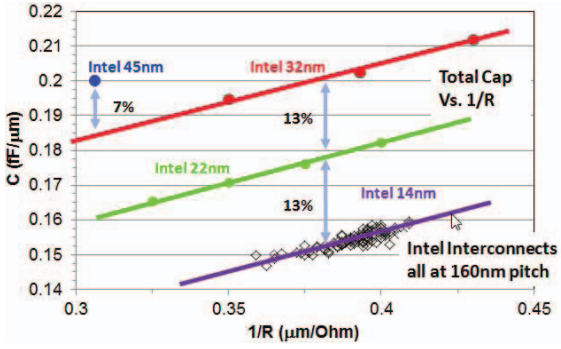


Fig 5. Historical Intel interconnect performance Trend compared at 160nm pitch. The 14nm process is air gap.

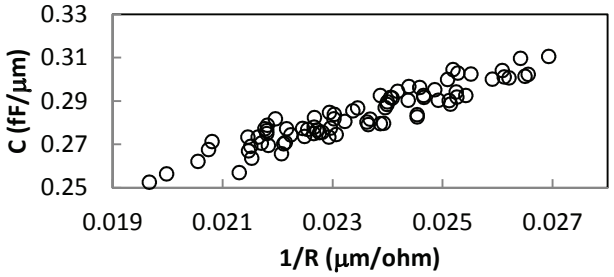


Figure 6: Capacitance vs inverse resistance of 52nm pitch M2.

demonstrated capable thermal mechanical performance by passing all standard environmental temperature and humidity, temp cycling, and thermal shock stress tests on thousands of assembled units. A portion of the thermo-mechanical stress reduction is attributed to stress attenuation by the new thick oxide M11 layer.

Intel's MIM capacitor has been enhanced to achieve twice the capacitance of Intel's 22nm technology MIM cap [1], achieving the highest reported capacitance density on a high volume logic product. The Tri-plate MIM provides >40 fF/µm$^2$ when used in a parallel configuration. This tri-layer MIM also provides the option of delivering higher breakdown voltage at reduced capacitance for decoupling higher voltage supplies.

## Summary

We have implemented a new, dense BE interconnect stack featuring 13 metal layers, including a stress relief layer, a tri-plate MIM, and multiple AG layers for improved performance. The interconnects deliver excellent performance and meet all reliability requirements. Microprocessors built on this technology are currently in high volume production at multiple Intel manufacturing facilities.

## Acknowledgements

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