## APPENDIX B

# SPICE DEVICE MODELS AND DESIGN SIMULATION EXAMPLES USING PSPICE AND MULTISIM

## Introduction

This appendix is concerned with the very important topic of using PSpice and Multisim to simulate the operation of electronic circuits. The need for and the role of computer simulation in circuit design was described in the preface. The appendix has three sections: Section B.1 presents a brief description of the models that SPICE uses to describe the operation of op amps, diodes, MOSFETs, and BJTs. Section B.2 presents design and simulation examples using PSpice. Finally, design and simulation examples utilizing Multisim are presented in Section B.3.

Besides the descriptions presented in this appendix, the reader will find the complete simulation files for each example on the CD accompanying the book.

## B.1 SPICE Device Models

To the designer, the value of simulation results is a direct function of the quality of the models used for the devices. The more faithfully the model represents the various characteristics of the device, the more accurately the simulation results will describe the operation of an actual fabricated circuit. In other words, to see the effect on circuit performance of various imperfections in device operation, these imperfections must be included in the device model used by the circuit simulator.

### B.1.1 The Op-Amp Model

In simulating circuits that use one or more op amps, it is useful to utilize a **macromodel** to represent each op amp. A macromodel is based on the observed terminal characteristics of the op amp rather than on the modeling of every transistor in the op-amp internal circuit. Macromodels can be developed from data-sheet specifications without knowledge of the details of the internal circuitry of the op amp.

**Linear Macromodel** The schematic capture of a linear macromodel for an internally compensated op amp with finite gain and bandwidth is shown in Fig. B.1. In this equivalent-circuit model, the gain constant $A_{0d}$ of the voltage-controlled voltage source $E_d$ corresponds

to the differential gain of the op amps at dc. Resistor $R_b$ and capacitor $C_b$ form a single-time-constant (STC) filter with a corner frequency

$$f_b = \frac{1}{2\pi R_b C_b} \tag{B.1}$$

The low-pass response of this filter is used to model the frequency response of the internally compensated op amp. The values of $R_b$ and $C_b$ used in the macromodel are chosen such that $f_b$ corresponds to the 3-dB frequency of the op amp being modeled. This is done by arbitrarily selecting a value for either $R_b$ or $C_b$ (the selected value does not need to be a practical one) and then using Eq. (B.1) to compute the other value. In Fig. B.1, the voltage-controlled voltage source $E_b$ with a gain constant of unity is used as a buffer to isolate the low-pass filter from any load at the op-amp output. Thus any op-amp loading will not affect the frequency response of the filter and hence that of the op amp.

The linear macromodel in Fig. B.1 can be further expanded to account for other op-amp nonidealities. For example, the equivalent-circuit model in Fig. B.2 can be used to model an internally compensated op amp while accounting for the following op-amp nonidealities:

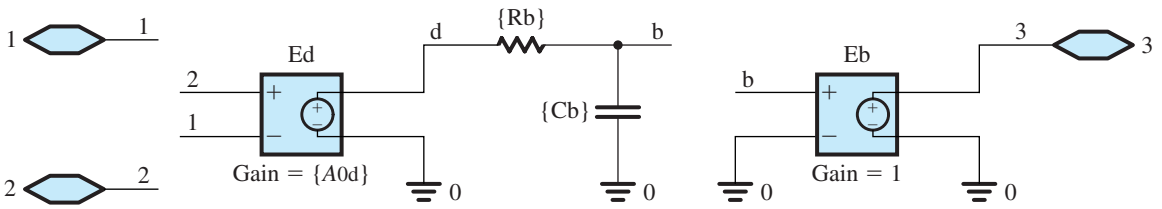



**Figure B.1** A linear macromodel used to model the finite gain and bandwidth of an internally compensated op amp.

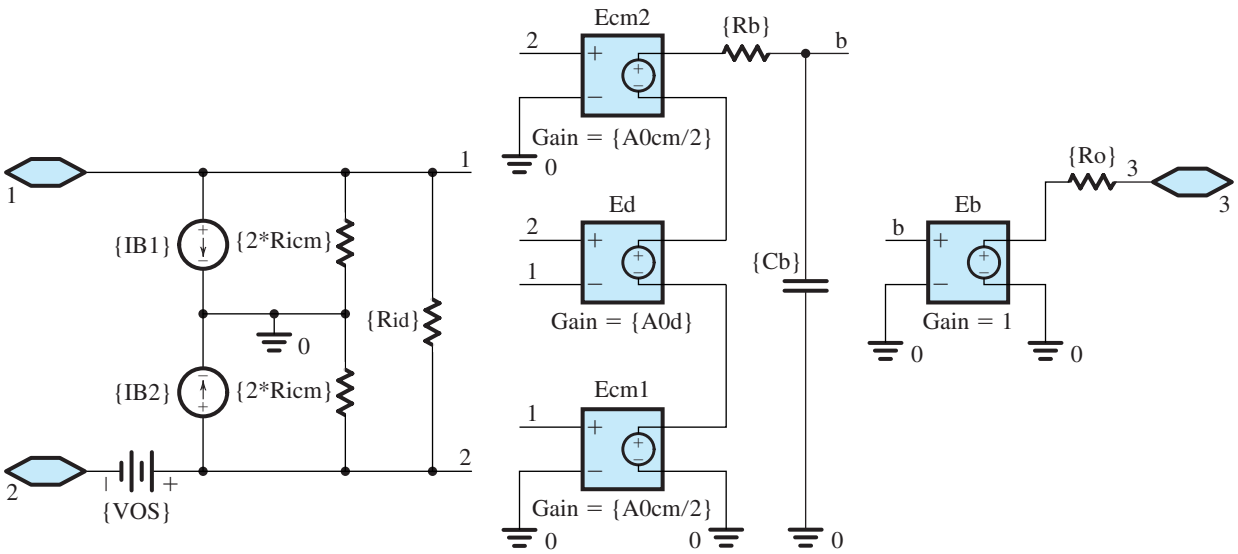



**Figure B.2** A comprehensive linear macromodel of an internally compensated op amp.

1. **Input Offset Voltage ($V_{OS}$).** The dc voltage source $V_{OS}$ models the op-amp input offset voltage.
2. **Input Bias Current ($I_B$) and Input Offset Current ($I_{OS}$).** The dc current sources $I_{B1}$ and $I_{B2}$ model the input bias current at each input terminal of the op amp, with

$$I_{B1} = I_B + \frac{I_{OS}}{2} \quad \text{and} \quad I_{B2} = I_B - \frac{I_{OS}}{2}$$

where $I_B$ and $I_{OS}$ are, respectively, the input bias current and the input offset current specified by the op-amp manufacturer.

3. **Common-Mode Input Resistance ($R_{icm}$).** If the two input terminals of an op amp are tied together and the input resistance (to ground) is measured, the result is the common-mode input resistance $R_{icm}$. In the macromodel of Fig. B.2, we have split $R_{icm}$ into two equal parts ($2R_{icm}$), each connected between one of the input terminals and ground.
4. **Differential-Input Resistance ($R_{id}$).** The resistance seen between the two input terminals of an op amp is the differential input resistance $R_{id}$.
5. **Differential Gain at DC ($A_{0d}$) and Common-Mode Rejection Ratio (CMRR).** The output voltage of an op amp at dc can be expressed as

$$V_3 = A_{0d}(V_2 - V_1) + \frac{A_{0cm}}{2}(V_1 + V_2) \tag{B.2}$$

where $A_{0d}$ and $A_{0cm}$ are, respectively, the differential and common-mode gains of the op amp at dc. For an op amp with a finite CMRR,

$$A_{0cm} = A_{0d}/\text{CMRR} \tag{B.3}$$

where CMRR is expressed in V/V (not in dB). In the macromodel of Fig. B.2, the voltage-controlled voltage sources $E_{cm1}$ and $E_{cm2}$ with gain constants of $A_{0cm}/2$ account for the finite CMRR while source $E_d$ models $A_{0d}$.

6. **Unity-Gain Frequency ($f_t$).** From Eq. (2.46), the 3-dB frequency $f_b$ and the unity-gain frequency (or gain-bandwidth product) $f_t$ of an internally compensated op amp with an STC frequency response are related by

$$f_b = \frac{f_t}{A_{0d}} \tag{B.4}$$

As in Fig. B.1, the finite op-amp bandwidth is accounted for in the macromodel of Fig. B.2 by setting the corner frequency of the filter formed by resistor $R_b$ and capacitor $C_b$ (Eq. B.1) to equal the 3-dB frequency of the op amp, $f_b$.

7. **Ouput Resistance ($R_o$).** The resistance seen at the output terminal of an op amp is the output resistance $R_o$.

The linear macromodels in Figs. B.1 and B.2 assume that the op-amp circuit is operating in its linear range and do not account for its nonideal performance when large signals are present at the output. Therefore, nonlinear effects, such as output saturation and slew rate, are not modeled.

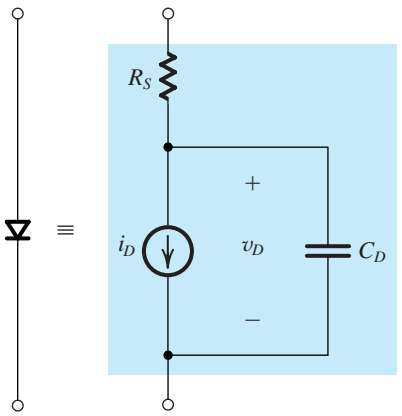
**Nonlinear Macromodel** The linear macromodel in Fig. B.2 can be expanded to account for the op-amp nonlinear performance. For example, the finite output voltage swing of the op amp can be modeled by placing limits on the output voltage of the voltage-controlled voltage

source $E_b$. In PSpice, this can be done using the ETABLE component in the analog-behavioral-modeling (ABM) library and setting the output voltage limits in the lookup table of this component. Further details on how to build nonlinear macromodels for the op amp can be found in the references on SPICE simulation. In general, robust macromodels that account for the nonlinear effects in an IC are provided by the op-amp manufacturers. Most simulators include such macromodels for some of the popular off-the-shelf ICs in their libraries. For example, PSpice and Multisim include models for the μA741, the LF411, and the LM324 op amps.

## B.1.2 The Diode Model

The large-signal SPICE model for the diode is shown in Fig. B.3. The static behavior is modeled by the exponential $i$–$v$ relationship. Here, for generality, a constant $n$ is included in the exponential. It is known as the **emission cofficient**, and its value ranges from 1 to 2. In our study of the diode in Chapter 3, we assumed $n = 1$. The dynamic behavior is represented by the nonlinear capacitor $C_D$, which is the sum of the diffusion capacitance $C_d$ and the junction capacitance $C_j$. The series resistance $R_S$ represents the total resistance of the $p$ and $n$ regions on both sides of the junction. The value of this parasitic resistance is ideally zero, but it is typically in the range of a few ohms for small-signal diodes. For small-signal analysis, SPICE uses the diode incremental resistance $r_d$ and the incremental values of $C_d$ and $C_j$.

Table B.1 provides a partial listing of the diode-model parameters used by SPICE, all of which should be familiar to the reader. But having a good device model solves only half of the modeling problem; the other half is to determine appropriate values for the model parameters. This is by no means an easy task. The values of the model parameters are determined using a combination of characterization of the device-fabrication process and specific measurements performed on the actual manufactured devices. Semiconductor manufacturers expend enormous effort and money to extract the values of the model parameters for their devices. For discrete diodes, the values of the SPICE model parameters can be determined from the diode data sheets, supplemented if needed by key measurements. Circuit simulators (such as PSpice) include in their libraries the model parameters of some of the popular off-the-shelf components. For instance, in Example PS4.1, we will use the commercially available D1N418 *pn*-junction diode whose SPICE model parameters are available in PSpice.




$$i_D = I_S\left(e^{v_D/nV_T} - 1\right)$$

$$C_D = C_d + C_j = \frac{\tau_T}{V_T} I_S e^{v_D/nV_T} + C_{j0}\Big/\left(1 - \frac{v_D}{V_0}\right)^m$$

**Figure B.3** The SPICE diode model.

**Table B.1** Parameters of the SPICE Diode Model (Partial Listing)

| SPICE Parameter | Book Symbol | Description | Units |
|---|---|---|---|
| IS | $I_S$ | Saturation current | A |
| N | $n$ | Emission coefficient | |
| RS | $R_S$ | Ohmic resistance | Ω |
| VJ | $V_0$ | Built-in potential | V |
| CJ0 | $C_{j0}$ | Zero-bias depletion (junction) capacitance | F |
| M | $m$ | Grading coefficient | |
| TT | $\tau_T$ | Transit time | s |
| BV | $V_{ZK}$ | Breakdown voltage | V |
| IBV | $I_{ZK}$ | Reverse current at $V_{ZK}$ | A |

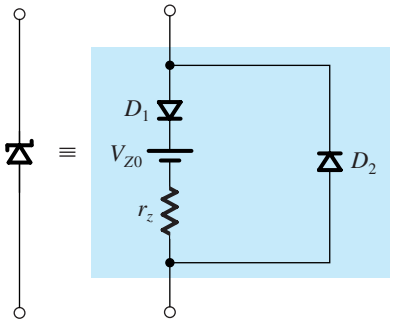



**Figure B.4** Equivalent-circuit model used to simulate the zener diode in SPICE. Diode $D_1$ is ideal and can be approximated in SPICE by using a very small value for $n$ (say $n = 0.01$).

## B.1.3 The Zener Diode Model

The diode model in Fig. B.3 does not adequately describe the operation of the diode in the breakdown region. Hence, it does not provide a satisfactory model for zener diodes. However, the equivalent-circuit model shown in Fig B.4 can be used to simulate a zener diode in SPICE. Here, diode $D_1$ is an ideal diode that can be approximated in SPICE by using a very small value for $n$ (say $n = 0.01$). Diode $D_2$ is a regular diode that models the forward-bias region of the zener (for most applications, the parameters of $D_2$ are of little consequence).

## B.1.4 MOSFET Models

To simulate the operation of a MOSFET circuit, a simulator requires a mathematical model to represent the characteristics of the MOSFET. The model we derived in Chapter 5 to represent the MOSFET is a simplified or first-order model. This model, called the **square-law model** because of the quadratic $i$–$v$ relationship in saturation, works well for transistors with relatively *long* channels. However, for devices with *short* channels, especially deep-submicron transistors, many physical effects that we neglected come into play, with the result that the derived first-order model no longer accurately represents the actual operation of the MOSFET (see Section 14.5).

The simple square-law model is useful for understanding the basic operation of the MOSFET as a circuit element and is indeed used to obtain approximate pencil-and-paper circuit designs. However, more elaborate models, which account for short-channel effects, are required to be able to predict the performance of integrated circuits with a certain degree of precision prior to fabrication. Such models have indeed been developed and continue to

be refined to more accurately represent the higher-order effects in short-channel transistors through a mix of physical relationships and empirical data. Examples include the Berkeley short-channel IGFET model (BSIM) and the EKV model, popular in Europe. Currently, semiconductor manufacturers rely on such sophisticated models to accurately represent the fabrication process. These manufacturers select a MOSFET model and then extract the values for the corresponding model parameters using both their knowledge of the details of the fabrication process and extensive measurements on a variety of fabricated MOSFETs. A great deal of effort is expended on extracting the model parameter values. Such effort pays off in fabricated circuits exhibiting performance very close to that predicted by simulation, thus reducing the need for costly redesign.

Although it is beyond the scope of this book to delve into the subject of MOSFET modeling and short-channel effects, it is important that the reader be aware of the limitations of the square-law model and of the availability of more accurate but, unfortunately, more complex MOSFET models. In fact, the power of computer simulation is more apparent when one has to use these complex device models in the analysis and design of integrated circuits.

SPICE-based simulators, like PSpice and Multisim, provide the user with a choice of MOSFET models. The corresponding SPICE model parameters (whose values are provided by the semiconductor manufacturer) include a parameter called LEVEL, which selects the MOSFET model to be used by the simulator. Although the value of this parameter is not always indicative of the accuracy, nor of the complexity of the corresponding MOSFET model, LEVEL = 1 corresponds to the simplest first-order model (called the Shichman-Hodges model), which is based on the square-law MOSFET equations presented in Chapter 5. For simplicity, we will use this model to illustrate the description of the MOSFET model parameters in SPICE and to simulate the example circuits in PSpice and Multisim. However, the reader is again reminded of the need to use a more sophisticated model than the level-1 model to accurately predict the circuit performance, especially for deep, submicron transistors.

**MOSFET Model Parameters** Table B.2 provides a listing of some of the MOSFET model parameters used in the level-1 model of SPICE. The reader should already be familiar with these parameters, except for a few, which are described next.

**MOSFET Diode Parameters** For the two reverse-biased diodes formed between each of the source and drain diffusion regions and the body (see Fig B.4), the saturation-current density is modeled in SPICE by the parameter JS. Furthermore, based on the parameters specified in Table B.2, SPICE will calculate the depletion-layer (junction) capacitances discussed in Section 8.2.1 as

$$C_{db} = \frac{\text{CJ}}{\left(1 + \dfrac{V_{DB}}{\text{PB}}\right)^{\text{MJ}}} \text{AD} + \frac{\text{CJSW}}{\left(1 + \dfrac{V_{DB}}{\text{PB}}\right)^{\text{MJSW}}} \text{PD} \tag{B.5}$$

$$C_{sb} = \frac{\text{CJ}}{\left(1 + \dfrac{V_{SB}}{\text{PB}}\right)^{\text{MJ}}} \text{AS} + \frac{\text{CJSW}}{\left(1 + \dfrac{V_{SB}}{\text{PB}}\right)^{\text{MJSW}}} \text{PS} \tag{B.6}$$

where AD and AS are the areas, while PD and PS are the perimeters of, respectively, the drain and source regions of the MOSFET. The first capacitance term in Eqs. (B.5) and (B.6) represents the depletion-layer (junction) capacitance over the bottom plate of the drain and source regions. The second capacitance term accounts for the depletion-layer capacitance along the sidewall (periphery) of these regions. Both terms are expressed using the formula

**Table B.2** Parameters of the SPICE Level-1 MOSFET Model (Partial Listing)

| SPICE Parameter | Book Symbol | Description | Units |
|---|---|---|---|
| | | **Basic Model Parameters** | |
| LEVEL | | MOSFET model selector | |
| TOX | $t_{ox}$ | Gate-oxide thickness | m |
| COX | $C_{ox}$ | Gate-oxide capacitance, per unit area | $F/m^2$ |
| UO | $\mu$ | Carrier mobility | $cm^2/V \cdot s$ |
| KP | $k'$ | Process transconductance parameter | $A/V^2$ |
| LAMBDA | $\lambda$ | Channel-length modulation coefficient | $V^{-1}$ |
| | | **Threshold Voltage Parameters** | |
| VTO | $V_{t0}$ | Zero-bias threshold voltage | V |
| GAMMA | $\gamma$ | Body-effect parameter | $V^{1/2}$ |
| NSUB | $N_A$, $N_D$ | Substrate doping | $cm^{-3}$ |
| PHI | $2\Phi_f$ | Surface inversion potential | V |
| | | **MOSFET Diode Parameters** | |
| JS | | Body-junction saturation-current density | $A/m^2$ |
| CJ | | Zero-bias body-junction capacitance, per unit area over the drain/source region | $F/m^2$ |
| MJ | | Grading coefficient, for area component | |
| CJSW | | Zero-bias body-junction capacitance, per unit length along F/m the sidewall (periphery) of the drain/source region | |
| MJSW | | Grading coefficient, for sidewall component | |
| PB | $V_0$ | Body-junction built-in potential | V |
| | | **MOSFET Dimension Parameters** | |
| LD | $L_{ov}$ | Lateral diffusion into the channel from the source/drain diffusion regions | m |
| WD | | Sideways diffusion into the channel from the body along the width | m |
| | | **MOS Gate-Capacitance Parameters** | |
| CGBO | | Gate-body overlap capacitance, per unit channel length | F/m |
| CGDO | $C_{ov}/W$ | Gate-drain overlap capacitance, per unit channel width | F/m |
| CGSO | $C_{ov}/W$ | Gate-source overlap capacitance, per unit channel width | F/m |

developed in Section 1.12.1 (Eq. 1.80). The values of AD, AS, PD, and PS must be specified by the user based on the dimensions of the device being used.

**MOSFET Dimension and Gate-Capacitance Parameters** In a fabricated MOSFET, the effective channel length $L_{\text{eff}}$ is shorter than the nominal (or drawn) channel length $L$ (as specified by the designer) because the source and drain diffusion regions extend slightly under the gate oxide during fabrication. Furthermore, the effective channel width $W_{\text{eff}}$ of the MOSFET is shorter than the nominal or drawn channel width $W$ because of the sideways diffusion into the channel from the body along the width. Based on the parameters specified in Table B.2,

$$L_{\text{eff}} = L - 2\text{LD} \tag{B.7}$$

$$W_{\text{eff}} = W - 2\text{WD} \tag{B.8}$$

In a manner analogous to using $L_{ov}$ to denote LD, we will use the symbol $W_{ov}$ to denote WD. Consequently, as indicated in Section 8.2.1, the gate-source capacitance $C_{gs}$ and the gate-drain capacitance $C_{gd}$ must be increased by an overlap component of, respectively,

$$C_{gs,ov} = W\,\text{CGSO} \tag{B.9}$$

and

$$C_{gd,ov} = W\,\text{CGDO} \tag{B.10}$$

Similarly, the gate-body capacitance $C_{gb}$ must be increased by an overlap component of

$$C_{gb,ov} = L\ \text{CGBO} \tag{B.11}$$

The reader may have observed that there is a built-in redundancy in specifying the MOSFET model parameters in SPICE. For example, the user may specify the value of KP for a MOSFET or, alternatively, specify TOX and UO and let SPICE compute KP as UO TOX. Similarly, GAMMA can be directly specified, or the physical parameters that enable SPICE to determine it can be specified (e.g., NSUB). In any case, *the user-specified values will always take precedence over (i.e., override) those values calculated by SPICE*. As another example, note that the user has the option of either directly specifying the overlap capacitances CGBO, CGDO, and CGSO or letting SPICE compute them as CGDO = CGSO = LD COX and CGBO = WD COX.

Table B.3 provides typical values for the level-1 MOSFET model parameters of a modern 0.18-μm CMOS technology and for older 0.5-μm and 5-μm CMOS technologies. The corresponding values for the minimum channel length $L_{\min}$, minimum channel width $W_{\min}$, and the maximum supply voltage $(V_{DD} + |V_{SS}|)_{\max}$ are as follows:

| Technology | $L_{\min}$ | $W_{\min}$ | $(V_{DD} + \|V_{SS}\|)_{\max}$ |
|---|---|---|---|
| 5-μm CMOS | 5 μm | 12.5 μm | 10 V |
| 0.5-μm CMOS | 0.5 μm | 1.25 μm | 3.3 V |
| 0.18-μm CMOS | 0.18 μm | 0.22 μm | 1.8 V |

When simulating a MOSFET circuit, the user needs to specify both the values of the model parameters and the dimensions of each MOSFET in the circuit being simulated. At least the channel length $L$ and width $W$ must be specified. The areas AD and AS and the perimeters PD and PS need to be specified for SPICE to model the body-junction capacitances (otherwise, zero capacitances would be assumed). The exact values of these geometry parameters depend on the actual layout of the device (Appendix A). However, to estimate these dimensions, we will assume that a metal contact is to be made to each of the source and drain regions of the MOSFET. For this purpose, typically, these diffusion regions must be extended *past* the end of the channel (i.e., in the $L$-direction in Fig. 5.1) by at least $2.75L_{\min}$. Thus, the minimum area and perimeter of a drain/source diffusion region with a contact are, respectively,

$$\text{AD} = \text{AS} = 2.75L_{\min}W \tag{B.12}$$

**Table B.3** Values of the Level-1 MOSFET Model Parameters for Two CMOS Technologies[1]

| | 5-μm CMOS Process | | 0.5-μm CMOS Process | | 0.18-μm CMOS Process | |
|---|---|---|---|---|---|---|
| | NMOS | PMOS | NMOS | PMOS | NMOS | PMOS |
| LEVEL | 1 | 1 | 1 | 1 | 1 | 1 |
| TOX | 8.50e-08 | 8.50e-08 | 9.50e-09 | 9.50e-09 | 4.08e-09 | 4.08e-09 |
| UO | 750 | 250 | 460 | 115 | 291 | 102 |
| LAMBDA | 0.01 | 0.03 | 0.1 | 0.2 | 0.08 | 0.11 |
| GAMMA | 1.4 | 0.65 | 0.5 | 0.45 | 0.3 | 0.3 |
| VTO | 1 | -1 | 0.7 | -0.8 | 0.5 | -0.45 |
| PHI | 0.7 | 0.65 | 0.8 | 0.75 | 0.84 | 0.8 |
| LD | 7.00e-07 | 6.00e-07 | 8.00e-08 | 9.00e-08 | 10e-9 | 10e.9 |
| JS | 1.00e-06 | 1.00e-06 | 1.00e-08 | 5.00e-09 | 8.38e-6 | 4.00e-07 |
| CJ | 4.00e-04 | 1.80e-04 | 5.70e-04 | 9.30e-04 | 1.60e-03 | 1.00e-03 |
| MJ | 0.5 | 0.5 | 0.5 | 0.5 | 0.5 | 0.45 |
| CJSW | 8.00e-10 | 6.00e-10 | 1.20e-10 | 1.70e-10 | 2.04e-10 | 2.04e-10 |
| MJSW | 0.5 | 0.5 | 0.4 | 0.35 | 0.2 | 0.29 |
| PB | 0.7 | 0.7 | 0.9 | 0.9 | 0.9 | 0.9 |
| CGBO | 2.00e-10 | 2.00e-10 | 3.80e-10 | 3.80e-10 | 3.80e-10 | 3.50e-10 |
| CGDO | 4.00e-10 | 4.00e-10 | 4.00e-10 | 3.50e-10 | 3.67e-10 | 3.43e-10 |
| CGSO | 4.00e-10 | 4.00e-10 | 4.00e-10 | 3.50e-10 | 3.67e-10 | 3.43e-10 |

[1]In PSpice, we have created MOSFET parts corresponding to the above models. Readers can find these parts in the SEDRA.olb library, which is available on the CD accompanying this book. The NMOS and PMOS parts for the 0.5-μm CMOS technology are labeled NMOS0P5_BODY and PMOS0P5_BODY, respectively. The NMOS and PMOS parts for the 5-μm CMOS technology are labelled NMOS5P0_BODY and PMOS5P0_BODY, respectively. Furthermore, parts NMOS5P0 and PMOS5P0 are created to correspond to, respectively, part NMOS0P5_BODY with its body connected to net 0 and part PMOS0P5_BODY with its body connected to net $V_{DD}$.

and

$$\text{PD} = \text{PS} = 2 \times 2.75 L_{\min} + W \tag{B.13}$$

Unless otherwise specified, we will use Eqs. (B.12) and (B.13) to estimate the dimensions of the drain/source regions in our examples.

Finally, we note that SPICE computes *the values for the parameters of the MOSFET small-signal model based on the dc operating point (bias point)*. These are then used by SPICE to perform the small-signal analysis (ac, or hand, analysis).

## B.1.5 The BJT Model

SPICE uses a general form of the BJT model that we discussed in Chapter 4 (Fig. 4.7). Known as the *transport* form of the **Ebers-Moll model**, it is shown in Fig. B.5. Here, the currents of the base–emitter diode ($D_{BE}$) and the base–collector diode ($D_{BC}$) are given, respectively, by

$$i_{BE} = \frac{I_S}{\beta_F}(e^{v_{BE}/n_F V_T} - 1) \tag{B.14}$$

and

$$i_{BC} = \frac{I_S}{\beta_R}(e^{v_{BC}/n_R V_T} - 1) \tag{B.15}$$

where $n_F$ and $n_R$ are the emission coefficients of the BEJ and BCJ, respectively. These coefficients are generalizations of the constant $n$ of the *pn*-junction diode (Fig. B.3). (We have so

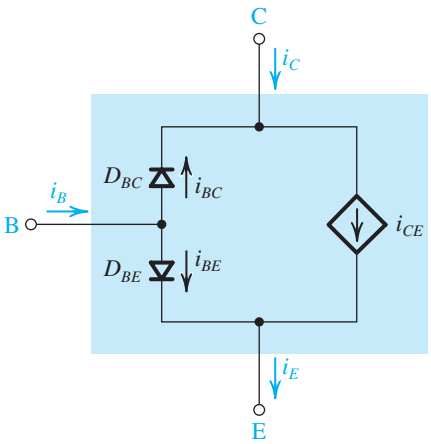



**Figure B.5** The transport form of the Ebers-Moll model for an *npn* BJT.

far assumed $n_F = n_R = 1$ ). The parameters $\beta_F$ and $\beta_R$ are, respectively, the forward and reverse $\beta$ of the BJT. The reverse $\beta$ is the current gain obtained when the collector and emitter are interchanged and is much smaller than the forward $\beta$. In fact, $\beta_R \ll 1$. The controlled current-source $i_{CE}$ in the transport model is defined as

$$i_{CE} = I_S(e^{v_{BE}/n_F V_T} - e^{v_{BC}/n_R V_T}) \tag{B.16}$$

Observe that $i_{CE}$ represents the current component of $i_C$ and $i_E$ that arises as a result of the minority carrier diffusion across the base, or **carrier transport** across the base (hence the name transport model).

The transport model can account for the Early effect in a forward-biased BJT by including the factor $(1 - v_{BC}/V_A)$ in the expression for the transport current $i_{CE}$ as follows:

$$i_{CE} = I_S(e^{v_{BE}/n_F V_T} - e^{v_{BC}/n_R V_T})\left(1 - \frac{v_{BC}}{V_A}\right) \tag{B.17}$$

Figure B.6 shows the model used in SPICE. Here, resistors $r_x$, $r_E$, and $r_C$ are added to represent the ohmic resistance of, respectively, the base, emitter, and collector regions. The dynamic operation of the BJT is modeled by two nonlinear capacitors, $C_{BC}$ and $C_{BE}$. Each of these capacitors generally includes a diffusion component (i.e., $C_{DC}$ and $C_{DE}$) and a depletion or junction component (i.e., $C_{JC}$ and $C_{JE}$) to account for the charge-storage effects within the BJT (as described in Section 8.2.2). Furthermore, the BJT model includes a depletion junction capacitance $C_{JS}$ to account for the collector–substrate junction in integrated-circuit BJTs, where a reverse-biased *pn*- junction is formed between the collector and the substrate (which is common to all components of the IC).

For small-signal (ac) analysis, the SPICE BJT model is equivalent to the hybrid-$\pi$ model of Fig. 8.8, but augmented with $r_E$, $r_C$, and (for IC BJTs) $C_{JS}$. Furthermore, the model includes a large resistance $r_\mu$ between the base and collector (in parallel with $C_\mu$) to account for the dependence of $i_B$ on $v_{CB}$. The resistance $r_\mu$ is very large, typically greater than $10\beta r_o$.

Although Fig. B.5 shows the SPICE model for the *npn* BJT, the corresponding model for the *pnp* BJT can be obtained by reversing the direction of the currents and the polarity of the diodes and terminal voltages.

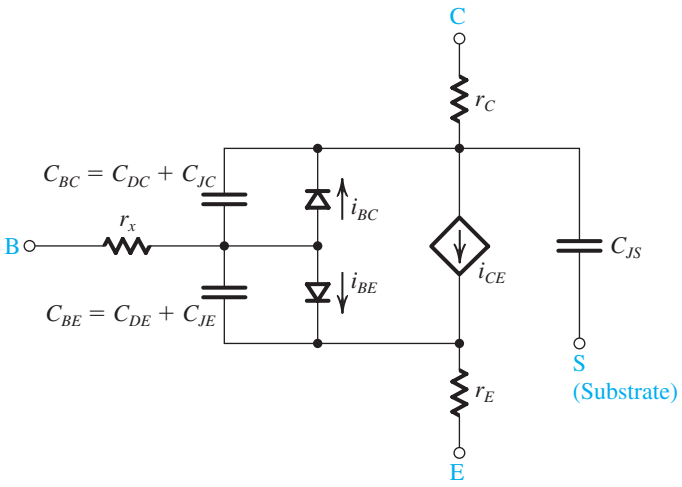



**Figure B.6** The SPICE large-signal model for an *npn* BJT.

**The SPICE Gummel-Poon Model of the BJT** The BJT model described above lacks a representation of some second-order effects present in actual devices. One of the most important such effects is the variation of the current gains, $\beta_F$ and $\beta_R$, with the current $i_C$. The Ebers-Moll model assumes $\beta_F$ and $\beta_R$ to be constant, thereby neglecting their current dependence (as depicted in Fig. 4.19). To account for this, and other second-order effects, SPICE uses a more accurate, yet more complex, BJT model called the Gummel-Poon model (named after H. K. Gummel and H. C. Poon, two pioneers in this field). This model is based on the relationship between the electrical terminal characteristics of a BJT and its base charge. It is beyond the scope of this book to delve into the model details. However, it is important for the reader to be aware of the existence of such a model.

In SPICE, the Gummel-Poon model automatically simplifies to the Ebers-Moll model when certain model parameters are not specified. Consequently, the BJT model to be used by SPICE need not be explicitly specified by the user (unlike the MOSFET case in which the model is specified by the LEVEL parameter). For discrete BJTs, the values of the SPICE model parameters can be determined from the data specified on the BJT data sheets, supplemented (if needed) by key measurements. For instance, in Example PS5.6.1, we will use the Q2N3904 *npn* BJT (from Fairchild Semiconductor) whose SPICE model is available in PSpice. In fact, the PSpice and Multisim library already includes the SPICE model parameters for many of the commercially available discrete BJTs. For IC BJTs, the values of the SPICE model parameters are determined by the IC manufacturer (using both measurements on the fabricated devices and knowledge of the details of the fabrication process) and are provided to the IC designers.

**The SPICE BJT Model Parameters** Table B.4 provides a listing of some of the BJT model parameters used in SPICE. The reader should be already familiar with these parameters. In the absence of a user-specified value for a particular parameter, SPICE uses a default value that typically results in the corresponding effect being ignored. For example, if no value is specified for the forward Early voltage (VAF), SPICE assumes that VAF = $\infty$ and does not account for the Early effect. Although ignoring VAF can be a serious issue in some circuits, the same is not true, for example, for the value of the reverse Early voltage (VAR).

**The BJT Model Parameters BF and BR in SPICE** Before leaving the SPICE model, a comment on $\beta$ is in order. SPICE interprets the user-specified model parameters BF and BR as the *ideal maximum* values of the forward and reverse dc current gains, respectively, versus the operating current. These parameters are not equal to the constant-current-independent parameters $\beta_F$ ($\beta_{dc}$) and $\beta_R$ used in the Ebers-Moll model for the forward and reverse dc current gains of the BJT. SPICE uses a current-dependent model for $\beta_F$ and $\beta_R$, and the user can specify other parameters (not shown in Table B.4) for this model. Only when such parameters are not specified, and the Early effect is neglected, will SPICE assume that $\beta_F$ and $\beta_R$ are constant and equal to BF and BR, respectively. Furthermore, SPICE computes values for both $\beta_{dc}$ and $\beta_{ac}$, the two parameters that we generally assume to be approximately equal. SPICE then uses $\beta_{ac}$ to perform small-signal (ac) analysis.

**Table B.4** Parameters of the SPICE BJT Model (Partial Listing)

| SPICE Parameter | Book Symbol | Description | Units |
|---|---|---|---|
| IS | $I_S$ | Saturation current | A |
| BF | $\beta_F$ | Ideal maximum forward current gain | |
| BR | $\beta_R$ | Ideal maximum reverse current gain | |
| NF | $n_F$ | Forward current emission coefficient | |
| NR | $n_R$ | Reverse current emission coefficient | |
| VAF | $V_A$ | Forward Early voltage | V |
| VAR | | Reverse Early voltage | V |
| RB | $r_x$ | Zero-bias base ohmic resistance | Ω |
| RC | $r_C$ | Collector ohmic resistance | Ω |
| RE | $r_E$ | Emitter ohmic resistance | Ω |
| TF | $\tau_F$ | Ideal forward transit time | s |
| TR | $\tau_R$ | Ideal reverse transit time | s |
| CJC | $C_{\mu 0}$ | Zero-bias base–collector depletion (junction) capacitance | F |
| MJC | $m_{BCJ}$ | Base–collector grading coefficient | |
| VJC | $V_{0c}$ | Base–collector built-in potential | V |
| CJE | $C_{je0}$ | Zero-bias base–emitter depletion (junction) capacitance | F |
| MJE | $m_{BEJ}$ | Base–emitter grading coefficient | |
| VJE | $V_{0e}$ | Base–emitter built-in potential | V |
| CJS | | Zero-bias collector–substrate depletion (junction) capacitance | F |
| MJS | | Collector–substrate grading coefficient | |
| VJS | | Collector–substrate built-in potential | V |

# B.2 PSpice Examples

## Example PS.2.1

### Performance of a Noninverting Amplifier

Consider an op amp with a differential input resistance of 2 MΩ, an input offset voltage of 1 mV, a dc gain of 100 dB, and an output resistance of 75 Ω. Assume the op amp is internally compensated and has an STC frequency response with a gain–bandwidth product of 1 MHz.

(a) Create a subcircuit model for this op amp in PSpice.
(b) Using this subcircuit, simulate the closed-loop noninverting amplifier in Fig. 2.12 with resistors $R_1$ = 1 kΩ and $R_2$ = 100 kΩ to find:
  (i) Its 3-dB bandwidth $f_{3dB}$.
  (ii) Its output offset voltage $V_{OSout}$.
  (iii) Its input resistance $R_{in}$.
  (iv) Its output resistance $R_{out}$.
(c) Simulate the step response of the closed-loop amplifier, and measure its rise time $t_r$. Verify that this time agrees with the 3-dB frequency measured above.

### Solution

To model the op amp in PSpice, we use the equivalent circuit in Fig. B.2, but with $R_{id}$ = 2 MΩ, $R_{icm} = \infty$ (open circuit), $I_{B1} = I_{B2} = 0$ (open circuit), $V_{OS}$ = 1 mV, $A_{0d} = 10^5$ V/V, $A_{0cm} = 0$ (short circuit), and $R_o$ = 75 Ω. Furthermore, we set $C_b$ = 1 μF and $R_b$ = 15.915 kΩ to achieve an $f_t$ = 1 MHz.

To measure the 3-dB frequency of the closed-loop amplifier, we apply a 1-V ac voltage at its input, perform an ac-analysis simulation in PSpice, and plot its output versus frequency. The output voltage, plotted in Fig. B.7, corresponds to the gain of the amplifier because we chose an input voltage of 1 V.

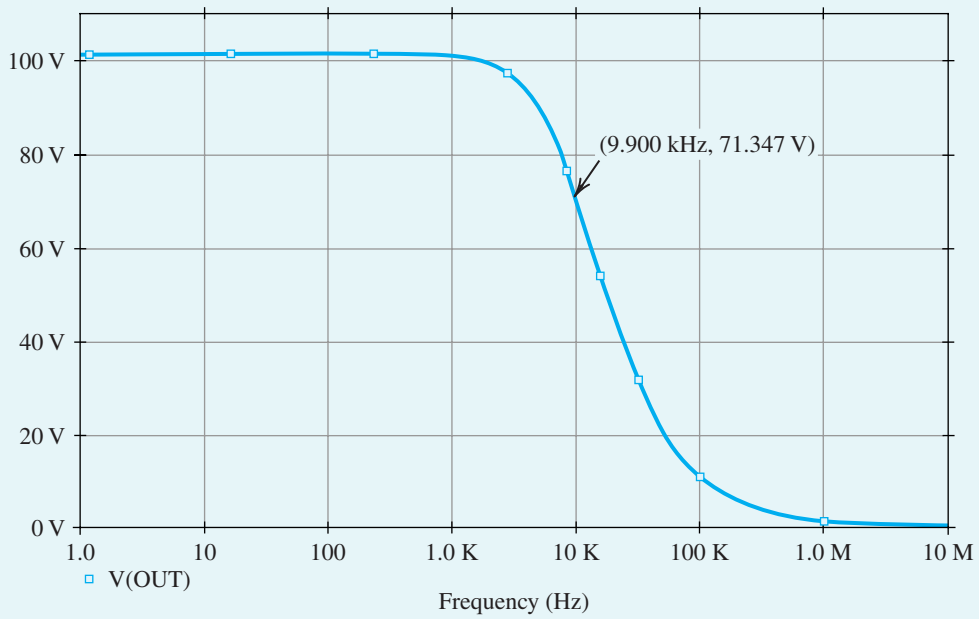



**Figure B.7** Frequency response of the closed-loop amplifier in Example PS.2.1.

**Example PS.2.1** *continued*

Thus, from Fig. B.7, the closed-loop amplifier has a dc gain of $G_0 = 100.9$ V/V, and the frequency at which its gain drops to $G_0/\sqrt{2} = 71.35$ V/V is $f_{3dB} = 9.9$ kHz, which agrees with Eq. (B.7).

The input resistance $R_{in}$ corresponds to the reciprocal of the current drawn out of the 1-V ac voltage source used in the above ac-analysis simulation at 0.1 Hz. (Theoretically, $R_{in}$ is the small-signal input resistance at dc. However, ac-analysis simulations must start at frequencies greater than zero, so we use 0.1 Hz to approximate the dc point.) Accordingly, $R_{in}$ is found to be 2 GΩ.

To measure $R_{out}$, we short-circuit the amplifier input to ground, inject a 1-A ac current at its output, and perform an ac-analysis simulation. $R_{out}$ corresponds to the amplifier output voltage at 0.1 Hz and is found to be 76 mΩ. Although an ac test voltage source could equally well have been used to measure the output resistance in this case, it is a good practice to attach a current source rather than a voltage source between the output and ground. This is because an ac current source appears as an open circuit when the simulator computes the dc bias point of the circuit while an ac voltage source appears as a short circuit, which can erroneously force the dc output voltage to zero. For similar reasons, an ac test voltage source should be attached in series with the biasing dc voltage source for measuring the input resistance of a voltage amplifier.

A careful look at $R_{in}$ and $R_{out}$ of the closed-loop amplifier reveals that their values have, respectively, increased and decreased by a factor of about 1000, relative to the corresponding resistances of the op amp. Such a large input resistance and small output resistance are indeed desirable characteristics for a voltage amplifier. This improvement in the small-signal resistances of the closed-loop amplifier is a direct consequence of applying negative feedback (through resistors $R_1$ and $R_2$) around the open-loop op amp. We will study negative feedback in Chapter 9, where we will also learn how the improvement factor (1000 in this case) corresponds to the ratio of the open-loop op-amp gain ($10^5$) to the closed-loop amplifier gain (100).

From Eqs. (2.55) and (2.53), the closed-loop amplifier has an STC low-pass response given by

$$\frac{V_o(s)}{V_i(s)} = \frac{G_0}{1 + \dfrac{s}{2\pi f_{3dB}}}$$

As described in Appendix E, the response of such an amplifier to an input step of height $V_{step}$ is given by

$$v_O(t) = V_{final}(1 - e^{-t/\tau}) \tag{B.18}$$

where $V_{final} = G_0 V_{step}$ is the final output-voltage value (i.e., the voltage value toward which the output is heading) and $\tau = 1/(2\pi f_{3dB})$ is the time constant of the amplifier. If we define $t_{10\%}$ and $t_{90\%}$ to be the time it takes for the output waveform to rise to, respectively, 10% and 90% of $V_{final}$, then from Eq. (B.18), $t_{10\%} \simeq 0.1\tau$ and $t_{90\%} \simeq 2.3\tau$. Therefore, the rise time $t_r$ of the amplifier can be expressed as

$$t_r = t_{90\%} - t_{10\%} = 2.2\tau = \frac{2.2}{2\pi f_{3dB}}$$

Therefore, if $f_{3dB} = 9.9$ kHz, then $t_r = 35.4$ μs. To simulate the step response of the closed-loop amplifier, we apply a step voltage at its input, using a piecewise-linear (PWL) source (with a very short rise time); then perform a transient-analysis simulation, and measure the voltage at the output versus time. In our simulation, we applied a 1-V step input, plotted the output waveform in Fig. B.8, and measured $t_r$ to be 35.3 μs.

The linear macromodels in Figs. B.1 and B.2 assume that the op-amp circuit is operating in its linear range; they do not account for its nonideal performance when large signals are present at the output. Therefore, nonlinear effects, such as output saturation and slew rate, are not modeled. This is why, in the step response of Fig. B.8, we could see an output voltage of 100 V when we applied a 1-V step input. However, IC op amps are not capable of producing such large output voltages. Hence, a designer must be very careful when using these models.

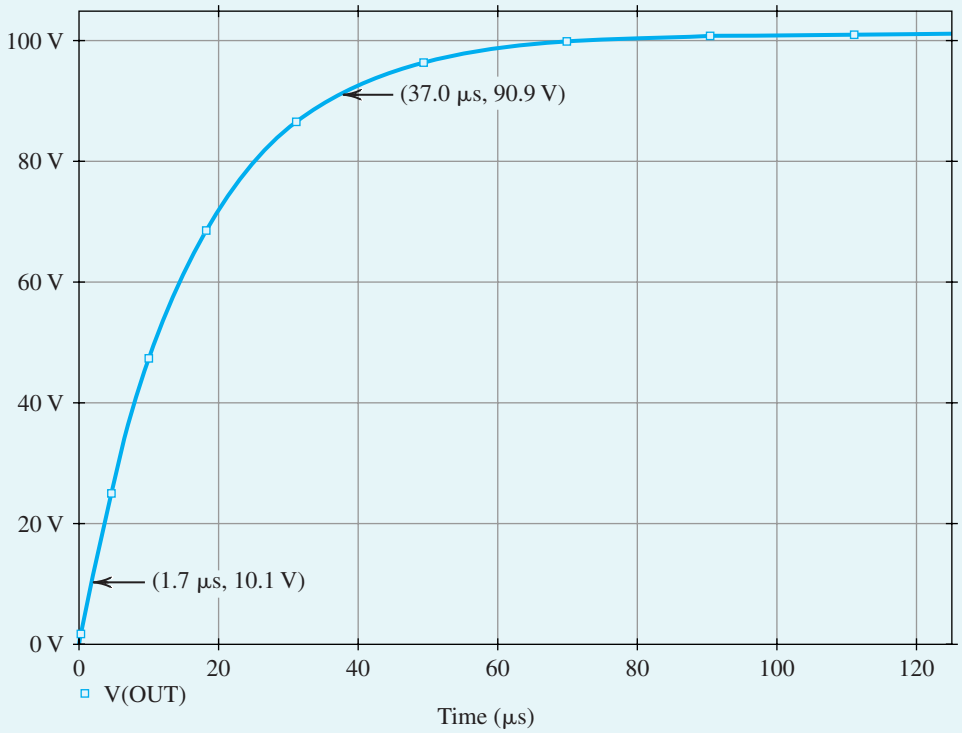



**Figure B.8** Step response of the closed-loop amplifier in Example PS.2.1.

It is important to point out that we also saw output voltages of 100 V or so in the ac analysis of Fig. B.7, where for convenience we applied a 1-V ac input to measure the gain of the closed-loop amplifier. So, would we see such large output voltages if the op-amp macromodel accounted for nonlinear effects (particularly output saturation)? The answer is yes, because in an ac analysis PSpice uses a linear model for nonlinear devices with the linear-model parameters evaluated at a bias point. Thus, we must keep in mind that the voltage magnitudes encountered in an ac analysis may not be realistic. In this case, the voltage and current ratios (e.g., the output-to-input voltage ratio as a measure of voltage gain) are of importance to the designer.

## Example PS.2.2

### Characteristics of the 741 OP Amp

Consider the µA741 op amp whose macromodel is available in PSpice. Use PSpice to plot the open-loop gain and hence determine $f_t$. Also, investigate the SR limitation and the output saturation of this op amp.

### Solution

Figure B.9 shows the schematic capture used to simulate the frequency response of the µA741 op amp.[1] The µA741 part has seven terminals. Terminals 7 and 4 are, respectively, the positive and negative dc power-supply

[1]The reader is reminded that the schematic capture diagram and the corresponding PSpice simulation files of all SPICE examples in this book can be found on the text's CD.

**Example PS.2.2** *continued*

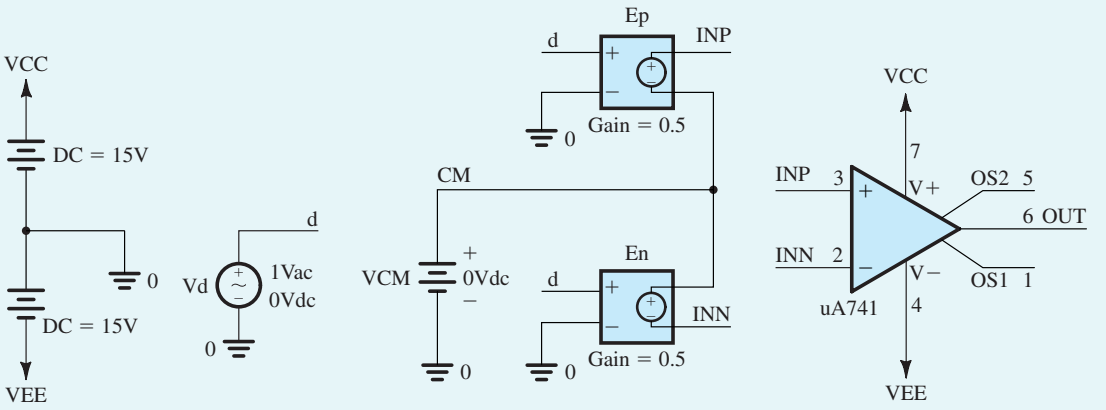



**Figure B.9** Simulating the frequency response of the μA741 op-amp in Example PS.2.2.

terminals of the op amp. The 741-type op amps are typically operated from ±15-V power supplies; therefore we connected the dc voltage sources $V_{CC} = +15$ V and $V_{EE} = -15$ V to terminals 7 and 4, respectively. Terminals 3 and 2 of the μA741 part correspond to the positive and negative input terminals, respectively, of the op amp. In general, as outlined in Section 2.1.3, the op-amp input signals are expressed as

$$v_{INP} = V_{CM} + \frac{V_d}{2}$$

$$v_{INN} = V_{CM} - \frac{V_d}{2}$$

where $v_{INP}$ and $v_{INN}$ are the signals at, respectively, the positive- and negative-input terminals of the op amp with $V_{CM}$ being the common-mode input signal (which sets the dc bias voltage at the op-amp input terminals) and $V_d$ being the differential input signal to be amplified. The dc voltage source $V_{CM}$ in Fig. B.9 is used to set the common-mode input voltage. Typically, $V_{CM}$ is set to the average of the dc power-supply voltages $V_{CC}$ and $V_{EE}$ to maximize the available input signal swing. Hence, we set $V_{CM} = 0$. The voltage source $V_d$ in Fig. B.9 is used to generate the differential input signal $V_d$. This signal is applied differentially to the op-amp input terminals using the voltage-controlled voltage sources $E_p$ and $E_n$, whose gain constants are set to 0.5.

Terminals 1 and 5 of part μA741 are the offset-nulling terminals of the op amp (as depicted in Fig. 2.36). However, a check of the PSpice netlist of this part (by selecting Edit → PSpice Model, in the Capture menus), reveals that these terminals are floating; therefore the offset-nulling characteristic of the op amp is not incorporated in this macromodel.

To measure $f_t$ of the op amp, we set the voltage of source $V_d$ to be 1-V ac, perform an ac-analysis simulation in PSpice, and plot the output voltage versus frequency as shown in Fig. B.10. Accordingly, the frequency at which the op-amp voltage gain drops to 0 dB is $f_t = 0.9$ MHz (which is close to the 1-MHz value reported in the data sheets for 741-type op amps).

To determine the slew rate of the μA741 op amp, we connect the op amp in a unity-gain configuration, as shown in Fig. B.11, apply a large pulse signal at the input with very short rise and fall times to

In these schematics (as shown in Fig. B.13), we use variable parameters to enter the values of the various circuit components. This allows one to investigate the effect of changing component values by simply changing the corresponding parameter values.

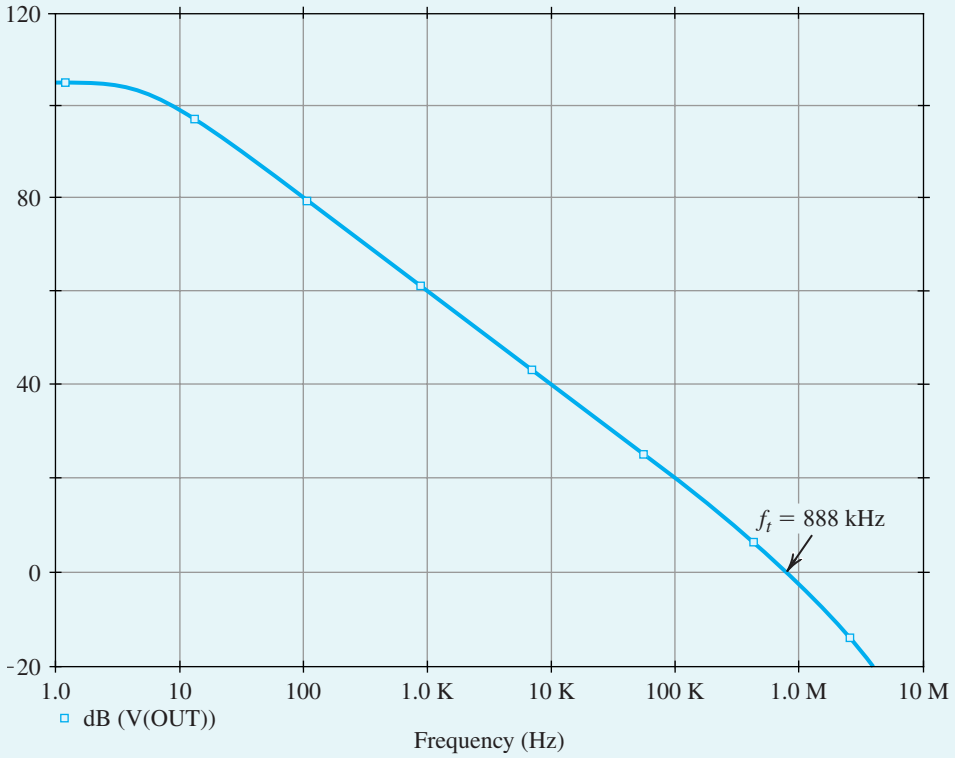



**Figure B.10** Frequency response of the μA741 op amp in Example PS.2.2.

cause slew-rate limiting at the output, perform a transient-analysis simulation in PSpice, and plot the output voltage as shown in Fg. B.12. The slope of the slew-rate limited output waveform corresponds to the slew-rate of the op amp and is found to be SR = 0.5 V/μs (which agrees with the value specified in the data sheets for 741-type opi amps).

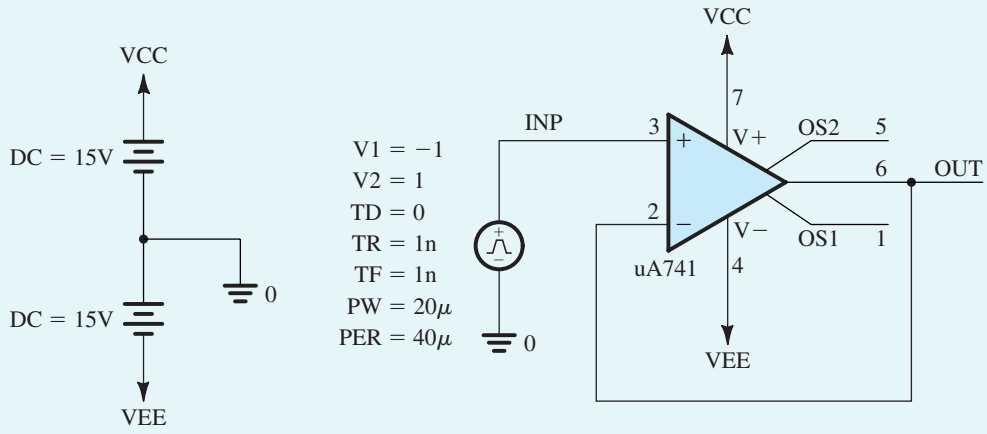



**Figure B.11** Circuit for determining the slew rate of the μA741 op amp in Example PS.5.2.2.

**Example PS.2.2** *continued*

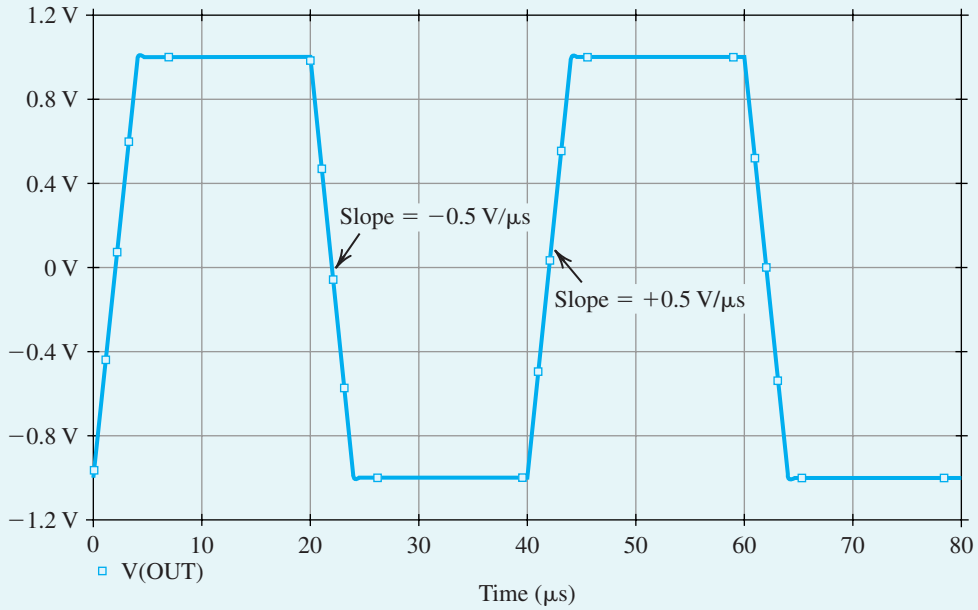



**Figure B.12** Square-wave response of the μA741 op amp connected in the unity-gain configuration shown in Fig. B.11.

To determine the maximum output voltage of the μA741 op amp, we set the dc voltage of the differential voltage source $V_d$ in Fig. B.9 to a large value, say +1 V, and perform a bias-point simulation in PSpice. The corresponding dc output voltage is the positive-output saturation voltage of the op amp. We repeat the simulation with the dc differential input voltage set to −1 V to find the negative-output saturation voltage. Accordingly, we find that the μA741 op amp has a maximum output voltage $V_{o\max} = 14.8$ V.

## Example PS.4.1

### Design of a DC Power Supply

In this example, we will design a dc power supply using the rectifier circuit whose capture schematic is shown in Fig. B.13. This circuit consists of a full-wave diode rectifier, a filter capacitor, and a zener voltage regulator. The only perhaps puzzling component is the $R_{\text{isolation}}$, the 100-MΩ resistor between the secondary winding of the transformer and ground. This resistor is included to provide dc continuity and thus "keep SPICE happy"; it has little effect on circuit operation.

Let it be required that the power supply (in Fig. B.13) provide a nominal dc voltage of 5 V and be able to supply a load current $I_{\text{load}}$ as large as 25 mA; that is, $R_{\text{load}}$ can be as low as 200 Ω. The power supply is fed from a 120-V (rms) 60-Hz ac line. Note that in the PSpice schematic (Fig. B.13), we use a sinusoidal voltage source with a 169-V peak amplitude to represent the 120-V rms supply (as 120-V rms = 169-V peak). Assume the availability of a 5.1-V zener diode having $r_z = 10$ Ω at $I_Z = 20$ mA (and thus $V_{Z0} = 4.9$ V), and that the required minimum current through the zener diode is $I_{Z\min} = 5$ mA.

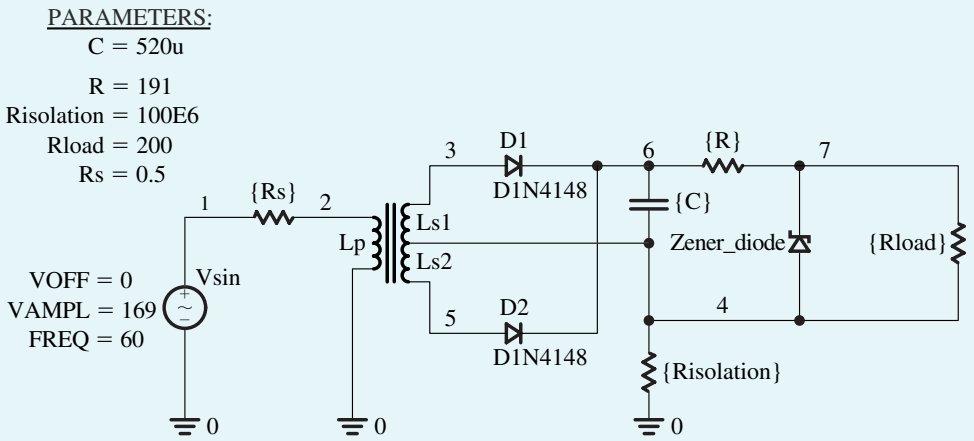



**Figure B.13** Schematic capture of the 5-V dc power supply in Example PS.4.1.

An approximate first-cut design can be obtained as follows: The 120-V (rms) supply is stepped down to provide 12-V (peak) sinusoids across each of the secondary windings using a 14:1 turns ratio for the center-tapped transformer. The choice of 12 V is a reasonable compromise between the need to allow for sufficient voltage (above the 5-V output) to operate the rectifier and the regulator, while keeping the PIV ratings of the diodes reasonably low. To determine a value for $R$, we can use the following expression:

$$R = \frac{V_{C\min} - V_{Z0} - r_z I_{Z\min}}{I_{Z\min} + I_{L\max}}$$

where an estimate for $V_{C\min}$, the minimum voltage across the capacitor, can be obtained by subtracting a diode drop (say, 0.8 V) from 12 V and allowing for a ripple voltage across the capacitor of, say, $V_r$ = 0.5 V. Thus, $V_{S\min} = 10.7$ V. Furthermore, we note that $I_{L\max} = 25$ mA and $I_{Z\min} = 5$ mA, and that $V_{Z0} = 4.9$ V and $r_z = 10\ \Omega$. The result is that $R = 191\ \Omega$.

Next, we determine $C$ using a restatement of Eq. (3.33) with $V_p/R$ replaced by the current through the 191-Ω resistor. This current can be estimated by noting that the voltage across $C$ varies from 10.7 V to 11.2 V, and thus has an average value of 10.95 V. Furthermore, the desired voltage across the zener is 5 V. The result is $C = 520\ \mu$F.

Now, with an approximate design in hand, we can proceed with the SPICE simulation. For the zener diode, we use the model of Fig. B.4, and assume (arbitrarily) that $D_1$ has $I_S = 100$ pA and $n = 0.01$ while $D_2$ has $I_S = 100$ pA and $n = 1.7$. For the rectifier diodes, we use the commercially available 1N4148 type[2] (with $I_S = 2.682$ nA, $n = 1.836$, $R_S = 0.5664\ \Omega$, $V_0 = 0.5$ V, $C_{j0} = 4$ pF, $m = 0.333$, $\tau_T = 11.54$ ns, $V_{ZK} = 100$ V, $I_{ZK} = 100\ \mu$A).

In PSpice, we perform a transient analysis and plot the waveforms of both the voltage $v_C$ across the smoothing capacitor $C$ and the voltage $v_O$ across the load resistor $R_{\text{load}}$. The simulation results for $R_{\text{load}} = 200\ \Omega$ ($I_{\text{load}} \simeq 25$ mA) are presented in Fig. B.14. Observe that $v_C$ has an average of 10.85 V and a ripple of ± 0.21 V. Thus, $V_r = 0.42$ V, which is close to the 0.5-V value that we would expect from the chosen value of $C$. The output voltage $v_O$ is very close to the required 5 V, with $v_O$ varying between 4.957 V and 4.977 V for a ripple of only 20 mV. The variations of $v_O$ with $R_{\text{load}}$ are illustrated in Fig. B.15 for $R_{\text{load}} = 500\ \Omega$, 250 Ω, 200 Ω, and 150 Ω. Accordingly, $v_O$ remains close to the nominal value of 5 V for $R_{\text{load}}$ as

[2]The 1N4148 model is included in the evaluation (EVAL) library of PSpice, which is available on the CD accompanying this book.

**Example PS.4.1** *continued*

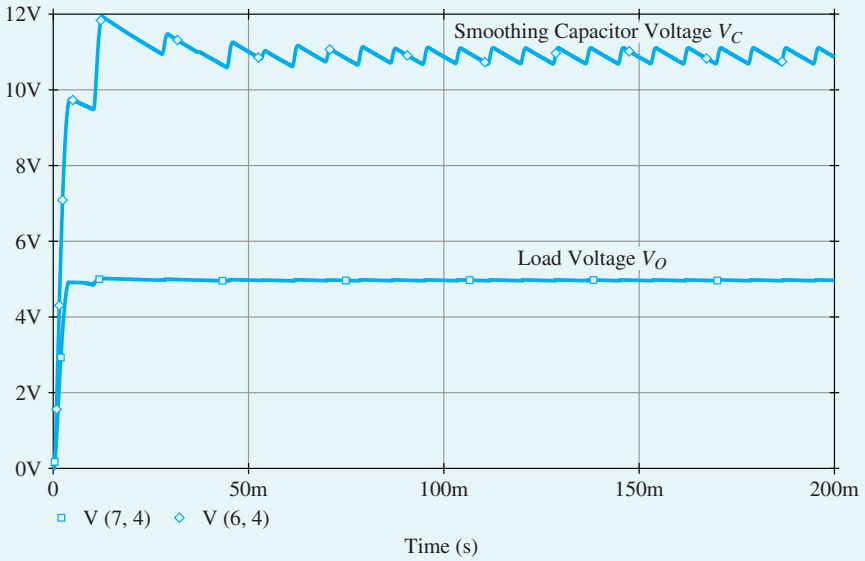



**Figure B.14** The voltage $v_C$ across the smoothing capacitor $C$ and the voltage $v_O$ across the load resistor $R_{load} = 200\ \Omega$ in the 5-V power supply of Example PS.4.1.

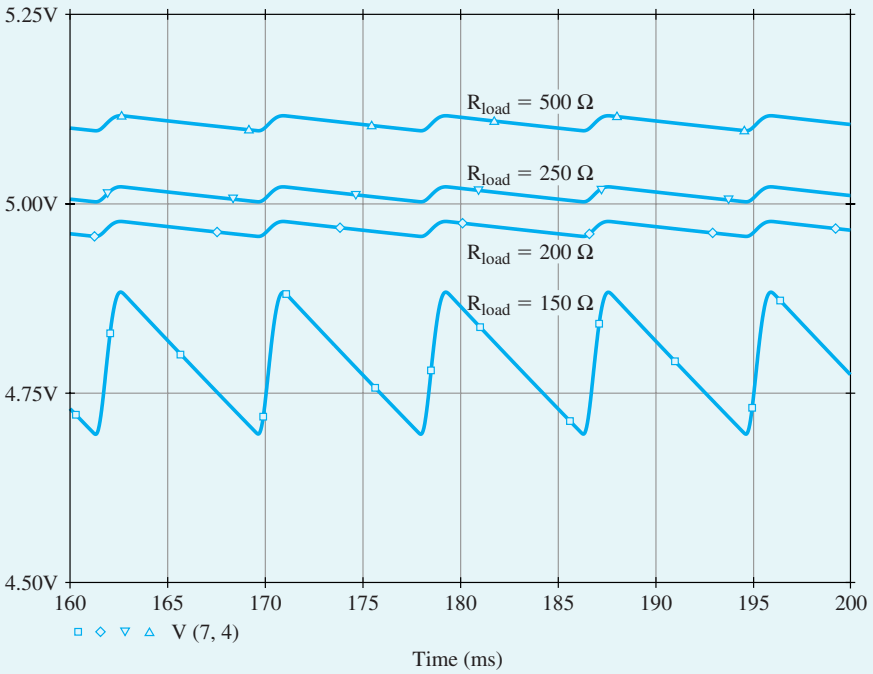



**Figure B.15** The output-voltage waveform from the 5-V power supply (in Example PS.4.1) for various load resistances: $R_{load} = 500\ \Omega$, 250 Ω, 200 Ω, and 150 Ω. The voltage regulation is lost at a load resistance of 150 Ω.

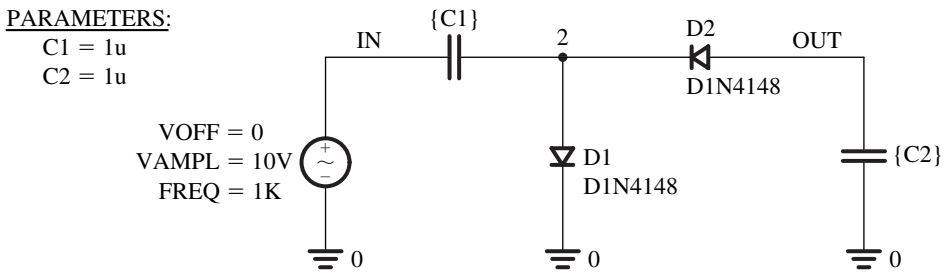
low as 200 Ω ($I_{load} \simeq 25$ mA). For $R_{load} = 150\ \Omega$ (which implies $I_{load} \simeq 33.3$ mA, greater than the maximum designed value), we see a significant drop in $v_O$ (to about 4.8 V), as well as a large increase in the ripple voltage at the output (to about 190 mV). This is because the zener regulator is no longer operational; the zener has in fact cut off.

We conclude that the design meets the specifications, and we can stop here. Alternatively, we may consider using further runs of PSpice to help with the task of fine-tuning the design. For instance, we could consider what happens if we use a lower value of $C$, and so on. We can also investigate other properties of the present design (e.g., the maximum current through each diode) and ascertain whether this maximum is within the rating specified for the diode.

## EXERCISE

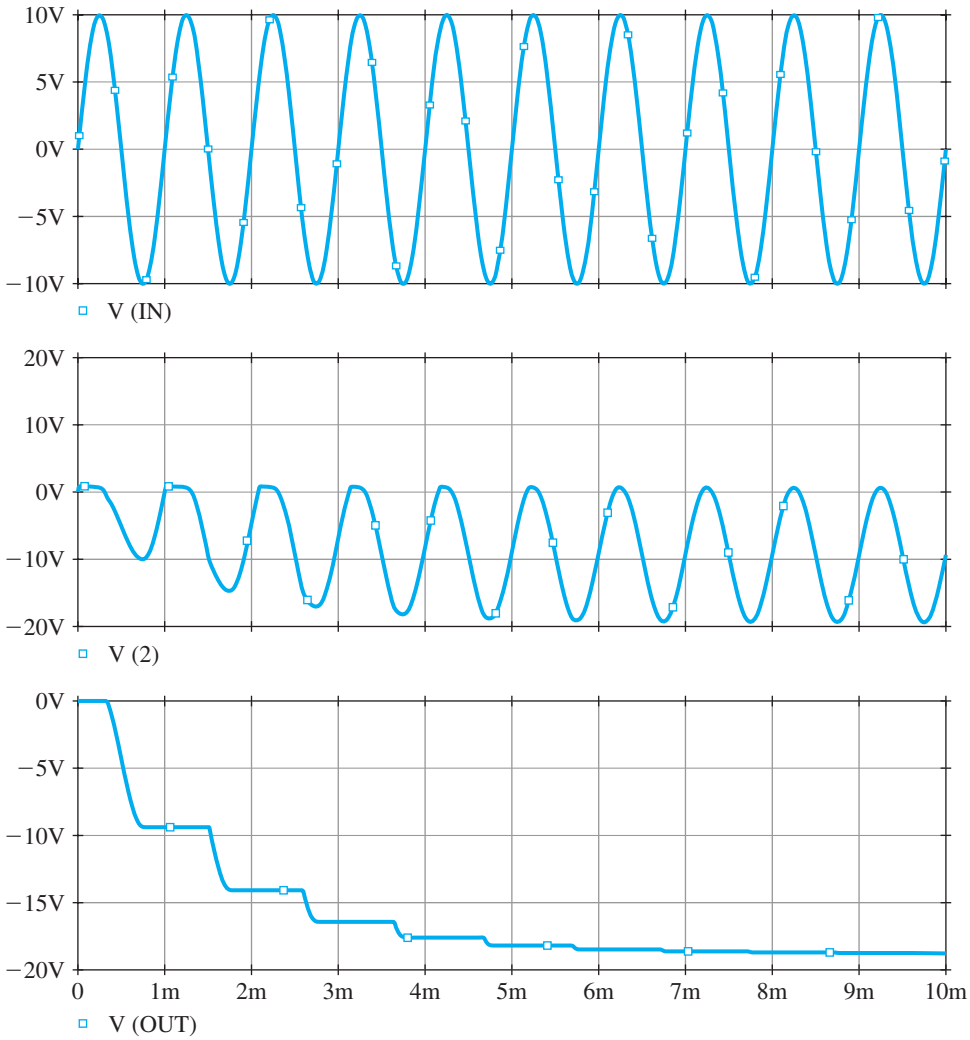
**B.1** Use PSpice to investigate the operation of the voltage doubler whose schematic capture is shown in Fig. B.16(a). Specifically, plot the transient behavior of the voltages $v_2$ and $v_{out}$ when the input is a sinusoid of 10-V peak and 1-kHz frequency. Assume that the diodes are of the 1N4148 type (with $I_S = 2.682$ nA, $n = 1.836$, $R_S = 0.5664\ \Omega$, $V_0 = 0.5$ V, $C_{j0} = 4$ pF, $m = 0.333$, $\tau_T = 11.54$ ns, $V_{ZK} = 100$ V, $I_{ZK} = 100\ \mu$A).

**Ans.** The voltage waveforms are shown in Fig. B.16(b).




(a)

**Figure B.16** (**a**) Schematic capture of the voltage-doubler circuit in Exercise B.1. **(b)** Various voltage waveforms in the voltage-doubler circuit. The top graph displays the input sine-wave voltage signal, the middle graph displays the voltage across diode $D_1$, and the bottom graph displays the voltage that appears at the output.




(b)

**Figure B.16** *continued*

## Example PS.5.1

### The CS Amplifier

In this example, we will use PSpice to analyze and verify the design of the CS amplifier whose capture schematic is shown in Fig. B.17.[3] Observe that the MOSFET has its source and body connected in order to cancel the body effect. We will assume a 0.5-μm CMOS technology for the MOSFET and use the SPICE level-1 model parameters listed in Table B.3. We will also assume a signal-source resistance $R_{sig}$ = 10 kΩ, a load resistance $R_L$ = 50 kΩ, and bypass and coupling capacitors of 10 μF. The targeted specifications for this CS amplifier are a midband gain $A_M$ = 10 V/V and a maximum power consumption $P$ = 1.5 mW. As should always be the case with computer simulation, we will begin with an approximate pencil-and-paper design. We will then use PSpice to fine-tune our design and to investigate the performance of the final design. In this way, maximum advantage and insight can be obtained from simulation.

With a 3.3-V power supply, the drain current of the MOSFET must be limited to $I_D = P/V_{DD} = 1.5\ \text{mW}/3.3\ \text{V} = 0.45\ \text{mA}$ to meet the power consumption specification. Choosing $V_{OV} = 0.3$ V (a typical value in low-voltage designs) and $V_{DS} = V_{DD}/3$ (to achieve a large signal swing at the output), the MOSFET can now be sized as

$$\frac{W}{L_{\text{eff}}} = \frac{I_D}{\frac{1}{2}k_n' V_{OV}^2(1+\lambda V_{DS})} = \frac{0.45\times 10^{-3}}{\frac{1}{2}(170.1\times 10^{-6})(0.3)^2[1+0.1(1.1)]} \simeq 53 \qquad \text{(B.19)}$$

where $k_n' = \mu_n C_{ox} = 170.1\ \mu\text{A/V}^2$ (from Table B.3). Here, $L_{\text{eff}}$ rather than $L$ is used to more accurately compute $I_D$. The effect of using $W_{\text{eff}}$ rather than $W$ is much less important because typically $W \gg W_{ov}$. Thus, choosing $L$ = 0.6 μm results in $L_{\text{eff}} = L - 2L_{ov} = 0.44$ μm and $W$ = 23.3 μm. Note that we chose $L$

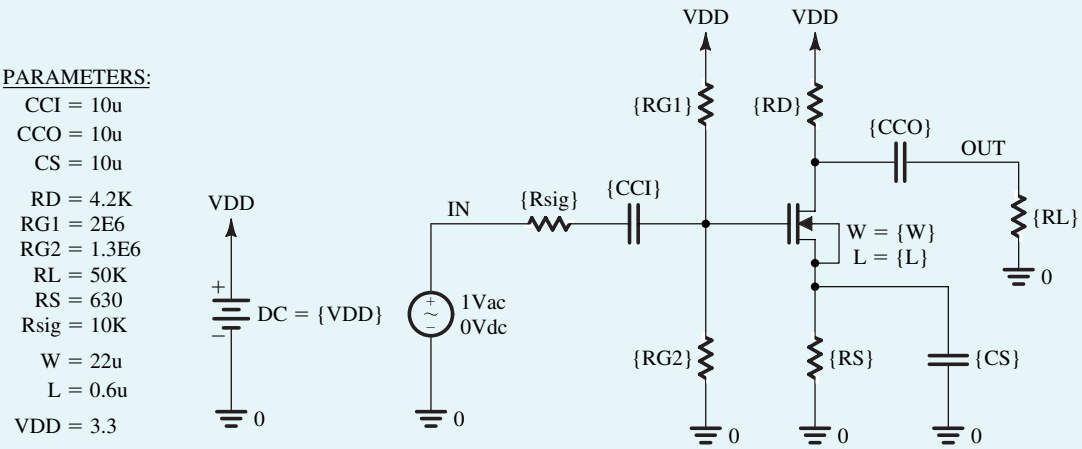



**Figure B.17** Schematic capture of the CS amplifier in Example PS.5.1.

[3]The reader is reminded that the schematic capture diagrams and the corresponding PSpice simulation files of all SPICE examples in this book can be found on the text's CD. In these schematics (as shown in Fig. B.17), we used variable parameters to enter the values of the various circuit components, including the dimensions of the MOSFET. This will allow the reader to investigate the effect of changing component values by simply changing the corresponding parameter values.

**Example PS.5.1** *continued*

slightly larger than $L_{min}$. This is a common practice in the design of analog ICs to minimize the effects of fabrication nonidealities on the actual value of $L$. As shown in the text, this is particularly important when the circuit performance depends on the matching between the dimensions of two or more MOSFETs (e.g., in the current-mirror circuits studied in Chapter 6).

Next, $R_D$ is calculated based on the desired voltage gain:

$$|A_v| = g_m(R_D \parallel R_L \parallel r_o) = 10 \text{ V/V} \Rightarrow R_D \simeq 4.2 \text{ k}\Omega \tag{B.20}$$

where $g_m = 3.0$ mA/V and $r_o = 22.2$ kΩ. Hence, the output bias voltage is $V_O = V_{DD} - I_D R_D = 1.39$ V. An $R_S = (V_O - V_{DD}/3)/I_D = 630\ \Omega$ is needed to bias the MOSFET at a $V_{DS} = V_{DD}/3$. Finally, resistors $R_{G1} = 2$ MΩ and $R_{G2} = 1.3$ MΩ are chosen to set the gate bias voltage at $V_G = I_D R_S + V_{OV} + V_{tn} \simeq 1.29$ V. Using large values for these gate resistors ensures that both their power consumption and the loading effect on the input signal source are negligible. Note that we neglected the body effect in the expression for $V_G$ to simplify our hand calculations.

We will now use PSpice to verify our design and investigate the performance of the CS amplifier. We begin by performing a bias-point simulation to verify that the MOSFET is properly biased in the saturation region and that the dc voltages and currents are within the desired specifications. Based on this simulation, we have decreased the value of $W$ to 22 μm to limit $I_D$ to about 0.45 mA. Next, to measure the midband gain $A_M$ and the 3-dB frequencies[4] $f_L$ and $f_H$, we apply a 1-V ac voltage at the input, perform an ac-analysis simulation, and plot the output-voltage magnitude (in dB) versus frequency as shown in Fig. B.18. This corresponds to the magnitude response of the CS amplifier because we chose a 1-V input signal.[5] Accordingly, the midband gain is $A_M = 9.55$ V/V and the 3-dB bandwidth is $BW = f_H - f_L \simeq 122.1$ MHz. Figure B.18 further shows that the gain begins to fall off at about 300 Hz but flattens out again at about 10 Hz. This flattening in the gain at low frequencies is due to a real transmission zero[6] introduced in the transfer function of the amplifier by $R_S$ together with $C_S$. This zero occurs at a frequency $f_Z = 1/(2\pi R_S C_S) = 25.3$ Hz, which is typically between the break frequencies $f_{P2}$ and $f_{P3}$ derived in Section 8.1.1. So, let us now verify this phenomenon by resimulating the CS amplifier with a $C_S = 0$ (i.e., removing $C_S$) in order to move $f_Z$ to infinity and remove its effect. The corresponding frequency response is plotted also in Fig. B.18. As expected, with $C_S = 0$, we do not observe any flattening in the low-frequency response of the amplifier. However, because the CS amplifier now includes a source resistor $R_S$, $A_M$ has dropped by a factor of 2.6. This factor is approximately equal to $(1 + g_m R_S)$, as expected from our study of the CS amplifier with a source-degeneration resistance in Section 5.6.4. Note that the bandwidth $BW$ has increased by approximately the same factor as the drop in gain $A_M$. As we will learn in Chapter 9 when we study negative feedback, the source-degeneration resistor $R_S$ provides negative feedback, which allows us to trade off gain for wider bandwidth.

To conclude this example, we will demonstrate the improved bias stability achieved when a source resistor $R_S$ is used (see the discussion in Section 5.7.2). Specifically, we will change (in the MOSFET level-1 model for part NMOS0P5) the value of the zero-bias threshold voltage parameter VT0 by ±15% and perform a bias-point simulation in PSpice. Table B.5 shows the corresponding variations in $I_D$ and $V_O$ for the case in which $R_S = 630\ \Omega$. For the case without source degeneration, we use an $R_S = 0$ in the

[4]No detailed knowledge of frequency-response calculations is required for this example; all that is needed is Section 5.8.6. Nevertheless, after the study of the frequency response of the CS amplifier in Sections 8.1 through 8.3, the reader will benefit by returning to this example and using PSpice to experiment further with the circuit.

[5]The reader should not be alarmed about the use of such a large signal amplitude. Recall that in a small-signal (ac) simulation, SPICE first finds the small-signal equivalent circuit at the bias point and then analyzes this linear circuit. Such ac analysis can, of course, be done with any ac signal amplitude. However, a 1-V ac input is convenient to use because the resulting ac output corresponds to the voltage gain of the circuit.

[6]Readers who have not yet studied poles and zeros can skip these few sentences.

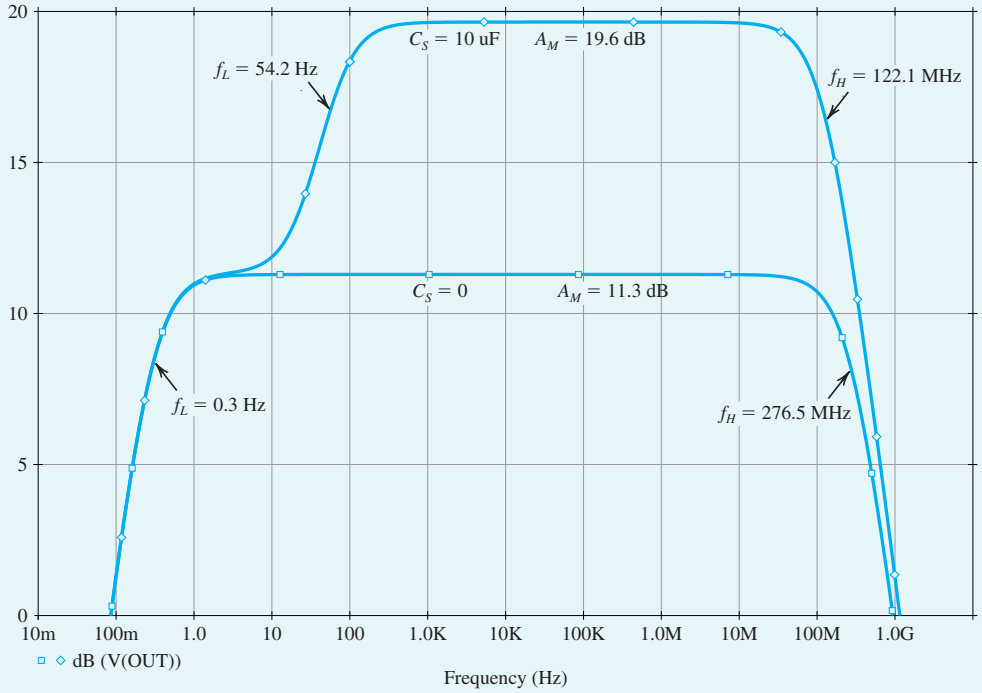



**Figure B.18** Frequency response of the CS amplifier in Example PS.5.1 with $C_S = 10$ μF and $C_S = 0$ (i.e., $C_S$ removed).

schematic of Fig. B.17. Furthermore, to obtain the same $I_D$ and $V_O$ in both cases (for the nominal threshold voltage $V_{t0} = 0.7$ V), we use an $R_{G2} = 0.88$ MΩ to reduce $V_G$ to around $V_{OV} + V_{tn} = 1$ V. The corresponding variations in the bias point are shown in Table B.5. Accordingly, we see that the source-degeneration resistor makes the bias point of the CS amplifier less sensitive to changes in the threshold voltage. In fact, the reader can show for the values displayed in Table B.5 that the variation in bias current $(\Delta I/I)$ is reduced by approximately the same factor, $(1 + g_m R_S)$. However, unless a large bypass capacitor $C_S$ is used, this reduced sensitivity comes at the expense of a reduction in the midband gain (as we observed in this example when we simulated the frequency response of the CS amplifier with a $C_S = 0$).

**Table B.5** Variations in the Bias Point with the MOSFET Threshold Voltage

| | $R_S = 630\Omega$ | | $R_S = 0$ | |
|---|---|---|---|---|
| $V_{tn0}$ | $I_D$ (mA) | $V_O$ (V) | $I_D$ (mA) | $V_O$ (V) |
| 0.60 | 0.56 | 0.962 | 0.71 | 0.33 |
| 0.7 | 0.46 | 1.39 | 0.45 | 1.40 |
| 0.81 | 0.36 | 1.81 | 0.21 | 2.40 |

## Example PS.6.1

### Dependence of the BJT $\beta$ on the Bias Current

In this example, we use PSpice to simulate the dependence of $\beta_{dc}$ on the collector bias current for the Q2N3904 discrete BJT (from Fairchild Semiconductor) whose model parameters are listed in Table B.6 and are available in PSpice.[7] As shown in the schematic capture[8] of Fig. B.19, the $V_{CE}$ of the BJT is fixed using a constant voltage source (in this example, $V_{CE} = 2$ V) and a dc current source $I_B$ is applied at the base. To illustrate the dependence of $\beta_{dc}$ on the collector current $I_C$, we perform a dc-analysis simulation in which the sweep variable is the current source $I_B$. The $\beta_{dc}$ of the BJT, which corresponds to the ratio of the collector current $I_C$ to the base current $I_B$, can then be plotted versus $I_C$ using Probe (the graphical interface of PSpice), as shown in Fig. B.20. We see that to operate at the maximum value of $\beta_{dc}$ (i.e., $\beta_{dc} = 163$), at $V_{CE} = 2$ V, the BJT must be biased at an $I_C = 10$ mA. Since increasing the bias current of a transistor increases the power dissipation, it is clear from Fig. B.20 that the choice of current $I_C$ is a trade-off between the current gain $\beta_{dc}$ and the power dissipation. Generally speaking, the optimum $I_C$ depends on the application and technology in hand. For example, for the Q2N3904 BJT operating at $V_{CE} = 2$ V, decreasing $I_C$ by a factor of 20 (from 10 mA to 0.5 mA) results in a drop in $\beta_{dc}$ of about 25% (from 163 to 123).

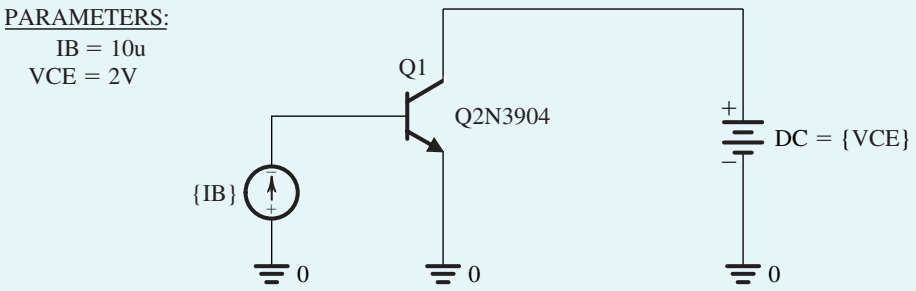



**Figure B.19** The PSpice test bench used to demonstrate the dependence of $\beta_{dc}$ on the collector bias current $I_C$ for the Q2N3904 discrete BJT (Example PS.6.1).

**Table B.6** Spice Model Parameters of the Q2N3904 Discrete BJT

| | | | | | | |
|---|---|---|---|---|---|---|
| IS=6.734F | XTI=3 | EG=1.11 | VAF=74.03 | BF=416.4 | NE=1.259 | ISE=6.734F |
| IKF=66.78M | XTB=1.5 | BR=.7371 | NC=2 | ISC=0 | IKR=0 | RC=1 |
| CJC=3.638P | MJC=.3085 | VJC=.75 | FC=.5 | CJE=4.493P | MJE=.2593 | VJE=.75 |
| TR=239.5N | TF=301.2P | ITF=.4 | VTF=4 | XTF=2 | RB=10 | |

[7] The Q2N3904 model is included in the evaluation (EVAL) library of PSpice which is available on the CD accompanying this book.

[8] The reader is reminded that the schematics diagrams and the corresponding PSpice simulation files of all SPICE examples in this book can be found on the text's CD. In these schematics (as shown in Fig. B.19), we use variable parameters to enter the values of the various circuit components. This allows one to investigate the effect of changing component values by simply changing the corresponding parameter values.

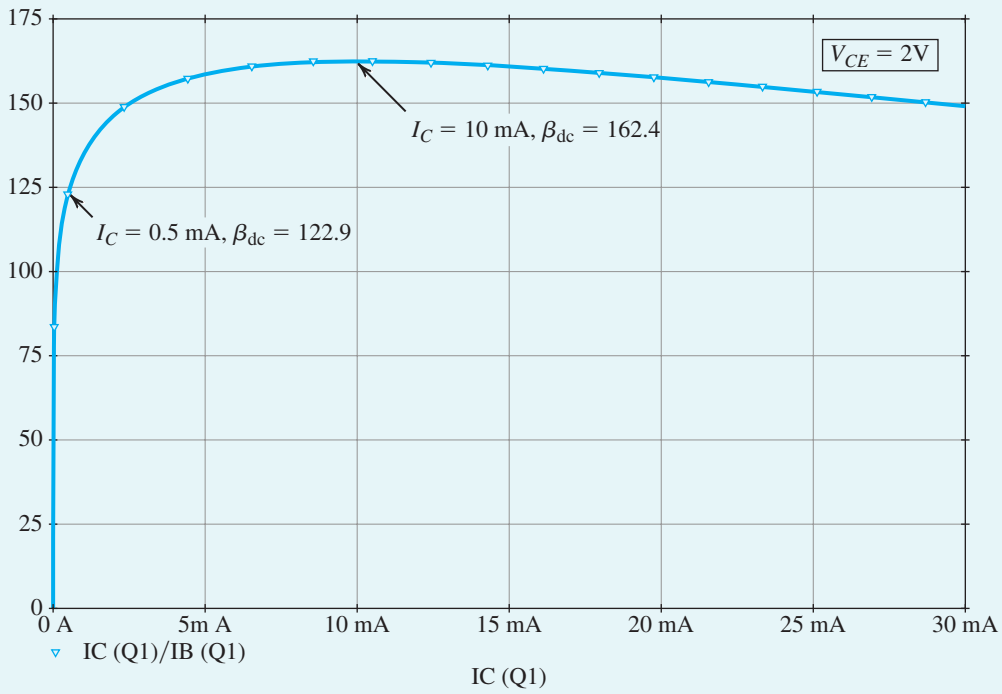



**Figure B.20** Dependence of $\beta_{dc}$ on $I_C$ (at $V_{CE} = 2$ V) in the Q2N3904 discrete BJT (Example PS.6.1).

## Example PS.6.2

### The CE Amplifier with Emitter Resistance

In this example, we use PSpice to analyze and verify the design of the CE amplifier. A schematic capture of the CE amplifier is shown in Fig. B.21. We will use part Q2N3904 for the BJT and a ±5-V power supply. We will also assume a signal source resistor $R_{sig} = 10$ kΩ, a load resistor $R_L = 10$ kΩ, and bypass and coupling capacitors of 10 μF. To enable us to investigate the effect of including a resistance in the signal path of the emitter, a resistor $R_{ce}$ is connected in series with the emitter bypass capacitor $C_E$. Note that the roles of $R_E$ and $R_{ce}$ are different. Resistor $R_E$ is the **dc emitter-degeneration resistor** because it appears in the dc path between the emitter and ground. It is therefore used to help stabilize the bias point for the amplifier. The equivalent resistance $R_e = R_E \| R_{ce}$ is the **small-signal emitter-degeneration resistance** because it appears in the ac (small-signal) path between the emitter and ground and helps stabilize the gain of the amplifier. In this example, we will investigate the effects of both $R_E$ and $R_e$ on the performance of the CE amplifier. However, as should always be the case with computer simulation, we will begin with an approximate pencil-and-paper design. In this way, maximum advantage and insight can be obtained from simulation.

Based on the plot of $\beta_{dc}$ versus $I_C$ in Fig. B.20, a collector bias current $I_C$ of 0.5 mA is selected for the BJT, resulting in $\beta_{dc} = 123$. This choice of $I_C$ is a reasonable compromise between power dissipation and current gain. Furthermore, a collector bias voltage $V_C$ of 0 V (i.e., at the mid–supply rail) is selected to

**Example PS.6.2** *continued*

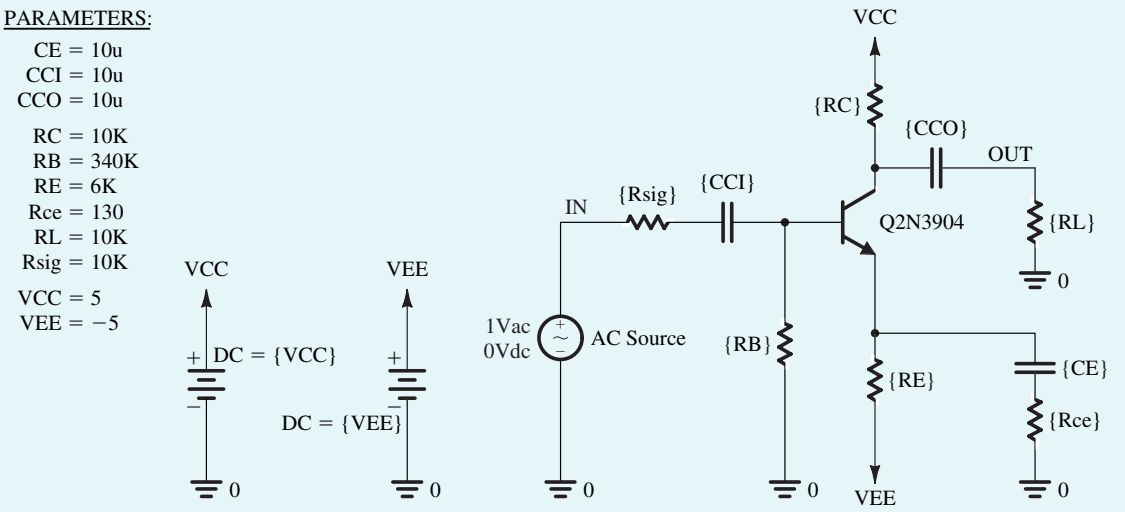



**Figure B.21** Schematic capture of the CE amplifier in Example PS.6.2.

achieve a high signal swing at the amplifier output. For $V_{CE} = 2$ V, the result is that $V_E = -2$ V requires bias resistors with values

$$R_C = \frac{V_{CC} - V_C}{I_C} = 10 \text{ k}\Omega$$

and

$$R_E = \frac{V_E - V_{EE}}{I_C} = 6 \text{ k}\Omega$$

Assuming $V_{BE} = 0.7$ V and using $\beta_{dc} = 123$, we can determine

$$R_B = -\frac{V_B}{I_B} = -\frac{0 - (V_{BE} + V_E)}{I_C/\beta_{dc}} = 320 \text{ k}\Omega$$

Next, the formulas of Section 4.8.3 can be used to determine the input resistance $R_{in}$ and the midband voltage gain $|A_M|$ of the CE amplifier:

$$R_{in} = R_B \| (\beta_{ac} + 1)(r_e + R_e) \tag{B.21}$$

$$|A_M| = \left| -\frac{R_{in}}{R_{sig} + R_{in}} \times \frac{R_C \| R_L}{r_e + R_e} \right| \tag{B.22}$$

For simplicity, we will assume $\beta_{ac} \simeq \beta_{dc} = 123$, resulting in

$$r_e = \left(\frac{\beta_{ac}}{\beta_{ac} + 1}\right)\left(\frac{V_T}{I_C}\right) = 49.6 \ \Omega$$

Thus, with no small-signal emitter degeneration (i.e., $R_{ce} = 0$), $R_{in} = 6.1$ kΩ and $|A_M| = 38.2$ V/V. Using Eq. (B.22) and assuming $R_B$ is large enough to have a negligible effect on $R_{in}$, it can be shown that

the emitter-degeneration resistor $R_e$ decreases the voltage gain $|A_M|$ by a factor of

$$\frac{1+\dfrac{R_e}{r_e}+\dfrac{R_{\text{sig}}}{r_\pi}}{1+\dfrac{R_{\text{sig}}}{r_\pi}}$$

Therefore, to limit the reduction in voltage gain to a factor of 2, we will select

$$R_e = r_e + \frac{R_{\text{sig}}}{\beta_{\text{ac}}+1} \tag{B.23}$$

Thus, $R_{ce} \simeq R_e = 130\ \Omega$. Substituting this value in Eqs. (B.21) and (B.22) shows that $R_{\text{in}}$ increases from 6.1 kΩ to 20.9 kΩ while $|A_M|$ drops from 38.2 V/V to 18.8 V/V.

We will now use PSpice to verify our design and investigate the performance of the CE amplifier. We begin by performing a bias-point simulation to verify that the BJT is properly biased in the active region and that the dc voltages and currents are within the desired specifications. Based on this simulation, we have increased the value of $R_B$ to 340 kΩ in order to limit $I_C$ to about 0.5 mA while using a standard 1% resistor value (Appendix H). Next, to measure the midband gain $A_M$ and the 3-dB frequencies[9] $f_L$ and $f_H$, we apply a 1-V ac voltage at the input, perform an ac-analysis simulation, and plot the output-voltage magnitude (in dB) versus frequency as shown in Fig. B.22. This corresponds to the magnitude response of the CE amplifier because we chose a 1-V input signal.[10] Accordingly, with no emitter degeneration, the midband gain is $|A_M| = 38.5$ V/V = 31.7 dB and the 3-dB bandwidth is $BW = f_H - f_L = 145.7$ kHz. Using an $R_{ce}$ of 130 Ω results in a drop in the midband gain $|A_M|$ by a factor of 2 (i.e., 6 dB). Interestingly, however, $BW$ has now increased by approximately the same factor as the drop in $|A_M|$. As we learned in Chapter 9 in our study of negative feedback, the emitter-degeneration resistor $R_{ce}$ provides negative feedback, which allows us to trade off gain for other desirable properties, such as a larger input resistance and a wider bandwidth.

To conclude this example, we will demonstrate the improved bias-point (or dc operating-point) stability achieved when an emitter resistor $R_E$ is used (see the discussion in Section 4.7.1). Specifically, we will increase/decrease the value of the parameter BF (i.e., the ideal maximum forward current gain) in the SPICE model for part Q2N3904 by a factor of 2 and perform a bias-point simulation. The corresponding change in BJT parameters ($\beta_{\text{dc}}$ and $\beta_{\text{ac}}$) and bias-point (including $I_C$ and $CE$) are presented in Table B.7 for the case of $R_E = 6$ kΩ. Note that $\beta_{\text{ac}}$ is not equal to $\beta_{\text{dc}}$ as we assumed, but is slightly larger. For the case without emitter degeneration, we will use $R_E = 0$ in the schematic of Fig. B.21. Furthermore, to maintain the same $I_C$ and $V_C$ in both cases at the values obtained for nominal BF, we use $R_B = 1.12$ MΩ to limit $I_C$ to approximately 0.5 mA. The corresponding variations in the BJT bias point are also shown in Table B.7. Accordingly, we see that emitter degeneration makes the bias point of the CE amplifier much less sensitive to changes in $\beta$. However, unless a large bypass capacitor $C_E$ is used, this reduced bias sensitivity comes at the expense of a reduction in the midband gain (as we observed in this example when we simulated the frequency response of the CE amplifier with an $R_e = 130\,\Omega$).

[9]No detailed knowledge of frequency-response calculations is required for this example; all that is needed is Section 4.8.6. Nevertheless, after the study of the frequency of the CE amplifier in Sections 8.1 through 8.3, the reader will benefit by returning to this example to experiment further with the circuit using PSpice.

[10]The reader should not be alarmed about the use of such a large signal amplitude. Recall that in a small-signal (ac) simulation, SPICE first finds the small-signal equivalent circuit at the dc bias point and then analyzes this linear circuit. Such ac analysis can, of course, be done with any ac signal amplitude. However, an I–V ac input is convenient to use because the resulting ac output corresponds to the voltage gain of the circuit.

Example PS.6.2 *continued*

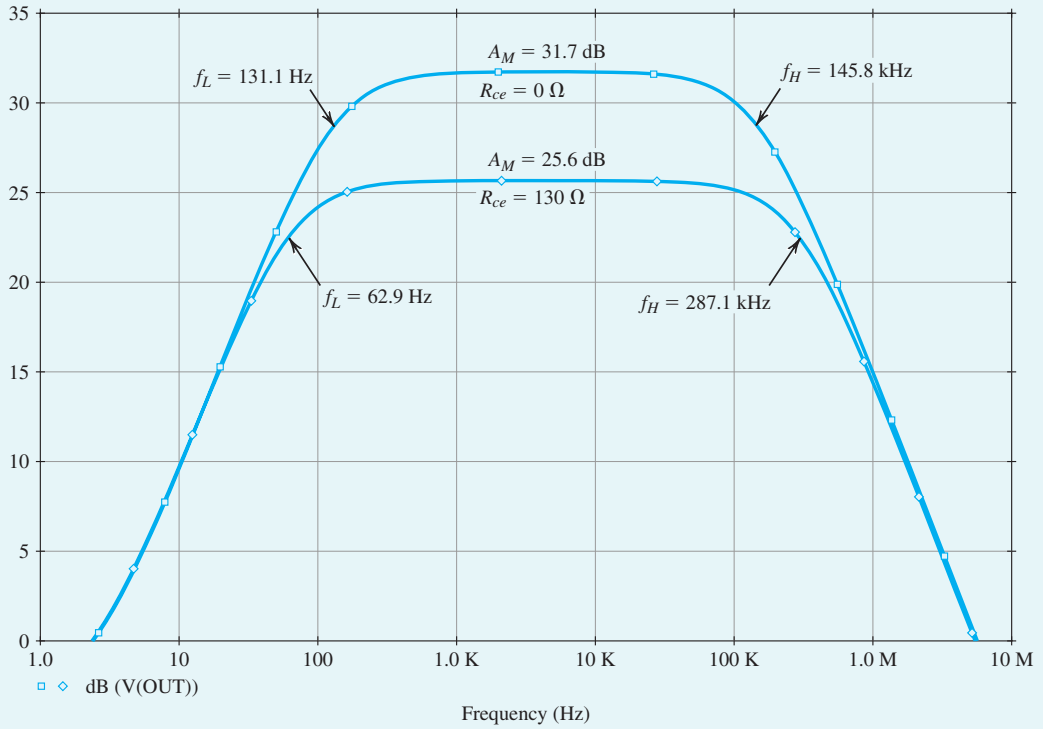



**Figure B.22** Frequency response of the CE amplifier in Example PS.6.2 with $R_{ce} = 0$ and $R_{ce} = 130\ \Omega$.

**Table B.7** Variations in the Bias Point of the CE Amplifier with the SPICE Model-Parameter BF of BJT

| | $R_E$ = 6 k | | | | $R_E$ = 0 | | | |
|---|---|---|---|---|---|---|---|---|
| BF (in SPICE) | $\beta_{ac}$ | $\beta_{dc}$ | $I_c$ (mA) | $V_c$ (V) | $\beta_{ac}$ | $\beta_{dc}$ | $I_c$ (mA) | $V_c$ (V) |
| 208 | 106 | 94.9 | 0.452 | 0.484 | 109 | 96.9 | 0.377 | 1.227 |
| 416.4 (nominal value) | 143 | 123 | 0.494 | 0.062 | 148 | 127 | 0.494 | 0.060 |
| 832 | 173 | 144 | 0.518 | −0.183 | 181 | 151 | 0.588 | −0.878 |

## Example PS.7.1

### The CMOS CS Amplifier

In this example, we will use PSpice to compute the dc transfer characteristic of the CS amplifier whose capture schematic is shown in Fig. B.23. We will assume a 5-μm CMOS technology for the MOSFETs and use parts NMOS5P0 and PMOS5P0 whose SPICE level-1 parameters are listed in Table B.3. To specify the dimensions of the MOSFETs in PSpice, we will use the multiplicative factor $m$ together with the channel length $L$ and the channel width $W$. The MOSFET parameter $m$, whose default value is 1, is used in SPICE to specify the number of MOSFETs connected in parallel. As depicted in Fig. B.24, a wide transistor with channel length $L$ and channel width $m \times W$ can be implemented using $m$ narrower transistors in parallel, each having a channel length $L$ and a channel width $W$. Thus, neglecting the channel-length modulation effect, the drain current of a MOSFET operating in the saturation region can be expressed as

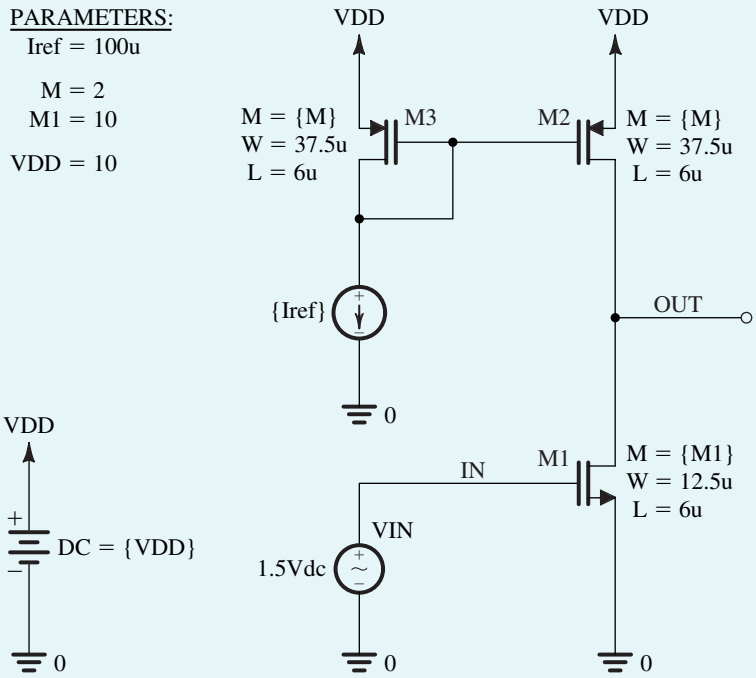
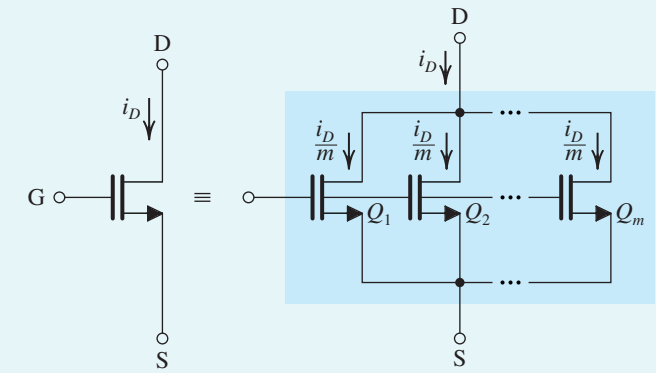



**Figure B.23** Schematic capture of the CS amplifier in Example PS.7.1.




Aspect ratio $= \frac{mW}{L}$ Aspect ratio of each MOSFET $= \frac{W}{L}$

**Figure B.24** Transistor equivalency.

$$I_D = \frac{1}{2}\mu C_{ox} m \frac{W}{L_{\text{eff}}} V_{OV}^2 \tag{B.24}$$

where $L_{\text{eff}}$ rather than $L$ is used to more accurately estimate the drain current.

The CS amplifier in Fig. B.23 is designed for a bias current of 100 μA assuming a reference current $I_{\text{ref}} = 100$ μA and $V_{DD} = 10$ V. The current mirror transistors $M_2$ and $M_3$ are sized for $V_{OV2} = V_{OV3} = 1$ V,

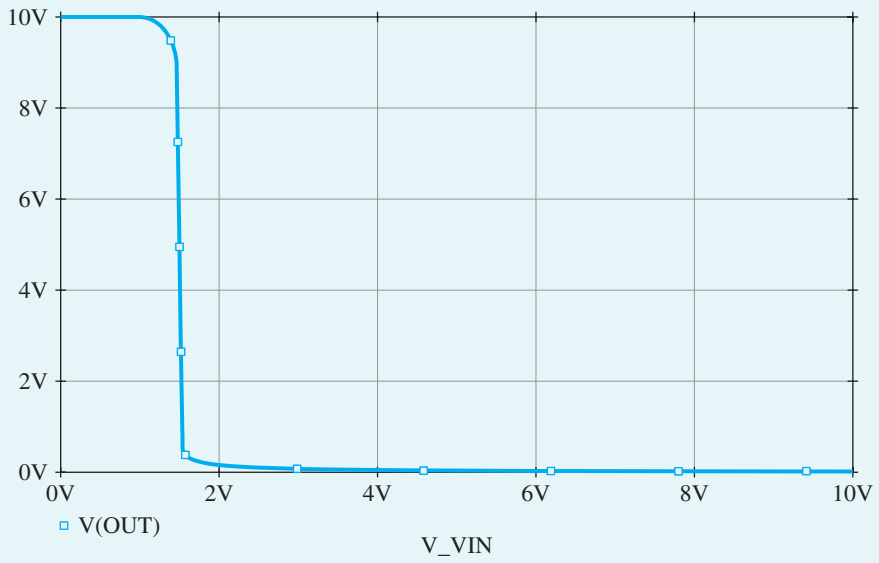
**Example PS.7.1** *continued*

while the input transistor $M_1$ is sized for $V_{OV1} = 0.5$ V. Note that a smaller overdrive voltage is selected for $M_1$ to achieve a larger voltage gain $G_v$ for the CS amplifier, since

$$G_v = -g_{m1}R'_L = -g_{m1}(r_{o1} \parallel r_{o2}) = -\frac{2}{V_{OV1}}\left(\frac{V_{An}V_{Ap}}{V_{An} + V_{Ap}}\right) \tag{B.25}$$

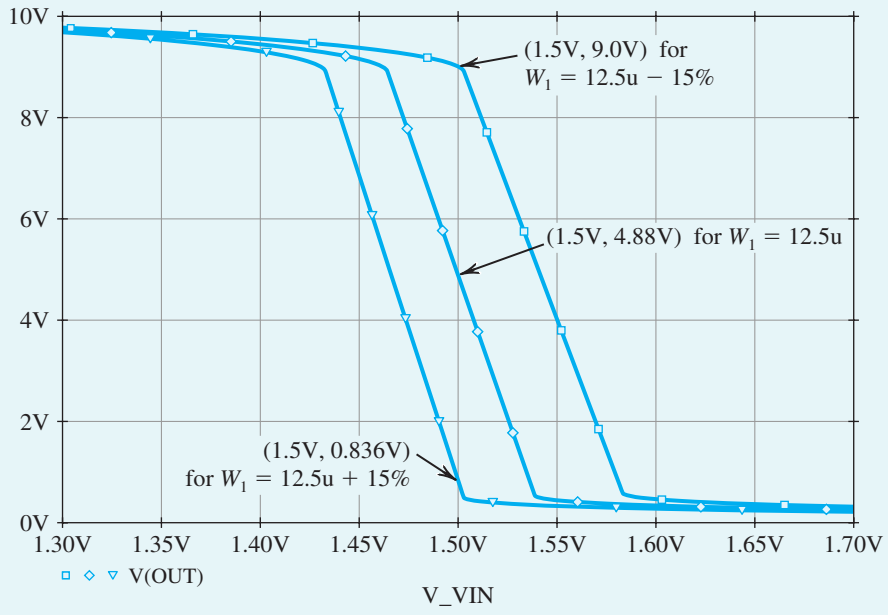
where $V_{An}$ and $V_{Ap}$ are the magnitudes of the Early voltages of, respectively, the NMOS and PMOS transistors. Unit-size transistors are used with $W/L = 12.5\ \mu m/6\ \mu m$ for the NMOS devices and $W/L = 37.5\ \mu m/6\ \mu m$ for the PMOS devices. Thus, using Eq. (B.24) together with the 5-μm CMOS process parameters in Table B.4, we find $m_1 = 10$ and $m_2 = m_3 = 2$ (rounded to the nearest integer). Furthermore, Eq. (B.25) gives $G_v = -100$ V/V.

To compute the dc transfer characteristic of the CS amplifier, we perform a dc analysis in PSpice with $V_{IN}$ swept over the range 0 to $V_{DD}$ and plot the corresponding output voltage $V_{OUT}$. Figure B.25 (a) shows the resulting transfer characteristic. The slope of this characteristic (i.e., $dV_{OUT}/dV_{IN}$) corresponds to the gain of the amplifier. The high-gain segment is clearly visible for $V_{IN}$ around 1.5 V. This corresponds to an overdrive voltage for $M_1$ of $V_{OV1} = V_{IN} - V_{tn} = 0.5$ V, as desired. To examine the high-gain region more closely, we repeat the dc sweep for $V_{IN}$ between 1.3 V and 1.7 V. The resulting transfer characteristic is plotted in Fig. B.25 (b, middle curve). Using the Probe graphical interface of PSpice, we find that the linear region of this dc transfer characteristic is bounded approximately by $V_{IN} = 1.465$ V and $V_{IN} = 1.539$ V. The corresponding values of $V_{OUT}$ are 8.838 V and 0.573 V. These results are close to the expected values. Specifically, transistors $M_1$ and $M_2$ will remain in the saturation region and, hence, the amplifier will operate in its linear region if $V_{OV1} \le V_{OUT} \le V_{DD} - V_{OV2}$ or $0.5\ V \le V_{OUT} \le 9$ V. From the results above, the voltage gain $G_v$ (i.e., the slope of the linear segment of the dc transfer characteristic) is approximately $-112$ V/V , which is reasonably close to the value obtained by hand ianalysis.




(a)

**Figure B.25** **(a)** Voltage transfer characteristic of the CS amplifier in Example PS.7.1. **(b)** Expanded view of the transfer characteristic in the high-gain region. Also shown are the transfer characteristics where process variations cause the width of transistor $M_1$ to change by +15% and −15% from its nominal value of $W_1 = 12.5$ μm.




(b)

**Figure 8.25** *continued*

Note from the dc transfer characteristic in Fig. B.25(b) that for an input dc bias of $V_{IN} = 1.5$ V, the output dc bias is $V_{OUT} = 4.88$ V. This choice of $V_{IN}$ maximizes the available signal swing at the output by setting $V_{OUT}$ at the middle of the linear segment of the dc transfer characteristic. However, because of the high resistance at the output node (or, equivalently, because of the high voltage gain), this value of $V_{OUT}$ is highly sensitive to the effect of process and temperature variations on the characteristics of the transistors. To illustrate this point, consider what happens when the width of $M_1$ (i.e., $W_1$, which is normally 12.5 μm) changes by ±15%. The corresponding dc transfer characteristics are shown in Fig. B.25(b). Accordingly, when $V_{IN} = 1.5$ V, $V_{OUT}$ will drop to 0.84 V if $W_1$ increases by 15% and will rise to 9.0 V if $W_1$ decreases by 15%. In practical circuit implementations, this problem is circumvented by using negative feedback to accurately set the dc bias voltage at the output of the amplifier and, hence, to reduce the sensitivity of the circuit to process variations. We studied negative feedback in Chapter 9.

## Example PS.8.1

### A Multistage Differential BJT Amplifier

The schematic capture of the multistage op-amp circuit analyzed in Examples 7.1 and 7.7 is shown in Fig. B.26.[11] Observe the manner in which the differential signal input $V_d$ and the common-mode input voltage $V_{CM}$ are applied. Such an input bias configuration for an op-amp circuit was presented and used in Example PS.2.2. In the following simulations, we will use parts Q2N3904 and Q2N3906 (from Fairchild

[11]This circuit cannot be simulated using the student evaluation version of PSpice. This is because, in this free version of PSpice, circuit simulation is restricted to circuits with no more than 10 transistors.

**Example PS.8.1** *continued*

Semiconductor) for the *npn* and *pnp* BJTs, respectively. The model parameters of these discrete BJTs are listed in Table B.8 and are available in PSpice.

**Table B.8** Spice Model Parameters of the Q2N3904 and Q2N3906 Discrete BJTs

| | | | | | | |
|---|---|---|---|---|---|---|
| **Q2N3904 Discrete BJT** | | | | | | |
| IS = 6.734f | XTI = 3 | EG = 1.11 | VAF = 74.03 | BF = 416.4 | NE = 1.259 | ISE = 6.734f |
| IKF = 66.78m | XTB = 1.5 | BR = .7371 | NC = 2 | ISC = 0 | IKR = 0 | RC = 1 |
| CJC = 3.638p | MJC = .3085 | VJC = .75 | FC = .5 | CJE = 4.493p | MJE = .2593 | VJE = .75 |
| TR = 239.5n | TF = 301.2p | ITF = .4 | VTF = 4 | XTF = 2 | RB = 10 | |
| **Q2N3906 Discrete BJT** | | | | | | |
| IS = 1.41f | XTI = 3 | EG = 1.11 | VAF = 18.7 | BF = 180.7 | NE = 1.5 | ISE = 0 |
| IKF = 80m | XTB = 1.5 | BR = 4.977 | NC = 2 | ISC = 0 | IKR = 0 | RC = 2.5 |
| CJC = 9.728p | MJC = .5776 | VJC = .75 | FC = .5 | CJE = 8.063p | MJE = .3677 | VJE = .75 |
| TR = 33.42n | TF = 179.3p | ITF = .4 | VTF = 4 | XTF = 6 | RB = 10 | |

**Table B.9** DC Collector Currents of the Op-Amp Circuit in Fig. B.26 as Computed by Hand Analysis (Example 8.6) and by PSpice

| | Collector Currents (mA) | | |
|---|---|---|---|
| Transistor | Hand Analysis (Example 8.6) | PSpice | Error (%) |
| $Q_1$ | 0.25 | 0.281 | −11.0 |
| $Q_2$ | 0.25 | 0.281 | −11.0 |
| $Q_3$ | 0.5 | 0.567 | −11.8 |
| $Q_4$ | 1.0 | 1.27 | −21.3 |
| $Q_5$ | 1.0 | 1.21 | −17.4 |
| $Q_6$ | 2.0 | 2.50 | −20.0 |
| $Q_7$ | 1.0 | 1.27 | −21.3 |
| $Q_8$ | 5.0 | 6.17 | −18.9 |
| $Q_9$ | 0.5 | 0.48 | +4.2 |

In PSpice, the common-mode input voltage $V_{CM}$ of the op-amp circuit is set to 0 V (i.e., to the average of the dc power-supply voltages $V_{CC}$ and $V_{EE}$) to maximize the available input signal swing. A bias-point simulation is performed to determine the dc operating point. Table B.9 summarizes the value of the dc collector currents as computed by PSpice and as calculated by the hand analysis in Example 7.6. Recall that our hand analysis assumed both $\beta$ and the Early voltage $V_A$ of the BJTs to be infinite. However, our SPICE simulations in Example PS.6.1 (where we investigated the dependence of $\beta$ on the collector current $I_C$) indicate that the Q2N3904 has $\beta \simeq 125$ at $I_C = 0.25$ mA. Furthermore, its forward Early voltage (SPICE parameter VAF) is 74 V, as given in Table B.8. Nevertheless, we observe from Table B.9 that the largest error in the calculation of the dc bias currents is on the order of 20%. Accordingly, we can conclude that a quick hand analysis using gross approximations can still yield reasonable results for a preliminary estimate and, of course, hand analysis yields much insight into the circuit operation. In addition to the dc bias currents listed in Table B.9, the bias-point simulation in PSpice shows that the output dc offset (i.e., $V_{\text{OUT}}$ when $V_d = 0$) is 3.62 V and that the input bias current $I_{B1}$ is 2.88 μA.

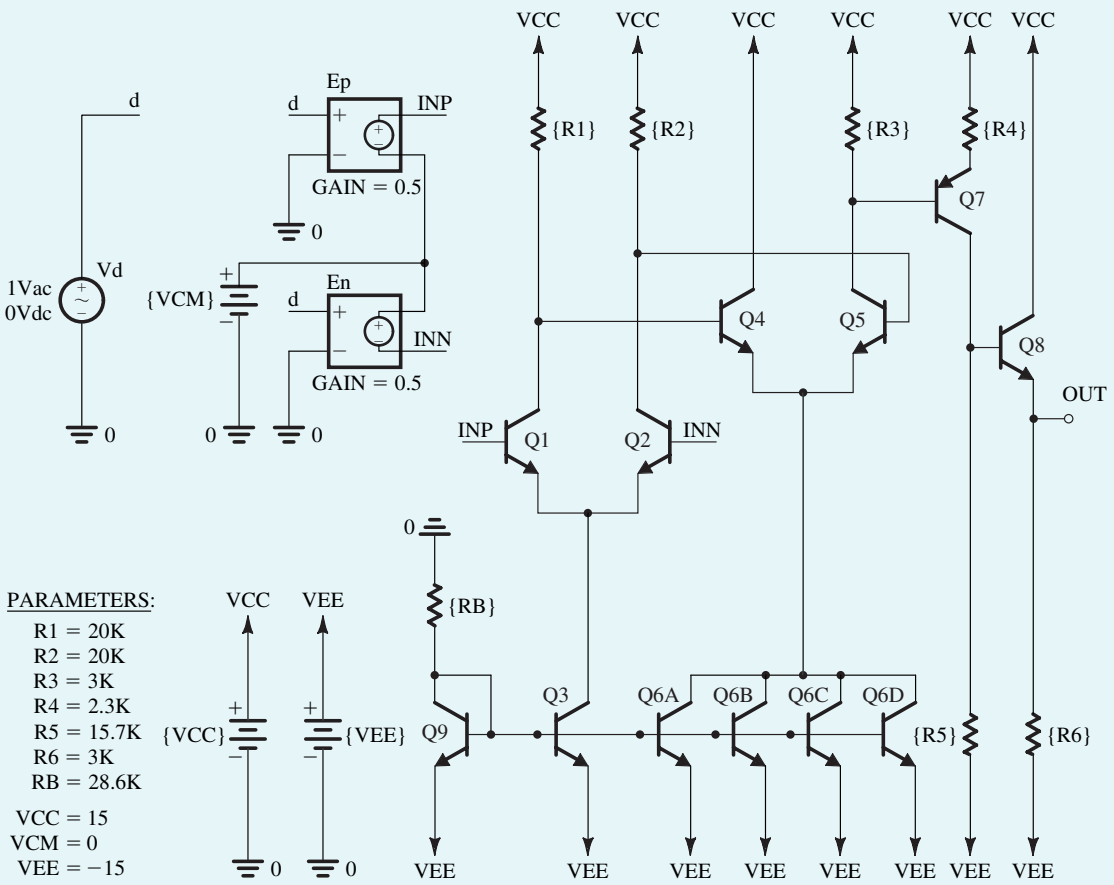
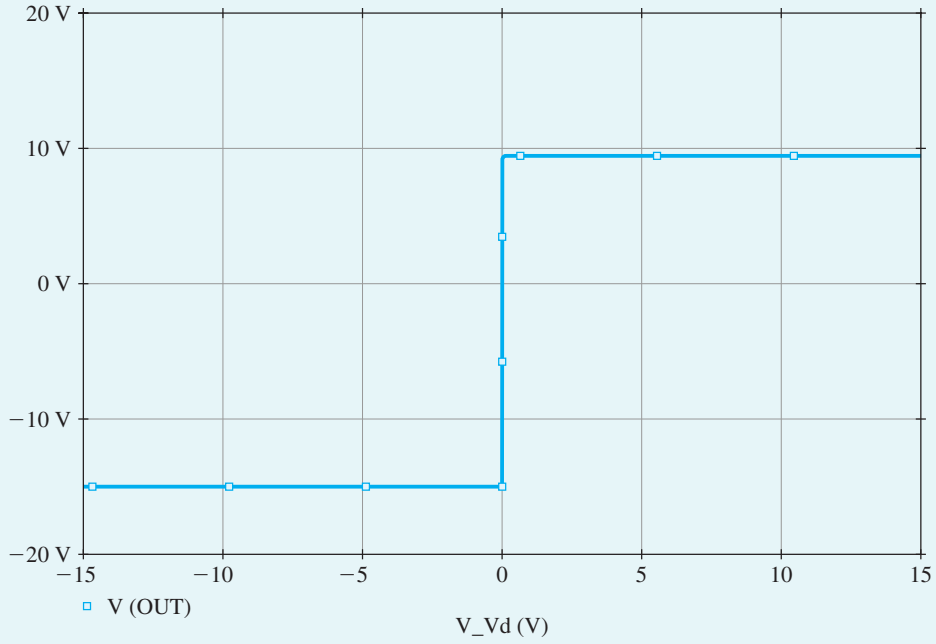


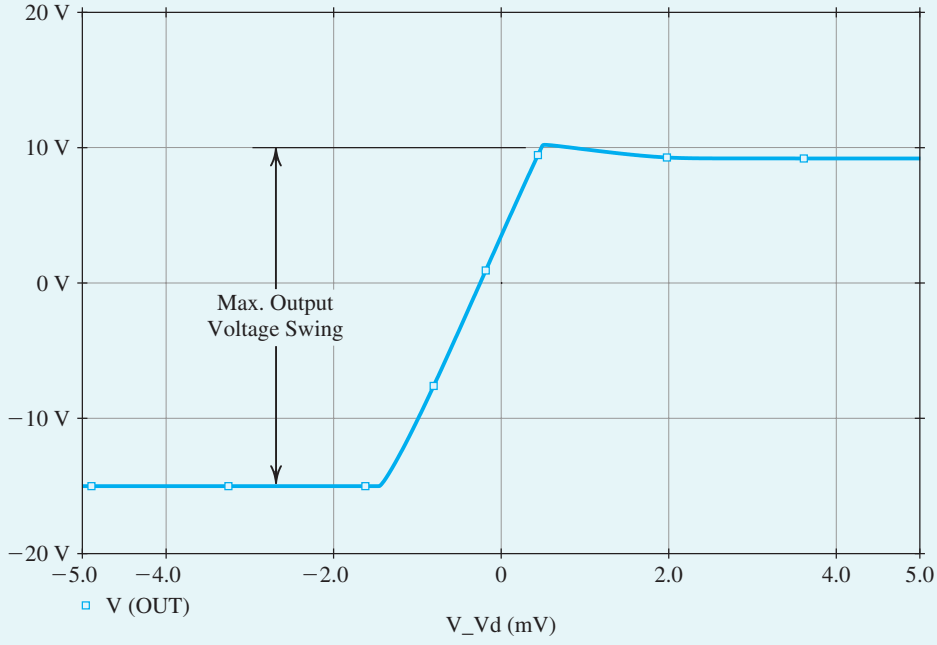

**Figure B.26** Schematic capture of the op-amp circuit in Example 6.6.

To compute the **large-signal differential transfer characteristic** of the op-amp circuit, we perform a dc-analysis simulation in PSpice with the differential voltage input $V_d$ swept over the range $-V_{EE}$ to $+V_{CC}$, and we plot the corresponding output voltage $V_{\text{OUT}}$. Figure B.27(a) shows the resulting dc transfer characteristic. The slope of this characteristic (i.e., $dV_{\text{OUT}}/dV_d$) corresponds to the differential gain of the amplifier. Note that, as expected, the high-gain region is in the vicinity of $V_d = 0$ V. However, the resolution of the input-voltage axis is too coarse to yield much information about the details of the high-gain region. Therefore, to examine this region more closely, the dc analysis is repeated with $V_d$ swept over the range $-5$ mV to $+5$ mV at increments of 10 μV. The resulting differential dc transfer characteristic is plotted in Fig. B.27(b). We observe that the linear region of the large-signal differential characteristic is bounded approximately by $V_d = -1.5$ mV and $V_d = +0.5$ mV. Over this region, the output level changes from $V_{\text{OUT}} = -15$ V to about $V_{\text{OUT}} = +10$ V in a linear fashion. Thus, the output voltage swing for this amplifier is between $-15$ V and $+10$ V, a rather asymmetrical range. A rough estimate for the differential gain of this amplifier can be obtained from the boundaries of the linear region as $A_d = [10 - (-15)]\ \text{V}/[0.5 - (-1.5)]\ \text{mV} = 12.5 \times 10^3\ \text{V/V}$. We also observe from Fig B.27(b) that $V_d \simeq -260$ μV when $V_{\text{OUT}} = 0$. Therefore, the amplifier has an input offset voltage $V_{OS}$ of +260 μV (by convention, the negative value of the $x$-axis intercept of the large-signal differential transfer characteristic). This corresponds to an output offset voltage of $A_d V_{OS} \simeq (12.5 \times 10^3)\ (260\ \mu\text{V}) = 3.25$ V, which is

**Example PS.8.1** *continued*




(a)




(b)

**Figure B.27** **(a)** The large-signal differential transfer characteristic of the op-amp circuit in Fig. B.26. The common-mode input voltage $V_{CM}$ is set to 0 V. **(b)** An expanded view of the transfer characteristic in the high-gain region.

close to the value found through the bias-point simulation. It should be emphasized that this offset voltage is inherent in the design and is not the result of component or device mismatches. Thus, it is usually referred to as a **systematic offset**.

Next, to compute the frequency response of the op-amp circuit[12] and to measure its differential gain $A_d$ and its 3-dB frequency $f_H$ in PSpice, we set the differential input voltage $V_d$ to be a 1-V ac signal (with 0-V dc level), perform an ac-analysis simulation, and plot the output voltage magnitude $|V_{OUT}|$ versus frequency. Figure B.28(a) shows the resulting frequency response. Accordingly, $A_d = 13.96 \times 10^3$ V/V or 82.8 dB, and $f_H = 256.9$ kHz. Thus, this value of $A_d$ is close to the value estimated using the large-signal differential transfer characteristic.

An approximate value of $f_H$ can also be obtained using the expressions derived in Section 8.8. Specifically,

$$f_H \simeq \frac{1}{2\pi R_{\text{eq}} C_{\text{eq}}} \tag{B.26}$$

where

$$C_{\text{eq}} = C_{\mu 2} + C_{\pi 5} + C_{\mu 5}[1 + g_{m5}(R_3 \parallel r_{o5} \parallel (r_{\pi 7} + (\beta + 1)R_4))]$$

and

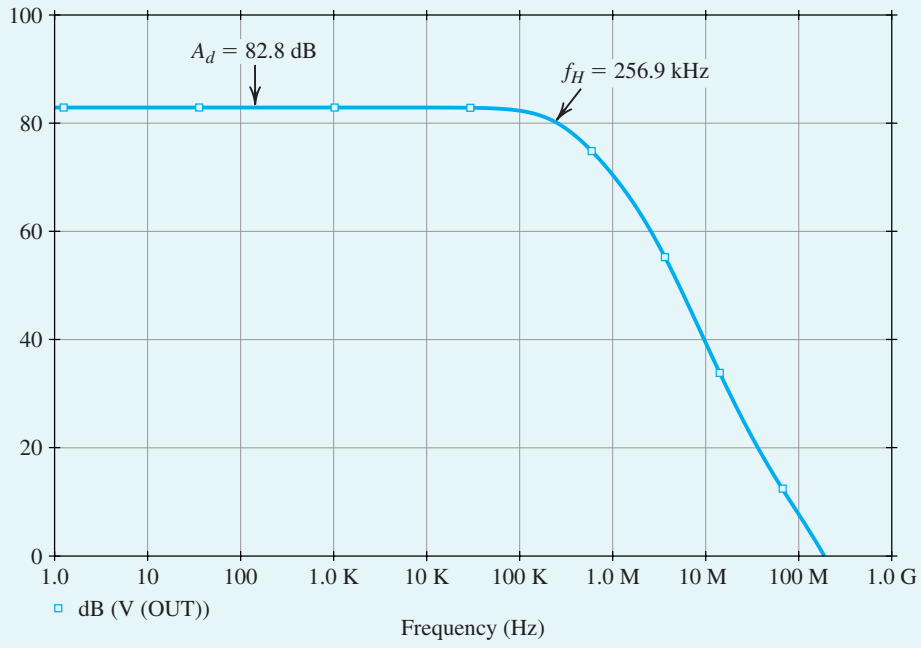
$$R_{\text{eq}} = R_2 \parallel r_{o2} \parallel r_{\pi 5}$$

The values of the small-signal parameters as computed by PSpice can be found in the output file of a bias-point (or an ac-analysis) simulation. Using these values results in $C_{\text{eq}} = 338$ pF, $R_{\text{eq}} = 2.91$ kΩ, and $f_H = 161.7$ kHz. However, this approximate value of $f_H$ is much smaller than the value computed by PSpice. The reason for this disagreement is that the foregoing expression for $f_H$ was derived (in Section 8.8) using the equivalent differential half-circuit concept. However, the concept is accurate only when it is applied to a symmetrical circuit. The op-amp circuit in Fig. B.26 is not symmetrical because the second gain stage formed by the differential pair $Q_4$–$Q_5$ has a load resistor $R_3$ in the collector of $Q_5$ only. To verify that the expression for $f_H$ in Eq. (B.26) gives a close approximation for $f_H$ in the case of a symmetric circuit, we insert a resistor $R_3'$ (whose size is equal to $R_3$) in the collector of $Q_4$. Note that this will have only a minor effect on the dc operating point. The op-amp circuit with $Q_4$ having a collector resistor $R_3'$ is then simulated in PSpice. Figure B.28(b) shows the resulting frequency response of this symmetric op amp, where $f_H = 155.7$ kHz. Accordingly, in the case of a perfectly symmetric op-amp circuit, the value of $f_H$ in Eq. (B.26) closely approximates the value computed by PSpice. Comparing the frequency responses of the nonsymmetric (Fig. B.28a) and the symmetric (Fig. B.28b) op-amp circuits, we note that the 3-dB frequency of the op amp drops from 256.9 kHz to 155.7 kHz when resistor $R_3'$ is inserted in the collector of $Q_4$ to make the op-amp circuit symmetrical. This is because, with a resistor $R_3'$, the collector of $Q_4$ is no longer at signal ground and, hence, $C_{\mu 4}$ experiences the Miller effect. Consequently, the high-frequency response of the op-amp circuit is degraded.

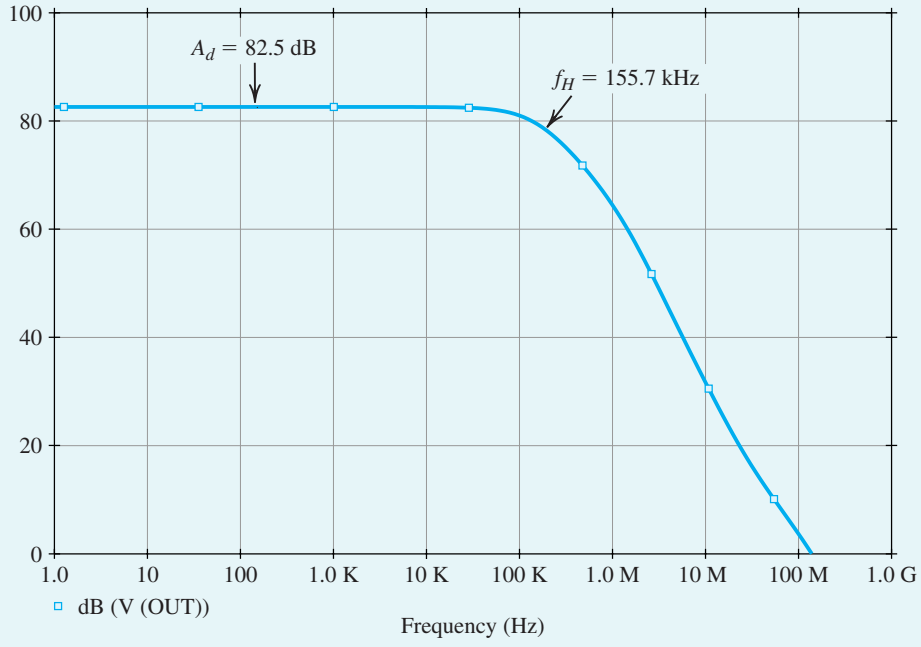
Observe that in the preceding ac-analysis simulation, owing to the systematic offset inherent in the design, the op-amp circuit is operating at an output dc voltage of 3.62 V. However, in an actual circuit implementation (with $V_{CM} = 0$), negative feedback is employed (see Chapters 2 and 9) and the output dc voltage is stabilized at zero. Thus, the small-signal performance of the op-amp circuit can be more accurately simulated by biasing the circuit so as to force operation at this level of output voltage. This can be easily done by applying a differential dc input of $-V_{OS}$. Superimposed on this dc

[12]This part of the example requires study of Sections 8.8 and 8.10.2.

Example PS.8.1 *continued*




(a)




(b)

**Figure B.28** Frequency response of **(a)** the op-amp circuit in Fig. B.26 and **(b)** the op-amp circuit in Fig. B.26 but with a resistor $R_3' = R_3$ inserted in the collector of $Q_4$ to make the op-amp circuit symmetrical.

input, we can apply an ac signal to perform an ac-analysis simulation for the purpose of, for example, computing the differential gain and the 3-dB frequency.

Finally, to compute the input common-mode range of the op-amp circuit in Fig. B.26, we perform a dc-analysis simulation in PSpice with the input common-mode voltage swept over the range $-V_{EE}$ to $V_{CC}$, while maintaining $V_d$ constant at $-V_{OS}$ in order to cancel the output offset voltage (as discussed earlier) and, thus, prevent premature saturation of the BJTs. The corresponding output voltage $V_{\text{OUT}}$ is plotted in Fig. B.29(a). From this common-mode dc transfer characteristic we find that the amplifier behaves linearly over the $V_{CM}$ range −14.1 V to +8.9 V, which is therefore the **input common-mode range**. In Example 7.6, we noted that the upper limit of this range is determined by $Q_1$ and $Q_2$ saturating, whereas the lower limit is determined by $Q_3$ saturating. To verify this assertion, we requested PSpice to plot the values of the collector–base voltages of these BJTs versus the input common-mode voltage $V_{CM}$. The results are shown in Fig. B.29(b), from which we note that our assertion is indeed correct (recall that an *npn* BJT enters its saturation region when its base–collector junction becomes forward biased, i.e., $V_{BC} \geq 0$ ).

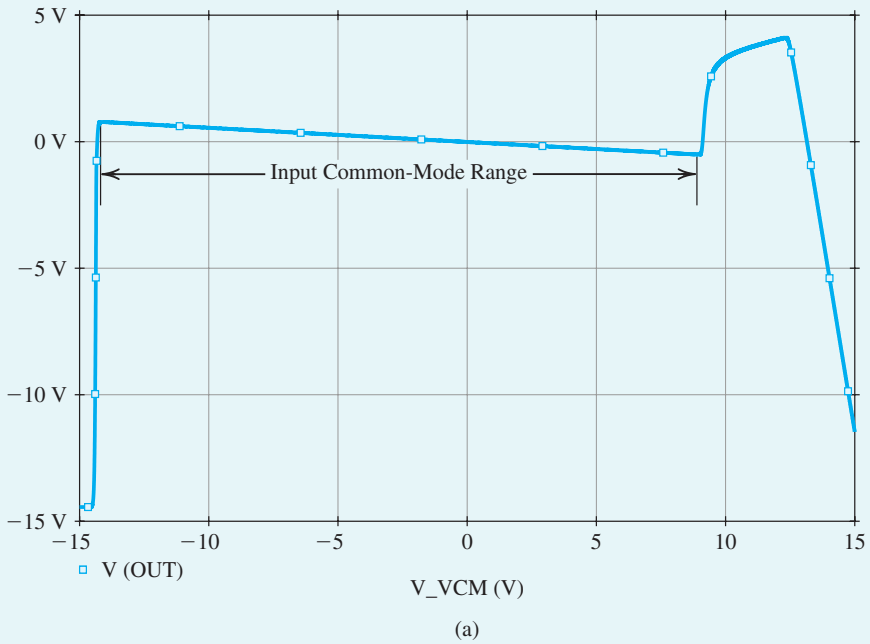
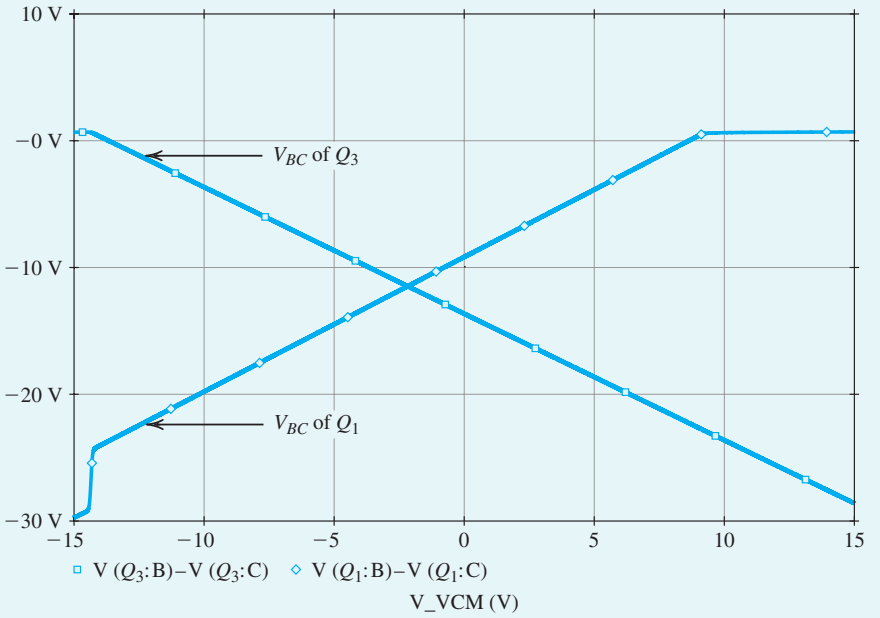



**Figure B.29** **(a)** The large-signal common-mode transfer characteristic of the op-amp circuit in Fig. B.26. The differential input voltage $V_d$ is set to $-V_{OS} = -260$ μV to prevent premature saturation. **(b)** The effect of the common-mode input voltage VCM on the linearity of the input stage of the op-amp circuit in Fig. B.26. The base–collector voltage of $Q_1$ and $Q_3$ is shown as a function of VCM. The input stage of the op-amp circuit leaves the active region when the base–collector junction of either $Q_1$ or $Q_3$ becomes forward biased (i.e., when VBC ≥ 0 ).

Example PS.8.1 *continued*




(b)

**Figure B.29** (*Contd.*).

## Example PS.9.1

### Frequency Response of the CMOS CS and the Folded-Cascode Amplifiers

In this example, we will use PSpice to compute the frequency response of both the CS and the folded-cascode amplifiers whose schematic capture diagrams are shown shortly in Figs. B.30 and B.32, respectively. We will assume that the dc bias levels at the output of the amplifiers are stabilized using negative feedback. However, before performing a small-signal analysis (an ac-analysis simulation) in SPICE to measure the frequency response, we will perform a dc analysis (a bias-point simulation) to verify that all MOSFETs are operating in the saturation region and, hence, ensure that the amplifier is operating in its linear region.

In the following, we will assume a 0.5-μm CMOS technology for the MOSFETs and use parts NMOSOP5 and PMOSOP5 whose SPICE level-1 model parameters are listed in Table B.3. To specify the dimensions of the MOSFETs in PSpice, we will use the multiplicative factor $m$, together with the channel length $L$ and channel width $W$ (as we did in Example PS.7.1).

### The CMOS CS Amplifier

The CS amplifier circuit in Fig. B.30 is identical to the one shown in Fig. 6.4, except that a current source is connected to the source of the input transistor $M_1$ to set its drain current $I_{D1}$ independently of its drain voltage $V_{D1}$. Furthermore, in our PSpice simulations, we used an impractically large bypass capacitor $C_S$ of 1 F. This sets the source of $M_1$ at approximately signal ground during the ac-analysis simulation. Accordingly, the CS amplifier circuits in Figs. 6.4 and B.30 are equivalent for the purpose of frequency-response

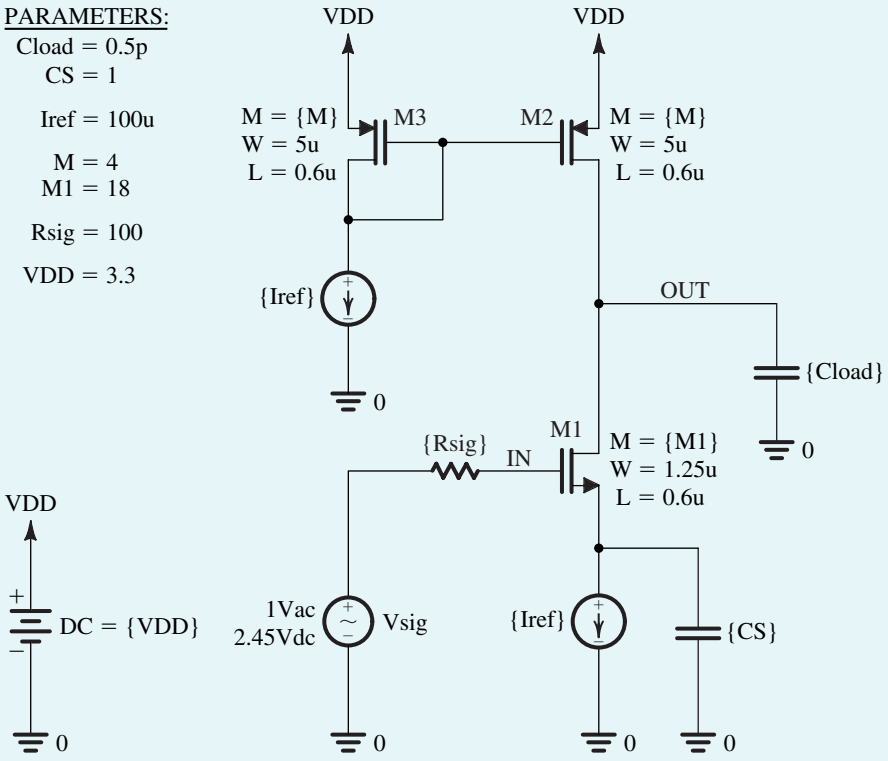



**Figure B.30** Schematic capture of the CS amplifier in Example PS.9.1

analysis. In Chapter 7, we found out, in the context of studying the differential pair, how the goals of this biasing approach for the CS amplifier are realized in practical IC implementations.

The CS amplifier in Fig. B.30 is designed assuming a reference current $I_{ref} = 100$ μA and $V_{DD} = 3.3$ V. The current-mirror transistors, $M_2$ and $M_3$, are sized for $V_{OV2} = V_{OV3} = 0.3$ V, while the input transistor $M_1$ is sized for $V_{OV1} = 0.15$ V. Unit-size transistors are used with $W/L = 1.25\ \mu m/0.6\ \mu m$ for the NMOS devices and $W/L = 5\ \mu m/0.6\ \mu m$ for the PMOS devices. Thus, using the square law $I_D - V_{OV}$ of the MOSFET together with the 0.5-μm CMOS process parameters in Table B.4, we find $m_1 = 18$ and $m_2 = m_3 = 4$. Furthermore, Eq. (B.25) gives $G_v = -44.4$ V/V for the CS amplifier.

In the PSpice simulations of the CS amplifier in Fig. B.30, the dc bias voltage of the signal source is set such that the voltage at the source terminal of $M_1$ is $V_{S1} = 1.3$ V. This requires the dc level of $V_{sig}$ to be $V_{OV1} + V_{tn1} + V_{S1} = 2.45$ V because $V_{tn1} \simeq 1$ V as a result of the body effect on $M_1$. The reasoning behind this choice of $V_{S1}$ is that, in a practical circuit implementation, the current source that feeds the source of $M_1$ is realized using a cascode current mirror such as the one in Fig. 6.32. In this case, the minimum voltage required across the current source (i.e., the minimum $V_{S1}$) is $V_t + 2V_{OV} = 1.3$ V, assuming $V_{OV} = 0.3$ V for the current-mirror transistors.

A bias-point simulation is performed in PSpice to verify that all MOSFETs are biased in the saturation region. Next, to compute the frequency response of the amplifier, we set the ac voltage of the signal source to 1 V, perform an ac-analysis simulation, and plot the output voltage magnitude versus frequency. Figure B.31(a) shows the resulting frequency response for $R_{sig} = 100\ \Omega$ and $R_{sig} = 1\ M\Omega$. In both cases, a load capacitance of $C_{load} = 0.5$ pF is used. The corresponding values of the 3-dB frequency $f_H$ of the amplifier are given in Table B.10.

**Example PS.9.1** *continued*

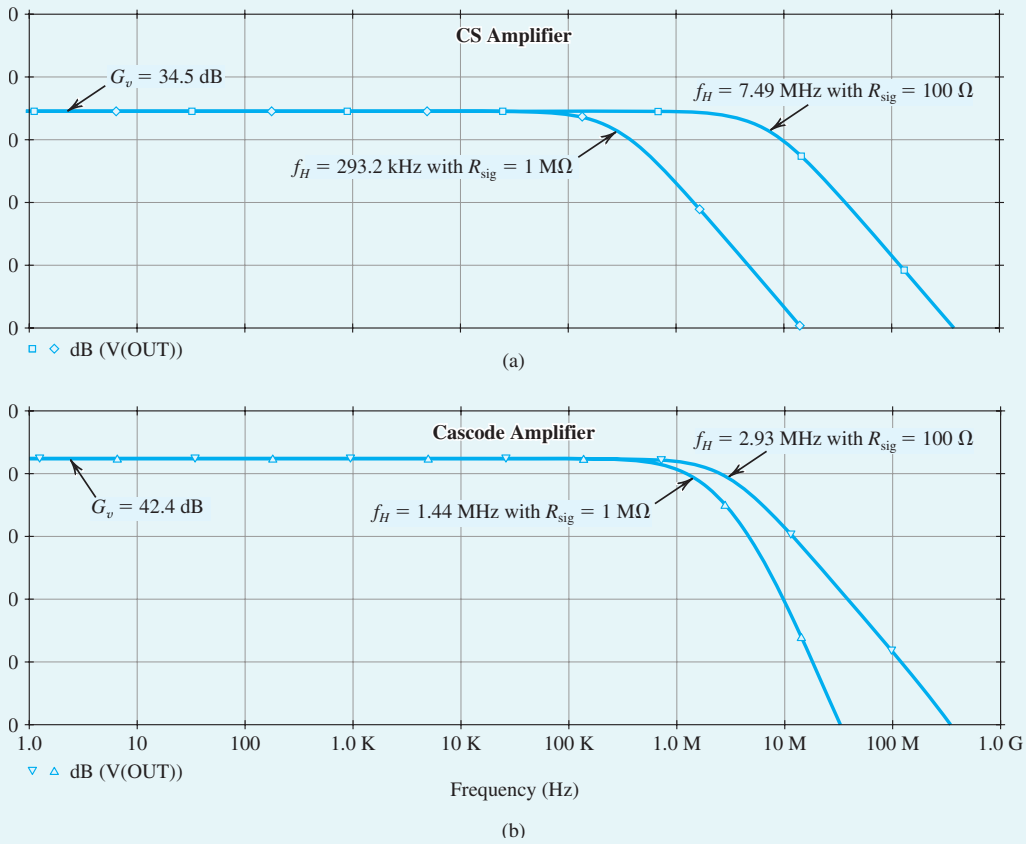



**Figure B.31** Frequency response of **(a)** the CS amplifier and **(b)** the folded-cascode amplifier in Example PS.9.1, with $R_{sig}$ = 100 Ω and $R_{sig}$ = 1 MΩ.

Observe that $f_H$ drops when $R_{sig}$ is increased. This is anticipated from our study of the high-frequency response of the CS amplifier in Section 8.3. Specifically, as $R_{sig}$ increases, the pole

$$f_{p,\,\text{in}} = \frac{1}{2\pi R_{\text{sig}} C_{\text{in}}} \tag{B.27}$$

formed at the amplifier input will have an increasingly significant effect on the overall frequency response of the amplifier. As a result, the effective time constant $\tau_H$ in Eq. (8.85) increases and $f_H$ decreases. When $R_{sig}$ becomes very large, as it is when $R_{sig}$ = 1 MΩ, a dominant pole is formed by $R_{sig}$ and $C_{in}$. This results in

$$f_H \simeq f_{p,\,\text{in}} \tag{B.28}$$

To estimate $f_{p,\text{in}}$, we need to calculate the input capacitance $C_{in}$ of the amplifier. Using Miller's theorem, we have

$$\begin{aligned} C_{\text{in}} &= C_{gs1} + C_{gd1}(1 + g_{m1}R'_L) \\ &= (\tfrac{2}{3}m_1 W_1 L_1 C_{ox} + C_{gs,\,ov1}) + C_{gd,\,ov1}(1 + g_{m1}R'_L) \end{aligned} \tag{B.29}$$

**Table B.10** Dependence of the 3-dB Bandwidth $f_H$ on $R_{sig}$ for the CS and the Folded-Cascode Amplifiers in Example PS.9.1

| | $f_H$ | |
|---|---|---|
| $R_{sig}$ | CS Amplifier | Folded-Cascode Amplifier |
| 100 Ω | 7.49 MHz | 2.93 MHz |
| 1 MΩ | 293.2 kHz | 1.44 MHz |

where

$$R'_L = r_{o1} \parallel r_{o2} \tag{B.30}$$

Thus, $C_{in}$ can be calculated using the values of $C_{gs1}$ and $C_{gd1}$, which are computed by PSpice and can be found in the output file of the bias-point simulation. Alternatively, $C_{in}$ can be found using Eq. (B.29) with the values of the overlap capacitances $C_{gs,\,ov1}$ and $C_{gd,\,ov1}$ calculated using the process parameters in Table B.4 (as described in Eqs. B.9 and B.10); that is:

$$C_{gs,\,ov1} = m_1 W_1 CGSO \tag{B.31}$$

$$C_{gd,\,ov1} = m_1 W_1 CGDO \tag{B.32}$$

This results in $C_{in} = 0.53$ pF when $|G_v| = g_{m1} R'_L = 53.2$ V/V. Accordingly, using Eqs. (B.27) and (B.28), $f_H = 300.3$ kHz when $R_{sig} = 1$ MΩ, which is close to the value computed by PSpice.

## The Folded-Cascode Amplifier

The folded-cascode amplifier circuit in Fig. B.32 is equivalent to the one in Fig. 6.16, except that a current source is placed in the source of the input transistor $M_1$ (for the same dc-biasing purpose as in the case of the CS amplifier). Note that, in Fig. B.32, the PMOS current mirror $M_3$–$M_4$ and the NMOS current mirror $M_5$–$M_6$ are used to realize, respectively, current sources $I_1$ and $I_2$ in the circuit of Fig. 6.16. Furthermore, the current transfer ratio of mirror $M_3$–$M_4$ is set to 2 (i.e., $m_3/m_4 = 2$). This results in $I_{D3} \simeq 2I_{ref}$. Hence, transistor $M_2$ is biased at $I_{D2} = I_{D3} - I_{D1} = I_{ref}$. The gate bias voltage of transistor $M_2$ is generated using the diode-connected transistors $M_7$ and $M_8$. The size and drain current of these transistors are set equal to those of transistor $M_2$. Therefore, ignoring the body effect,

$$V_{G2} = V_{DD} - V_{SG7} - V_{SG8} \simeq V_{DD} - 2(|V_{tp}| + |V_{OVp}|)$$

where $V_{OVp}$ is the overdrive voltage of the PMOS transistors in the amplifier circuit. These transistors have the same overdrive voltage because their $I_D/m$ is the same. Thus, such a biasing configuration results in $V_{SG2} = |V_{tp}| + |V_{OVp}|$ as desired, while setting $V_{SD3} = |V_{tp}| + |V_{OVp}|$ to improve the bias matching between $M_3$ and $M_4$.

The folded-cascode amplifier in Fig. B.32 is designed assuming a reference current $I_{ref} = 100$ μA and $V_{DD} = 3.3$ V (similar to the case of the CS amplifier). All transistors are sized for an overdrive voltage of 0.3 V, except for the input transistor $M_1$, which is sized for $V_{OV1} = 0.15$ V. Thus, since $I_D = \frac{1}{2}\mu C_{ox} m (W/L_{eff}) V_{OV}^2$, all the MOSFETs in the amplifier circuit are designed using $m = 4$, except for $m_1 = 18$.

The midband voltage gain of the folded-cascode amplifier in Fig. B.32 can be expressed as

$$G_v = -g_{m1} R_{out} \tag{B.33}$$

where

$$R_{out} = R_{out2} \parallel R_{out5} \tag{B.34}$$

**Example PS.9.1** *continued*

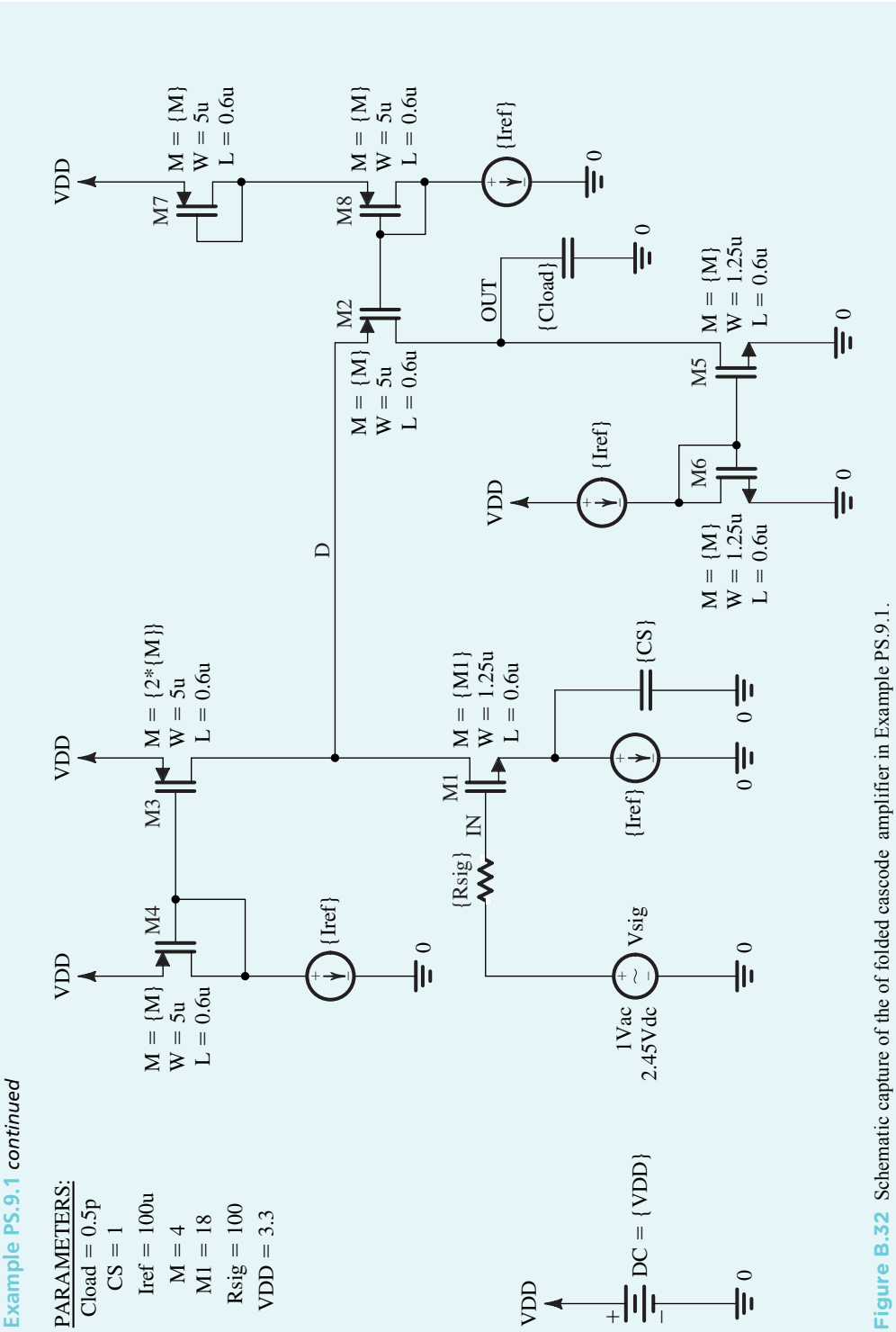



**Figure B.32** Schematic capture of the of folded cascode amplifier in Example PS.9.1.

is the output resistance of the amplifier. Here, $R_{out2}$ is the resistance seen looking into the drain of the cascode transistor $M_2$, while $R_{out5}$ is the resistance seen looking into the drain of the current-mirror transistor $M_5$. Using Eq. (6.25), we have

$$R_{out2} \simeq (g_{m2}r_{o2})R_{s2} \tag{B.35}$$

where

$$R_{s2} = r_{o1} \| r_{o3} \tag{B.36}$$

is the effective resistance at the source of $M_2$. Furthermore,

$$R_{out5} = r_{o5} \tag{B.37}$$

Thus, for the folded-cascoded amplifier in Fig. B.32,

$$R_{out} \simeq r_{o5} \tag{B.38}$$

and

$$G_v \simeq -g_{m1}r_{o5} = -2\frac{V_{An}}{V_{OV1}} \tag{B.39}$$

Using the 0.5-μm CMOS parameters, this gives $R_{out} = 100$ kΩ and $G_v = -133$ V/V. Therefore, $R_{out}$ and hence $|G_v|$ of the folded-cascode amplifier in Fig. B.32 are larger than those of the CS amplifier in Fig. B.30 by a factor of 3.

Figure B.31(b) shows the frequency response of the folded-cascode amplifier as computed by PSpice for the cases of $R_{sig} = 100\ \Omega$ and $R_{sig} = 1$ MΩ. The corresponding values of the 3-dB frequency $f_H$ of the amplifier are given in Table B.10. Observe that when $R_{sig}$ is small, $f_H$ of the folded-cascode amplifier is lower than that of the CS amplifier by a factor of approximately 2.6, approximately equal to the factor by which the gain is increased. This is because when $R_{sig}$ is small, the frequency response of both amplifiers is dominated by the pole formed at the output node, that is,

$$f_H \simeq f_{p,out} = \frac{1}{2\pi}\frac{1}{R_{out}C_{out}} \tag{B.40}$$

Since the output resistance of the folded-cascode amplifier is larger than that of the CS amplifier (by a factor of approximately 3, as found through the hand analysis above) while their output capacitances are approximately equal, the folded-cascode amplifier has a lower $f_H$ in this case.

On the other hand, when $R_{sig}$ is large, $f_H$ of the folded-cascode amplifier is much higher than that of the CS amplifier. This is because, in this case, the effect of the pole at $f_{p,in}$ on the overall frequency response of the amplifier becomes significant. Since, due to the Miller effect, $C_{in}$ of the CS amplifier is much larger than that of the folded-cascode amplifier, its $f_H$ is much lower in this case. To confirm this point, observe that $C_{in}$ of the folded-cascode amplifier can be estimated by replacing $R'_L$ in Eq. (B.29) with the total resistance $R_{d1}$ between the drain of $M_1$ and ground. Here,

$$R_{d1} = r_{o1} \| r_{o3} \| R_{in2} \tag{B.41}$$

where $R_{in2}$ is the input resistance of the common-gate transistor $M_2$ and can be obtained using an approximation of the relationship in Eq. (6.34) as

$$R_{in2} \simeq \frac{r_{o2} + r_{o5}}{g_{m2}r_{o2}} \tag{B.42}$$

Thus,

$$R_{d1} \simeq r_{o1} \| r_{o3} \| \left(\frac{r_{o2} + r_{o5}}{g_{m2}r_{o2}} \simeq \frac{2}{g_{m2}}\right) \tag{B.43}$$

**Example PS.9.1** *continued*

Therefore, $R_{d1}$ is much smaller than $R_L'$ in Eq. (B.30). Hence, $C_{\text{in}}$ of the folded-cascode amplifier in Fig. B.32 is indeed much smaller than that of the CS amplifier in Fig. B.30. This confirms that the folded-cascode amplifier is much less impacted by the Miller effect and, therefore, can achieve a much higher $f_H$ when $R_{sig}$ is large.

The midband gain of the folded-cascode amplifier can be significantly increased by replacing the current mirror $M_5$–$M_6$ with a current mirror having a larger output resistance, such as the cascode current mirror in Fig. 6.32 whose output resistance is approximately $g_m r_o^2$. In this case, however, $R_{\text{in2}}$ and hence $R_{d1}$ increase, causing an increased Miller effect and a corresponding reduction in $f_H$.

Finally, it is interesting to observe that the frequency response of the folded-cascode amplifier, shown in Fig. B.31(b), drops beyond $f_H$ at approximately –20 dB/decade when $R_{\text{sig}} = 100\ \Omega$ and at approximately –40 dB/decade when $R_{sig} = 1\ \text{M}\Omega$. This is because when $R_{\text{sig}}$ is small, the frequency response is dominated by the pole at $f_{p,\text{out}}$. However, when $R_{sig}$ is increased, $f_{p,\text{in}}$ is moved closer to $f_{p,\text{out}}$ and both poles contribute to the gain falloff.

## Example PS.10.1

### Determining the Loop Gain of a Feedback Amplifier

This example illustrates the use of SPICE to compute the loop gain $A\beta$. For this purpose, we shall use the shunt–series feedbck amplifier shown in Fig. B.33 (see also Problem 9.101).

To compute the loop gain, we set the input signal $V_S$ to zero, and we choose to break the feedback loop between the collector of $Q_1$ and the base of $Q_2$. However, in breaking the feedback loop, we must ensure that the following two conditions that existed prior to breaking the feedback loop do not change: (1) the dc bias situation and (2) the ac signal termination.

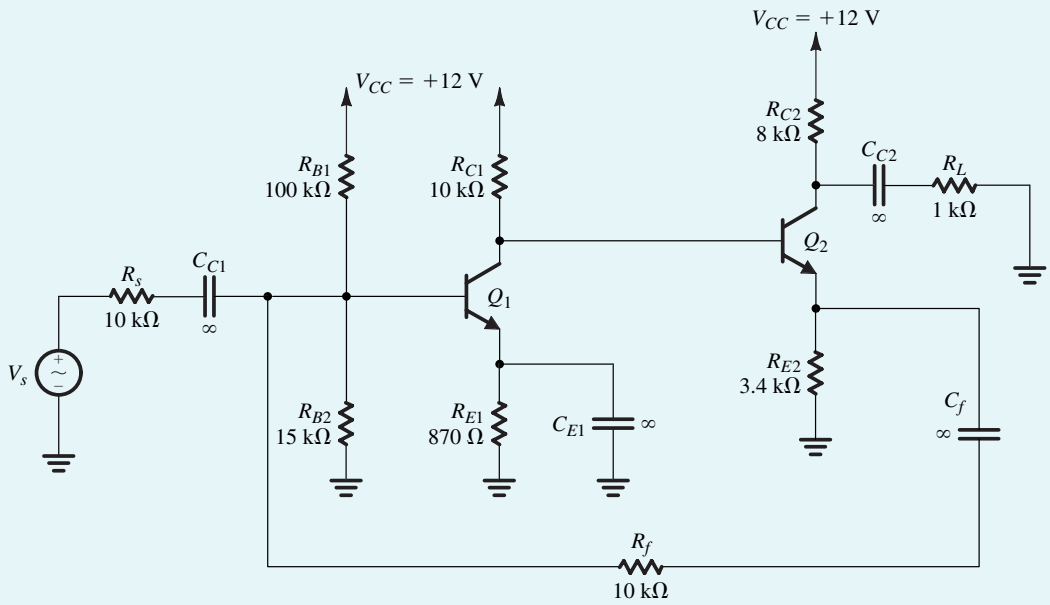



**Figure B.33** Circuit of the shunt–series feedback amplifier in Example PS.10.1.

To break the feedback loop without disturbing the dc bias conditions of the circuit, we insert a large inductor $L_{break}$, as shown in Fig. B.34(a). Using a value of, say, $L_{break}$ = 1 GH will ensure that the loop is opened for ac signals while keeping dc bias conditions unchanged.

To break the feedback loop without disturbing the signal termination conditions, we must load the loop output at the collector of $Q_1$ with a termination impedance $Z_t$ whose value is equal to the impedance seen looking into the loop input at the base of $Q_2$. Furthermore, to avoid disturbing the dc bias conditions, $Z_t$ must be connected to the collector of $Q_1$ via a large coupling capacitor. However, it is not always easy to determine the value of the termination impedance $Z_t$. So, we will describe two simulation methods to compute the loop gain without explicitly determining $Z_T$.

**Method 1** *Using the open-circuit and short-circuit transfer functions*

As described in Section 9.9, the loop gain can be expressed as

$$A\beta = -1 \Big/ \left(\frac{1}{T_{oc}} + \frac{1}{T_{sc}}\right)$$

where $T_{oc}$ is the open-circuit voltage transfer function and $T_{sc}$ is the short-circuit voltage transfer function.

The circuit for determining $T_{oc}$ is shown in Fig. B.34(b). Here, an ac test signal voltage $V_t$ is applied to the loop input at the base of $Q_2$ via a large coupling capacitor (having a value of, say, 1 kF) to avoid disturbing the dc bias conditions. Then,

$$T_{oc} = \frac{V_{oc}}{V_t}$$

where $V_{oc}$ is the ac open-circuit output voltage at the collector of $Q_1$.

In the circuit for determining $T_{sc}$ (Fig. B.34), an ac test signal current $I_t$ is applied to the loop input at the base of $Q_2$. Note that a coupling capacitor is not needed in this case because the ac current source appears as an open circuit at dc, and, hence, does not disturb the dc bias conditions.

The loop output at the collector of $Q_1$ is ac short-circuited to ground via a large capacitor $C_{to}$. Then,

$$T_{sc} = \frac{I_{sc}}{I_t}$$

where $I_{sc}$ is the ac short-circuit output current at the collector of $Q_1$.

**Method 2** *Using a replica circuit*

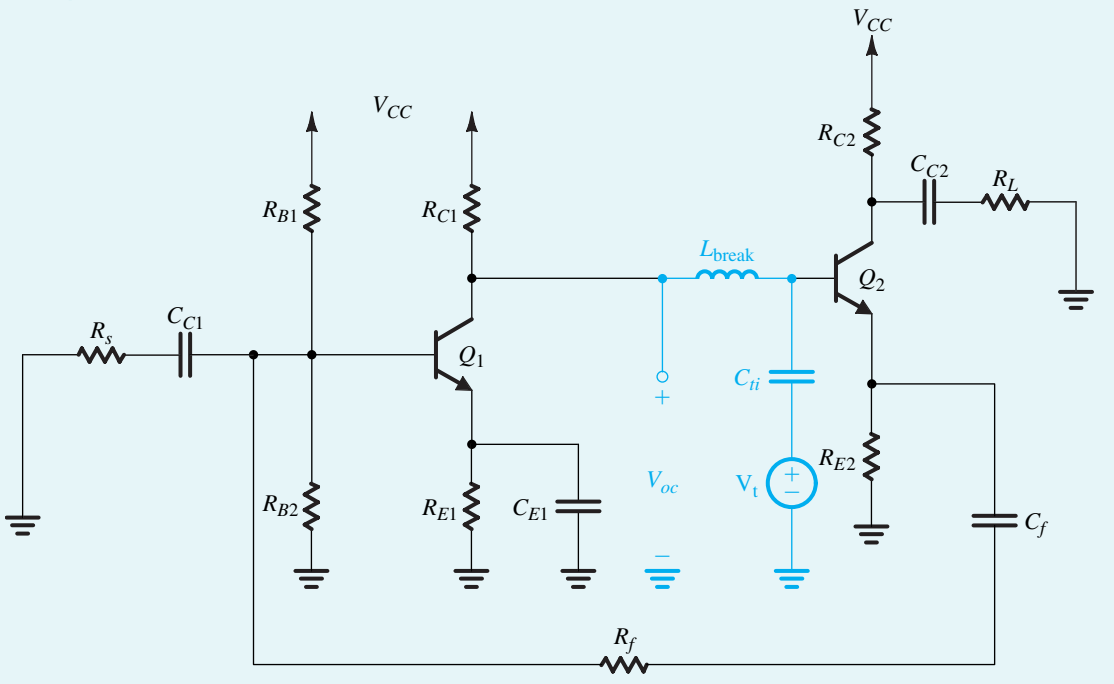
As shown in Fig. B.35, a replica of the feedback amplifier circuit can be simply used as a termination impedance. Here, the feedback loops of both the amplifier circuit and the replica circuit are broken using a large inductor $L_{break}$ to avoid disturbing the dc bias conditions. The loop output at the collector of $Q_1$ in the amplifier circuit is then connected to the loop input at the base of $Q_2$ in the replica circuit via a large coupling capacitor $C_{to}$ (again, to avoid disturbing the dc bias conditions). Thus, for ac signals, the loop output at the collector of $Q_1$ in the amplifier circuit sees an impedance equal to that seen before the feedback loop is broken. Accordingly, we have ensured that the conditions that existed in the amplifier circuit prior to breaking the loop have not changed.

Next, to determine the loop gain $A\beta$, we apply an ac test signal voltage $V_t$ via a large coupling capacitor $C_{ti}$ to the loop input at the base of $Q_2$ in the amplifier circuit. Then, as described in Section 9.9,

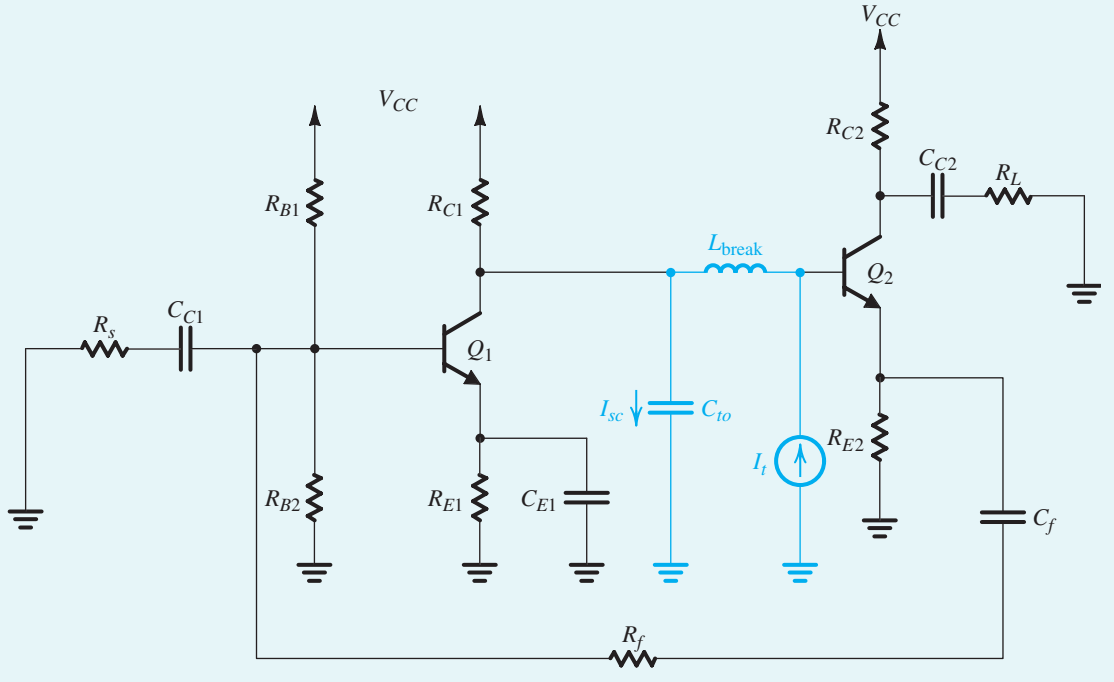
$$A\beta = -\frac{V_r}{V_t}$$

where $V_r$ is the ac returned signal at the loop output at the collector of $Q_1$ in the amplifier circuit.

Example PS.10.1 *continued*




(a)




(b)

**Figure B.34** Circuits for simulating **(a)** the open-circuit voltage transfer function $T_{oc}$ and **(b)** the short-circuit current transfer function $T_{sc}$ of the feedback amplifier in Fig. B.33 for the purpose of computing its loop gain.

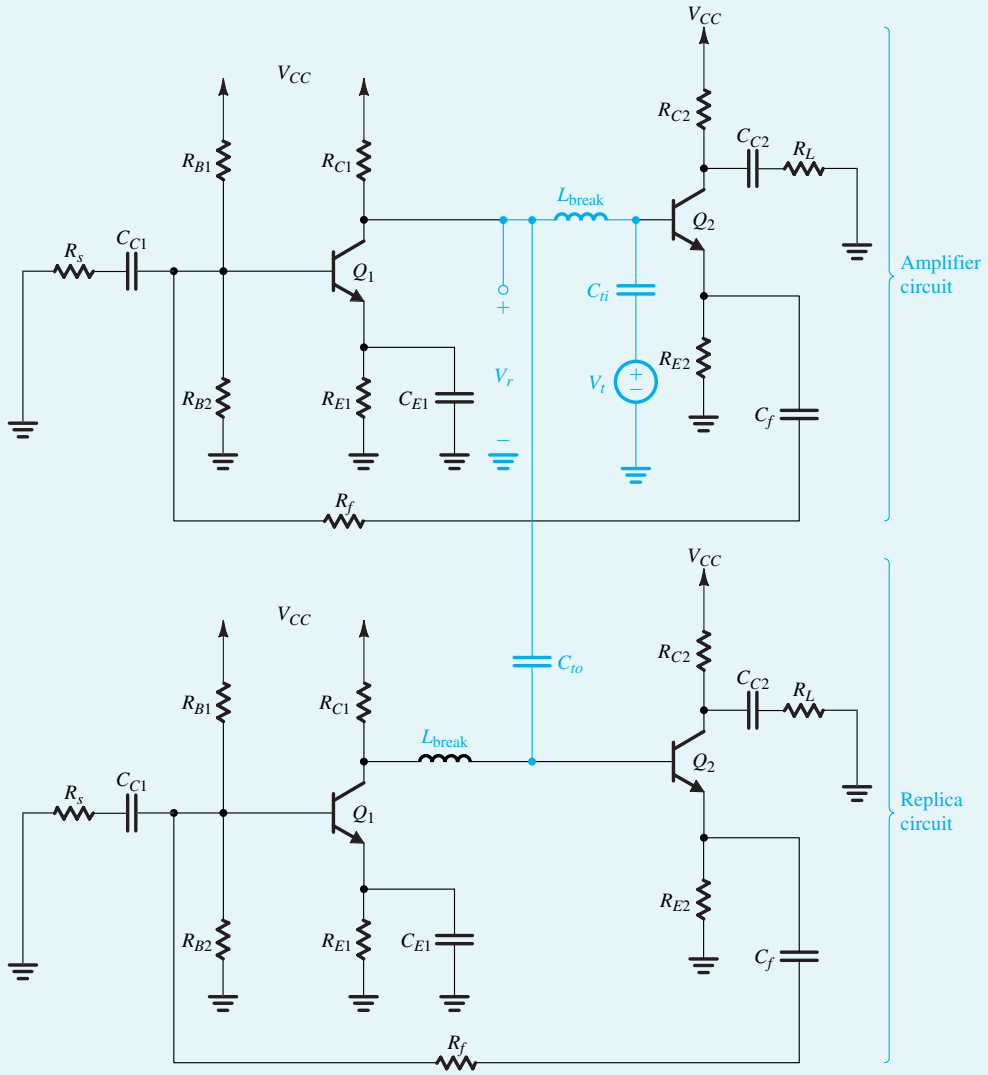



**Figure B.35** Circuit for simulating the loop gain of the feedback amplifier circuit in Fig. B.33 using the replica-circuit method.

To compute the loop gain $A\beta$ of the feedback amplifier circuit in Fig. B.33 using PSpice, we choose to simulate the circuit in Fig. B.35. In the PSpice simulations, we used part Q2N3904 (whose SPICE model is given in Table B.6) for the BJTs, and we set $L_{\text{break}}$ to be 1 GH and the coupling and bypass capacitors to be 1 kF. The magnitude and phase of $A\beta$ are plotted in Fig. B.36, from which we see that the feedback amplifier has a gain margin of 53.7 dB and a phase margin of 88.7°.

**Example PS.10.1** *continued*

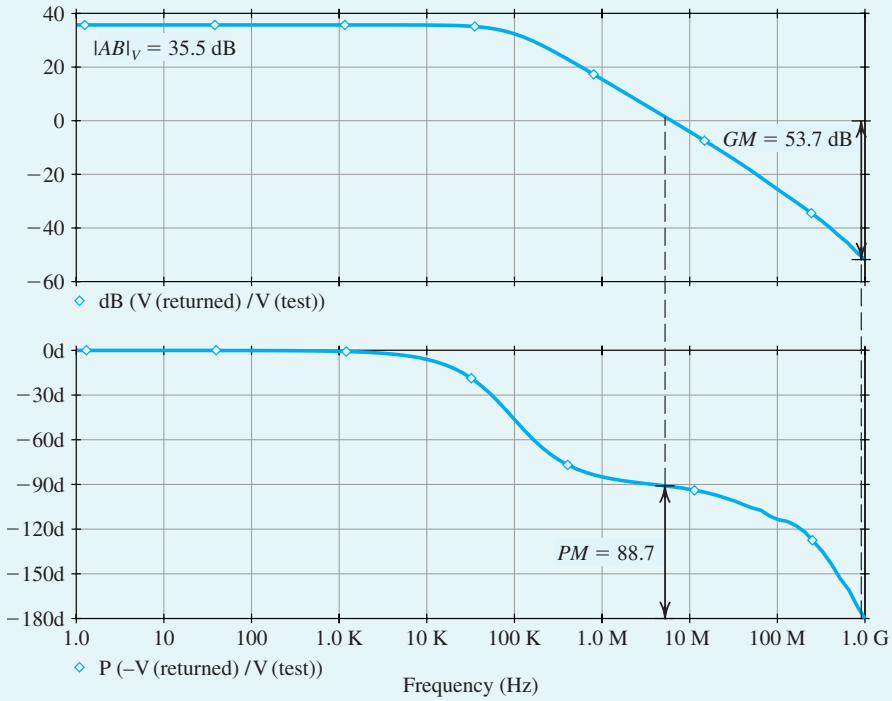



**Figure B.36** **(a)** Magnitude and **(b)** phase of the loop gain $A\beta$ of the feedback amplifier circuit in Fig. B.33.

## Example PS.11.1

### Class B BJT Output Stage

We investigate the operation of the class B output stage whose schematic capture is shown in Fig. B.37. For the power transistors, we use the discrete BJTs MJE243 and MJE253 (from ON Semiconductor),[13] which are rated for a maximum continuous collector current $I_{C\max} = 4$ A and a maximum collector–emitter voltage of $V_{CE\max} = 100$ V. To permit comparison with the hand analysis performed in Example 13.1, in the simulation, we use component and voltage values identical (or close) to those of the circuit designed in Example 13.1. Specifically, we use a load resistance of 8 Ω, an input sine-wave signal of 17.9-V peak and 1-kHz frequency, and 23-V power supplies. In PSpice, a transient-analysis simulation is performed over the interval 0 ms to 3 ms, and the waveforms of various node voltages and branch currents are plotted. In this example, Probe (the graphical interface of PSpice) is utilized to compute various power-dissipation values. Some of the resulting waveforms are displayed in Fig. B.38. The upper and middle graphs show the load voltage and current, respectively. The peak voltage amplitude is 16.9 V, and the peak current amplitude is 2.1 A. If one looks carefully, one can observe that both exhibit crossover distortion. The bottom

[13] In PSpice, we have created BJT parts for these power transistors based on the values of the SPICE model parameters available on the data sheets available from ON Semiconductor. Readers can find these parts (labeled QMJE243 and QMJE253) in the SEDRA.olb library, which is available on the CD accompanying this book.

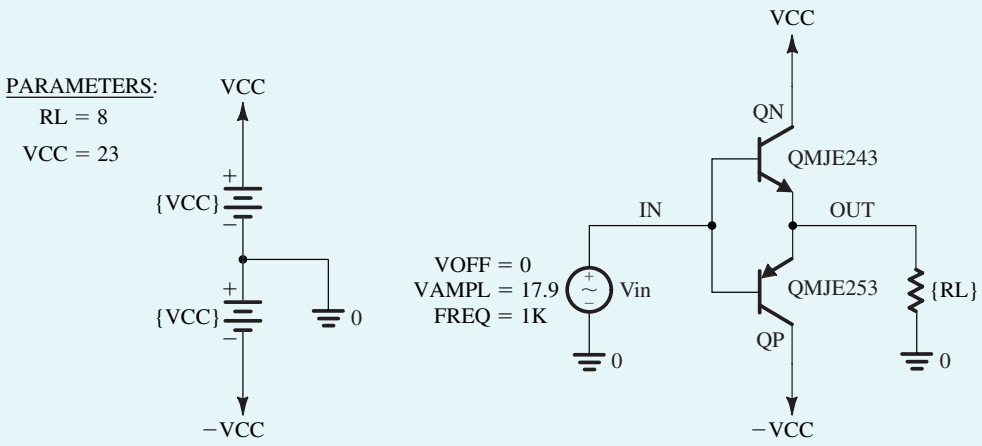



**Figure B.37** Capture schematic of the class B output stage in Example PS.11.1.

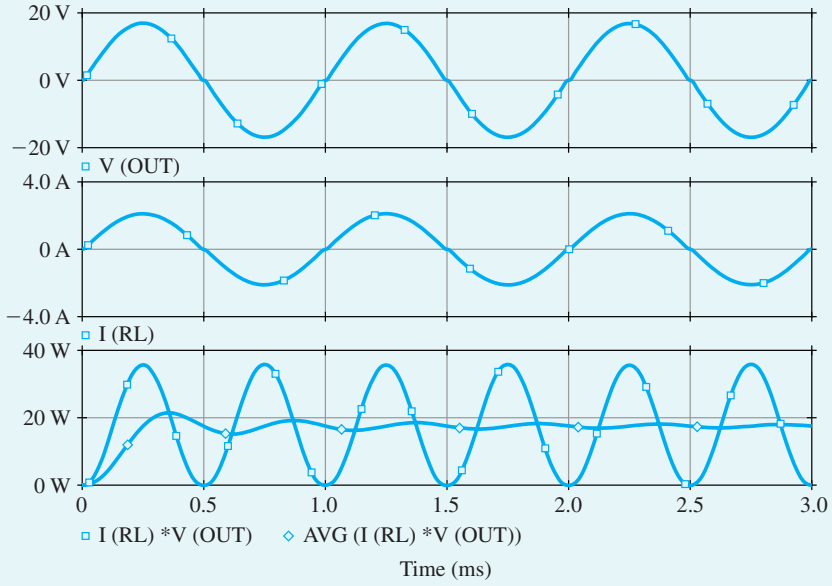



**Figure B.38** Several waveforms associated with the class B output stage (shown in Fig. B.37) when excited by a 17.9-V, 1-kHz sinusoidal signal. The upper graph displays the voltage across the load resistance, the middle graph displays the load current, and the lower graph displays the instantaneous and average power dissipated by the load.

graph displays the instantaneous and the average power dissipated in the load resistance as computed using Probe by multiplying the voltage and current values to obtain the instantaneous power, and taking a running average for the average load power $P_L$. The transient behavior of the average load power, which eventually settles into a quasiconstant steady state of about 17.6 W, is an artifact of the PSpice algorithm used to compute the running average of a waveform.

The upper two graphs of Fig. B.39 show the voltage and current waveforms, respectively, of the positive supply, $+V_{CC}$. The bottom graph shows the instantaneous and average power supplied by $+V_{CC}$.

**Example PS.11.1** *continued*

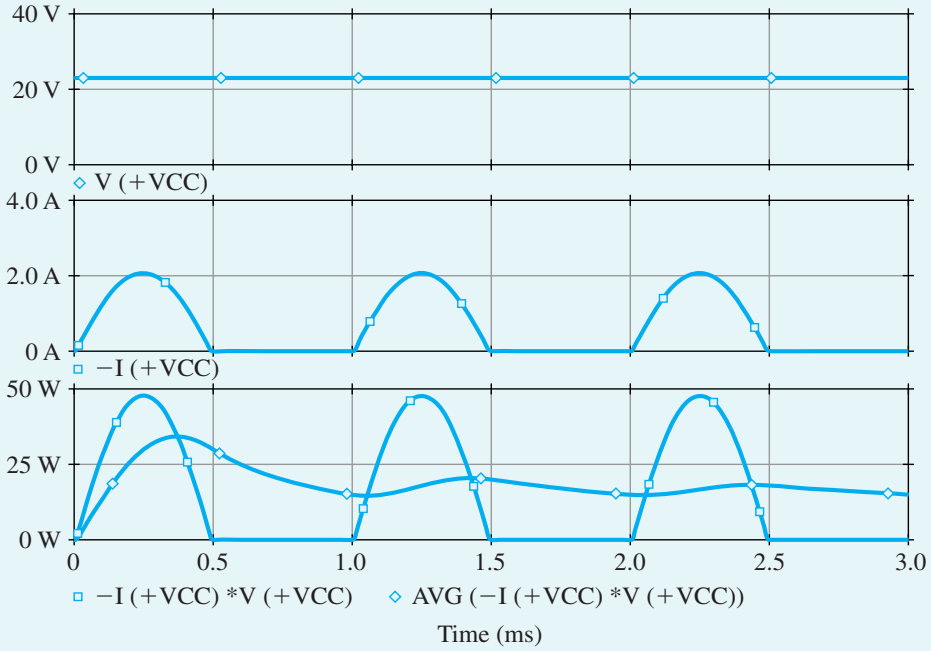



**Figure B.39** The voltage (upper graph), current (middle graph), and instantaneous and average power (bottom graph) supplied by the positive voltage supply ($+V_{CC}$) in the circuit of Fig. B.37.

Similar waveforms can be plotted for the negative supply, $-V_{CC}$. The average power provided by each supply is found to be about 15 W, for a total supply power $P_S$ of 30 W. Thus, the power-conversion efficiency can be computed to be

$$\eta = P_L/P_S = \frac{17.6}{30} \times 100\% = 58.6\%$$

Figure B.40 shows plots of the voltage, current, and power waveforms associated with transistor $Q_P$. Similar waveforms can be obtained for $Q_N$. As expected, the voltage waveform is a sinusoid, and the current waveform consists of half-sinusoids. The waveform of the instantaneous power, however, is rather unusual. It indicates the presence of some distortion as a result of driving the transistors rather hard. This can be verified by reducing the amplitude of the input signal. Specifically, when the amplitude is reduced to about 17 V, the "dip" in the power waveform vanishes. The average power dissipated in each of $Q_N$ and $Q_P$ can be computed by Probe and are found to be approximately 6 W.

Table B.11 provides a comparison of the results found from the PSpice simulation and the corresponding values obtained using hand analysis in Example 13.1. Observe that the two sets of results are quite close.

To investigate the crossover distortion further, we present in Fig. B.41 a plot of the voltage transfer characteristic (VTC) of the class B output stage. This plot is obtained through a dc-analysis simulation with $v_{IN}$ swept over the range –10 V to +10 V in 1.0-mV increments. Using Probe, we determine that the slope of the VTC is nearly unity and that the dead band extends from –0.60 V to +0.58 V. The effect of the crossover distortion can be quantified by performing a Fourier analysis on the output voltage waveform in PSpice. This analysis decomposes the waveform generated through a transient analysis into its

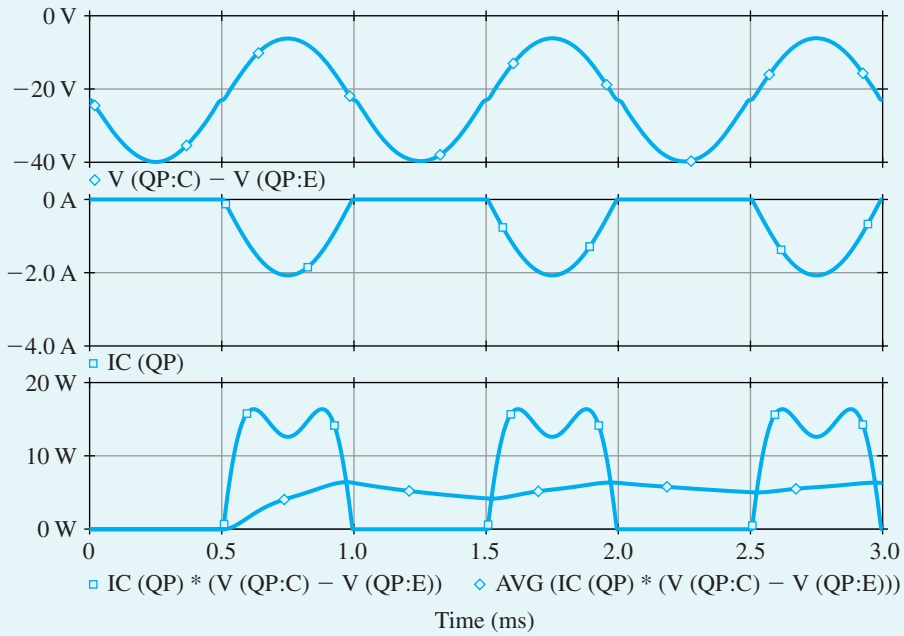



**Figure B.40** Waveforms of the voltage across, the current through, and the power dissipated in the *pnp* transistor $Q_P$ of the output stage shown in Fig. B.37.

**Table B.11** Various Power Terms Associated with the Class B Output Stage Shown in Fig. B.37 as Computed by Hand and by PSpice Analysis

| Power/Efficiency | Equation | Hand Analysis (Example PS.11.1) | PSpice | Error %[1] |
|---|---|---|---|---|
| $P_S$ | $\frac{2}{\pi}\frac{\hat{V}_o}{R_L}V_{CC}$ | 31.2 W | 30.0 W | 4 |
| $P_D$ | $\frac{2}{\pi}\frac{\hat{V}_o}{R_L}V_{CC}-\frac{1}{2}\frac{\hat{V}_o^2}{R_L}$ | 13.0 W | 12.4 W | 4.6 |
| $P_L$ | $\frac{1}{2}\frac{\hat{V}_o^2}{R_L}$ | 18.2 W | 17.6 W | 3.3 |
| $\eta$ | $\frac{P_L}{P_S}\times 100\%$ | 58.3% | 58.6% | –0.5 |

[1]Relative percentage error between the values predicted by hand and by PSpice.

Fourier-series components. Further, PSpice computes the total harmonic distortion (THD) of the output waveform. The results obtained from the simulation output file are shown on the next page.

These Fourier components are used to plot the line spectrum shown in Fig. B.42. We note that the output waveform is rather rich in odd harmonics and that the resulting THD is rather high (2.14%).

**Example PS.11.1** *continued*

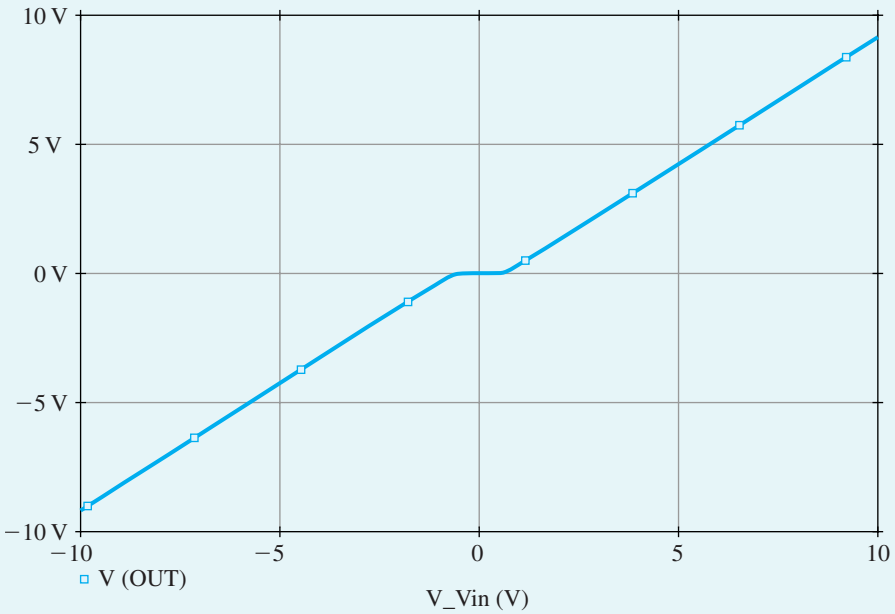



**Figure B.41** Transfer characteristic of the class B output stage of Fig. B.37.

```
FOURIER COMPONENTS OF TRANSIENT RESPONSE V(OUT)

DC COMPONENT = -1.525229E-02

HARMONIC    FREQUENCY     FOURIER     NORMALIZED     PHASE     NORMALIZED
   NO         (HZ)       COMPONENT    COMPONENT      (DEG)    PHASE (DEG)

    1     1.000E+03    1.674E+01    1.000E+00   -2.292E-03    0.000E+00
    2     2.000E+03    9.088E-03    5.428E-04    9.044E+01    9.044E+01
    3     3.000E+03    2.747E-01    1.641E-02   -1.799E+02   -1.799E+02
    4     4.000E+03    4.074E-03    2.433E-04    9.035E+01    9.036E+01
    5     5.000E+03    1.739E-01    1.039E-02   -1.799E+02   -1.799E+02
    6     6.000E+03    5.833E-04    3.484E-05    9.159E+01    9.161E+01
    7     7.000E+03    1.195E-01    7.140E-03   -1.800E+02   -1.799E+02
    8     8.000E+03    5.750E-04    3.435E-05    9.128E+01    9.129E+01
    9     9.000E+03    9.090E-02    5.429E-03   -1.800E+02   -1.799E+02
   10     1.000E+04    3.243E-04    1.937E-05    9.120E+01    9.122E+01

TOTAL HARMONIC DISTORTION = 2.140017E+00 PERCENT
```

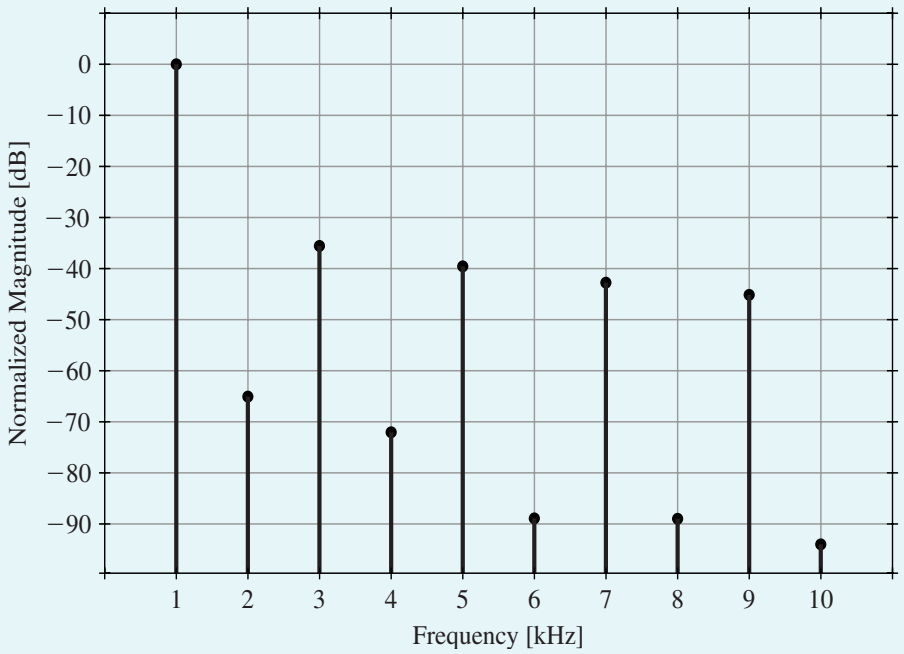



**Figure B.42** Fourier-series components of the output waveform of the class B output stage in Fig. B.37.

## Example PS.12.1

### Frequency Compensation of the Two-Stage CMOS Op Amp

In this example, we will use PSpice to aid in designing the frequency compensation of the two-stage CMOS circuit whose capture schematic is shown in Fig. B.43. PSpice will then be employed to determine the frequency response and the slew rate of the op amp. We will assume a 0.5-μm *n*-well CMOS technology for the MOSFETs and will use the SPICE level-1 model parameters listed in Table B.4. Observe that to eliminate the body effect and improve the matching between $M_1$ and $M_2$, the source terminals of the input PMOS transistors $M_1$ and $M_2$ are connected to their *n* well.

The op-amp circuit in Fig. B.43 is designed using a reference current $I_{REF} = 90\ \mu A$, a supply voltage $V_{DD} = 3.3$ V, and a load capacitor $C_L = 1$ pF. Unit-size transistors with $W/L = 1.25\ \mu m/0.6\ \mu m$ are used for both the NMOS and PMOS devices. The transistors are sized for an overdrive voltage $V_{OV} = 0.3$ V. The corresponding multiplicative factors are given in Fig. B.43.

In PSpice, the common-mode input voltage $V_{CM}$ of the op-amp circuit is set to $V_{DD}/2 = 1.65$ V. A bias-point simulation is performed to determine the dc operating point. Using the values found in the simulation output file for the small-signal parameters of the MOSFETs, we obtain[14]

[14]Recall that $G_{m1}$ and $G_{m2}$ are the transconductances of, respectively, the first and second stages of the op amp. Capacitors $C_1$ and $C_2$ represent the total capacitance to ground at the output nodes of, respectively, the first and second stages of the op amp.

**Example PS.12.1** *continued*

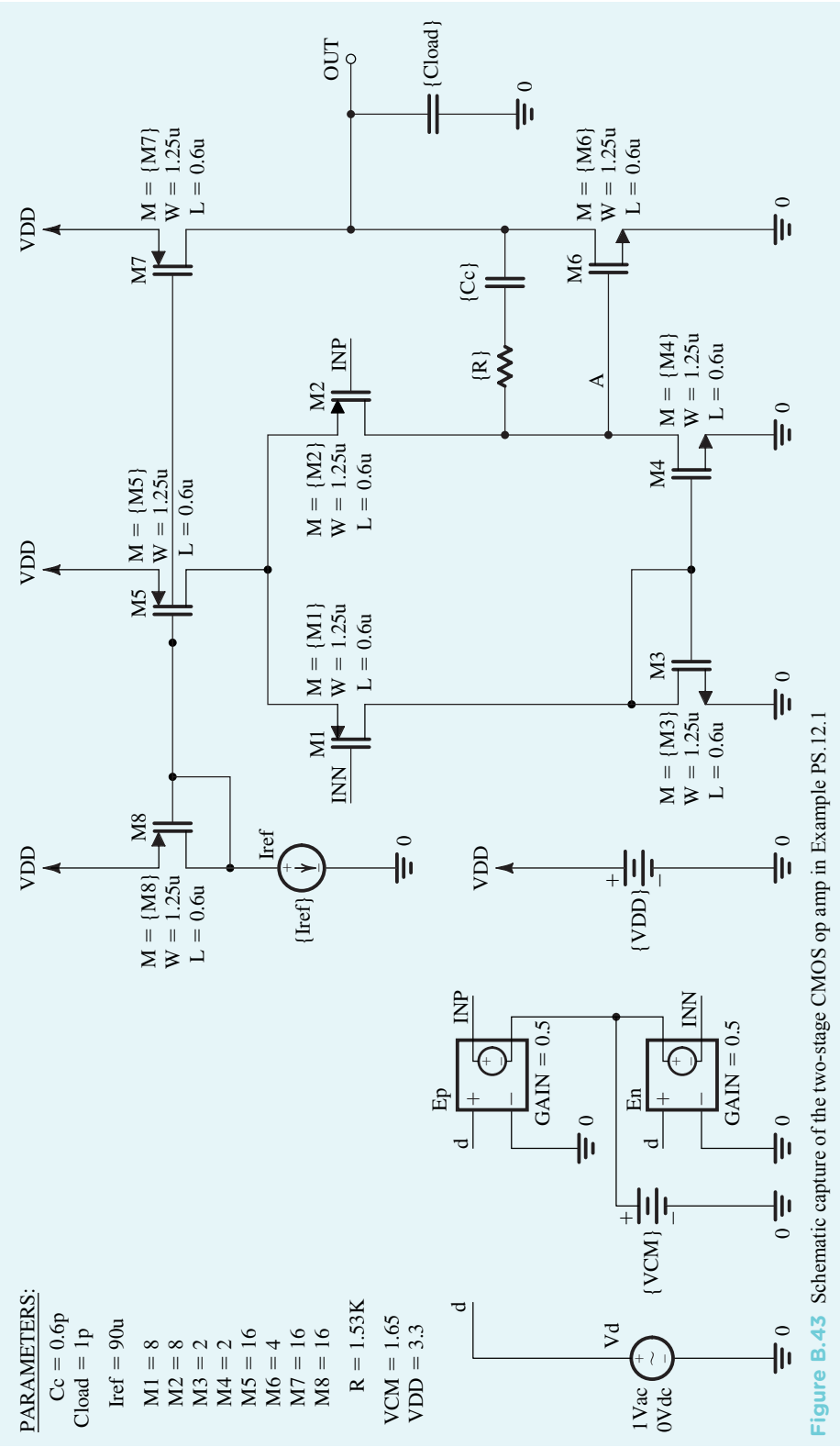



**Figure B.43** Schematic capture of the two-stage CMOS op amp in Example PS.12.1

$$G_{m1} = 0.333 \text{ mA/V}$$
$$G_{m2} = 0.650 \text{ mA/V}$$
$$C_1 = 26.5 \text{ fF}$$
$$C_2 = 1.04 \text{ pF}$$

using Eqs. (10.7), (10.14), (10.25), and (10.26), respectively. Then, using Eq. (10.28), the frequency of the second, nondominant, pole can be found as

$$f_{P2} \simeq \frac{G_{m2}}{2\pi C_2} = 97.2 \text{ MHz}$$

In order to place the transmission zero, given by Eq. (10.38), at infinite frequency, we select

$$R = \frac{1}{G_{m2}} = 1.53 \text{ k}\Omega$$

Now, using Eq. (10.38), the phase margin of the op amp can be expressed as

$$\text{PM} = 90° - \tan^{-1}\left(\frac{f_t}{f_{P2}}\right) \tag{B.44}$$

where $f_t$ is the unity-gain frequency, given in Eq. (10.31),

$$f_t = \frac{G_{m1}}{2\pi C_C} \tag{B.45}$$

Using Eqs. (B.44) and (B.45), we determine that compensation capacitors of $C_C = 0.78$ pF and $C_C = 2$ pF are required to achieve phase margins of PM = 55° and PM = 75°, respectively.

Next, an ac-analysis simulation is performed in PSpice to compute the frequency response of the op amp and to verify the foregoing design values. It was found that with $R = 1.53$ kΩ, we needed $C_C = 0.6$ pF and $C_C = 1.8$ pF to set PM = 55° and PM = 75°, respectively. We note that these values are reasonably close to those predicted by hand analysis. The corresponding frequency responses for the compensated op amp are plotted in Figs. B.44 and B.45. For comparison, we also show the frequency response of the uncompensated op amp ($C_C = 0$). Observe that the unity gain frequency $f_t$ drops from 70.2 MHz to 26.4 MHz as $C_C$ is increased to improve PM (as anticipated from Eq. B.45).

Rather than increasing the compensation capacitor $C_C$, the value of the series resistor $R$ can be increased to improve the phase margin PM: For a given $C_C$, increasing $R$ above $1/G_{m2}$ places the transmission zero at a negative real-axis location (Eq. 10.38), where the phase it introduces *adds* to the phase margin. Thus, PM can be improved without affecting $f_t$. To verify this point, we set $C_C$ to 0.6 pF and simulate the op-amp circuit in PSpice for the cases of $R = 1.53$ kΩ and $R = 3.2$ kΩ. The corresponding frequency response is plotted in Fig. B.46. Observe how $f_t$ is approximately independent of $R$. However, by increasing $R$, PM is improved from 55° to 75°.

Increasing the PM is desirable because it reduces the overshoot in the step response of the op amp. To verify this point, we simulate in PSpice the step response of the op amp for PM = 55° and PM = 75°. To do that, we connect the op amp in a unity-gain configuration, apply a small (10-mV) pulse signal at the input with very short (1-ps) rise and fall times to emulate a step input, perform a transient-analysis simulation, and plot the output voltage as shown in Fig. B.47. Observe that the overshoot in the step response drops from 15% to 1.4% when the phase margin is increased from 55° to 75°.

We conclude this example by computing $SR$, the slew rate of the op amp. From Eq. (10.40),

$$SR = 2\pi f_t V_{OV} = \frac{G_{m1}}{C_C} V_{OV} = 166.5 \text{ V/}\mu\text{s}$$

**Example PS.12.1** *continued*

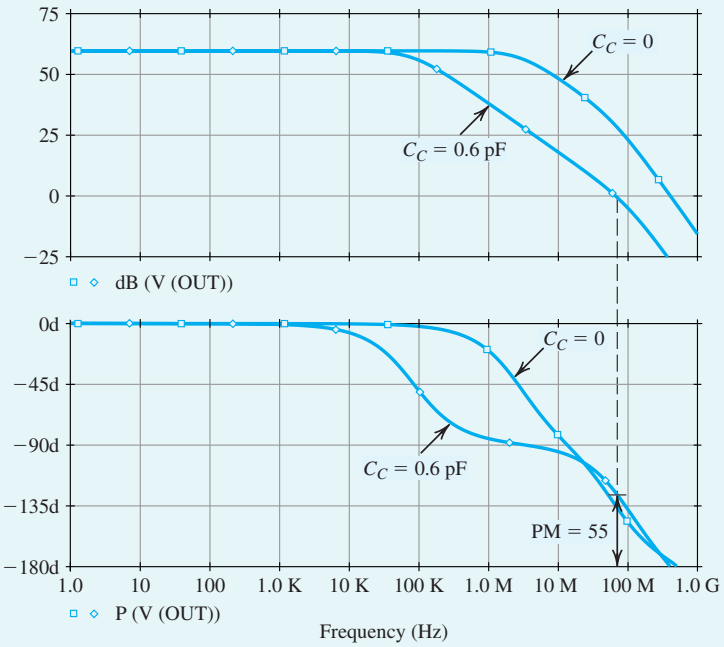



**Figure B.44** Magnitude and phase response of the op-amp circuit in Fig. B.43: $R = 1.53$ kΩ, $C_C = 0$ (no frequency compensation), and $C_C = 0.6$ pF (PM = 55°).

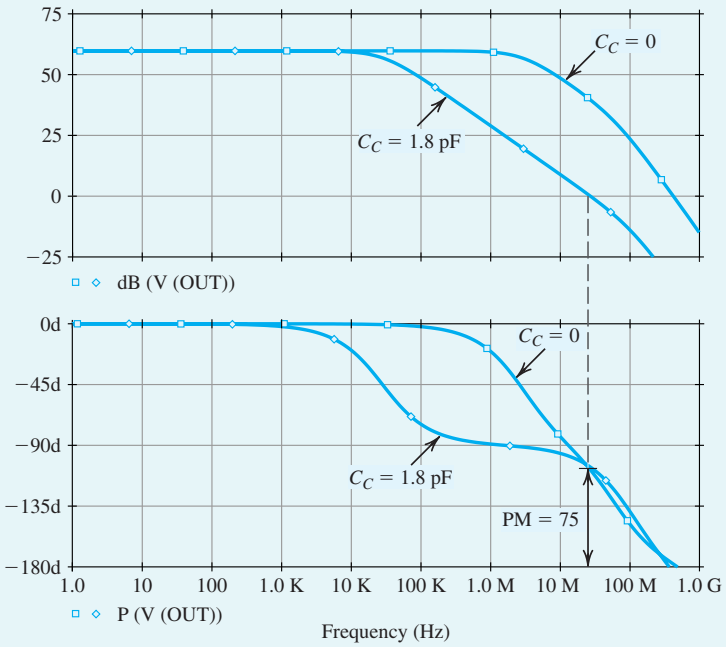



**Figure B.45** Magnitude and phase response of the op-amp circuit in Fig. B.43: $R = 1.53$ kΩ, $C_C = 0$ (no frequency compensation), and $C_C = 1.8$ pF (PM = 75°).

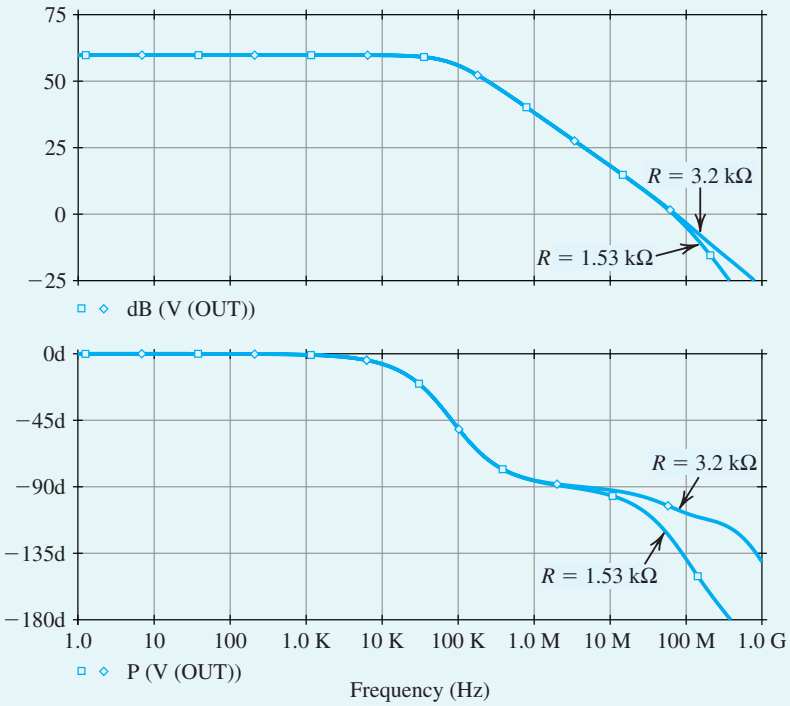



**Figure B.46** Magnitude and phase response of the op-amp circuit in Fig. B.43: $C_C = 0.6$ pF, $R = 1.53$ kΩ (PM = 55°), and $R = 3.2$ kΩ (PM = 75°).

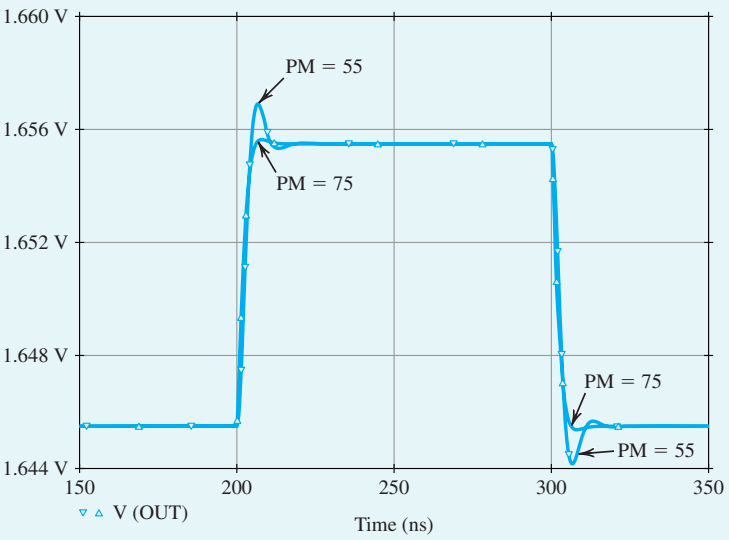



**Figure B.47** Small-signal step response (for a 10-mV step input) of the op-amp circuit in Fig. B.43 connected in a unity-gain configuration: PM = 55° ($C_C = 0.6$ pF, $R = 1.53$ kΩ) and PM = 75° ($C_C = 0.6$ pF, $R = 3.2$ kΩ).

when $C_C = 0.6$ pF. Next, to determine *SR* using PSpice (see Example PS.2.2), we again connect the op amp in a unity-gain configuration and perform a transient-analysis simulation. However, we now apply

**Example PS.12.1** *continued*

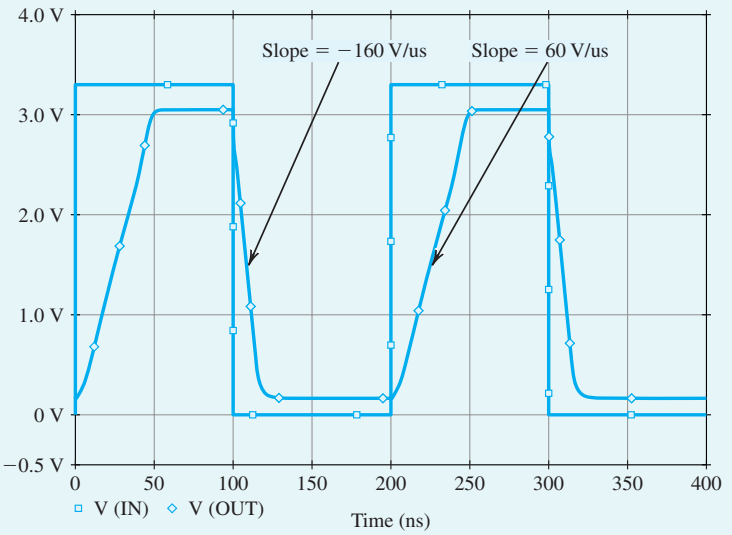



**Figure B.48** Large-signal step response (for a 3.3-V step-input) of the op-amp circuit in Fig. B.43 connected in a unity-gain configuration. The slope of the rising and falling edges of the output waveform correspond to the slew rate of the op amp.

a large pulse signal (3.3 V) at the input to cause slew-rate limiting at the output. The corresponding output-voltage waveform is plotted in Fig. B.48. The slope of the slew-rate-limited output waveform corresponds to the slew rate of the op amp and is found to be $SR = 160$ V/μs and 60 V/μs for the negative- and positive-going output, respectively. These results, with the unequal values of $SR$ in the two directions, differ from those predicted by the simple model for the slew-rate limiting of the two-stage op-amp circuit (Section 10.1.6). The difference can perhaps be said to be a result of transistor $M_4$ entering the triode region and its output current (which is sourced through $C_C$) being correspondingly reduced. Of course, the availability of PSpice should enable the reader to explore this point further.

## Example PS.13.1

### Operation of the CMOS Inverter

In this example, we will use PSpice to simulate the CMOS inverter whose schematic capture is shown in Fig, B.49. We will assume a 0.5-μm CMOS technology for the MOSFETs and use parts NMOS0P5 and PMOS0P5 whose level-1 model parameters are listed in Table B.4. In addition to the channel length $L$ and the channel width $W$, we have used the multiplicative factor $m$ to specify the dimensions of the MOSFETs. The MOSFET parameter $m$, whose default value is 1, is used in SPICE to specify the number of unit-size MOSFETs connected in parallel (see Fig. B.24). In our simulations, we will use unit-size transistors with $L = 0.5$ μm and $W = 1.25$ μm. We will simulate the inverter for two cases: (a) setting $m_p/m_n = 1$ so that the NMOS and PMOS transistors have equal widths, and (b) setting $m_p/m_n = \mu_n/\mu_p = 4$ so that the PMOS transistor is four times wider than the NMOS transistor (to compensate for the lower mobility in $p$-channel devices as compared with $n$-channel ones). Here, $m_n$ and $m_p$ are the multiplicative factors of, respectively, the NMOS and PMOS transistors of the inverter.

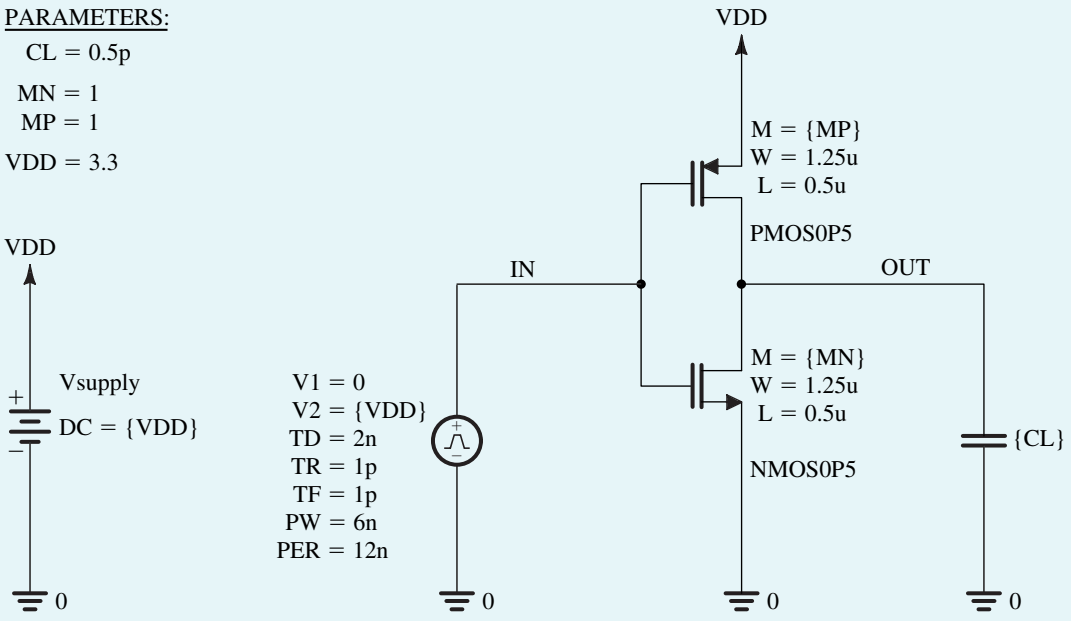



**Figure B.49** Schematic capture of the CMOS inverter in Example PS.13.1.

To compute both the voltage transfer characteristic (VTC) of the inverter and its supply current at various values of the input voltage $V_{in}$, we apply a dc voltage source at the input and perform a dc analysis with $V_{in}$ swept over the range of 0 to $V_{DD}$. The resulting VTC is plotted in Fig. B.50. Note that the slope of the VTC in the switching region (where both the NMOS and PMOS devices are in saturation) is not infinite as predicted from the simple theory presented in Chapter 14 (Section 14.2, Fig. 14.20). Rather, the nonzero value of $\lambda$ causes the inverter gain to be finite. Using the derivative feature of Probe, we can find the two points on the VTC at which the inverter gain is unity (i.e., the VTC slope is −1 V/V) and, hence, determine $V_{IL}$ and $V_{IH}$. Using the results given in Fig. B.50, the corresponding noise margins are $NM_L = NM_H = 1.34$ V for the inverter with $m_p/m_n = 4$, while $NM_L = 0.975$ V and $NM_H = 1.74$ V for the inverter with $m_p/m_n = 1$. Observe that these results correlate reasonably well with the values obtained using the approximate formula in Eq. (14.58). Furthermore, note that with $m_p/m_n = \mu_n/\mu_p = 4$, the NMOS and PMOS devices are closely matched and, hence, the two noise margins are equal.

The threshold voltage $V_M$ of the CMOS inverter is defined as the input voltage $v_{IN}$ that results in an identical output voltage $v_{OUT}$, that is,

$$V_M = v_{IN}\big|_{v_{OUT} = v_{IN}} \tag{B.46}$$

Thus, as shown in Fig. B.51, $V_M$ is the intersection of the VTC, with the straight line corresponding to $v_{OUT} = v_{IN}$ (this line can be simply generated in Probe by plotting $v_{IN}$ versus $v_{OUT}$, as shown in Fig. B.51). Note that $V_M \simeq (V_{DD}/2)$ for the inverter with $m_p/m_n = 4$. Furthermore, decreasing $m_p/m_n$ decreases $V_M$. Figure B.51 also shows the inverter supply current versus $v_{IN}$. Observe that the location of the supply-current peak shifts with the threshold voltage.

**Example PS.13.1** *continued*

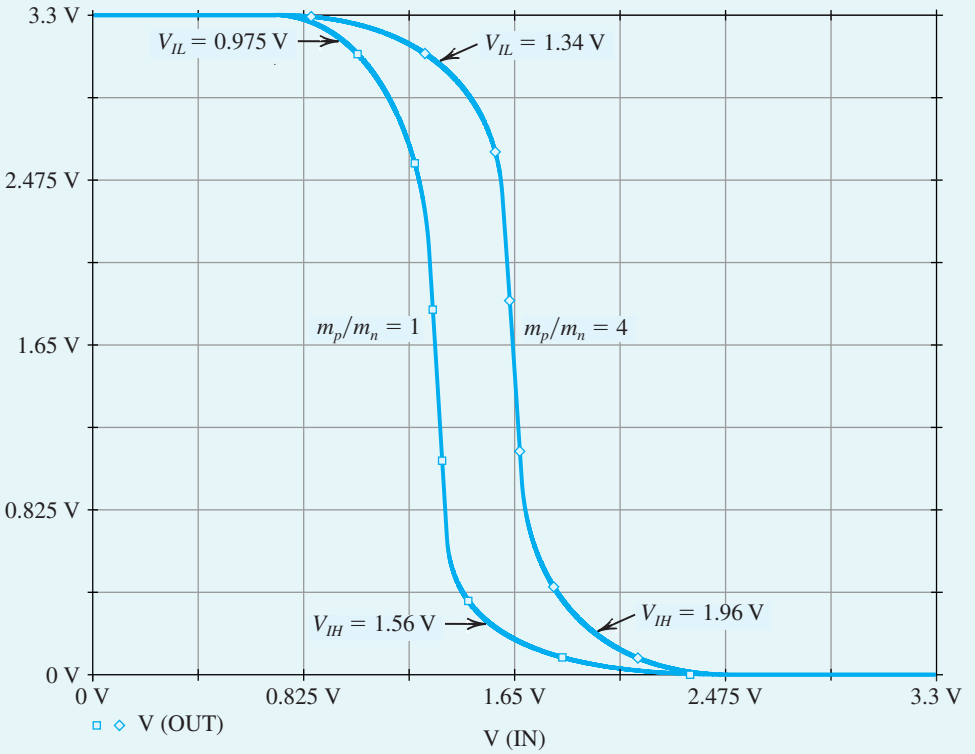
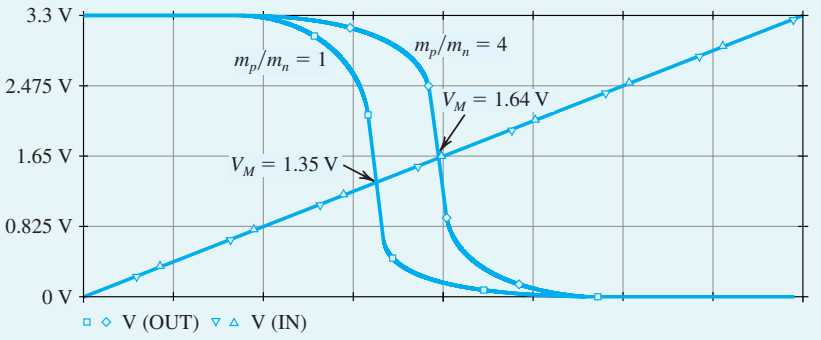
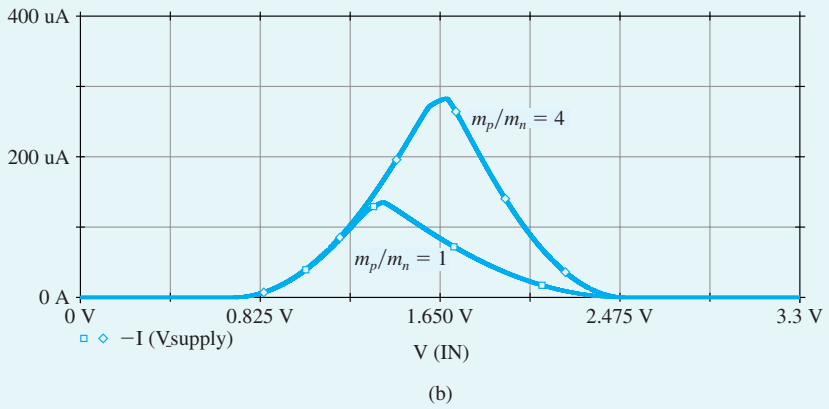



**Figure B.50** Input–output voltage transfer characteristic (VTC) of the CMOS inverter in Example PS.13.1 with $m_p/m_n = 1$ and $m_p/m_n = 4$.




(a)

**Figure B.51** **(a)** Output voltage and **(b)** supply current versus input voltage for the CMOS inverter in Example PS.13.1 with $m_p/m_n = 1$ and $m_p/m_n = 4$.




(b)

**Figure B.51** (*Contd.*)

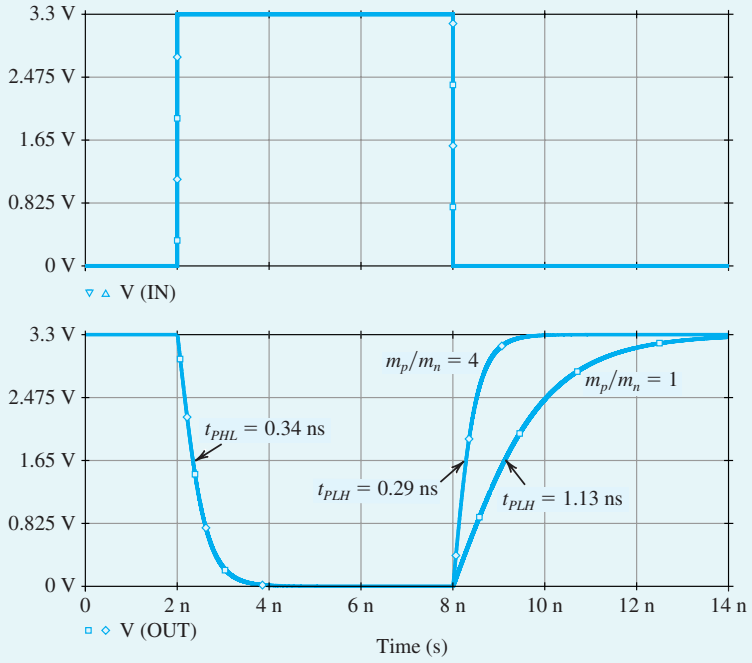



**Figure B.52** Transient response of the CMOS inverter in Example PS.13.1 with $m_p/m_n = 1$ and $m_p/m_n = 4$.

To investigate the dynamic operation of the inverter with PSpice, we apply a pulse signal at the input (Fig. B.49), perform a transient analysis, and plot the input and output waveforms as shown in Fig. B.52. The rise and fall times of the pulse source are chosen to be very short. Note that increasing $m_p/m_n$ from 1 to 4 decreases $t_{PLH}$ (from 1.13 ns to 0.29 ns) because of the increased current available to charge $C_L$, with only a minor increase in $t_{PHL}$ (from 0.33 ns to 0.34 ns). The two propagation delays, $t_{PLH}$ and $t_{PHL}$, are not exactly equal when $m_p/m_n = 4$, because the NMOS and PMOS transistors are still not perfectly matched (e.g., $V_{tn} \neq |V_{tp}|$).

## Example PS.14.1

### Static and Dynamic Operation of an ECL Gate

In this example, we use PSpice to investigate the static and dynamic operation of the ECL gate (studied in Section 15.4) whose schematic capture is shown in Fig. B.53.

Having no access to the actual values for the SPICE model parameters of the BJTs utilized in commercially available ECL, we have selected parameter values representative of the technology utilized that, from our experience, would lead to reasonable agreement between simulation results and the measured

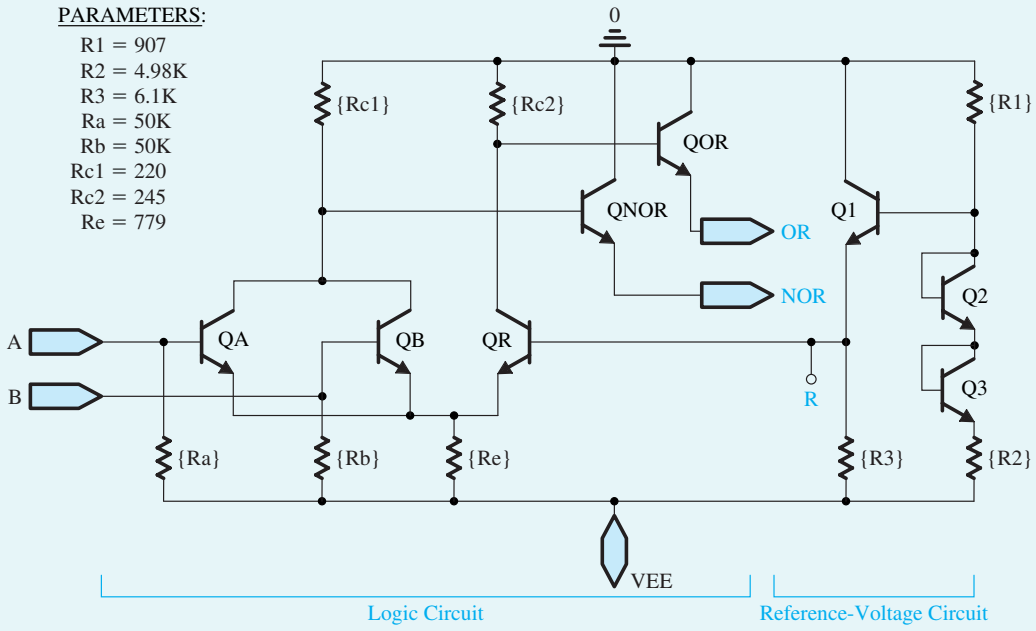



**Figure B.53** Schematic capture of the two-input ECL gate for Example PS.14.1

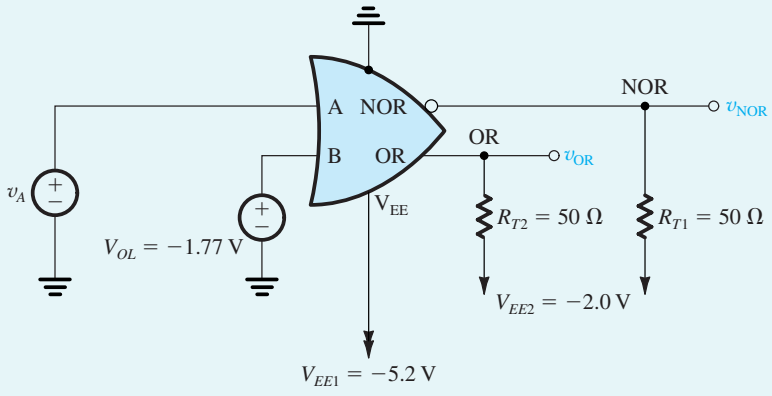



**Figure B.54** Circuit arrangement for computing the voltage transfer characteristics of the ECL gate in Fig. B.53.

performance data supplied by the manufacturer. It should be noted that this problem would not be encountered by an IC designer using SPICE as an aid; presumably, the designer would have full access to the proprietary process parameters and the corresponding device model parameters. In any case, for the simulations we conducted, we have utilized the following BJT model parameter values[15]: $I_S = 0.26$ fA, $\beta_F = 100$; $\beta_R = 1$, $\tau_F = 0.1$ ns, $C_{je} = 1$ pF, $C_{jc} = C_\mu = 1.5$ pF, and $|V_A| = 100$ V.

We use the circuit arrangement of Fig. B.54 to compute the voltage transfer characteristics of the ECL gate, that is, $v_{OR}$ and $v_{NOR}$ versus $v_A$, where $v_A$ is the input voltage at terminal A. For this investigation, the other input is deactivated by applying a voltage $v_B = V_{OL} = -1.77$ V. In PSpice, we perform a dc-analysis simulation with $v_A$ swept over the range –2 V to 0 V in 10-mV increments and plot $v_{OR}$ and $v_{NOR}$ versus $v_A$. The simulation results are shown in Fig. B.55. We immediately recognize the VTCs as those we have seen and (partially) verified by manual analysis in Section 15.4. The two transfer curves are symmetrical about an input voltage of –1.32 V. PSpice also determined that the voltage $V_R$ at the base of the reference transistor $Q_R$ has exactly this value (–1.32 V), which is also identical to the value we determined by hand analysis of the reference-voltage circuit.

Utilizing Probe (the graphical interface of PSpice), one can determine the values of the important parameters of the VTC, as follows:

OR output: $V_{OL} = -1.77$ V, $V_{OH} = -0.88$ V, $V_{IL} = -1.41$ V, and $V_{IH} = -1.22$ V; thus, $NM_H = 0.34$ V and $NM_L = 0.36$ V

NOR output: $V_{OL} = -1.78$ V, $V_{OH} = -0.88$ V, $V_{IL} = -1.41$ V, and $V_{IH} = -1.22$ V; thus, $NM_H = 0.34$ V and $NM_L = 0.37$ V

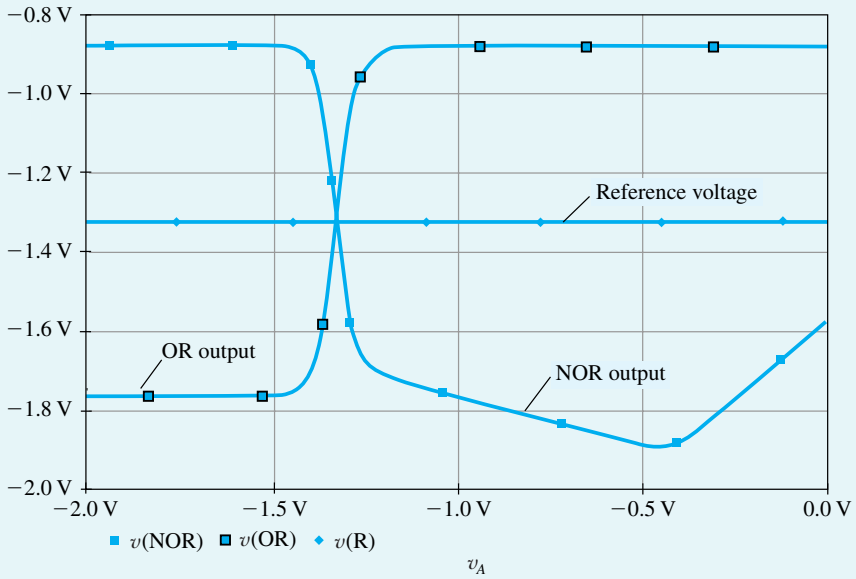


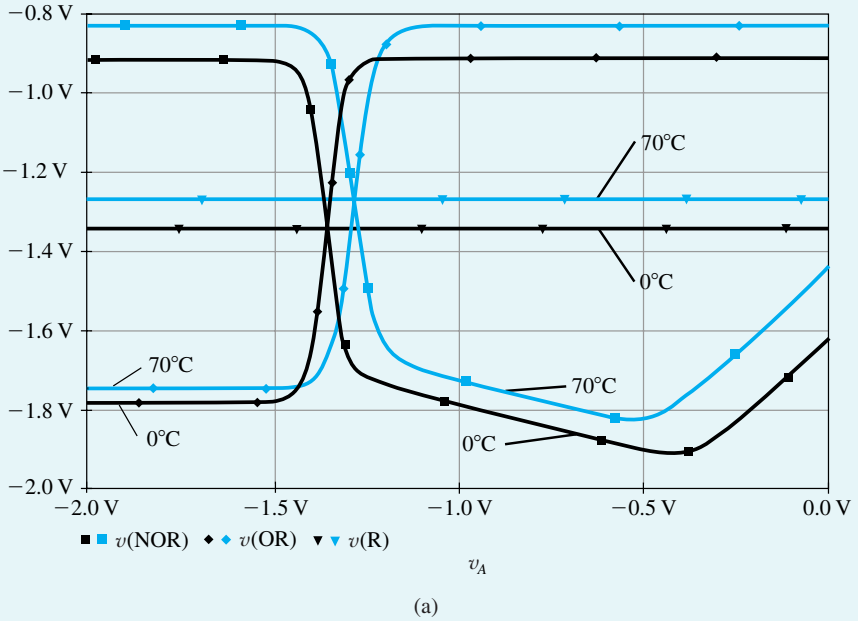

**Figure B.55** Voltage transfer characteristics of the OR and NOR outputs (see Fig. B.54) for the ECL gate shown in Fig. B.53. Also indicated is the reference voltage, $V_R = -1.32$ V.

[15]In PSpice, we have created a part called QECL based on these BJT model parameter values. Readers can find this part in the SEDRA.olb library, which is available on the CD accompanying this book.

**Example PS.14.1** *continued*

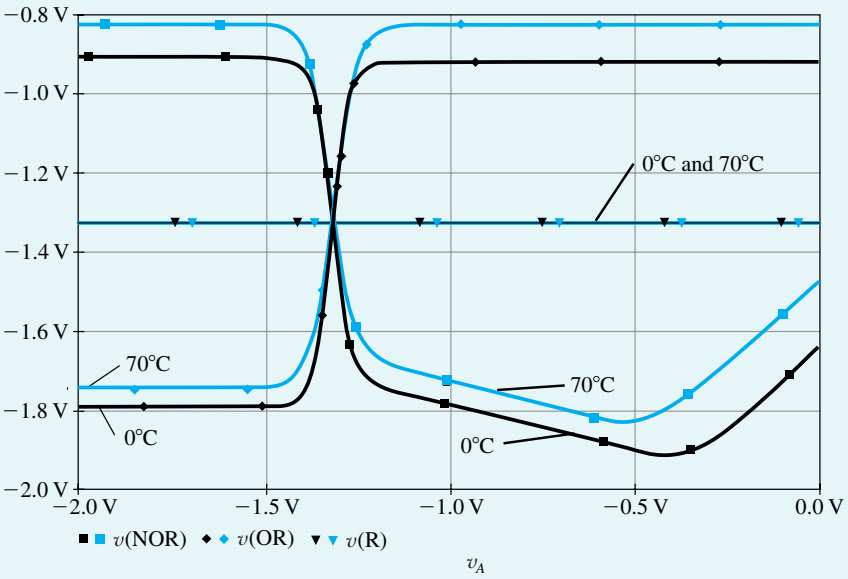
These values are remarkably close to those found by pencil-and-paper analysis in Section 15.4.

We next use PSpice to investigate the temperature dependence of the transfer characteristics. The reader will recall that in Section 15.4, we discussed this point at some length and carried out a hand analysis in Example 15.7. Here, we use PSpice to find the voltage transfer characteristics at two temperatures, 0°C and 70°C (the VTCs shown in Fig. B.55 were computed at 27°C) for two different cases: the first case with $V_R$ generated as in Fig. B.53, and the second with the reference-voltage circuit eliminated and a constant, temperature-independent reference voltage of −1.32 V applied to the base of $Q_R$. The simulation results are displayed in Fig. B.56. Figure B.56(a) shows plots of the transfer characteristics for the case in which the reference circuit is utilized, and Fig. B.56(b) shows plots for the case in which a constant reference voltage is employed. Figure B.56(a) indicates that as the temperature is varied and $V_R$ changes, the values of $V_{OH}$ and $V_{OL}$ also change but remain centered on $V_R$. In other words, the low and high noise margins remain nearly equal. As mentioned in Section 15.4 and demonstrated in the analysis of Example 15.4, this is the basic idea behind making $V_R$ temperature dependent. When $V_R$ is not temperature dependent, the symmetry of $V_{OL}$ and $V_{OH}$ around $V_R$ is no longer maintained, as demonstrated in Fig. B.56(b). Finally, we show some of the values obtained in Table B.12. Observe that for the temperature-compensated case, the average value of $V_{OL}$ and $V_{OH}$ remains very close to $V_R$. The reader is encouraged to compare these results to those obtained in Example 15.4.




(a)

**Figure B.56** Comparing the voltage transfer characteristics of the OR and NOR outputs (see Fig. B.54) of the ECL gate shown in Fig. B.53, with the reference voltage $V_R$ generated using: **(a)** the temperature-compensated bias network of Fig. B.53; **(b)** a temperature-independent voltage source.




(b)

**Figure B.56** (*Contd.*).

**Table B.12** PSpice-Computed Parameter Values of the ECL Gate, With and Without Temperature Compensation, at Two Different Temperatures

| | | Temperature-Compensated | | Not Temperature-Compensated | |
|---|---|---|---|---|---|
| Temperature | Parameter | OR | NOR | OR | NOR |
| 0°C | $V_{OL}$ | −1.779 V | −1.799 V | −1.786 V | −1.799 V |
| | $V_{OH}$ | −0.9142 V | −0.9092 V | −0.9142 V | −0.9092 V |
| | $V_{\text{avg}} = \frac{V_{OL} + V_{OH}}{2}$ | −1.3466 V | −1.3541 V | −1.3501 V | −1.3541 V |
| | $V_R$ | −1.345 V | −1.345 V | −1.32 V | −1.32 V |
| | $\lvert V_{\text{avg}} - V_R \rvert$ | 1.6 mV | 9.1 mV | 30.1 mV | 34.1 mV |
| 70°C | $V_{OL}$ | −1.742 V | −1.759 V | −1.729 V | −1.759 V |
| | $V_{OH}$ | −0.8338 V | −0.8285 V | −0.8338 V | −0.8285 V |
| | $V_{\text{avg}} = \frac{V_{OL} + V_{OH}}{2}$ | −1.288 V | −1.294 V | −1.2814 V | −1.294 V |
| | $V_R$ | −1.271 V | −1.271 V | −1.32 V | −1.32 V |
| | $\lvert V_{\text{avg}} - V_R \rvert$ | 17 mV | 23 mV | 38 mV | 26.2 mV |

The dynamic operation of the ECL gate is investigated using the arrangement of Fig. B.57. Here, two gates are connected by a 1.5-m coaxial cable having a characteristic impedance ($Z_0$) of 50 Ω. The manufacturer specifies that signals propagate along this cable (when it is *properly terminated*) at about half the speed of light, or 15 cm/ns. Thus we would expect the 1.5-m cable we are using to introduce a delay $t_d$ of 10 ns. Observe that in this circuit (Fig. B.57), resistor $R_{T1}$ provides the proper cable termination. The cable is

**Example PS.14.1** *continued*

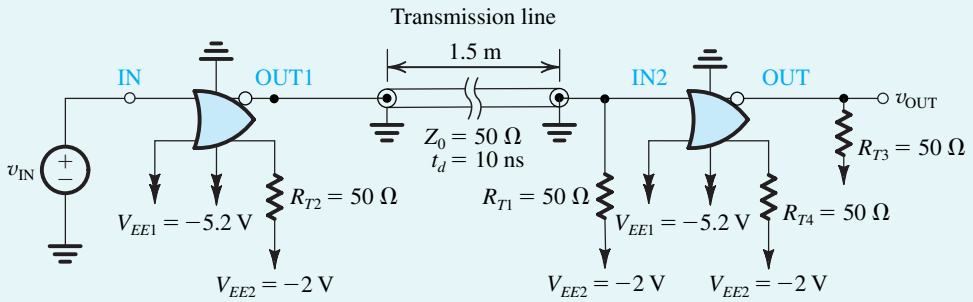



**Figure B.57** Circuit arrangement for investigating the dynamic operation of ECL. Two ECL gates (Fig. B.53) are connected in cascade via a 1.5-m coaxial cable which has a characteristic impedance $Z_0 = 50\ \Omega$ and a propagation delay $t_d = 10$ ns. Resistor $R_{T1}$ (50 Ω) provides proper termination for the coaxial cable.

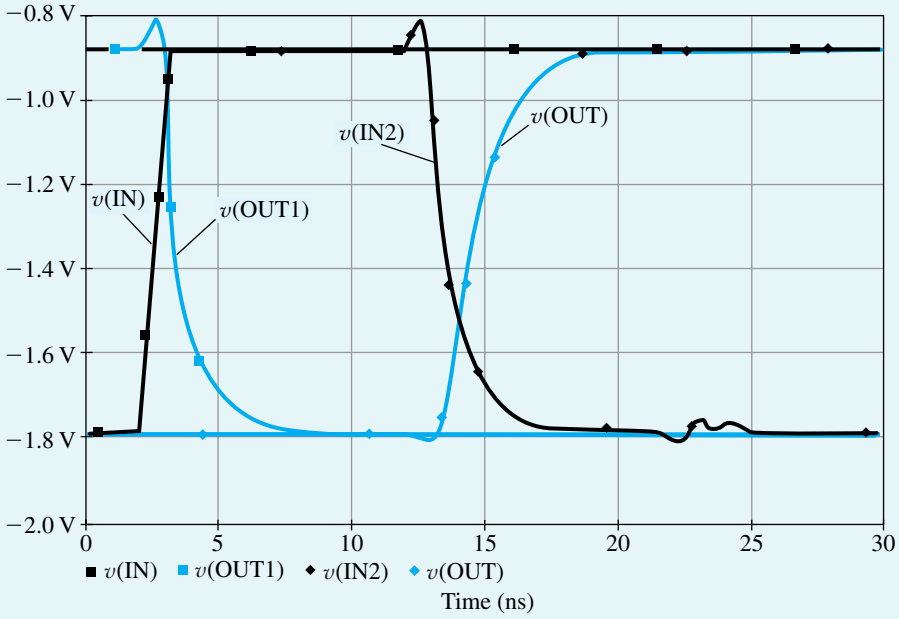



**Figure B.58** Transient response of a cascade of two ECL gates interconnected by a 1.5-m coaxial cable having a characteristic impedance of 50 Ω and a delay of 10 ns (see Fig. B.57).

assumed to be lossless and is modeled in PSpice using the *transmission line* element (the T part in the Analog library) with $Z_0 = 50\ \Omega$ and $t_d = 10$ ns. A voltage step, rising from –1.77 V to –0.884 V in 1 ns, is applied to the input of the first gate, and a transient analysis over a 30-ns interval is requested. Figure B.58 shows plots of the waveforms of the input, the voltage at the output of the first gate, the voltage at the input of the second gate, and the output. Observe that despite the very high edge speeds involved, the waveforms are reasonably clean and free of excessive ringing and reflections. This is particularly remarkable because the signal is being transported over a relatively long distance. A detailed examination of the waveforms reveals that the delay along the cable is indeed 10 ns, and the delay of the second gate is about 1.06 ns.

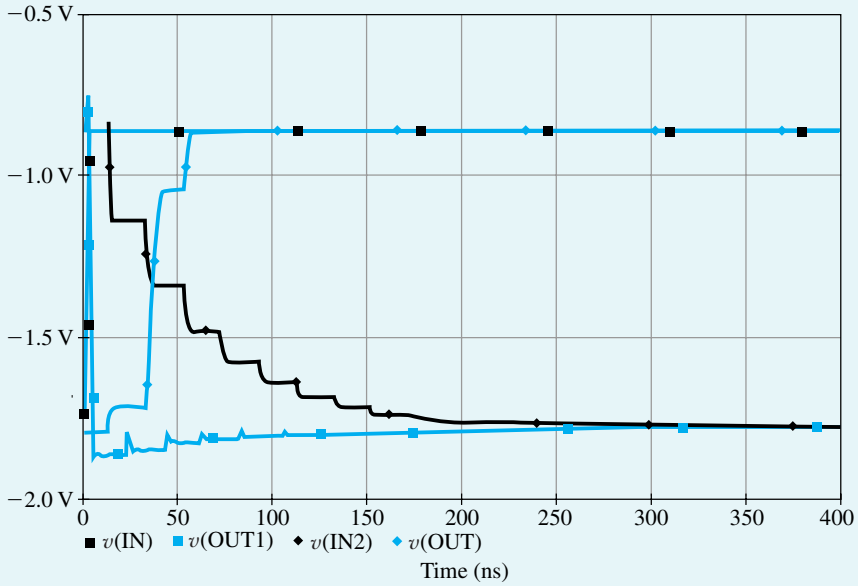



**Figure B.59** Transient response of a cascade of two ECL gates interconnected by a 1.5-m cable having a characteristic impedance of 300 Ω. The termination resistance $R_{T1}$ (see Fig. B.57) was kept unchanged at 50 Ω. Note the change in time scale of the plot.

Finally, to verify the need for properly terminating the transmission line, the dynamic analysis is repeated, this time with the 50-Ω coaxial cable replaced with a 300-Ω twisted-pair cable while keeping the termination resistance unchanged. The results are the slow rising and falling and long-delayed waveforms shown in Fig. B.59. (Note the change of plotting scale.)

## Example PS.16.1

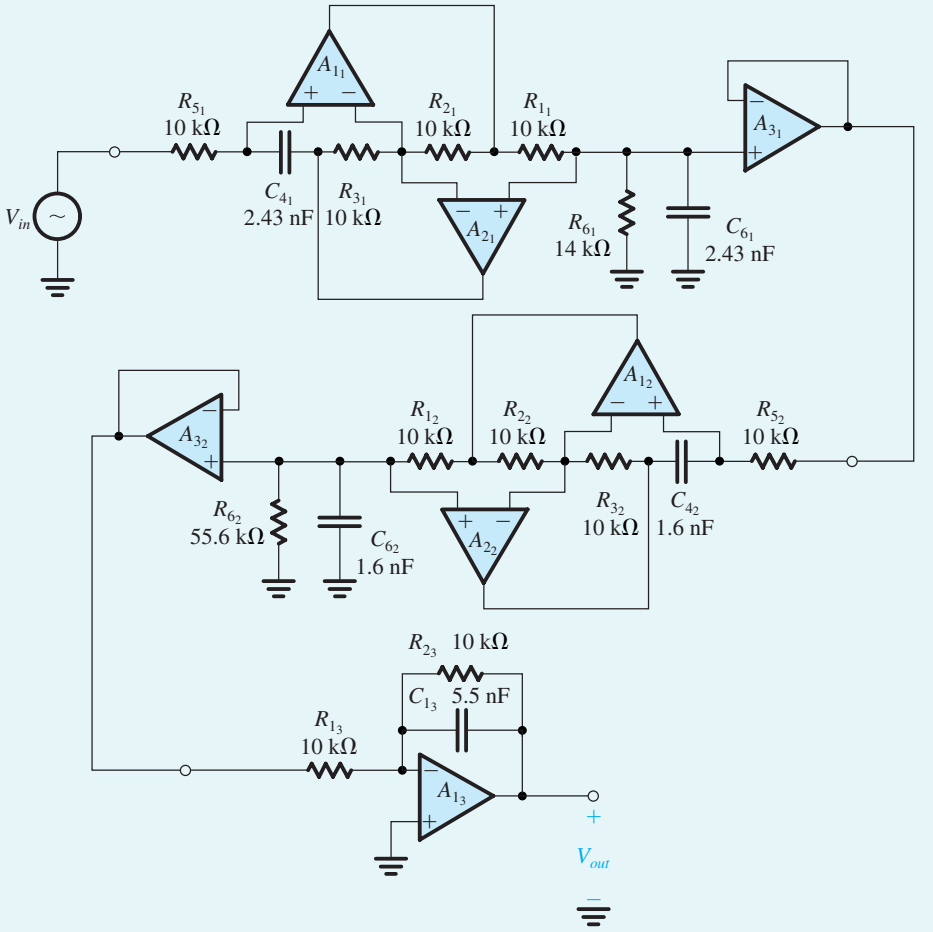
### Verification of the Design of a Fifth-Order Chebyshev Filter

In this example we show how SPICE can be utilized to verify the design of a fifth-order Chebyshev filter. Specifically, we simulate the operation of the circuit whose component values were obtained in Exercise 11.20. The complete circuit is shown in Fig. B.60(a). It consists of a cascade of two second-order simulated-LCR resonators using the Antoniou circuit and a first-order op amp–RC circuit. Using PSpice, we would like to compare the magnitude of the filter response with that computed directly from its transfer function. Here, we note that PSpice can also be used to perform the latter task by using the Laplace transfer-function block in the analog-behavioral-modeling (ABM) library.

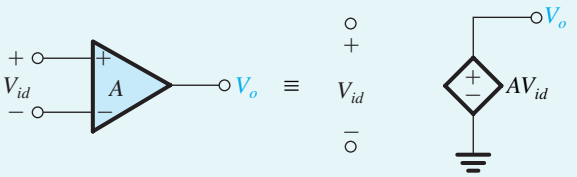
Since the purpose of the simulation is simply to verify the design, we assume ideal components. For the op amps, we utilize a near-ideal model, namely, a voltage-controlled voltage source (VCVS) with a gain of $10^6$ V/V, as shown in Fig. B.60(b).[16]

[16]SPICE models for the op amp are described in Section B.1.1

Example PS.16.1 *continued*



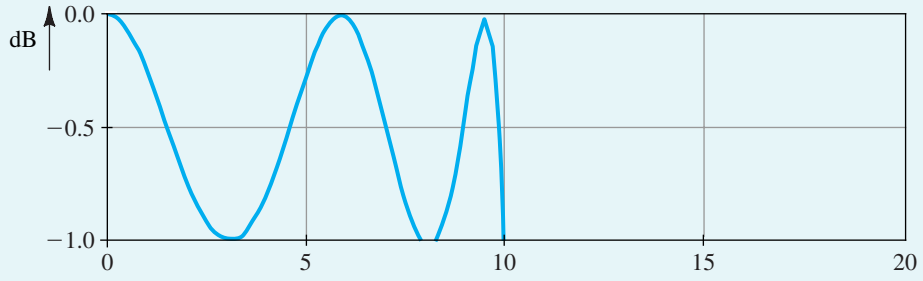

(a)



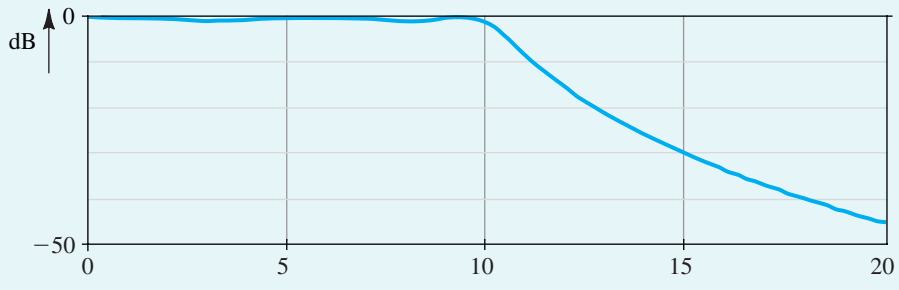

(b)

**Figure B.60** Circuits for Example PS.16.1 **(a)** Fifth-order Chebyshev filter circuit implemented as a cascade of two second-order simulated LCR resonator circuits and a single first-order op amp–RC circuit. **(b)** VCVS representation of an ideal op amp with gain $A$.

In SPICE, we apply a 1-V ac signal at the filter input, perform an ac-analysis simulation over the range 1 Hz to 20 kHz, and plot the output voltage magnitude versus frequency, as shown in Fig. B.61.




(a)




(b)

**Figure B.61** Magnitude response of the fifth-order lowpass filter circuit shown in Fig. B.60: **(a)** an expanded view of the passband region; **(b)** a view of both the passband and stopband regions.

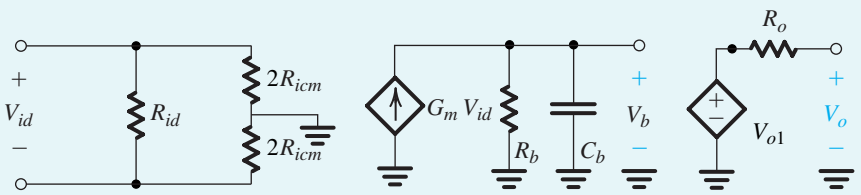
Both an expanded view of the passband and a view of the entire magnitude response are shown. These results are almost identical to those computed directly from the ideal transfer function, thereby verifying the correctness of the design.

## Example PS.16.2

### Effect of Finite Op-Amp Bandwidth on the Operation of the Two-Integrator-Loop Filter

In this example, we investigate the effect of the finite bandwidth of practical op amps on the response of a two-integrator-loop bandpass filter utilizing the Tow-Thomas biquad circuit of Fig. 11.25(b). The circuit is designed to provide a bandpass response with $f_0 = 10$ kHz, $Q = 20$, and a unity center-frequency gain. The op amps are assumed to be of the 741 type. Specifically, we model the terminal behavior of the op amp with the single-time-constant linear network shown in Fig. B.62. Since the analysis performed here is a small-signal (ac) analysis that ignores nonlinearities, no nonlinearities are included in this op-amp

**Example PS.16.2** *continued*




$$A_0 = G_m R_1 \qquad \omega_b = 1/R_b C_b$$

**Figure B.62** One-pole equivalent-circuit macromodel of an op amp operated within its linear region.

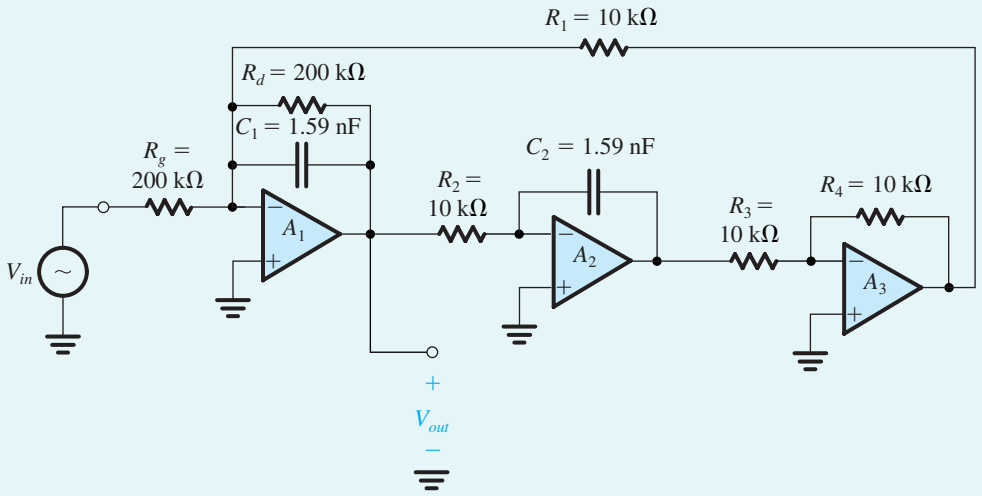



**Figure B.63** Circuit for Example PS.16.2 Second-order bandpass filter implemented with a Tow-Thomas biquad circuit having $f_0 = 10$ kHz, $Q = 20$, and unity center-frequency gain.

macromodel. (If the effects of op-amp nonlinearities are to be investigated, a transient analysis should be performed.) The following values are used for the parameters of the op-amp macromodel in Fig. B.62:

$$R_{id} = 2\ \text{M}\Omega \qquad R_{icm} = 500\ \text{M}\Omega \qquad R_o = 75\ \Omega$$
$$G_m = 0.19\ \text{mA/V} \qquad R_b = 1.323 \times 10^9\ \Omega \qquad C_b = 30\ \text{pF}$$

These values result in the specified input and output resistances of the 741-type op amp. Further, they provide a dc gain $A_0 = 2.52 \times 10^5$ V/V and a 3-dB frequency $f_b$ of 4 Hz, again equal to the values specified for the 741. Note that the selection of the individual values of $G_m$, $R_b$, and $C_b$ is immaterial as long as $G_m R_b = A_0$ and $C_b R_b = 1/2\pi f_b$.

The Tow-Thomas circuit simulated is shown in Fig. B.63. The circuit is simulated in PSpice for two cases: (1) assuming 741-type op amps and using the linear macromodel in Fig. B.62; and (2) assuming ideal op amps with dc gain of $A_0 = 10^6$ V/V and using the near-ideal model in Fig. B.60. In both cases,

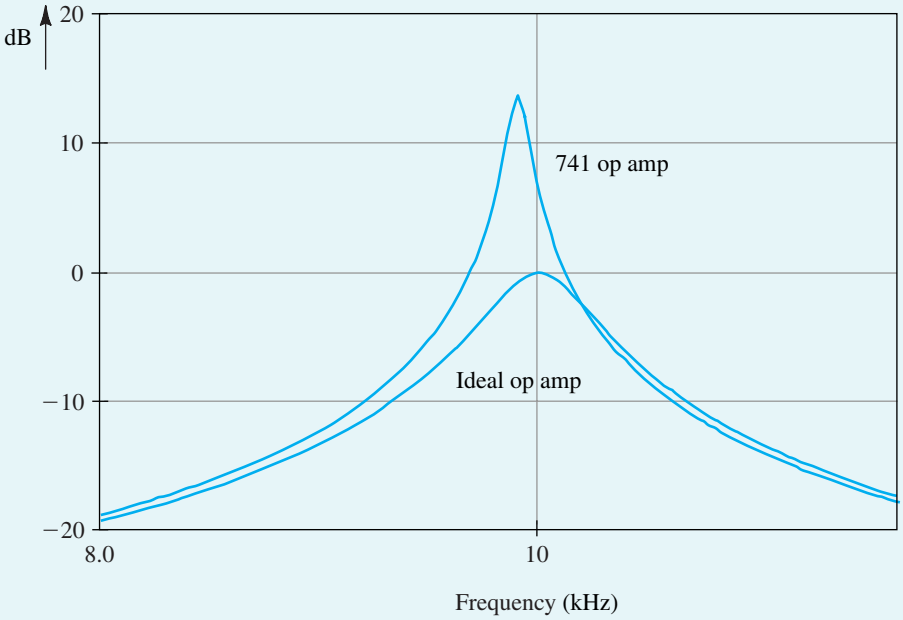


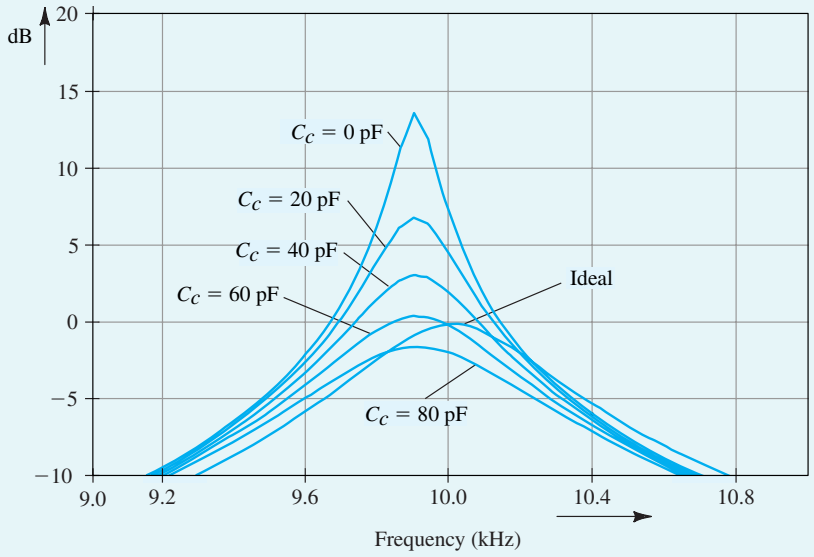

**Figure B.64** Comparing the magnitude response of the Tow-Thomas biquad circuit (shown in Fig. B.63) constructed with 741-type op amps, with the ideal magnitude response. These results illustrate the effect of the finite dc gain and bandwidth of the 741 op amp on the frequency response of the Tow-Thomas biquad circuit.

we apply a 1-V ac signal at the filter input, perform an ac-analysis simulation over the range 8 kHz to 12 kHz, and plot the output-voltage magnitude versus frequency.

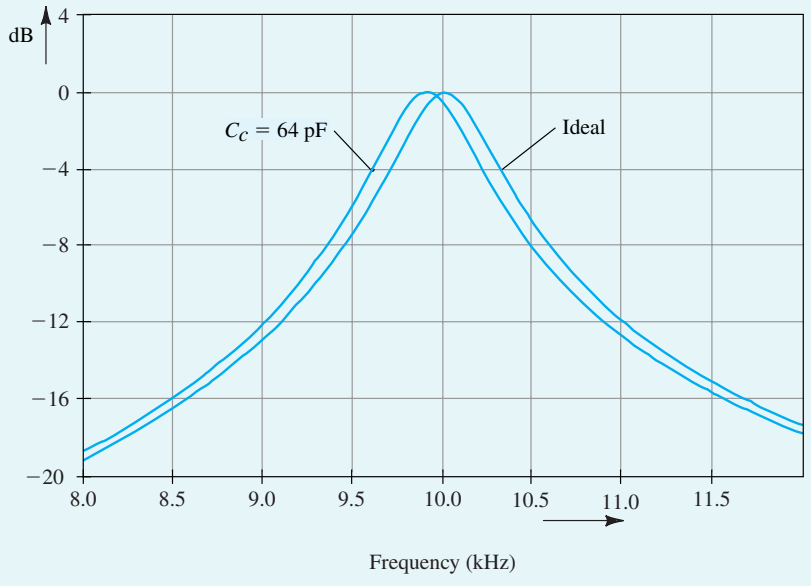
The simulation results are shown in Fig. B.64, from which we observe the significant deviation between the response of the filter using the 741 op amp and that using the near-ideal op-amp model. Specifically, the response with practical op amps shows a deviation in the center frequency of about −100 Hz, and a reduction in the 3-dB bandwidth from 500 Hz to about 110 Hz. Thus, in effect, the filter $Q$ factor has increased from the ideal value of 20 to about 90. This phenomenon, known as *Q-enhancement,* is predictable from an analysis of the two-integrator-loop biquad with the finite op-amp bandwidth taken into account [see Sedra and Brackett (1978)]. Such an analysis shows that $Q$-enhancement occurs as a result of the excess phase lag introduced by the finite op-amp bandwidth. The theory also shows that the $Q$-enhancement effect can be compensated for by introducing phase lead around the feedback loop. This can be accomplished by connecting a small capacitor, $C_c$, across resistor $R_2$. To investigate the potential of such a compensation technique, we repeat the PSpice simulation with various capacitance values. The results are displayed in Fig. B.65(a). We observe that as the compensation capacitance is increased from 0 pF, both the filter $Q$ and the resonance peak of the filter response move closer to the desired values. It is evident, however, that a compensation capacitance of 80 pF causes the response to deviate further from the ideal. Thus, optimum compensation is obtained with a capacitance value between 60 pF and 80 pF. Further experimentation using PSpice enabled us to determine that such an optimum is obtained with a compensation capacitance of 64 pF. The corresponding response is shown, together with the ideal response, in Fig. B.65(b). We note that although the filter $Q$ has been restored to its ideal value, there remains a deviation in the center frequency. We shall not pursue this matter any

**Example PS.16.2** *continued*

further here; our objective is not to present a detailed study of the design of two-integrator-loop biquads; rather, it is to illustrate the application of SPICE in investigating the nonideal performance of active-filter circuits, generally.




(a)




(b)

**Figure B.65** **(a)** Magnitude response of the Tow-Thomas biquad circuit with different values of compensation capacitance. For comparison, the ideal response is also shown. **(b)** Comparing the magnitude response of the Tow-Thomas biquad circuit using a 64-pF compensation capacitor and the ideal response.

## Example PS.17.1

### Wien-Bridge Oscillator

For our first example on oscillators, we shall simulate the operation of the Wien-bridge oscillator whose schematic capture is shown in Fig. B.66. The component values are selected to yield oscillations at 1 kHz. We would like to investigate the operation of the circuit for different settings of $R_{1a}$ and $R_{1b}$, with $R_{1a} + R_{1b} = 50\ \text{k}\Omega$. Since oscillation just starts when $(R_2 + R_{1b})/R_{1a} = 2$ (see Exercise 12.4), that is, when $R_{1a} = 20\ \text{k}\Omega$ and $R_{1b} = 30\ \text{k}\Omega$, we consider three possible settings: (a) $R_{1a} = 15\ \text{k}\Omega$, $R_{1b} = 35\ \text{k}\Omega$; (b) $R_{1a} = 18\ \text{k}\Omega$, $R_{1b} = 32\ \text{k}\Omega$; and (c) $R_{1a} = 25\ \text{k}\Omega$, $R_{1b} = 25\ \text{k}\Omega$. These settings correspond to loop gains of 1.33, 1.1, and 0.8, respectively.

In PSpice, a 741-type op amp and 1N4148-type diodes are used to simulate the circuit in Fig. 12.42.[17] A transient-analysis simulation is performed with the capacitor voltages initially set to zero. This demonstrates that the op-amp offset voltage is sufficient to cause the oscillations to start without the need for special start-up circuitry. Figure B.67 shows the simulation results. The graph in Fig. B.67(a) shows the

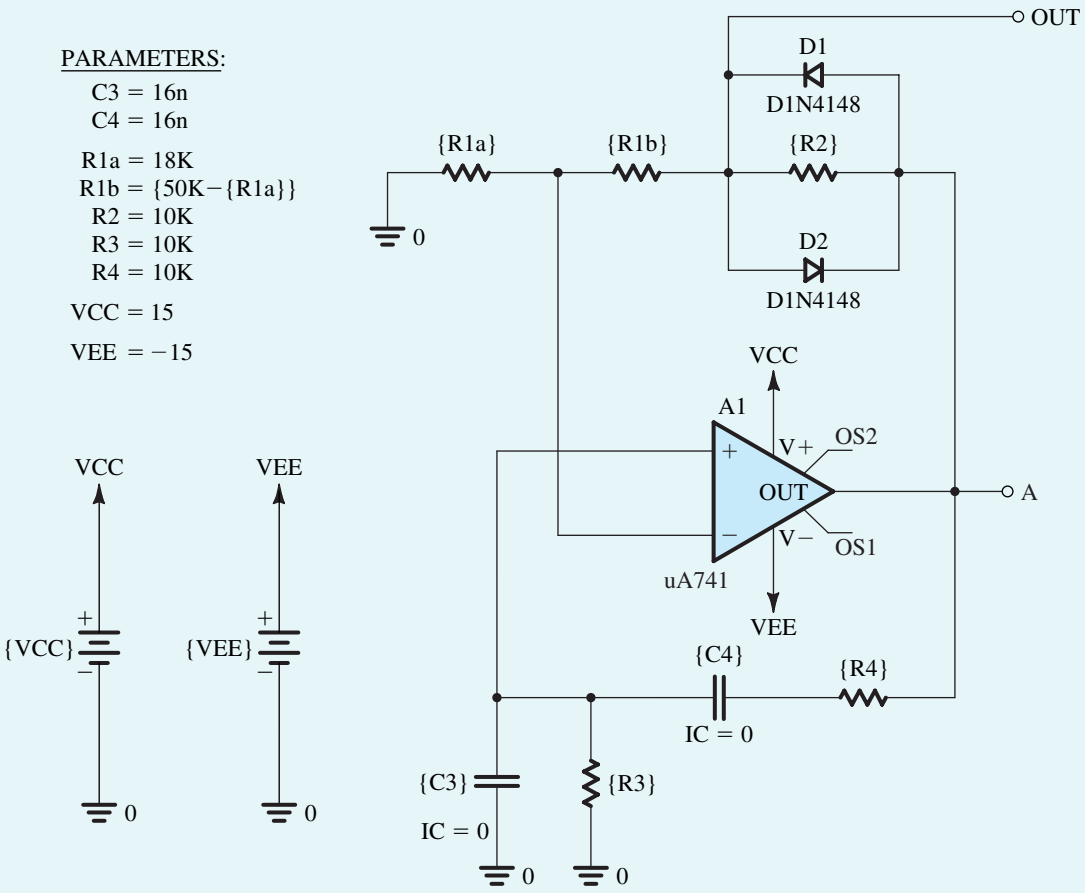
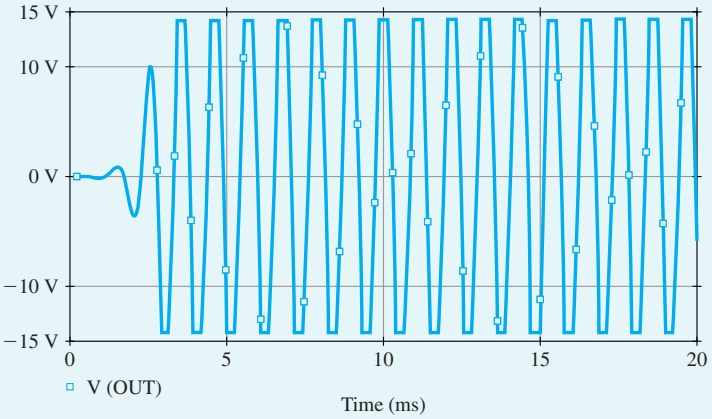


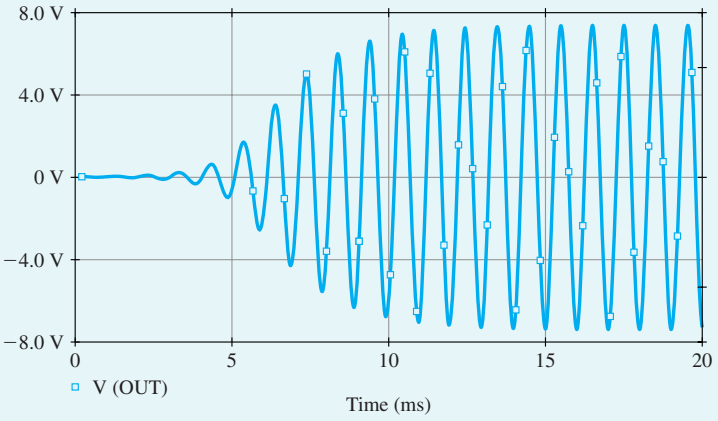

**Figure B.66** Example PS.17.1: Schematic capture of a Wien-bridge oscillator.

[17]The SPICE models for the 741 op amp and the 1N4148 diode are available in PSpice. The 741 op amp was characterized in Example PS.2.2. The 1N4148 diode was used in Example PS.4.1.

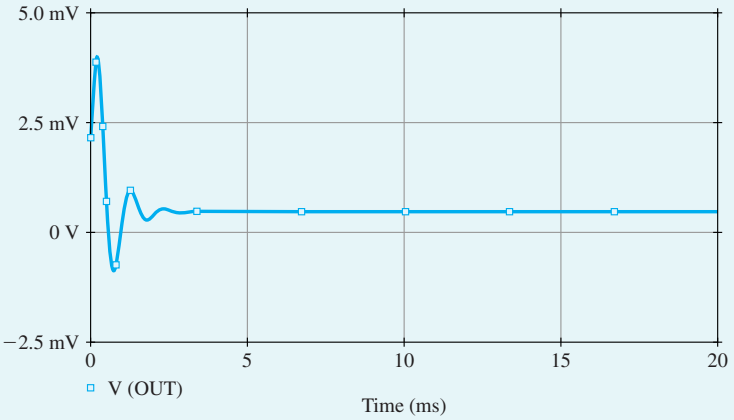
**Example PS.17.1** *continued*




(a) $R_{1a}$ = 15 kΩ, Loop Gain = 1.33




(b) $R_{1a}$ = 18 kΩ, Loop Gain = 1.1




(c) $R_{1a}$ = 25 kΩ, Loop Gain = 0.8

**Figure B.67** Start-up transient behavior of the Wien-bridge oscillator shown in Fig. B.66 for various values of loop gain.

output waveform obtained for a loop gain of 1.33 *V/V*. Observe that although the oscillations grow and stabilize rapidly, the distortion is considerable. The output obtained for a loop gain of 1.1, shown in Fig. B.67(b), is much less distorted. However, as expected, as the loop gain is reduced toward unity, it takes longer for the oscillations to build up and for the amplitude to stabilize. For this case, the frequency is 986.6 Hz, which is reasonably close to the design value of 1 kHz, and the amplitude is 7.37 V. Finally, for a loop gain of 0.8, the output shown in Fig. B.67(c) confirms our expectation that sustained oscillations cannot be obtained when the loop gain is less than unity.

PSpice can be used to investigate the spectral purity of the output sine wave. This is achieved using the Fourier analysis facility. It is found that in the steady state, the output for the case of a loop gain of 1.1 has a THD figure of 1.88%. When the oscillator output is taken at the op-amp output (voltage $v_A$), a THD of 2.57% is obtained, which, as expected, is higher than that for the voltage $v_{OUT}$, but not by very much. The output terminal of the op amp is of course a much more convenient place to take the output.

## Example PS.17.2

### Active-Filter-Tuned Oscillator

In this example, we use PSpice to verify our contention that a superior op amp–oscillator can be realized using the active-filter-tuned circuit of Fig. 12.11. We also investigate the effect of changing the value of the filter $Q$ factor on the spectral purity of the output sine wave.

Consider the circuit whose schematic capture is shown in Fig. B.68. For this circuit, the center frequency is 1 kHz, and the filter $Q$ is 5 when $R_1 = 50$ kΩ and 20 when $R_1 = 200$ kΩ. As in the case of the Wien-bridge circuit in Example PS.17.1, 741-type op amps and 1N4148-type diodes are utilized. In PSpice, a transient-analysis simulation is performed with the capacitor voltages initially set to zero. To be able to compute the Fourier components of the output, the analysis interval chosen must be long enough to allow the oscillator to reach a steady state. The time to reach a steady state is in turn determined by the value of the filter $Q$; the higher the $Q$, the longer it takes the output to settle. For $Q = 5$, it was determined, through a combination of approximate calculations and experimentation using PSpice, that 50 ms is a reasonable estimate for the analysis interval. For plotting purposes, we use 200 points per period of oscillation.

The results of the transient analysis are plotted in Fig. B.69. The upper graph shows the sinusoidal waveform at the output of op amp $A_1$ (voltage $v_1$). The lower graph shows the waveform across the diode limiter (voltage $v_2$). The frequency of oscillation is found to be very close to the design value of 1 kHz. The amplitude of the sine wave is determined using Probe (the graphical interface of PSpice) to be 1.15 V (or 2.3 V p-p). Note that this is lower than the 3.6 V estimated in Exercise 12.7. The latter value, however, was based on an estimate of 0.7-V drop across each conducting diode in the limiter. The lower waveform in Fig. B.69 indicates that the diode drop is closer to 0.5 V for a 1 V peak-to-peak amplitude of the pseudo-square wave. We should therefore expect the peak-to-peak amplitude of the output sinusoid to be lower than 3.6 V by the same factor, and indeed it is approximately the case.

In PSpice, the Fourier analysis of the output sine wave indicates that THD = 1.61%. Repeating the simulation with $Q$ increased to 20 (by increasing $R_1$ to 200 kΩ), we find that the value of THD is reduced to 1.01%. Thus, our expectations that the value of the filter $Q$ can be used as an effective means for controlling the THD of the output waveform are confirmed.

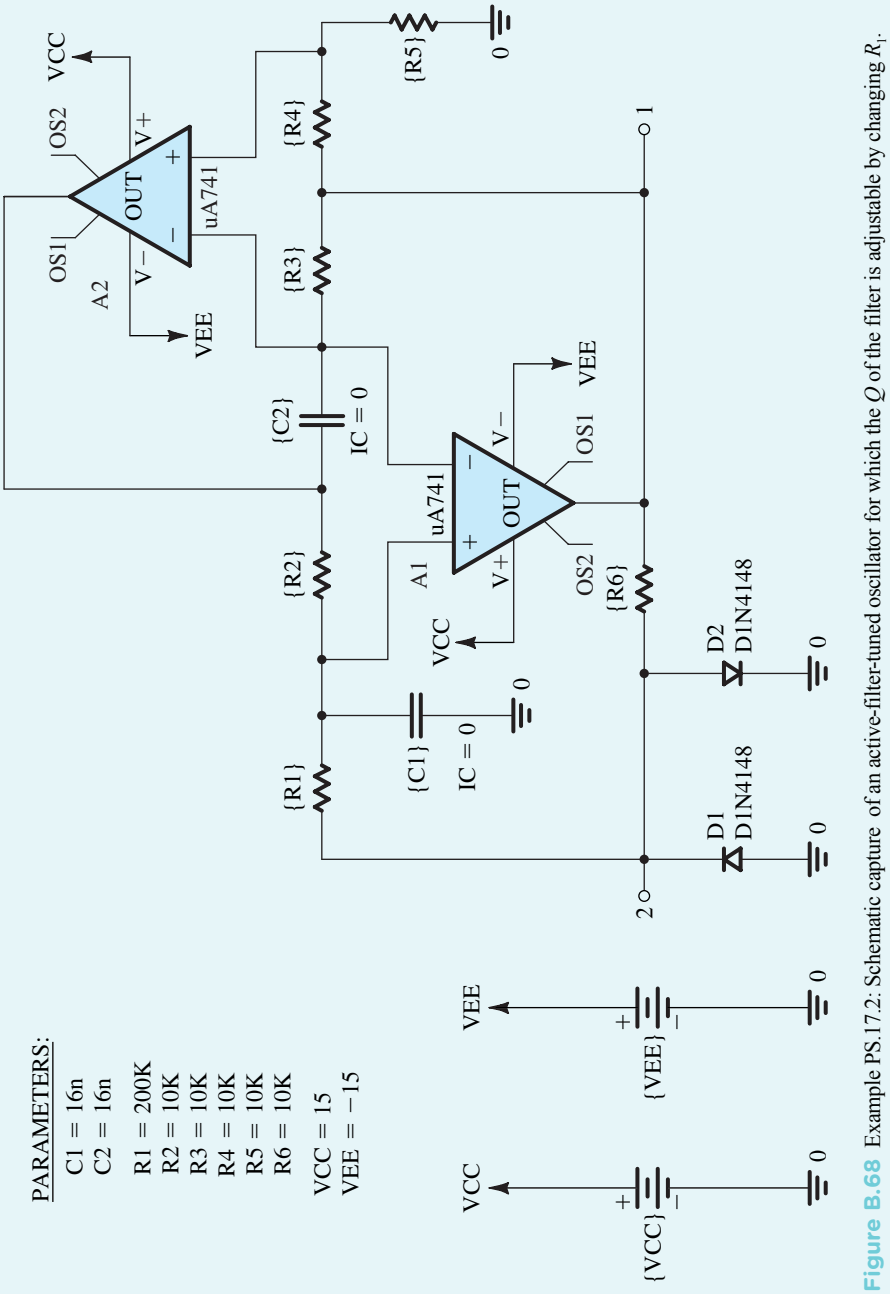



Figure B.68 Example PS.17.2: Schematic capture of an active-filter-tuned oscillator for which the $Q$ of the filter is adjustable by changing $R_1$.

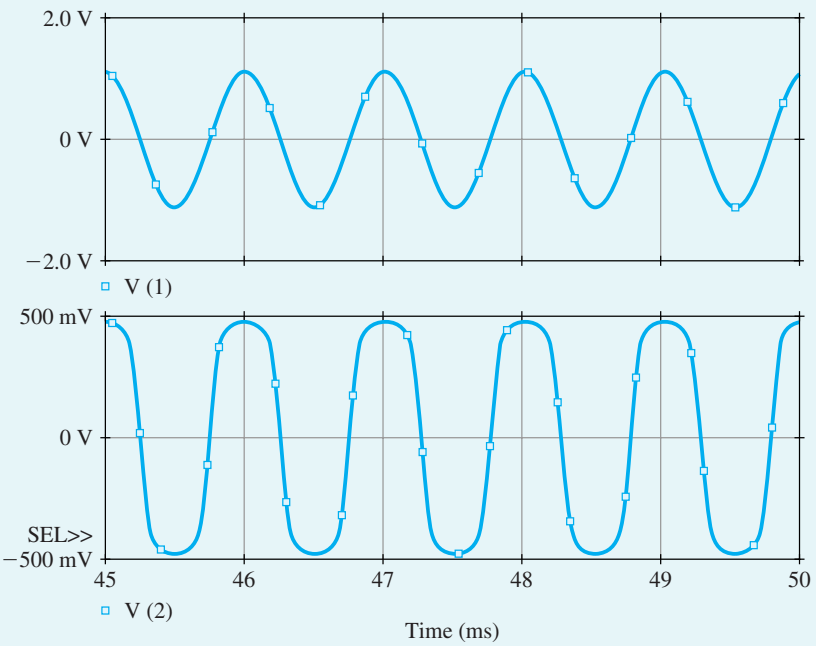



**Figure B.69** Output waveforms of the active-filter-tuned oscillator shown in Fig. B.68 for $Q = 5$ ($R_1 = 50$ kΩ).

## B.3 Multisim Examples

### Example MS.5.1

#### The CS Amplifier

In this example, we will use Multisim to characterize a CS amplifier whose schematic capture is shown in Fig. B.70. We will assume a 0.18-μm CMOS technology for the MOSFET and use typical SPICE level-1 model parameters for this technology, as provided in Table B.4. We will also assume a signal-source resistance $R_{sig} = 10\ \text{k}\Omega$, a load resistance $R_L = 50\ \text{k}\Omega$, and bypass and coupling capacitors of 10 μF. The targeted specifications for this CS amplifier are a voltage gain $|A_v| = 10$ V/V and a maximum power consumption $P = 0.45$ mW. As should always be the case with computer simulation, we will begin with an approximate hand-analysis design. We will then use Multisim to fine-tune our design and to investigate the performance of the final design.

The amplifier specifications are summarized in Table B.13.

#### Hand Design

With a 1.8-V power supply, the drain current of the MOSFET must be limited to $I_D = P/V_{DD} = 0.45$ mW/1.8 V = 0.25 mA to meet the power consumption specification. Choosing $V_{OV} = 0.15$ V and $V_{DS} = V_{DD}/3 = 0.6$ V (to achieve a large signal swing at the output), the MOSFET can now be sized as

**Example MS.5.1** *continued*

| DEVICE PARAMETERS | |
|---|---|
| NAME | Q1:NMOS |
| W | 15.48u |
| L | 0.2u |
| KP | 291u |
| LD | 0.01u |
| VID | 0.45 |
| LAMBDA | 0.08 |
| GAMMA | 0.3 |

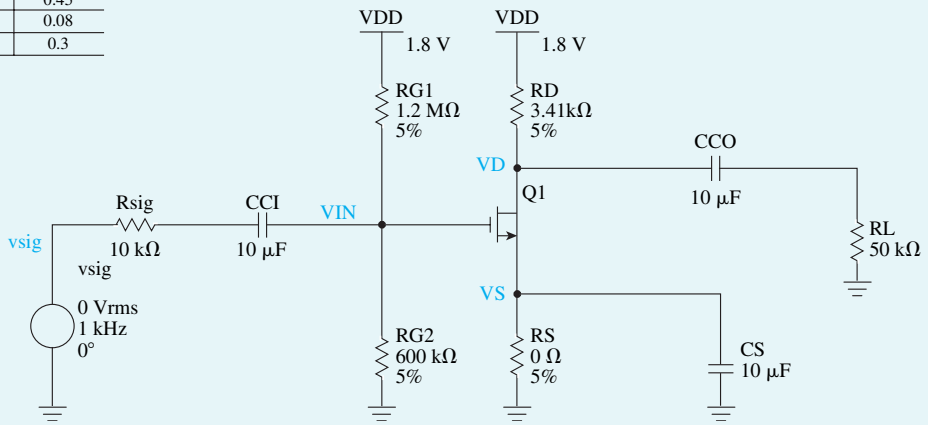



**Figure B.70** Capture schematic of the CS amplifier.

**Table B.13** CS Amplifier Specifications

| Parameters | Value |
|---|---|
| Power | 0.45 mW |
| $R_{sig}$ | 10 kΩ |
| $R_L$ | 50 kΩ |
| $\lvert A_v \rvert$ | 10 V/V |
| $V_{DD}$ | 1.8 V |

$$\frac{W}{L_{\text{eff}}} = \frac{I_D}{\frac{1}{2}k_n' V_{OV}{}^2(1+\lambda V_{DS})} = \frac{250\times 10^{-6}}{\frac{1}{2}\times 246.2\times 10^{-2}\times 0.15^6\times(1+0.08\times 0.6)} \simeq 86$$

where $k_n' = \mu_n C_{\text{ox}} = 246.2\,\mu\text{A/V}^2$. Here, $L_{\text{eff}}$ rather than $L$ is used to more accurately compute $I_D$.

The effect of using $W_{\text{eff}}$ instead of $W$ is much less important, because typically $W \gg W_{ov}$. Thus, choosing $L = 0.200$ µm results in $L_{\text{eff}} = L - 2L_{ov} = 0.180$ µm, and $W = 86 \times L_{\text{eff}} = 15.48$ µm.

Note that we chose $L$ slightly larger than $L_{\text{min}}$. This is a common practice in the design of analog ICs to minimize the effects of fabrication nonidealities on the actual value of $L$. As we have seen, this is particularly important when the circuit performance depends on the matching between the dimensions of two or more MOSFETs (e.g., in the current-mirror circuits studied in Chapter 6).

Next, $R_D$ is calculated based on the desired voltage gain:

$$\lvert A_v \rvert = g_m(R_D \| R_L \| r_o) = 10\text{V/V} \Rightarrow R_D \simeq 3.41\text{k}\Omega$$

where

$$g_m = \frac{2I_D}{V_{OV}} = \frac{2\times 0.25\times 10^{-3}}{0.15} = 3.33\ \text{mA/V}$$

and

$$r_o = \frac{V_A}{I_D} = \frac{12.5}{0.25 \times 10^{-3}} = 50\ \text{k}\Omega$$

Hence, the dc bias voltage is $V_D = V_{DD} - I_D R_D = 0.9457$ V.

To stabilize the bias point of the CS amplifier, we include a resistor in the source lead. In other words, to bias the MOSFET at $V_{DS} = V_{DD}/3$, we need an

$$R_s = \frac{V_S}{I_D} = \frac{(V_D - V_{DD}/3)}{I_D} = \frac{0.3475}{0.25 \times 10^{-3}} = 1.39\ \text{k}\Omega$$

However, as a result of including such a resistor, the gain drops by a factor of $(1 + g_m R_S)$. Therefore, we include a capacitor, $C_S$, to eliminate the effect of $R_S$ on ac operation of the amplifier and gain.

Finally, choosing the current in the biasing branch to be 1 μA gives $R_{G1} + R_{G2} = V_{DD}/1\mu A = 1.8\ \Omega$. Also, we know that

$$V_{GS} = V_{OV} + V_t = 0.15 + 0.45 = 0.6\ \text{V} \Rightarrow V_G = V_S + 0.6 = 0.3475 + 0.6 = 0.9475\ \text{V}$$

Hence,

$$\frac{R_{G2}}{R_{G1} + R_{G2}} = \frac{V_G}{V_{DD}} = \frac{0.9475}{1.8} \Rightarrow R_{G1} = 0.8525\ \text{M}\Omega,\ R_{G2} = 0.9475\text{M}\Omega$$

Using large values for these gate resistors ensures that both their power consumption and the loading effect on the input signal source are negligible.

## Simulation

**Amplifier Biasing** We will now use Multisim to verify our design and investigate the performance of the CS amplifier. We begin by performing a bias-point simulation to verify that the MOSFET is properly biased in the saturation region and that the dc voltages and currents match the expected values (refer to this example's simulation file: Ch5_CS_Amplifier_Ex_DC.ms10). The results are shown in Fig. B.71.

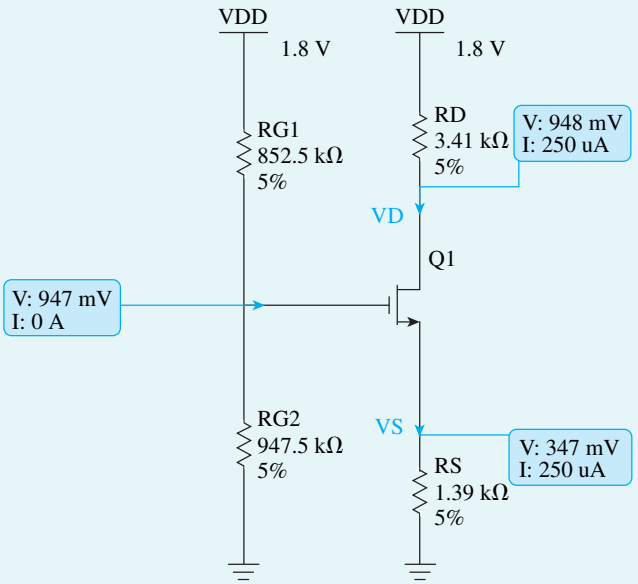



**Figure B.71** DC bias-point analysis of the CS amplifier.

**Example MS.5.1** *continued*

**Amplifier Gain** We can also verify if our design provides the desired gain. This can be done by performing transient response analysis, as set up in Ch5_CS_Amplifier_Ex_gain.ms10. As can be seen from Fig. B.72, $|G_v| \simeq |A_v| \simeq 11$ V/V. Note the values of overall voltage gain $G_v$ and $A_v$ are close since $R_{in} = (R_{G1}||R_{G2}) \gg R_{sig}$. In the case where the capacitor $C_S$ is not included ($C_S = 0$), the gain drops by a factor of 5.63 (approximately equal to $1 + g_m R_S$) to 1.95. This is as expected from our study of the CS amplifier with a source-degeneration resistance.

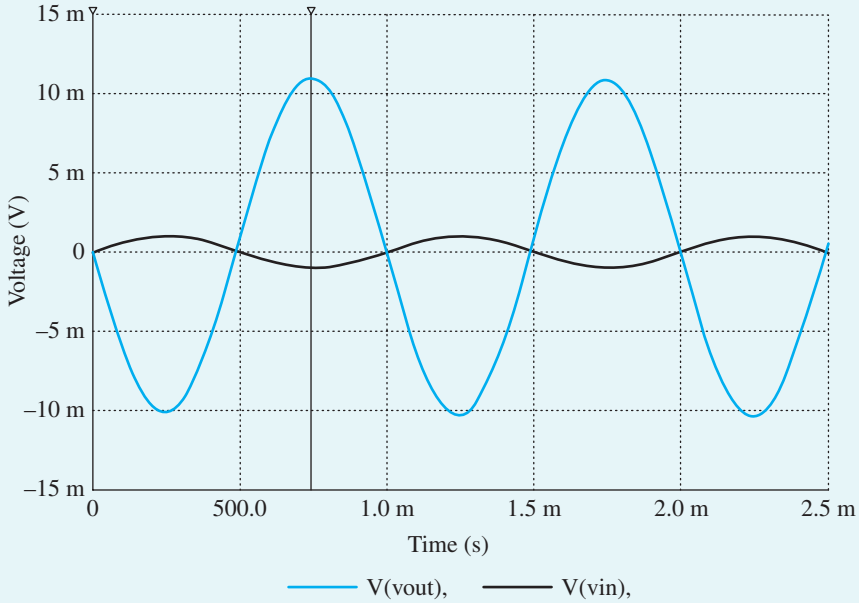



**Figure B.72** $A_v$ and $G_v$ of the CS amplifier: transient analysis.

**Investigating Amplifier Bias Stability** We can also demonstrate the improved bias stability achieved when a source resistor $R_S$ is used. Specifically, we change (in the MOSFET level-1 model) the value of the zero-bias threshold voltage parameter *VT0* by ± 0.1 V and perform bias-point simulation in Multisim. Table B.14 shows the corresponding variations in $I_D$ and $V_D$ for the case in which $R_S$ = 1.39 kΩ. For the case without source degeneration, we use an $R_S = 0$ in the given schematic. Furthermore, to obtain the same $I_D$ and $V_D$ in both cases (for the nominal threshold voltage $V_{t0} = 0.45$ V), we use $R_{G1} = 1.2$ MΩ and $R_{G2} = 0.6$ MΩ.

**Table B.14** Variations in *VT0*

| With $R_S = 1.39$ kΩ | | | | |
|---|---|---|---|---|
| *VT0* (V) | $I_D$ (μA) | $I_D$ % Change | $V_D$ (V) | $V_D$ % Change |
| 0.45 | 250 | 0 | 0.948 | 0 |
| 0.35 | 309 | 23.60% | 0.748 | -21.10% |
| 0.55 | 192 | -37.86% | 1.14 | 20.25% |

| Without $R_S$ | | | | |
|---|---|---|---|---|
| 0.45 | 255.96 | 0 | 0.9292 | 0 |
| 0.35 | 492 | 96.80% | 0.122 | -87.13% |
| 0.55 | 30.1 | -90.26% | 1.7 | 127.27% |

Also, Table B.15 shows the worst case deviation of $I_D$ and $V_D$ values, when imposing 5% tolerance on the resistors that determine the gate voltage.

**Table B.15** Variations Due to Resistor Tolerances

| | | | With $R_S$ = 1.39 kΩ s | | | |
|---|---|---|---|---|---|---|
| | $R_{G1}$ (MΩ) | $R_{G2}$ (MΩ) | $I_D$ (μA) | $I_D$ % Change | $V_D$ (V) | $V_D$ % Change |
| Nominal | 0.8525 | 0.9475 | 250 | 0 | 947.67 | 0 |
| $I_D$ low $V_D$ high | 0.895 | 0.9 | 223.86 | -10.44% | 1.037 | 9.39% |
| $I_D$ high $V_D$ low | 0.81 | 0.995 | 276.1 | 10.46% | 0.858 | -9.41% |
| | | | Without $R_S$ | | | |
| | $R_{G1}$ (MΩ) | $R_{G2}$ (MΩ) | $I_D$ (μA) | $I_D$ % Change | $V_D$ (V) | $V_D$ % Change |
| Nominal | 1.2 | 0.6 | 255.96 | 0 | 0.9292 | 0 |
| $I_D$ low $V_D$ high | 1.26 | 0.57 | 143.28 | -44.02% | 1.311 | 41.44% |
| $I_D$ high $V_D$ low | 1.14 | 0.63 | 398.62 | 55.74% | 0.447 | -52.47% |

Accordingly, we see that the source-degeneration resistor makes the bias point of the CS amplifier less sensitive to changes in the threshold voltage and the values of gate resistors. However, unless a large bypass capacitor $C_S$ is used, this reduced sensitivity comes at the expense of a reduction in gain.

**Largest Allowable Input Signal Swing** Next, we wish to analyze this amplifier circuit to determine the largest allowable $v_{sig}$ for which the transistor remains in saturation:

$$v_{DS} \geq v_{GS} - v_t$$

By enforcing this condition, with equality, at the point $v_{GS}$ is maximum and $v_{DS}$ is correspondingly minimum, we write:

$$v_{DS,\min} \geq v_{GS,\max} - v_{t0}$$

$$v_{DS} - |G_v| v_{sig} = V_{GS} + v_{sig} - v_{t0}$$

$$v_{sig} = \frac{V_{DS} - V_{GS} + V_{t0}}{(1 + |G_v|)} = \frac{0.9475 - 0.6 + 0.45}{11} = 72.5 \text{ mV}$$

This can be verified from Ch5_CS_Amplifier_Ex_swing.ms10 simulation setup. If we increase the source signal's amplitude beyond approximately 73 mV, we can observe the distortion in the output signal, indicating that the MOSFET has entered the triode region.

**Amplifier Linearity** Finally, we can investigate the linearity of the designed amplifier. To do so, we use the setup in Ch5_CS_Amplifier_Ex_linearity.ms10. In this case, we use a triangular waveform and increase the amplitude of the signal until the output waveform begins to show nonlinear distortion (i.e., the rising and falling edges are no longer straight lines). Based on hand analysis, linearity holds as long as $v_{in} \ll 2V_{ov}$. According to the simulation results, linearity holds until $v_{in}$ reaches the value of approximately 30 mV, which is one-tenth of the value of $2V_{ov}$.

## Example MS.6.1

### Dependence of $\beta$ on the Bias Current

In this example, we use Multisim to investigate the dependence of $\beta_{dc}$ on the collector bias current of the Q2N3904 discrete BJT (from Fairchild Semiconductor) whose model parameters are listed in Table B.16 and are available in Multisim. As shown in the schematic capture of Fig. B.73, the $V_{CE}$ of the BJT is fixed using a constant voltage source (in this example, $V_{CE} = 2$ V) and a dc current source $I_B$ is applied at the base. To obtain the dependence of $\beta_{dc}$ on the collector current $I_C$, we perform a dc-analysis simulation in which the sweep variable is the current source $I_B$. The $\beta_{dc}$ of the BJT, which corresponds to the ratio of the collector current $I_C$ to the base current $I_B$, can then be plotted versus $I_C$ (by exporting the data to a graphing software), as shown in Fig. B.74. We see that to operate at the maximum value of $\beta_{dc}$ (i.e., $\beta_{dc} = 163$), at $V_{CE} = 2$ V, the BJT must be biased at an $I_C = 10$ mA. Since increasing the bias current of a transistor increases the power dissipation, it is clear from Fig. B.74 that the choice of current $I_C$ is a trade-off between the current gain $\beta_{dc}$ and the power dissipation. Generally speaking, the optimum $I_C$ depends on the application and technology in hand. For example, for the Q2N3904 BJT operating at $V_{CE} = 2$ V, decreasing $I_C$ by a factor of 20 (from 10 mA to 0.5 mA) results in a drop in $\beta_{dc}$ of about 25% (from 163 to 123).

**Table B.16** SPICE Model Parameters of the Q2N3904 Discrete BJT

| | | | | | | |
|---|---|---|---|---|---|---|
| Is = 6.734f | Bf = 416.4 | Xtb = 1.5 | Ikr = 0 | Vjc = .75 | Vje = .75 | Vtf = 4 |
| Xti = 3 | Ne = 1.259 | Br = .7371 | Rc = 1 | Fc = .5 | Tr = 239.5n | Xtf = 2 |
| Eg = 1.11 | Ise = 6.734f | Nc = 2 | Cjc = 3.638p | Cje = 4.493p | Tf = 301.2p | Rb = 10 |
| Vaf = 74.03 | Ikf = 66.78m | Isc = 0 | Mjc = .3085 | Mje = .2593 | Itf = .4 | |

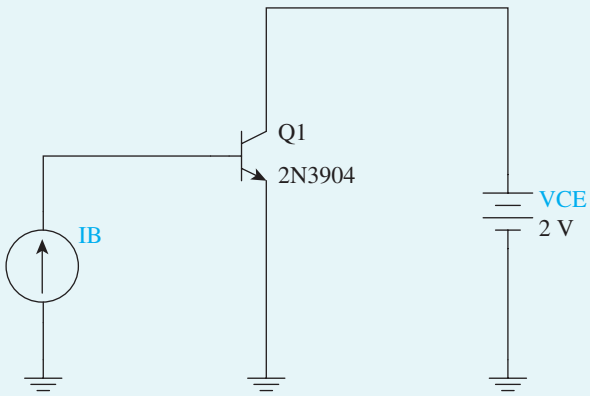



**Figure B.73** The test bench used to investigate the dependence of $\beta_{dc}$ on the bias current for the Q2N3904 discrete BJT.

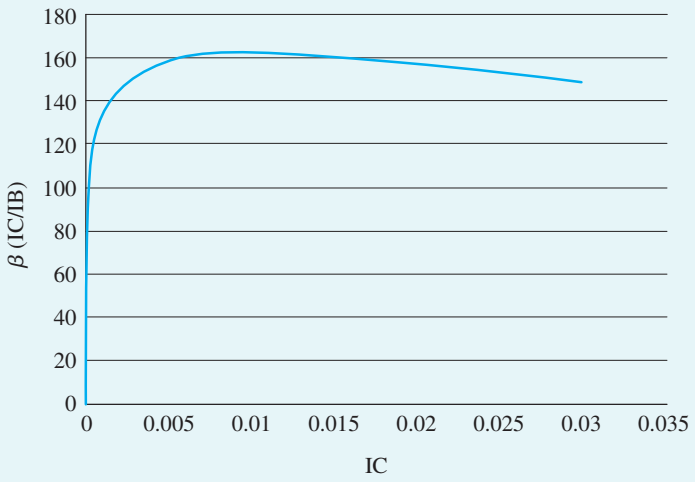



**Figure B.74** Dependence of $\beta_{dc}$ on $I_C$ (at $V_{CE} = 2$ V) in the Q2N3904 discrete BJT.

## Example MS.6.2

### The CE Amplifier with Emitter Resistance

In this example, we use Multisim to compute the voltage gain and frequency response of the CE amplifier and investigate its bias-point stability. A schematic capture of the CE amplifier is shown in Fig. B.75. We will use part Q2N3904 for the BJT and a ±5-V power supply. We will assume a signal-source resistor $R_{sig} = 10$ kΩ, a load resistor $R_L = 10$ kΩ, and bypass and coupling capacitors of 10 μF. To enable us to investigate the effect of including a resistance in the signal path of the emitter, a resistor $R_{ce}$ is connected in series with the emitter bypass capacitor $C_E$. Note that the roles of $R_E$ and $R_{ce}$ are different. Resistor $R_E$ is the dc emitter-degeneration resistor because it appears in the dc path between the emitter and ground. It is therefore used to help stabilize the bias point for the amplifier. The equivalent resistance $R_e = R_E \parallel R_{ce}$ is the small-signal emitter-degeneration resistance because it appears in the ac (small-signal) path between the emitter and ground and helps stabilize the gain of the amplifier. In this example, we will investigate the effects of both $R_E$ and $R_e$ on the performance of the CE amplifier. However, as should always be the case with computer simulation, we will begin with an approximate hand analysis. In this way, maximum advantage and insight can be obtained from simulation.

Based on the plot of $\beta_{dc}$ versus $I_B$ in Fig. B.74, a collector bias current $I_C$ (i.e., $\beta_{dc} I_B$) of 0.5 mA is selected for the BJT, resulting in $\beta_{dc} = 123$. This choice of $I_C$ is a reasonable compromise between power dissipation and current gain. Furthermore, a collector bias voltage $V_C$ of 0 V (i.e., at the mid–supply rail) is selected to achieve a high signal swing at the amplifier output. For $V_{CE} = 2$ V, the result is that $V_E = -2$ V, requiring bias resistors with values

$$R_C = \frac{V_{CC} - V_C}{I_C} = 10 \text{ k}\Omega$$

$$R_E = \frac{V_E - V_{EE}}{I_C} = 320 \text{ k}\Omega$$

Assuming $V_{BE} = 0.7$ V and $\beta_{dc} = 123$, we can determine

$$R_B = -\frac{V_B}{I_B} = -\frac{V_{BE} + V_E}{I_C / \beta_{dc}} = 320 \text{ k}\Omega$$

**Example MS.6.2** *continued*

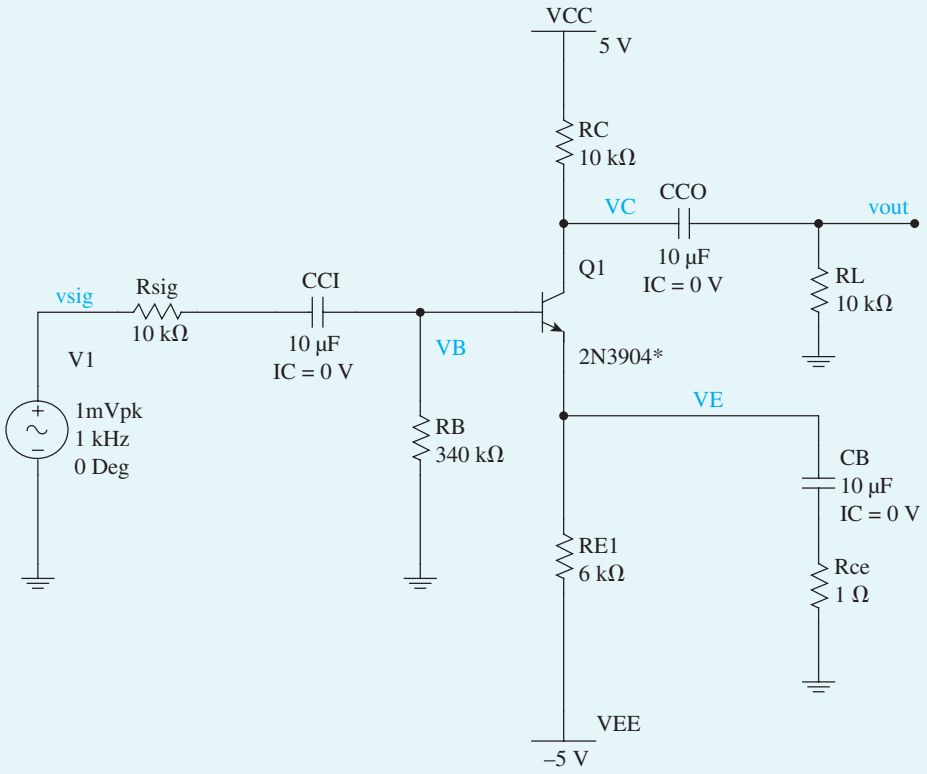



**Figure B.75** Schematic capture of the CE amplifier.

Next, the input resistance $R_{in}$ and the voltage gain $|A_v|$ of the CE amplifier:

$$R_{in} = R_B(\beta_{ac} + 1)(r_e + R_e)$$

$$|A_v| = \left| -\frac{R_{in}}{R_{sig} + R_{in}} \times \frac{R_C \| R_L}{r_e + R_e} \right|$$

For simplicity, we will assume $\beta_{ac} \simeq \beta_{dc} = 123$, resulting in

$$r_e = \left(\frac{\beta_{ac}}{\beta_{ac} + 1}\right)\left(\frac{V_T}{I_c}\right) = 49.6\Omega$$

Thus, with no small-signal emitter degeneration (i.e., $R_{ce} = 0$), $R_{in} = 6.1$ kΩ and $|A_v| = 38.2$ V/V. Using the equation found for $|A_v|$ and assuming that $R_B$ is large enough to have a negligible effect on $R_{in}$, it can be shown that the emitter-degeneration resistance $R_e$ decreases the voltage gain $|A_v|$ by a factor of

$$\frac{1 + \dfrac{R_e}{r_e} + \dfrac{R_{sig}}{r_\pi}}{1 + \dfrac{R_{sig}}{r_\pi}}$$

Therefore, to limit the reduction in voltage gain to a factor of 2, we will select

$$R_e = r_e + \frac{R_{sig}}{\beta_{ac} + 1}$$

Thus, $R_{ce} \simeq R_e = 130\,\Omega$. Substituting this value in the equations found for $|A_v|$ and $R_{in}$ shows that $R_{in}$ increases from 6.1 kΩ to 20.9 kΩ while $|A_v|$ drops from 38.2 V/V to 18.8 V/V.

We will now use Multisim to verify our design and investigate the performance of the CE amplifier. We begin by performing a bias-point simulation to verify that the BJT is properly biased in the active region and that the dc voltages and currents meet the desired specifications. Based on this simulation forward, we have increased the value of $R_B$ to 340 kΩ in order to limit $I_C$ to about 0.5 mA while using a standard 1% resistor value. Next, to measure the gain $A_v$, we conduct a transient response analysis, as set up in Ch6_CE_Amplifier_Ex.ms10. Accordingly, with no emitter degeneration, the gain is $|A_v| = 38.5$ V/V. Using $R_{ce} = 130\,\Omega$ results in a drop in the gain by a factor of 2 (as can be seen from Fig. B.76).

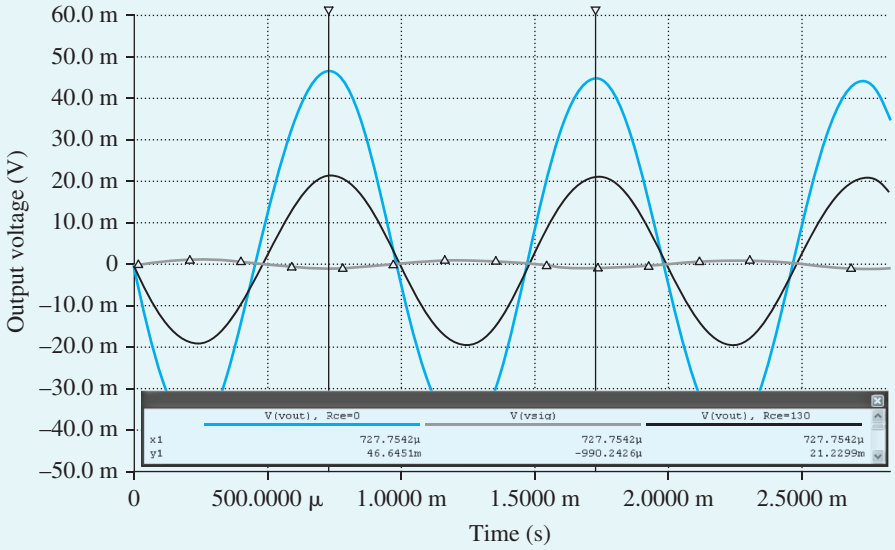



**Figure B.76** Transient analysis of the CE amplifier with $R_{ce} = 0$ and $R_{ce} = 130\Omega$.

Thus far in this example, we have assumed that the voltage gain of the BJT amplifier is constant and independent of the frequency of the input signal. However, as mentioned in Section 4.8.6, this is not true, since it implies that the amplifier has infinite bandwidth. To illustrate the finite bandwidth, we compute the frequency response of the amplifier. The plot of the output-voltage magnitude (in dB) versus frequency is shown in Fig. B.77. With no emitter degeneration, the midband gain is $|A_M| = 38.5$ V/V = 31.7 dB and the 3-dB bandwidth is $BW = f_H - f_L = 145.7$ kHz. Using an $R_{ce}$ of 130Ω results in a drop in the midband gain $|A_M|$ by a factor of 2 (consistent with what we observed previously in our transient analysis). Interestingly, however, $BW$ has now increased by approximately the same factor as the drop in $|A_M|$. As we learned in Chapter 9, the emitter-degeneration resistor $R_{ce}$ provides negative feedback, which allows us to trade off gain for other desirable properties such as a larger input resistance and a wider bandwidth.

To conclude this example, we will demonstrate the improved bias-point (or dc operating point) stability achieved when an emitter resistor $R_E$ is used. Specifically, we will increase/decrease the value of the parameter $BF$ (i.e., the ideal maximum forward current gain) in the SPICE model for part Q2N3904 by a factor of 2 and read the bias-point probes. The corresponding change in BJT parameter ($\beta_{dc}$) and bias-point ($I_C$ and $V_{CE}$) are presented in Table B.17 for the case of $R_E = 6\,\text{k}\Omega$.

**Example MS.6.2** *continued*

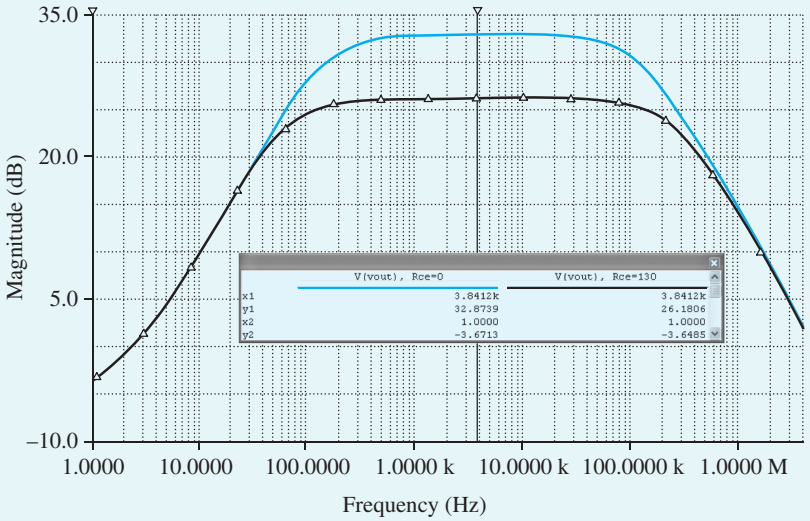



**Figure B.77** Frequency response of the CE amplifier with $R_{ce} = 0$ and $R_{ce} = 130\,\Omega$.

**Table B.17** Variations in the Bias Point of the CE Amplifier with the SPICE Model Parameter *BF* of BJT

| *BF* (in SPICE) | $R_E = 6\ \text{k}\Omega$ | | | $R_E = 0$ | | |
|---|---|---|---|---|---|---|
| | $\beta_{dc}$ | $I_C$ (mA) | $V_C$ (V) | $\beta_{dc}$ | $I_C$ (mA) | $V_C$ (V) |
| 208 | 94.9 | 0.452 | 0.484 | 96.9 | 0.377 | 1.227 |
| 416.4 (nominal value) | 123 | 0.494 | 0.062 | 127 | 0.494 | 0.060 |
| 832 | 144 | 0.518 | -0.183 | 151 | 0.588 | -0.878 |

For the case without emitter degeneration, we will use $R_E = 0$ in the schematic of Fig. B.75. Furthermore, to maintain the same $I_C$ and $V_C$ in both cases at the values obtained for nominal *BF*, we use $R_B = 1.12\ \text{M}\Omega$ to limit $I_C$ to approximately 0.5 mA. The corresponding variations in the BJT bias point are also shown in Table B.17. Accordingly, we see that emitter degeneration makes the bias point of the CE amplifier much less sensitive to changes in $\beta$. However, unless a large bypass capacitor $C_E$ is used, this reduced bias sensitivity comes at the expense of a reduction in gain (as we observed in this example when we simulated the transient response of the CE amplifier with an $R_{ce} = 130\,\Omega$).

## Example MS.7.1

### The CMOS CS Amplifier

In this example, we will use Multisim to characterize the CMOS CS amplifier whose schematic capture is shown in Fig. B.78. We will assume a 0.18-μm CMOS technology for the MOSFET and use typical SPICE level-1 model parameters for this technology as given in Table B.4. We will begin with an approximate hand-analysis design. We will then use Multisim to investigate the performance of the final design. The targeted specifications for this CMOS CS amplifier are a voltage gain $|G_v| = 50$ V/V and a bias current $I_D$ of 100 μA.

The amplifier specifications are summarized in Table B.18.

**Table B.18** CMOS CS Amplifier Specifications

| Specification | Value |
|---|---|
| $I_D$ | 100 µA |
| $\|G_v\|$ | 50 V/V |
| $V_{DD}$ | 1.8 V |

| NMOS | |
|---|---|
| Vtn | 0.5 V |
| \|VAn\| | 12.5 V |
| kn' | 246.2uA/V^2 |
| I | 0.1 mA |
| L | 0.2 um |
| W | 0.523 um |

| PMOS | |
|---|---|
| Vtp | –0.5 V |
| \|VAp\| | 9V |
| kp' | –86.1 uA/V^2 |
| I | 0.1 mA |
| L | 0.2 um |
| W | 0.46 um |

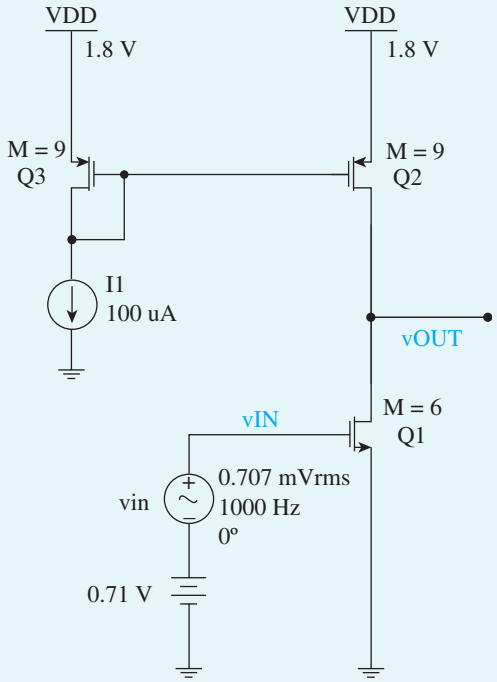



**Figure B.78** Schematic capture of the CMOS CS amplifier.

## Hand Design

For the design of this amplifier we choose $L = 0.20$ µm, so that similar to Example MS.5.1, we have $L_{\text{eff}} = 0.18$ µm. For this channel length, and in 0.18-µm CMOS technology, the magnitudes of the Early voltages of the NMOS and PMOS transistors are $V_{An} = 12.5$ V and $|V_{Ap}| = 9$ V, respectively. Therefore, the value of $V_{OV1}$ can now be calculated as follows:

$$G_v = -g_m R_L' = -g_m(r_{o1} \| r_{o2}) = -\frac{2}{V_{OV1}}\left(\frac{V_{An}|V_{Ap}|}{V_{An}|V_{Ap}|}\right)$$

$$V_{OV1} = -\frac{2}{G_v}\left(\frac{V_{An}|V_{Ap}|}{V_{An}|V_{Ap}|}\right) = -\frac{2}{(-50)}\left(\frac{12.5 \times 9}{12.5 + 9}\right) \simeq 0.21\text{V}$$

MOSFET 1 can now be sized (by ignoring the channel-length modulation) as

$$\frac{W_1}{L_{\text{eff}}} = \frac{I_D}{\frac{1}{2}k_n' V_{OV1}^2} = \frac{100 \times 10^{-6}}{\frac{1}{2} \times 246.2 \times 10^{-6} \times 0.21^2} \simeq 18.42$$

**Example MS.7.1** *continued*

where, as mentioned, $L_{\text{eff}} = 0.180\ \mu\text{m}$, and similar to Example MS.5.1, $k_n' = 246.2\ \mu\text{A/V}^2$. This yields $W_1 = 18.42\ L_{eff} = 3.32\ \mu\text{m}$. To specify the dimensions of the MOSFETs in Multisim, we will use the multiplicative factor $m$; its default value is 1, and it is used in SPICE to specify the number of MOSFETs connected in parallel. As depicted in Fig. B.79, a transistor with channel length $L$ and channel width $m \times W$ can be implemented using $m$ narrower transistors in parallel, each having a channel length $L$ and a channel width $W$. In this example, a unit-size NMOS transistor is used with $W_1/L_1 = 0.52\mu\text{m}/0.2\mu\text{m}$. Thus, we find $m_1 = 3.32/0.52 \simeq 6$.

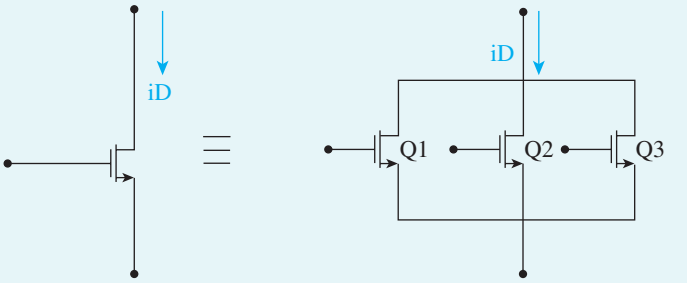



**Figure B.79** Transistor equivalency.

Furthermore, MOSFETs 2 and 3 must be sized to have reasonably small $V_{OV}$ for the bias current $I_D$ of 100 μA. This allows large signal-swing at the output of the amplifier. Similar to our previous approach, by choosing $|V_{OV2}| = 0.3$ V, and noting $|D_{DS,2}| \simeq (V_{DD}/2) = 0.9$V (mid–rail voltage):

$$\frac{W_2}{L_{\text{eff}}} = \frac{I_D}{\frac{1}{2}|k_p'|V_{OV2}^2(1 + |\lambda_2||V_{DS,2}|)} = \frac{100 \times 10^{-6}}{\frac{1}{2} \times 86.1 \times 10^{-6} \times 0.3^2 \times (1 + 0.11 \times 0.9)} \simeq 23.5$$

where $L_{eff} = 0.18\ \mu\text{m}$ and $|k_p'| = 86.1\mu\text{A/V}^2$. This yields $W_2 = 23.5 \times L_{\text{eff}} = 4.23\mu\text{m}$. In this example, unit-size PMOS transistors are used with $W_2/L_2 = W_3/L_3 = 0.46\mu\text{m}/0.2\mu\text{m}$. Thus, we find $m_2 = m_3 = 4.23/0.46 \simeq 9$.

## Simulation

**Amplifier Biasing** Now our design can be verified using the simulation tool. The schematic is in Ch7_CMOS_CS_Amplifier_ Ex_VTC.ms10. Based on the simulation results, $|G_v| = 54$ V/V and $I_D = 101\ \mu\text{A}$. Therefore, the simulation results confirm that the designed CMOS CS amplifier meets the specifications.

**DC Voltage Transfer Characteristic** To compute the dc transfer characteristic of the CS amplifier, we perform a dc analysis in Multisim with $V_{\text{IN}}$ swept over the range 0 to $V_{DD}$ and plot the corresponding output voltage $V_{\text{OUT}}$.

Figure B.80(a) shows the resulting transfer characteristic. The slope of the VTC curve at $V_{GSI} = 0.71$ V corresponds to the desired gain of the amplifier. To examine the high-gain region more closely, we repeat the dc sweep for $V_{\text{IN}}$ between 0.6 V and 0.8 V. The resulting transfer characteristic is plotted in Fig. B.80b (middle curve). Using the cursor of the Grapher in Multisim, we find that the linear region of this dc transfer characteristic is bounded approximately by $V_{\text{IN}} = 0.698$ V and $V_{\text{IN}} = 0.721$ V. The corresponding values of $V_{\text{OUT}}$ are 1.513 V and 0.237 V. These results are close to the expected values. Specifically, transistors $Q_1$

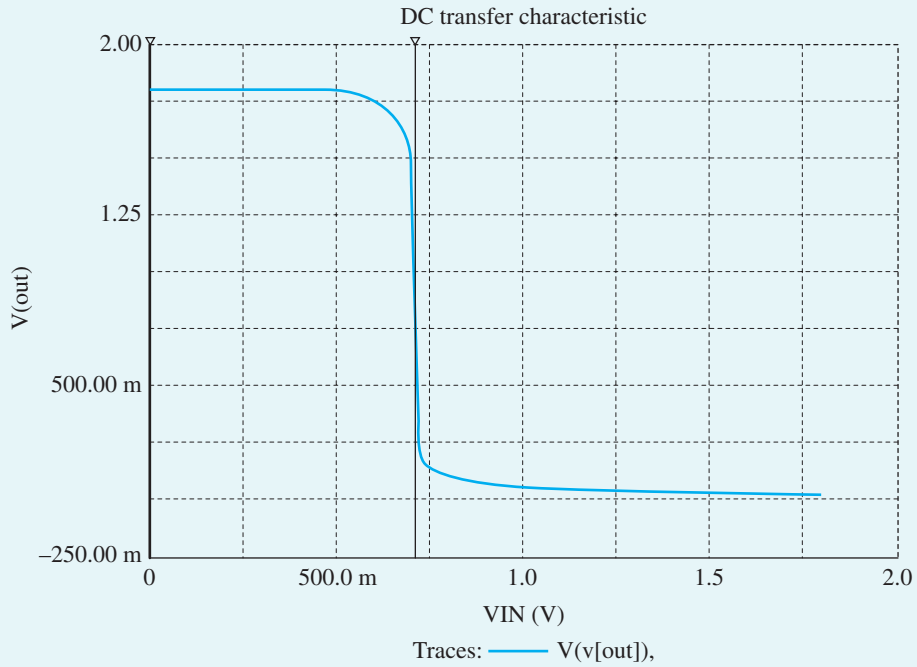



**Figure B.80** **(a)** Voltage transfer characteristic of the CMOS CS amplifier.

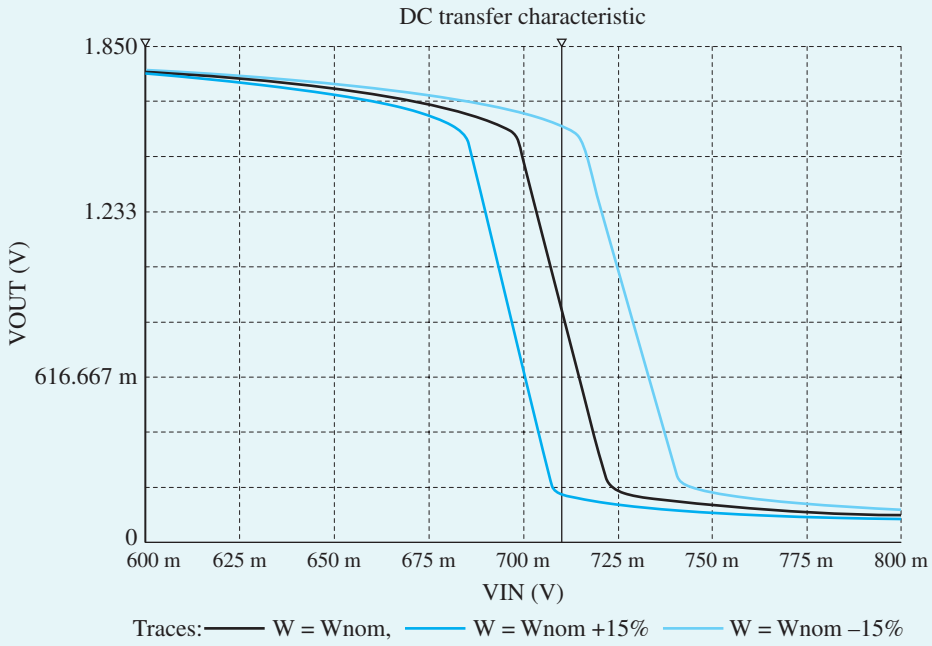



**Figure B.80** **(b)** Expanded view of the transfer characteristics in the high-gain region for $W = W_{\text{nominal}} \pm 15\%$.

**Example MS.7.1** *continued*

and $Q_2$ will remain in the saturation region and, hence, the amplifier will operate in its linear region if $V_{OV1} \le V_{OUT} \le V_{DD} - |V_{OV2}|$ or $0.21\text{V} \le V_{OUT} \le 1.5$ V. From the results above, the voltage gain $G_v$ (i.e., the slope of the linear segment of the dc transfer characteristic) is approximately –54 V/V, which exceeds but is reasonably close to the targeted gain.

Note, from the dc transfer characteristic in Fig. 80(b), that for an input dc bias of $V_{IN} = 0.710$ V, the output dc bias is $V_{OUT} = 0.871$ V. This choice of $V_{IN}$ maximizes the available signal swing at the output by setting $V_{OUT}$ at approximately the middle of the linear segment of the dc transfer characteristic.

**Using Transient Analysis to Verify $G_v$** This can be done by conducting transient response analysis, as set up in Ch7_CMOS_CS_Amplifier_ Ex_gain.ms10. As can be seen from Fig. B.81, $|G_v| \simeq |A_v| \simeq$ 54 V/V.

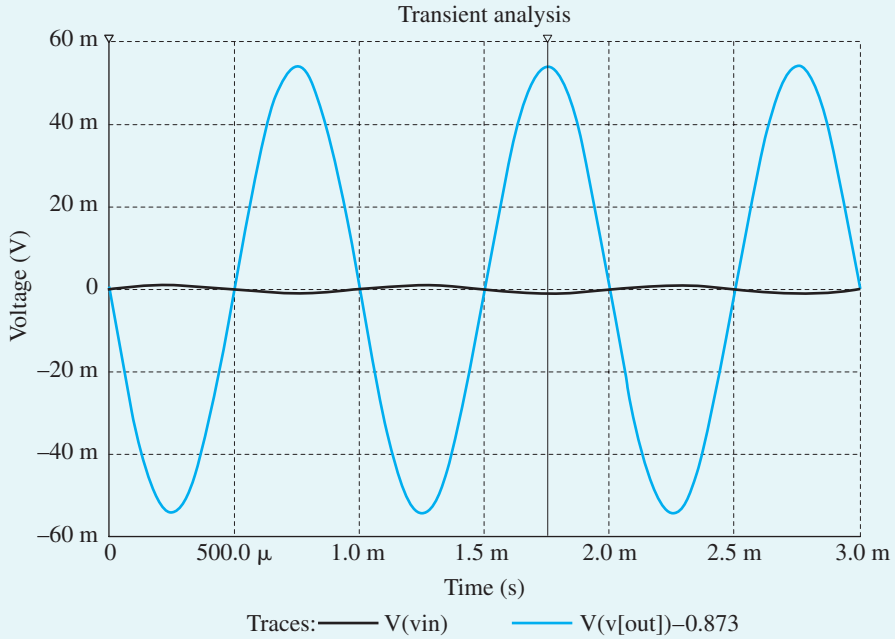



**Figure B.81** $G_v$ of the CMOS CS amplifier (transient analysis).

**Sensitivity to Process Variations** Because of the high resistance at the output node (or, equivalently, because of the high voltage gain), the value of $V_{OUT}$ is highly sensitive to the effect of process and temperature variations on the characteristics of the transistors. To illustrate this point, consider what happens when the width of $Q_1$ (i.e., $W_1$) changes by ±15%. The corresponding dc transfer characteristics are shown in Fig. B.80(b). Accordingly, when $V_{IN} = 0.71$ V, $V_{OUT}$ will drop to 0.180 V if $W_1$ increases by 15%, and will rise to 1.556 V if $W_1$ decreases by 15%. In practical circuit implementations, this problem is alleviated by using negative feedback to accurately set the dc bias voltage at the output of the amplifier and, hence, to reduce the sensitivity of the circuit to process variations. We studied the topic of negative feedback in Chapter 9.

## Example MS.7.2

### The Folded-Cascode Amplifier

In this example, we will use Multisim to design the folded-cascode amplifier whose schematic capture is shown in Fig. B.82. We will assume a 0.18-μm CMOS technology for the MOSFET and use typical SPICE level-1 model parameters for this technology, excluding the intrinsic capacitance values. We will begin with an approximate hand-analysis design. We will then use Multisim to verify that the designed circuit meets the specifications. The targeted specifications for this folded-cascode amplifier are a dc gain $|G_v| = 100$ V/V and a bias current $I_D$ of 100 μA. Note that while this design does not provide a very high gain, its bandwidth is large (see Chapter 8).

The amplifier specifications are summarized in Table B.19.

| NMOS | |
|---|---|
| Vtn | 0.5 V |
| \|VAn\| | 12.5 V |
| kn' | 246.2uA/V^2 |
| IREF | 0.1 mA |
| L | 0.2 um |
| W | 0.48 um |

| PMOS | |
|---|---|
| Vtp | –0.5 V |
| \|VAp\| | 9V |
| kp' | –86.1 μA/V^2 |
| IREF | 0.1 mA |
| L | 0.2 um |
| W | 0.64 um |

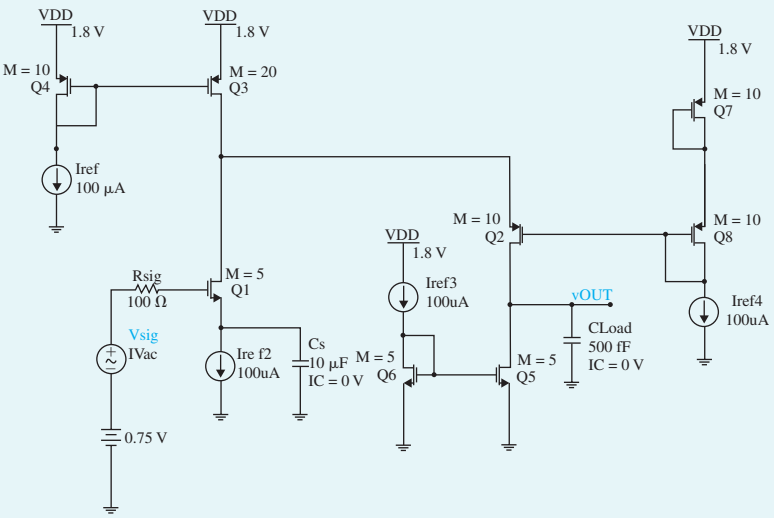



**Figure B.82** Schematic capture of the folded-cascode amplifier.

**Table B.19** Folded-Cascode Amplifier Specifications

| Parameters | Value |
|---|---|
| $I_D$ | 100 μA |
| $\|G_v\|$ | 100 V/V |
| $V_{DD}$ | 1.8 V |

### Hand Design

For the design of this amplifier we choose $L = 200$ μm, so we have $L_{\text{eff}} = 180$ μm. For this channel length, and in 0.18-μm CMOS technology, the magnitudes of the Early voltages of the NMOS and PMOS transistors are $V_{An} = 12.5$ V and $|V_{Ap}| = 9$ V, respectively.

The folded-cascode amplifier in Fig. B.82 is equivalent to the one in Fig. 6.16, except that a current source is placed in the source of the input transistor $Q_1$ (for the same dc-biasing purpose as in the case of the CS amplifier). Note that in Fig. B.82, the PMOS current mirror $Q_3$–$Q_4$ and the NMOS current mirror $Q_5$–$Q_6$ are used to realize, respectively, current sources $I_1$ and $I_2$ in the circuit of Fig. 6.16. Furthermore, the current transfer ratio of mirror $Q_3$–$Q_4$ is set to 2 (i.e., $m_3/m_4 = 2$). This results in $I_{D3} \simeq 2I_{\text{ref}}$. Hence, transistor $Q_2$ is biased at $I_{D2} - I_{D3} - I_{D1} = I_{\text{ref}}$.

**Example MS.7.2** *continued*

The overall dc voltage gain of the folded-cascode amplifier under design can be expressed by using Eq. (6.22) as

$$G_v = -g_{m1}R_{\text{out}}$$

where

$$R_{\text{out}} = R_{\text{out2}} \parallel R_{\text{out5}}$$

is the output resistance of the amplifier. Here, $R_{\text{out2}}$ is the resistance seen looking into the drain of the cascode transistor $Q_2$, while $R_{\text{out5}}$ is the resistance seen looking into the drain of the current mirror transistor $Q_5$. Using Eq. (6.25), we have

$$R_{\text{out2}} \simeq (g_{m2}r_{o2})R_{S2}$$

where

$$R_{S2} = (r_{o1} \parallel r_{o3})$$

is the effective resistance at the source of $Q_2$. Furthermore,

$$R_{\text{out5}} = r_{o5}$$

Thus, for the folded-cascode amplifier in Fig. B.82,

$$R_{\text{out}} \simeq r_{o5}$$

and

$$G_v = -g_{m1}r_{o5} = -2\frac{V_{An}}{V_{OV1}}$$

Therefore, based on the given information, the value of $V_{OV1}$ can be determined:

$$V_{ov1} = 2\frac{V_{An}}{|G_v|} = 2\frac{12.5}{100} = 0.25\text{V}$$

The gate bias voltage of transistor $Q_2$ is generated using the diode-connected transistors $Q_7$ and $Q_8$. The size and drain currents of these transistors are set equal to those of transistor $Q_2$. Therefore, ignoring the body effect,

$$V_{G,2} = V_{DD} - V_{SG,7} - V_{SG,8} = V_{DD} - 2(|V_{tp}| + |V_{OV,P}|)$$

where $V_{OV,P}$ is the overdrive voltage of the PMOS transistors in the amplifier circuit. Thus, such a biasing configuration results in $V_{SG,2} = |V_{tp}| + |V_{OV,P}| = 0.5 + 0.25 = 0.75V$ as desired, while setting $V_{SD,3} = |V_{tp}| + |V_{OV,P}| = 0.75V$ to improve the bias matching between $Q_3$ and $Q_4$. For this example, all transistors are sized for an overdrive voltage of 0.25 V. Also, to simplify the design procedure, we ignore the channel-length modulation effect. As a result, using unit-size NMOS transistors with $W_n/L_n = 0.48\ \mu\text{m}/0.2\ \mu\text{m}$, and unit-size PMOS transistors with $W_p/L_p = 0.64\ \mu\text{m}/0.2\ \mu\text{m}$, the corresponding multiplicative factor $m$ for each transistor can be calculated by rounding to the nearest integer the value of $m$:

$$m = \frac{I_D}{\frac{1}{2}k'\left(\frac{W}{L_{\text{eff}}}\right)V_{OV}^2}$$

Table B.20 summarizes the relevant design information and the calculated $m$ values for each transistor.

**Table B.20** Transistor Sizes

| Transistor | $I_D$ (μA) | $V_{OV}$ (V) | $W$ (μm) | $L_{\text{eff}}$ (μm) | $K$ (μA/V$^2$) | $m$ |
|---|---|---|---|---|---|---|
| 1 | 100 | 0.25 | 0.48 | 0.18 | 246.2 | 5 |
| 2 | 100 | 0.25 | 0.64 | 0.18 | 86.1 | 10 |
| 3 | 200 | 0.25 | 0.64 | 0.18 | 86.1 | 20 |
| 4 | 100 | 0.25 | 0.64 | 0.18 | 86.1 | 10 |
| 5 | 100 | 0.25 | 0.48 | 0.18 | 246.2 | 5 |
| 6 | 100 | 0.25 | 0.48 | 0.18 | 246.2 | 5 |
| 7 | 100 | 0.25 | 0.64 | 0.18 | 86.1 | 10 |
| 8 | 100 | 0.25 | 0.64 | 0.18 | 86.1 | 10 |

## Simulation

**Verifying $G_v$** Now our design can be verified by reading probes or conducting transient response analysis, as set up in Ch7_Folded_Cascode _ Ex.ms10. Based on the simulation results, $|G_v| = 102$ V/V (Fig B.83) and $I_{D1} = I_{D2} = 100$ μA. Therefore, the simulation results confirm that the designed folded-cascode amplifier meets the specifications.

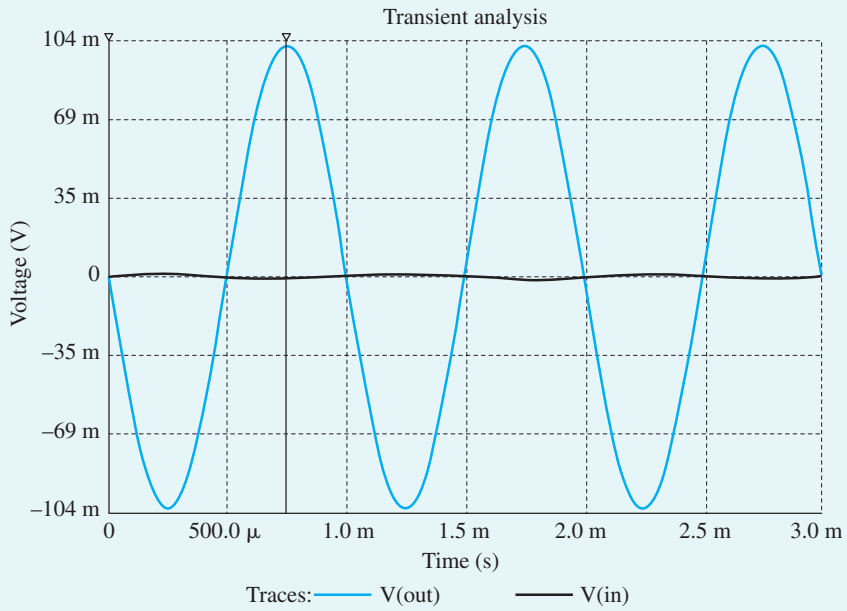



**Figure B.83** $G_v$ of the folded-cascode amplifier (transient analysis).

**Sensitivity to Channel Length Modulation** In the hand design of this example, the channel-length modulation effect was ignored (except for the role of $r_{o5}$ in determining the gain). However, the simulation took the finite $r_o$ of each transistor into account. Furthermore, one can investigate the effect of changes in the Early voltages by modifying the value of lambda for each transistor in the design.

## Example MS.8.1

### The Two-Stage CMOS Op Amp

In this example, we will design the two-stage CMOS op amp whose schematic capture is shown in Fig. B.84. Once designed, the circuit's characteristics, such as the input common-mode range, the common-mode rejection ratio, the output-voltage range, and the input offset voltage will be evaluated.

The first stage is differential pair $Q_1$–$Q_2$ (which is actively loaded with the current mirror formed by $Q_3$ and $Q_4$), with bias current supplied by the current mirror formed by $Q_8$, and $Q_5$, which utilizes the reference bias current $I_{REF}$. The second stage consists of $Q_6$, which is a common-source amplifier actively loaded with the current source transistor $Q_7$.

For the design of this CMOS op amp, we will assume a 0.18-µm CMOS technology for the MOSFETs and use typical SPICE level-1 model parameters for this technology, excluding the intrinsic capacitance values. We will begin with an approximate hand-analysis design. We will then use Multisim to verify that the implemented circuit meets the specifications. The targeted specifications for this op amp are a dc open-loop voltage gain $|A_v|$ = 2500 V/V, with each of transistors $Q_1$, $Q_2$, $Q_3$, and $Q_4$ conducting a drain current of 100 µA.

| NMOS | |
|---|---|
| Vtn | 0.5 V |
| \|VAn\| | 12.5V |
| kn' | 246.2µA/V^2 |
| IREF | 0.2mA |
| L | 0.2 um |
| W | 0.48 um |

| PMOS | |
|---|---|
| Vtp | –0.5 V |
| \|VAp\| | 9V |
| kp' | –86.1 µA/V^2 |
| IREF | 0.1mA |
| L | 0.2 um |
| W | 0.64 um |

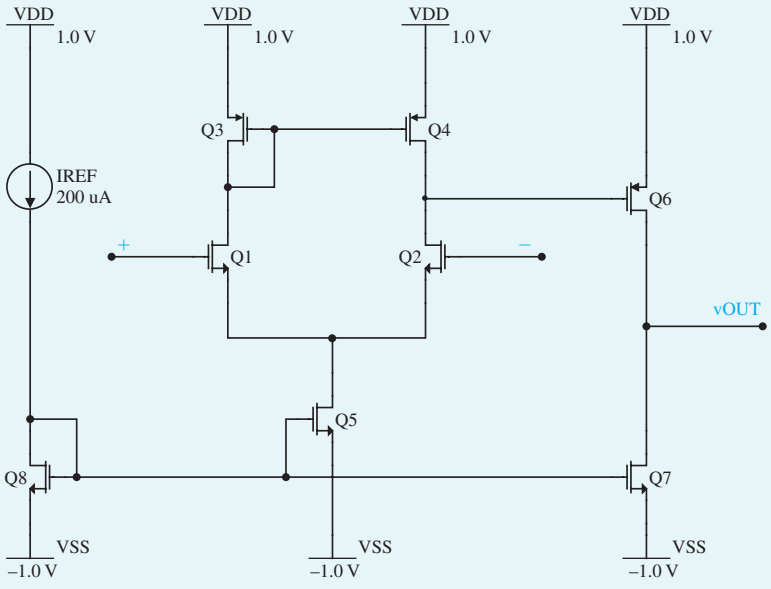



**Figure B.84** Schematic capture of the two-stage CMOS op amp.

To achieve the targeted specifications, a biasing current $I_{REF}$ = 200 µA is used, and the transistors $Q_5$, $Q_6$, $Q_7$, and $Q_8$ will be sized so that they conduct the drain current of 200 µA. Also, the open-loop voltage gain for this design is the product of the voltage gains of the two stages. Accordingly, each stage is designed to contribute a voltage gain of –50 V/V, so as to achieve the specified open-loop voltage gain.

The amplifier specifications are summarized in Table B.21.

**Table B.21** Two-Stage CMOS Op-Amp Specifications

| Parameter | Value |
|---|---|
| $I_{(Q1, Q2, Q3, \text{and } Q4)}$ | 100 µA |
| $I_{(Q5, Q6, Q7, \text{and } Q8)}$ | 200 µA |
| $\lvert A_1 \rvert$ | 50 V/V |
| $\lvert A_2 \rvert$ | 50 V/V |
| $V_{DD}$ | 1 V |
| $V_{SS}$ | –1 V |

**Hand Design** For the design of this amplifier we choose $L = 0.200$ µm, so we have $L_{\text{eff}} = 0.180$ µm. For this channel length, and in 0.18-µm CMOS technology, the magnitudes of the Early voltages of the NMOS and PMOS transistors are $V_{An} = 12.5$ V and $|V_{Ap}| = 9$ V.

The two-stage CMOS op amp in Fig. B.84 is equivalent to the one in Fig. 7.41, except that the first stage is an NMOS differential amplifier and the second stage is a PMOS common source. Note that the differential voltage gain of the first stage can be expressed using Eq. (7.176) as:

$$A_1 = -g_{m1}(r_{o2} \parallel r_{o4})$$

Hence,

$$A_1 = -\frac{2}{V_{OV1}}\left(\frac{V_{An}|V_{Ap}|}{V_{An} + |V_{Ap}|}\right)$$

resulting in

$$V_{OV1} = -\frac{2}{A_1}\left(\frac{V_{An}|V_{Ap}|}{V_{An} + |V_{Ap}|}\right) = -\frac{2}{(-50)}\left(\frac{12.5 \times 9}{12.5 + 9}\right) \simeq 0.21\text{V}$$

Also, the voltage gain of the second stage is provided by Eq. (7.177) as

$$A_2 = -g_{m6}(r_{o6} \parallel r_{o7})$$

Therefore,

$$A_2 = -\frac{2}{V_{OV6}}\left(\frac{V_{An}|V_{Ap}|}{V_{An} + |V_{Ap}|}\right)$$

resulting in

$$V_{OV6} = -\frac{2}{A_2}\left(\frac{V_{An}|V_{Ap}|}{V_{An} + |V_{Ap}|}\right) = -\frac{2}{(-50)}\left(\frac{12.5 \times 9}{12.5 + 9}\right) \simeq 0.21\text{V}$$

For this example, all transistors are sized for an overdrive voltage of 0.21 V. Furthermore, to simplify the design procedure, we ignore the channel-length modulation effect. As a result, using unit-size NMOS transistors with $W_n/L_n = 0.64\,\mu\text{m}/0.2\,\mu\text{m}$, and unit-size PMOS transistors with $W_n/L_n = 0.48\mu\text{m}/0.2\mu\text{m}$, the corresponding multiplicative factor $m$ for each transistor can be calculated by rounding to the nearest integer value which is calculated as $m$:

$$m = \frac{I_D}{\frac{1}{2}k'\left(\frac{W}{L_{\text{eff}}}\right)V_{OV}^2}$$

Table B.22 summarizes the relevant information and the calculated $m$ values for each transistor.

**Example MS.8.1** *continued*

**Table B.22** Transistor Sizes

| Transistor | $I_D$ (μA) | $V_{OV}$ (V) | $W$ (μm) | $L_{\text{eff}}$ (μm) | k′ (μA/V²) | $m$ |
|---|---|---|---|---|---|---|
| 1 | 100 | 0.21 | 0.48 | 0.18 | 246.2 | 7 |
| 2 | 100 | 0.21 | 0.48 | 0.18 | 246.2 | 7 |
| 3 | 100 | 0.21 | 0.64 | 0.18 | 86.1 | 15 |
| 4 | 100 | 0.21 | 0.64 | 0.18 | 86.1 | 15 |
| 5 | 200 | 0.21 | 0.48 | 0.18 | 246.2 | 14 |
| 6 | 200 | 0.21 | 0.64 | 0.18 | 86.1 | 30 |
| 7 | 200 | 0.21 | 0.48 | 0.18 | 246.2 | 14 |
| 8 | 200 | 0.21 | 0.48 | 0.18 | 246.2 | 14 |

## Simulation

**Verifying $A_v$** Now our design can be verified by reading probes, as set up in Ch8_ Two_Stage_Op_ Amp_Ex.ms10. Based on the simulation results we read $|A_1| = 57$ V/V, $|A_2| = 58.6$ V/V, $|A_v| = 3340$ V/V, $I_{(Q1,\ Q2,\ Q3,\ \text{and}\ Q4)} = 97$ μA, $I_{Q5} = 194$ μA, $I_{(Q6,\ Q7)} = 202$ μA, and $I_{Q8} = 200$ μA. These values are somewhat different from the targeted specifications. The deviations can be attributed to the fact that we rounded the values of $m$ to the nearest integer and ignored the effect of channel-length modulation, that is, the term $(1 + \lambda V_{DS})$, when calculating the multiplicative factor. To get closer to our targeted specifications, we may use the obtained $V_{DS}$ values for each transistor, from the original design, to estimate new multiplicative factor values by taking the term $(1 + \lambda V_{DS})$ into account. Table B.23 shows the revised multiplicative factor values.

**Table B.23** Revised Transistor Multiplicative Factors

| Transistor | $m$ |
|---|---|
| 1 | 6 |
| 2 | 6 |
| 3 | 14 |
| 4 | 14 |
| 5 | 13 |
| 6 | 26 |
| 7 | 13 |
| 8 | 13 |

The revised design is evaluated by reading probes, as set up in Ch8_Two_Stage_Op_Amp_revised_ Ex.ms10. The simulation results show $|A_1| = 54$ V/V, $|A_2| = 58.2$ V/V, $|A_v| = 3145$ V/V, $I_{(Q1,\ Q2,\ Q3,\ \text{and}\ Q4)} = 103$ μA, $I_{Q5} = 206$ μA, $I_{(Q6,\ Q7)} = 205$ μA, and $I_{Q8} = 200$ μA, from which we see that the voltage gains are closer to the targeted specifications.

One should note that the discrepancies between the hand-design and simulation results in this simulation example are more apparent because errors in each stage add up.

Next, we will explore some important characteristics of the designed two-stage CMOS op amp.

**Input Common-Mode Range** The upper limit of the input common-mode range is the value of input voltage at which $Q_1$ and $Q_2$ leave the saturation region. This occurs when the input voltage exceeds

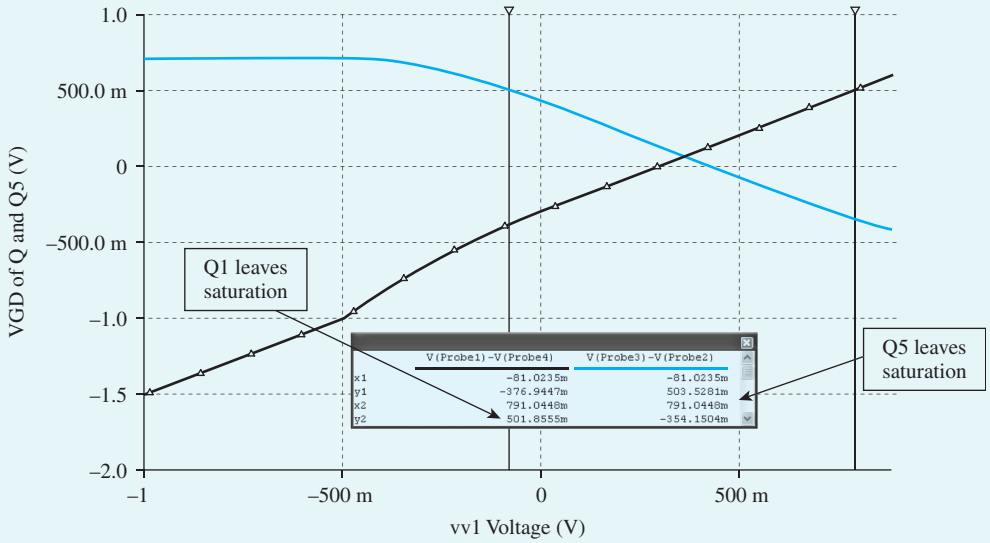



**Figure B.85** Input common–mode range of the two-stage CMOS op amp.

the drain voltage of $Q_1$ by $V_{tn} = 0.5$ V. Since the drain of $Q_1$ is at $1 - (0.21 + 0.5) = 0.29$ V, then the upper limit of the input common-mode range is $v_{ICM\max} = 0.29 + 0.5 = 0.79\text{V}$.

The lower limit of the input common-mode range is the value of input voltage at which $Q_5$ leaves the saturation region. Since for $Q_5$ to operate in saturation the voltage across it (i.e., $V_{DS5}$) should at least be equal to the overdrive voltage at which it is operating (i.e., 0.21 V), the highest voltage permitted at the drain of $Q_5$ should be –0.79 V. It follows that the lowest value of $v_{ICM}$ should be $v_{ICM\min} = -0.08$ V.

To verify the results using the simulation tool, we swept the input common-mode voltage $v_{\text{ICM}}$ from –1 V to 1 V and plotted the resulting $v_{GD}$ of $Q_1$ and $Q_5$ (as set up in Ch8_Two_Stage_Op_Amp_Ex_CM_Range.ms10). As can be seen from Fig. B.85, both transistors $Q_1$ and $Q_5$ stay in saturation for the input common-mode range of $-0.08\ \text{V} \le v_{ICM} \le 0.79\ \text{V}$, as indicated by cursors.

**Common-Mode Rejection Ratio (CMRR) of the First Stage** The value of the CMRR of the first stage (the active-loaded MOS differential amplifier) is determined from Eq. B.147. Note that the value of $R_{SS}$ in the provided equation corresponds to the output resistance of $Q_5$ (i.e., $r_{o5}$). Thus,

$$\text{CMRR} \equiv \frac{|A_1|}{|A_{cm}|} = \frac{50}{1/2g_{m3}r_{o5}} = 100g_{m3}r_{o5} = 100\frac{2\times 100\times 10^{-6}}{0.21}\frac{12.5}{200\times 10^{-6}} = 5952.4 = 75.5\ \text{dB}$$

Using the simulation tool, the value of CMRR is calculated by dividing the previously obtained $A_1$ value (54 V/V) by the common-mode gain of the first stage as measured in Ch8_Two_Stage_Op_Amp_Ex_CMRR.ms10. This yields

$$\text{CMRR} \equiv \frac{|A_1|}{|A_{cm}|} = \frac{54}{78\times 10^{-3}} = 6923 = 76.8\ \text{dB}$$

**Output Voltage Range** The lowest allowable output voltage is the value at which $Q_7$ leaves the saturation region, which is $-V_{SS} + V_{OV7} = -1 + 0.21 = 0.79$ V. The highest allowable output voltage is the value at which $Q_6$ leaves saturation, which is $V_{DD} - |-V_{OV6}| = 1 - 0.21 = 0.79$ V. Thus, the output-voltage range is –0.79 V to 0.79 V.

As set up in Ch8_Two_Stage_Op_Amp_Ex_Output_Range.ms10, to verify the calculated output voltage range, we swept the input voltage from –2 mV to 2 mV (we used a small input voltage due to high

**Example MS.8.1** *continued*

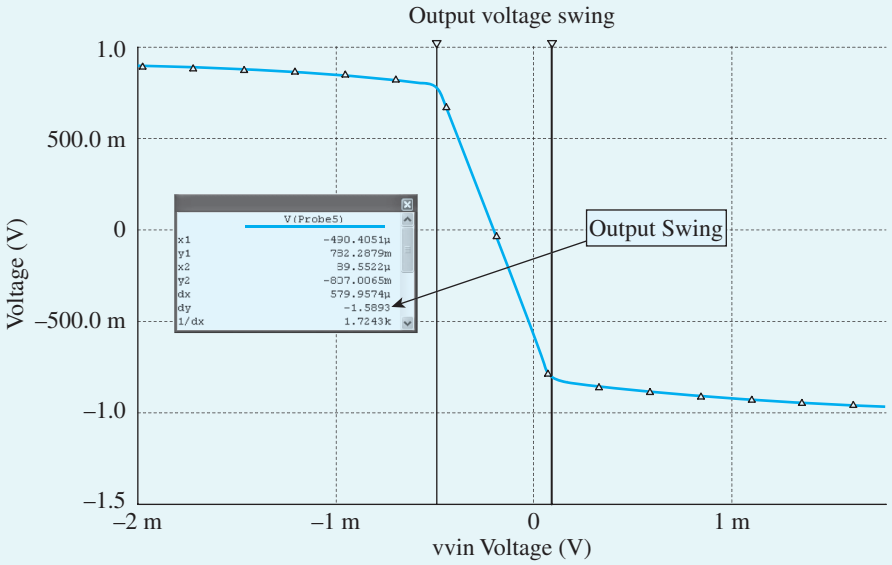



**Figure B.86** Output-voltage range of the two-stage CMOS op amp.

gain). As can be seen from Fig. B.86, the output level changes from –0.795 V to 0.784 V, a rather symmetrical range. Therefore, the simulation results confirm our hand-analysis calculations.

**Input Offset Voltage** Although, theoretically, there should be no systematic offset, we do observe an output offset voltage $V_o$. As defined by Eq. 7.102, the input offset voltage, $V_{OS}$, can be obtained as

$$V_{OS} = \frac{V_O}{A_v}$$

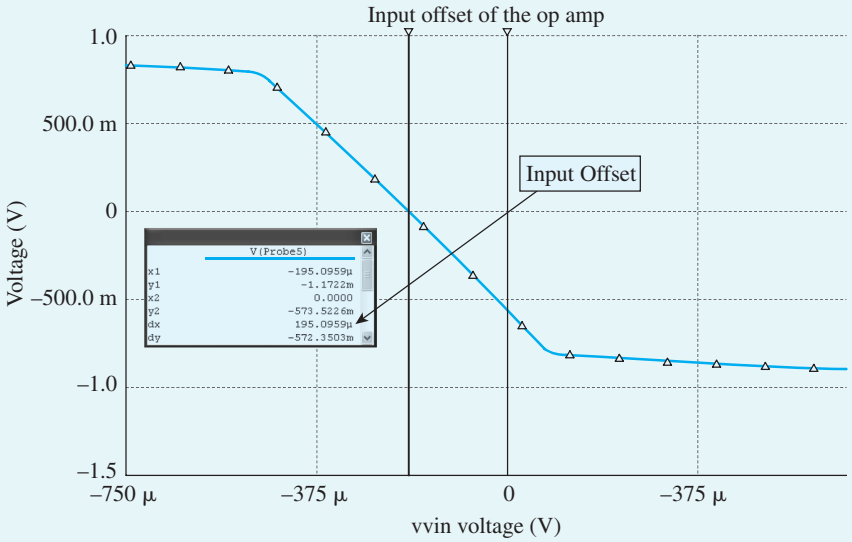



**Figure B.87** Input offset voltage of the two-stage CMOS op amp.

Equivalently, if we apply a voltage $-V_{OS}$ between the input terminals of the differential amplifier, the output voltage should be reduced to zero. This equivalency can be verified using the simulation tool (Ch8_Two_Stage_Op_Amp_Ex_Output_Range.ms10). When both the input terminals are grounded, the probe at the output reads the dc voltage 0.574 V. Also, when we apply the voltage $V_{OS} = (0.574/3145) \simeq 183\,\mu V$, between the input terminals, the output voltage is reduced to zero (Fig. B.87). Hence, the op amp has an input offset voltage of $V_{OS} = 195\ \mu V$, which approximately corresponds to an output offset voltage of $V_O = 0.574$ V.

## Example MS.9.1

### Frequency Response of the Discrete CS Amplifier

In this example, we will investigate the frequency response of the CS amplifier of Example MS.5.1. By using Multisim to perform "ac analysis" on the designed CS amplifier, we are able to measure the mid-band gain $A_M$ and the 3-dB frequencies $f_L$ and $f_H$, and to plot the output-voltage magnitude (in dB) versus frequency. Figure B.88 shows the schematic capture of the CS amplifier.

| DEVICE PARAMETERS | |
|---|---|
| NAME | Q1:NMOS |
| W | 15.48u |
| L | 0.2u |
| KP | 246u |
| LD | 0.01u |
| VT0 | 0.45 |
| LAMBDA | 0.08 |
| GAMMA | 0.3 |

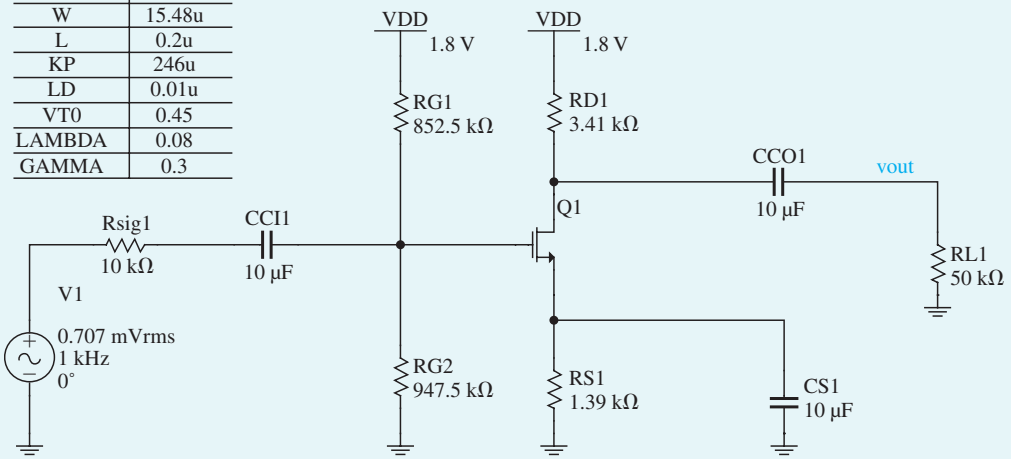



**Figure B.88** Schematic capture of discrete CS amplifier.

### Hand Analysis

**Midband Gain** The midband gain of this CS amplifier can be determined using Eq. (8.9) as follows:

$$A_M = \frac{R_{in}}{R_{in} + R_{sig}}[g_m(R_D \| R_L)]$$

$$R_{in} = (R_{G1} \| R_{G2}) = 852.5 \times 10^3 \| 947.5 \times 10^3 = 448.75 \times 10^3\,\Omega$$

$$g_m = 3.33\ \text{mA/V}$$

$$A_M = \frac{448.75 \times 10^3}{448.75 \times 10^3 + 10 \times 10^3}[3.33 \times 10^{-3}(3.41 \times 10^3 \| 50 \times 10^3)] \simeq 10\ \text{V/V}$$

**Example MS.9.1** *continued*

**Low-Frequency Poles and Zero** We know from Section 8.1.1 that the low-frequency poles are as follows:

$$f_{P1} = \frac{1}{2\pi \times C_{CI}(R_{\text{sig}} + R_{\text{in}})} = \frac{1}{2\pi \times 10 \times 10^{-6}[(10 \times 10^{3}) + 448.75 \times 10^{3}]}$$

$$f_{P1} = 0.0347 \text{ Hz}$$

$$f_{P2} = \frac{1}{2\pi \times C_{CO}(R_D + R_L)} = \frac{1}{2\pi \times 10 \times 10^{-6}(3.41 \times 10^{3}) + (50 \times 10^{3})}$$

$$f_{P2} = 0.30 \text{ Hz}$$

$$f_{P3} = \frac{1}{2\pi \times C_S}\left(g_m + \frac{1}{R_S}\right) = \frac{1}{2\pi \times 10 \times 10^{-6}}\left[(3.33 \times 10^{-3}) + \frac{1}{1.39 \times 10^{3}}\right]$$

$$f_{P3} = 64.4 \text{ Hz}$$

And the location of the real transmission zero is determined as

$$f_Z = \frac{1}{2\pi \times C_S R_S} = \frac{1}{2\pi \times (10 \times 10^{-6})(1.39 \times 10^{3})}$$

$$f_Z = 11.45 \text{ Hz}$$

Upon observing the relative magnitude of each of the poles, we can conclude that $f_{P3}$ will determine $f_L$, the lower 3-dB frequency of the amplifier gain,

$$f_L \simeq f_{P3} \simeq 11.45 \text{ Hz}$$

**High-Frequency Rolloff** The high-frequency rolloff of the amplifier gain is caused by the MOSFET internal capacitance. The typical values for 0.180 μm CMOS technology are given in Table B.4. We know from Eq. (8.54) in Section 8.3.1 that

$$f_H = \frac{1}{2\pi \times C_{\text{in}} R'_{\text{sig}}}$$

$$R'_{\text{sig}} = 10 \times 10^{3} \| 448.75 \times 10^{3} = 9.78 \times 10^{3}$$

$$C_{\text{in}} = W\{C_{gs0} + C_{gd0}[1 + g_m(R_L \| R_L)]\}$$

Note that $C_{gs0}$ and $C_{gd0}$ are per-unit-width values provided in the models.

$$C_{\text{in}} = (15.48 \times 10^{-6}) \times (0.3665 \times 10^{-9}) \times [1 + 1 + 3.33 \times 10^{-3}(50 \times 10^{3} \| 3.41 \times 10^{-3})]$$

$$C_{\text{in}} = 0.716 \text{ fF}$$

$$f_H = \frac{1}{2\pi \times 0.716 \times 10^{-15} \times 9.78 \times 10^{3}}$$

$$f_H \simeq 191 \text{ MHz}$$

Now we can determine the bandwidth, $BW$, of the CS amplifier:

$$BW = f_H - f_L$$

$$BW \simeq f_H = 191 \text{ MHz}$$

## Simulation

Figure B.89 shows the magnitude plot of the frequency response of this CS amplifier.

Based on the simulation results, the midband gain is $A_M$ = 9.80 V/V. Also, $f_L$ = 60.8 Hz and $f_H$ = 192.2 MHz, resulting in 3-dB bandwidth of $BW = f_L - f_H$ = 192.2 MHz. Figure B.89 further shows that

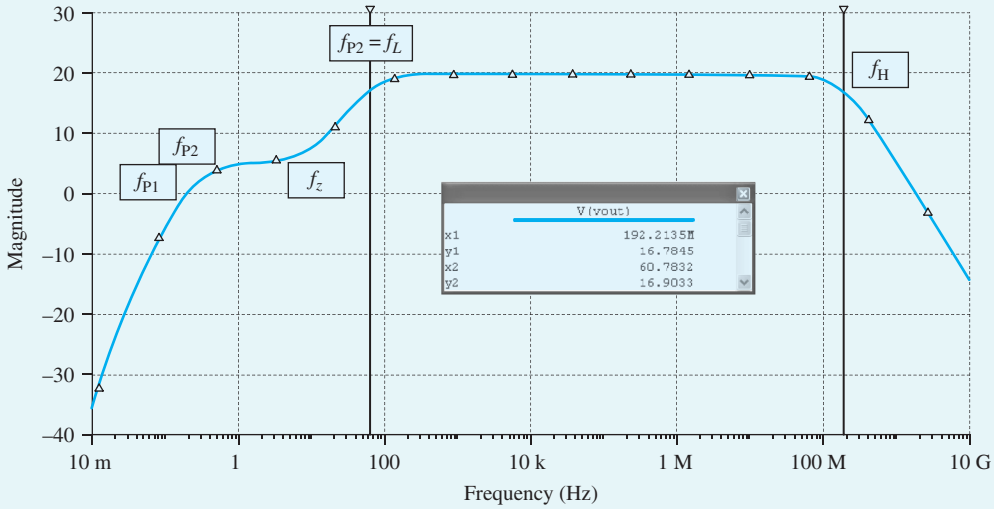



**Figure B.89** Frequency response of the CS amplifier.

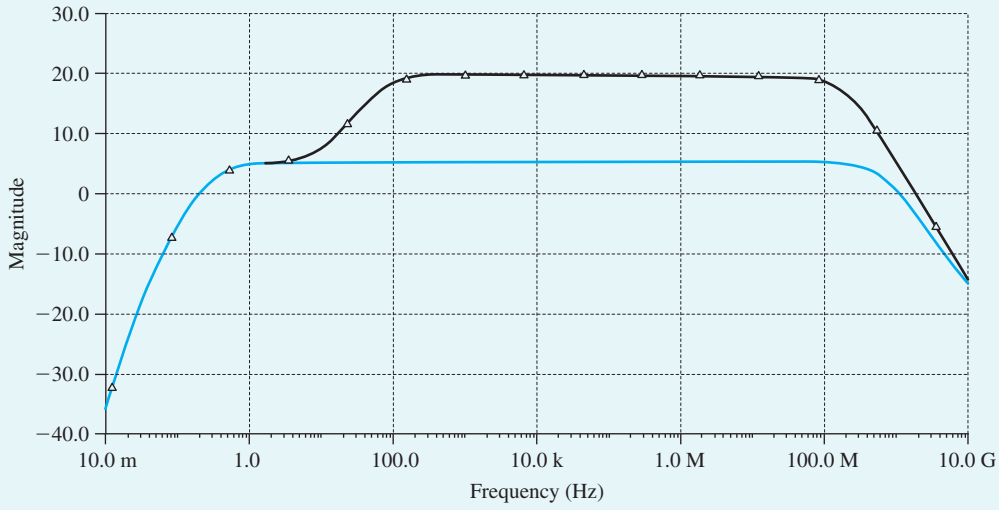



**Figure B.90** Frequency response of the CS amplifier with $C_S = 10$ μF and $C_S = 0$.

(moving toward the left) the gain begins to fall off at about 300 Hz, but flattens out again at about 12.2 Hz. This flattening in the gain at low frequencies is due to a real transmission zero introduced in the transfer function of the amplifier by $R_S$ together with $C_S$, with a frequency $f_Z - = 1/2\pi R_S C_S = 11.45$ Hz. Students are encouraged to investigate this relationship by using the simulation tool to modify the values of $R_S$ and $C_S$ and observing the corresponding change in the zero frequency. Note this value of zero is typically between the break frequencies $f_{P2}$ and $f_{P3}$. The simulation is set up in Ch9 _CS_Amplifier_Ex.ms10.

We can further verify this phenomenon by resimulating the CS amplifier with a $C_S = 0$ (i.e., removing $C_S$) in order to move $f_Z$ to infinity and remove its effect. The corresponding frequency response is plotted in Fig. B.90. As expected with $C_S = 0$, we do not observe any flattening in the low-frequency response of the amplifier. However, because the CS amplifier now includes a source resistor $R_S$, the value of $A_M$ has dropped by a factor of 5.4. This factor is approximately equal to $(1 + g_m R_S)$, as expected from our

**Example MS.9.1** *continued*

study of the CS amplifier with a source-degeneration resistance. Note that the bandwidth $BW$ has increased by approximately the same factor as the drop in gain $A_M$. As we learned in Chapter 9 in our study of negative feedback, the source-degeneration resistor $R_S$ provides negative feedback, which allows us to trade off gain for a wider bandwidth.

## Example MS.9.2

### The Frequency Response of CMOS CS Amplifier and the Folded-Cascode Amplifier

In this example, we will investigate the frequency response of the CMOS CS amplifier and the folded-cascode amplifier studied in Examples MS.7.1 and MS.7.2. The circuit diagram of the CMOS CS amplifier is given in Fig. B.91.

By using Multisim to perform "ac analysis" on the designed CMOS CS amplifier, we are able to measure the midband gain $A_M$ and the 3-dB frequency $f_H$, and to plot the output-voltage magnitude (in dB) versus frequency for two different cases of $R_{sig}$ (100 Ω and 1 MΩ), as shown in Fig. B.92.

Observe that $f_H$ decreases when $R_{sig}$ is increased. This is anticipated from our study of the high-frequency response of the CS amplifier. Specifically, as $R_{sig}$ increases, the pole

$$f_{p,\text{in}} = \frac{1}{2\pi}\frac{1}{R_{sig}C_{in}}$$

formed at the amplifier input will have an increasingly significant effect on the overall frequency response of the amplifier. As a result, the effective time constant $\tau_H$ increases and $f_H$ decreases. When $R_{sig}$ becomes very large, as it is when $R_{sig} = 1$ MΩ, a dominant pole is formed by $R_{sig}$ and $C_{in}$. This results in

$$f_H \simeq f_{p,\text{in}}$$

To estimate $f_{p,\text{in}}$, we need to calculate the input capacitance $C_{in}$ of the amplifier. Using Miller's theorem, we have

$$C_{in} = C_{gs1} + C_{gd1}(1 + g_{m1}R'_L)$$

where

$$R'_L = r_{o1} \parallel r_{o2}$$

The value of $C_{in}$ can be calculated by using the overlap capacitances $C_{gs,ov1}$ and gate-to-channel $C_{gs}$ and $C_{gd,ov1}$ as follows:

$$C_{gs,ov1} = m_1 W_1 CGSO = (5 \times 0.48 \times 10^{-6}) \times (0.3665 \times 10^{-9}) = 0.880 \text{ fF}$$

$$C_{gd,ov1} = m_1 W_1 CGDO = (5 \times 0.48 \times 10^{-6}) \times (0.3665 \times 10^{-9}) = 0.880 \text{ fF}$$

For $C_{gs}$, we write

$$C_{gs\_channel} = \frac{2}{3} m_1 W_1 L C_{ox} = \frac{2}{3}\left[(5 \times 0.48 \times 10^{-6}) \times (0.18 \times 10^{-6})\left(\frac{3.9 \times 8.85 \times 10^{-12}}{4.08 \times 10^{-9}}\right)\right]$$

$$C_{gs\_channel} = 2.48 \text{ fF}$$

$$C_{gs} = 2.48 \text{ fF} + 0.880 \text{ fF} = 3.36 \text{ fF}$$

This results in $C_{in} = 45.78$ fF when $|G_v| = 50$ V/V. Accordingly,

$$f_H \simeq \frac{1}{2\pi}\frac{1}{1 \times 10^6 \times 43.3 \times 10^{-15}} = 3.48 \text{ MHz}$$

which is close to the value computed by Multisim (i.e., $f_H = 3.66$ MHz).

| NMOS | |
|---|---|
| Vtn | 0.5 V |
| \|VAn\| | 12.5V |
| kn' | 246.2uA/V^2 |
| IREF | 0.1mA |
| L | 0.2 um |
| W | 0.48 um |

| PMOS | |
|---|---|
| Vtp | –0.5 V |
| \|VAp\| | 9V |
| kp' | –86.1 uA/V^2 |
| IREF | 0.1mA |
| L | 0.2 um |
| W | 0.64 um |

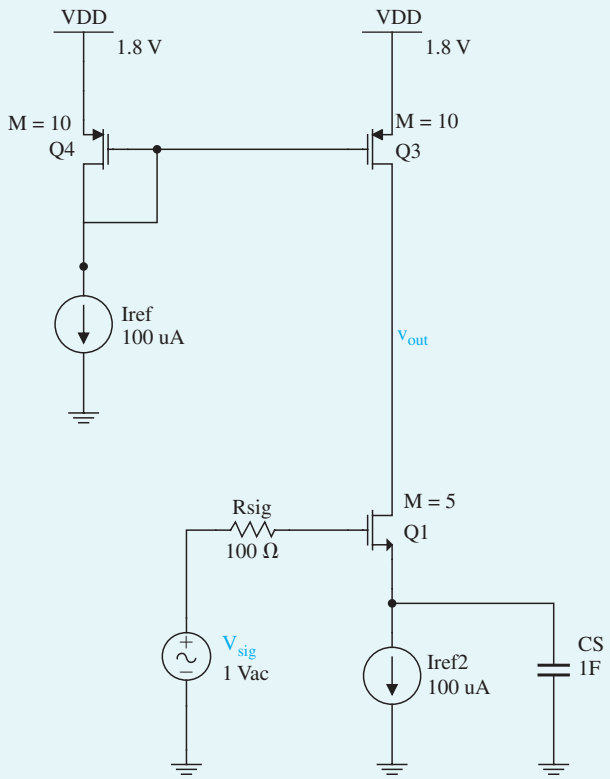



**Figure B.91** Schematic capture of the CMOS CS amplifier.

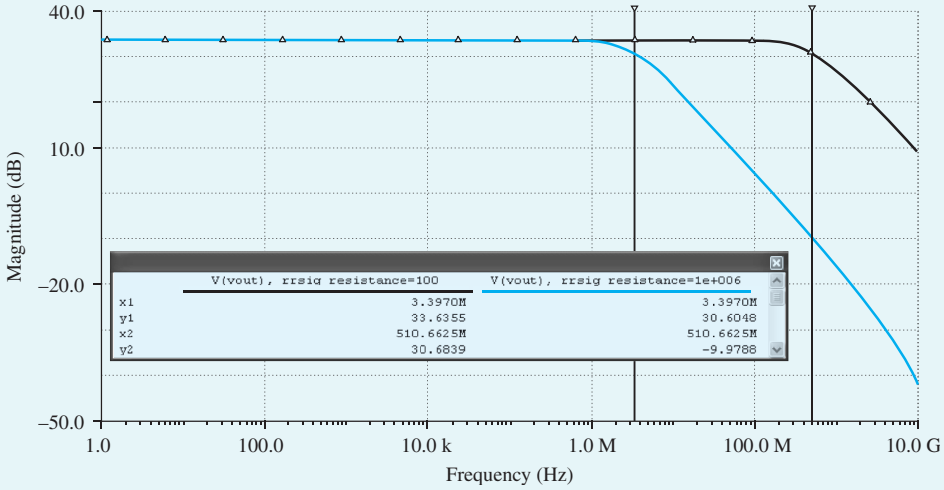



**Figure B.92** Frequency response of the CMOS CS amplifier with $R_{sig}$ = 100 Ω and $R_{sig}$ = 1 MΩ.

**Example MS.9.2** *continued*

**The Folded-Cascode Amplifier** Next, we will investigate the frequency response of the folded-cascode amplifier and compare its performance with that of the CS amplifier. Figure B.93 shows the circuit diagram of the folded-cascode amplifier.

| NMOS | |
|---|---|
| Vtn | 0.5 V |
| \|VAn\| | 12.5V |
| kn' | 246.2uA/V^2 |
| IREF | 0.1mA |
| L | 0.2 um |
| W | 0.48 um |

| PMOS | |
|---|---|
| Vtp | –0.5 V |
| \|VAp\| | 9V |
| kp' | –86.1 uA/V^2 |
| IREF | 0.1mA |
| L | 0.2 um |
| W | 0.64 um |

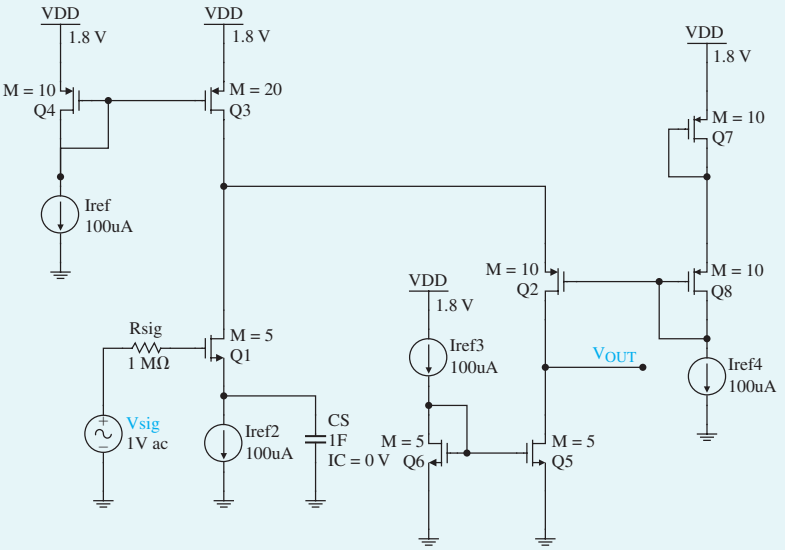



**Figure B.93** Schematic capture of the Folded-Cascode amplifier.

Figure B.94 shows the frequency response of the folded-cascode amplifier as simulated by Multisim for the cases of $R_{sig}$ = 100Ω and 1 MΩ. The corresponding values of the 3-dB frequency $f_H$ of the amplifier are given in Table B.24.

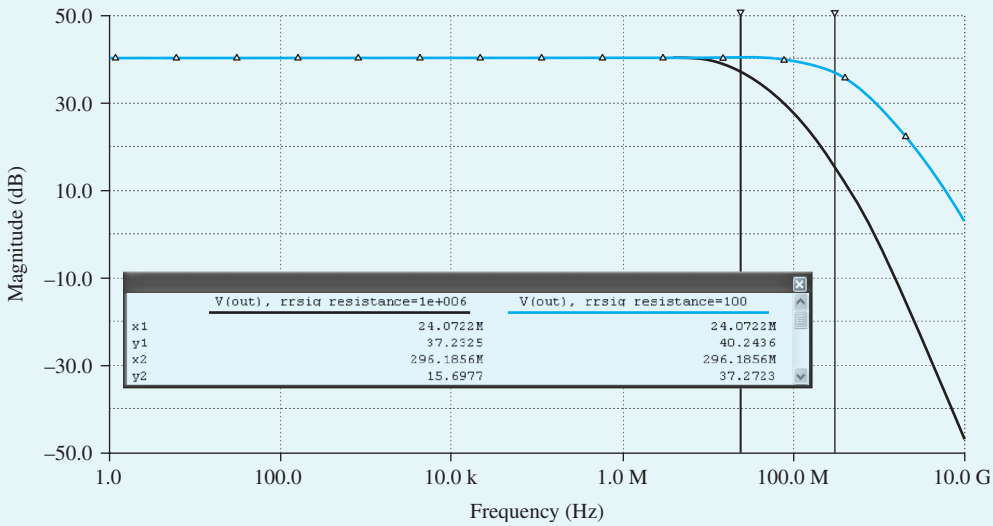



**Figure B.94** Frequency response of the folded-cascode amplifier with $R_{sig}$ = 100 Ω and $R_{sig}$ = 1 MΩ.

**Table B.24** Dependence of $f_H$ for the Designed Amplifiers

| $R_{sig}$ | $f_H$ | |
|---|---|---|
| | CS Amplifier | Folded-Cascode Amplifier |
| 100 Ω | 510.7 MHz | 296.2 MHz |
| 1 MΩ | 3.39 MHz | 24.0 MHz |

First, note that for the designed folded-cascode amplifier, $R_{\text{out}} = 125\ \text{k}\Omega$ and $|G_v| = 100$ V/V. Thus, $R_{\text{out}}$ and $G_v$ are larger than those of the CS amplifier (by a factor of 2). Note that these calculations can be found in Examples MS.7.1 and MS.7.2.

Also, observe that when $R_{\text{sig}}$ is small, $f_H$ of the folded-cascode amplifier is lower than that of the CS amplifier by a factor of about 1.8, approximately equal to the factor by which the gain is increased. This is because when $R_{\text{sig}}$ is small, the frequency response of both amplifiers is dominated by the pole formed at the output node, that is,

$$f_H \simeq f_{p,\text{out}} = \frac{1}{2\pi} \frac{1}{R_{\text{out}} C_{\text{out}}}$$

Now the output resistance of the folded-cascode amplifier is larger than that of the CS amplifier, while their output capacitances are approximately equal. Therefore, the folded-cascode amplifier has a lower $f_H$ in this case.

On the other hand, when $R_{\text{sig}}$ is large, $f_H$ of the folded-cascode amplifier is much higher than that of the CS amplifier. This is because in this case, the effect of the pole at $f_{p,\text{in}}$ on the overall frequency response of the amplifier becomes dominant. Since, owing to the Miller effect, $C_{\text{in}}$ of the CS amplifier is much larger than that of the folded-cascode amplifier, its $f_H$ is much lower.

To confirm this point, observe that $C_{\text{in}}$ of the folded-cascode amplifier can be estimated by replacing $R'_L$ in the equation used to compute $C_{\text{in}}$ for the CS amplifier, with the total resistance $R_{d1}$, between the drain of $Q_1$ and ground. Here,

$$R_{d1} = r_{01} \parallel r_{03} \parallel R_{\text{in}2}$$

where $R_{\text{in}2}$ is the input resistance of the common-gate transistor $Q_2$ and can be obtained using an approximation of the relationship found for input resistance of the common-gate amplifier:

$$R_{\text{in}2} \simeq \frac{r_{o2} + r_{o5}}{g_{m2} r_{o2}}$$

Thus,

$$R_{d1} \simeq r_{o1} \parallel r_{o3} \parallel \frac{r_{o2} + r_{o5}}{g_{m2} r_{o2}} = \frac{2}{g_{m2}}$$

Therefore, $R_{d1}$ is much smaller than $R'_L$ (in the CS amplifier $\simeq r_{o1} \parallel r_{o3}$). Hence, $C_{\text{in}}$ of the designed folded-cascode amplifier is indeed much smaller than that of the CS amplifier because the $(1 + g_m R')$ multiplier is smaller for the folded-cascode device. This confirms that the folded-cascode amplifier is much less impacted by the Miller effect and, therefore, can achieve a much higher $f_H$ when $R_{\text{sig}}$ is large.

The midband gain of the folded-cascode amplifier can be significantly increased by replacing the current mirror $Q_5$–$Q_6$ with a current mirror having a larger output resistance, such as the cascode current mirror in Fig. 6.32, whose output resistance is approximately $g_m r_o^2$. In this case, however, $R_{\text{in}2}$ and, hence, $R_{d1}$ increase, causing an increased Miller effect and a corresponding reduction in $f_H$.

Finally, it is interesting to observe that the frequency response of the folded-cascode amplifier shown in Fig. B.94 drops beyond $f_H$ at approximately –20 dB/decade when $R_{\text{sig}} = 100\ \Omega$ and at approximately –40 dB/decade when $R_{\text{sig}} = 1\text{M}\Omega$. This is because when $R_{\text{sig}}$ is small, the frequency response is dominated by the pole at $f_{p,\text{out}}$. However, when $R_{\text{sig}}$ is increased, $f_{p,\text{in}}$ is moved closer to $f_{p,\text{out}}$, and both poles contribute to the gain falloff.

## Example MS.10.1

### A Two-Stage CMOS Op Amp with Series–Shunt Feedback

In this example, we will investigate the effect of applying a series–shunt feedback to the two-stage CMOS op amp whose schematic capture is shown in Fig. B.95.

The first stage is a differential pair $Q_1$–$Q_2$ (which is actively loaded with the current mirror formed by $Q_3$ and $Q_4$) with bias current supplied by a current mirror formed by $Q_8$ and $Q_5$, which utilizes the reference bias current $I_{REF}$. The second stage consists of $Q_6$, which is a common-drain amplifier actively loaded with a current source load (transistor $Q_7$).

For the implementation of this CMOS op amp, we will use a 0.18-µm CMOS technology for the MOSFETs and typical SPICE level-1 model parameters for this technology, including the intrinsic

| NMOS | |
|---|---|
| Vtn | 0.5 V |
| \|VAn\| | 12.5V |
| kn' | 246.2uA/V^2 |
| L | 0.2 um |
| W | 0.48 um |
| | |

| PMOS | |
|---|---|
| Vtp | –0.5 V |
| \|VAp\| | 9V |
| kp' | –86.1 µA/V^2 |
| L | 0.2 um |
| W | 0.64 um |
| | |

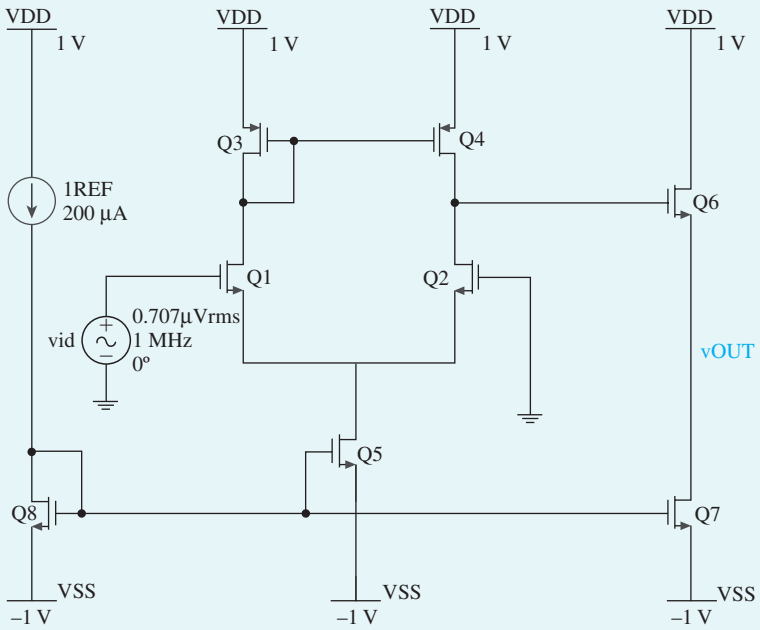



**Figure B.95** Schematic capture of the two-stage CMOS op amp.

capacitance values. The targeted specifications are an unloaded dc open-loop voltage gain $|A_v| = 50$ V/V, and closed-loop voltage gain $|A_f| = 10$ V/V, with each of transistors $Q_1$, $Q_2$, $Q_3$, and $Q_4$ biased at a drain current of 100 µA.

To achieve the targeted specifications, a biasing current $I_{REF} = 200$ µA is used, and the transistors $Q_5$, $Q_6$, $Q_7$, and $Q_8$ will be sized to conduct drain currents of 200 µA. The dc open-loop voltage gain for this amplifier is the product of the voltage gains of the two stages. Since the gain of the second stage (source follower) is approximately 1 V/V, the first stage must be designed to provide the full voltage gain of 50 V/V to achieve the specified open-loop voltage gain.

The amplifier specifications are summarized in Table B.25.

| **Table B.25** Two-Stage CMOS Op-Amp Specifications | |
|---|---|
| Parameters | Value |
| $I_{(Q1,\ Q2,\ Q3,\ \text{and}\ Q4)}$ | 100 μA |
| $I_{(Q5,\ Q6,\ Q7,\ \text{and}\ Q8)}$ | 200 μA |
| $\lvert A_1 \rvert$ | 50 V/V |
| $\lvert A_2 \rvert$ | 1 V/V |
| $\lvert A_f \rvert$ | 10 V/V |
| $V_{DD}$ | 1 V |
| $V_{SS}$ | –1 V |

## Hand Design

**Design of the Two-Stage Op Amp** The first stage of this CMOS op amp is identical to the first stage of the op amp we designed in Example MS.8.1, to which the reader is referred. Also, transistors $Q_6$ and $Q_7$ are sized to provide the bias current of 200 μA in the second stage.

As a result, using unit-size NMOS transistors with $W_n/L_n = 0.48\ \mu\text{m}/0.20\ \mu\text{m}$, and unit-size PMOS transistors with $W_p/L_p = 0.64\ \mu\text{m}/0.20\ \mu\text{m}$, the corresponding multiplicative factor $m$ for each transistor can be calculated as found in Example MS.8.1 (with the difference here that $Q_6$ and $Q_7$ have the same dimensions). Table B.26 summarizes the relevant information and the calculated $m$ values for the transistor.

| **Table B.26** Transistor Sizes | | |
|---|---|---|
| Transistor | $I_D$ (μA) | $m$ |
| 1 | 100 | 6 |
| 2 | 100 | 6 |
| 3 | 100 | 14 |
| 4 | 100 | 14 |
| 5 | 200 | 13 |
| 6 | 200 | 13 |
| 7 | 200 | 13 |
| 8 | 200 | 13 |

**Design of the Feedback Network** First we need to determine the value of the feedback factor $\beta$ for this series–shunt feedback amplifier. The $\beta$ network can be implemented using a voltage divider, as shown in Fig. B.96. The resistor values are chosen large enough (in comparison to the output resistance of the designed two-stage op amp) to minimize the effect of loading. Therefore, effectively,

$$A \simeq A_v$$

where $A$ is the open-loop gain of the amplifier (with loading). Now we can calculate the required feedback factor, $\beta$, as follows:

$$\lvert A_f \rvert = \frac{A_v}{1 + A_v\beta} = \frac{50}{1 + 50\beta} = 10\text{V/V}$$

$$\beta = 0.08$$

**Example MS.10.1** *continued*

The resistor values of this voltage divider are selected to provide voltage divisions of 0.08 ($R_1$ = 92 kΩ and $R_2$ = 8kΩ).

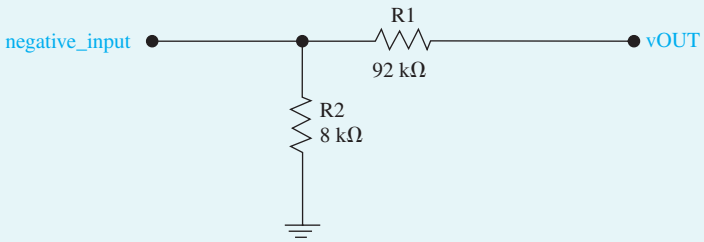



**Figure B.96** $\beta$ Network.

## Simulation

Now we will simulate our designed circuit to verify our hand design and study the effect of feedback on the dc-gain, bandwidth, and output resistance of the amplifier.

**Verifying $A_v$** The schematic capture of the two-stage CMOS amplifier is in Fig. B.95. We can verify the dc voltage gain of this amplifier by performing frequency-response analysis as set up in Ch10_OpAmp_Ex_Av.ms10.

As can be seen from Fig. B.97, $|A_v|$ = 35.0 dB ≃ 56.2 V/V, which is close to the targeted specification.

**Verifying $A$** The schematic capture of the $A$-circuit is given in Fig. B98.

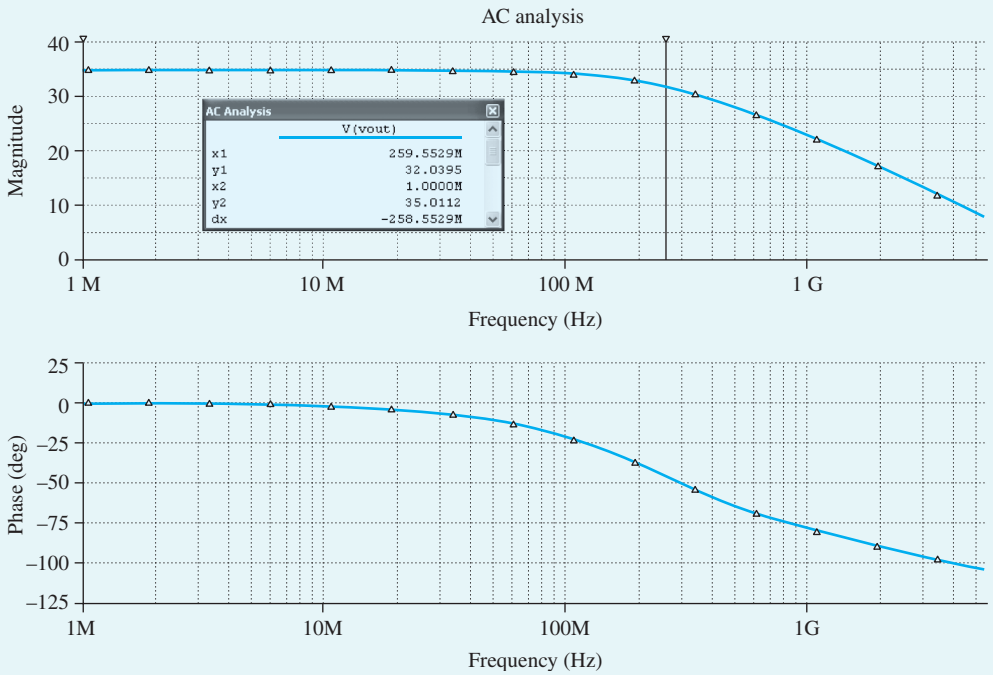



**Figure B.97** Frequency response of the two–stage CMOS op-amp amplifier.

| NMOS | |
|---|---|
| Vtn | 0.5 V |
| \|VAn\| | 12.5V |
| kn' | 246.2μA/V^2 |
| L | 0.2 um |
| W | 0.48 um |
| | |

| PMOS | |
|---|---|
| Vtp | –0.5 V |
| \|VAp\| | 9V |
| kp' | –86.1 uA/V^2 |
| L | 0.2 um |
| W | 0.64 um |
| | |

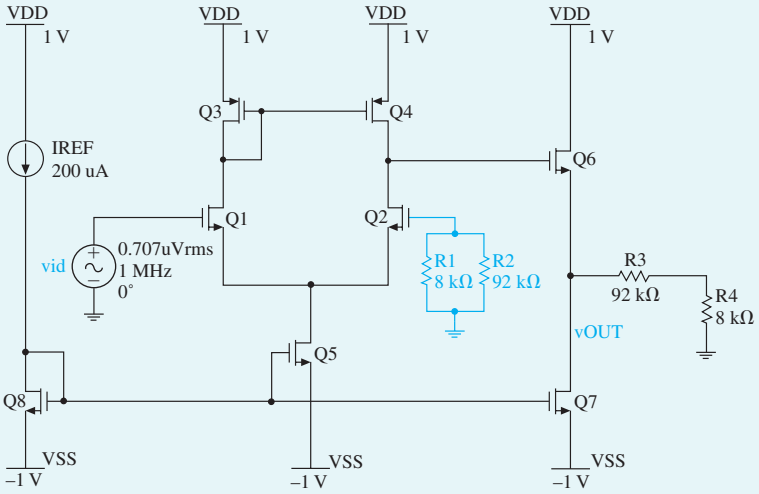



**Figure B.98** Schematic capture of the $A$ circuit.

We can verify the open-loop voltage gain of this circuit by performing a frequency-response analysis as set up in Ch10_OpAmp_Ex_A.ms10. As can be seen from Fig. B.99, $|A| = 34.9$ dB $\simeq 55.6$ V/V, which is close to the value of $A_v$. This supports our assumption of $A \simeq A_v$.

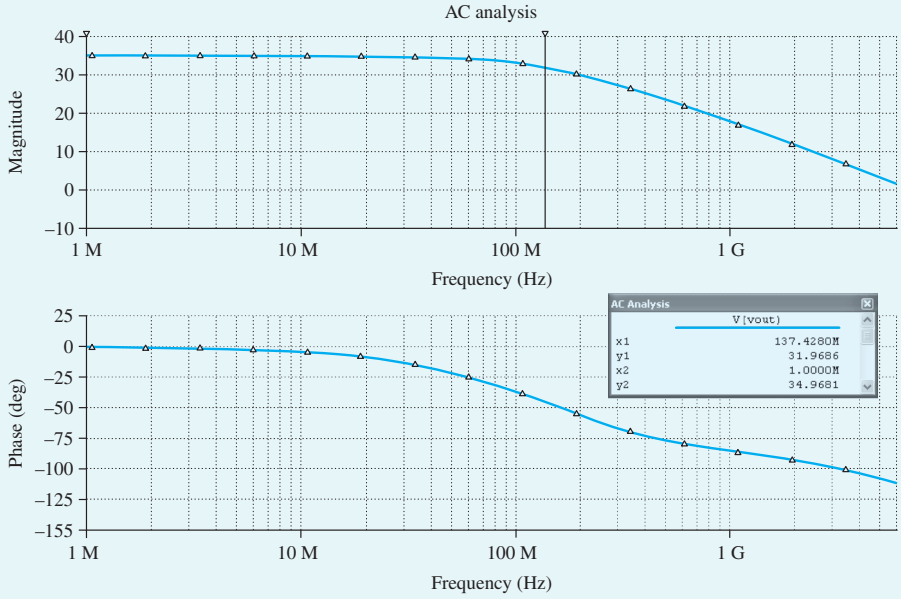



**Figure B.99** Schematic capture of the $A$- circuit.

**Verifying $A_f$** The schematic capture of the closed-loop circuit is given in Fig. B.100. As can be seen from this schematic, the $\beta$-network establishes a series connection at the input and a shunt connection at the output of the original two-stage CMOS op amp.

**Example MS.10.1** *continued*

We can verify the closed-loop voltage gain by performing a frequency-response analysis as set up in Ch10_OpAmp_Ex_Af.ms10. As can be seen from Fig. B.101, $|A_f| = 20.2$ dB $\simeq$ 10.2 V/V, which is close to the targeted specification for $A_f$.

| NMOS | |
|---|---|
| Vtn | 0.5 V |
| \|VAn\| | 12.5V |
| kn' | 246.2uA/V^2 |
| L | 0.2 um |
| W | 0.48 um |
| | |

| PMOS | |
|---|---|
| Vtp | –0.5 V |
| \|VAp\| | 9V |
| kp' | –86.1 uA/V^2 |
| L | 0.2 um |
| W | 0.64 um |
| | |

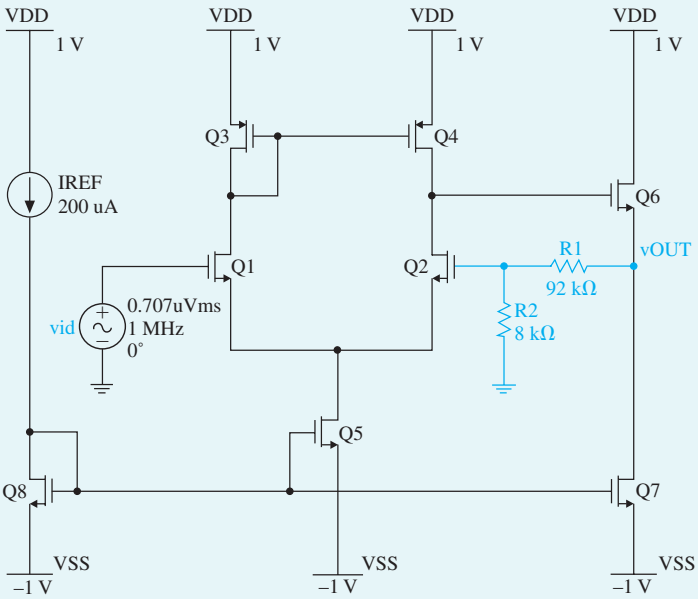



**Figure B.100** Schematic capture of the closed-loop circuit.

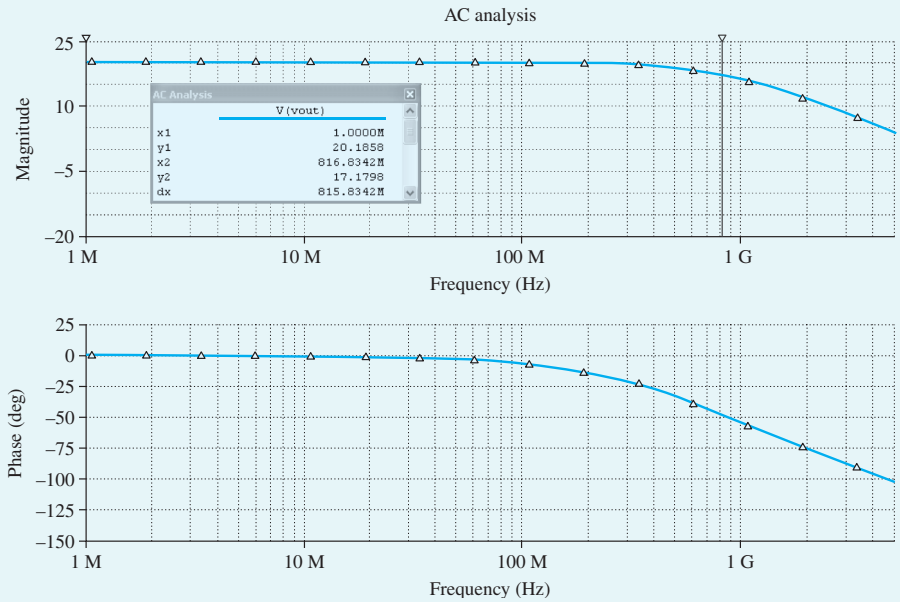



**Figure B.101** Frequency response of the closed-loop circuit.

**Investigating the Effect of Feedback** In addition to the frequency-response analysis, which provided information on the dc voltage gain and the 3-dB bandwidth, we used Multisim to find the output resistances of the open-loop and closed-loop circuits (as set up in Ch10_OpAmp_Ex_A.ms10 and Ch10_OpAmp_Ex_Af.ms10). Table B.27 summarizes our findings for open-loop ($A$ circuit) and closed-loop circuits.

**Table B.27** Effect of Feedback on Gain, 3-dB Bandwidth, and Output Resistor

| Circuit | Gain (V/V) | 3-dB Bandwidth (MHz) | $R_{out}$ (Ω) |
|---|---|---|---|
| Open loop | 55.6 | 137 | 492.6 |
| Closed loop | 10.2 | 816 | 89.3 |

It can be seen from Table B.27 that the series–shunt feedback connection causes the dc voltage gain and the output resistance of the circuit to decrease by a factor of 5.5, while the 3-dB bandwidth increases by approximately the same factor. This factor is equal to $1 + A\beta$, the amount of the feedback. This is as expected and corresponds to what we learned in Chapter 9.

## Example MS.11.1

### Class B Bipolar Output Stage

In this example, we will design a class B output stage to deliver an average power of 20 W to an 8-Ω load. The schematic capture of a class B output stage implemented using BJTs is shown in Fig. B.102. We then will investigate various characteristics of the designed circuit such as crossover distortion and power-conversion efficiency. For this design, we are to select $V_{CC}$ about 5 V greater than the peak output voltage in order to avoid transistor saturation and signal distortion.

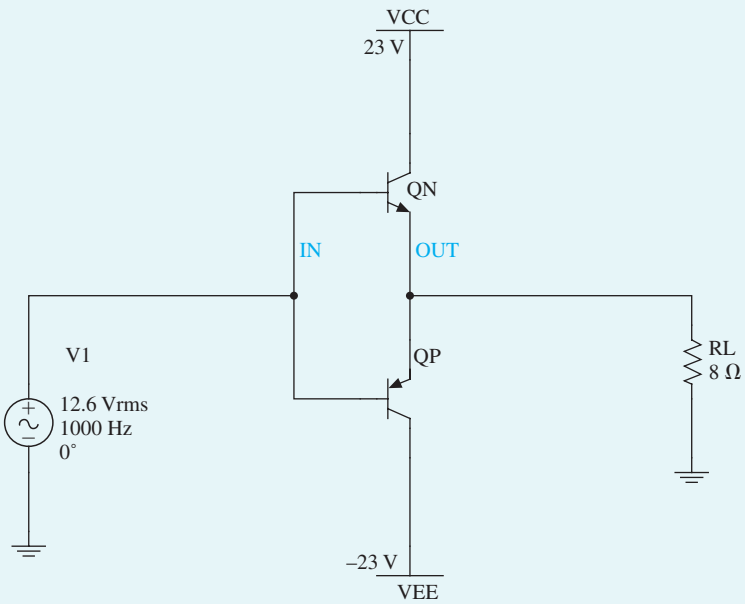



**Figure B.102** Schematic capture of class B output stage.

**Example MS.11.1** *continued*

The circuit specifications are summarized in Table B.28.

**Table B.28** Class B Output Stage Specifications

| Specification | Value |
|---|---|
| $P_L$ | 20 W |
| $R_L$ | 8Ω |
| $V_{CC}$ | $\hat{V}$ + 5 V |

## Hand Design

We know from Eq. (13.12) that

$$P_L = \frac{1}{2}\frac{\hat{V}^2}{R_L}$$

Thus

$$V = \sqrt{2P_L R_L} = \sqrt{2 \times 20 \times 8}$$
$$V = 17.9 \text{ V}$$

which leads to $V_{CC} = 23$ V.

The peak current drawn from the supply will be

$$I_O = \frac{\hat{V}}{R_L} = \frac{17.9}{8}$$
$$I_o = 2.24\text{A}$$

Now we can use Eq. (13.13) to calculate the average power drawn from each of the supplies

$$P_{S+} = P_{S-} = \frac{1}{\pi}\frac{\hat{V}}{R_L}V_{CC} = \frac{1}{\pi} \times 2.24 \times 23$$
$$P_{S+} = P_{S-} = 16.4 \text{ W}$$
$$P_S = P_{S+} + P_{S-} = 16.4 + 16.4 = 32.8 \text{ W}$$

Therefore, the power-conversion efficiency, η , is

$$\eta = \frac{P_L}{P_S} \times 100\% = \frac{17.9}{32.8} \times 100\% = 61\%$$

Now we can utilize Eq. (13.22) to calculate the maximum power dissipated in each of the transistors as

$$P_{DN\max} = P_{DP\max} = \frac{V_{CC}^2}{\pi^2 R_L} = \frac{(23)^2}{\pi^2 \times 8}$$
$$P_{DN\max} = P_{DP\max} = 6.7 \text{ W}$$

## Simulation

Next, we use Multisim to verify the operation of the class B output stage designed above. For simulation purposes, we will use discrete-power transistors MJE243 and MJE253 (from ON Semiconductor), which are rated for a maximum continuous collector current $I_{C\max} = 4$ A and a maximum collector–emitter voltage $V_{CE\max}$ of 100 V.

**Load Power $P_L$** To measure the amount of power delivered to the load, we will utilize Transient Analysis in Multisim as set up in Ch11_Class_B_Ex.ms10. The transient analysis simulation is performed over the interval 0 ms to 2 ms, and the waveforms of the voltage at the output node and the output current are plotted in Fig. B.103.

As can be seen in Fig. B.103, the peak voltage amplitude is approximately 16.9 V and the peak current amplitude is 2.1 A. Upon a closer look at the current and voltage waveforms, we can observe that both exhibit crossover distortion. The bottom graph in Fig. B.103 shows the instantaneous and the

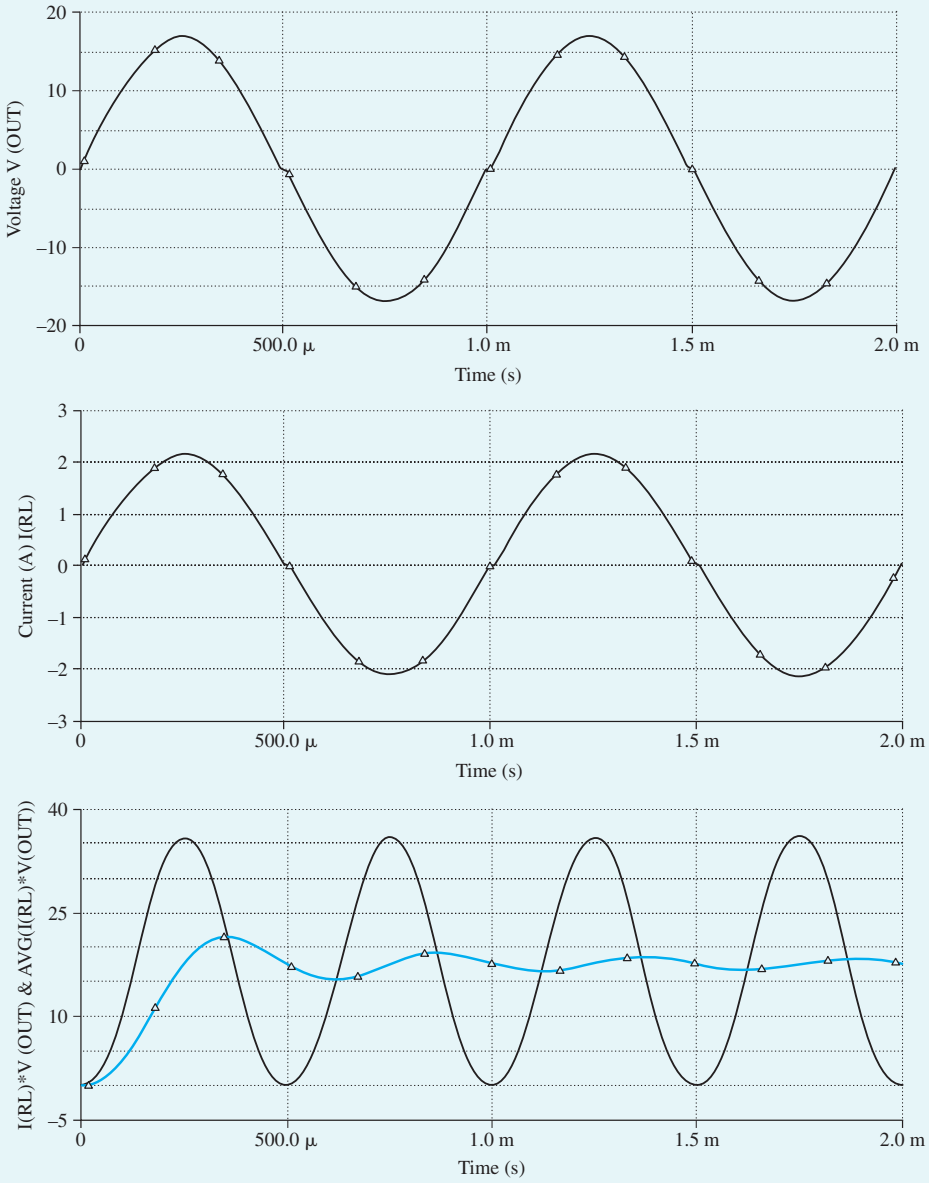



**Figure B.103** Load voltage, current, and instantaneous and average load power.

**Example MS.11.1** *continued*

average power dissipated in the load resistance. These waveforms were obtained by multiplying the current and voltage waveforms, and by taking the running average for the average power, $P_L$. The transient behavior of average power eventually settles into a quasiconstant steady-state value of 17.6 W.

**Supply Power, $P_S$** Similarly, we can plot instantaneous voltage and current at the $V_{CC}$ and $V_{EE}$ nodes to measure the value of $P_S$. Figure B.104 shows the voltage, current, instantaneous, and average power for $+V_{CC}$. We can plot these quantities for $-V_{EE}$ as well. However, owing to symmetry, we do not need to generate plots for the negative voltage supply. The average power provided by $+V_{CC}$, $P_{S+}$, is 15 W. Therefore, the total power provided by both voltage supplies is 30 W.

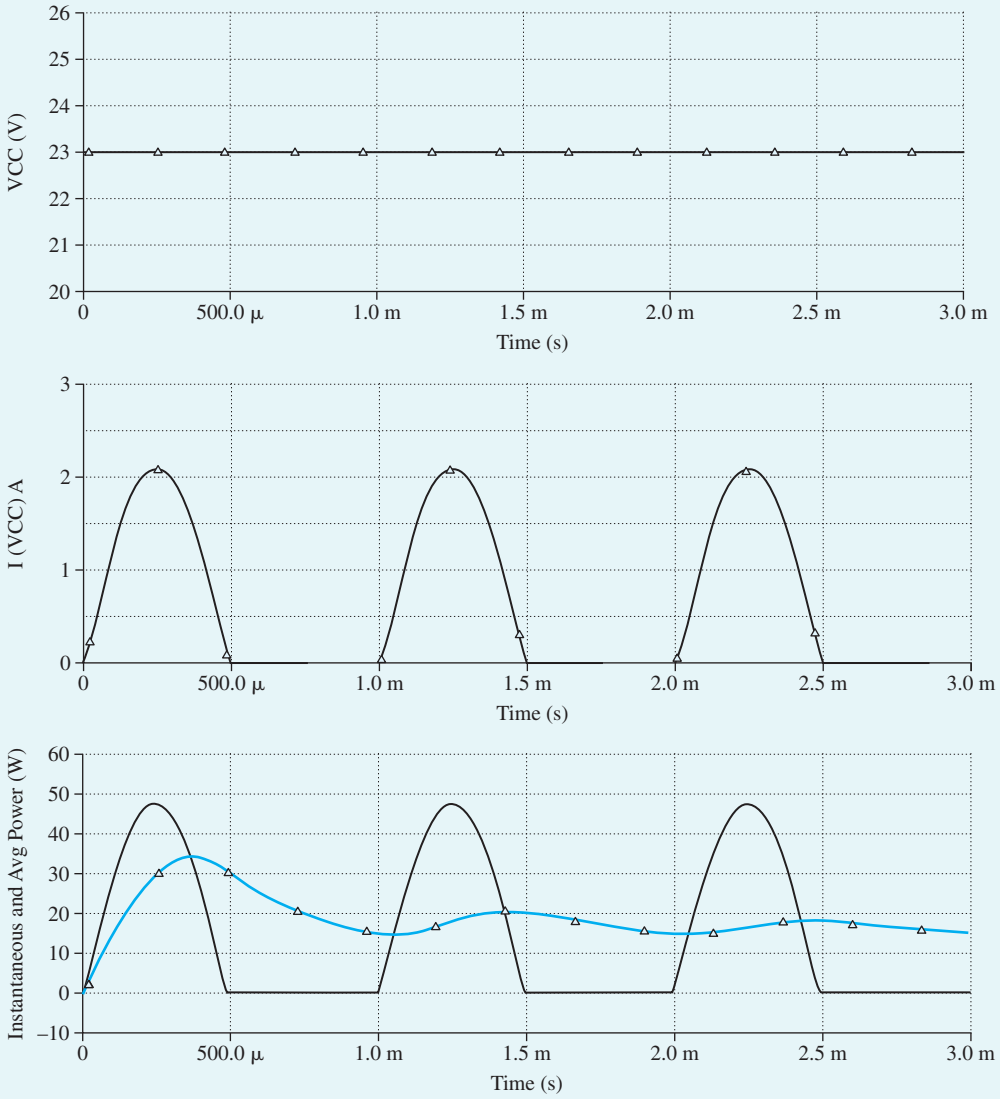



**Figure B.104** Supply voltage, current, and instantaneous and average supply power.

**Power-Conversion Efficiency, η** Now we can calculate the power-conversion efficiency of the simulated circuit as follows.

$$\eta = \frac{P_L}{P_S} \times 100\% = \frac{17.6}{30} \times 100\% = 58.6\%$$

**Transistor Power Dissipation, $P_D$** Figure B.103 shows voltage, current, instantaneous and average power plots for $Q_p$ only. A similar plot can be obtained for $Q_n$ to measure the power dissipated in the *npn* device. As expected, the voltage waveform is a sinusoid, and the current waveform consists of half-sinusoids. The waveform of instantaneous power is rather unusual. It indicates the presence of some distortion as a result of driving the transistors rather hard. This can be verified by reducing the amplitude of the input signal. Students are encouraged to investigate this point. The average power dissipated in $Q_p$, as measured from Fig. B.105, is approximately 6 W. Therefore, the total power dissipated in the transistors is 12 W.

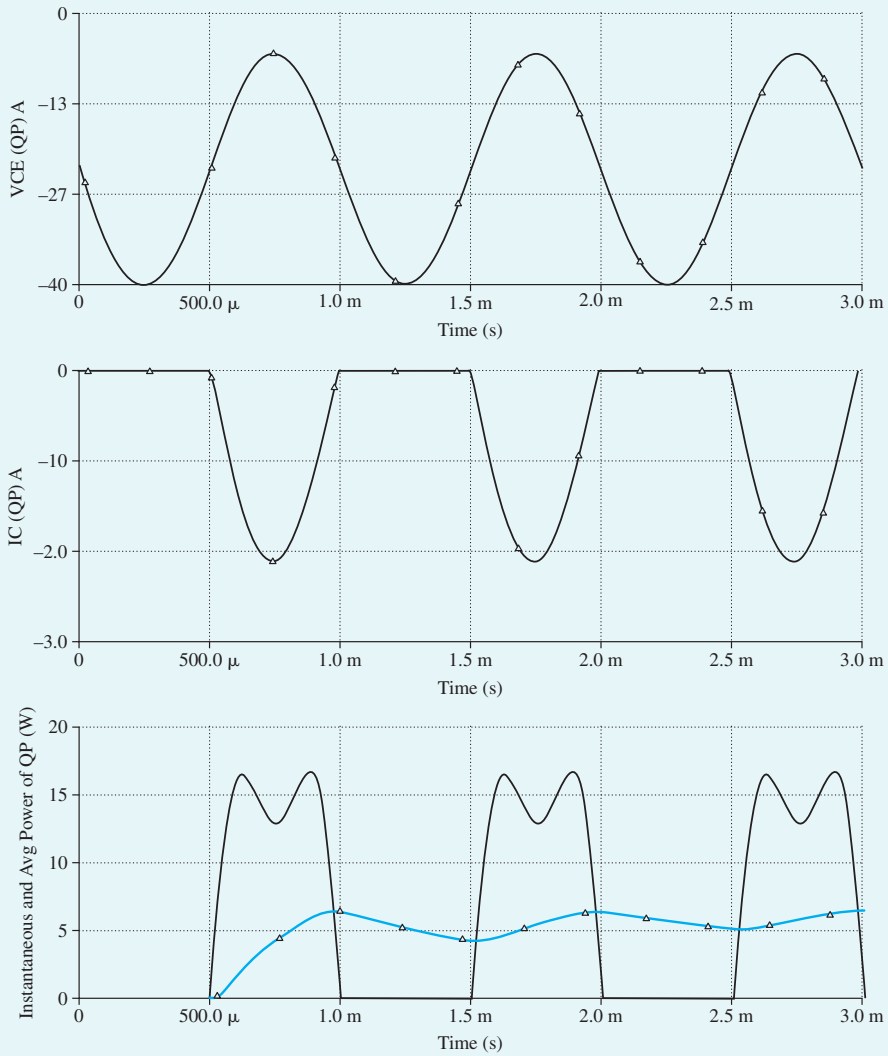



**Figure B.105** Voltage, current, and instantaneous and average power for $Q_p$.

**Example MS.11.1** *continued*

The simulation results and hand-design calculations are summarized in Table B.29. Observe that the values are quite close, which verifies our design of the class B output stage.

**Table B.29** Summary of Simulation and Hand-Design Results

| Measurement | Hand Design | Simulated | Error % |
|---|---|---|---|
| $P_L$ | 17.9 W | 17.6 W | 1.7 |
| $P_S$ | 32.8 W | 30 W | 8.5 |
| $P_D$ | 13.4 W | 12 W | 10.4 |
| $n$ | 61% | 58.6% | 3.9 |

**Crossover Distortion** We can further investigate the crossover distortion of this circuit by utilizing the voltage transfer characteristics (VTC) curve of the class B output stage. The plot is obtained through a dc sweep analysis in Multisim where $v_{IN}$ is swept over the range –10 V to 10 V in 1.0-mV increments. From the resulting VTC curve, shown in Fig. B.106, we can see that the dead band extends from –0.605 V to 0.56 V. The effect of crossover distortion can be quantified by performing a Fourier analysis on the output voltage in Multisim.

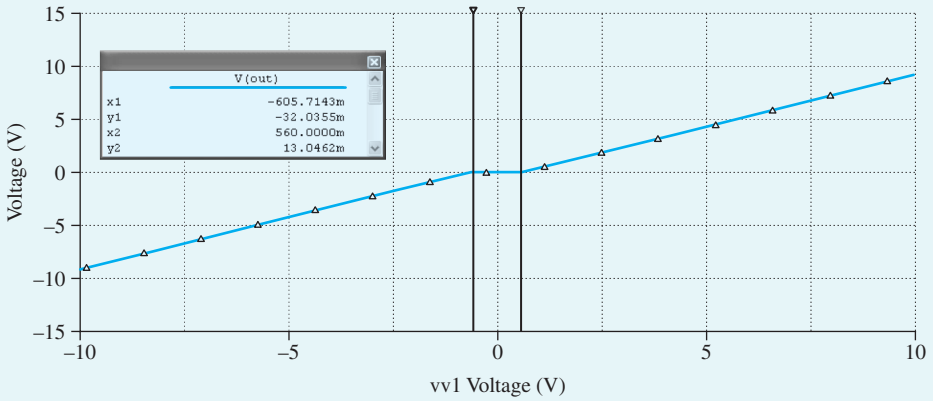



**Figure B.106** VTC of class B output stage.

**Total Harmonic Distortion (THD)** This analysis decomposes the waveform generated via transient analysis into its Fourier-series components. Furthermore, Multisim computes the THD of the output waveform, and the results are shown in Fig. B.107.

| | | | | | | |
|---|---|---|---|---|---|---|
| 4 | THD: | 2.12781 % | | | | |
| 5 | Gridsize: | 256 | | | | |
| 6 | Interpolation Degree: | 1 | | | | |
| 7 | | | | | | |
| 8 | Harmonic | Frequency | Magnitude | Phase | Norm. Mag | Norm. Phase |
| 9 | 1 | 1000 | 16.7351 | -0.0017584 | 1 | 0 |
| 10 | 2 | 2000 | 0.0104931 | 90.328 | 0.00062701 | 90.3297 |
| 11 | 3 | 3000 | 0.274201 | -179.99 | 0.0163847 | -179.98 |
| 12 | 4 | 4000 | 0.00492676 | 91.2479 | 0.000294396 | 91.2497 |
| 13 | 5 | 5000 | 0.172473 | 179.997 | 0.0103061 | 179.999 |
| 14 | 6 | 6000 | 0.00165276 | 92.6225 | 9.87598e-005 | 92.6243 |
| 15 | 7 | 7000 | 0.117776 | 179.948 | 0.00703764 | 179.949 |
| 16 | 8 | 8000 | 0.00148745 | 95.535 | 8.8882e-005 | 95.5368 |

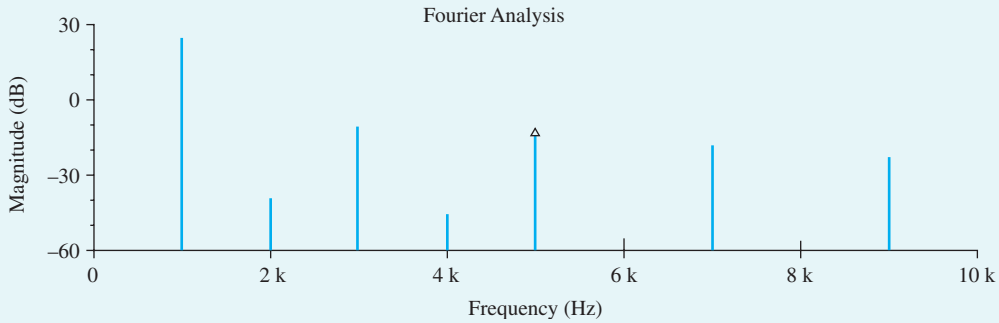



**Figure B.107** Fourier-series components of the output voltage and class B output stage THD.

From the Fourier analysis, we note that the waveform is rather rich in odd harmonics and that the resulting THD is 2.13%, which is rather high.

## Example MS.12.1

### A Two-Stage CMOS Op Amp with Frequency Compensation

In this example, we will use Multisim to aid in designing the frequency compensation of the two-stage CMOS circuit whose schematic is shown in Fig. B.108. Multisim will then be employed to determine the frequency response and the slew rate of the op amp. We will assume a 0.5-μm CMOS technology for the MOSFETs and use typical SPICE level-1 model parameters for this technology.

The op-amp circuit in Fig. B.108 is designed using a reference current $I_{REF} = 90\ \mu A$, a supply voltage $V_{DD} = 3.3$ V, and a load capacitor $C_L = 1$ pF. Unit-size transistors with $W/L = 1.25\mu m/0.6\mu m$ are used for both the NMOS and PMOS devices. The transistors are sized for an overdrive voltage $V_{OV} = 0.3$ V. The corresponding multiplicative factors are shown in Fig. B.108.

In Multisim, the common-mode input voltage $V_{CM}$ of the op-amp circuit is set to $V_{DD}/2 = 1.65$V, and DC Operating Point Analysis is performed to determine the dc bias conditions. Using the values found from the simulation results for the small-signal parameters of the MOSFETs, we obtain

$$G_{m1} = 0.333 \text{ mA/V}$$

$$G_{m2} = 0.650 \text{ mA/V}$$

$$C_1 = 26.5 \text{ fF}$$

$$C_2 = 1.04 \text{ pF}$$

**Example MS.12.1** *continued*

| NMOS | |
|---|---|
| Vtn | 0.7 V |
| LAMBDA | 0.1 |
| kn' | 246.2uA/V^2 |
| IREF | 0.09 mA |
| L | 0.6 um |
| W | 1.25 um |

| PMOS | |
|---|---|
| Vtp | –0.7 V |
| LAMBDA | 0.2 |
| kp' | –86.1 uA/V^2 |
| IREF | 0.09 mA |
| L | 0.6 um |
| W | 1.25 um |

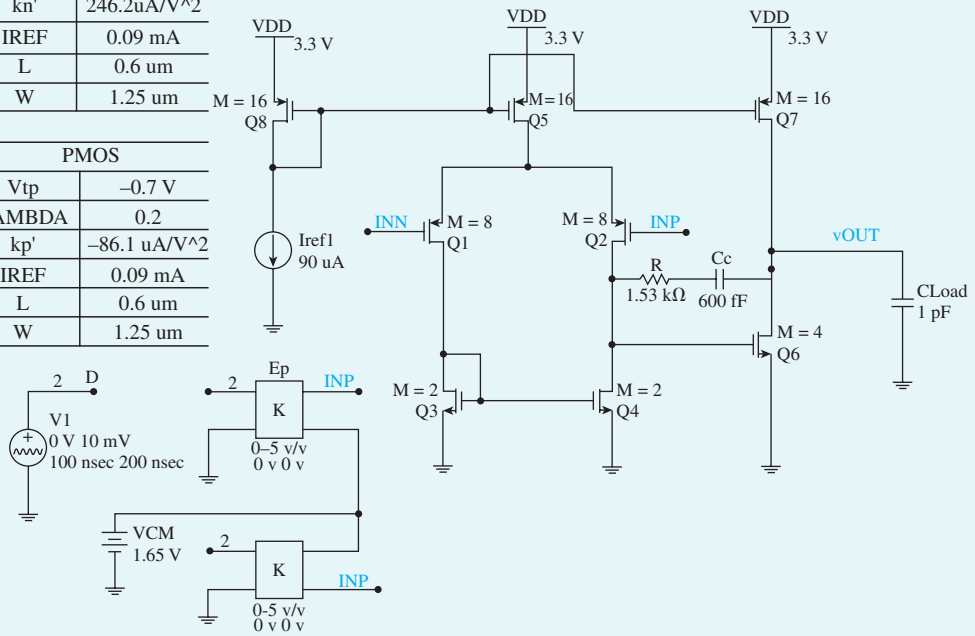



**Figure B.108** Schematic capture of the two-stage CMOS op amp.

using Eqs. (10.7), (10.14), (10.25), and (10.26) respectively. Recall that $G_{m1}$ and $G_{m2}$ are the transconductances of, respectively, the first and second stages of the op amp. Capacitors $C_1$ and $C_2$ represent the total capacitance to ground at the output nodes of, respectively, the first and second stage of the op amp.

Then, using Eq. (10.28), the frequency of the second, nondominant, pole can be found as

$$f_{P2} \simeq \frac{G_{m2}}{2\pi C_2} = 97.2 \text{ MHz}$$

To place the transmission zero, given by Eq. (10.38), at infinite frequency, we select

$$R = \frac{1}{G_{m2}} = 1.53 \text{ k}\Omega$$

Now, using Eq. (10.37), the phase margin of the op amp can be expressed as

$$\text{PM} = 90° - \tan^{-1}\left(\frac{f_t}{f_{P2}}\right)$$

where $f_t$ is the unity-gain frequency, given in Eq. (10.31):

$$f_1 = \frac{G_{m1}}{2\pi C_C}$$

Using the above two equations we determine that compensation capacitors of $C_C = 0.78$ pF and $C_C = 2$ pF are required to achieve phase margins of $PM = 55°$ and $PM = 75°$, respectively.

Next, an ac-analysis simulation is performed in Multisim to compute the frequency response of the op amp and to verify the foregoing design values (as set up in Ch12_Two_Stage_CMOS_OpAmp_ Ex_Freq-Resp.ms10). It

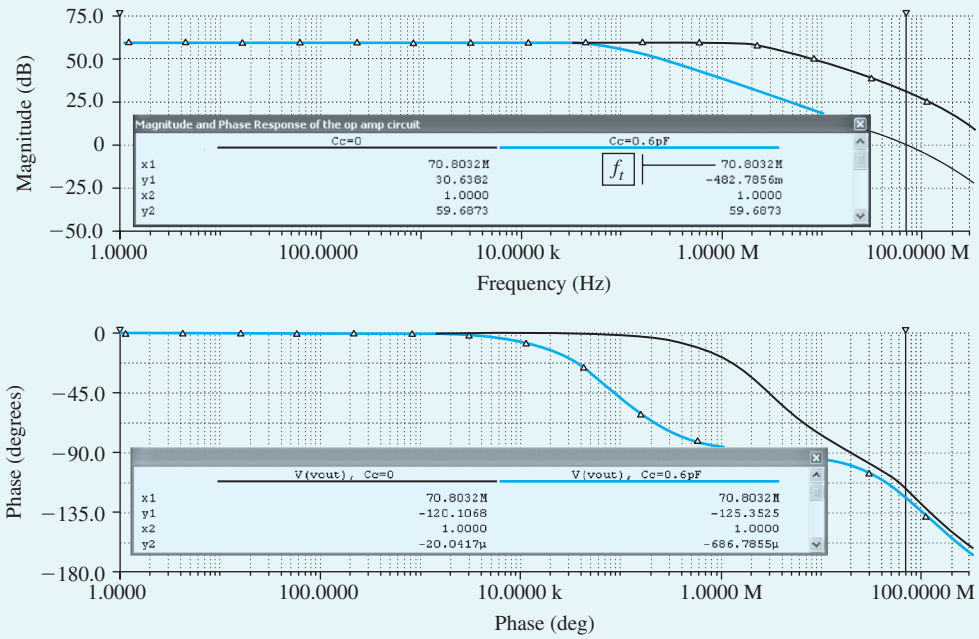



**Figure B.109** Magnitude and phase response of the op-amp circuit with $R = 1.53$ k, $C_C = 0$ (no frequency compensation), and $C_C = 1.8$ pF (PM = 75°).

was found that, with $R = 1.53$ kΩ, we needed $C_C = 0.6$ pF and $C_C = 1.8$ pF to set $PM = 55°$ and $PM = 75°$, respectively. We note that these values are reasonably close to those predicted by hand analysis. The corresponding frequency responses for the compensated op amps are plotted in Figs. B.109 and B.110. For comparison, we also show the frequency response of the uncompensated op amp ($C_C = 0$). Observe that the unity-gain frequency $f_t$ drops from 70.8 MHz to 26.4 MHz as $C_C$ is increased to improve $PM$.

Rather than increasing the compensation capacitor $C_C$ to improve the phase margin, the value of the series resistor $R$ can be increased: for a given $C_C$, increasing $R$ above $1/G_{m2}$ places the transmission zero at a negative real-axis location (Eq. 10.38), where the phase it introduces *adds* to the phase margin. Thus, $PM$ can be improved without affecting $f_t$. To verify this point, we set $C_C$ to 0.6 pF and simulate the op-amp circuit in Multisim for the cases of $R = 1.53$ kΩ and $R = 3.2$ kΩ. The corresponding frequency response is plotted in Fig. B.111. Observe how $f_t$ is approximately independent of $R$. However, by increasing $R$, we can improve $PM$ from 55° to 75°.

Increasing the $PM$ is desirable because it reduces the overshoot in the step response of the op amp. To verify this point, we simulate in Multisim the step response of the op amp for $PM = 55°$ and $PM = 75°$. To do that, we connect the op amp in a unity-gain configuration, apply a small (10-mV) pulse signal at the input with very short (1-ps) rise and fall times to emulate a step input, perform a transient analysis simulation (as set up in Ch12_Two_Stage_CMOS_OpAmp_Ex_Small-Signal.ms10), and plot the output voltage as shown in Fig. B.112. Observe that the overshoot in the step response drops from 15% to 1.4% when the phase margin is increased from 55° to 75°.

We conclude this example by computing $SR$, the slew rate of the op amp. From Eq. (10.40), we have

$$SR = 2\pi f_t V_{OV} = \frac{G_{m1}}{C_C} V_{OV} = 166.5 \text{ V/}\mu s$$

**Example MS.12.1** *continued*

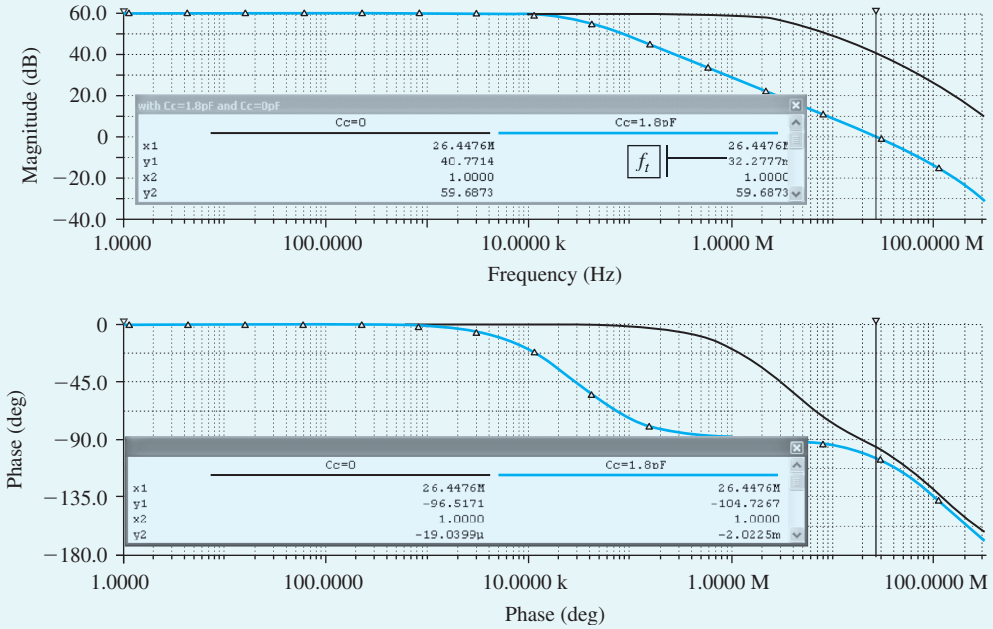



**Figure B.110** Magnitude and phase response of the op-amp circuit with $R = 1.53$ kΩ, $C_C = 0$ (no frequency compensation), and $C_C = 1.8$ pF ($PM = 75°$).

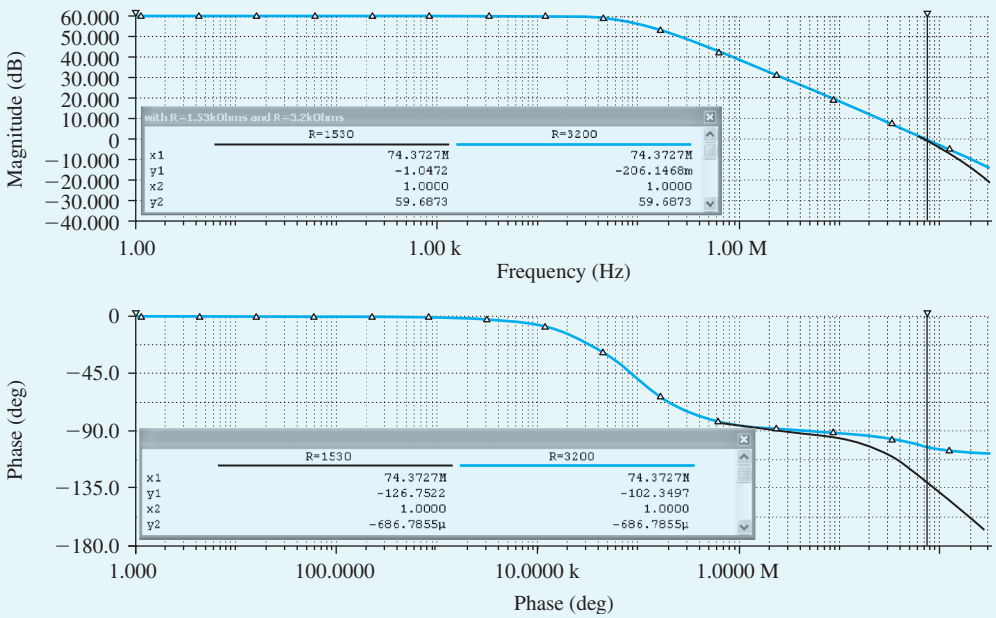



**Figure B.111** Magnitude and phase response of the op amp circuit with $C_C = 0.6$ pF, $R = 1.53$ kΩ ($PM = 55°$), and $R = 3.2$ kΩ ($PM = 75°$).

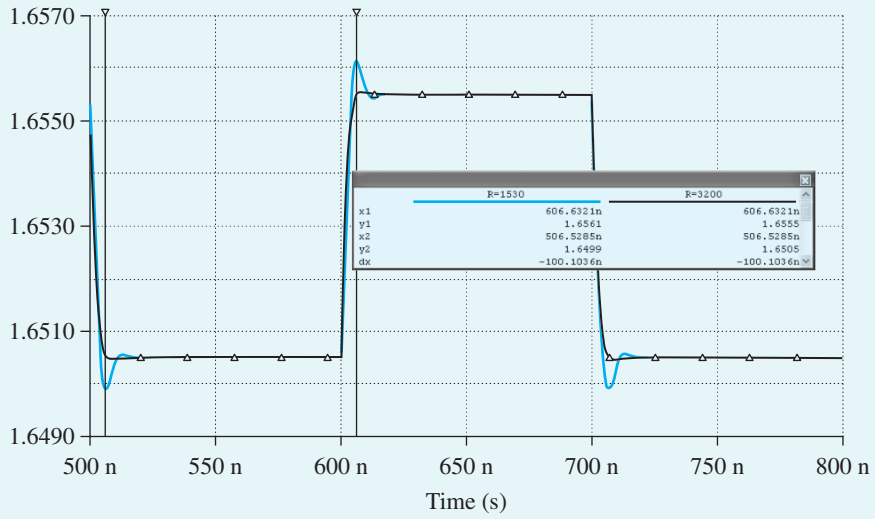



**Figure B.112** Small-signal step response (for a 10-mV step input) if the op-amp circuit is connected in a unity-gain configuration: $PM = 55°$ ($C_C = 0.6$ pF, $R = 1.53$ kΩ) and $PM = 75°$ ($C_C = 0.6$ pF, $R = 3.2$ kΩ).

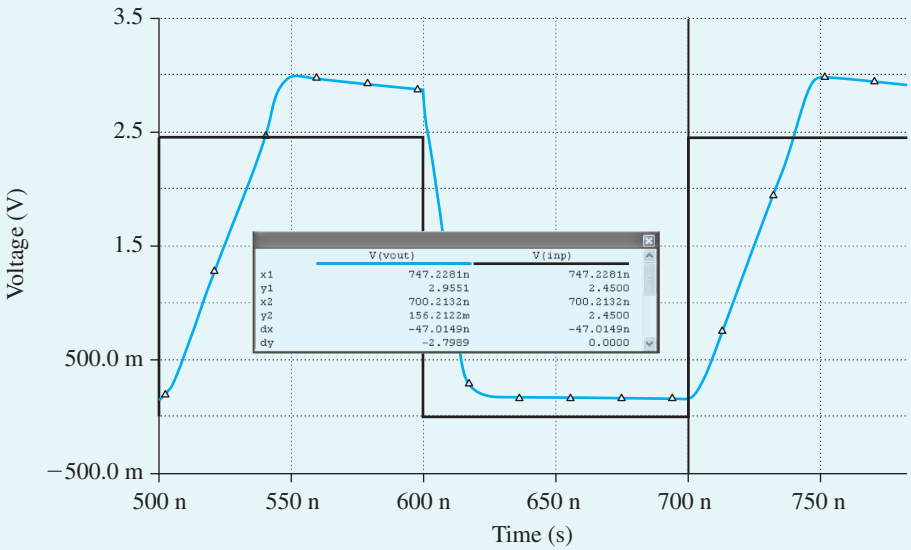



**Figure B.113** Large-signal step response (for a 2.2-V step input) if the op-amp circuit is connected in a unity-gain configuration. The slope of the rising and falling edges of the output waveform correspond to the slew rate of the op amp.

when $C_C = 0.6$ pF. Next, to determine SR using Multisim, we again connect the op amp in a unity-gain configuration and perform a transient analysis simulation (as set up in Ch12_Two_Stage_CMOS_OpAmp_Ex_Large-Signal.ms10). However, we now apply a large pulse signal (2.2 V) at the input to cause slew-rate limiting at the output. The corresponding output voltage waveform is plotted in Fig. B.113. The slope of the slew-rate-limited output waveform corresponds to the slew rate of the op amp and is found to be $SR = 160$ V/μs and 60 V/μs for the negative- and positive-going output, respectively. These results, with the

**Example MS.12.1** *continued*

unequal values of *SR* in the two directions, differ from those predicted by the simple model for the slew-rate limiting of the two-stage op-amp circuit. The difference can perhaps be said to be a result of transistor $Q_4$ entering the triode region and its output current (which is sourced through $C_C$) being correspondingly reduced. Of course, the availability of Multisim should enable the reader to explore this point further.

## Example MS.13.1

### The CMOS Inverter

In this example, we will use Multisim to design a CMOS inverter whose schematic capture is shown in Fig. B.114. We will assume a 0.18-μm CMOS technology for the MOSFETs and use typical SPICE level-1 model parameters for this technology, including the intrinsic capacitance values. This model does not take into account the short-channel effects for this technology. Also, the load capacitance is assumed to be dominated by the extrinsic component $C_{ext}$ (resulting from the wiring and the input capacitance of the driven gates), where the value used in this example is 15 fF. We will begin with an approximate hand-analysis design. We will then use Multisim to verify that the designed circuit meets the specifications. The targeted specification for this inverter is a high-to-low propagation delay ($t_{PHL}$) of less than 45 ps. Once designed, the other characteristics of this inverter such as low-to-high propagation delay ($t_{PLH}$), noise margins, and threshold voltage will be investigated.

The inverter specifications are summarized in Table B.30.

**Table B.30** CMOS Inverter Specifications

| Parameters | Value |
|---|---|
| $t_{PHL}$ | 45 ps |
| $C_L$ | 15 fF |
| $V_{DD}$ | 1.8 V |

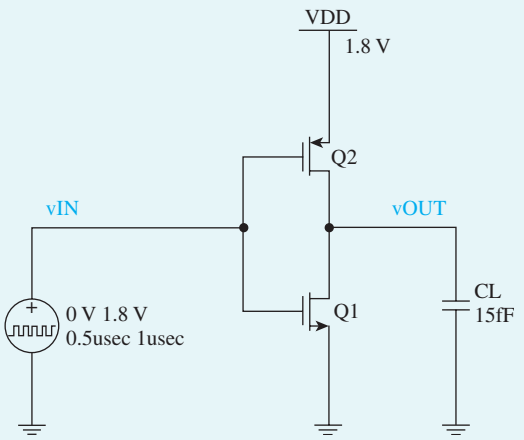



**Figure B.114** Schematic capture of the CMOS inverter.

## Hand Design

For the design of this inverter we choose $L = 0.2$ µm, so we have $L_{\text{eff}} = 0$ .180 µm. As mentioned earlier, to minimize area, all channels are usually made equal to the minimum length permitted by the given technology. To meet the specified $t_{PHL}$, we need to size $(W/L_{\text{eff}})_n$ carefully. Once sized, $(W/L_{\text{eff}})_p = 2(W/L_{\text{eff}})_n$ is chosen, which is a compromise between area, noise margins, and $t_{PLH}$.

The value of $t_{PHL}$ can be estimated using Eq. (14.64) as

$$t_{PHL} = \frac{\alpha_n C}{k'_n\left(\frac{W}{L_{\text{eff}}}\right)V_{DD}} = \frac{15 \times 10^{-15}\alpha_n}{246.2 \times 10^{-6}\left(\frac{W}{L_{\text{eff}}}\right)1.8}$$

where $\alpha_n$ is a factor determined by the relative values of $V_t$ and $V_{DD}$ ($V_{tn}/V_{DD=0.5/1.8=0.278}$):

$$\alpha_n = \frac{2}{7/4^{-3}(V_{tn}/V_{DD}) + (V_{tn}/V_{DD})^2} = 2.01$$

Based on the above equations, the specified $t_{PHL}$ can be achieved by selecting the ratio $(W/L_{\text{eff}})_n = 1.5$ and consequently $(W/L_{\text{eff}})_n = 3$ . Table B.31 summarizes the relevant sizing information for each transistor. The third column of this table shows the transconductance parameter values for each transistor (which are typical values for 0.18-µm CMOS technology).

**Table B.31** Transistor Sizes

| Transistor | $W$ (µm) | $L_{\text{eff}}$ (µm) | $k'$ (µA/V$^2$) |
|---|---|---|---|
| NMOS | 0.27 | 0.18 | 246.2 |
| PMOS | 0.54 | 0.18 | 86.1 |

Note that for the selected width values, the intrinsic capacitances $C_{gd1}$ and $C_{gd2}$ are insignificant in comparison to the load capacitance. This confirms our initial assumption that in our hand calculations of delay, we could neglect $C_{gd1}$ an $C_{gd2}$ (which vary proportionally with width).

## Simulation

**Verifying Propagation Delay** To investigate the dynamic operation of the inverter and to verify that the design meets the specified $t_{PHL}$, we apply an ideal pulse signal at the input and perform a transient analysis, as set up in Ch13_CMOS_Inverter_tPHL_Ex.ms10. Then, we plot the input and output waveforms as shown in Fig. B.115. Based on the simulated response, $t_{PHL} = 40.5$ ps (as indicated in Fig. B.115). Similarly, we obtain $t_{PLH} = 60.3$ ps, resulting in the inverter propagation delay ($t_P$) of 50.4 ps. Therefore, the specified high-to-low propagation delay specification is met, and $t_P$ takes a reasonable value.

**Voltage Transfer Characteristic (VTC)** To compute both the VTC of the inverter and its supply current at various values of the input voltage $V_{\text{in}}$, we apply a dc voltage source at the input and perform a dc sweep with $V_{\text{in}}$ swept over the range 0 to $V_{DD}$, as set up in Ch13_CMOS_Inverter_VTC_Ex.ms10. The resulting VTC is plotted in Fig. B.116. Note that the slope of the VTC in the switching region (where the NMOS and PMOS devices are both in saturation) is not infinite as predicted from the simple theory presented earlier. Rather, the nonzero value of λ causes the inverter gain to be finite. The two points on the VTC at which the inverter gain is unity (i.e., the VTC slope is –1 V/V) and that determine $V_{IL}$ and $V_{IH}$ are indicated in Fig. B.116. The corresponding noise margins are $NM_L = 0.76$ V and $NM_H = 0.81$V. Note that the design provides high tolerance to noise, since noise margins are reasonably high ($NM_L$ and $NM_H$ are 42% and 45% of the supply voltage). This implies that the inverter would provide the correct logic output for an input noise variation of up to approximately 40% of the $V_{DD}$.

**Example MS.13.1** *continued*

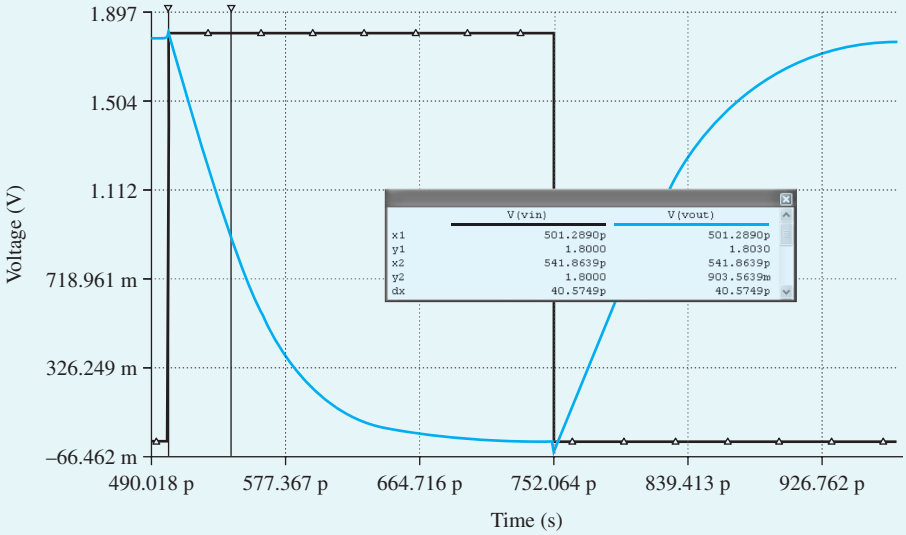



**Figure B.115** Time domain response of the CMOS inverter to measure $t_{PHL}$.

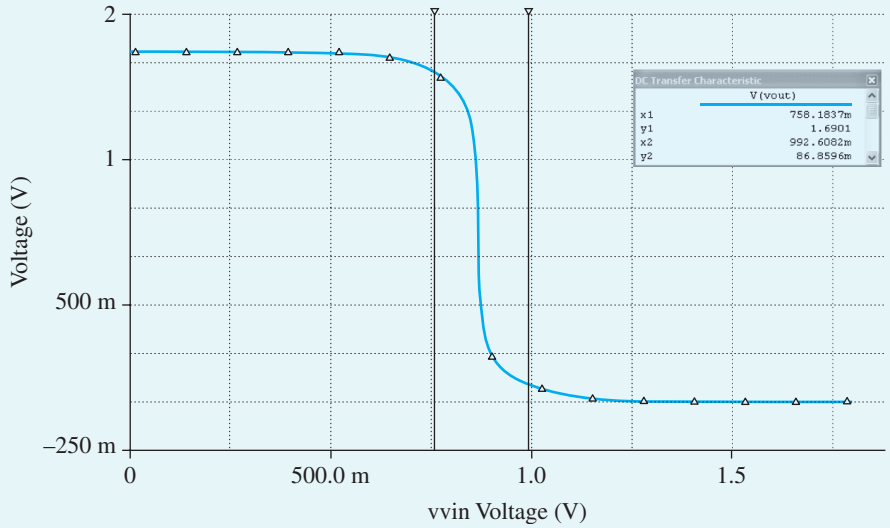



**Figure B.116** Output voltage versus input voltage for the inverter (to measure low and high noise margins $NM_L$ and $NM_H$).

The threshold voltage $V_M$ of the CMOS inverter is defined as the input voltage $v_{\text{IN}}$ that results in an identical switching output voltage $v_{\text{OUT}}$, that is,

$$V_M = v_{\text{IN}} \big| v_{OUT} = v_{IN}$$

Thus, as shown in Fig. B.117, $V_M$ is at the intersection of the VTC with the straight line corresponding to $v_{\text{OUT}} = v_{\text{IN}}$. This line can be simply generated by plotting $v_{\text{IN}}$ on the vertical axis, in addition to $v_{\text{OUT}}$. Note that $V_M = 0.87$ V, which is very close to the desired value of $V_{DD}/2 = 0.9$V, as desired.

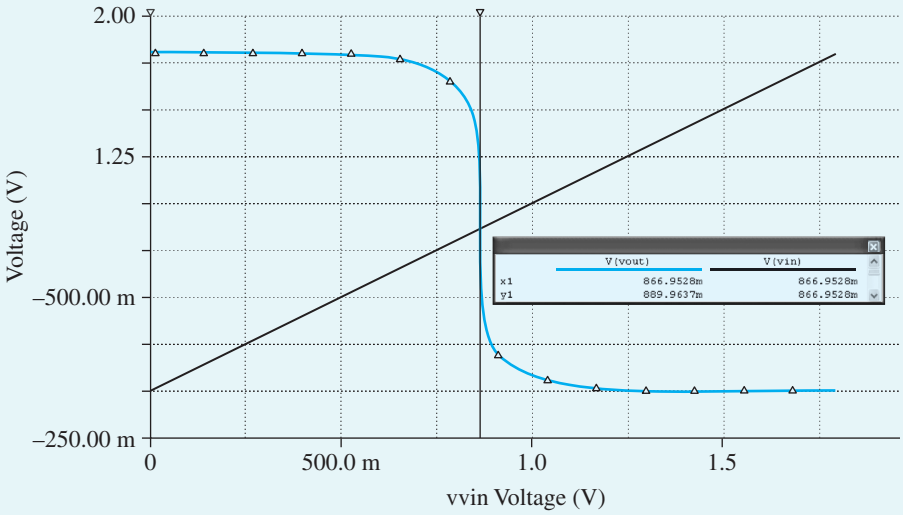



**Figure B.117** Output voltage versus input voltage for the inverter (to the threshold voltage measure $V_{th}$).

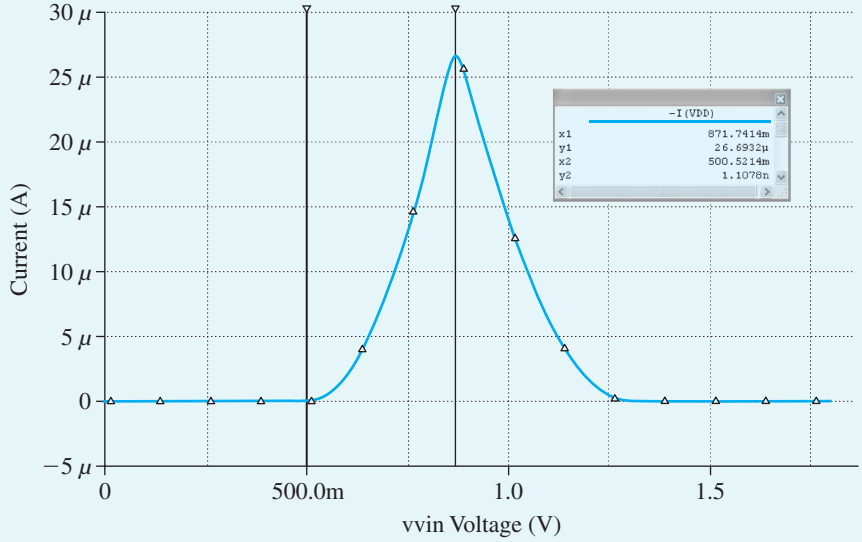



**Figure B.118** Supply current versus input voltage for the inverter.

Finally, the supply current is plotted versus input voltage in Fig. B.118. Observe that in the transition region, where the inverter is switching, the current is no longer zero. Specifically, the peak current occurs at the inverter threshold voltage.