5.11 THE JUNCTION FIELD-EFFECT TRANSISTOR (JFET)

The **junction field-effect transistor,** or JFET, is perhaps the simplest transistor available. It has some important characteristics, notably a very high input resistance. Unfortunately, however (for the JFET), the MOSFET has an even higher input resistance. This, together with the many other advantages of MOS transistors, has made the JFET virtually obsolete. Currently, its applications are limited to discrete-circuit design, where it is used both as an amplifier and as a switch. Its integrated-circuit applications are limited to the design of the differential input stage of some operational amplifiers, where advantage is taken of its high input resistance (compared to the BJT). In this section, we briefly consider JFET operation and characteristics. Another important reason for including the JFET in the study of electronics is that it helps in understanding the operation of gallium arsenide devices, the subject of the next section.

Device Structure

As with other FET types, the JFET is available in two polarities: *n*-channel and *p*-channel. Fig. 5.69(a) shows a simplified structure of the *n*-channel JFET. It consists of a slab of *n*-type silicon with *p*-type regions diffused on its two sides. The *n* region is the channel, and the *p*-type regions are electrically connected together and form the gate. The device operation is based on reverse-biasing the *pn* junction between gate and channel. Indeed, it is the reverse bias on this junction that is used to control the channel width and hence the current flow from drain to source. The major role that this *pn* junction plays in the operation of this FET has given rise to its name: Junction Field-Effect Transistor (JFET).

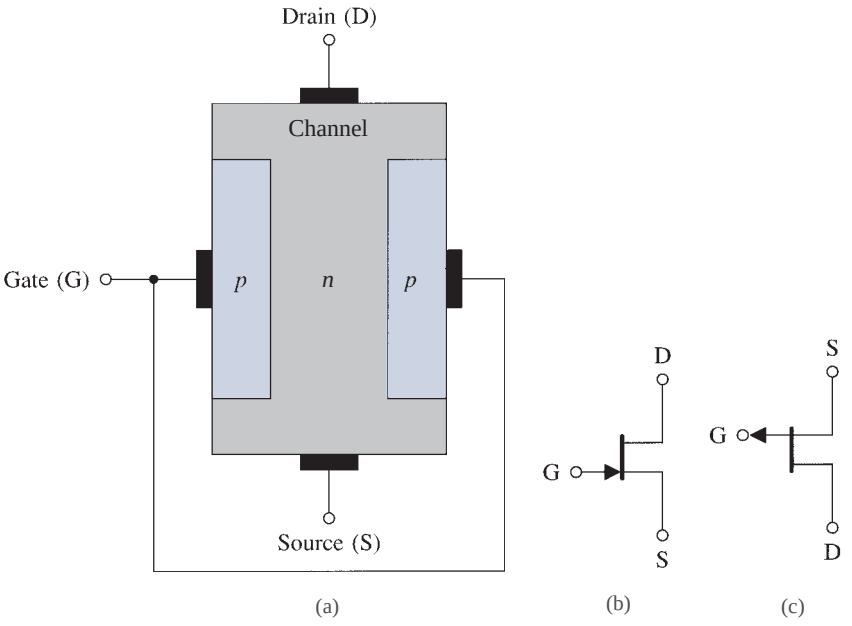


FIGURE 5.69 **(a)** Basic structure of *n*-channel JFET. This is a simplified structure utilized to explain device operation. **(b)** Circuit symbol for the *n*-channel JFET. **(c)** Circuit symbol for the *p*-channel JFET.

It should be obvious that a *p*-channel device can be fabricated by simply reversing all the semiconductor types, thus using *p*-type silicon for the channel and *n*-type silicon for the gate regions.

Figures 5.69(b) and (c) show the circuit symbols for JFETs of both polarities. Observe that the device polarity (*n*-channel or *p*-channel) is indicated by the direction of the arrowhead on the gate line. This arrowhead points in the forward direction of the gate–channel *pn* junction. Although the JFET is a symmetrical device whose source and drain can be interchanged, it is useful in circuit design to designate one of these two terminals as source and the other as drain. The circuit symbol achieves this designation by placing the gate closer to the source than to the drain.

Physical Operation

Consider an *n*-channel JFET and refer to Fig. 5.70(a). (Note that to simplify matters, we will not show the electrical connection between the gate terminals; it is assumed, however, that the two terminals labeled G are joined together.) With $v_{GS} = 0$, the application of a voltage v_{DS} causes current to flow from the drain to the source. When a negative v_{GS} is applied, the depletion region of the gate–channel junction widens and the channel becomes correspondingly narrower; thus the channel resistance increases and the current i_D (for a given v_{DS}) decreases. Because v_{DS} is small, the channel is almost of uniform width. The JFET is simply operating as a resistance whose value is controlled by v_{GS}. If we keep increasing v_{GS} in the negative direction, a value is reached at which the depletion region occupies the entire channel. At this value of v_{GS} the channel is completely depleted of charge carriers (electrons); the channel has in effect disappeared. This value of v_{GS} is therefore the threshold voltage of the device, V_t, which is obviously negative for an *n*-channel JFET. For JFETs the threshold voltage is called the **pinch-off voltage** and is denoted V_P.

Consider next the situation depicted in Fig. 5.70(b). Here v_{GS} is held constant at a value greater (that is, less negative) than V_P, and v_{DS} is increased. Since v_{DS} appears as a voltage drop across the length of the channel, the voltage increases as we move along the channel from source to drain. It follows that the reverse-bias voltage between gate and channel varies at different points along the channel and is highest at the drain end. Thus the channel acquires a tapered shape and the i_D–v_{DS} characteristic becomes nonlinear. When the reverse bias at the drain end, v_{GD}, falls below the pinch-off voltage V_P, the channel is pinched off at the drain end and the drain current saturates. The remainder of the description of JFET operation follows closely that given for the depletion MOSFET.

The description above clearly indicates that the JFET is a depletion-type device. Its characteristics should therefore be similar to those of the depletion-type MOSFET. This is true with a very important exception: While it is possible to operate the depletion-type MOSFET in the enhancement mode (by simply applying a positive v_{GS} if the device is *n* channel) this is impossible in the JFET case. If we attempt to apply a positive v_{GS}, the gate–channel *pn* junction becomes forward biased and the gate ceases to control the channel. Thus the maximum v_{GS} is limited to 0 V, though it is possible to go as high as 0.3 V or so since a *pn* junction remains essentially cut off at such a small forward voltage.

Current–Voltage Characteristics

The current–voltage characteristics of the JFET are identical to those of the depletion-mode MOSFET studied in Section 5.3 except that for the JFET the maximum v_{GS} allowed is

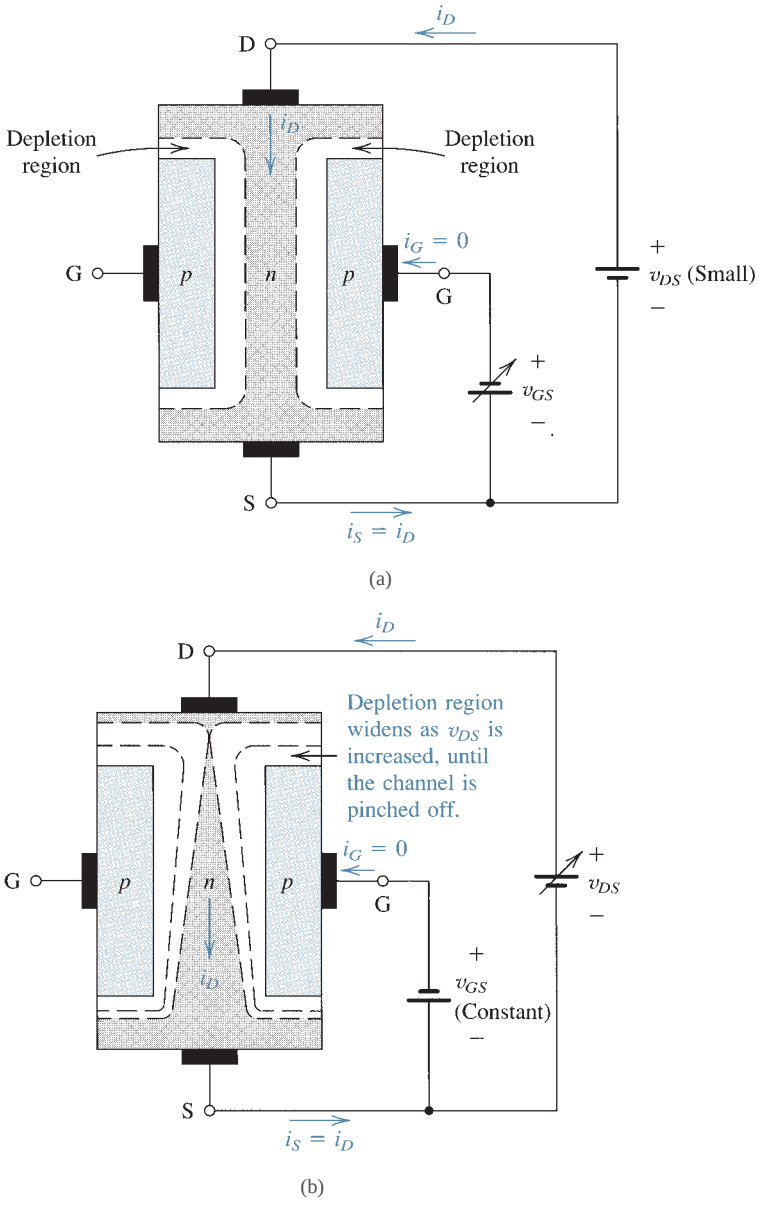


FIGURE 5.70 Physical operation of the *n*-channel JFET: **(a)** For small v_{DS} the channel is uniform and the device functions as a resistance whose value is controlled by v_{GS}. **(b)** Increasing v_{DS} causes the channel to acquire a tapered shape and eventually pinch-off occurs. Note that, though not shown, the two gate regions are electrically connected.

normally 0 V. Furthermore, the JFET is specified in terms of the pinch-off voltage V_P (equal to V_t of the MOSFET) and the *d*rain-to-source current with the gate shorted to the source, I_{DSS}, which corresponds to $\frac{1}{2}k_n'V_t^2$ for the MOSFET. With these substitutions, the *n*-channel JFET characteristics can be described as follows:

Cutoff: $v_{GS} \leq V_P$, $i_D = 0$

Triode region: $V_P \le v_{GS} \le 0$, $v_{DS} \le v_{GS} - V_P$

$$i_D = I_{DSS}\left[2\left(1 - \frac{v_{GS}}{V_P}\right)\left(\frac{v_{DS}}{-V_P}\right) - \left(\frac{v_{DS}}{V_P}\right)^2\right] \tag{5.116}$$

Saturation (pinch-off) region: $V_P \le v_{GS} \le 0$, $v_{DS} \ge v_{GS} - V_P$

$$i_D = I_{DSS}\left(1 - \frac{v_{GS}}{V_P}\right)^2 (1 + \lambda v_{DS}) \tag{5.117}$$

where λ is the inverse of the Early voltage; $\lambda = 1/V_A$, and V_A and λ are positive for *n*-channel devices.

Recalling that for an *n*-channel device, V_P is negative, we see that operation in the pinch-off region is obtained when the drain voltage is greater than the gate voltage by at least $|V_P|$.

Since the gate–channel junction is always reverse-biased, only a leakage current flows through the gate terminal. From Chapter 3, we know that such a current is of the order of 10^{-9} A. Although i_G is very small, and is assumed zero in almost all applications, it should be noted that the gate current in a JFET is many orders of magnitude greater than the gate current in a MOSFET. Of course the latter is so tiny because of the insulated gate structure. Another complication arises in the JFET because of the strong dependence of gate leakage current on temperature—approximately doubling for every 10°C rise in temperature, just as in the case of a reverse-biased diode (see Chapter 3).

The *p*-Channel JFET

The current–voltage characteristics of the *p*-channel JFET are described by the same equations as the *n*-channel JFET. Note, however, that for the *p*-channel JFET, V_P is positive, $0 \le v_{GS} \le V_P$, v_{DS} is negative, λ and V_A are negative, and the current i_D flows out of the drain terminal. To operate the *p*-channel JFET in pinch-off, $v_{DS} \le v_{GS} - V_P$, which in words means that the drain voltage must be lower than the gate voltage by at least $|V_P|$. Otherwise, with $v_{DS} \ge v_{GS} - V_P$, the *p*-channel JFET operates in the triode region.

The JFET Small-Signal Model

The JFET small-signal model is identical to that of the MOSFET [see Fig. 5.34(b)]. Here, g_m is given by

$$g_m = \left(\frac{2I_{DSS}}{|V_P|}\right)\left(1 - \frac{V_{GS}}{V_P}\right) \tag{5.118a}$$

or alternatively by

$$g_m = \left(\frac{2I_{DSS}}{|V_P|}\right)\sqrt{\frac{I_D}{I_{DSS}}} \tag{5.118b}$$

where V_{GS} and I_D are the dc bias quantities, and

$$r_o = \frac{|V_A|}{I_D} \tag{5.119}$$

At high frequencies, the equivalent circuit of Fig. 5.67(c) applies with C_{gs} and C_{gd} being both depletion capacitances. Typically, $C_{gs} = 1$ to 3 pF, $C_{gd} = 0.1$ to 0.5 pF, and $f_T = 20$ to 100 MHz.

EXERCISES

In Exercises 5.43 to 5.46, let the *n*-channel JFET have $V_P = -4$ V and $I_{DSS} = 10$ mA, and unless otherwise specified assume that in pinch-off (saturation) the output resistance is infinite.

5.43 For $v_{GS} = -2$ V, find the minimum v_{DS} for the device to operate in pinch-off. Calculate i_D for $v_{GS} = -2$ V and $v_{DS} = 3$ V.

Ans. 2 V; 2.5 mA

5.44 For $v_{DS} = 3$ V, find the change in i_D corresponding to a change in v_{GS} from −2 to −1.6 V.

Ans. 1.1 mA

5.45 For small v_{DS}, calculate the value of r_{DS} at $v_{GS} = 0$ V and at $v_{GS} = -3$ V.

Ans. 200 Ω; 800 Ω

5.46 If $V_A = 100$ V, find the JFET output resistance r_o when operating in pinch-off at a current of 1 mA, 2.5 mA, and 10 mA.

Ans. 100 kΩ; 40 kΩ; 10 kΩ

D5.47 The JFET in the circuit of Fig. E5.47 has $V_P = -3$ V, $I_{DSS} = 9$ mA, and $\lambda = 0$. Find the values of all resistors so that $V_G = 5$ V, $I_D = 4$ mA, and $V_D = 11$ V. Design for 0.05 mA in the voltage divider.

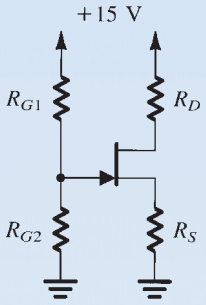


FIGURE E5.47

Ans. $R_{G1} = 200$ kΩ; $R_{G2} = 100$ kΩ; $R_S = 1.5$ kΩ; $R_D = 1$ kΩ

5.48 For the JFET circuit designed in Exercise 5.47, let an input signal v_i be capacitively coupled to the gate, a large bypass capacitor be connected between the source and ground, and the output signal v_o be taken from the drain through a large coupling capacitor. The resulting common-source amplifier is shown in Fig. E5.48. Calculate g_m and r_o (assuming $V_A = 100$ V). Also find R_i, $A_v \equiv (v_o/v_i)$, and R_o.

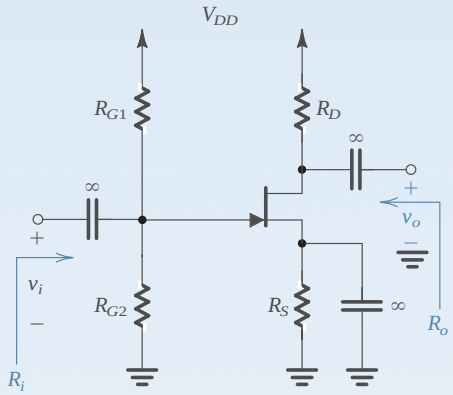


FIGURE E5.48

Ans. 4 mA/V; 25 kΩ; 66.7 kΩ; −3.8 V/V; 962 Ω

5.12 GALLIUM ARSENIDE (GaAs) DEVICES—THE MESFET[10]

The devices discussed thus far, and indeed the devices used in most of the circuits studied in this book, are made of silicon. This reflects the situation that has existed in the microelectronics industry for at least three decades. Furthermore, owing to the advances that are continually being made in silicon device and circuit technologies, the dominance of silicon as the most useful semiconductor material is expected to continue for many years to come. Nevertheless, another semiconductor material has been making inroads into digital applications that require extremely high speeds of operation and analog applications that require very high operating frequencies. We refer to gallium arsenide (GaAs), a compound semiconductor formed of gallium, which is in the third column of the periodic table of elements, and arsenic, which is in the fifth column; thus GaAs is known as a III-V semiconductor.

The major advantage that GaAs offers over silicon is that electrons travel much faster in *n*-type GaAs than in silicon. This is a result of the fact that the electron drift mobility μ_n (which is the constant that relates the electron drift velocity to the electric field; velocity = $\mu_n E$) is five to ten times higher in GaAs than in silicon. Thus for the same input voltages, GaAs devices have higher output currents, and thus higher g_m, than the corresponding silicon devices. The larger output currents enable faster charging and discharging of load and parasitic capacitances and thus result in increased speeds of operation.

Gallium arsenide devices have been used for some years in the design of discrete-component amplifiers for microwave applications (in the 10^9 Hz or GHz frequency range). More recently, GaAs has begun to be employed in the design of very-high-speed digital integrated circuits and in analog ICs, such as op amps, that operate in the hundreds of MHz frequency range. Although the technology is still relatively immature, suffering from yield and reliability problems and generally limited to low levels of integration, it offers great potential. Therefore, this book includes a brief study of GaAs devices and circuits. Specifically, the basic GaAs devices are studied in this section; their basic amplifier circuit configurations are discussed in Section 6.8; and GaAs digital circuits are studied in Section 14.8.

The Basic GaAs Devices

Although there are a number of GaAs technologies currently in various stages of development, we shall study the most mature of these technologies. The active device available in this technology is an *n*-channel field effect transistor known as the **metal semiconductor FET** or **MESFET.** The technology also provides a type of diode known as the **Schottky-barrier diode (SBD).** (Recall that the SBD was briefly introduced in Section 3.9.) The structure of these two basic devices is illustrated by their cross sections, depicted in Fig. 5.71. The GaAs circuit is formed on an undoped GaAs substrate. Since the conductivity of undoped GaAs is very low, the substrate is said to be semi-insulating. This turns out to be an advantage for GaAs technology as it simplifies the process of isolating the devices on the chip from one another, as well as resulting in smaller parasitic capacitances between the devices and the circuit ground.

As indicated in Fig. 5.71, a Schottky-barrier diode consists of a metal–semiconductor junction. The metal, referred to as the Schottky-barrier metal to distinguish it from the different kind of metal used to make a contact (see Long and Butner (1990) for a detailed explanation of the difference), forms the anode of the diode. The *n*-type GaAs forms the

[10] The material in this section is required only for the study of the GaAs circuits in Sections 6.8 and 14.8. Otherwise, this section can be skipped without loss of continuity.

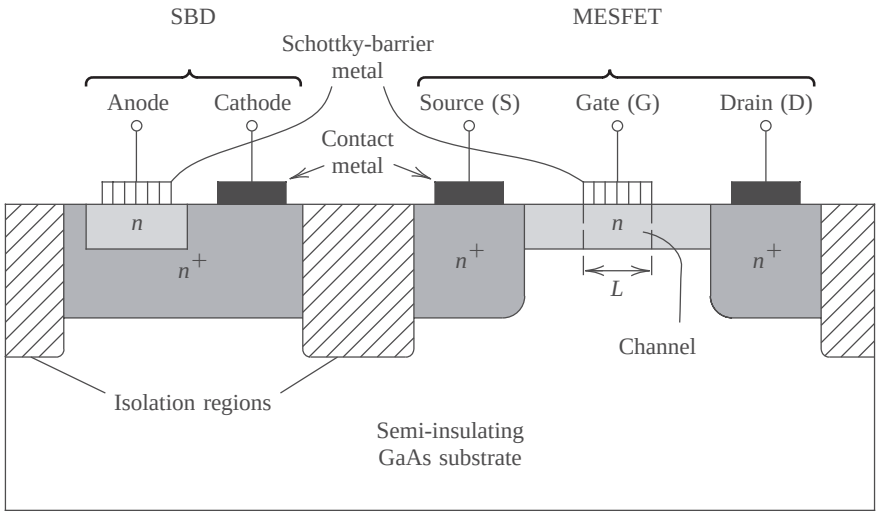


FIGURE 5.71 Cross-section of a GaAs Schottky-barrier diode (SBD) and a MESFET.

cathode. Note that heavily doped *n*-type GaAs (indicated by n^+) is used between the *n* region and the cathode metal contact in order to keep the parasitic series resistance low.

The gate of the MESFET is formed by Schottky-barrier metal in direct contact with the *n*-type GaAs that forms the channel region. The channel length L is defined by the length of the gate electrode, and similarly for the width W (in the direction perpendicular to the page). To reduce the parasitic resistances between the drain and source contacts and the channel, the two contacts are surrounded with heavily doped (n^+) GaAs.

Since the main reason for using GaAs circuits is to achieve high speed/frequency of operation, the channel length is made as small as possible. Typically $L = 0.2$–2 μm. Also, usually all the transistors on the IC chip are made to have the same length, leaving only the width W of each device to be specified by the circuit designer.

Only *n*-channel MESFETs are available in GaAs technology. This is because holes have a relatively low drift mobility in GaAs, making *p*-channel MESFETs unattractive. The lack of complementary transistors is a definite disadvantage of GaAs technology. Correspondingly, it makes the task of the circuit designer even more challenging than usual.

Device Operation

The MESFET operates in a very similar manner to the JFET, with the Schottky metal playing the role of the *p*-type gate of the JFET (refer to Fig. 5.69). Basically, a depletion region forms in the channel below the gate surface, and the thickness of the depletion region is controlled by the gate voltage v_{GS}. This in turn effects control over the channel dimensions and thus on the current that flows from drain to source in response to an applied v_{DS}. The latter voltage causes the channel to have a tapered shape, with pinch-off eventually occurring at the drain end of the channel.

The most common GaAs MESFETs available are of the depletion type with a threshold voltage V_t (or, equivalently, pinch-off voltage V_P) in the range of –0.5 to –2.5 V. These devices can be operated with v_{GS} values ranging from the negative V_t to positive values as high as a few tenths of a volt. However, as v_{GS} reaches 0.7 V or so, the Schottky-barrier diode between gate and channel conducts heavily and the gate voltage no longer effectively

controls the drain-to-source current. Gate conduction, which is not possible in MOSFETs, is another definite disadvantage of the MESFET.

Although less common, enhancement-mode MESFETs are available in certain technologies. These normally-off devices are obtained by arranging that the depletion region existing at $v_{GS} = 0$ extends through the entire channel depth, thus blocking the channel and causing $i_D = 0$. To cause current to flow from drain to source the channel must be opened by applying to the gate a positive voltage of sufficient magnitude to reduce the thickness of the depletion region below that of the channel region. Typically, the threshold voltage V_t is between 0.1 and 0.3 V.

The above description of MESFET operation suggests that the i_D–v_{DS} characteristics should saturate at $v_{DS} = v_{GS} - V_t$, as is the case in a silicon JFET. It has been observed, however, that the i_D–v_{DS} characteristics of GaAs MESFETs saturate at lower values of v_{DS} and, furthermore, that the saturation voltages v_{DSsat} do not depend strongly on the value of v_{GS}. This "early saturation" phenomenon comes about because the velocity of the electrons in the channel does not remain proportional to the electric field (which in turn is determined by v_{DS} and L; $E = v_{DS}/L$) as is the case in silicon; rather, the electron velocity reaches a high peak value and then saturates (that is, becomes constant independent of v_{DS}). The velocity-saturation effect is even more pronounced in short-channel devices ($L \leq 1\ \mu$m), occurring at values of v_{DS} lower than $(v_{GS} - V_t)$.

Finally, a few words about the operation of the Schottky-barrier diode. Forward current is conducted by the majority carriers (electrons) flowing into the Schottky-barrier metal (the anode). Unlike the *pn*-junction diode, minority carriers play no role in the operation of the SBD. As a result, the SBD does not exhibit minority-carrier storage effects, which give rise to the diffusion capacitance of the *pn*-junction diode. Thus, the SBD has only one capacitive effect, that associated with the depletion-layer capacitance C_j.

Device Characteristics and Models

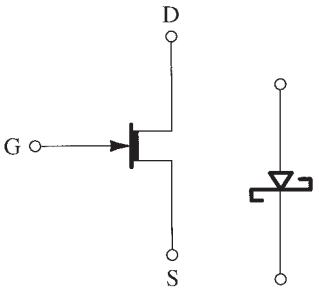
A first-order model for the MESFET, suitable for hand calculations, is obtained by neglecting the velocity-saturation effect, and thus the resulting model is almost identical to that of the JFET though expressed somewhat differently in order to correspond to the literature:

$$\begin{aligned} i_D &= 0 \qquad \text{for } v_{GS} < V_t \\ i_D &= \beta[2(v_{GS} - V_t)v_{DS} - v_{DS}^2](1 + \lambda v_{DS}) \qquad \text{for } v_{GS} \geq V_t,\ v_{DS} < v_{GS} - V_t \\ i_D &= \beta(v_{GS} - V_t)^2(1 + \lambda v_{DS}) \qquad \text{for } v_{GS} \geq V_t,\ v_{DS} \geq v_{GS} - V_t \end{aligned} \tag{5.120}$$

The only differences between these equations and those for the JFETs are (1) the channel-length modulation factor, $1 + \lambda v_{DS}$, is included also in the equation describing the triode region (also called the ohmic region) simply because λ of the MESFET is rather large and including this factor results in a better fit to measured characteristics; and (2) a transconductance parameter β is used so as to correspond with the MESFET literature. Obviously, β is related to I_{DSS} of the JFET and $k'(W/L)$ of the MOSFET. (Note, however, that this β has absolutely nothing to do with β of the BJT!)

A modification of this model to account for the early saturation effects is given in Hodges and Jackson (1988).

Figure 5.72(a) shows the circuit symbol for the depletion-type *n*-channel GaAs MESFET. Since only one type of transistor (*n* channel) is available, all devices will be drawn the



(a) (b)

FIGURE 5.72 Circuit symbols for **(a)** an *n*-channel depletion-type GaAs MESFET, and **(b)** a Schottky-barrier diode (SBD).

same way, and there should be no confusion as to which terminal is the drain and which is the source.

The circuit symbol of the Schottky-barrier diode is depicted in Fig. 5.72(b). In spite of the fact that the physical operation of the SBD differs from that of the *pn*-junction diode, their *i–v* characteristics are identical. Thus the *i–v* characteristic of the SBD is given by the same exponential relationship studied in Chapter 3. For the GaAs SBD, the constant n is typically in the range of 1 to 1.2.

The small-signal model of the MESFET is identical to that of other FET types. The parameter values are given by

$$g_m = 2\beta(V_{GS} - V_t)(1 + \lambda V_{DS}) \tag{5.121}$$

$$r_o \equiv \left[\frac{\partial i_D}{\partial v_{DS}}\right]^{-1} = 1/\lambda\beta(V_{GS} - V_t)^2 \tag{5.122}$$

The MESFET, however, has a rather high value for λ (0.1 to 0.3 V^{-1}) which results in a small output resistance r_o. This turns out to be a serious drawback of GaAs MESFET technology, resulting in low voltage-gain obtainable from each stage. Furthermore, it has been found that r_o decreases at high frequencies. Circuit design techniques for coping with the low r_o will be presented in Section 6.8.

For easy reference, Table 5.2 gives typical values for device parameters in a GaAs MESFET technology. The devices in this technology have a channel length $L = 1$ μm. The values given are for a device with a width $W = 1$ μm. The parameter values for actual devices can be obtained by appropriately scaling by the width W. This process is illustrated in the following example. Unless otherwise specified, the values of Table 5.2 are to be used for the exercises and the end-of-chapter problems.

TABLE 5.2 **Typical Parameter Values for GaAs MESFETS and Schottky Diodes in $L = 1$ μm Technology, Normalized for $W = 1$ μm**

V_t	-1.0 V
β	10^{-4} A/V^2
λ	0.1 V^{-1}
I_S	10^{-15} A
n	1.1

EXAMPLE 5.11

Figure 5.73 shows a simple GaAs MESFET amplifier, with the W values of the transistors indicated. Assume that the dc component of v_I, that is V_{GS1}, biases Q_1 at the current provided by the current source Q_2 so that both devices operate in saturation and that the dc output is at half of the supply voltage. Find:

(a) the β values for Q_1 and Q_2;

(b) V_{GS1};

(c) g_{m1}, r_{o1}, and r_{o2}; and

(d) the small-signal voltage gain.

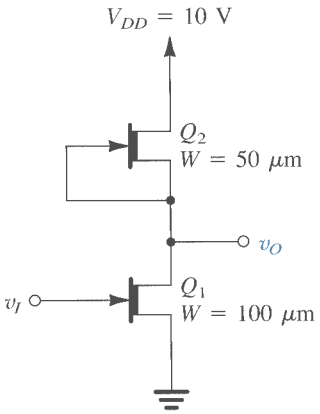


FIGURE 5.73 Circuit for Example 5.11: a simple MESFET amplifier.

Solution

(a) The values of β can be obtained by scaling the value given in Table 5.2 using the specified values of W,

$$\beta_1 = 100 \times 10^{-4} = 10^{-2}\ \text{A/V}^2 = 10\ \text{mA/V}^2$$
$$\beta_2 = 50 \times 10^{-4} = 5 \times 10^{-3}\ \text{A/V}^2 = 5\ \text{mA/V}^2$$

(b)

$$\begin{aligned} I_{D2} &= \beta_2 (V_{GS2} - V_t)^2 (1 + \lambda V_{DS2}) \\ &= 5(0 + 1)^2 (1 + 0.1 \times 5) \\ &= 7.5\ \text{mA} \end{aligned}$$

$$\begin{aligned} I_{D1} &= I_{D2} = 7.5\ \text{mA} \\ 7.5 &= \beta_1 (V_{GS1} - V_t)^2 (1 + \lambda V_{DS1}) \\ &= 10(V_{GS1} + 1)^2 (1 + 0.1 \times 5) \end{aligned}$$

Thus,

$$V_{GS1} = -0.3\ \text{V}$$

(c)

$$g_{m1} = 2 \times 10(-0.3 + 1)(1 + 0.1 \times 5)$$
$$= 21 \text{ mA/V}$$
$$r_{o1} = \frac{1}{0.1 \times 10(-0.3 + 1)^2} = 2 \text{ k}\Omega$$
$$r_{o2} = \frac{1}{0.1 \times 5(0 + 1)^2} = 2 \text{ k}\Omega$$

(d)

$$A_v = -g_{m1}(r_{o1} /\!/ r_{o2})$$
$$= -21 \times (2 /\!/ 2) = -21 \text{ V/V}$$

EXERCISE

5.49 For a MESFET with the gate shorted to the source and having $W = 10$ μm, find the minimum voltage between drain and source to operate in saturation. For $V_{DS} = 5$ V, find the current I_D. What is the output resistance of this current source?

Ans. 1 V; 1.5 mA; 10 kΩ

As already mentioned, the main reason for using GaAs devices and circuits is their high frequency and high speed of operation. A remark is therefore in order on the internal capacitances and f_T of GaAs transistors. For a particular GaAs technology with $L = 1$ μm, C_{gs} (at $V_{GS} = 0$ V) is 1.6 fF/μm-width, and C_{gd} (at $V_{DS} = 2$ V) is 0.16 fF/μm-width. Thus for a MESFET with $W = 100$ μm, $C_{gs} = 0.16$ pF and $C_{gd} = 0.016$ pF. f_T typically ranges from 5 to 15 GHz.

6.8 GaAs AMPLIFIERS[3]

Gallium arsenide (GaAs) technology makes possible the design of amplifiers having very wide bandwidths, in the hundreds of megahertz or even gigahertz range. In this section we shall study some of the circuit design techniques that have been developed over the last few years for the design of GaAs amplifiers. As will be seen, these techniques aim to circumvent the major problem of the MESFET, namely, its low output resistance in saturation. Before proceeding with this section the reader is advised to review the material on GaAs devices presented in Section 5.12.

Current Sources

Current sources play a fundamental role in the design of integrated-circuit amplifiers, being employed both for biasing and as active loads. In GaAs technology, the simplest way to implement a current source is to connect the gate of a depletion-type MESFET to its source,

[3] This section can be omitted with no loss in continuity.

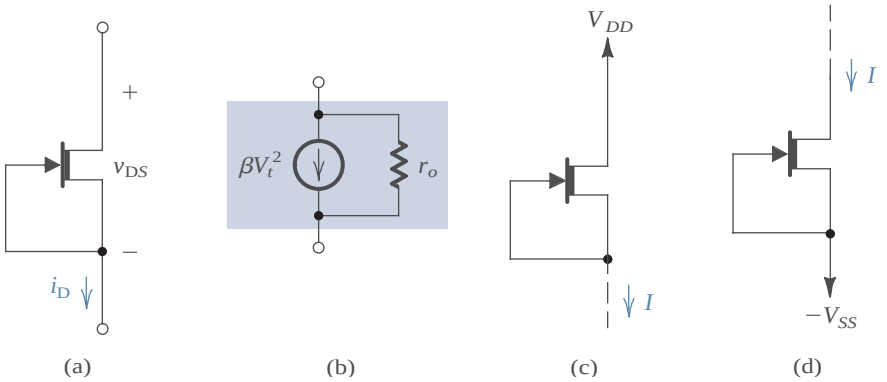


FIGURE 6.39 **(a)** The basic MESFET current source; **(b)** equivalent circuit of the current source; **(c)** the current source connected to a positive power supply to source currents to loads at voltages $\leq V_{DD} - |V_t|$; **(d)** the current source connected to a negative power supply to sink currents from loads at voltages $\geq -V_{SS} + |V_t|$.

as shown in Fig. 6.39(a). Provided that v_{DS} is maintained greater than $|V_t|$, the MESFET will operate in saturation and the current i_D will be

$$i_D = \beta V_t^2 (1 + \lambda v_{DS}) \tag{6.126}$$

Thus the current source will have the equivalent circuit shown in Fig. 6.39(b), where the output resistance is the MESFET r_o,

$$r_o = 1/\lambda\beta V_t^2 \tag{6.127}$$

In JFET terminology, $\beta V_t^2 = I_{DSS}$ and $\lambda = 1/|V_A|$; thus

$$r_o = |V_A|/I_{DSS} \tag{6.128}$$

Since for the MESFET, λ is relatively high (0.1 to 0.3 V^{-1}) the output resistance of the current source of Fig. 6.39(a) is usually low, rendering this current-source realization inadequate for most applications. Before considering means for increasing the effective output resistance of the current source, we show in Fig. 6.39(c) how the basic current source can be connected to *source* currents to a load whose voltage can be as high as $V_{DD} - |V_t|$. Alternatively, the same device can be connected as shown in Fig. 6.39(d) to *sink* currents from a load whose voltage can be as low as $-V_{SS} + |V_t|$.

EXERCISE

6.23 Using the device data given in Table 5.2 (page 456), find the current provided by a 10-μm-wide MESFET connected in the current-source configuration. Let the source be connected to a –5-V supply and find the current when the drain voltage is –4V. What is the output resistance of the current source? What change in current occurs if the drain voltage is raised by +4V?

Ans. 1.1 mA; 10 kΩ; 0.4 mA

A Cascode Current Source

The output resistance of the current source can be increased by utilizing the cascode configuration as shown in Fig. 6.40. The output resistance R_o of the cascode current source can be

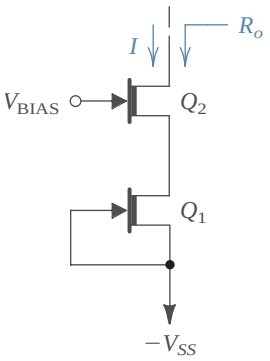


FIGURE 6.40 Adding the cascode transistor Q_2 increases the output resistance of the current source by the factor $g_{m2}r_{o2}$; that is, $R_o = g_{m2}r_{o2}r_{o1}$.

found by using Eq. (6.116),

$$R_o \simeq g_{m2}r_{o2}r_{o1} \tag{6.129}$$

Thus, adding the cascode transistor Q_2 raises the output resistance of the current source by the factor $g_{m2}r_{o2}$, which is the intrinsic voltage gain of Q_2. For GaAs MESFETs, $g_{m2}r_{o2}$ is typically 10 to 40. To allow a wide range of voltages at the output of the cascode current source, V_{BIAS} should be the lowest value that results in Q_1 operating in saturation.

EXERCISE

D6.24 For the cascode current source of Fig. 6.40 let $V_{SS} = 5$ V, $W_1 = 10$ μm, and $W_2 = 20$ μm, and assume that the devices have the typical parameter values given in Table 5.2. (a) Find the value of V_{BIAS} that will result in Q_1 operating at the edge of the saturation region (i.e., $V_{DS1} = |V_t|$) when the voltage at the output is –3 V. (b) What is the lowest allowable voltage at the current-source output? (c) What value of output current is obtained for $V_O = -3$ V? (d) What is the output resistance of the current source? (e) What change in output current results when the output voltage is raised from –3 V to +1 V?

Ans. (a) –4.3 V; (b) –3.3 V; (c) 1.1 mA; (d) 310 kΩ; (e) 0.013 mA

Increasing the Output Resistance by Bootstrapping

Another technique frequently employed to increase the effective output resistance of a MESFET, including the current-source-connected MESFET, is known as **bootstrapping.** The bootstrapping idea is illustrated in Fig. 6.41(a). Here the circuit inside the box senses the voltage at the bottom node of the current source, v_A, and causes a voltage v_B to appear at the top node of a value

$$v_B = V_S + \alpha v_A \tag{6.130}$$

where V_S is the dc voltage required to operate the current-source transistor in saturation ($V_S \geq |V_t|$) and α is a constant ≤1. The incremental output resistance of the bootstrapped current source can be found by causing the voltage v_A to increase by an increment v_a. From Eq. (6.130) we find that the resulting increment in v_B is $v_b = \alpha v_a$. The incremental current through the current source is therefore $(v_a - v_b)/r_o$ or $(1 - \alpha)v_a/r_o$. Thus the output resistance R_o is

$$R_o = \frac{v_a}{(1-\alpha)v_a/r_o} = \frac{r_o}{1-\alpha} \tag{6.131}$$

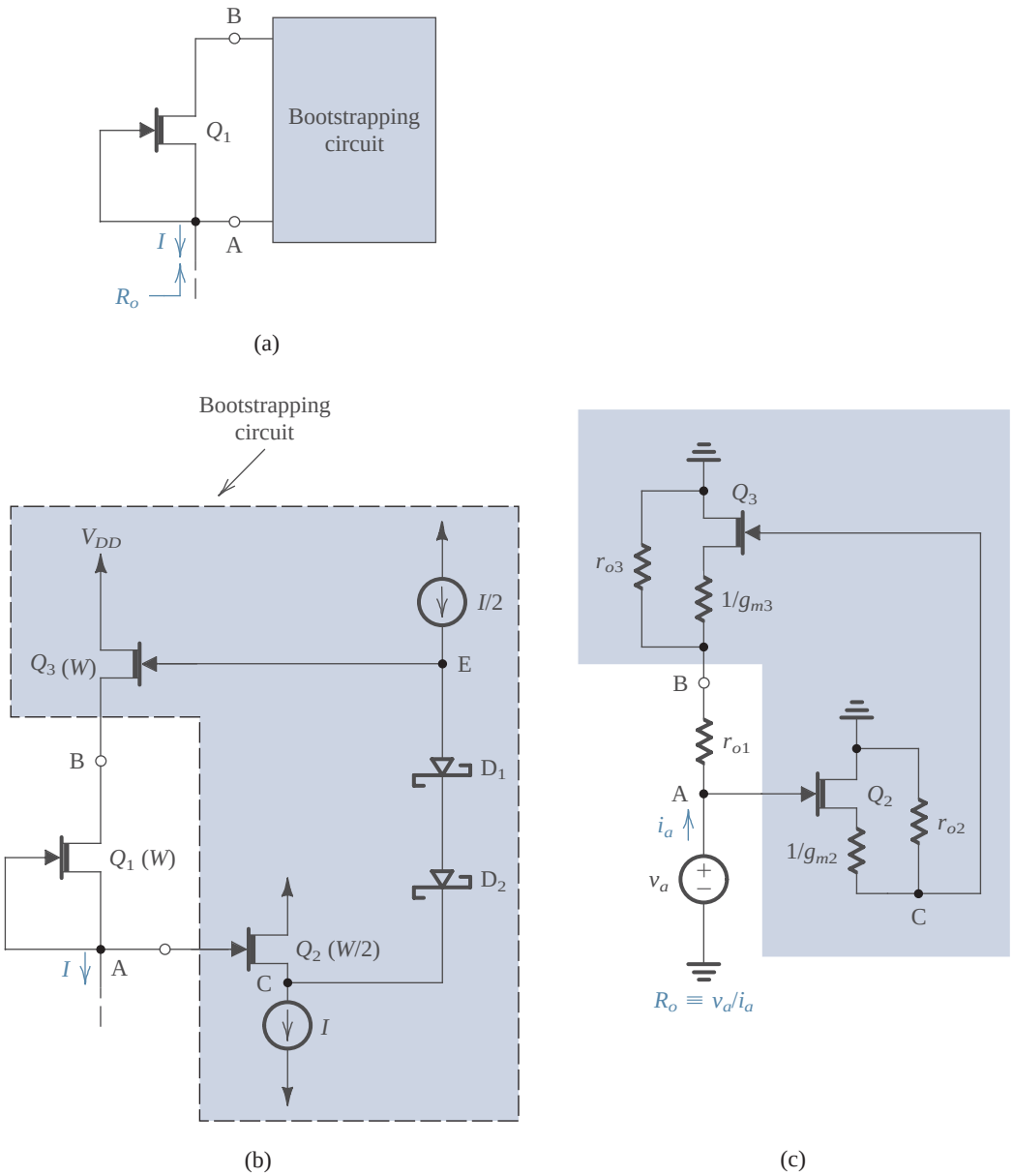


FIGURE 6.41 Bootstrapping of a MESFET current source Q_1: **(a)** basic arrangement; **(b)** an implementation; **(c)** small-signal equivalent circuit model of the circuit in (b), for the purpose of determining the output resistance R_o.

Thus, bootstrapping increases the output resistance by the factor $1/(1-\alpha)$, which increases as α approaches unity. Perfect bootstrapping is achieved with $\alpha = 1$, resulting in $R_o = \infty$.

From the above we observe that the bootstrapping circuit senses whatever change occurs in the voltage at one terminal of the current source and causes an almost equal change to occur at the other terminal, thus maintaining an almost constant voltage across the current source and minimizing the change in current through the current-source transistor. The

action of the bootstrapping circuit can be likened to that of a person who attempts to lift himself off the ground by pulling on the straps of his boots (!), the origin of the name of this circuit technique, which, incidentally, predates GaAs technology. Bootstrapping is a form of positive feedback; the signal v_b that is fed back by the bootstrapping circuit is in phase with (has the same polarity as) the signal that is being sensed, v_a. Feedback will be studied formally in Chapter 8.

An implementation of the bootstrapped current source is shown in Fig. 6.41(b). Here transistor Q_2 is a source follower used to buffer node A, whose voltage is being sensed. The width of Q_2 is half that of Q_1 and is operating at half the bias current. (Transistors Q_1 and Q_2 are said to operate at the same **current density.**) Thus V_{GS} of Q_2 will be equal to that of Q_1—namely, zero—and hence $V_C = V_A$. The two Schottky diodes behave as a battery of approximately 1.4 V, resulting in the dc voltage at node E being 1.4 V higher than V_C. Note that the signal voltage at node C appears intact at node E; only the dc level is shifted. The diodes are said to perform **level shifting,** a common application of Schottky diodes in GaAs MESFET technology.

Transistor Q_3 is a source follower that is operating at the same current density as Q_1, and thus its V_{GS} must be zero, resulting in $V_B = V_E$. The end result is that the bootstrapping circuit causes a dc voltage of 1.4 V to appear across the current-source transistor Q_1. Provided that $|V_t|$ of Q_1 is less than 1.4 V, Q_1 will be operating in saturation as required.

To determine the output resistance of the bootstrapped current source, apply an incremental voltage v_a to node A, as shown in Fig. 6.41(c). Note that this small-signal equivalent circuit is obtained by implicitly using the T model (including r_o) for each FET and assuming that the Schottky diodes act as a perfect level shifter (that is, as an ideal dc voltage of 1.4 V with zero internal resistance). Analysis of this circuit is straightforward and yields

$$\alpha \equiv \frac{v_b}{v_a} = \frac{g_{m3}r_{o3}\dfrac{g_{m2}r_{o2}}{g_{m2}r_{o2}+1} + \dfrac{r_{o3}}{r_{o1}}}{g_{m3}r_{o3} + \dfrac{r_{o3}}{r_{o1}} + 1} \tag{6.132}$$

which is smaller than, but close to, unity, as required. The output resistance R_o is then obtained as

$$\begin{aligned} R_o \equiv \frac{v_a}{i_a} &= \frac{r_{o1}}{1-\alpha} \\ &= r_{o1}\frac{g_{m3}r_{o3} + (r_{o3}/r_{o1}) + 1}{g_{m3}r_{o3}/(g_{m2}r_{o2}+1) + 1} \end{aligned} \tag{6.133}$$

For $r_{o3} = r_{o1}$, assuming that $g_{m3}r_{o3}$ and $g_{m2}r_{o2}$ are $\gg 1$, and using the relationships for g_m and r_o for Q_2 and Q_3, one can show that

$$R_o \simeq r_{o1}(g_{m3}r_{o3}/2) \tag{6.134}$$

which represents an increase of about an order of magnitude in output resistance. Unfortunately, however, the circuit is rather complex.

A Simple Cascode Configuration–The Composite Transistor

The rather low output resistance of the MESFET places a severe limitation on the performance of MESFET current sources and various MESFET amplifiers. This problem can be alleviated by using the composite MESFET configuration shown in Fig. 6.42(a) in place of a

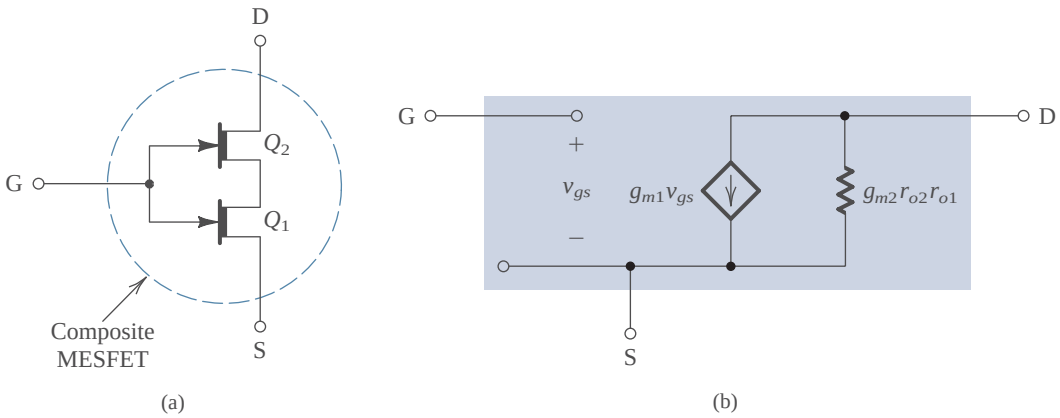


FIGURE 6.42 (**a**) The composite MESFET and (**b**) its small-signal model.

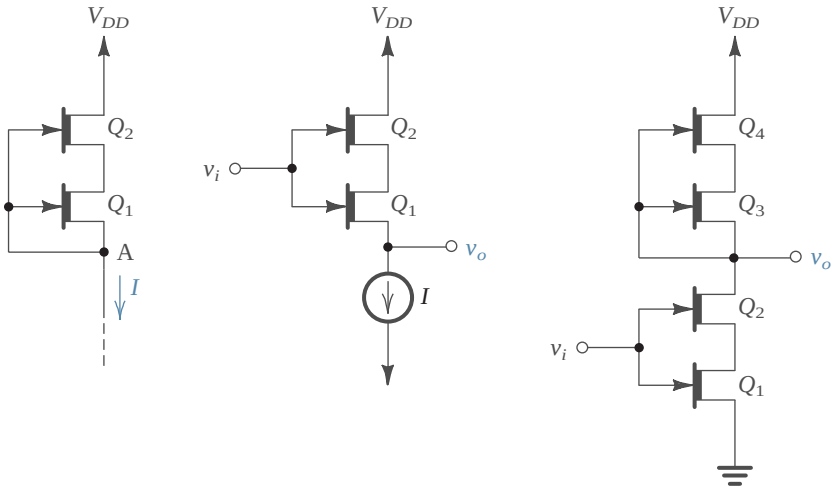
single MESFET. This circuit is unique to GaAs MESFETs and works only because of the early-saturation phenomenon observed in these devices. Recall from the discussion in Section 5.12 that **early saturation** refers to the fact that in a GaAs MESFET the drain current saturates at a voltage v_{DSsat} that is lower than $v_{GS} - V_t$.

In the composite MESFET of Fig. 6.42(a), Q_2 is made much wider than Q_1. It follows that since the two devices are conducting the same current, Q_2 will have a gate-to-source voltage v_{GS2} whose magnitude is much closer to $|V_t|$ than $|v_{GS1}|$ is (thus, $|v_{GS2}| \gg |v_{GS1}|$). For instance, if we use the devices whose typical parameters are given in Table 5.2 and ignore for the moment channel-length modulation ($\lambda = 0$), we find that for $W_1 = 10\ \mu$m and $W_2 = 90\ \mu$m, at a current of 1 mA, $v_{GS1} = 0$ and $v_{GS2} = -\frac{2}{3}$ V. Now, since the drain-to-source voltage of Q_1 is $v_{DS1} = -v_{GS2} + v_{GS1}$, we see that v_{DS1} will be positive and close to but lower than $v_{GS1} - V_t$ ($\frac{2}{3}$ V in our example compared to 1 V). Thus in the absence of early saturation, Q_1 would be operating in the triode region. With early saturation, however, it has been found that saturation-mode operation is achieved for Q_1 by making Q_2 5 to 10 times wider.

The composite MESFET of Fig. 6.42(a) can be thought of as a cascode configuration, in which Q_2 is the cascode transistor, but without a separate bias line to feed the gate of the cascode transistor (as in Fig. 6.40). By replacing each of Q_1 and Q_2 with their small-signal models one can show that the composite device can be represented with the equivalent circuit model of Fig. 6.42(b). Thus while g_m of the composite device is equal to that of Q_1, the output resistance is increased by the intrinsic gain of Q_2, $g_{m2}r_{o2}$, which is typically in the range 10 to 40. This is a substantial increase and is the reason for the attractiveness of the composite MESFET.

The composite MESFET can be employed in any of the applications that can benefit from its increased output resistance. Some examples are shown in Fig. 6.43. The circuit in Fig. 6.43(a) is that of a current source with increased output resistance. Another view of the operation of this circuit can be obtained by considering Q_2 as a source follower that causes the drain of Q_1 to follow the voltage changes at the current-source terminal (node A), thereby bootstrapping Q_1 and increasing the effective output resistance of the current source. This alternative interpretation of circuit operation has resulted in its alternative name: the **self-bootstrapped** current source.

The application of the composite MESFET as a source follower is depicted in Fig. 6.43(b). Assuming the bias-current source I to be ideal, we can write for the gain of



(a) (b) (c)

FIGURE 6.43 Applications of the composite MESFET: **(a)** as a current source; **(b)** as a source follower; and **(c)** as a gain stage.

this follower

$$\frac{v_o}{v_i} = \frac{r_{o,\text{eff}}}{r_{o,\text{eff}} + (1/g_{m1})}$$

$$= \frac{g_{m2} r_{o2} r_{o1}}{g_{m2} r_{o2} r_{o1} + (1/g_{m1})} \tag{6.135}$$

which is much closer to the ideal value of unity than is the gain of a single MESFET source follower.

EXERCISE

6.25 Using the device data given in Table 5.2, contrast the voltage gain of a source follower formed using a single MESFET having $W = 10$ μm with a composite MESFET follower with $W_1 = 10$ μm and $W_2 = 90$ μm. In both cases assume biasing at 1 mA and neglect λ while calculating g_m (for simplicity).

Ans. Single: 0.952 V/V; composite: 0.999 V/V

A final example of the application of the composite MESFET is shown in Fig. 6.43(c). The circuit is a gain stage utilizing a composite MESFET (Q_1, Q_2) as a driver and another composite MESFET (Q_3, Q_4) as a current-source load. The small-signal gain is given by

$$\frac{v_o}{v_i} = -g_{m1} R_o \tag{6.136}$$

where R_o is the output resistance,

$$R_o = r_{o,\text{eff}}(Q_1, Q_2) // r_{o,\text{eff}}(Q_3, Q_4)$$

$$= g_{m2} r_{o2} r_{o1} // g_{m4} r_{o4} r_{o3} \tag{6.137}$$

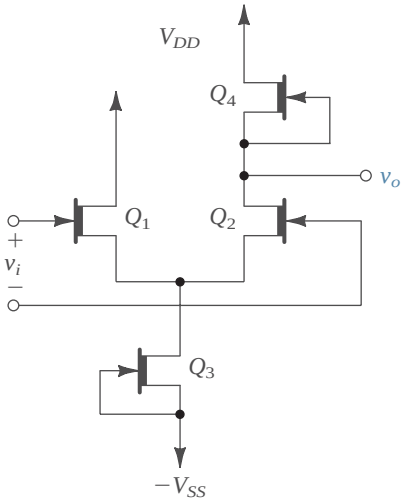


FIGURE 6.44 A simple MESFET differential amplifier.

Differential Amplifiers

The simplest possible implementation of a differential amplifier in GaAs MESFET technology is shown in Fig. 6.44. Here Q_1 and Q_2 form the differential pair, Q_3 forms the bias current source, and Q_4 forms the active (current-source) load. The performance of the circuit is impaired by the low output resistances of Q_3 and Q_4. The voltage gain is given by

$$\frac{v_o}{v_i} = -g_{m2}(r_{o2} /\!/ r_{o4}) \tag{6.138}$$

The gain can be increased by using one of the improved current-source implementations discussed above. Also, a rather ingenious technique has been developed for enhancing the gain of the MESFET differential pair. The circuit is shown in Fig. 6.45(a). While the drain

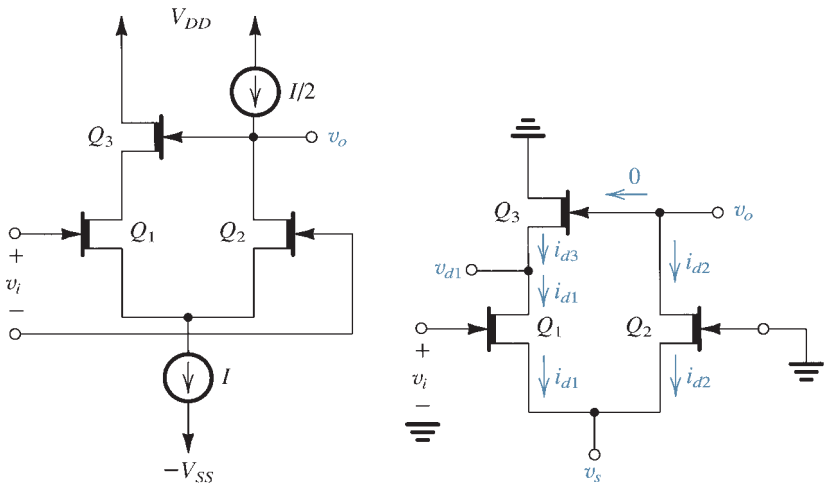


FIGURE 6.45 **(a)** A MESFET differential amplifier whose gain is enhanced by the application of positive feedback through the source follower Q_3; **(b)** small-signal analysis of the circuit in (a).

of Q_2 is loaded with a current-source load (as before), the output signal developed is fed back to the drain of Q_1 via the source follower Q_3. The small-signal analysis of the circuit is illustrated in Fig. 6.45(b) where the current sources I and $I/2$ have been assumed ideal and thus replaced with open circuits. To determine the voltage gain, we have grounded the gate terminal of Q_2 and applied the differential input signal v_i to the gate of Q_1. The analysis proceeds along the following steps:

1. From the output node we see that $i_{d2} = 0$.
2. From the sources node, since $i_{d2} = 0$, we find that $i_{d1} = 0$.
3. From the node at the drain of Q_1, since $i_{d1} = 0$, we find that $i_{d3} = 0$.
4. Writing for each transistor

$$i_d = g_m v_{gs} + v_{ds} / r_o = 0$$

we obtain three equations in the three unknowns v_{d1}, v_s, and v_o. The solution yields

$$\frac{v_o}{v_i} = g_{m1} r_{o1} \Big/ \left[\frac{g_{m1} r_{o1} + 1}{g_{m2} r_{o2} + 1} - \frac{g_{m3} r_{o3}}{g_{m3} r_{o3} + 1} \right] \tag{6.139}$$

If all three transistors have the same geometry and are operating at equal dc currents, their g_m and r_o values will be equal and the expression in Eq. (6.139) reduces to

$$\frac{v_o}{v_i} \simeq (g_m r_o)^2 \tag{6.140}$$

Thus application of positive feedback through follower Q_3 enables one to obtain a gain equal to the square of that naturally available from a single stage!

EXERCISE

6.26 Using the device data given in Table 5.2, find the gain of the differential amplifier circuit of Fig. 6.45(a) for $I = 10$ mA and $W_1 = W_2 = W_3 = 100$ μm.

Ans. 784 V/V

14.8 GALLIUM-ARSENIDE DIGITAL CIRCUITS

We conclude our study of digital-circuit families with a discussion of logic circuits implemented using the emerging technology of gallium arsenide. An introduction to this technology and its two basic devices, the MESFET and the Schottky-barrier diode (SBD), was given in Section 5.12. We urge the reader to review Section 5.12 before proceeding with the study of this section.

The major advantage that GaAs technology offers is a higher speed of operation than currently achievable using silicon devices. Gate delays of 10 to 100 ps have been reported for GaAs circuits. The disadvantages are a relatively high power dissipation per gate (1 to 10 mW); relatively small voltage swings and, correspondingly, narrow noise margins; low packing density, mostly as a result of the high-power dissipation per gate; and low manufacturing yield. The present state of affairs is that a few specialized manufacturers produce SSI, MSI, and some LSI digital circuits performing relatively specialized functions, with a cost per gate considerably higher than that of silicon digital ICs. Nevertheless, the very high

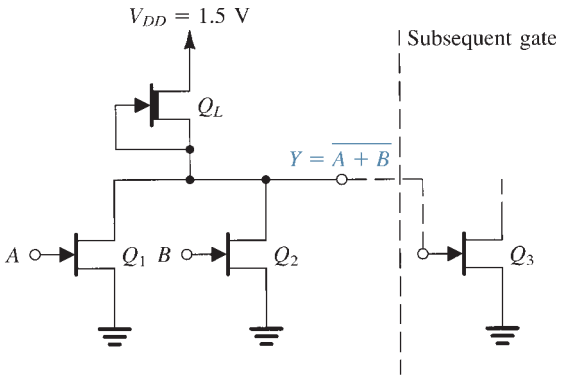


FIGURE 14.47 A DCFL GaAs gate implementing a two-input NOR function. The gate is shown driving the input transistor Q_3 of another gate.

speeds of operation achievable in GaAs circuits make it a worthwhile technology whose applications will possibly grow.

Unlike the CMOS logic circuits that we have studied in Chapter 13, and the bipolar logic families that we have studied in earlier sections of this chapter, there are no standard GaAs logic-circuit families. The lack of standards extends not only to the topology of the basic gates but also to the power-supply voltages used. In the following we present examples of the most popular GaAs logic gate circuits.

Direct-Coupled FET Logic (DCFL)

Direct-coupled FET logic (DCFL) is the simplest form of GaAs digital logic circuits. The basic gate is shown in Fig. 14.47. The gate utilizes enhancement MESFETs, Q_1 and Q_2, for the input switching transistors, and a depletion MESFET for the load transistor Q_L. The gate closely resembles the now obsolete depletion-load MOSFET circuit. The GaAs circuit of Fig. 14.47 implements a two-input NOR function.

To see how the MESFET circuit of Fig. 14.47 operates, ignore input B and consider the basic inverter formed by Q_1 and Q_L. When the input voltage applied to node A, v_I, is lower than the threshold voltage of the enhancement MESFET Q_1, denoted V_{tE}, transistor Q_1 will be off. Recall that V_{tE} is positive and for GaAs MESFETs is typically 0.1 to 0.3 V. Now if the gate output Y is open circuited, the output voltage will be very close to V_{DD}. In practice, however, the gate will be driving another gate, as indicated in Fig. 14.47, where Q_3 is the input transistor of the subsequent gate. In such a case, current will flow from V_{DD} through Q_L and into the gate terminal of Q_3. Recalling that the gate to source of a GaAs MESFET is a Schottky-barrier diode that exhibits a voltage drop of about 0.7 V when conducting, we see that the gate conduction of Q_3 will clamp the output high voltage (V_{OH}) to about 0.7 V. This is in sharp contrast to the MOSFET case, where no gate conduction takes place.

Figure 14.48 shows the DCFL inverter under study with the input of the subsequent gate represented by a Schottky diode Q_3. With $v_I < V_{tE}$, $i_1 = 0$ and i_L flows through Q_3 resulting in $v_O = V_{OH} \simeq 0.7$ V. Since V_{DD} is usually low (1.2 to 1.5 V) and the threshold voltage of Q_L, V_{tD}, is typically –0.7 to –1 V, Q_L will be operating in the triode region. (To simplify matters, we shall ignore in this discussion the early-saturation effect exhibited by GaAs MESFETs.)

As v_I is increased above V_{tE}, Q_1 turns on and conducts a current denoted i_1. Initially, Q_1 will be in the saturation region. Current i_1 subtracts from i_L, thus reducing the current in Q_3. The voltage across Q_3, v_O, decreases slightly. However, for the present discussion we shall assume that v_O will remain close to 0.7 V as long as Q_3 is conducting. This will continue until v_I reaches the value that results in $i_1 = i_L$. At this point, Q_3 ceases conduction

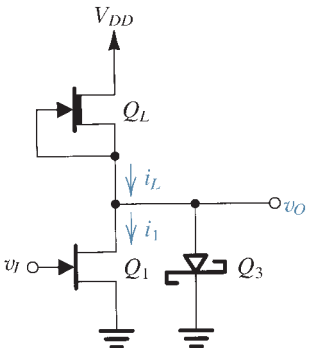


FIGURE 14.48 The DCFL gate with the input of the subsequent gate represented by a Schottky diode Q_3.

and can be ignored altogether. Further increase in v_I results in i_1 increasing, v_O decreasing, and $i_L = i_1$. When $(V_{DD} - v_O)$ exceeds $|V_{tD}|$, Q_L saturates; and when v_O falls below v_I by V_{tE}, Q_1 enters the triode region. Eventually, when $v_I = V_{OH} = 0.7$ V, $v_O = V_{OL}$, which is typically 0.1 to 0.2 V.

From the description above we see that the output voltage swing of the DCFL gate is limited by gate conduction to a value less than 0.7 V (typically 0.5 V or so). Further details on the operation of the DCFL gate are illustrated by the following example.

EXAMPLE 14.3

Consider a DCFL gate fabricated in a GaAs technology for which $L = 1$ μm, $V_{tD} = -1$ V, $V_{tE} = 0.2$ V, β (for 1-μm width) $= 10^{-4}$ A/V^2, and $\lambda = 0.1$ V^{-1}. Let the widths of the input MESFETs be 50 μm, and let the width of the load MESFET be 6 μm. $V_{DD} = 1.5$ V. Using a constant-voltage-drop model for the gate-source Schottky diode with $V_D = 0.7$ V, and neglecting the early-saturation effect of GaAs MESFETs (that is, using Eqs. 5.120 to describe MESFET operation), find V_{OH}, V_{OL}, V_{IH}, NM_H, NM_L, the static power dissipation, and the propagation delay for a total equivalent capacitance at the gate output of 30 fF.

Solution

From the description above of the operation of the DCFL gate we found that $V_{OH} = 0.7$ V. To obtain V_{OL}, we consider the inverter in the circuit of Fig. 14.48 and let $v_I = V_{OH} = 0.7$ V. Since we expect $v_O = V_{OL}$ to be small, we assume Q_1 to be in the triode region and Q_L to be in saturation. (Q_3 is of course off.) Equating i_1 and i_L gives the equation

$$\beta_1[2(0.7 - 0.2)V_{OL} - V_{OL}^2](1 + 0.1V_{OL}) = \beta_L[0 - (-1)]^2[1 + 0.1(1.5 - V_{OL})]$$

To simplify matters, we neglect the terms $0.1V_{OL}$ and substitute $\beta_L/\beta_1 = W_L/W_1 = 6/50$ to obtain a quadratic equation in V_{OL} whose solution gives $V_{OL} \simeq 0.17$ V.

Toward obtaining the value of V_{IL} we shall first find the value of v_I at which $i_1 = i_L$, the diode Q_3 turns off, and v_O begins to decrease. Since at this point $v_O = 0.7$ V, we assume that Q_1 is in saturation. Transistor Q_L has a v_{DS} of 0.8 V, which is less than $|V_{tD}|$ and is thus in the triode region. Equating i_1 and i_L gives

$$\beta_1(v_I - 0.2)^2(1 + 0.1 \times 0.7) = \beta_L[2(1)(1.5 - 0.7) - (1.5 - 0.7)^2][1 + 0.1(1.5 - 0.7)]$$

Substituting $\beta_L/\beta_1 = W_L/W_1 = 6/50$ and solving the resulting equation yields $v_I = 0.54$ V. Figure 14.49 shows a sketch of the transfer characteristic of the inverter. The slope dv_O/dv_I at

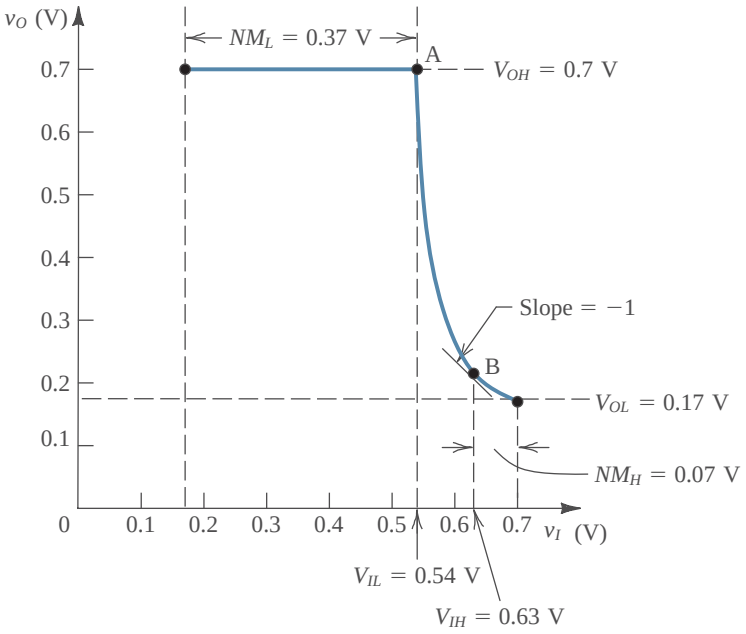


FIGURE 14.49 Transfer characteristic of the DCFL inverter of Fig. 14.48.

point A can be found to be −14.2 V/V. We shall consider point A as the point at which the inverter begins to switch from the high-output state; thus $V_{IL} \simeq 0.54$ V.

To obtain V_{IH}, we find the co-ordinates of point B at which $dv_O/dv_I = -1$. This can be done using a procedure similar to that employed for the MOSFET inverters and assuming Q_1 to be in the triode region and Q_L to be in saturation. Neglecting terms in $0.1v_O$, the result is $V_{IH} \simeq 0.63$ V. The noise margins can now be found as

$$NM_H \equiv V_{OH} - V_{IH} = 0.7 - 0.63 = 0.07 \text{ V}$$

$$NM_L \equiv V_{IL} - V_{OL} = 0.54 - 0.17 = 0.37 \text{ V}$$

The static power dissipation is determined by finding the supply current I_{DD} in the output-high and the output-low cases. When the output is high (at 0.7 V), Q_L is in the triode region and the supply current is

$$I_{DD} = \beta_L[2(0+1)(1.5-0.7) - (1.5-0.7)^2][1 + 0.1(1.5-0.7)]$$

Substituting $\beta_L = 10^{-4} \times W_L = 0.6$ mA/V^2 results in

$$I_{DD} = 0.61 \text{ mA}$$

When the output is low (at 0.17 V), Q_L is in saturation and the supply current is

$$I_{DD} = \beta_L(0+1)^2[1 + 0.1(1.5-0.17)] = 0.68 \text{ mA}$$

Thus the average supply current is

$$I_{DD} = \tfrac{1}{2}(0.61 + 0.68) = 0.645 \text{ mA}$$

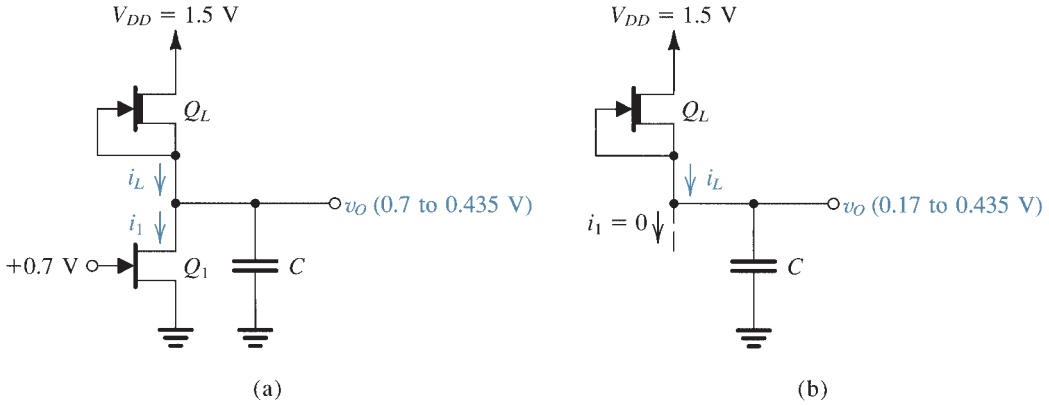


FIGURE 14.50 Circuits for calculating the propagation delays of the DCFL inverter: **(a)** t_{PHL}; **(b)** t_{PLH}.

and the static power dissipation is

$$P_D = 0.645 \times 1.5 \simeq 1 \text{ mW}$$

The propagation delay t_{PHL} is the time for the output voltage of the inverter to decrease from $V_{OH} = 0.7$ V to $\frac{1}{2}(V_{OH} + V_{OL}) = 0.435$ V. During this time v_I is at the high level of 0.7 V, and the capacitance C (assumed to be 30 fempto Farads [fF]) is discharged by $(i_1 - i_L)$; refer to Fig. 14.50(a). The average discharge current is found by calculating i_1 and i_L at the beginning and at the end of the discharge interval. The result is that i_1 changes from 1.34 mA to 1.28 mA and i_L changes from 0.61 mA to 0.66 mA. Thus the discharge current $(i_1 - i_L)$ changes from 0.73 mA to 0.62 mA for an average value of 0.675 mA. Thus

$$t_{PHL} = \frac{C\Delta V}{I} = \frac{30 \times 10^{-15}(0.7 - 0.435)}{0.675 \times 10^{-3}} = 11.8 \text{ ps}$$

To determine t_{PLH} we refer to the circuit in Fig. 14.50(b) and note that during t_{PLH}, v_O changes from $V_{OL} = 0.17$ V to $\frac{1}{2}(V_{OH} + V_{OL}) = 0.435$ V. The charging current is the average value of i_L, which changes from 0.8 mA to 0.66 mA. Thus $i_{L|\text{average}} = 0.73$ mA and

$$t_{PLH} = \frac{30 \times 10^{-15} \times (0.435 - 0.17)}{0.73 \times 10^{-3}} = 10.9 \text{ ps}$$

The propagation delay of the DCFL gate can now be found as

$$t_P = \frac{1}{2}(t_{PHL} + t_{PLH}) = 11.4 \text{ ps}$$

As a final remark, we note that the analysis above was done using simplified device models; our objective is to show how the circuit works rather than to find accurate performance measures. These can be obtained using SPICE simulation with more elaborate models [see Roberts and Sedra (1997)].

Logic Gates Using Depletion MESFETs

The DCFL circuits studied above require both enhancement and depletion devices and thus are somewhat difficult to fabricate. Also, owing to the fact that the voltage swings and noise margins are rather small, very careful control of the value of V_{tE} is required in fabrication. As an alternative, we now present circuits that utilize depletion devices only.

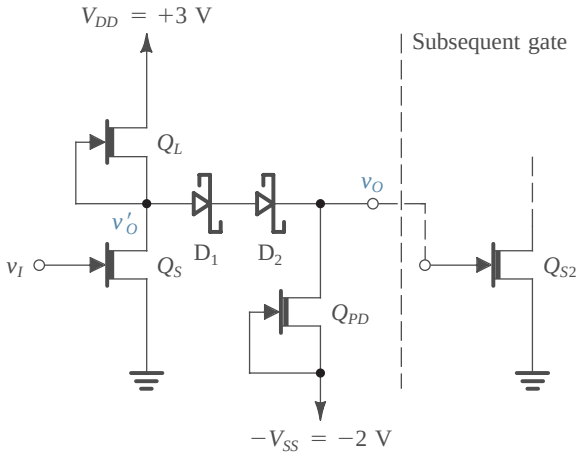


FIGURE 14.51 An inverter circuit utilizing depletion-mode devices only. Schottky diodes are employed to shift the output logic levels to values compatible with the input levels required to turn the depletion MESFET Q_S on and off. This circuit is known as FET logic (FL).

Figure 14.51 shows the basic inverter circuit of a family of GaAs logic circuits known at FET logic (FL). The heart of the FL inverter is formed by the switching transistor Q_S and its load Q_L—both depletion-type MESFETs. Since the threshold voltage of a depletion MESFET, V_{tD}, is negative, a negative voltage $<V_{tD}$ is needed to turn Q_S off. On the other hand the output low voltage at the drain of Q_S will always be positive. It follows that the logic levels at the drain of Q_S are not compatible with the levels required at the gate input. The incompatibility problem is solved by simply shifting the level of the voltage v'_O down by two diode drops, that is, by approximately 1.4 V. This level shifting is accomplished by the two Schottky diodes D_1 and D_2. The depletion transistor Q_{PD} provides a constant-current bias for D_1 and D_2. To ensure that Q_{PD} operates in the saturation region at all times, its source is connected to a negative supply $-V_{SS}$, and the value of V_{SS} is selected to be equal to or greater than the lowest level of $v_O(V_{OL})$ plus the magnitude of the threshold voltage, $|V_{tD}|$. Transistor Q_{PD} also supplies the current required to discharge a load capacitance when the output voltage of the gate goes low, hence the name "pull-down" transistor and the subscript *PD*.

To see how the inverter of Fig. 14.51 operates, refer to its transfer characteristic, shown in Fig. 14.52. The circuit is usually designed using MESFETs having equal channel lengths (typically 1 μm) and having widths $W_S = W_L = 2W_{PD}$. The transfer characteristic shown is for the case $V_{tD} = -0.9$ V. For v_I lower than V_{tD}, Q_S will be off and Q_L will operate in saturation, supplying a constant current I_L to D_1 and D_2. Transistor Q_{PD} will also operate in saturation with a constant current $I_{PD} = \frac{1}{2}I_L$. The difference between the two currents will flow through the gate terminal of the input transistor of the next gate in the chain, Q_{S2}. Thus the input Schottky diode of Q_{S2} clamps the output voltage v_O to approximately 0.7 V, which is the output high level, V_{OH}. (Note that for this discussion we shall neglect the finite output resistance in saturation.)

As v_I is raised above V_{tD}, Q_S turns on. Since its drain is at +2.1 V, Q_S will operate in the saturation region and will take away some of the current supplied by Q_L. Thus the current flowing into the gate of Q_{S2} decreases by an equal amount. If we keep increasing v_I, a value is reached for which the current in Q_S equals $\frac{1}{2}I_L$, thus leaving no current to flow through the gate of Q_{S2}. This corresponds to the point labeled A on the transfer characteristic. A further slight increase in v_I will cause the voltage v'_O to fall to the point B where Q_S enters the triode region. The segment AB of the transfer curve represents the high-gain region of operation, having a slope equal to $-g_{ms}R$ where R denotes the total equivalent resistance at the drain node. Note that this segment is shown as vertical in Fig. 14.52 because we are neglecting the output resistance in saturation.

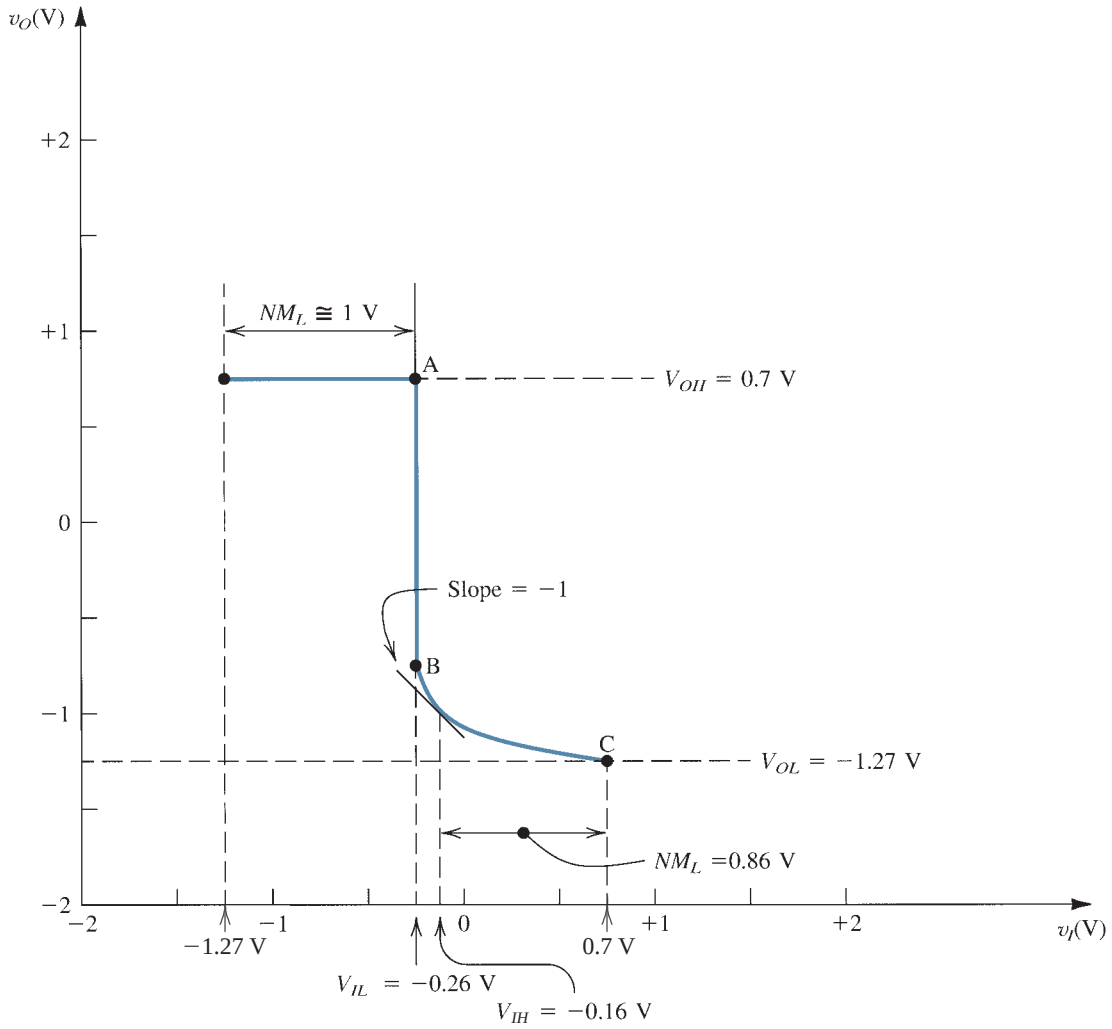


FIGURE 14.52 Transfer characteristic of the FL inverter of Fig. 14.51.

The segment BC of the transfer curve corresponds to Q_S operating in the triode region. Here Q_L and Q_{PD} continue to operate in saturation and D_1 and D_2 remain conducting. Finally, for $v_I = V_{OH} = 0.7$ V, $v_O = V_{OL}$, which for the case $V_{tD} = -0.9$ V can be found to be −1.3 V.

EXERCISE

14.30 Verify that the co-ordinates of points A, B, and C of the transfer characteristic are as indicated in Fig. 14.52. Let $V_{tD} = -0.9$ V and $\lambda = 0$.

As indicated in Fig. 14.52, the FL inverter exhibits much higher noise margins than those for the DCFL circuit. The FL inverter, however, requires two power supplies.

The FL inverter can be used to construct a NOR gate by simply adding transistors with drain and source connected in parallel with those of Q_S.

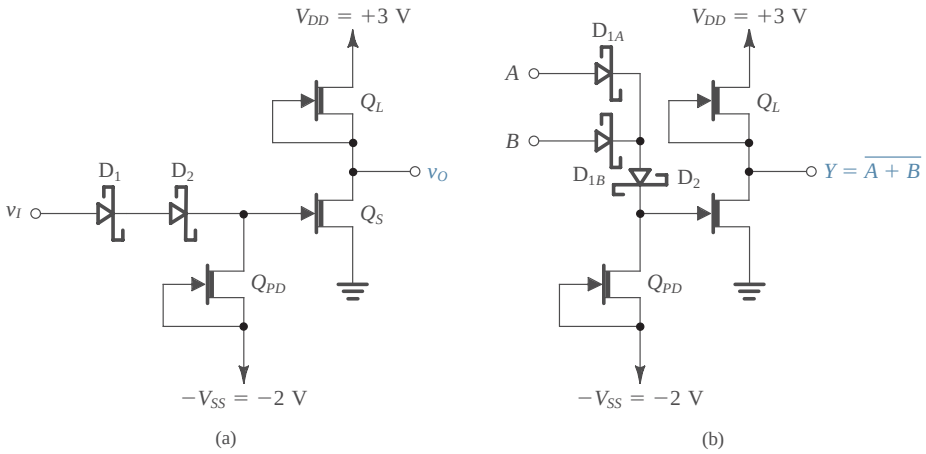


FIGURE 14.53 **(a)** An SDFL inverter. **(b)** An SDFL NOR gate.

Schottky Diode FET Logic (SDFL)

If the diode level-shifting network of the FL inverter is connected at the input side of the gate, rather than at the output side, we obtain the circuit shown in Fig. 14.53(a). This inverter operates in much the same manner as the FL inverter. The modified circuit, however, has a very interesting feature: The NOR function can be implemented by simply connecting additional diodes, as shown in Fig. 14.53(b). This logic form is known as Schottky diode FET logic (SDFL). SDFL permits higher packing density than other forms of MESFET logic because only an additional diode, rather than an additional transistor, is required for each additional input, and diodes require much smaller areas than transistors.

Buffered FET Logic (BFL)

Another variation on the basic FL inverter of Fig. 14.51 is possible. A source follower can be inserted between the drain of Q_S and the diode level-shifting network. The resulting gate, shown for the case of a two-input NOR, is depicted in Fig. 14.54. This form of GaAs logic circuit is known as buffered FET logic (BFL). The source-follower transistor Q_{SF} increases the output current-driving capability, thus decreasing the low-to-high propagation time. FL, BFL, and SDFL feature propagation delays of the order of 100 ps and power dissipation of the order of 10 mW/gate.

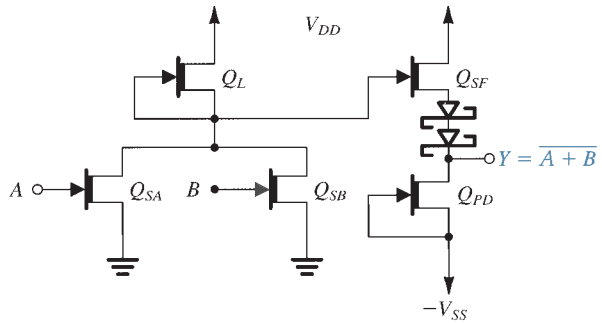


FIGURE 14.54 A BFL two-input NOR gate. The gate is formed by inserting a source-follower transistor Q_{SF} between the inverting stage and the level-shifting stage.

14.3 TRANSISTOR–TRANSISTOR LOGIC (TTL OR T^2L)

For more than two decades (late 1960s to late 1980s) TTL enjoyed immense popularity. Indeed, the bulk of digital systems applications employing SSI and MSI packages were designed using TTL.

We shall begin this section with a study of the evolution of TTL from DTL. In this way we shall explain the function of each of the stages of the complete TTL gate circuit. Characteristics of standard TTL gates will be studied in Section 14.4. Standard TTL, however, has now been virtually replaced with more advanced forms of TTL that feature improved performance. These will be discussed in Section 14.5.

Evolution of TTL from DTL

The basic DTL gate circuit in discrete form was discussed in the previous section (see Fig. 14.6). The integrated-circuit form of the DTL gate is shown in Fig. 14.7 with only one input indicated. As a prelude to introducing TTL, we have drawn the input diode as a diode-connected transistor (Q_1), which corresponds to how diodes are made in IC form.

This circuit differs from the discrete DTL circuit of Fig. 14.6 in two important aspects. First, one of the steering diodes is replaced by the base–emitter junction of a transistor (Q_2) that is either cut off (when the input is low) or in the active mode (when the input is high). This is done to reduce the input current and thereby increase the fan-out capability of the gate. A detailed explanation of this point, however, is not relevant to our study of TTL. Second, the resistance R_B is returned to ground rather than to a negative supply, as was done in the earlier discrete circuit. An obvious advantage of this is the elimination of the additional power supply. The disadvantage, however, is that the reverse base current available to remove the excess charge stored in the base of Q_3 is rather small. We shall elaborate on this point below.

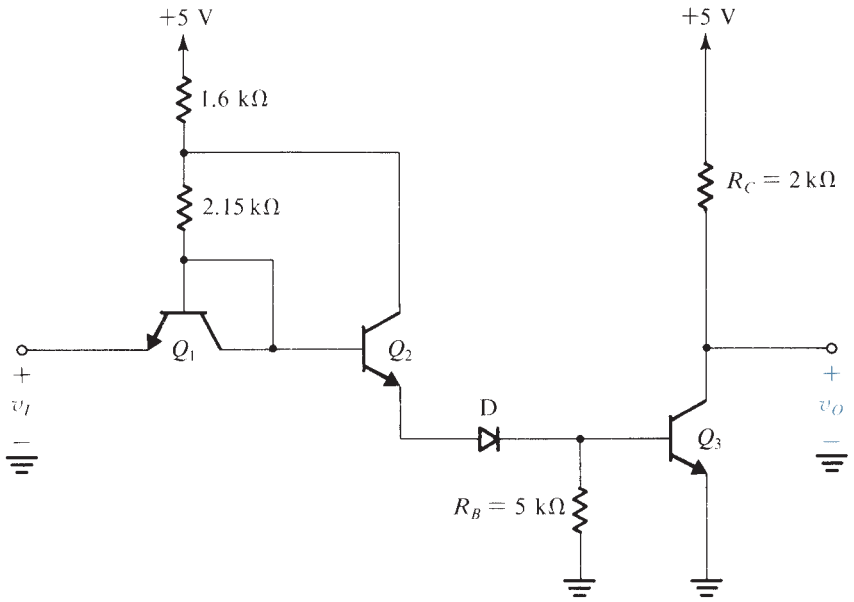


FIGURE 14.7 IC form of the DTL gate with the input diode shown as a diode-connected transistor (Q_1). Only one input terminal is shown.

EXERCISE

14.4 Consider the DTL gate circuit shown in Fig. 14.7 and assume that $\beta(Q_2) = \beta(Q_3) = 50$. (a) When $v_I = 0.2$ V, find the input current. (b) When $v_I = +5$ V, find the base current of Q_3.

Ans. (a) 1.1 mA; (b) 1.6 mA

Reasons for the Slow Response of DTL

The DTL gate has relatively good noise margins and reasonably good fan-out capability. Its response, however, is rather slow. There are two reasons for this: first, when the input goes low and Q_2 and D turn off, the charge stored in the base of Q_3 has to leak through R_B to ground. The initial value of the reverse base current that accomplishes this "base discharging" process is approximately 0.7 V/R_B, which is about 0.14 mA. Because this current is quite small in comparison to the forward base current, the time required for the removal of base charge is rather long, which contributes to lengthening the gate delay.

The second reason for the relatively slow response of DTL derives from the nature of the output circuit of the gate, which is simply a common-emitter transistor. Figure 14.8 shows the output transistor of a DTL gate driving a capacitive load C_L. The capacitance C_L represents the input capacitance of another gate and/or the wiring and parasitic capacitances that are inevitably present in any circuit. When Q_3 is turned on, its collector voltage cannot instantaneously fall because of the existence of C_L. Thus Q_3 will not immediately saturate but rather will operate in the active region. The collector of Q_3 will therefore act as a constant-current source and will sink a relatively large current (βI_B). This large current will rapidly discharge C_L. We thus see that the common-emitter output stage features a short turn-on time. However, turnoff is another matter.

Consider next the operation of the common-emitter output stage when Q_3 is turned off. The output voltage will not rise immediately to the high level (V_{CC}). Rather, C_L will charge up to V_{CC} through R_C. This is a rather slow process, and it results in lengthening the DTL gate delay (and similarly the RTL gate delay).

Having identified the two reasons for the slow response of DTL, we shall see in the following how these problems are remedied in TTL.

Input Circuit of the TTL Gate

Figure 14.9 shows a conceptual TTL gate with only one input terminal indicated. The most important feature to note is that the input diode has been replaced by a transistor. One can

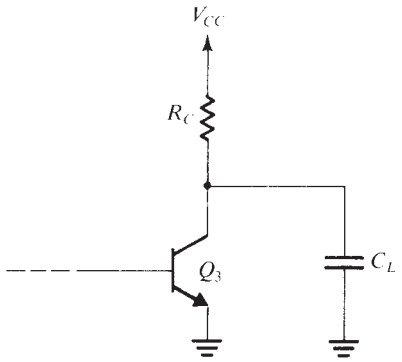


FIGURE 14.8 The output circuit of a DTL gate driving a capacitive load C_L.

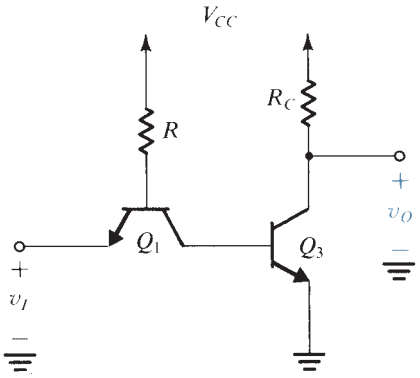


FIGURE 14.9 Conceptual form of TTL gate. Only one input terminal is shown.

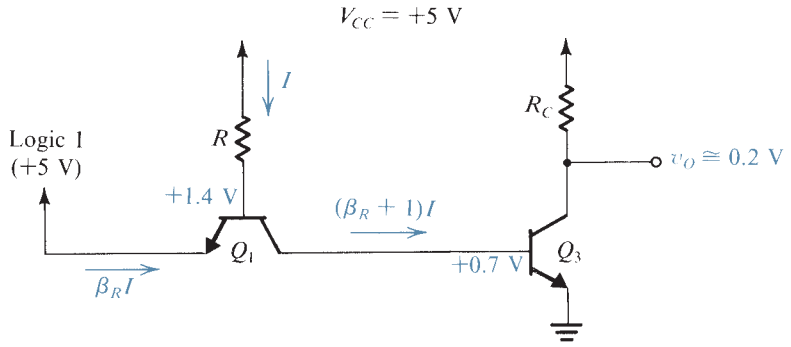


FIGURE 14.10 Analysis of the conceptual TTL gate when the input is high.

think of this simply as if the short circuit between base and collector of Q_1 in Fig. 14.7 has been removed.

To see how the conceptual TTL circuit of Fig. 14.9 works, let the input v_I be high (say, $v_I = V_{CC}$). In this case current will flow from V_{CC} through R, thus forward-biasing the base–collector junction of Q_1. Meanwhile, the base–emitter junction of Q_1 will be reverse-biased. Therefore Q_1 will be operating in the **inverse active mode**—that is, in the active mode but with the roles of emitter and collector interchanged. The voltages and currents will be as indicated in Fig. 14.10, where the current I can be calculated from

$$I = \frac{V_{CC} - 1.4}{R}$$

In actual TTL circuits Q_1 is designed to have a very low reverse β ($\beta_R \simeq 0.02$). Thus the gate input current will be very small, and the base current of Q_3 will be approximately equal to I. This current will be sufficient to drive Q_3 into saturation, and the output voltage will be low (0.1 to 0.2 V).

Next let the gate input voltage be brought down to the logic-0 level (say, $v_I \simeq 0.2$ V). The current I will then be diverted to the emitter of Q_1. The base–emitter junction of Q_1 will become forward-biased, and the base voltage of Q_1 will therefore drop to 0.9 V. Since Q_3 *was* in saturation, its base voltage will remain at +0.7 V pending the removal of the excess charge stored in the base region. Figure 14.11 indicates the various voltage and current values immediately after the input is lowered. We see that Q_1 will be operating in the normal

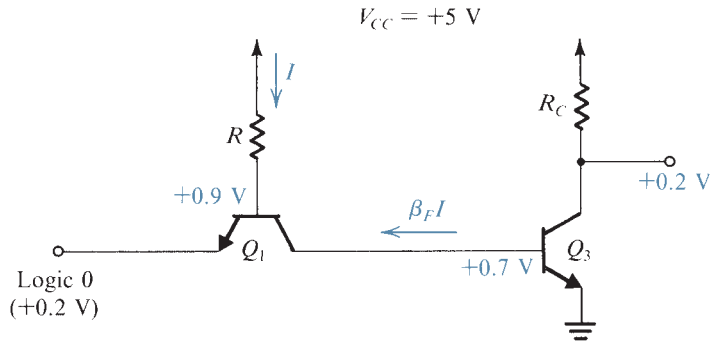


FIGURE 14.11 Voltage and current values in the conceptual TTL circuit immediately after the input voltage is lowered.

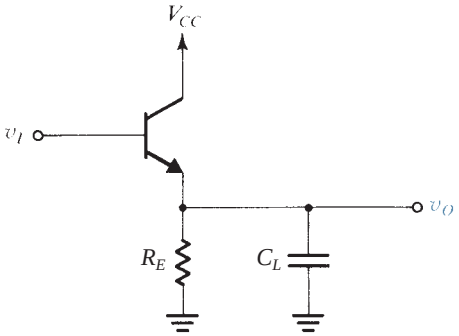


FIGURE 14.12 An emitter-follower output stage with capacitive load.

active mode[3] and its collector will carry a large current ($\beta_F I$). This large current rapidly discharges the base of Q_3 and drives it into cutoff. We thus see the action of Q_1 in speeding up the turn-off process.

As Q_3 turns off, the voltage at its base is reduced, and Q_1 enters the saturation mode. Eventually the collector current of Q_1 will become negligibly small, which implies that its V_{CEsat} will be approximately 0.1 V and the base of Q_3 will be at about 0.3 V, which keeps Q_3 in cutoff.

Output Circuit of the TTL Gate

The above discussion illustrates how one of the two problems that slow down the operation of DTL is solved in TTL. The second problem, the long rise time of the output waveform, is solved by modifying the output stage, as we shall now explain.

First, recall that the common-emitter output stage provides fast discharging of load capacitance but rather slow charging. The opposite is obtained in the emitter-follower output stage shown in Fig. 14.12. Here, as v_I goes high, the transistor turns on and provides a low output resistance (characteristic of emitter followers), which results in fast charging of C_L. On the other hand, when v_I goes low, the transistor turns off and C_L is then left to discharge slowly through R_E.

[3] Although the collector voltage of Q_1 is lower than its base voltage by 0.2 V, the collector–base junction will in effect be cut off and Q_1 will be operating in the active mode.

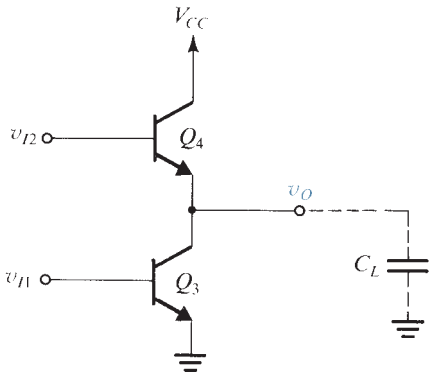


FIGURE 14.13 The totem-pole output stage.

It follows that an optimum output stage would be a combination of the common-emitter and the emitter-follower configurations. Such an output stage, shown in Fig. 14.13, has to be driven by two *complementary* signals v_{I1} and v_{I2}. When v_{I1} is high v_{I2} will be low, and in this case Q_3 will be on and saturated, and Q_4 will be off. The common-emitter transistor Q_3 will then provide the fast discharging of load capacitance and in steady state provide a low resistance (R_{CEsat}) to ground. Thus when the output is low, the gate can *sink* substantial amounts of current through the saturated transistor Q_3.

When v_{I1} is low and v_{I2} is high, Q_3 will be off and Q_4 will be conducting. The emitter follower Q_4 will then provide fast charging of load capacitance. It also provides the gate with a low output resistance in the high state and hence with the ability to *source* a substantial amount of load current.

Because of the appearance of the circuit in Fig. 14.13, with Q_4 stacked on top of Q_3, the circuit has been given the name **totem-pole output stage.** Also, because of the action of Q_4 in *pulling up* the output voltage to the high level, Q_4 is referred to as the **pull-up transistor.** Since the pulling up is achieved here by an active element (Q_4), the circuit is said to have an **active pull-up.** This is in contrast to the **passive pull-up** of RTL and DTL gates. Of course, the common-emitter transistor Q_3 provides the circuit with **active pull-down.** Finally, note that a special **driver circuit** is needed to generate the two complementary signals v_{I1} and v_{I2}.

EXAMPLE 14.1

We wish to analyze the circuit shown together with its driving waveforms in Fig. 14.14 to determine the waveform of the output signal v_O. Assume that Q_3 and Q_4 have $\beta = 50$.

Solution

Consider first the situation before v_{I1} goes high—that is, at time $t < 0$. In this case Q_3 is off and Q_4 is on, and the circuit can be simplified to that shown in Fig. 14.15. In this simplified circuit we have replaced the voltage divider (R_1, R_2) by its Thévenin equivalent. In the steady state, C_L will be charged to the output voltage v_O, whose value can be obtained as follows:

$$5 = 10 \times I_B + V_{BE} + I_E \times 0.5 + 2.5$$

Substituting $V_{BE} \simeq 0.7$ V and $I_B = I_E/(\beta + 1) = I_E/51$ gives $I_E = 2.59$ mA. Thus the output voltage v_O is given by

$$v_O = 2.5 + I_E \times 0.5 = 3.79 \text{ V}$$

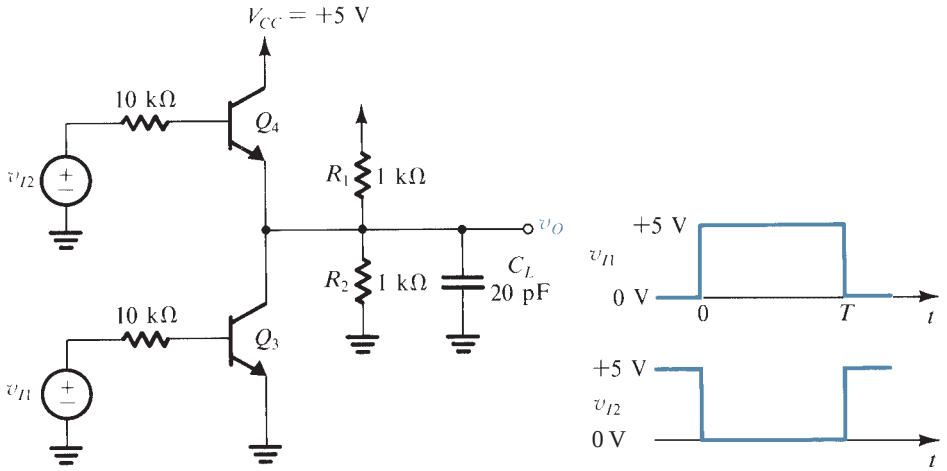


FIGURE 14.14 Circuit and input waveforms for Example 14.1.

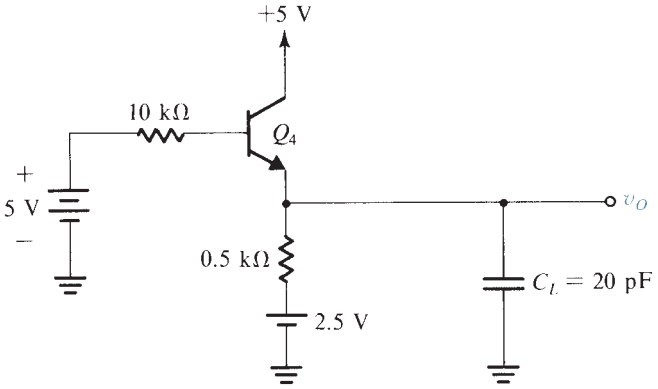


FIGURE 14.15 The circuit of Fig. 14.14 when Q_3 is off.

We next consider the circuit as v_{I1} goes high and v_{I2} goes low. Transistor Q_3 turns on and transistor Q_4 turns off, and the circuit simplifies to that shown in Fig. 14.16. Again we have used the Thévenin equivalent of the divider (R_1, R_2). We shall also assume that the switching times of the transistors are negligibly small. Thus at $t = 0+$ the base current of Q_3 becomes

$$I_B = \frac{5 - 0.7}{10} = 0.43 \text{ mA}$$

Since at $t = 0$ the collector voltage of Q_3 is 3.79 V, and since this value cannot change instantaneously because of C_L, we see that at $t = 0+$ transistor Q_3 will be in the active mode. The collector current of Q_3 will be βI_B, which is 21.5 mA, and the circuit will have the equivalent shown in Fig. 14.17(a). A simpler version of this equivalent circuit, obtained using Thévenin's theorem, is shown in Fig. 14.17(b).

The equivalent circuit of Fig. 14.17 applies as long as Q_3 remains in the active mode. This condition persists while C_L is being discharged and until v_O reaches about +0.3 V, at which time Q_3 enters saturation. This is illustrated by the waveform in Fig. 14.18. The time for the output

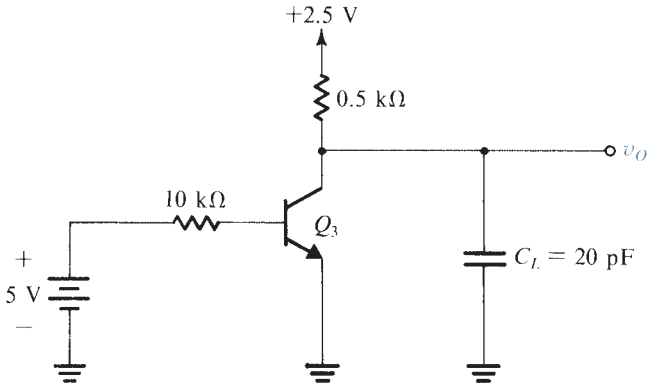


FIGURE 14.16 The circuit of Fig. 14.14 when Q_4 is off.

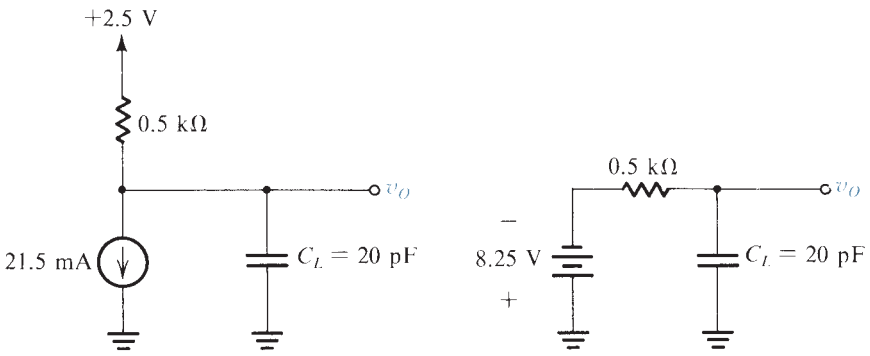


FIGURE 14.17 **(a)** Equivalent circuit for the circuit in Fig. 14.16 when Q_3 is in the active mode. **(b)** Simpler version of the circuit in (a) obtained using Thévenin's theorem.

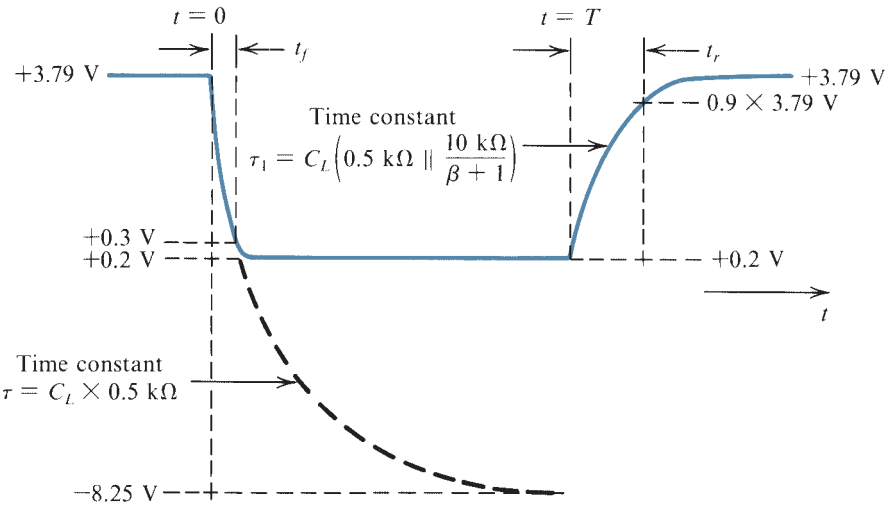


FIGURE 14.18 Details of the output voltage waveform for the circuit in Fig. 14.14.

voltage to fall from +3.79 V to +0.3 V, which can be considered the **fall time** t_f, can be obtained from

$$-8.25-(-8.25-3.79)e^{-t_f/\tau}=0.3$$

which results in

$$t_f \simeq 0.34\tau$$

where

$$\tau = C_L \times 0.5\ \text{k}\Omega = 10\ \text{ns}$$

Thus $t_f = 3.4$ ns.

After Q_3 enters saturation, the capacitor discharges further to the final steady-state value of V_{CEsat} (≃0.2 V). The transistor model that applies during this interval is more complex; since the interval in question is quite short, we shall not pursue the matter further.

Consider next the situation as v_{I1} goes low and v_{I2} goes high at $t = T$. Transistor Q_3 turns off as Q_4 turns on. We shall assume that this occurs immediately, and thus at $t = T+$ the circuit simplifies to that in Fig. 14.15. We have already analyzed this circuit in the steady state and thus know that eventually v_O will reach +3.79 V. Thus v_O rises exponentially from +0.2 V toward +3.79 V with a time constant of $C_L\{0.5\ \text{k}\Omega//[10\ \text{k}\Omega/(\beta+1)]\}$, where we have neglected the emitter resistance r_e. Denoting this time constant τ_1, we obtain $\tau_1 = 2.8$ ns. Defining the rise time t_r as the time for v_O to reach 90% of the final value, we obtain $3.79-(3.79-0.2)e^{-t_r/\tau_1} = 0.9\times 3.79$, which results in $t_r = 6.4$ ns. Figure 14.18 illustrates the details of the output voltage waveform.

The Complete Circuit of the TTL Gate

Figure 14.19 shows the complete TTL gate circuit. It consists of three stages: the input transistor Q_1, whose operation has already been explained, the driver stage Q_2, whose function is to generate the two complementary voltage signals required to drive the totem-pole circuit,

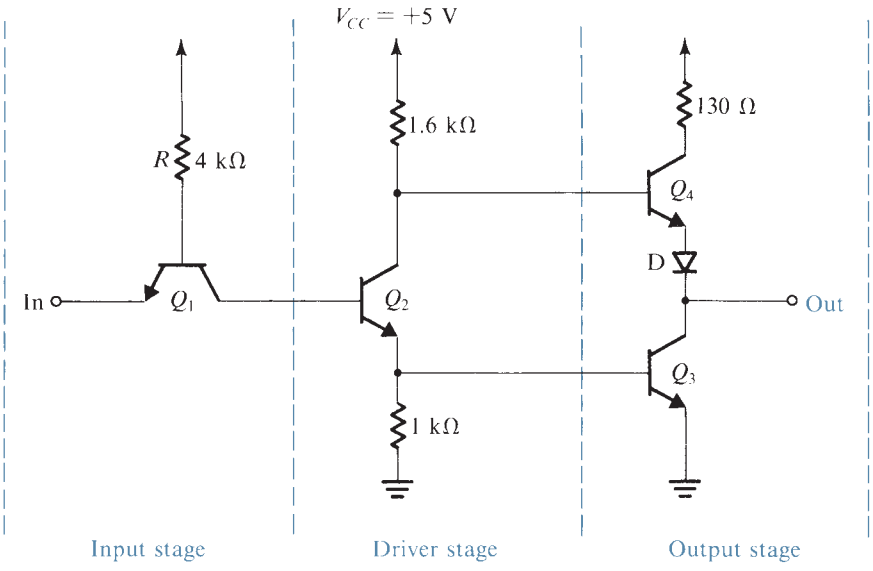


FIGURE 14.19 The complete TTL gate circuit with only one input terminal indicated.

which is the third (output) stage of the gate. The totem-pole circuit in the TTL gate has two additional components: the 130-Ω resistance in the collector circuit of Q_4 and the diode D in the emitter circuit of Q_4. The function of these two additional components will be explained shortly. Notice that the TTL gate is shown with only one input terminal indicated. Inclusion of additional input terminals will be considered in Section 14.4.

Because the driver stage Q_2 provides two complementary (that is, out-of-phase) signals, it is known as a **phase splitter.**

We shall now provide a detailed analysis of the TTL gate circuit in its two extreme states: one with the input high and one with the input low.

Analysis When the Input Is High

When the input is high (say, +5 V), the various voltages and currents of the TTL circuit will have the values indicated in Fig. 14.20. The analysis illustrated in Fig. 14.20 is quite straightforward, and the order of the steps followed is indicated by the circled numbers. As expected, the input transistor is operating in the inverse active mode, and the input current, called the **input high current** I_{IH}, is small; that is,

$$I_{IH} = \beta_R I \simeq 15\ \mu\text{A}$$

where we assume that $\beta_R \simeq 0.02$.

The collector current of Q_1 flows into the base of Q_2, and its value is sufficient to saturate the phase-splitter transistor Q_2. The latter supplies the base of Q_3 with sufficient current to drive it into saturation and lower its output voltage to $V_{CE\text{sat}}$ (0.1 to 0.2 V). The voltage at the collector of Q_2 is $V_{BE3} + V_{CE\text{sat}}(Q_2)$, which is approximately +0.9 V. If diode D were not included, this voltage would be sufficient to turn Q_4 on, which is contrary to the proper operation of the totem-pole circuit. Including diode D ensures that both Q_4 and D remain off.

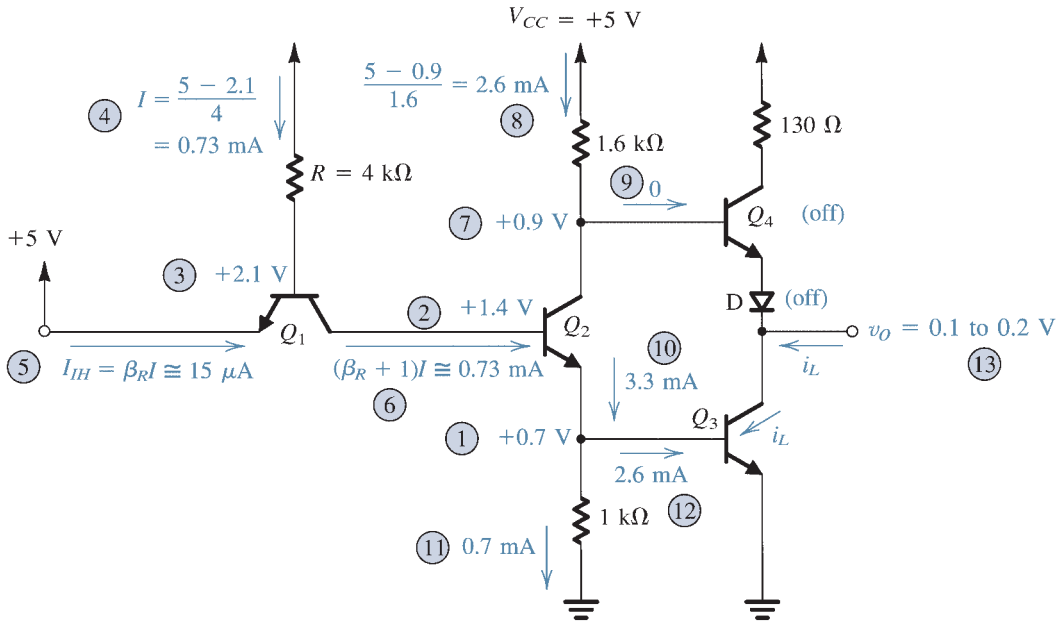


FIGURE 14.20 Analysis of the TTL gate with the input high. The circled numbers indicate the order of the analysis steps.

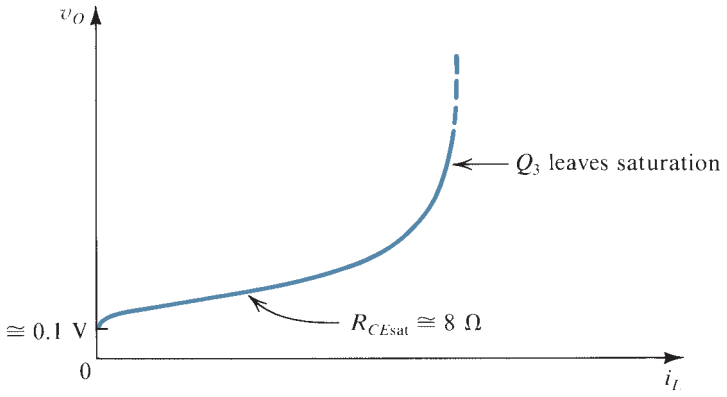


FIGURE 14.21 The v_O–i_L characteristic of the TTL gate when the output is low.

The saturated transistor Q_3 then establishes the low output voltage of the gate (V_{CEsat}) and provides a low impedance to ground.

In the low-output state the gate can sink a load current i_L, provided that the value of i_L does not exceed $\beta \times 2.6$ mA, which is the maximum collector current that Q_3 can sustain while remaining in saturation. Obviously the greater the value of i_L, the greater the output voltage will be. To maintain the logic-0 level below a certain specified limit, a corresponding limit has to be placed on the load current i_L. As will be seen shortly, it is this limit that determines the maximum fan-out of the TTL gate.

Figure 14.21 shows a sketch of the output voltage v_O versus the load current i_L of the TTL gate when the output is low. This is simply the v_{CE}–i_C characteristic curve of Q_3 measured with a base current of 2.6 mA. Note that at $i_L = 0$, v_O is the offset voltage, which is about 100 mV.

EXERCISE

14.5 Assume that the saturation portion of the v_O–i_L characteristic shown in Fig. 14.21 can be approximated by a straight line (of slope = 8 Ω) that intersects the v_O axis at 0.1 V. Find the maximum load current that the gate is allowed to sink if the logic-0 level is specified to be ≤0.3 V.

Ans. 25 mA

Analysis When the Input Is Low

Consider next the operation of the TTL gate when the input is at the logic-0 level (≃0.2 V). The analysis is illustrated in Fig. 14.22, from which we see that the base–emitter junction of Q_1 will be forward-biased and the base voltage will be approximately +0.9 V. Thus the current I can be found to be approximately 1 mA. Since 0.9 V is insufficient to forward-bias the series combination of the collector–base junction of Q_1 and the base–emitter junction of Q_2 (at least 1.2 V would be required), the latter will be off. Therefore the collector current of Q_1 will be almost zero and Q_1 will be saturated, with $V_{CEsat} \simeq 0.1$ V. Thus the base of Q_2 will be at approximately +0.3 V, which is indeed insufficient to turn Q_2 on.

The gate input current in the low state, called **input-low current** I_{IL}, is approximately equal to the current I (≃ 1 mA) and flows out of the emitter of Q_1. If the TTL gate is driven

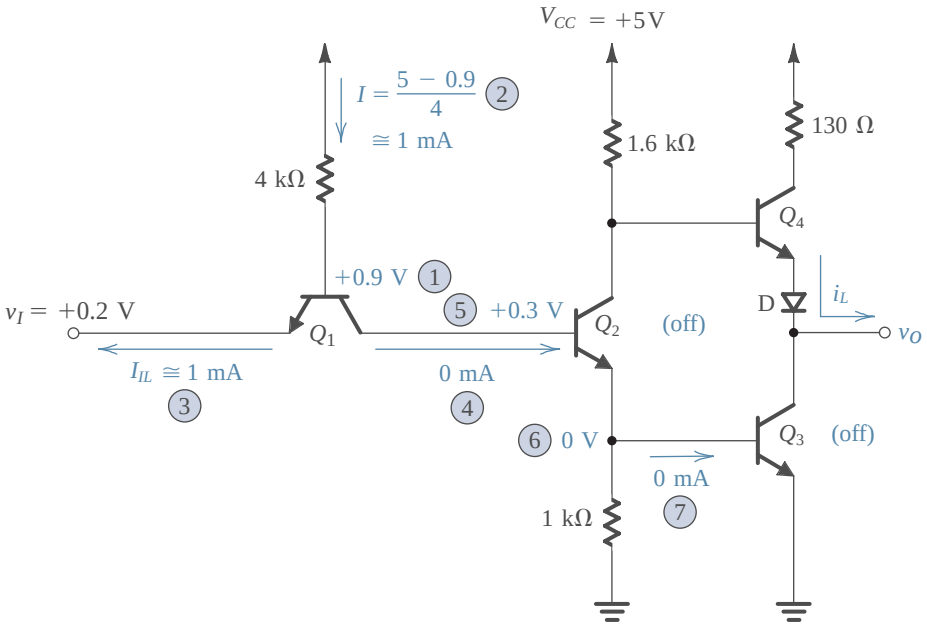


FIGURE 14.22 Analysis of the TTL gate when the input is low. The circled numbers indicate the order of the analysis steps.

by another TTL gate, the output transistor Q_3 of the driving gate should sink this current I_{IL}. Since the output current that a TTL gate can sink is limited to a certain maximum value, the maximum fan-out of the gate is directly determined by the value of I_{IL}.

EXERCISES

14.6 Consider the TTL gate analyzed in Exercise 14.5. Find its maximum allowable fan-out using the value of I_{IL} calculated above.

Ans. 25

14.7 Use Eq. (4.114) to find V_{CEsat} of transistor Q_1 when the input of the gate is low (0.2 V). Assume that $\beta_F = 50$ and $\beta_R = 0.02$.

Ans. 98 mV

Let us continue with our analysis of the TTL gate. When the input is low, we see that both Q_2 and Q_3 will be off. Transistor Q_4 will be on and will supply (source) the load current i_L. Depending on the value of i_L, Q_4 will be either in the active mode or in the saturation mode.

With the gate output terminal open, the current i_L will be very small (mostly leakage) and the two junctions (base–emitter junction of Q_4 and diode D) will be barely conducting. Assuming that each junction has a 0.65-V drop and neglecting the voltage drop across the 1.6-kΩ resistance, we find that the output voltage will be

$$v_O \simeq 5 - 0.65 - 0.65 = 3.7 \text{ V}$$

As i_L is increased, Q_4 and D conduct more heavily, but for a range of i_L, Q_4 remains in the active mode, and v_O is given by

$$v_O = V_{CC} - \frac{i_L}{\beta + 1} \times 1.6\ \text{k}\Omega - V_{BE4} - V_D \tag{14.4}$$

If we keep increasing i_L, a value will be reached at which Q_4 saturates. Then the output voltage becomes determined by the 130-Ω resistance according to the approximate relationship

$$v_O \simeq V_{CC} - i_L \times 130 - V_{CEsat}(Q_4) - V_D \tag{14.5}$$

Function of the 130-Ω Resistance

At this point the reason for including the 130-Ω resistance should be evident: It is simply to limit the current that flows through Q_4, especially in the event that the output terminal is accidentally short-circuited to ground. This resistance also limits the supply current in another circumstance, namely, when Q_4 turns on while Q_3 is still in saturation. To see how this occurs, consider the case where the gate input was high and then is suddenly brought down to the low level. Transistor Q_2 will turn off relatively fast because of the availability of a large reverse current supplied to its base terminal by the collector of Q_1. On the other hand, the base of Q_3 will have to discharge through the 1-kΩ resistance, and thus Q_3 will take some time to turn off. Meanwhile Q_4 will turn on, and a large current pulse will flow through the series combination of Q_4 and Q_3. Part of this current will serve the useful purpose of charging up any load capacitance to the logic-1 level. The magnitude of the current pulse will be limited by the 130-Ω resistance to about 30 mA.

The occurrence of these current pulses of short duration (called **current spikes**) raises another important issue. The current spikes have to be supplied by the V_{CC} source and, because of its finite source resistance, will result in voltage spikes (or "glitches") superimposed on V_{CC}. These voltage spikes could be coupled to other gates and flip-flops in the digital system and thus might produce false switching in other parts of the system. This effect, which might loosely be called **crosstalk,** is a problem in TTL systems. To reduce the size of the voltage spikes, capacitors (called bypass capacitors) should be connected between the supply rail and ground at frequent locations. These capacitors lower the impedance of the supply-voltage source and hence reduce the magnitude of the voltage spikes. Alternatively, one can think of the bypass capacitors as supplying the impulsive current spikes.

EXERCISES

14.8 Assuming that Q_4 has $\beta = 50$ and that at the verge of saturation $V_{CEsat} = 0.3$ V, find the value of i_L at which Q_4 saturates.

Ans. 4.16 mA

14.9 Assuming that at a current of 1 mA the voltage drops across the emitter–base junction of Q_4 and the diode D are each 0.7 V, find v_O when $i_L = 1$ mA and 10 mA. (Note the result of the previous exercise.)

Ans. 3.6 V; 2.7 V

14.10 Find the maximum current that can be sourced by a TTL gate while the output high level (V_{OH}) remains greater than the minimum guaranteed value of 2.4 V.

Ans. 12.3 mA; or, more accurately, taking the base current of Q_4 into account, 13.05 mA

14.4 CHARACTERISTICS OF STANDARD TTL

Because of its historical popularity and continued importance, TTL will be studied further in this and the next sections. In this section we shall consider some of the important characteristics of standard TTL gates. Special improved forms of TTL will be dealt with in Section 14.5.

Transfer Characteristic

Figure 14.23 shows the TTL gate together with a sketch of its voltage transfer characteristic drawn in a piecewise-linear fashion. The actual characteristic is, of course, a smooth curve. We shall now explain the transfer characteristic and calculate the various break-points and slopes. It will be assumed that the output terminal of the gate is open.

Segment *AB* is obtained when transistor Q_1 is saturated, Q_2 and Q_3 are off, and Q_4 and D are on. The output voltage is approximately two diode drops below V_{CC}. At point *B* the phase splitter (Q_2) begins to turn on because the voltage at its base reaches 0.6 V (0.5 V + V_{CEsat} of Q_1).

Over segment *BC*, transistor Q_1 remains saturated, but more and more of its base current *I* gets diverted to its base–collector junction and into the base of Q_2, which operates as a linear amplifier. Transistor Q_4 and diode D remain on, with Q_4 acting as an emitter follower. Meanwhile the voltage at the base of Q_3, although increasing, remains insufficient to turn Q_3 on (less than 0.6 V).

Let us now find the slope of segment *BC* of the transfer characteristic. Let the input v_I increase by an increment Δv_I. This increment appears at the collector of Q_1, since the saturated Q_1 behaves (approximately) as a three-terminal short circuit as far as signals are

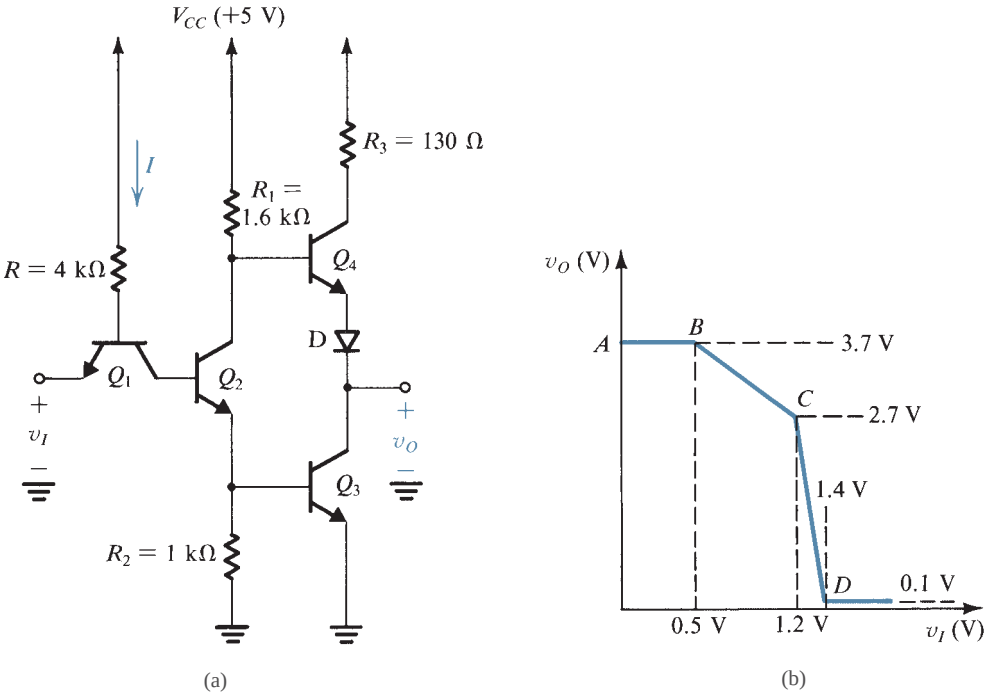


FIGURE 14.23 The TTL gate and its voltage transfer characteristic.

concerned. Thus at the base of Q_2 we have a signal Δv_I. Neglecting the loading of emitter follower Q_4 on the collector of Q_2, we can find the gain of the phase splitter from

$$\frac{v_{c2}}{v_{b2}} = \frac{-\alpha_2 R_1}{r_{e2} + R_2} \tag{14.6}$$

The value of r_{e2} will obviously depend on the current in Q_2. This current will range from zero (as Q_2 begins to turn on) to the value that results in a voltage of about 0.6 V at the emitter of Q_2 (the base of Q_3). This value is about 0.6 mA and corresponds to point C on the transfer characteristic. Assuming an average current in Q_2 of 0.3 mA, we obtain $r_{e2} \simeq 83\ \Omega$. For $\alpha = 0.98$, Eq. (14.6) results in a gain value of 1.45. Since the gain of the output follower Q_4 is close to unity, the overall gain of the gate, which is the slope of the BC segment, is about –1.45.

As already implied, breakpoint C is determined by Q_3 starting to conduct. The corresponding input voltage can be found from

$$\begin{aligned} v_I(C) &= V_{BE3} + V_{BE2} - V_{CE\text{sat}}(Q_1) \\ &= 0.6 + 0.7 - 0.1 = 1.2\ \text{V} \end{aligned}$$

At this point the emitter current of Q_2 is approximately 0.6 mA. The collector current of Q_2 is also approximately 0.6 mA; neglecting the base current of Q_4, the voltage at the collector of Q_2 is

$$v_{C2}(C) = 5 - 0.6 \times 1.6 \cong 4\ \text{V}$$

Thus Q_2 is still in the active mode. The corresponding output voltage is

$$v_O(C) = 4 - 0.65 - 0.65 = 2.7\ \text{V}$$

As v_I is increased past the value of $v_I(C) = 1.2$ V, Q_3 begins to conduct and operates in the active mode. Meanwhile, Q_1 remains saturated, and Q_2 and Q_4 remain in the active mode. The circuit behaves as an amplifier until Q_2 and Q_3 saturate and Q_4 cuts off. This occurs at point D on the transfer characteristic, which corresponds to an input voltage $v_I(D)$ obtained from

$$\begin{aligned} v_I(D) &= V_{BE3} + V_{BE2} + V_{BC1} - V_{BE1} \\ &= 0.7 + 0.7 + 0.7 - 0.7 = 1.4\ \text{V} \end{aligned}$$

Note that we have in effect assumed that at point D transistor Q_1 is still saturated, but with $V_{CE\text{sat}} \simeq 0$. To see how this comes about, note that from point B on, more and more of the base current of Q_1 is diverted to its base–collector junction. Thus while the drop across the base–collector junction increases, that across the base–emitter junction decreases. At point D these drops become almost equal. For $v_I > v_I(D)$ the base–emitter junction of Q_1 cuts off; thus Q_1 leaves saturation and enters the inverse active mode.

Calculation of gain over the segment CD is a relatively complicated task. This is due to the fact that there are two paths from input to output: one through Q_3 and one through Q_4. A simple but gross approximation for the gain of this segment can be obtained from the coordinates of points C and D in Fig. 14.23(b), as follows:

$$\begin{aligned} \text{Gain} &= -\frac{v_O(C) - v_O(D)}{v_I(D) - v_I(C)} \\ &= -\frac{2.7 - 0.1}{1.4 - 1.2} = -13\ \text{V/V} \end{aligned}$$

From the transfer curve of Fig. 14.23(b) we can determine the critical points and the noise margins as follows: $V_{OH} = 3.7$ V; V_{IL} is somewhere in the range of 0.5 V to 1.2 V, and thus a conservative estimate would be 0.5 V; $V_{OL} = 0.1$ V; $V_{IH} = 1.4$ V; $NM_H = V_{OH} - V_{IH} = 2.3$ V; and $NM_L = V_{IL} - V_{OL} = 0.4$ V. It should be noted that these values are computed assuming that the gate is not loaded and without taking into account power-supply or temperature variations.

EXERCISE

14.11 Taking into account the fact that the voltage across a forward-biased *pn* junction changes by about –2 mV/°C, find the coordinates of points *A*, *B*, *C*, and *D* of the gate transfer characteristic at –55°C and at +125°C. Assume that the characteristic in Fig. 14.23(b) applies at 25°C, and neglect the small temperature coefficient of V_{CEsat}.

Ans. At –55°C: (0, 3.38), (0.66, 3.38), (1.52, 2.16), (1.72, 0.1); at +125°C: (0, 4.1), (0.3, 4.1), (0.8, 3.46), (1.0, 0.1)

Manufacturers' Specifications

Manufacturers of TTL usually provide curves for the gate transfer characteristic, the input *i*–*v* characteristic, and the output *i*–*v* characteristic, measured at the limits of the specified operating temperature range. In addition, guaranteed values are usually given for the parameters V_{OL}, V_{OH}, V_{IL}, and V_{IH}. For standard TTL (known as the 74 series) these values are $V_{OL} = 0.4$ V, $V_{OH} = 2.4$ V, $V_{IL} = 0.8$ V, and $V_{IH} = 2$ V. These limit values are guaranteed for a specified tolerance in power-supply voltage and for a maximum fan-out of 10. From our discussion in Section 14.3 we know that the maximum fan-out is determined by the maximum current that Q_3 can sink while remaining in saturation and while maintaining a saturation voltage lower than a guaranteed maximum ($V_{OL} = 0.4$ V). Calculations performed in Section 14.3 indicate the possibility of a maximum fan-out of 20 to 30. Thus the figure specified by the manufacturer is appropriately conservative.

The parameters V_{OL}, V_{OH}, V_{IL}, and V_{IH} can be used to compute the noise margins as follows:

$$NM_H = V_{OH} - V_{IH} = 0.4 \text{ V}$$

$$NM_L = V_{IL} - V_{OL} = 0.4 \text{ V}$$

EXERCISES

14.12 In Section 14.3 we found that when the gate input is high, the base current of Q_3 is approximately 2.6 mA. Assume that this value applies at 25°C and that at this temperature $V_{BE} \simeq 0.7$ V. Taking into account the –2-mV/°C temperature coefficient of V_{BE} and neglecting all other changes, find the base current of Q_3 at –55°C and at +125°C.

Ans. 2.2 mA; 3 mA

14.13 Figure E14.13 shows sketches of the i_L–v_O characteristics of a TTL gate when the output is low. Use these characteristics together with the results of Exercise 14.12 to calculate the value of β of transistor Q_3 at –55°C, +25°C, and +125°C.

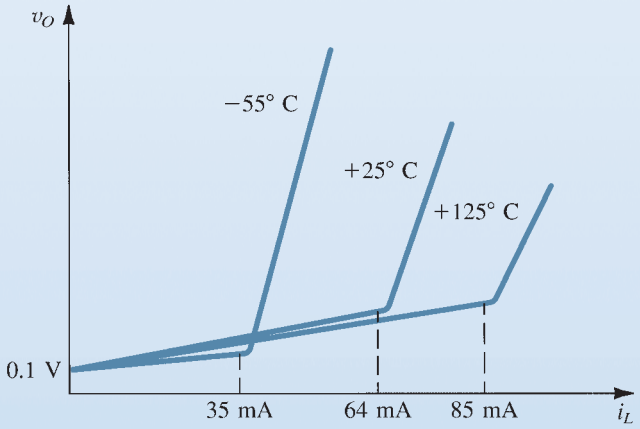


FIGURE E14.13

Ans. 16; 25; 28

Propagation Delay

The propagation delay of TTL gates is defined conventionally as the time between the 1.5-V points of corresponding edges of the input and output waveforms. For standard TTL (also known as *medium-speed* TTL) t_P is typically about 10 ns.

As far as power dissipation is concerned it can be shown (see Exercise 14.14) that when the gate output is high the gate dissipates 5 mW, and when the output is low the dissipation is 16.7 mW. Thus the average dissipation is 11 mW, resulting in a delay-power product of about 100 pJ.

EXERCISE

14.14 Calculate the value of the supply current (I_{CC}), and hence the power dissipated in the TTL gate, when the output terminal is open and the input is (a) low at 0.2 V (see Fig. 14.22) and (b) high at +5 V (see Fig. 14.20).

Ans. (a) 1 mA, 5 mW; (b) 3.33 mA, 16.7 mW

Dynamic Power Dissipation

In Section 14.3 the occurrence of supply current spikes was explained. These spikes give rise to additional power drain from the V_{CC} supply. This **dynamic power** is also dissipated in the gate circuit. It can be evaluated by multiplying the average current due to the spikes by V_{CC}, as illustrated by the solution of Exercise 14.15.

EXERCISE

14.15 Consider a TTL gate that is switched on and off at the rate of 1 MHz. Assume that each time the gate is turned off (that is, the output goes high) a supply-current pulse of 30-mA amplitude and 2-ns width occurs. Also assume that no current spike occurs when the gate is turned on. Calculate the average supply current due to the spikes, and the dynamic power dissipation.

Ans. 60 μA; 0.3 mW

The TTL NAND Gate

Figure 14.24 shows the basic TTL gate. Its most important feature is the **multiemitter transistor** Q_1 used at the input. Figure 14.25 shows the structure of the multiemitter transistor.

It can be easily verified that the gate of Fig. 14.24 performs the NAND function. The output will be high if one (or both) of the inputs is (are) low. The output will be low in only

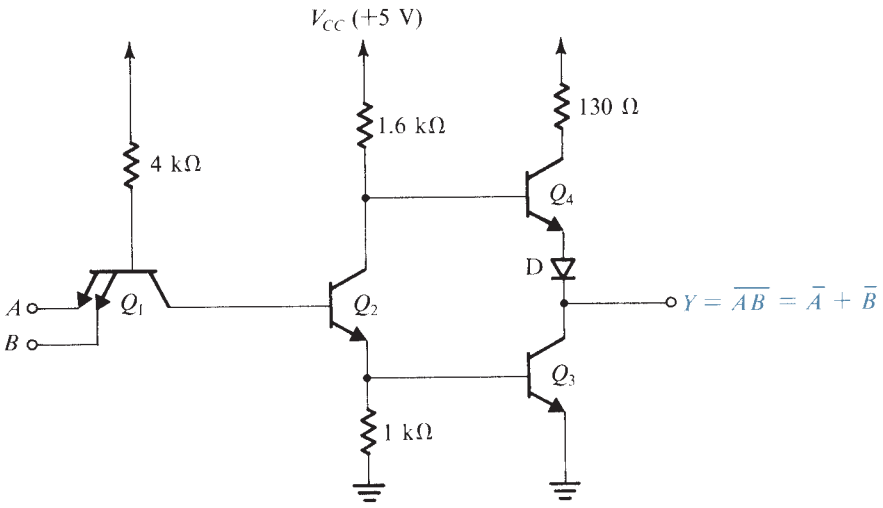


FIGURE 14.24 The TTL NAND gate.

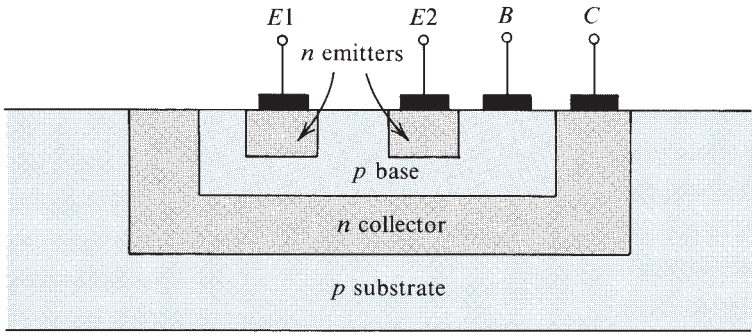


FIGURE 14.25 Structure of the multiemitter transistor Q_1.

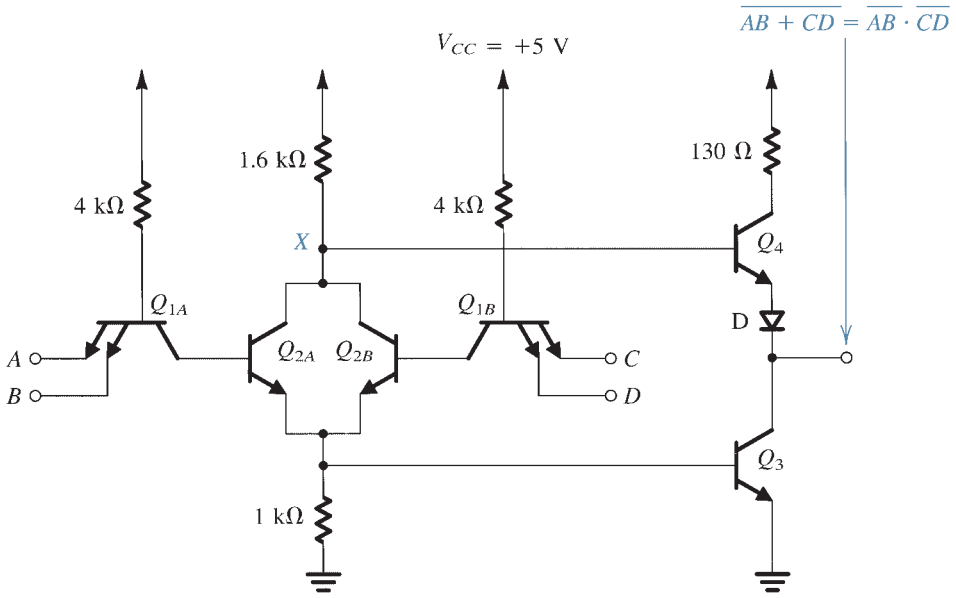


FIGURE 14.26 A TTL AND-OR-INVERT gate.

one case: when both inputs are high. Extension to more than two inputs is straightforward and is achieved by diffusing additional emitter regions.

Although theoretically an unused input terminal may be left open-circuited, this is generally not a good practice. An open-circuit input terminal acts as an "antenna" that "picks up" interfering signals and thus could cause erroneous gate switching. An unused input terminal should therefore be connected to the positive power supply *through a resistance* (of, say, 1 kΩ). In this way the corresponding base–emitter junction of Q_1 will be reverse-biased and thus will have no effect on the operation of the gate. The series resistance is included in order to limit the current in case of breakdown of the base–emitter junction due to transients on the power supply.

Other TTL Logic Circuits

On a TTL MSI chip there are many cases in which logic functions are implemented using "stripped-down" versions of the basic TTL gate. As an example we show in Fig. 14.26 the TTL implementation of the AND-OR-INVERT function. As shown, the phase-splitter transistors of two gates are connected in parallel, and a single output stage is used. The reader is urged to verify that the logic function realized is as indicated.

At this point it should be noted that the totem-pole output stage of TTL does *not* allow connecting the output terminals of two gates to realize the AND function of their outputs (known as the wired-AND connection). To see the reason for this, consider two gates whose outputs are connected together, and let one gate have a high output and the other have a low output. Current will flow from Q_4 of the first gate through Q_3 of the second gate. The current value will fortunately be limited by the 130-Ω resistance. Obviously, however, no useful logic function is realized by this connection.

The lack of wired-AND capability is a drawback of TTL. Nevertheless, the problem is solved in a number of ways, including doing the paralleling at the phase-splitter stage, as illustrated in Fig. 14.26. Another solution consists of deleting the emitter-follower transistor

altogether. The result is an output stage consisting solely of the common-emitter transistor Q_3 without even a collector resistance. Obviously, one can connect the outputs of such gates together to a common collector resistance and achieve a wired-AND capability. TTL gates of this type are known as **open-collector TTL.** The obvious disadvantage is the slow rise time of the output waveform.

Another useful variant of TTL is the **tristate** output arrangement explored in Exercise 14.16.

EXERCISE

14.16 The circuit shown in Fig. E14.16 is called tristate TTL. Verify that when the terminal labeled $\overline{\text{Third state}}$ is high, the gate functions normally and that when this terminal is low, both transistors Q_3 and Q_4 cut off and the output of the gate is an open circuit. The latter state is the third state, or the high-output-impedance state.

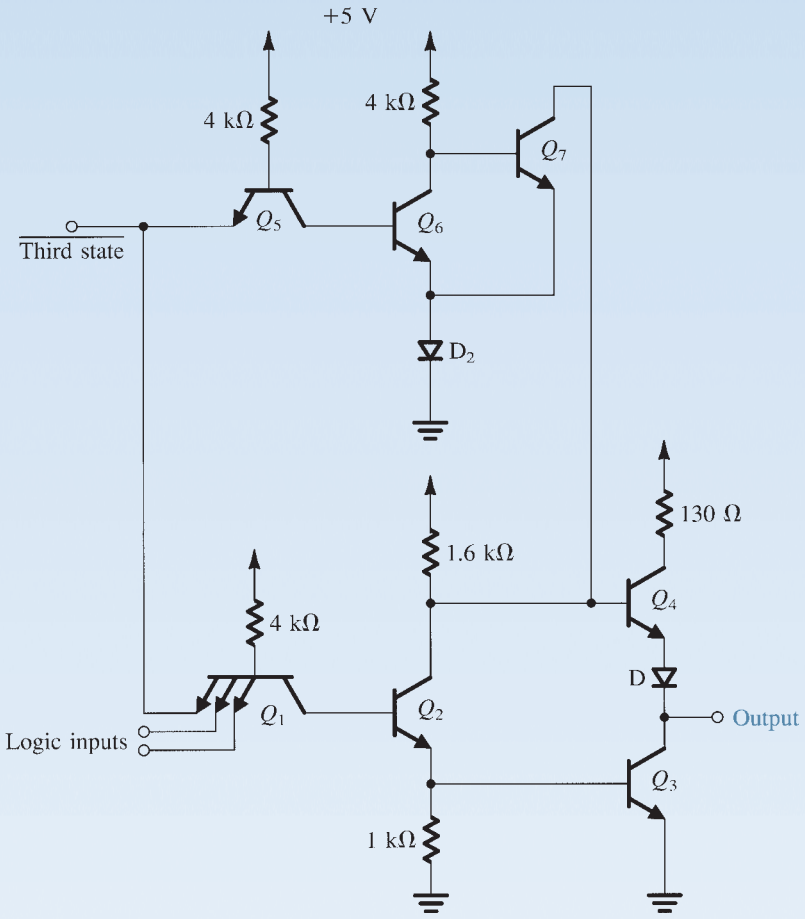


FIGURE E14.16

Tristate TTL enables the connection of a number of TTL gates to a common output line (or *bus*). At any particular time the signal on the bus will be determined by the one TTL gate

that is *enabled* (by raising its third-state input terminal). All other gates will be in the third state and thus will have no control of the bus.

14.5 TTL FAMILIES WITH IMPROVED PERFORMANCE

The standard TTL circuits studied in the two previous sections were introduced in the mid-1960s. Since then, several improved versions have been developed. In this section we shall discuss some of these improved TTL subfamilies. As will be seen the improvements are in two directions: increasing speed and reducing power dissipation.

The speed of the standard TTL gate of Fig. 14.24 is limited by two mechanisms: first, transistors Q_1, Q_2, and Q_3 saturate, and hence we have to contend with their finite storage time. Although Q_2 is discharged reasonably quickly because of the active mode of operation of Q_1, as already explained, this is not true for Q_3, whose base charge has to leak out through the 1-kΩ resistance in its base circuit. Second, the resistances in the circuit, together with the various transistor and wiring capacitances, form relatively long time constants, which contribute to lengthening the gate delay.

It follows that there are two approaches to speeding up the operation of TTL. The first is to prevent transistor saturation and the second is to reduce the values of all resistances. Both approaches are utilized in the Schottky TTL circuit family.

Schottky TTL

In Schottky TTL, transistors are prevented from saturation by connecting a low-voltage-drop diode between base and collector, as shown in Fig. 14.27. These diodes, formed as a metal-to-semiconductor junction, are called Schottky diodes and have a forward voltage drop of about 0.5 V. We have briefly discussed Schottky diodes in Section 3.9. Schottky diodes[4] are easily fabricated and do not increase chip area. In fact, the Schottky TTL fabrication process has been designed to yield transistors with smaller areas and thus higher β and f_T than those produced by the standard TTL process. Figure 14.27 also shows the symbol used to represent the combination of a transistor and a Schottky diode, referred to as a Schottky transistor.

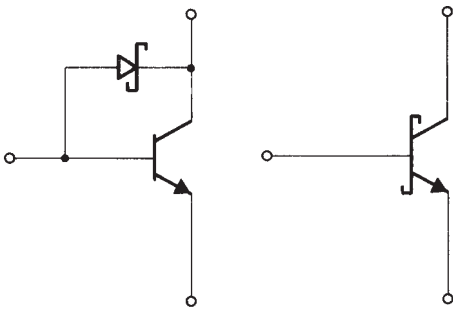


FIGURE 14.27 **(a)** A transistor with a Schottky diode clamp. **(b)** Circuit symbol for the connection in (a), known as a Schottky transistor.

[4] Note that silicon Schottky diodes exhibit voltage drops of about 0.5 V, whereas GaAs Schottky diodes (Section 5.12) exhibit voltage drops of about 0.7 V.