

Homework 8 Yash Shah

Problem 5.1b

S.16.1 —

	Virtual Page	TLB	PT	Valid	Tag	Physical Page
4669 0x123d	1	M	H	1 1 1	6 7 3 1	12 4 6 13
2227 0x0863	0	M	H	1 1 1	0 7 3 1	5 4 6 13
13916 0x365c	3	H	H	1 1 1	0 7 3 1	5 4 6 13
34587 0x871b	8	M	H	1 1 1	0 7 3 1	5 4 6 13
48870 0xbeef6	6	M	H	1 1 1	0 8 3 11	5 14 6 12
12608 0x3140	3	H	H	1 1 1	0 8 3 6	5 14 6 12
49225 0xe040	0	M	M	1 1	0 8 3 6	15 14 6 12

5.16.2 —

Address	Virtual Page	TLB	PT	Valid	Tag	Physical Page
4669 0x123d	1	M	H	1	11	12
				1	7	4
				1	3	6
2227 0x08b3	0	M	H	1	1	13
				1	11	12
				1	7	4
13916 0x265c	3	H	H	1	3	6
				1	1	13
				1	2	13
34587 0x8716	8	M	H	1	7	4
				1	3	6
				1	1	13
48870 0xbeeb6	11	M	H	1	0	5
				1	7	4
				1	3	6
12608 0x3140	3	H	H	1	11	12
				1	2	13
				1	7	4
49225 0xe040	12	M	M	1	3	6
				1	2	15
				1	0	5

Large page size could reduce the number of misses, but that could also increase the risk that the cache block is too small to fit the page.

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Address	Virtual Page	TLB				Valid	Tag	Physical Page	
		TLB	PT	Valid	Index				
4669 0x123d	1	M	H	1	b	12	1		
				1	7	4	0		
				1	3	6	1		
2227 0x0863	0	M	H	1	1	13	0		
				1	0	5	1		
				1	7	4	0		
13916 0x365c	3	H	H	1	3	6	1		
				1	1	13	0		
				1	0	5	1		
34587 0x8716	8	M	H	1	7	4	0		
				1	3	6	1		
				1	1	13	0		
48810 0xbbe6	b	M	H	1	0	5	1		
				1	3	6	1		
				1	11	12	0		
12608 0x3140	3	H	H	1	0	5	1		
				1	3	6	1		
				1	6	12	0		
49225 0xe040	c	M	M	1	c	15	1		
				1	8	14	0		
				1	3	6	1		
				1	b	12	0		

Address	Virtual Page	TLB	PT	Valid		Physical Page	Index
					Tag		
4669 0x123d	1	M	H	1	b	12	0
				1	7	4	1
				1	3	6	0
2227 0x08b3	0	M	H	1	1	13	1
				1	0	5	0
				1	7	4	1
13916 0x365c	3	H	H	1	3	6	0
				1	1	13	1
				1	0	5	0
34587 0x871b	8	M	H	1	7	4	1
				1	3	6	0
				1	1	13	1
48870 0xbee6	6	M	H	1	0	5	0
				1	8	14	1
				1	3	6	0
12608 0x3140	3	H	H	1	11	12	1
				1	0	5	0
				1	8	14	1
49225 0xe040	c	M	M	1	c	15	0
				1	8	14	1
				1	3	6	0
				1	b	12	1

5.16.4 —

Address	Virtual Page	TLB	PT	Valid	Tag	Physical Page	Index
4669 0x123d	1	M	H	1	6	12	0
				1	7	4	1
				1	3	6	2
				0	1	13	3
2227 0x08b3	0	M	H	1	0	5	0
				1	7	4	1
				1	3	6	2
				0	1	13	3
18916 0x365c	3	H	H	1	0	5	0
				1	7	4	1
				1	3	6	2
				0	1	13	3
34587 0x8716	8	M	H	1	0	5	0
				1	7	4	1
				1	3	6	2
				0	1	13	3
48810 0xbeec6	6	M	H	1	0	5	0
				1	3	14	1
				1	11	6	2
				0	11	12	3
12608 0x3140	3	H	H	1	0	5	0
				1	3	14	1
				1	6	6	2
				0	6	12	3
49225 0xe040	6	M	M	1	2	15	0
				1	3	14	1
				1	6	6	2
				0	6	12	3

5.16.5 —

TLB caches frequently-used virtual-to-physical address mappings. Without a TLB, virtual memory accesses would need to be handled by the CPU in a slower way, leading to slower overall performance.

Problem 5.20

5.20.1 —

0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0
M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M	M

5.20.2 —

0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0
M	M	M	M	M	M	M	M	H	H	M	M	M	M	H	M	M

5.20.3 —

0	1	2	3	4	5	6	7	0	1	2	3	4	5	6	7	0
M	M	M	M	H	M	M	H	H	M	H	M	H	M	M	H	M

5.20.4 —

MRU has locality — maximizes the hit dependency on the data present in the cache.
MRU most optimal policy, 3 total hits

5.20.5 —

Optimal policies depend on specific access patterns of each application or workload.
It's extremely difficult to have a one-size-fits-all solution, so it's more important to use prediction.

5.20.6 —

Choosing not to cache \Rightarrow possible more hits

Choosing to cache \Rightarrow address that is cached cannot all be stored in the size of the cache