

CS M51A, Fall 2022, Assignment 2

(Total Mark: 100 points, 10%)

Due: Wed Oct 26, 10:00 AM Pacific Time

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Note: You must complete the assignments entirely on your own,
without discussing with others.

1. A logical family has the following ranges of voltages to represent the high and low values: HIGH=2V to 3.3V, LOW=0.0V to 0.8V.

(a) (2 Points) For the following signal values, determine the corresponding logic values:

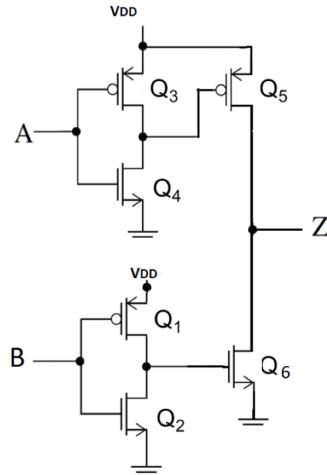
- 3V. *High*
- 0.5V. *Low*
- -5.0V. *undefined behavior*
- 1.2V. *undefined behavior*

(b) (4 Points) For a module with inputs x and y and output z you have performed the following set of measures (all in volts): What type of gate does this circuit implement?

x	y	z
0.2 ^L	0.2 ^H	2.8 ^H
0.3 ^L	3.0 ^H	0.2 ^L
3.1 ^H	0.4 ^L	0.2 ^L
3.0 ^H	3.1 ^H	0.3 ^L

*NOR gate because all z values
are L if at least one output is high,
and if both are H, then it is low.*

2. (a) (6 Points) Given the circuit below, complete the table below, determining the resistances for Q_1 to Q_6 and the final output Z . The transistors Q_1 to Q_6 should be High or Low (show by 'H' or 'L') resistance. The output Z may be 0, 1, float (show by -) or short (show by *). Remember short means the output is connected to both VDD and ground at the same time.

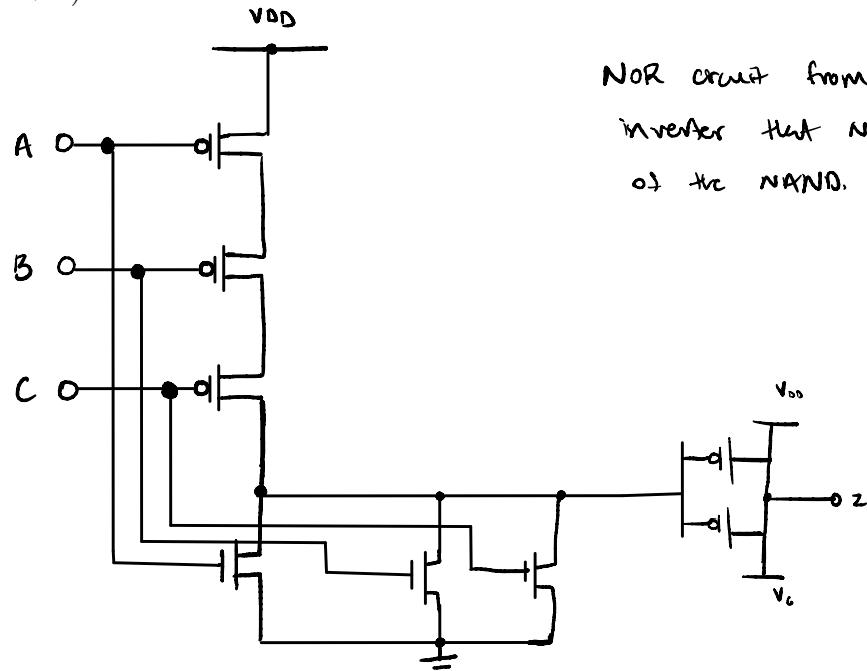


A	B	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Z
0	0	L	H	L	H	H	L	1
0	1	H	L	L	H	H	H	-
1	0	L	H	H	L	L	L	*
1	1	H	L	H	L	L	H	0

- (b) (4 Points) Explain why we would not use the transistor configuration given above in practice.

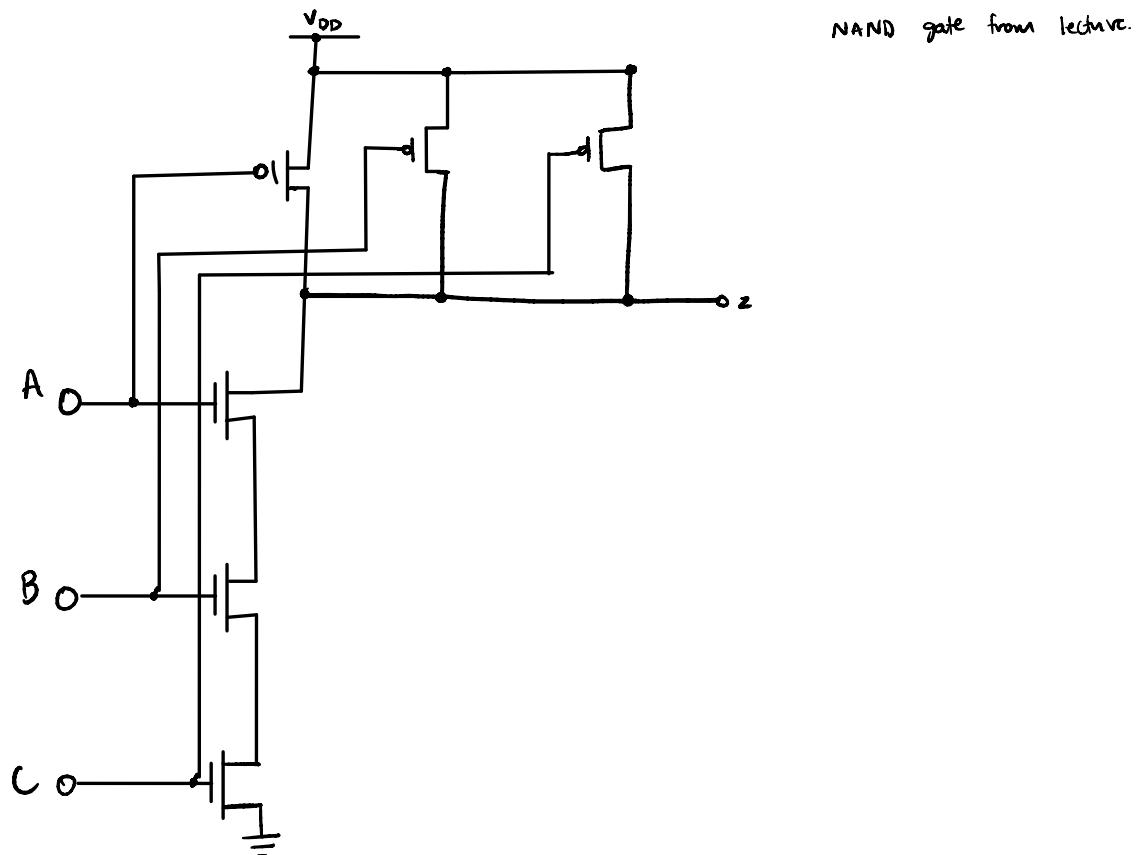
This circuit has inputs that would cause Z to have a floating charge or cause the circuit to short circuit, effectively making the circuit not computable if $a + b$. Hence, the transistor configuration would misrepresent data / have undefined output which is simply wrong. The circuit must have an output that is 1 or 0 for an actualized representation.

3. (a) (4 Points) Draw a circuit (using PMOS and NMOS transistors) which performs $F = (A + B + C)$. Do not use more than 8 transistors in total.



NOR circuit from class with inverter that NOT's the result of the NAND.

- (b) (4 Points) Draw a circuit (using PMOS and NMOS transistors) which performs $F = (A' + B' + C')$. Do not use more than 6 transistors in total.



NAND gate from lecture.

4. (a) (8 Points) Write the boolean algebra function for the following table.

	00	01	11	10
0	1	1	1	1
1	0	0	1	0
	x'	y'	z'	z

$$xyz + z' \Rightarrow z' + xy$$

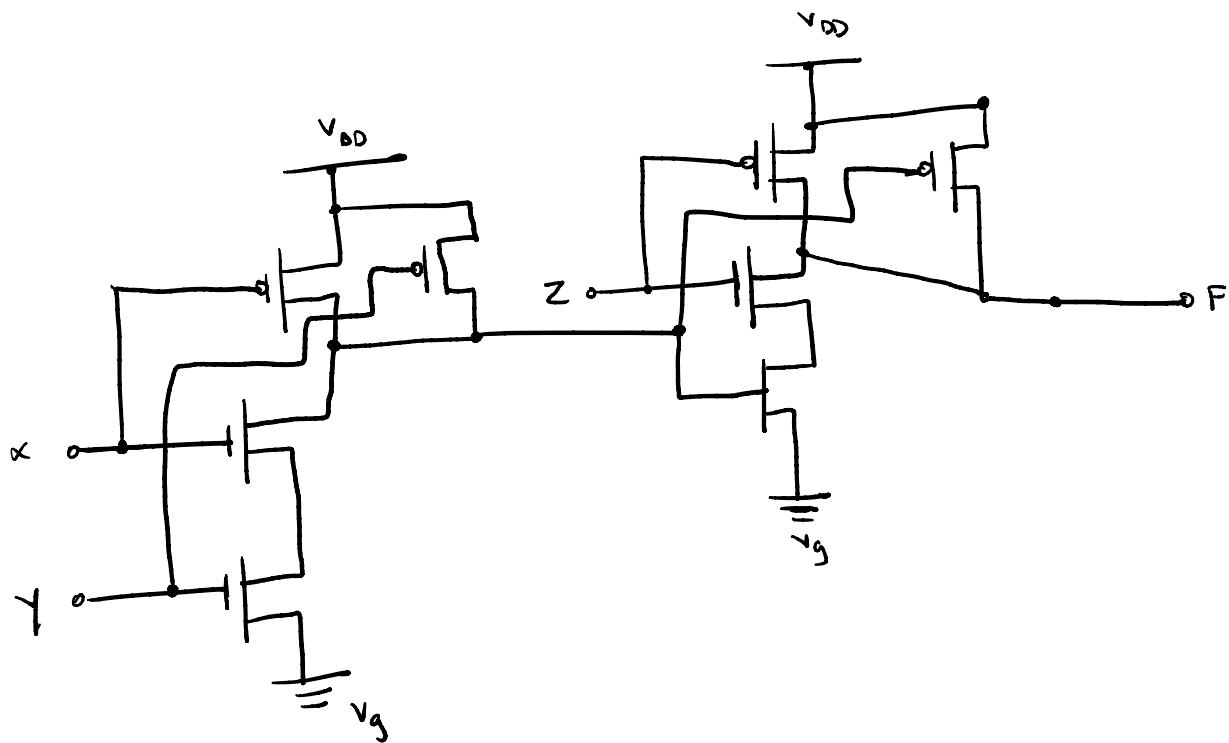
de-morgan's

X	Y	Z	F
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

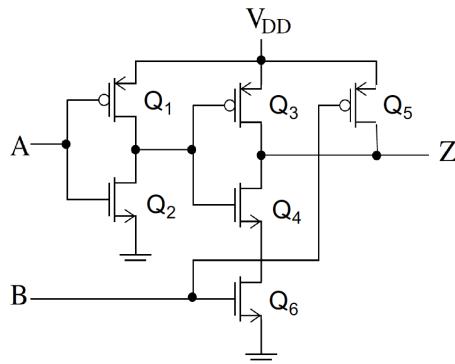
$$F = z' + xy$$

(b) (8 Points) Implement the function from part (a) using PMOS and NMOS transistors. Use at most 8 transistors total.

$$\begin{aligned} F &= z' + xy \\ &= (z \cdot (xy))' \quad \text{least } \underbrace{\Rightarrow \text{NAND, NOR}}_{\text{double NAND}} \end{aligned}$$



5. (a) (6 Points) Given the circuit below, complete the table below, determining the resistances for Q_1 to Q_6 and the final output Z . The transistors Q_1 to Q_6 should be High or Low (show by 'H' or 'L') resistance. The output Z may be 0, 1, float (show by -) or short (show by *).



A	B	Q_1	Q_2	Q_3	Q_4	Q_5	Q_6	Z
0	0	L	H	H	L	L	H	1
0	1	L	H	H	L	H	L	0
1	0	H	L	L	H	L	H	1
1	1	H	L	L	H	H	L	1

- (b) (4 Points) Write sum of MINTERMS and product of MAXTERMS for Z .

Sum of minterm = $A'B' + AB' + AB$

Product of maxterm = $A + B'$

6. (a) (4 Points) Write the sum of minterms and product of maxterms function for the following table.

A	B	F
0	0	0
0	1	1
1	0	0
1	1	0

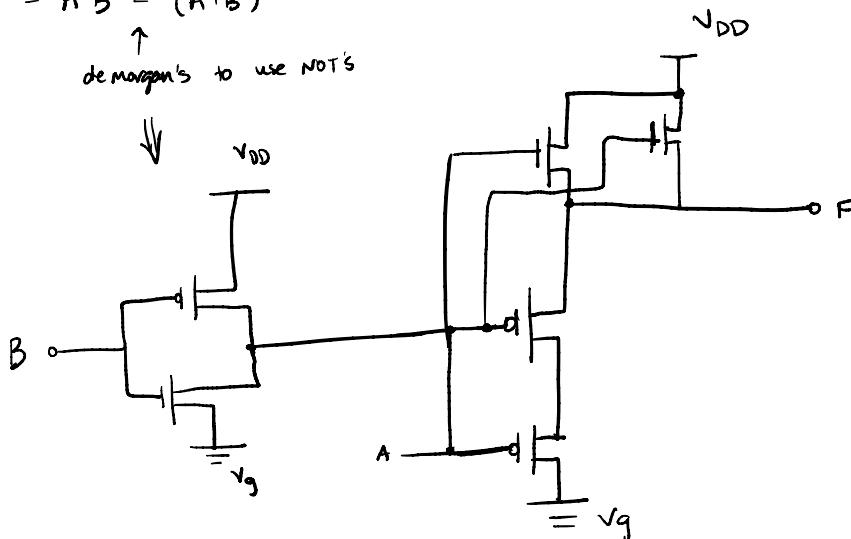
$$\text{minterms: } F = A'B$$

$$\text{maxterms: } F = (A+B)(A'+B)(A'+B')$$

- (b) (4 Points) Implement F using PMOS and NMOS transistors. Use at most 6 transistors in total; only the signal itself can be used as input.

$$F = A'B = (A+B')$$

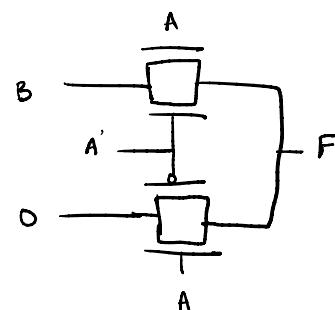
↑
de Morgan's to use NOT's



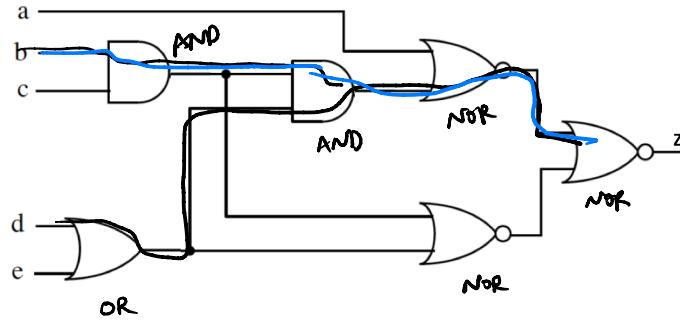
- (c) (4 Points) Implement F using inverters and transmission gates; you may use logic 0, logic 1 or the signal itself as input.

A	B	F
0	0	0
0	1	1
1	0	0
1	1	0

A	F
0	1
1	0



7. Consider the following system where the output Z has a load (L) of 4.



Gate Type	Fan-in	Propagation Delays (ns)	
		t_{pLH}	t_{pHL}
NOT	1	$0.02 + 0.038L$	$0.05 + 0.017L$
NAND	2	$0.05 + 0.038L$	$0.08 + 0.027L$
NOR	2	$0.06 + 0.075L$	$0.07 + 0.016L$
AND	2	$0.08 + 0.038L$	$0.09 + 0.027L$
OR	2	$0.08 + 0.075L$	$0.09 + 0.016L$

- (a) (4 Points) determine the low to high propagation delay $t_{pLH}(d, z)$ of the output z.

$$t_{pLH}(\text{OR} + \text{AND} + \text{NOR} + \text{NOR})$$

$$0.08 + 0.075L + 0.08 + 0.038L + 0.07 + 0.016L + 0.06 + 0.075$$

$$\begin{aligned} 0.29 + 0.204L^4 &= 0.28 + 0.816 \\ &= 1.106 \end{aligned}$$

$$t_{pLH}(d, z) = 1.106 \text{ ns}$$

- (b) (4 Points) determine the high to low propagation delay $t_{pHL}(b, z)$ of the output z.

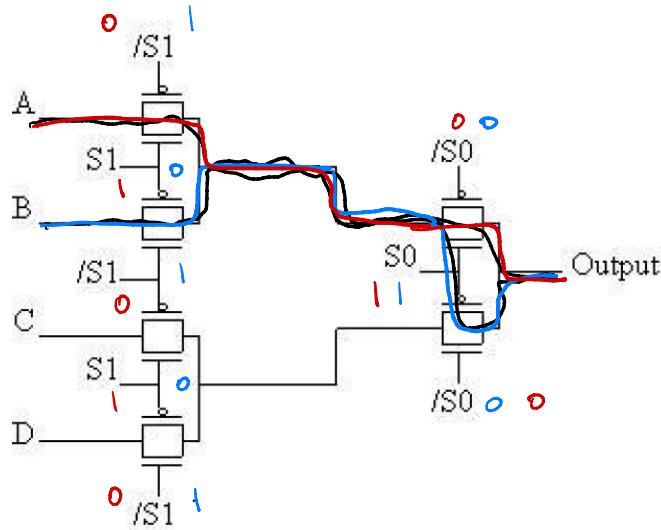
$$t_{pHL}(\text{AND} + \text{AND} + \text{NOR} + \text{NOR})$$

$$0.09 + 0.027L + 0.09 + 0.027L + 0.06 + 0.075L + 0.07 + 0.016L$$

$$0.31 + 0.145(4) = 0.89$$

$$t_{pHL} = 0.89 \text{ ns}$$

8. Consider the following circuit, where $/S_1$ and $/S_0$ present complement (NOT) of S_1 and S_0 , respectively.



(a) (4 Points) What is the value of output when $S_0=1$, $S_1=0$.

B

(b) (4 Points) What is the value of output when $S_0=1$, $S_1=1$.

A

(c) (4 Points) Write a sum of product expression for the output in terms of A, B, C, D, S_0, S_1 .

S_0	S_1	Output
0	0	D
0	1	C
1	0	B
1	1	A

In the circuit we have $S_0 = 0, S_0' = 1$
 $S_1 = 0, S_1' = 1$

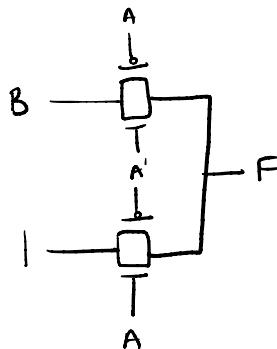
Therefore, using the table

$\Rightarrow F = S_0' S_1' D + S_0 S_1' C + S_0' S_1 B + S_1' S_1 A$

9. Use transmission gates to implement the following logical expressions; you may use logic 0, logic 1, the signal itself or its complement as input, e.g. A, A', 0, 1 are all valid input of your design:

(a) (4 Points) $F = A + B$ (OR gate)

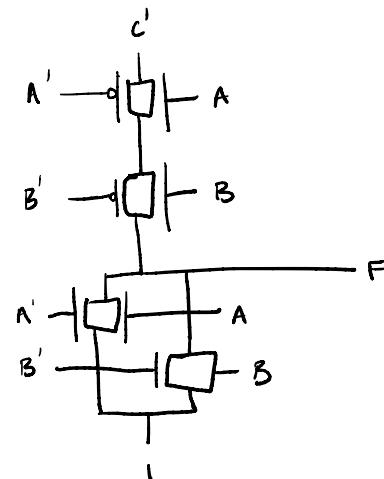
A	B	F
0	0	0
0	1	1
1	0	1
1	1	1



(b) (4 Points) $F = (ABC)'$ (3-input NAND gate)

A	B	C	F
0	0	0	1
1	0	0	1
0	1	0	1
0	0	1	1
0	1	1	1
1	0	1	1
1	1	0	1
1	1	1	0

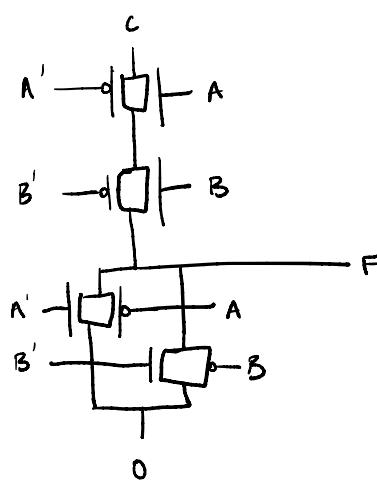
A	B	F
0	0	1
1	0	1
0	1	1
0	0	1
1	0	1
1	1	0



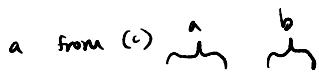
(c) (4 Points) $F = ABC$ (3-input AND gate)

A	B	C	F
0	0	0	0
1	0	0	0
0	1	0	0
0	0	1	0
0	1	1	0
1	0	1	0
1	1	0	0
1	1	1	1

A	B	F
0	0	0
1	0	0
0	1	0
0	0	0
1	0	0
1	1	1



a or b from (a)



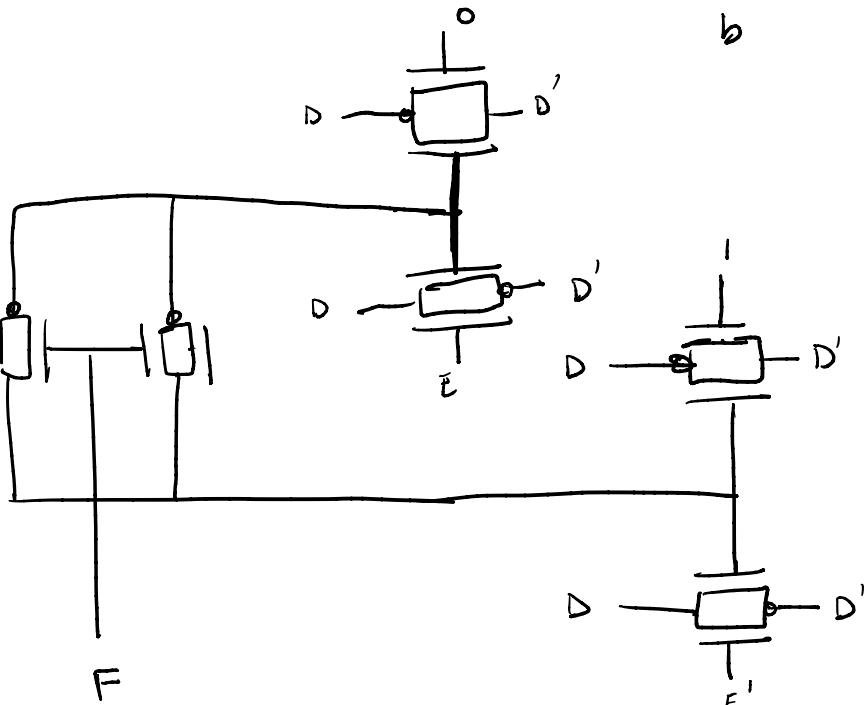
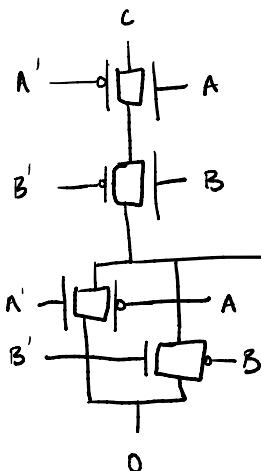
$$(d) \text{ (4 Points)} F = ABC + DE$$

$$b = \begin{array}{c|cc|c} D & E & b \\ \hline 0 & 0 & 0 \\ 0 & 1 & 0 \\ 1 & 0 & 1 \\ 1 & 1 & 1 \end{array} \xrightarrow{D=0} 0$$

$$\begin{array}{c|cc} D & b \\ \hline 0 & 0 \\ 1 & E \end{array}$$

$$b' = \begin{array}{c|cc|c} D & E & b' \\ \hline 0 & 0 & 1 \\ 0 & 1 & 1 \\ 1 & 0 & 1 \\ 1 & 1 & 0 \end{array} \xrightarrow{D=1} 1 \quad \begin{array}{c|cc} D & b' \\ \hline 0 & 1 \\ 1 & E' \end{array}$$

a



10. (2 Points) For a transmission gate, why are both PMOS and NMOS used?

PMOS passes a strong 1 and weak 0, while NMOS passes a weak 1 and strong 0.

Therefore, they complement each other to cover both cases of low and high values without degradation to the circuit and the outputs.