CS M51A, Fall 2022, Assignment 4
(Total Mark: 100 points, 10%)

Due: Tue Nov 29th, 10:00 AM Pacific Time

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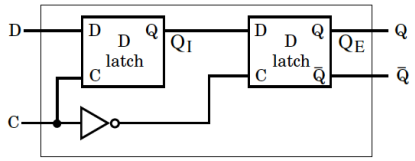
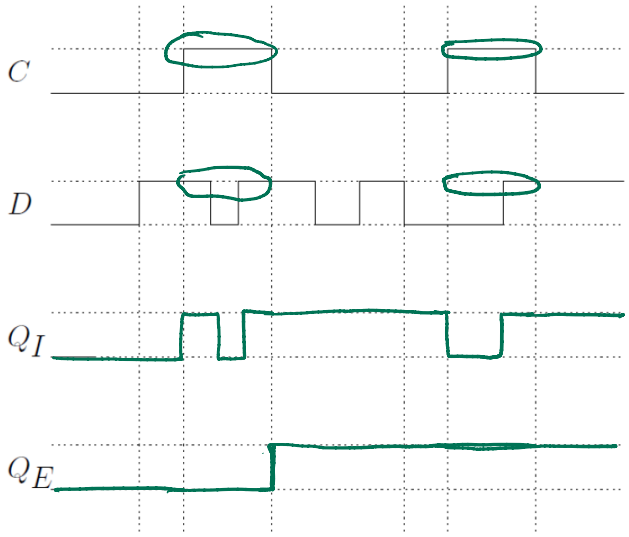
Note: You must complete the assignments entirely on your own, without discussing with others.

1. (8 Points) Consider the D flip-flop illustrated in the diagram below:



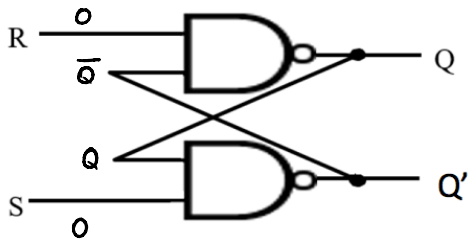
In the Figure below are traces of C and D; draw the resulting traces of QI and QE.



2. In class, we designed an SR-latch using NOR gates. Suppose instead we try to implement it using NAND gates as given below:

NAND:

A	B	O
0	0	1
0	1	1
1	0	1
1	1	0



R	S	Q	$\overline{Q}$	
0	0	1	1	undefined
0	1	1	0	set state
1	0	0	1	reset state
1	1	Q'	Q	

(a) (4 Points) What setting of R and S sets Q to 1 and Q' to 0?

R = 0 S = 1

(b) (4 Points) What setting of R and S sets Q to 0 and Q' to 1?

R = 1 S = 0

(c) (4 Points) What setting of R and S sets Q to Q and Q' to Q'?

R = 1 S = 1

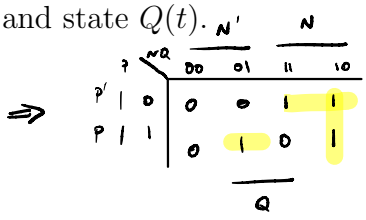
3. A PN flip-flop has four operations: 0(reset), 1(set), no change (output remains unchanged) and toggle (output changes to its complement), when inputs P and N are 00, 01, 10, 11, respectively.

(a) (4 Points) If we use $Q(t)$ to represent the output of a PN flip-flop at time t, fill in the following table:

P	N	$Q(t+1)$
0	0	0
0	1	1
1	0	$Q(t)$
1	1	$Q'(t)$

(b) (4 Points) Write the expression for $Q(t+1)$ in terms of present input (P and N) and state $Q(t)$.

P	N	Q(t)	Q(t+1)
0	0	0	0
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0
1	1	0	1
1	0	1	1
1	1	1	0



$Q(t+1) = N'Q(t)P + NP' + NQ'(t)$

(c) (8 Points) Show the state transition table and state diagram of a PN flip-flop with input($P \in \{0,1\}$ and $N \in \{0,1\}$), output ($z = Q(t)$) and state ($Q(t) \in 0,1$).

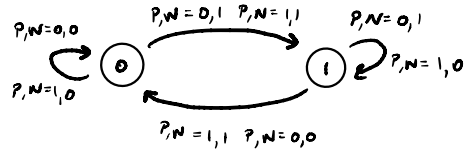
Q(t)	Q(t+1)	P	N
0	0	x	0
0	1	x	1
1	0	x	x
1	1	x	x

$0 = NP' + N \Rightarrow N=0 \quad P=x$

$1 = NP' + N \Rightarrow N=1 \quad P=x$

$0 = N'P + NP' \Rightarrow N=x \quad P=x$

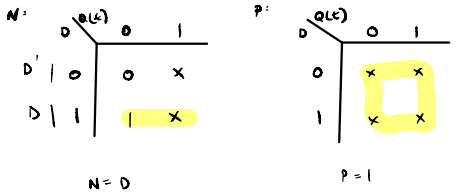
$1 = N'P + NP' \Rightarrow N=x \quad P=x$



(d) (4 Points) Show how a PN flip-flop can be converted to a D flip-flop.

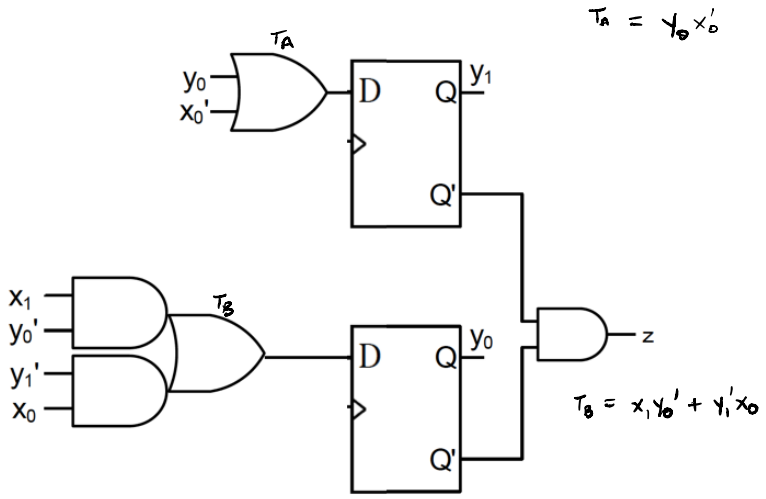
D-flip flop $\Rightarrow$

D	Q(t)	Q(t+1)	P	N
0	0	0	x	0
1	0	1	x	1
0	1	0	x	x
1	1	1	x	x



PN-flip flop can be converted to a D-flip flop with N=D, P=1

4. We would like to analyze the following sequential network. It has two input bits x_1 and x_0, with a single output bit z. Note, both D Flip-flops connect to the same CLK, not shown in the figure for simplicity.



(a) (4 Points) Write expressions for z, $y_1(t+1)$ and $y_0(t+1)$ in terms of inputs (x_1 and x_0) and present states (y_1 and y_0).

$Y_0(t+1) = T_B$

$= x_1 y_0' + x_0 y_1'$

$z = y_0' y_1'$

$Y_1(t+1) = T_A$

$= x_0' + y_0'$

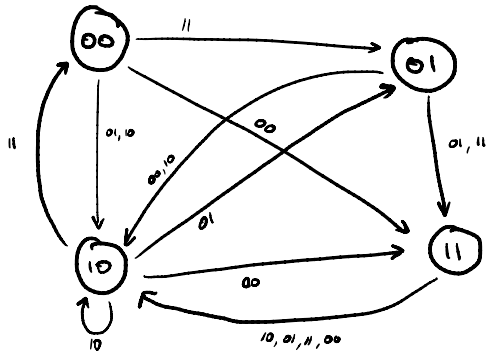
(b) (4 Points) Using the expressions, fill in the table below.

PS	Input $x_1(t)x_0(t)$				Output
$y_1(t)y_0(t)$	00	01	10	11	z
00	10	01	11	01	1
01	10	11	10	11	0
10	10	00	11	01	0
11	10	10	10	10	0
	$y_1(t+1)y_0(t+1)$				
	NS				

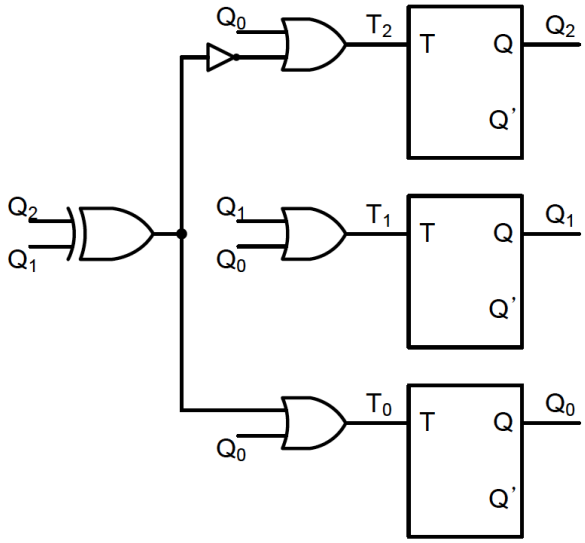
(c) (4 Points) Is this a Moore or Mealy machine?

Moore Machine — output of machine depends on only present state

(d) (4 Points) Draw the state diagram for this system



5. We would like to analyze the sequential system shown below. It is a autonomous counter which outputs a fixed string of numbers. The system does not have any input and the output changes at every clock cycle.



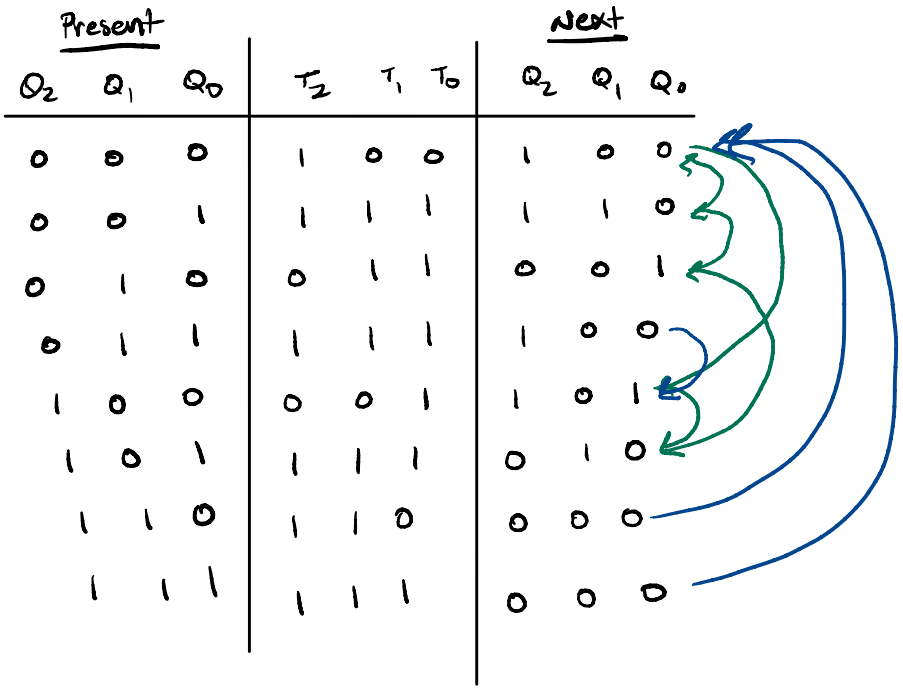
a) (6 Points) Write the expressions for T2, T1, and T0.

$T_0 = Q_1 Q_2 + Q_1' Q_2' + Q_0$

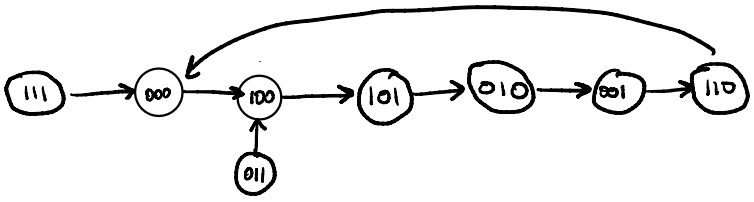
$T_1 = Q_1 + Q_0$

$T_2 = Q_1' Q_2 + Q_1 Q_2' + Q_0$

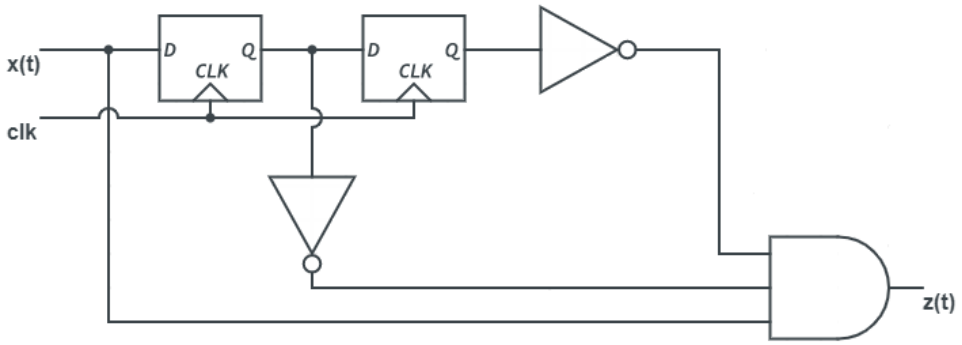
b) (6 points) Show the state transition table for the system, indicating the next states for each present state.



c) (4 points) Draw the state transition diagram of the system.



6. The following sequential system implements a pattern detector.



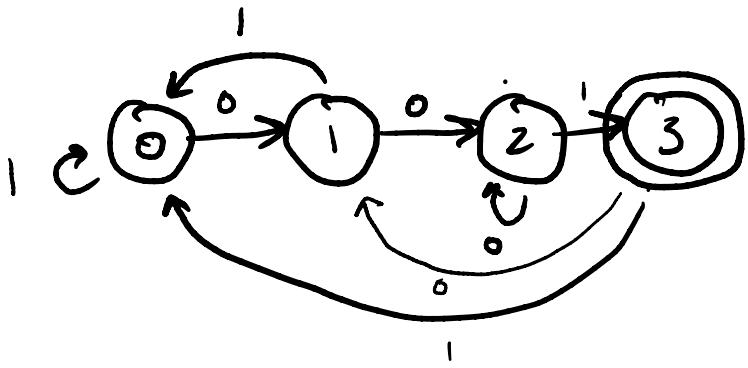
(4 Points) What pattern does this system detect?

Since the two D-flip flops have inverters appended at the end of it, for z(t) = 1, Q was to equal 0 (inverted to 1) and x(t) = 1

Therefore the pattern this system detects is 001.

7. Using D flip-flops, design a sequential system with one binary input $x(t)$ and one binary output $z(t)$. The output is 1 whenever pattern 001 are observed; otherwise the output is 0.

a) (4 Points) Draw the state diagram for this system

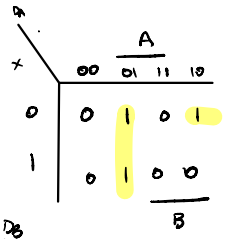


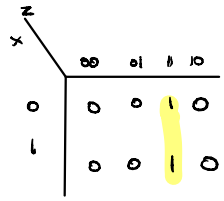
b) (4 Points) Draw the state transition table

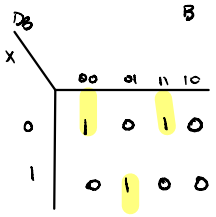
	PS	Inputs x=0	Inputs x=1	output
S_0	00	01	00	0
S_1	01	10	00	0
S_2	10	10	11	0
S_3	11	01	00	1

c) (4 Points) Draw the K-maps for each D (input of D flip-flops) and output z

PS	Input	NS	D_A	D_B	Z
00	0	01	0	1	0
00	1	00	0	0	
01	0	10	1	0	0
01	1	00	0	0	
10	0	10	1	0	0
10	1	11	1	1	
11	0	01	0	1	1
11	1	00	0	0	







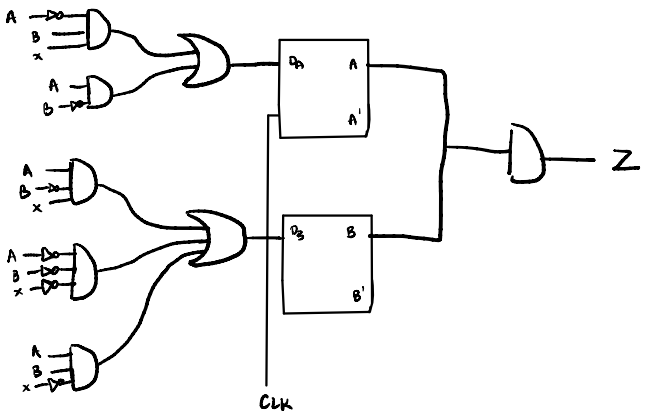
d) (4 Points) Write switching expressions for each D (input of D flip-flops) and output z

$D_A = A'Bx + AB'$

$D_B = AB'x + A'B'x' + ABx'$

$Z = AB$

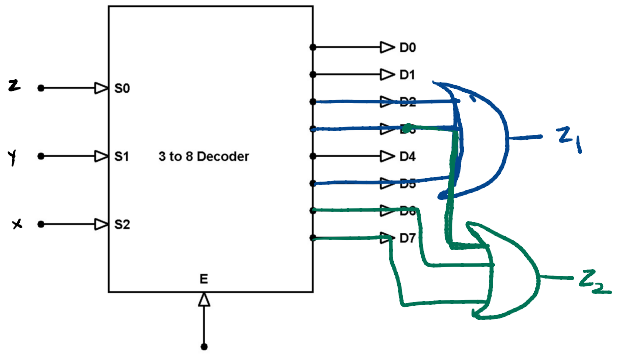
e) (4 Points) Draw your gate-level design (using gates and D flip-flops)



8. (4 Points) Using the following decoder, AND and OR Gates, implement the following function. Please show which decoder's input must be connected to x, y and z.

   z_1 = xy'z+x'yz'+x'yz
   z_2 = xyz+xyz'+x'yz

	S_2 x	S_1 y	S_0 z		
D_0	0	0	0	x'y'z'	
D_1	0	0	1	x'y'z	
D_2	0	1	0	x'yz'	z_1
D_3	0	1	1	x'yz	z_1, z_2
D_4	1	0	0	xy'z'	
D_5	1	0	1	xy'z	z_1
D_6	1	1	0	xyz'	z_2
D_7	1	1	1	xyz	z_2



$$z_1 = D_2 + D_3 + D_5$$
$$= x'yz' + x'yz + xy'z$$

$$z_2 = D_3 + D_6 + D_7$$
$$= x'yz + xyz' + xyz$$