Q14

For hardware —

- 1 cycle for add
- 1 cycle to shift w/ mults (simultaneous)
- 1 cycle to check and finish

$\Rightarrow 8 \cdot 3 \cdot 4 = 96$ time units

For software —

- 2 cycle for add (determine instruction and execute add)
- 2 cycle to shift w/ mults
- 1 cycle to check and finish

$\Rightarrow 8 \cdot 5 \cdot 4 = 160$ time units

Hardware — 96 time units

Software — 160 time units

Q15

if 32 bits require 31 adders needed to perform a multiply $\Rightarrow$ 8 bits wide $\Rightarrow$ 7 adders needed

4 time units for each adder $\Rightarrow$ $7 \cdot 4 =$ 28 time units

Q16

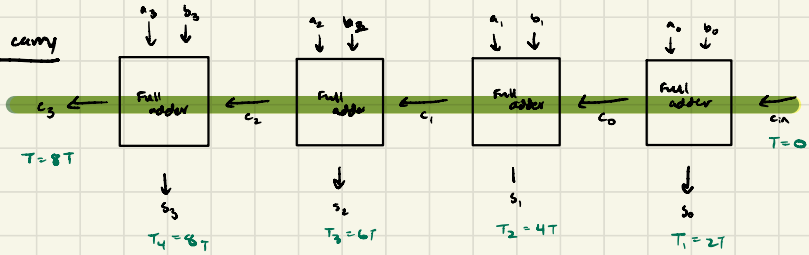
Tree structure diagram $\Rightarrow$ $\log_2$(n bits wide) = levels to place adders

8 bits wide $\Rightarrow$ 7 adders in n levels

$\log_2(8) = 3 \Rightarrow 3 \cdot 4 =$ 12 time units to perform multiply in 3 levels w/ 7 adders

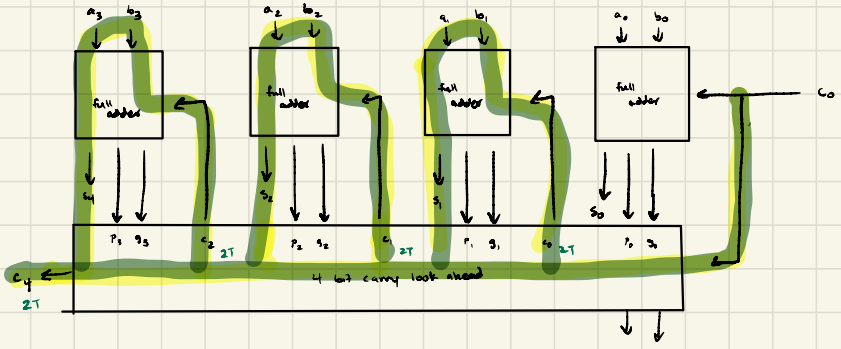
B28

Ripple carry



4 bit carry · 2T for each adder = 8T for 4 bit ripple carry adder

carry lookahead



Each computation is done in 2T because computed in parallel ⇒ 2T for carry lookahead

$$CLA = \frac{RC}{4}$$

B29

16 bit ripple carry ⇒ 2T for each 1 bit adder ⇒ 16 · 2T = 32T to compute ripple carry

4 4bit groups for carry look ahead ⇒ 2T for each 4 bit carry lookahead as shown in B.28 ⇒ 2T · 4 = 8T for carry lookahead

$$CLA = \frac{RC}{4}$$

B30

64 bit adder using 4 bit groups ⇒ 16 bit adder w/ 1 bit groups ⇒ 32T for ripple carry from B.29

16 bit groups use CLA using 4 bit groups ⇒ 2T for each 4 bit CLA ⇒ 2T · 4 = 8T for carry look ahead

$$CLA = \frac{RC}{4}$$