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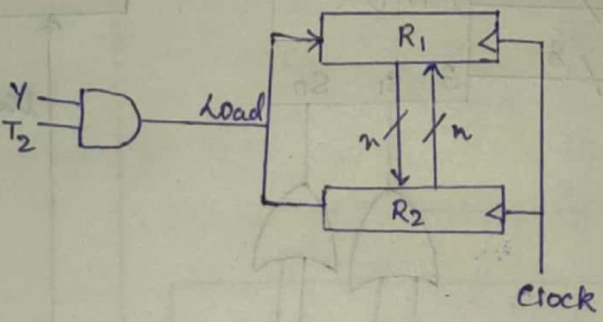
CHAPTER:
REGISTER TRANSFER AND MICROOPERATIONS:

(1) Show the block diagram of the hardware that implements the following register transfer statements:

$$YT_2 : R_2 \leftarrow R1 \;,\; R1 \leftarrow R2$$

Soln



(2) The outputs of four registers, R0, R1, R2, R3, are connected through 4-to-1-line multiplexers to the inputs of a fifth register, R5. Each register is 8 bits long. The required transfers are dictated by 4 timing variables T_0 through T_3 as follows:

T_0 : $R_5 \leftarrow R0$

T_1 : $R5 \leftarrow R1$

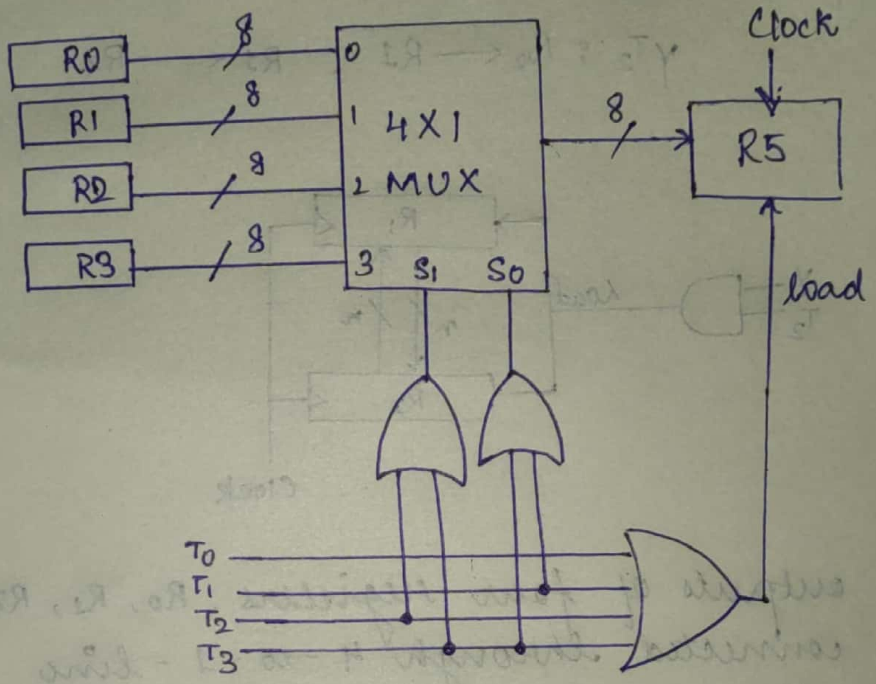
T_2: $R5 \leftarrow R2$

T_3: $R5 \leftarrow R3$.

The timing variables are mutually exclusive. which means only one variable is equal to 1 at any given time, while the other three are equal to 0. Draw a block diagram showing hardware implementation of the register transfers. Include the connections necessary from the four timing variables to the selection inputs of the multiplexers and the load input of register R5.

Solu

Hardware implementation:



$S_1 = T_2 + T_3$

$S_0 = T_1 + T_3$

$load = T_0 + T_1 + T_2 + T_3$.

T_0	T_1	T_2	T_3	S_1	S_0	Load
0	0	0	0	X	X	0
1	0	0	0	0	0	1
0	1	0	0	0	1	1
0	0	1	0	1	0	1
0	0	0	1	1	1	1

(3) Represent the following conditional statement by two register transfer statement with control functions.

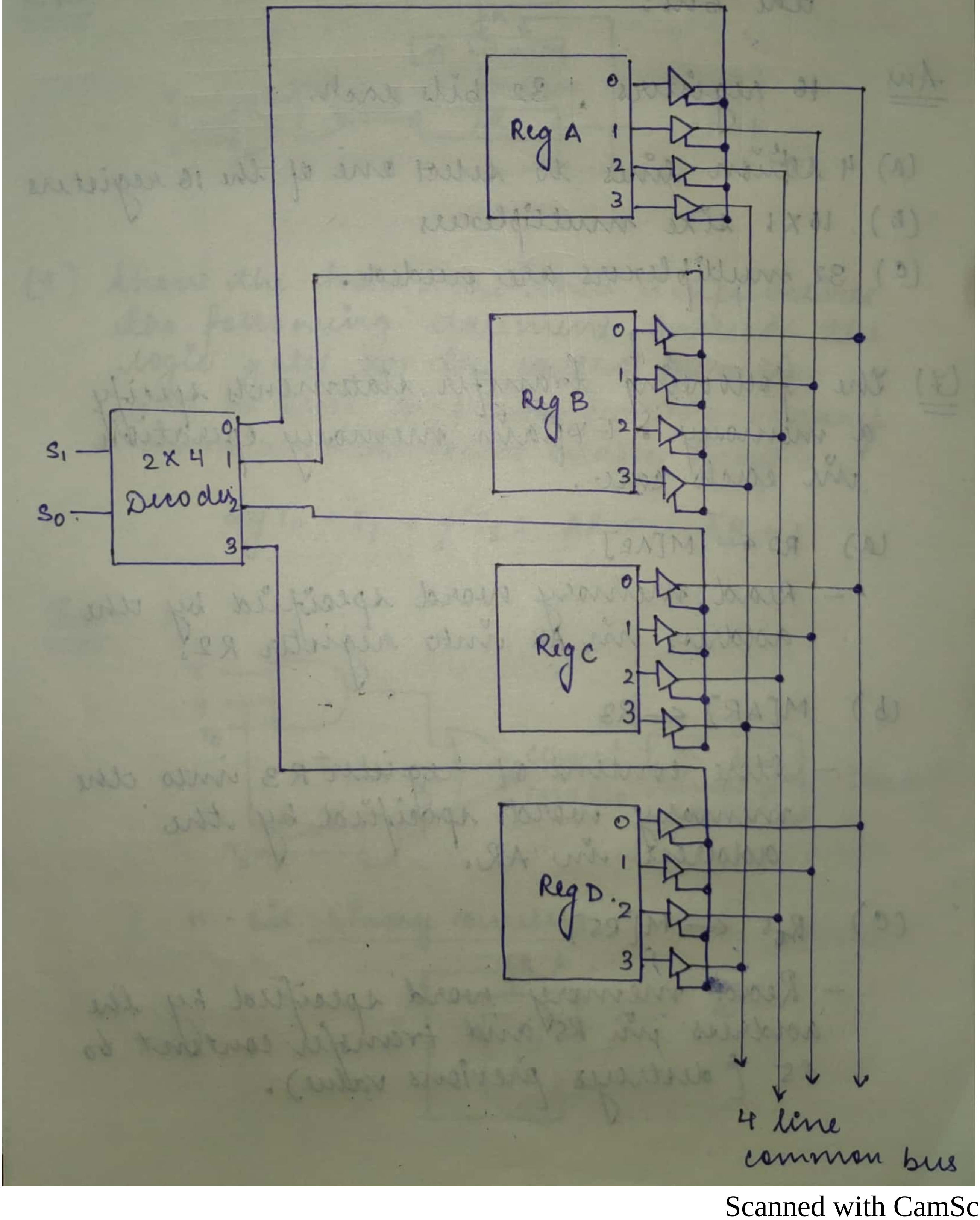
If (P = 0) then (R1 ← R2) else if (Q=1) then (R1 ← R3)

Soln

P : R1 ← R2

P'Q : R1 ← R3.

(5) Draw a diagram of a bus system similar to the one shown but use three state buffers and a decoder instead of a multiplexer.



(6) A digital computer has a common bus system for 16 registers of 32 bits each. The bus is constructed with multiplexers.

(a) How many selection inputs are there in each multiplexers?

(b) What size of multiplexers are needed?

(c) How many multiplexers are there in the bus?

Ans 16 registers, 32 bits each.

(a) 4 selection lines to select one of the 16 registers

(b) 16 X 1 size multiplexers

(c) 32 multiplexers are needed.

(7) The following transfer statements specify a memory. Explain memory operation in each case.

(a) R2 ← M[AR]

- Read memory word specified by the address in AR into register R2.

(b) M[AR] ← R3

- Store content of register R3 into the memory word specified by the address in AR.

(c) R5 ← M[R5]

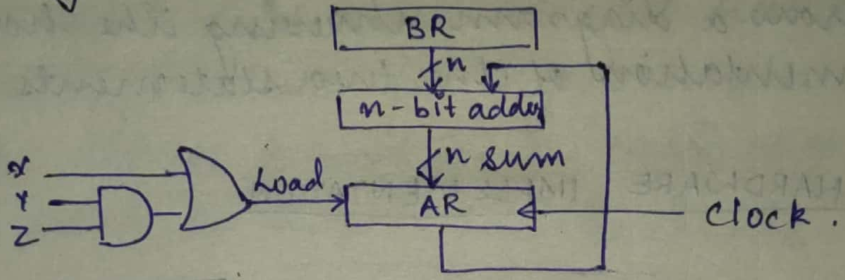
- Read memory word specified by the address in R5 and transfer content to R5 (destroys previous value).

(8) Draw a block diagram for the hardware that implements the following statements:

$x + yz : AR \leftarrow AR + BR$.

where AR and BR are two n-bit registers and x, y, z are control variables. Include the logic gates for control function.

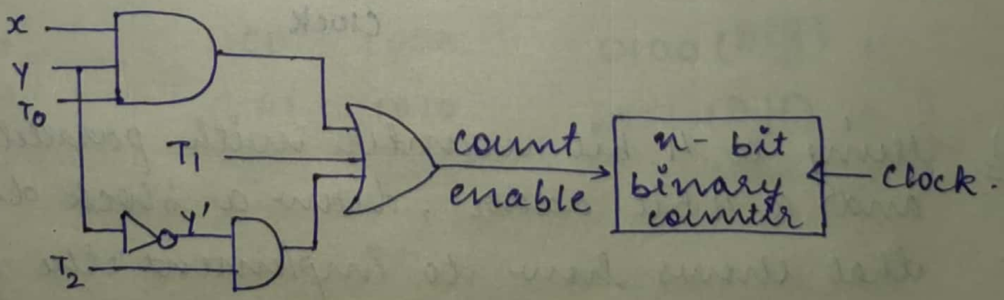
Soln



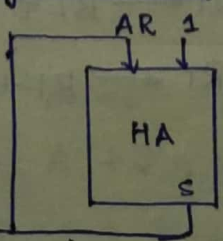
(9) Show the hardware that implements the following statement. Include the logic gates for the control function and a block diagram for the binary counter with count enable input.

$xyT_0 + T_1 + y'T_2 : AR \leftarrow AR + 1$

Soln



n-bit binary counter:



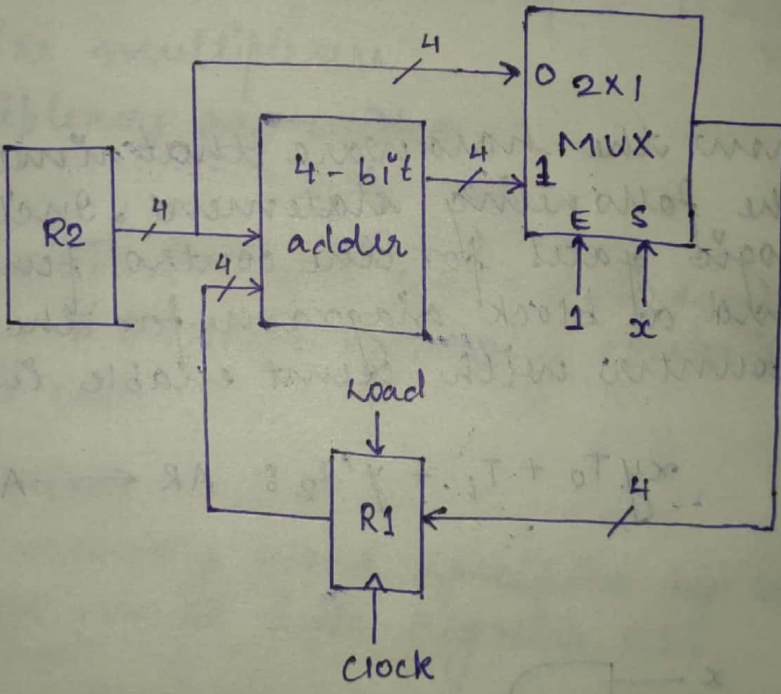
(10) consider the following register transfer statement for two 4-bit register R1 & R2.

$xT : R1 \leftarrow R1 + R2$

$x'T : R1 \leftarrow R2$

Every time that variable T=1, either the content of R2 is added to the content of R1 if x=1, or the content of R2 is transferred to R1 if x=0. Draw a diagram showing the hardware implementation of the two statements.

Soln HARDWARE IMPLEMENTATION

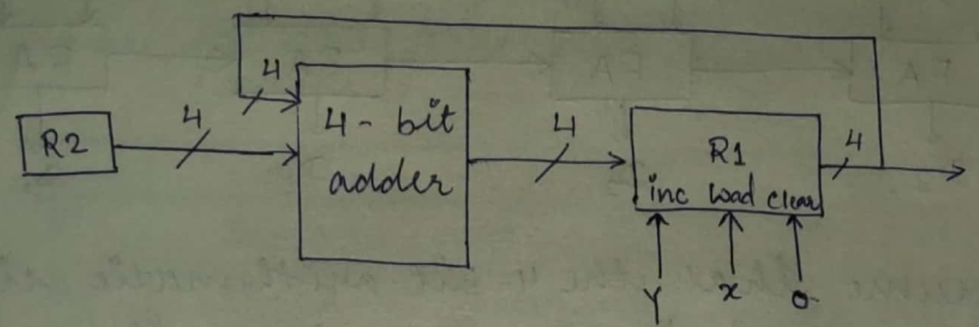


(11) Using a 4 bit counter with parallel load and a 4 bit adder, draw a block diagram that shows how to implement the following statements:

$x : R1 \leftarrow R1 + R2$ Add R2 to R1

$x'y : R1 \leftarrow R1 + 1$ Increment R1

Soln



(12) The adder - subtractor circuit has the following values for input modes M and data inputs A and B. In each case, determin the value of outputs : S_3, S_2, S_1, S_0 & C_4.

	M	A	B
a.	0	0111	0110
b.	0	1000	1001
c.	1	1100	1000
d.	1	0101	1010
e.	1	0000	0001

Soln

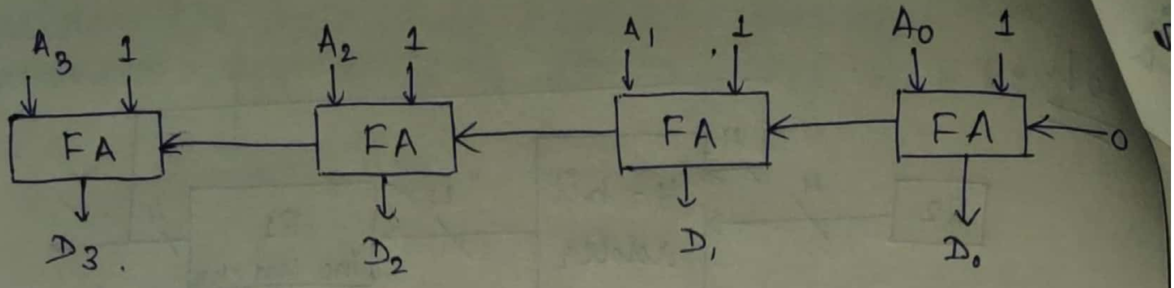
	M	A	B	Sum/Diff	Carry
a.	0	0111	0110	1101 (Sum)	0
b.	0	1000	1001	0001 (Sum)	1
c.	1	1100	1000	0100 (Diff)	1
d.	1	0101	1010	1011 (Diff)	0 } 2's C
e.	1	0000	0001	1111 (Diff)	0

(13) Design a 4-bit combinational circuit decrementer using four full-adder circuits.

Soln Decrementer = A - 1

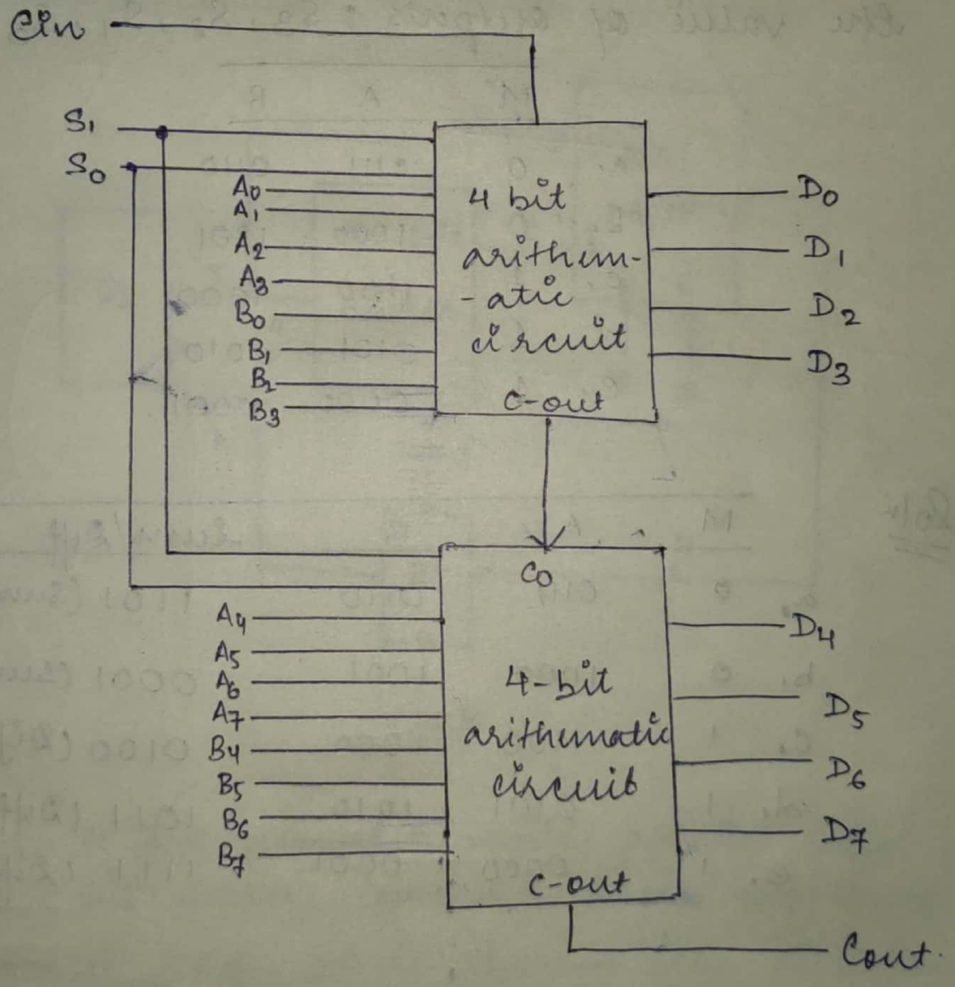
= A + 2's complement of 1

= A + 1111



(14) Assume that the 4-bit arithmatic circuit is enclosed in one IC package. Show the connections among two such ICs to form an 8-bit arithematic circuit.

Soln



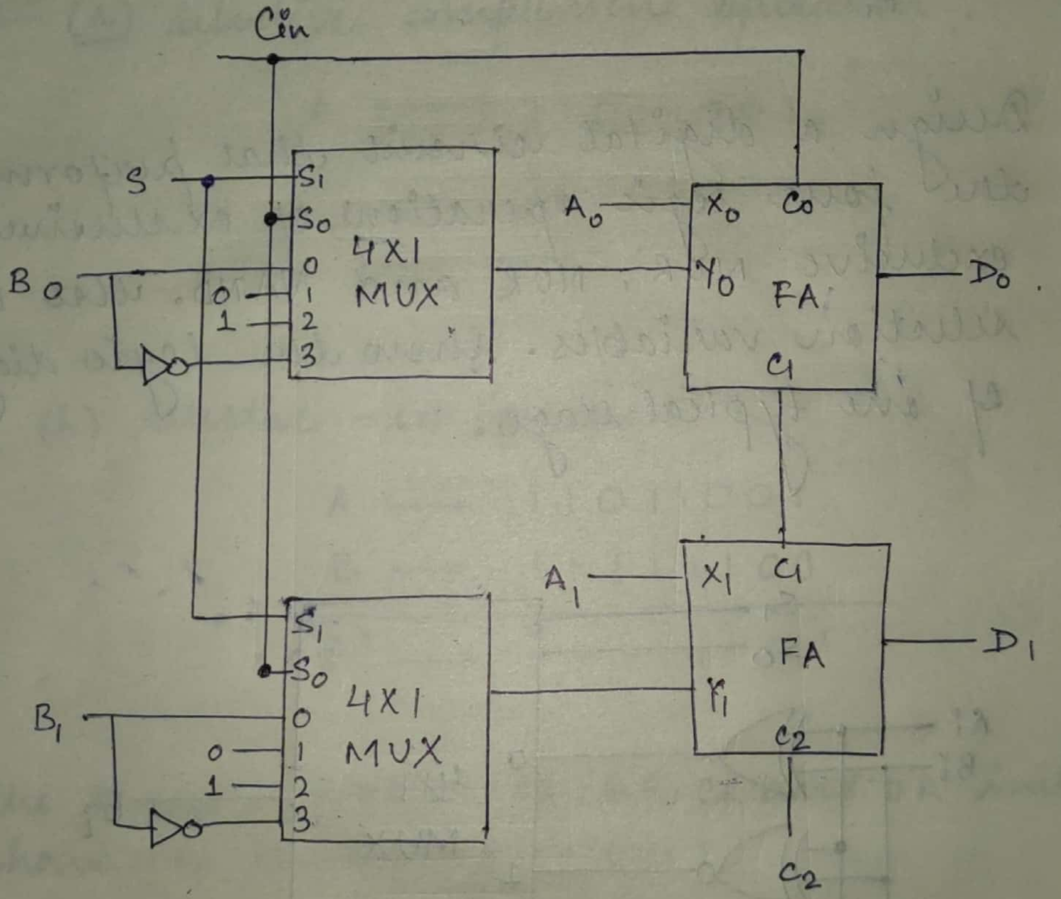
8- bit arithematic circuit

(15) Design an arithematic circuit with one selection variable s and two n-bit data inputs A and B. The circuit generates the following four arithematic operations in conjunction

with the input carry Cin. Draw the logic diagram for the first two stages.

S	Cin = 0	cin = 1
0	D = A+B (add)	D = A+1 (increment)
1	D = A-1 (decrement)	D = A+$\bar{B}$ +1 (subtrac

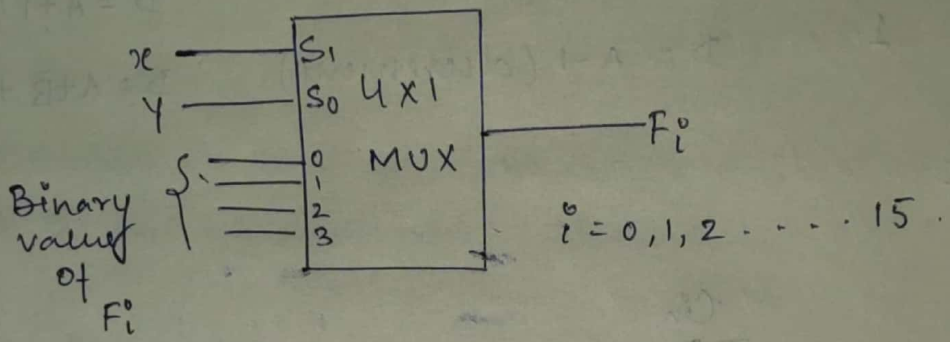
Soln



S	Cin	X	Y	
0	0	A	B	(A+B
0	1	A	0	(A+1)
1	0	A	1	(A-1)
1	1	A	$\bar{B}$	(A-B)

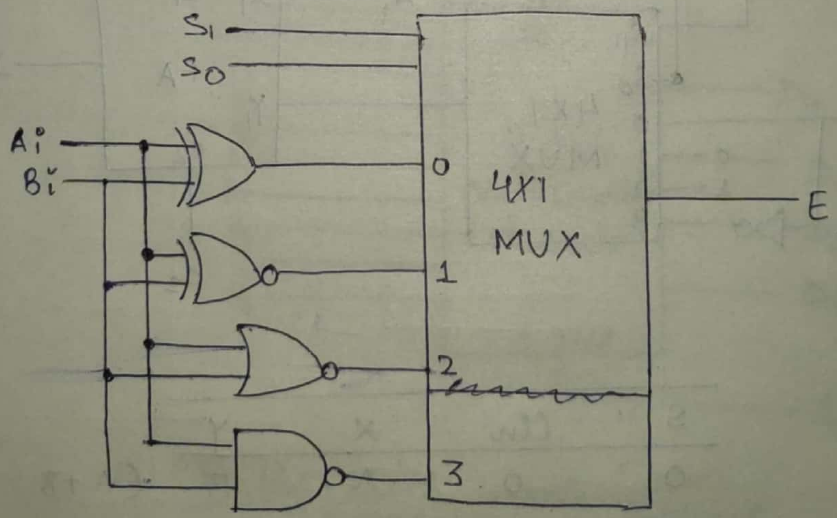
(16) Derive a combinational circuit that selects and generates any of the 16 logic functions listed in Table 5.5.

Soln



(17) Design a digital circuit that performs the four logic operations of exclusive-OR, exclusive NOR, NOR and NAND. Use two selection variables. Show the logic diagram of one typical stage.

Soln



(1

Logic circuit

(18) Register A holds the 8-bit binary 11011001. Determine the B operand and the logic microoperation to be performed in order to change the value of A to

(a) 01101101

(b) 11111101

Soln

(a) Selective complement operation.

$A \longrightarrow 11011001$

$B \longrightarrow 10110100$

$A \oplus B. \longrightarrow 01101101$

(b) Selective-set operation.

$A \longrightarrow 11011001$

$B \longrightarrow 11111100$

$A \vee B \longrightarrow 11111101$

(19) The 8-bit registers AR, BR, CR and DR initially have the following values:

AR = 11110010
BR = 11111111
CR = 10111001
DR = 11101010

Determine the 8-bit values in each register after the execution of the following sequence of microoperations

$AR \leftarrow AR + BR$ Add BR to AR

$CR \leftarrow CR \wedge DR$, $BR \leftarrow BR+1$. Add DR to CR, increment BR

$AR \leftarrow AR - CR$. Subtract CR from AR.

Soln (A) $AR \leftarrow AR + BR$

```
  11110010
+ 11111111
----------
  11110001
```

AR = 11110001 , BR = 11111111

(b) $CR \leftarrow CR \wedge DR$, $BR \leftarrow BR+1$

```
CR →      10111001          BR → 11111111
DR →      11101010                     +1
                                 --------
CR∧DR →   10101000               00000000
```

CR = 10101000

BR = 00000000

(c) $AR \leftarrow AR - CR$

```
AR →   11110001
CR →   10101000
       --------
       01001001
```

AR = 01001001

BR = 00000000

CR = 10101000

DR = 11101010

(20) An 8-bit register contains the binary value 10011100. What is the register value after an arithmatic shift right? Starting from initial number 10011100,

determine the register value after an arithematic shift left, and state whether there is an overflow.

Soln Initial number : 10011100

Arithematic shift right : 11001110

Arithematic shift left : 00111000 → overflow because a -ve number changed to +ve.

(21) Starting from an initial value of R = 11011101, determine the sequence of binary values in R after a logical shift left, followed by a circular shift right. followed by a logical shift right and a circular shift left.

Soln R = 11011101

Logical shift left : 10111010.

circular shift right : 01011101

Logical shift right : 00101110.

circular shift left : 01011100.

(22) - What is the value of output H in Fig 5.12 if input A is 1001, S = 1, $I_R = 1$ and $I_L = 0$.

Soln If S = 1,

Then shift left operation

A_0 A_1 A_2 A_3 I_L
1 0 0 1 0
↙ ↙ ↙ ↙ ↙
H = 0 0 1 0 (Shift left)

Q23 What is wrong with the following register transfer statements:

a) $xT : AR \leftarrow \overline{AR}$, $AR \leftarrow 0$.

Cannot complement and clear the same register at the same time.

(b) $yT : R1 \leftarrow R2$, $R1 \leftarrow R3$.

Cannot transfer two different values ~~[illegible]~~ (R2 & R3) to the same register (R1) at the same time

(c) $xT : PC \leftarrow AR$, $PC \leftarrow PC+1$

Cannot transfer a new value into a register (PC) and increment the original value by one at the same time.