



THE UNIVERSITY *of* EDINBURGH

*Analogue IC Design*

# FET Amplifiers (Part2)

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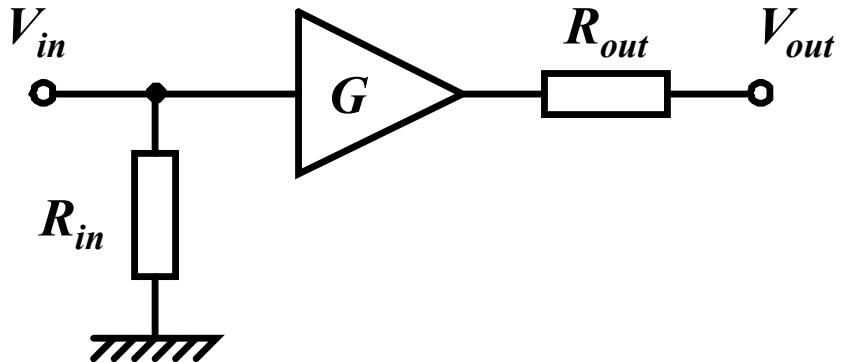
# nMOS I-V Summary

- Shockley 1st order transistor models

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ \beta \left( V_{gs} - V_t - \frac{V_{ds}}{2} \right) V_{ds} & V_{ds} < V_{dsat} \quad \text{linear} \\ \frac{\beta}{2} (V_{gs} - V_t)^2 & V_{ds} > V_{dsat} \quad \text{saturation} \end{cases}$$

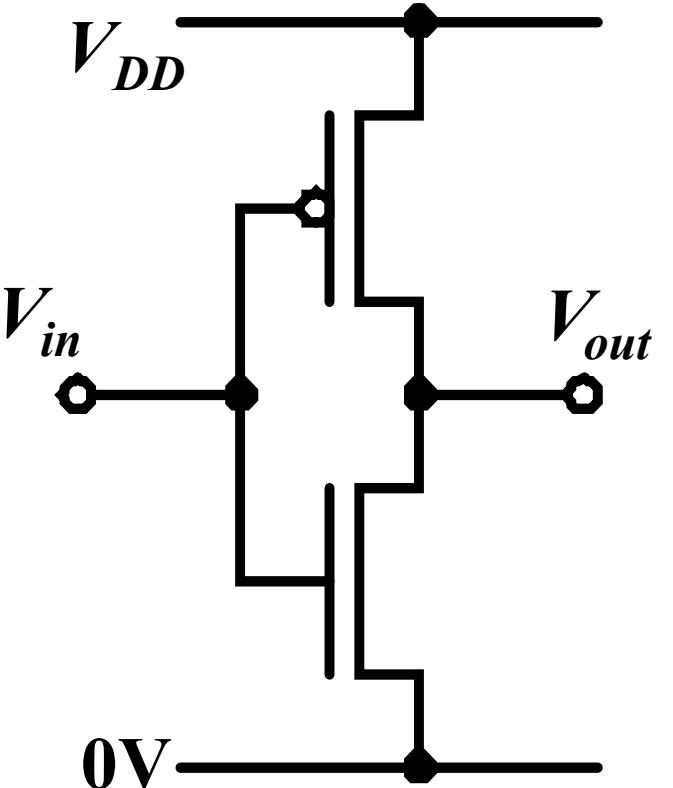
# Basic Amplifier Model

- This is one of the most useful amplifier models
- $R_{in}$  is the amplifier input impedance (usually infinite for MOS circuits)
- $R_{out}$  is the amplifier output impedance
- $G$  is the amplifier gain, usually negative
- This model, however, is incomplete when used with MOS circuits



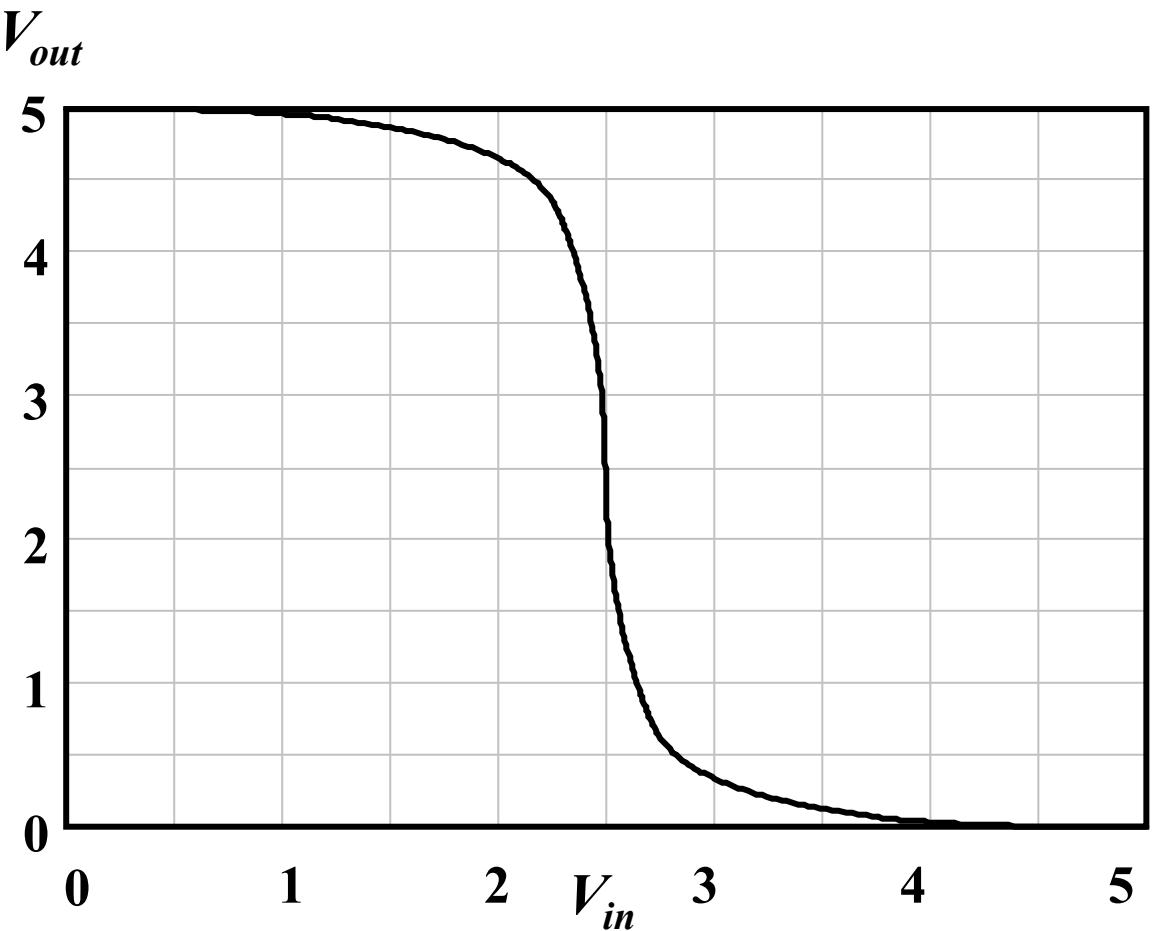
# Two Transistor (CMOS) Amplifier

- The standard CMOS inverter makes an excellent analogue amplifier
- High gain
- Not too bad for noise
- Problems
  - Correct DC bias hard to establish
  - Takes lots of DC current

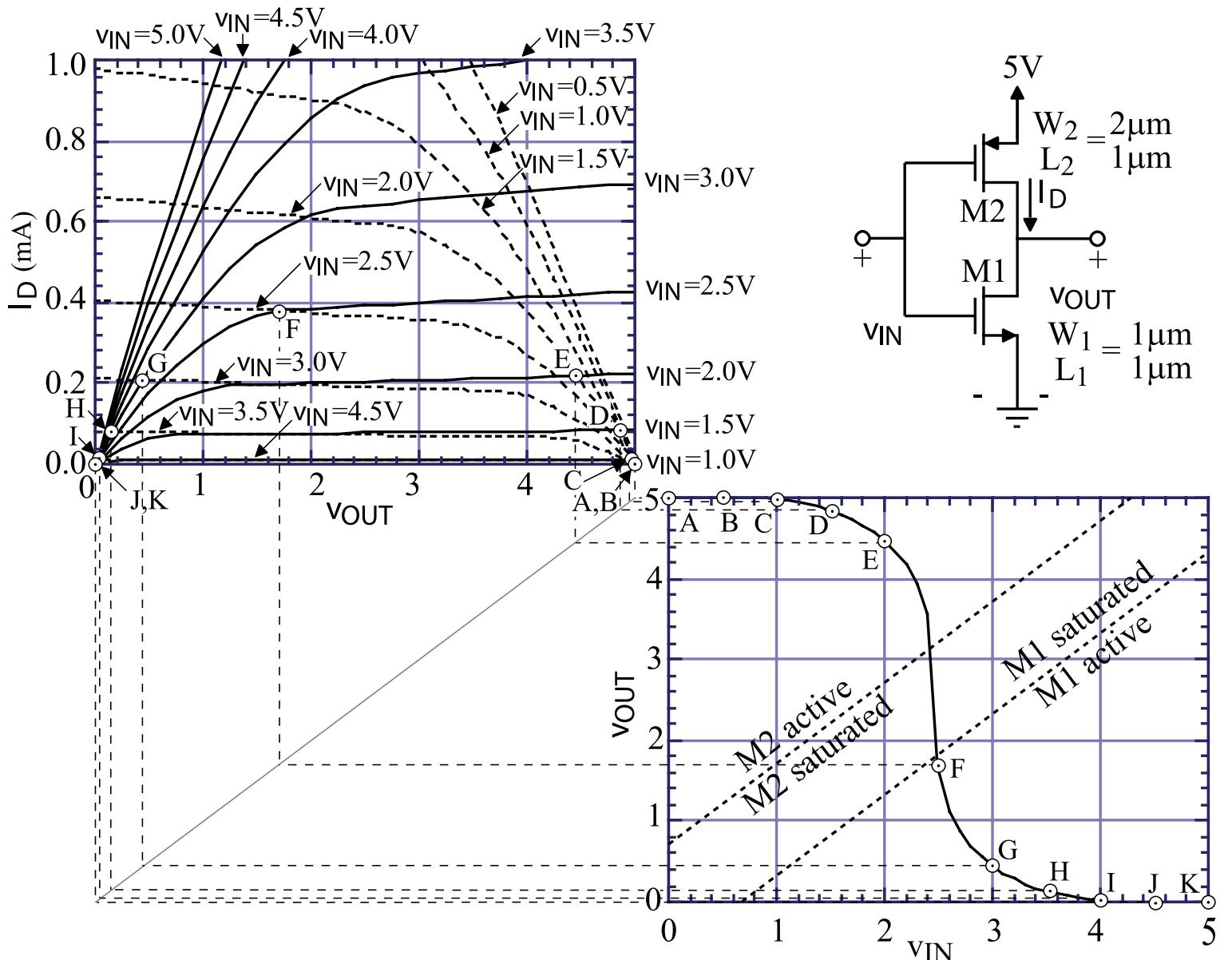


# Two Transistor (CMOS) Amplifier

- High gain region near  $V_{in} = V_{DD}/2$
- Exact bias position process dependent
- Produce DC bias voltage from identical inverter with  $V_{in}$  tied to  $V_{out}$



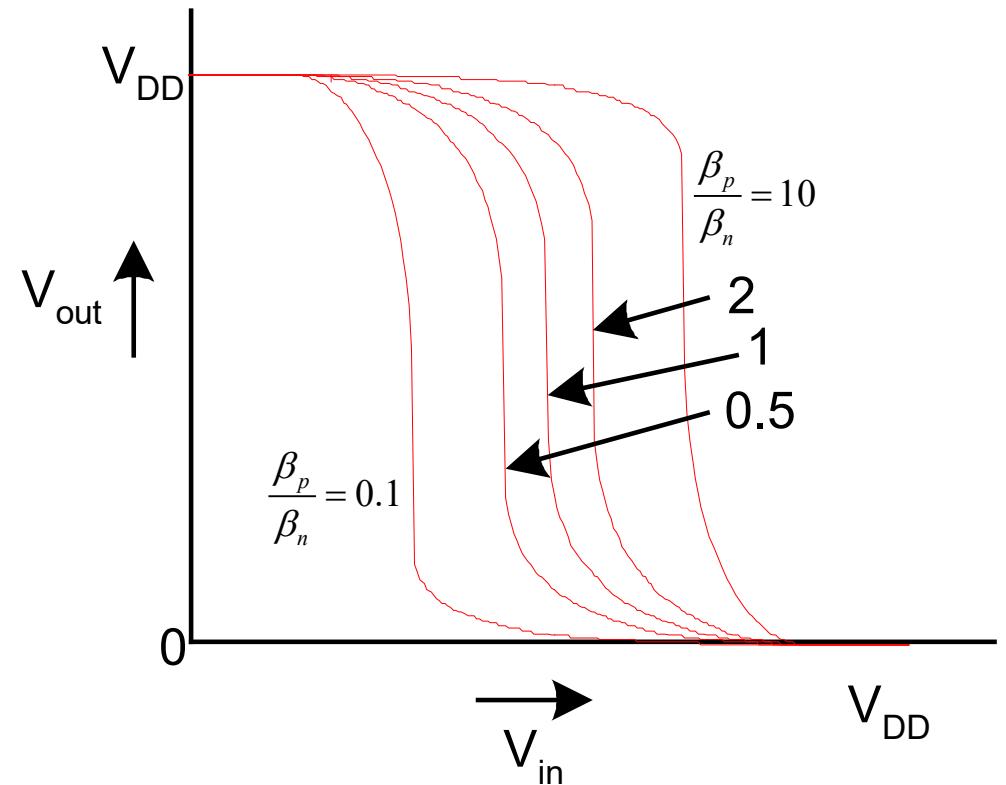
# Two Transistor (CMOS) Amplifier



# Two Transistor (CMOS) Amplifier

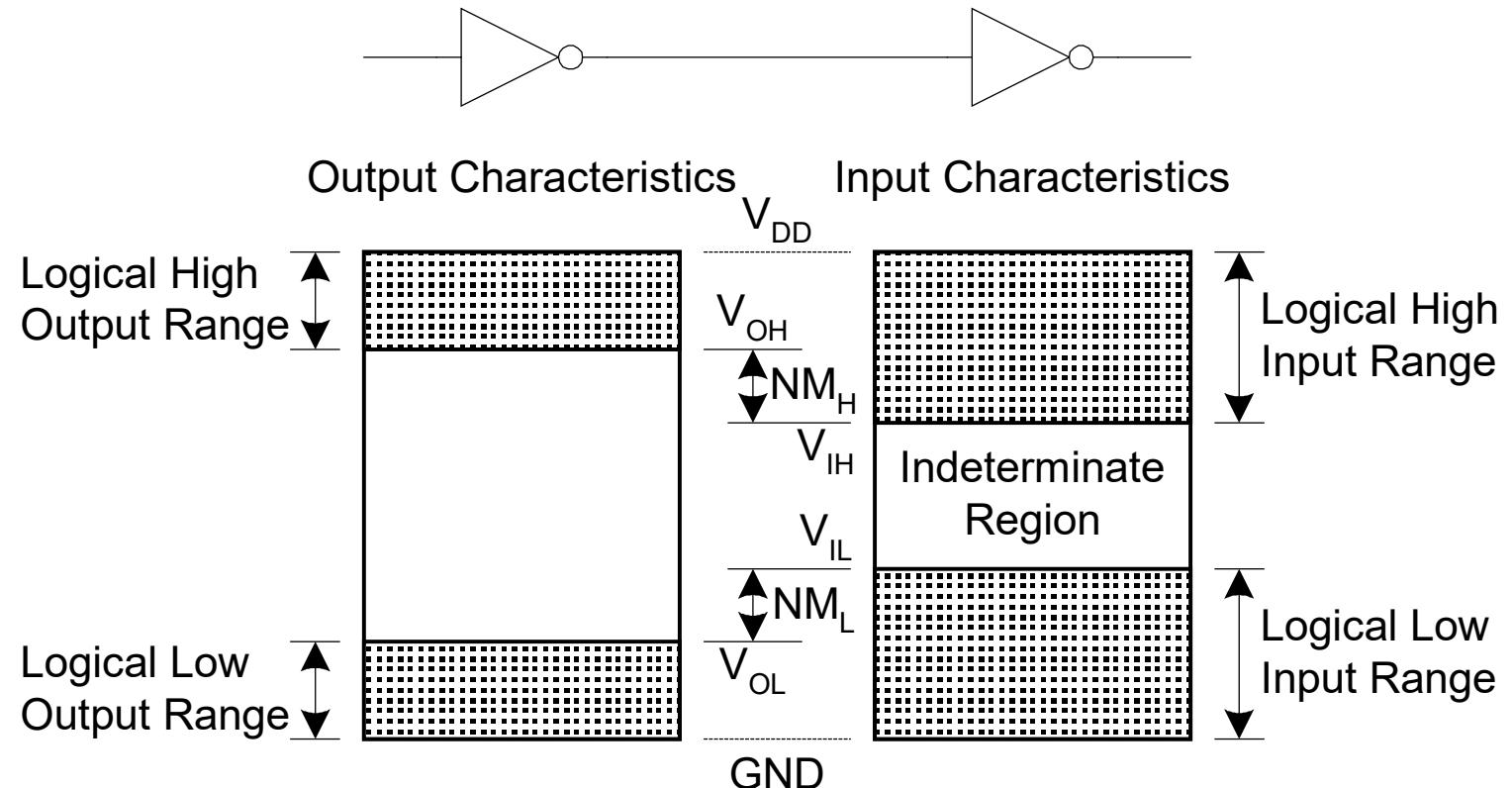
- Midpoint is  $V_M$

$$V_M = \frac{V_{DD} - V_{tp} + V_{tn} \sqrt{\frac{\beta_n}{\beta_p}}}{1 + \sqrt{\frac{\beta_n}{\beta_p}}}$$



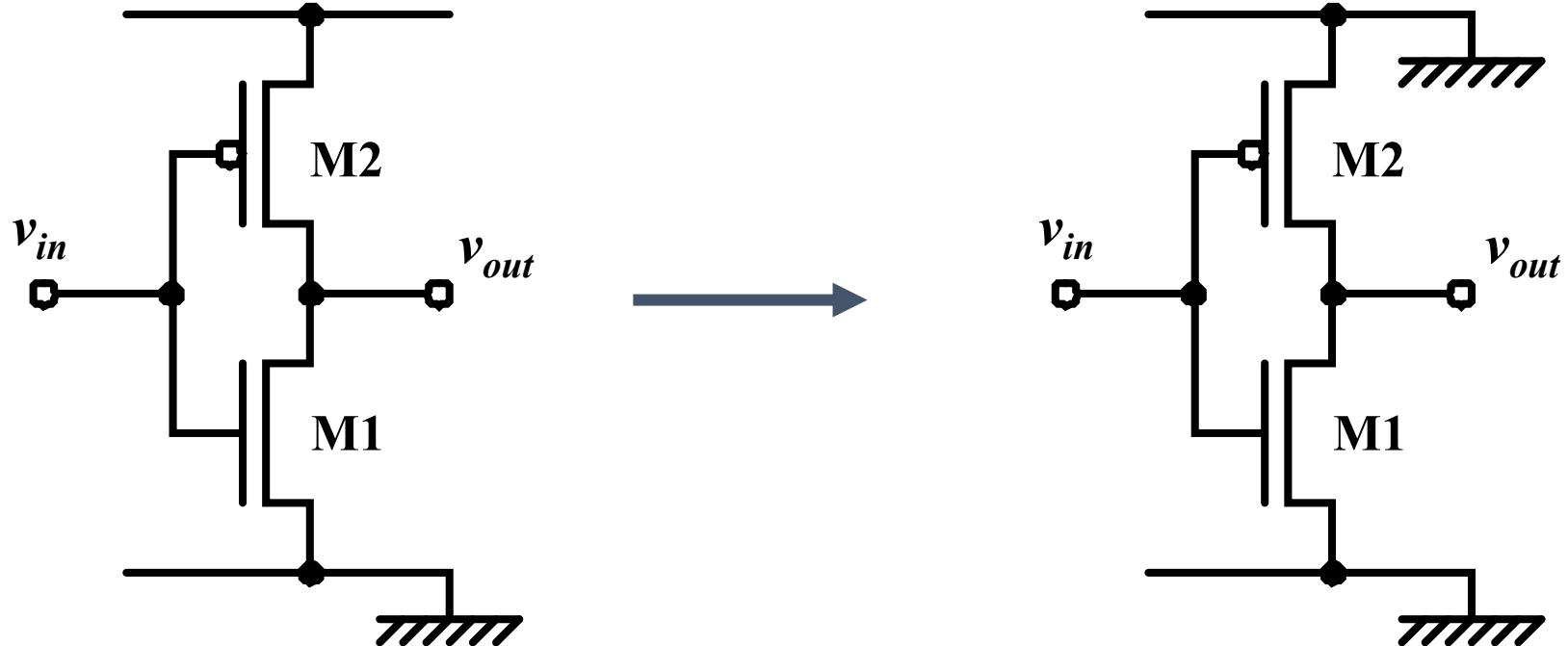
# Two Transistor (CMOS) Amplifier

- How much noise can a gate input see before it does not recognize the input?



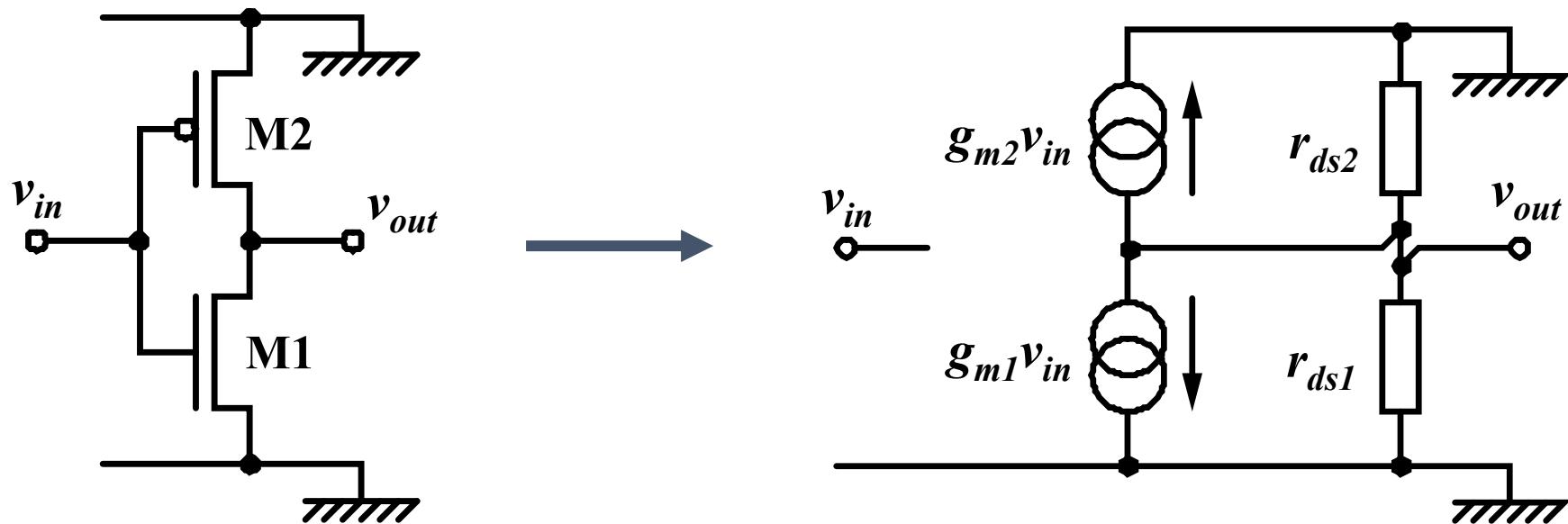
# Two Transistor (CMOS) Amplifier

- Now let us make up the small-signal model for this CMOS inverter
- First set DC voltages to zero



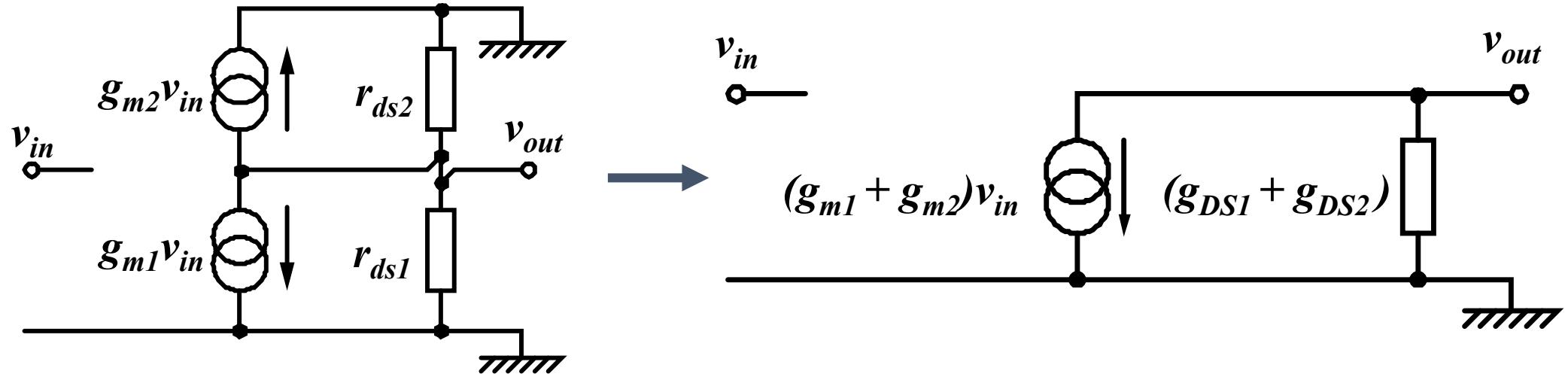
# Two Transistor (CMOS) Amplifier

- Now substitute the small-signal model for each FET
- Note that the P-channel FET arrow points *up*
- Observe how many things are in parallel here. Obvious candidates for a tidy-up.



# Two Transistor (CMOS) Amplifier

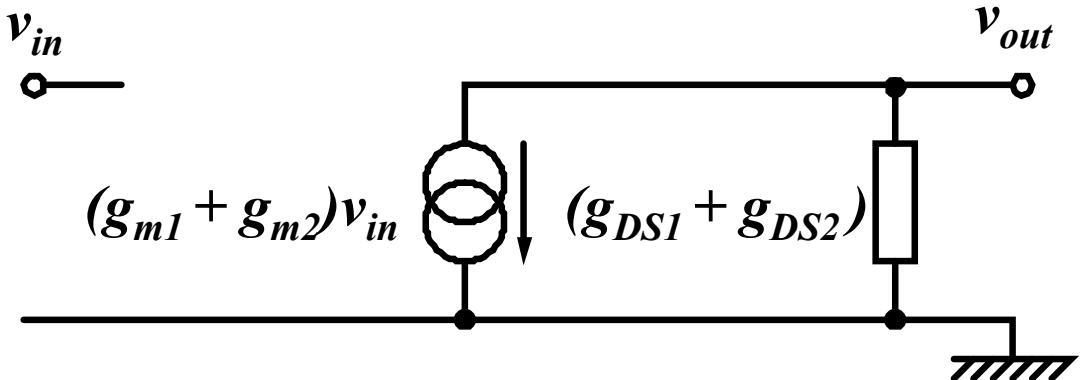
- The analysis is simple - all the current goes through the resistor so  $v_{out}$  is developed across it.
- Note that  $v_{out}$  will be *negative*



# Two Transistor (CMOS) Amplifier

- Clearly:-

$$\frac{v_{out}}{v_{in}} = - \left( \frac{g_{m1} + g_{m2}}{g_{DS1} + g_{DS2}} \right)$$



- Since  $g_m \propto \sqrt{I_{DS}}$  and  $g_{DS} \propto I_{DS}$  this gain is *inversely proportional* to  $\sqrt{I_{DS}}$
- The inverter *output impedance* is equal to  $(g_{DS1} + g_{DS2})^{-1}$

# Two Transistor (CMOS) Amplifier

- In linear region if  $V_{ds} \ll 2(V_{gs} - V_t)$

$$I_D \approx \mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH}) V_{DS}$$

- Then

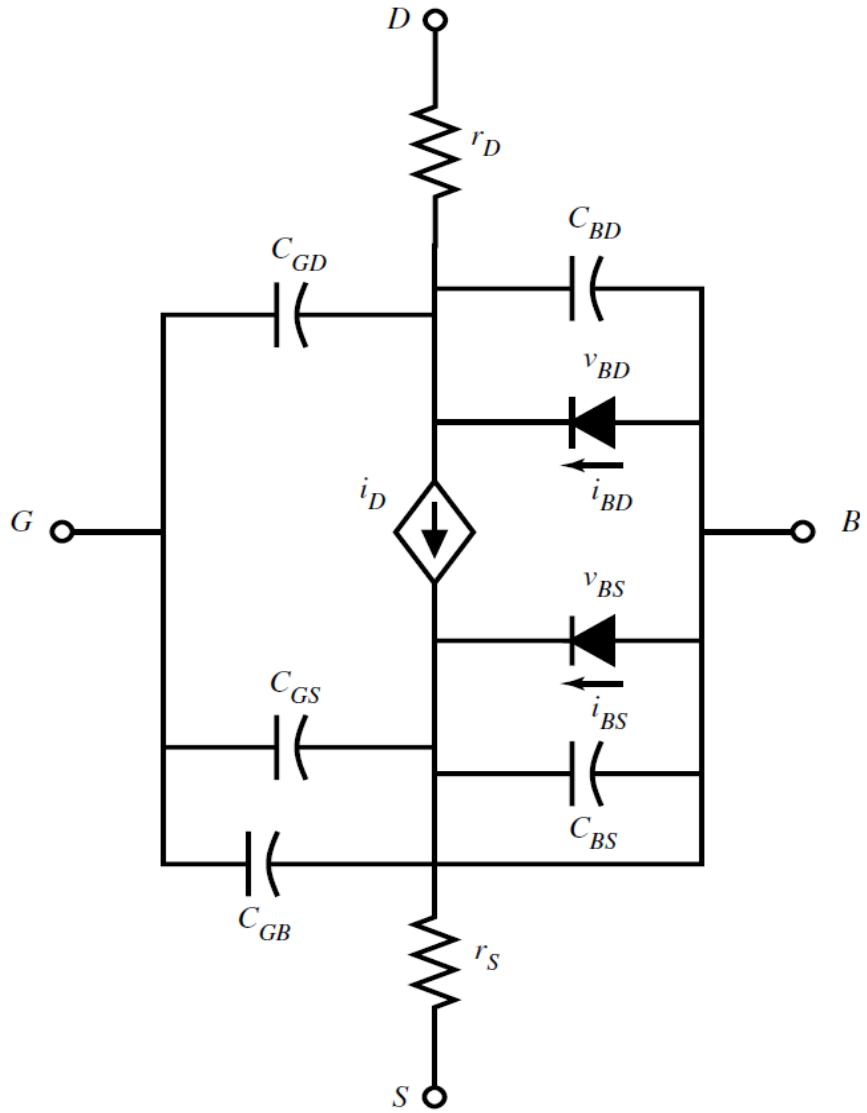
$$R_{on} = \frac{1}{\mu_n C_{ox} \frac{W}{L} (V_{GS} - V_{TH})}$$

$$R_n = \frac{1}{\beta_n (V_{DD} - V_{tn})}$$

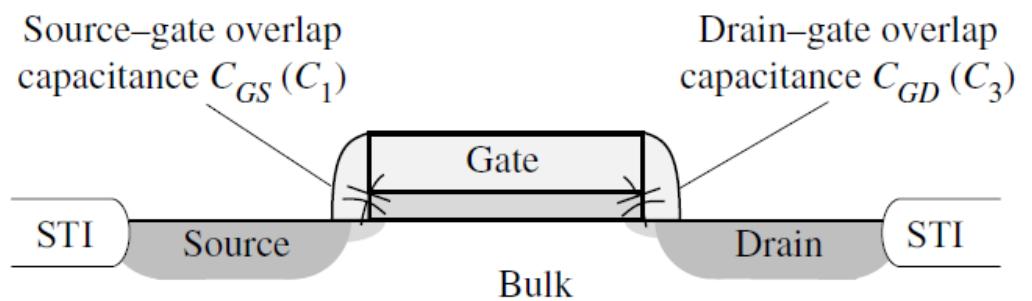
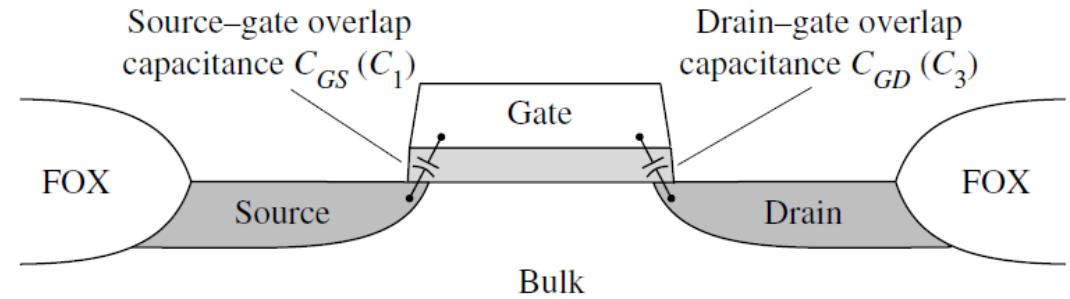
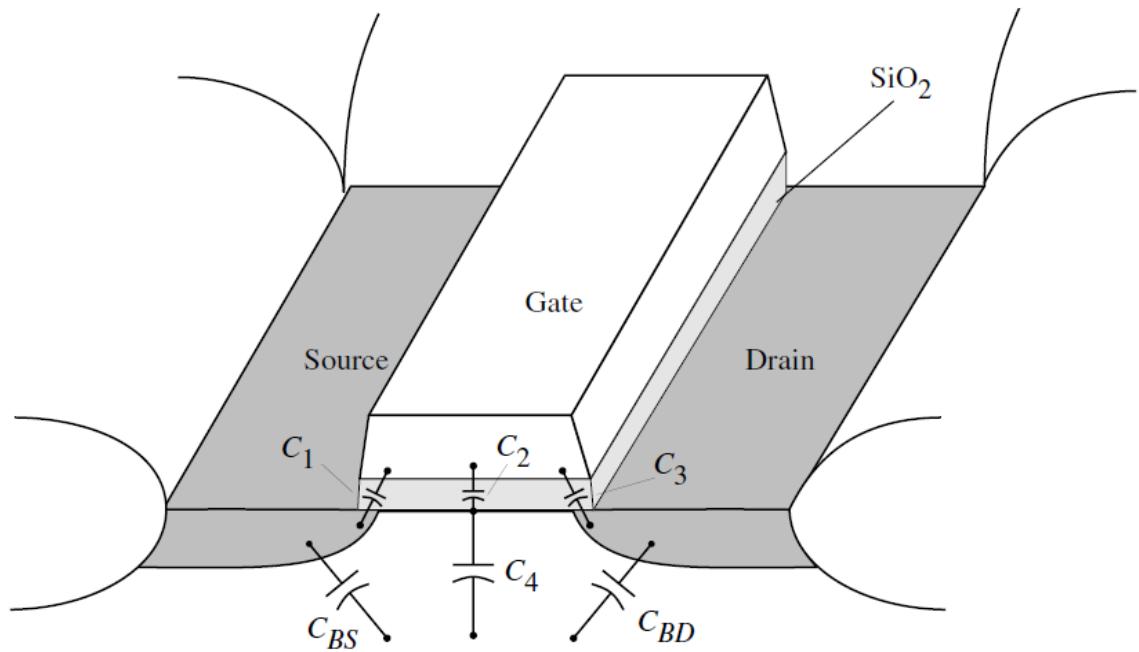
$$R_p = \frac{1}{\beta_p (V_{DD} - |V_{tp}|)}$$

# Two Transistor (CMOS) Amplifier

- Full large signal model of FET

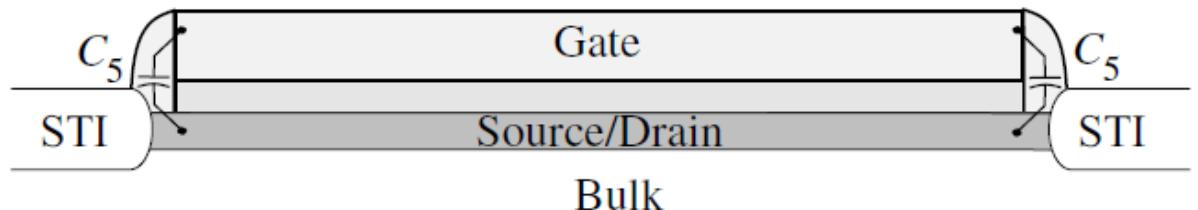
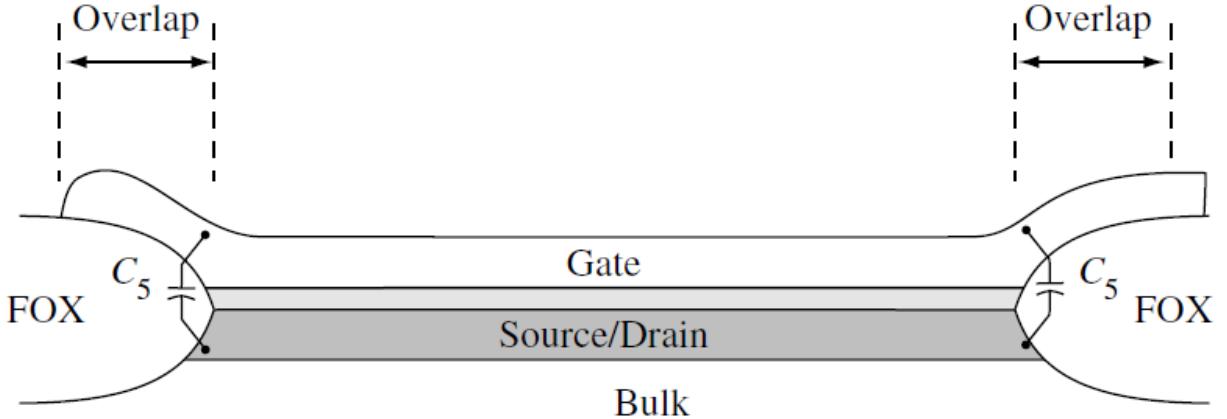


# Two Transistor (CMOS) Amplifier



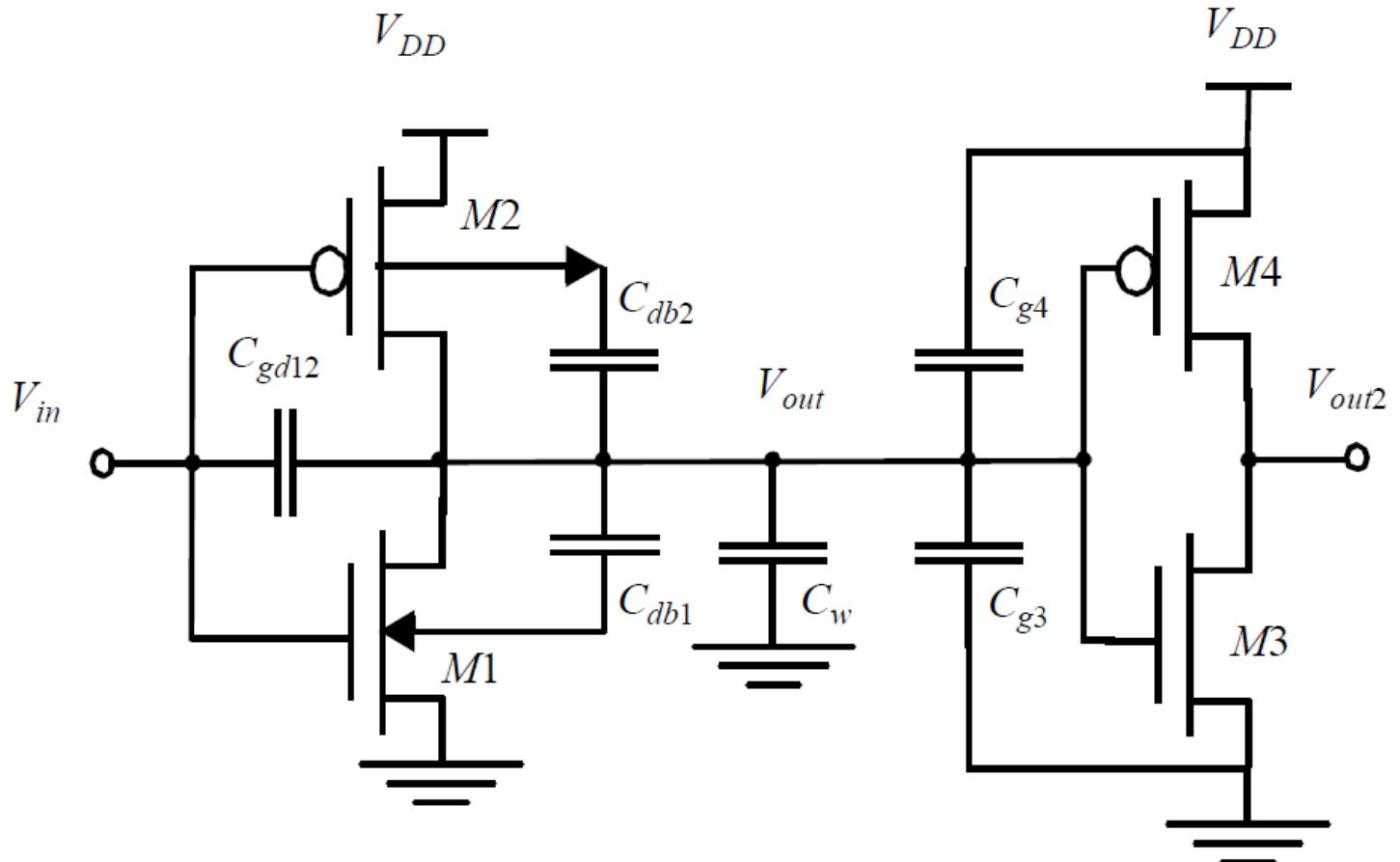
# Two Transistor (CMOS) Amplifier

$C_{GB}$



# Two Transistor (CMOS) Amplifier

- Parasitic capacitances in digital inverter circuits

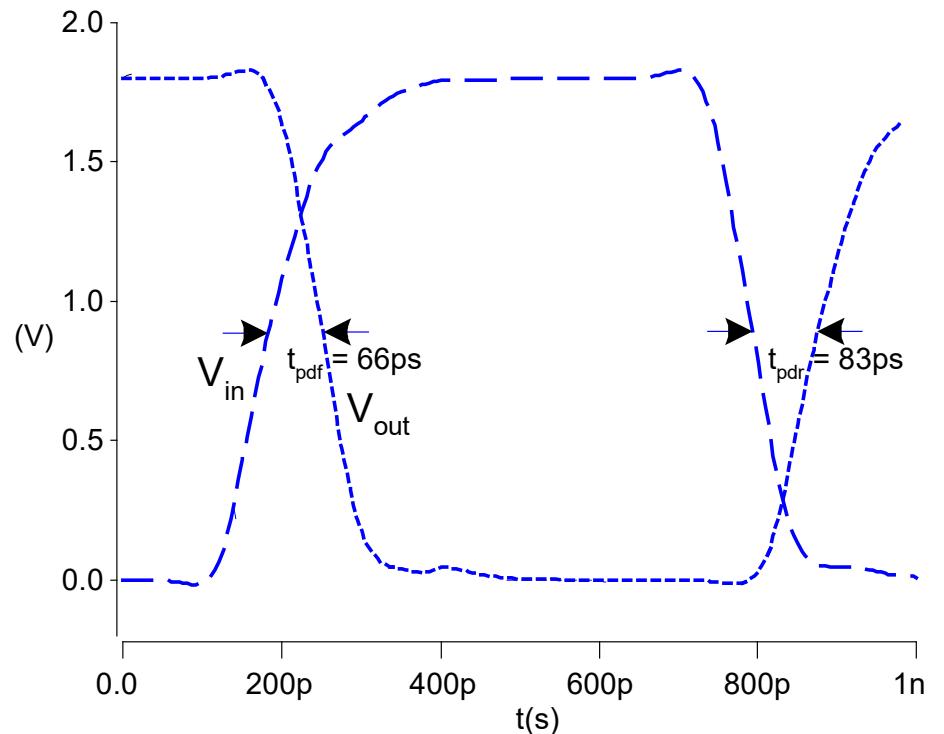
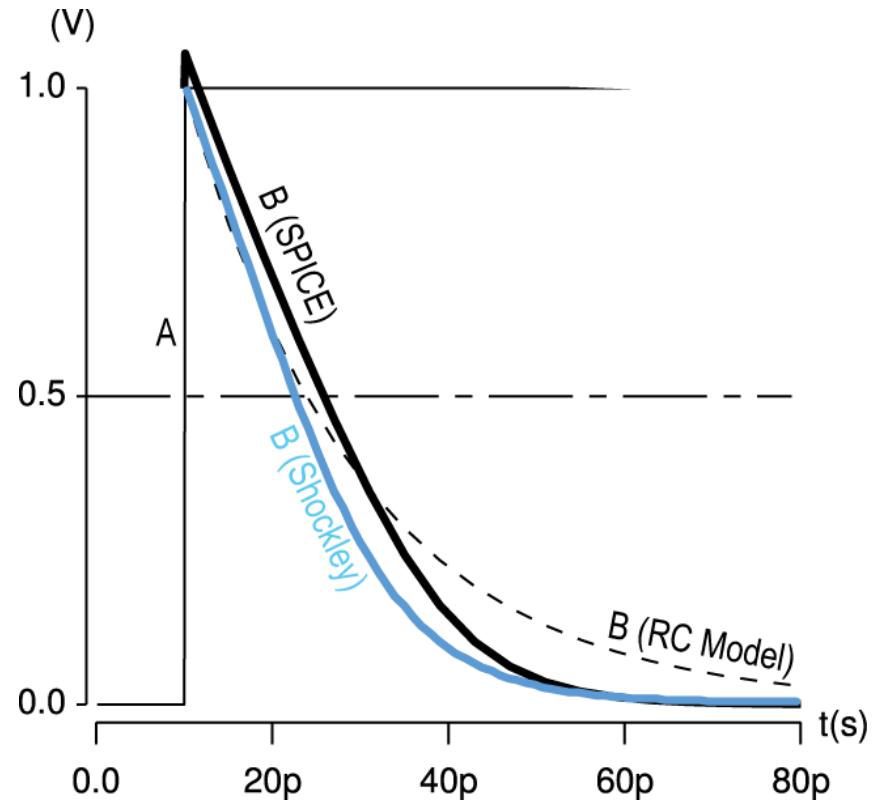


# Two Transistor (CMOS) Amplifier

Capacitor	Expression
$C_{gd1}$	$2 \text{ CGD}0_n W_n$
$C_{gd2}$	$2 \text{ CGD}0_p W_p$
$C_{db1}$	$K_{eqn} AD_n CJ + K_{eqswn} PD_n CJSW$
$C_{db2}$	$K_{eqp} AD_p CJ + K_{eqswp} PD_p CJSW)$
$C_{g3}$	$(\text{CGD}0_n + \text{CGSO}_n) W_n + C_{ox} W_n L_n$
$C_{g4}$	$(\text{CGD}0_p + \text{CGSO}_p) W_p + C_{ox} W_p L_p$
$C_w$	From Extraction
$C_L$	$\Sigma$

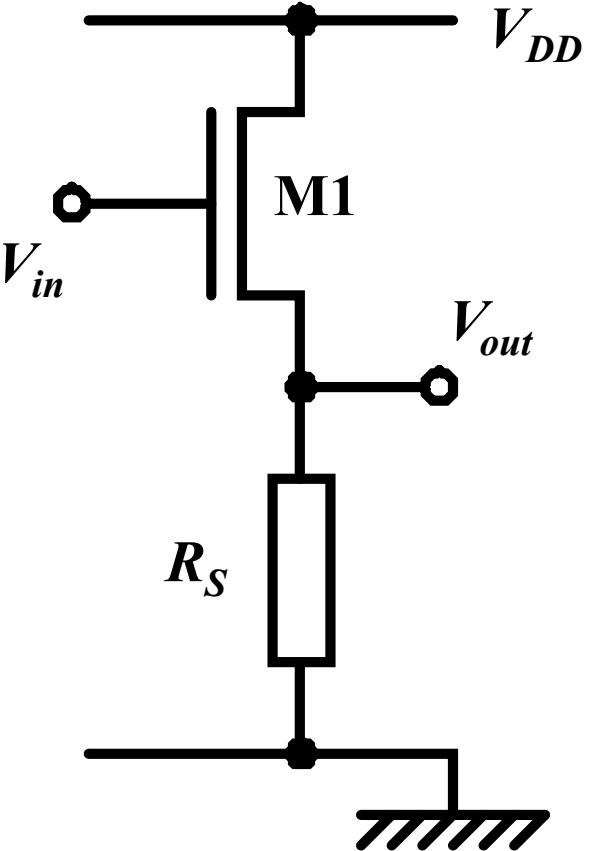
# Two Transistor (CMOS) Amplifier

- Propagation delay ( $t_p$ ) of an digital inverter



# Source follower

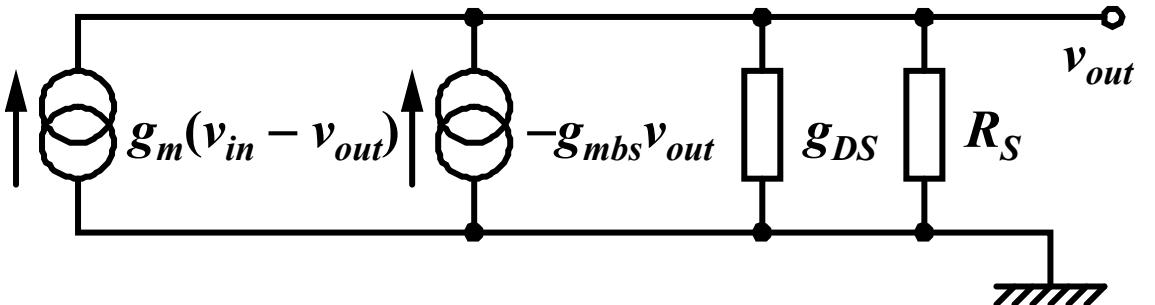
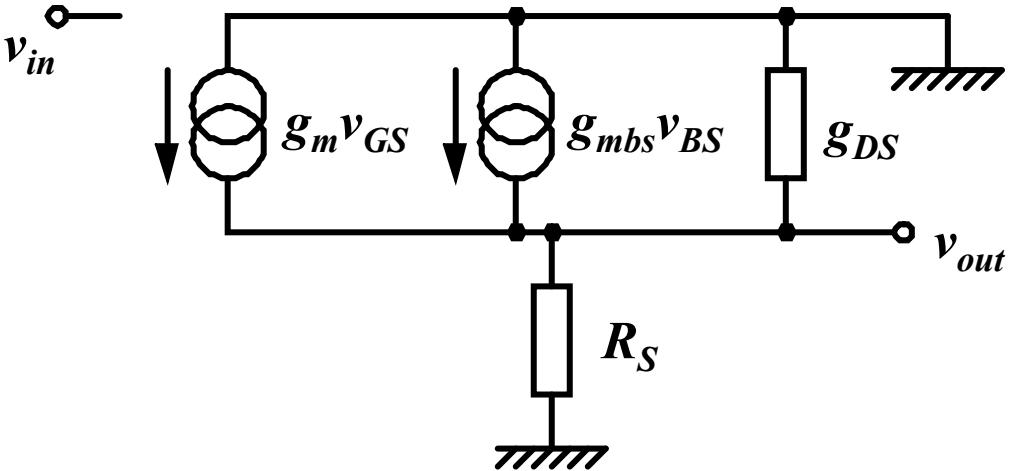
- The source follower (common-drain circuit) has a gain of  $\approx 1$
- High input impedance and low output impedance
- Used as buffer
- Very prone to body effect as  $V_{BS} = V_{out}$  and  $v_{out}$  is large



# Source follower

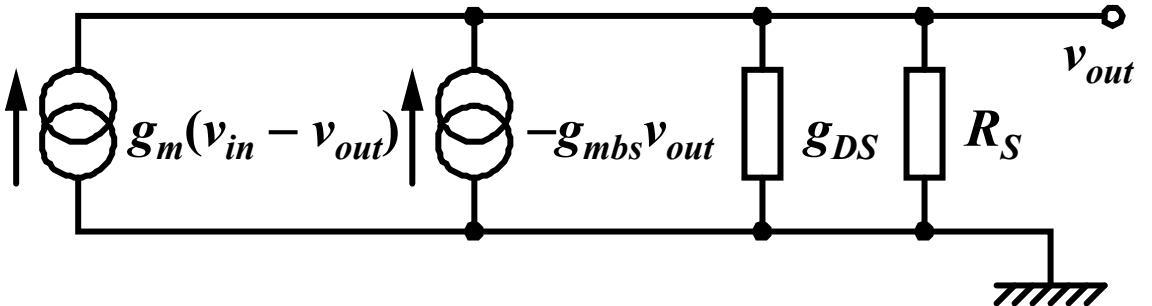


- First we have the model by direct substitution
  - Then we tidy it up to get the model shown here



# Source follower

- Sum the currents into the  $v_{out}$  node



- $g_m(v_{in} - v_{out}) - g_{mbs}v_{out} + (0 - v_{out})(g_{DS} + G_S) = 0$

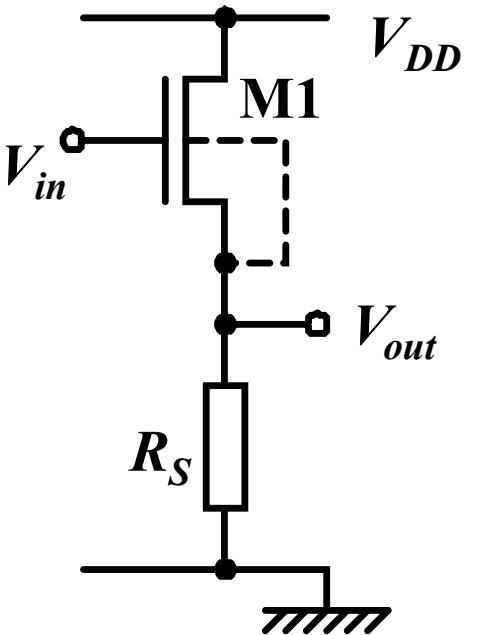
$$\Rightarrow \frac{v_{out}}{v_{in}} = \frac{g_m}{g_m + g_{mbs} + g_{DS} + G_S}$$

- This is usually slightly below one

# Source follower



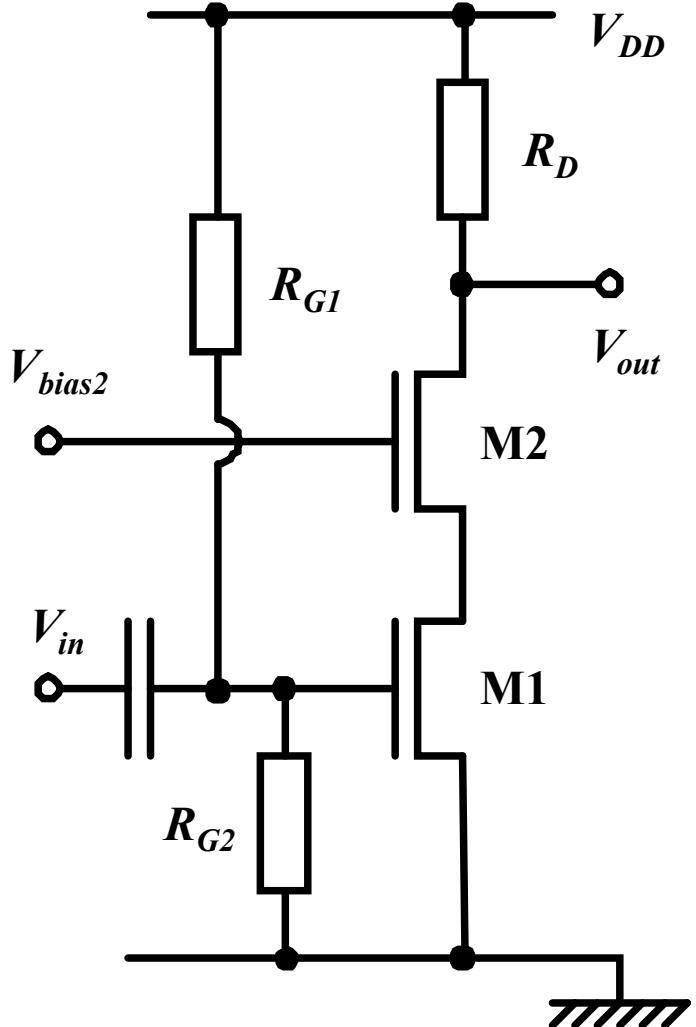
- Solution to the body-effect problem
    - connect source to bulk
  - This can work, *if* the process allows it, *but* the bulk capacitance is attached to  $V_{out}$ , crippling the bandwidth



- In some circuits it is possible to connect source and bulk to remove body effect but the bulk capacitance is always a problem as a result

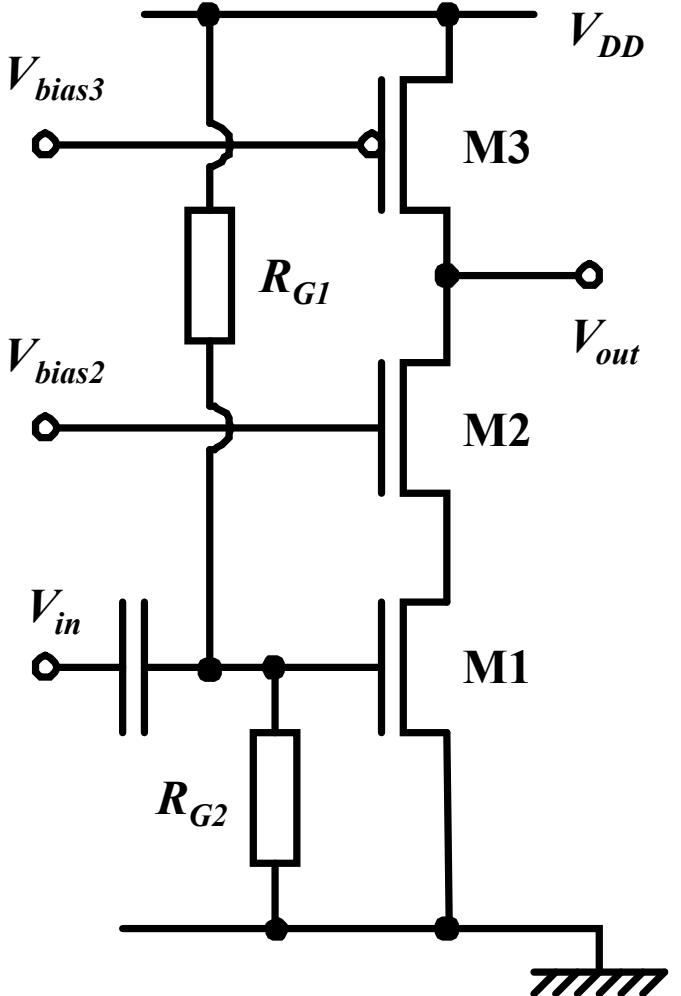
# Cascode amplifiers

- Shown here is a “cascode” amplifier
- Note extra transistor M2
- $R_D$  may be current source or any of the loads discussed
- $V_{bias2}$  is a constant so  $V_{S2}$  is approximately constant
- Therefore  $V_{D1}$  is approximately constant



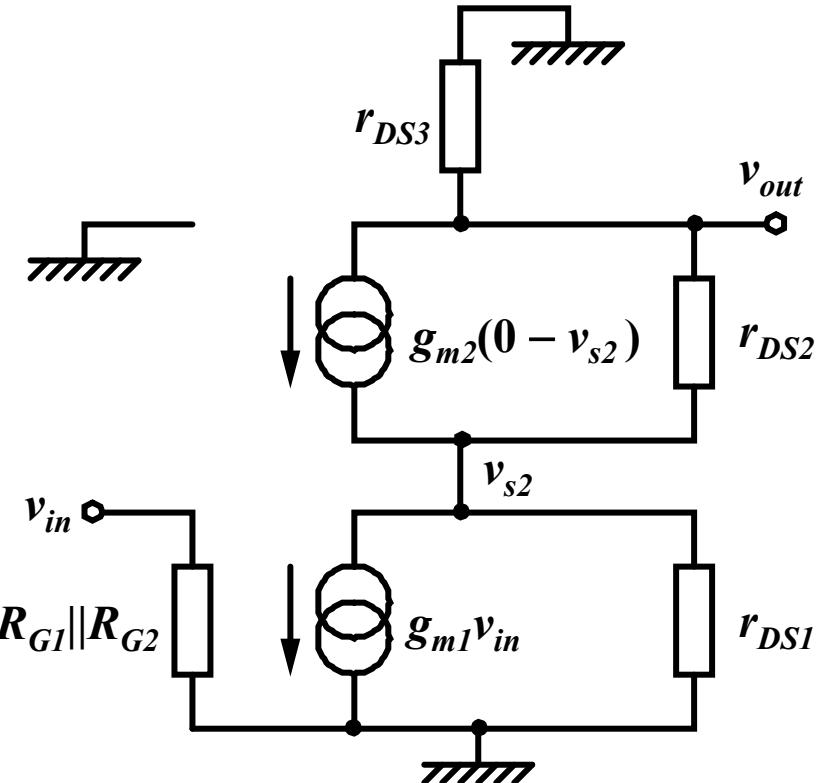
# Cascode amplifiers

- Note current-source load, M3
- Since  $V_{D1}$  is approximately constant there is (almost) no  $\lambda$  term in M1. Hence output resistance of M1 is very high
- No Miller effect since  $C_{GD1}$  is connected between amplifier input and (near) ground



# Cascode amplifiers - Gain

- Here is the small-signal model of the cascode amp
- $g_{m2}v_{s2} = (v_{out} - v_{s2})g_{DS2} + v_{out}g_{DS3}$
- $g_{m1}v_{in} + v_{s2}g_{DS1} + g_{m2}v_{s2} + (v_{s2} - v_{out})g_{DS2} = 0$



$$\frac{v_{out}}{v_{in}} = - \frac{g_{m1}(g_{m2} + g_{DS2})}{g_{DS3}(g_{m2} + g_{DS2} + g_{DS1}) + g_{DS1}g_{DS2}} \approx - \frac{g_{m1}}{g_{DS3}}$$

# Cascode amplifiers - Gain

- small-signal gain of the cascode amp:

$$\frac{v_{out}}{v_{in}} = \frac{-g_{m1}(g_{m2} + g_{DS2})}{g_{DS3}(g_{m2} + g_{DS1} + g_{DS2}) + g_{DS1}g_{DS2}}$$

- Small signal gain without cascode:

$$\frac{v_{out}}{v_{in}} = \frac{-g_{m1}}{g_{DS1} + g_{DS3}}$$

# Cascode amplifiers - Gain

- small-signal gain of the cascode amp:

$$\frac{A_v(\text{cascode})}{A_v(\text{normal})} = \frac{(g_{DS1} + g_{DS3})(g_{DS2} + g_{m2})}{g_{DS1}g_{DS2} + g_{DS3}(g_{m2} + g_{DS1} + g_{DS2})}$$

- Assume M3 is ideal current source hence  $g_{DS3}=0$ :

$$\frac{A_v(\text{cascode})}{A_v(\text{normal})} = \frac{g_{DS1}(g_{DS2} + g_{m2})}{g_{DS1}g_{DS2}} = \frac{(g_{DS2} + g_{m2})}{g_{DS2}} \approx \frac{g_{m2}}{g_{DS2}}$$

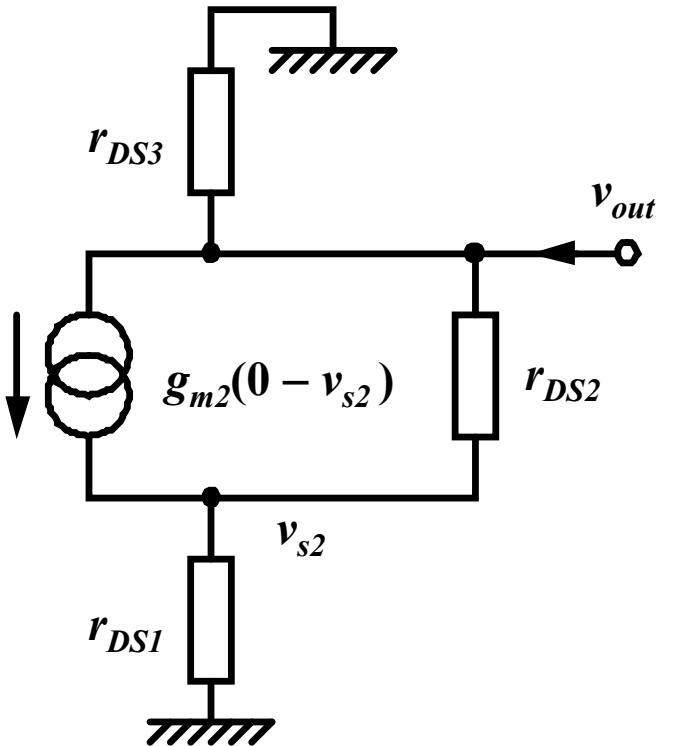
# Cascode amplifiers - Rout

- $i_o + g_{m2}v_{S2} = (v_{out} - v_{S2})g_{DS2} + v_{out}g_{DS3}$

- $v_{S2}g_{DS1} + g_{m2}v_{S2} + (v_{S2} - v_{out})g_{DS2} = 0$

- $R_{out} = \frac{(g_{m2} + g_{DS2} + g_{DS1})}{g_{DS3}(g_{m2} + g_{DS2} + g_{DS1}) + g_{DS1}g_{DS2}} \approx r_{DS3}$

- Suppose  $g_{DS3} = 0$ . Then  $R_{out} = \frac{(g_{m2} + g_{DS2} + g_{DS1})}{g_{DS1}g_{DS2}} \approx \frac{g_{m2}}{g_{DS1}g_{DS2}}$



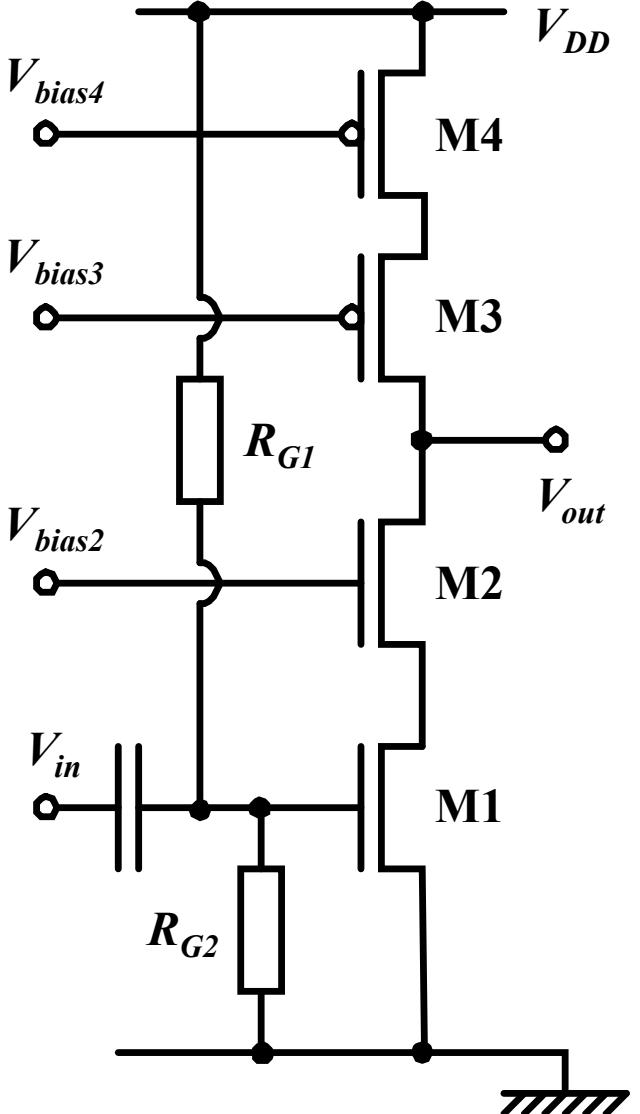
# Cascode amplifiers

- Here we also have a cascode load

$$\bullet \quad R_{out(low)} = \frac{g_{m2}}{g_{DS1}g_{DS2}} \quad R_{out(upper)} = \frac{g_{m3}}{g_{DS3}g_{DS4}}$$

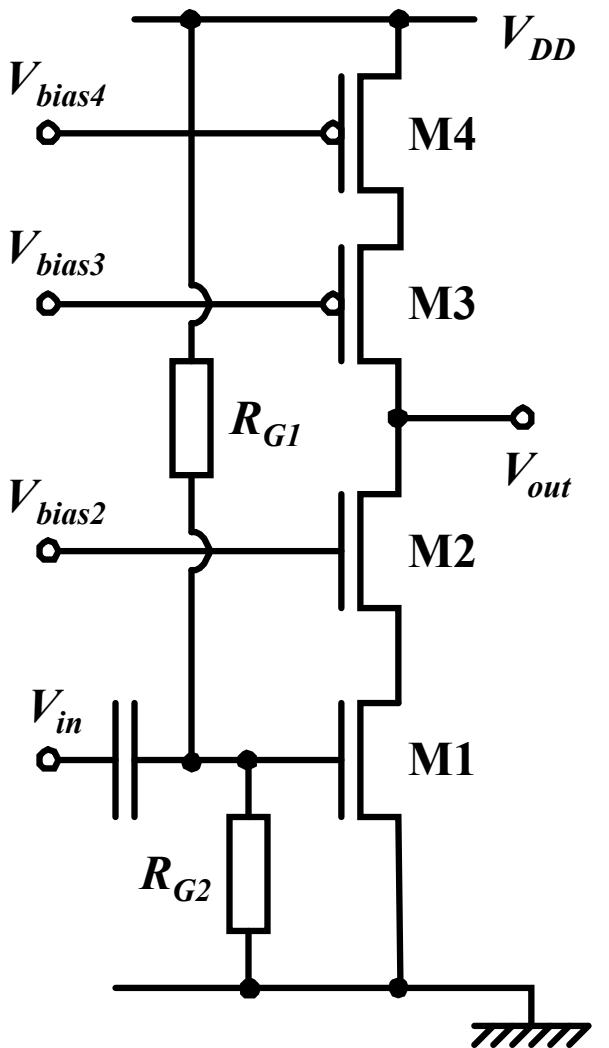
$$\bullet \quad R_{out} = \frac{g_{m2}g_{DS3}g_{DS4} + g_{m3}g_{DS1}g_{DS2}}{g_{DS1}g_{DS2}g_{DS3}g_{DS4}}$$

$$\bullet \quad R_{out} = \frac{\sqrt{2\beta_2\beta_3}}{I_{DS}^{3/2}(\lambda_N^2\sqrt{\beta_3} + \lambda_P^2\sqrt{\beta_2})}$$



# Cascode amplifiers

- The AC gain is given by the input transistor transconductance,  $g_{m1}$ , multiplied by  $R_{out}$
- $$Gain = -\frac{g_{m1}(g_{m2}g_{DS3}g_{DS4} + g_{m3}g_{DS1}g_{DS2})}{g_{DS1}g_{DS2}g_{DS3}g_{DS4}}$$
- $$Gain = -\frac{2\sqrt{\beta_1\beta_2\beta_3}}{I_{DS}(\lambda_N^2\sqrt{\beta_3} + \lambda_P^2\sqrt{\beta_2})}$$
- Observe gain  $\propto 1/I_{DS}$

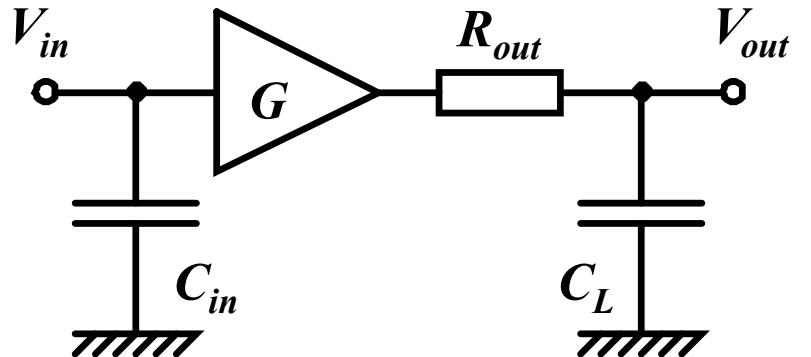


# Cascode amplifiers

- The output resistance of an amplifier, when cascaded by transistor M2, rises by a factor of about  $g_{m2}/g_{DS2}$
- The gain of an amplifier, when cascaded by transistor M2, rises by a factor of about  $g_{m2}/g_{DS2}$
- This is not a co-incidence!

# Another Circuit Model

- This model, including the circuit capacitances, is more useful as they are the major problem in CMOS design

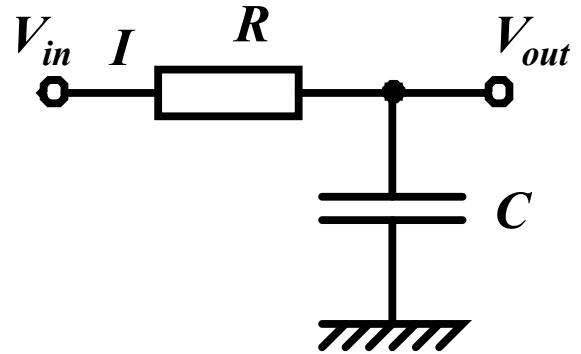


- Note that  $R_{in}$ , not very useful in MOS design, has gone
- $C_{in}$  - amplifier input capacitance, usually gate capacitance
- $C_{out}$  - amplifier load capacitance, usually stray capacitance and the capacitance of the stage being *driven*.
- This is all more interesting when two amps are cascaded

# Reminder of AC Circuit Analysis

- The AC circuit of most interest is the R-C low-pass filter. Its *frequency response* is most important
- The magnitude of the total impedance of this circuit is  $|Z|$ , given by:-

$$|Z| = \sqrt{R^2 + X_C^2} \text{ where } X_C = (1/2\pi f C) \equiv (1/\omega C)$$



- The magnitude of the current in the circuit,  $|I|$ , is given by:-  $|I| = |V_{in}| / |Z|$
- $|V_{out}|$  is given by

$$|V_{out}| = |I|X_C = (|V_{in}|X_C) / |Z|$$

# Reminder of AC Circuit Analysis

- We have:-

$$|V_{out}| = (|V_{in}| X_C) / |Z|$$

- Therefore

$$\frac{|V_{out}|}{|V_{in}|} = \frac{X_C}{|Z|} = \frac{X_C}{\sqrt{R^2 + X_C^2}}$$

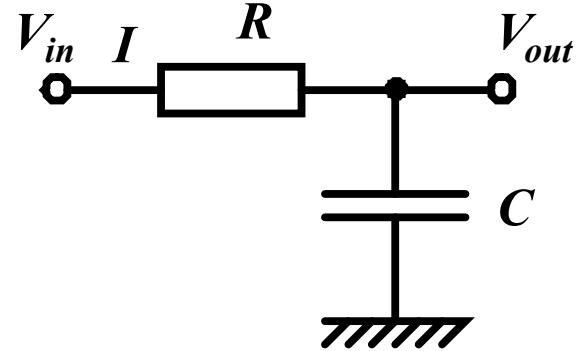
- The *bandwidth* of a circuit is defined to be the frequency at which

$$|V_{out} / V_{in}| = 1 / \sqrt{2}$$

- In this case, that would be when  $X_C = R$

- Therefore, circuit bandwidth,  $f_c =$

$$\frac{1}{2\pi RC}$$

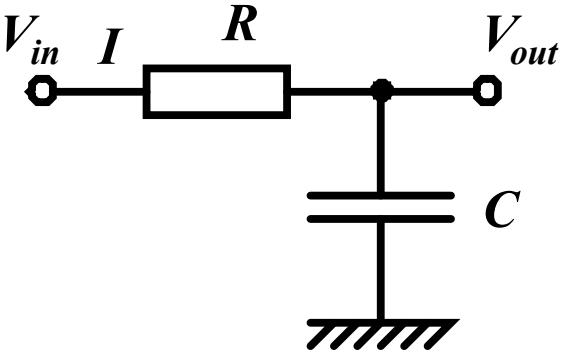


# AC Circuit Analysis

- The *impedance* of a capacitor is  $Z_C = 1/(j\omega C)$  where

$$j = \sqrt{-1}$$

- $\omega = 2\pi f$  ( $f$  is frequency in Hertz)



- Hence

$$\frac{V_{out}}{V_{in}} = \frac{1/j\omega C}{R + 1/j\omega C} = \frac{1}{1 + j\omega RC}$$

$$\left| \frac{V_{out}}{V_{in}} \right| = \frac{1}{\sqrt{1 + (\omega RC)^2}}$$

and

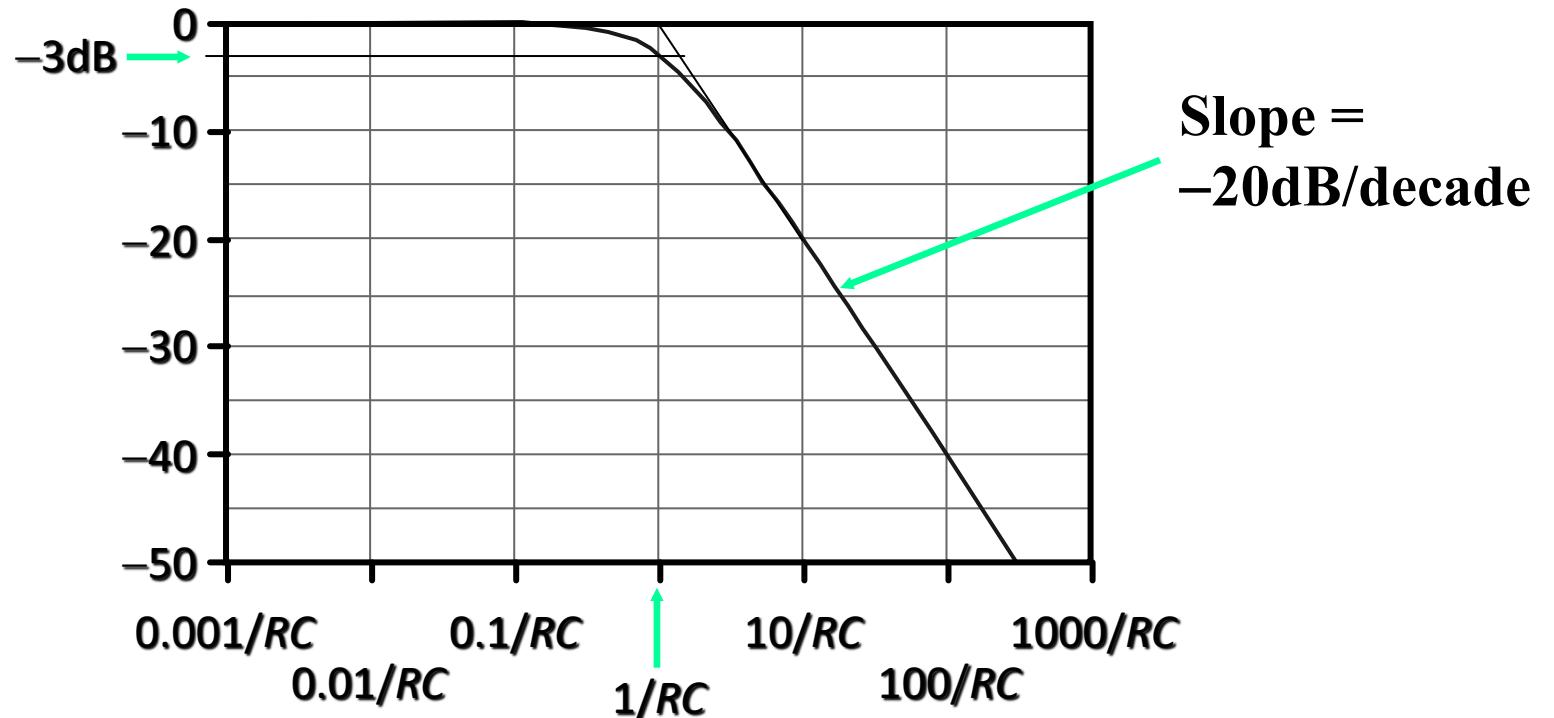
$$\text{Arg}\left(\frac{V_{out}}{V_{in}}\right) = -\tan^{-1}(\omega RC)$$

# AC Circuit Analysis

- Plot

$$\left| \frac{V_{out}}{V_{in}} \right| = \frac{1}{\sqrt{1 + (\omega RC)^2}}$$

with increasing  $\omega$



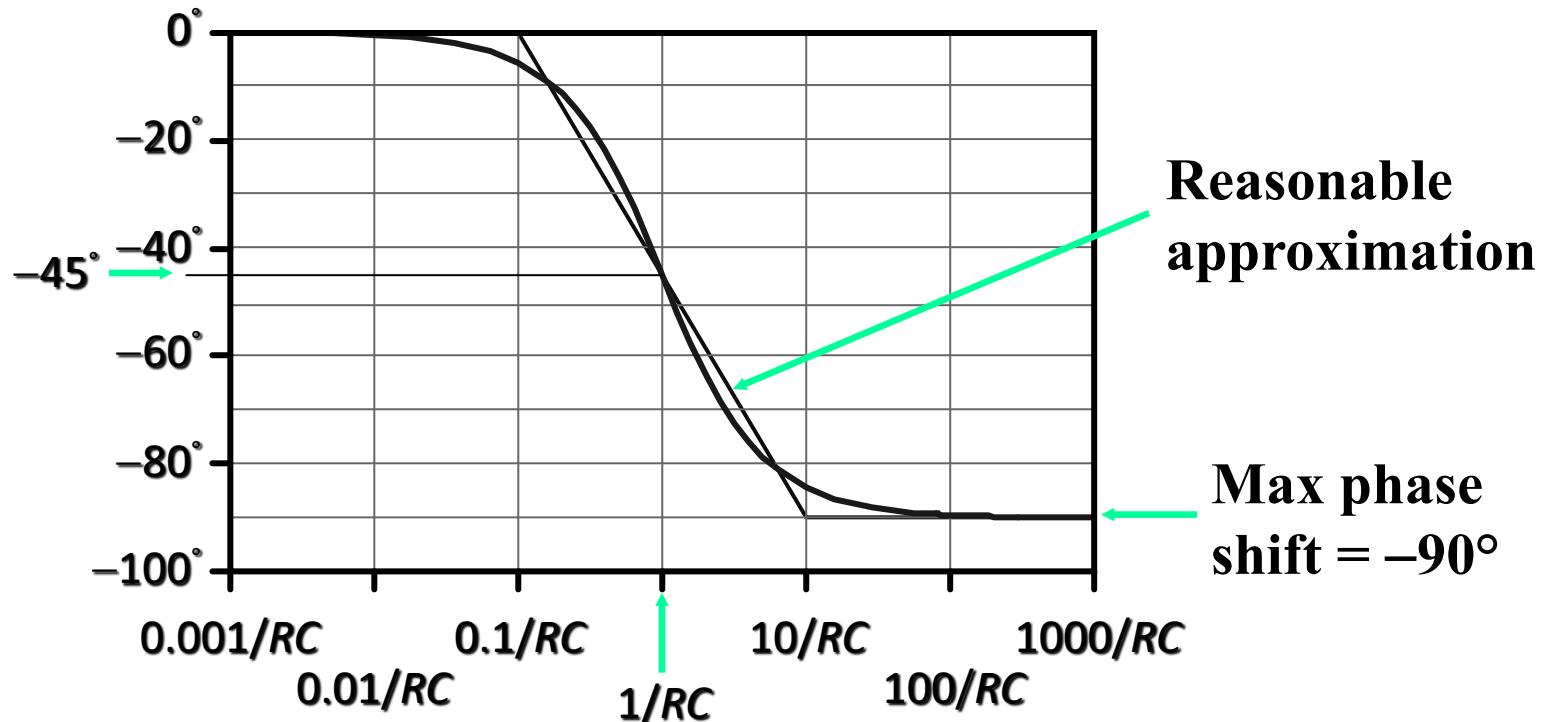
Slope =  
**-20dB/decade**

# AC Circuit Analysis

- Plot

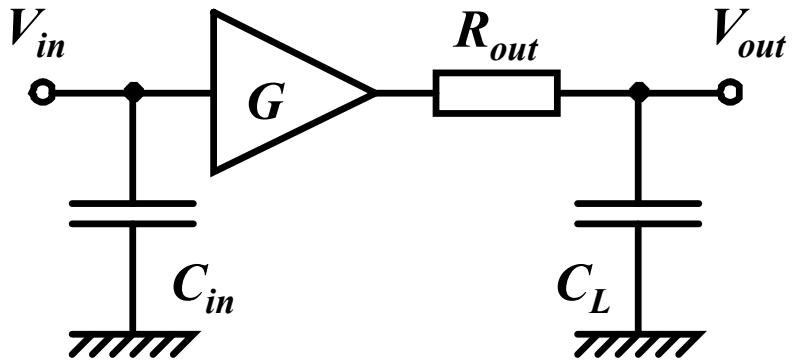
$$\text{Arg}\left(\frac{V_{out}}{V_{in}}\right) = -\tan^{-1}(\omega RC)$$

with increasing  $\omega$



# Amplifier Bandwidth

- Now we see how the AC response of the amplifier will be affected by  $R_{out}$  and the load capacitance,  $C_L$



- The bandwidth of the amplifier,  $f$ , will be given

by:-  $\omega = 1 / R_{out} C_L \Rightarrow f = \frac{1}{2\pi R_{out} C_L}$

- This is a *serious* problem!

# Two Transistor (CMOS) Amplifier

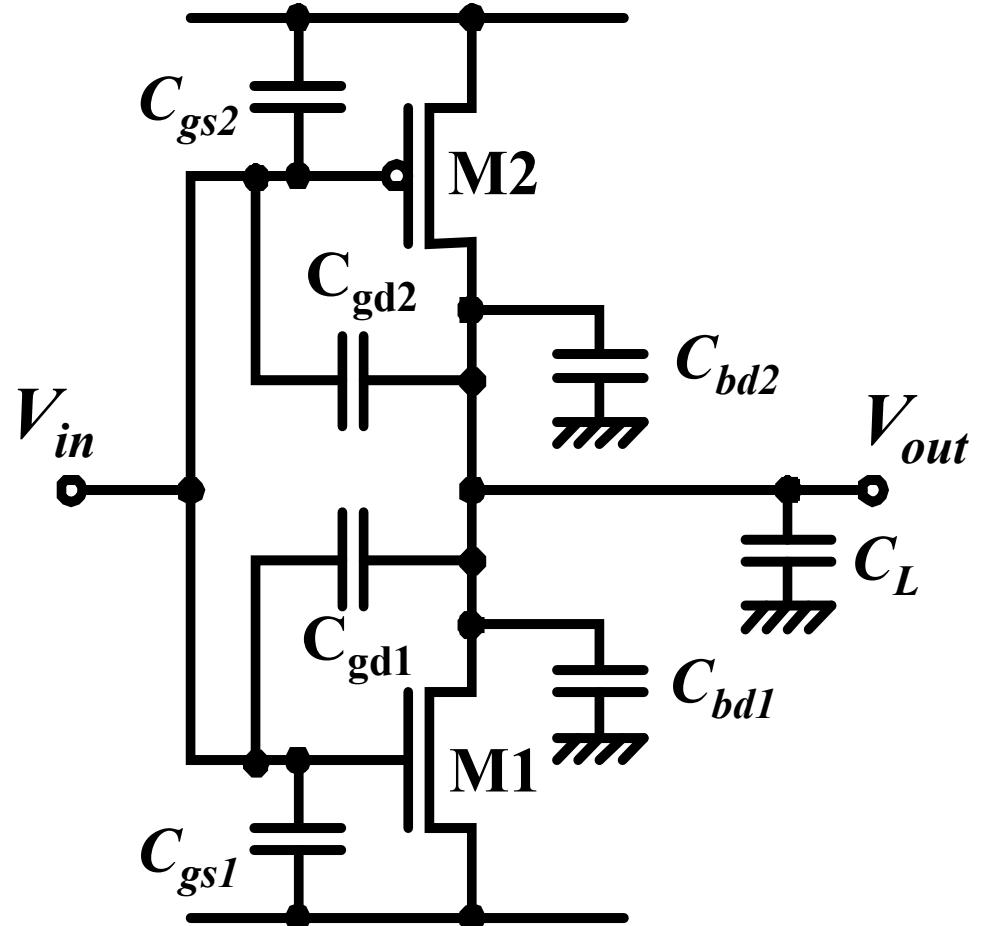
- First take the basic circuit

**Add Gate/Source caps**

**Add Bulk/Drain caps**

**Add Gate/Drain caps**

**Don't forget the load cap!**



# Two Transistor (CMOS) Amplifier

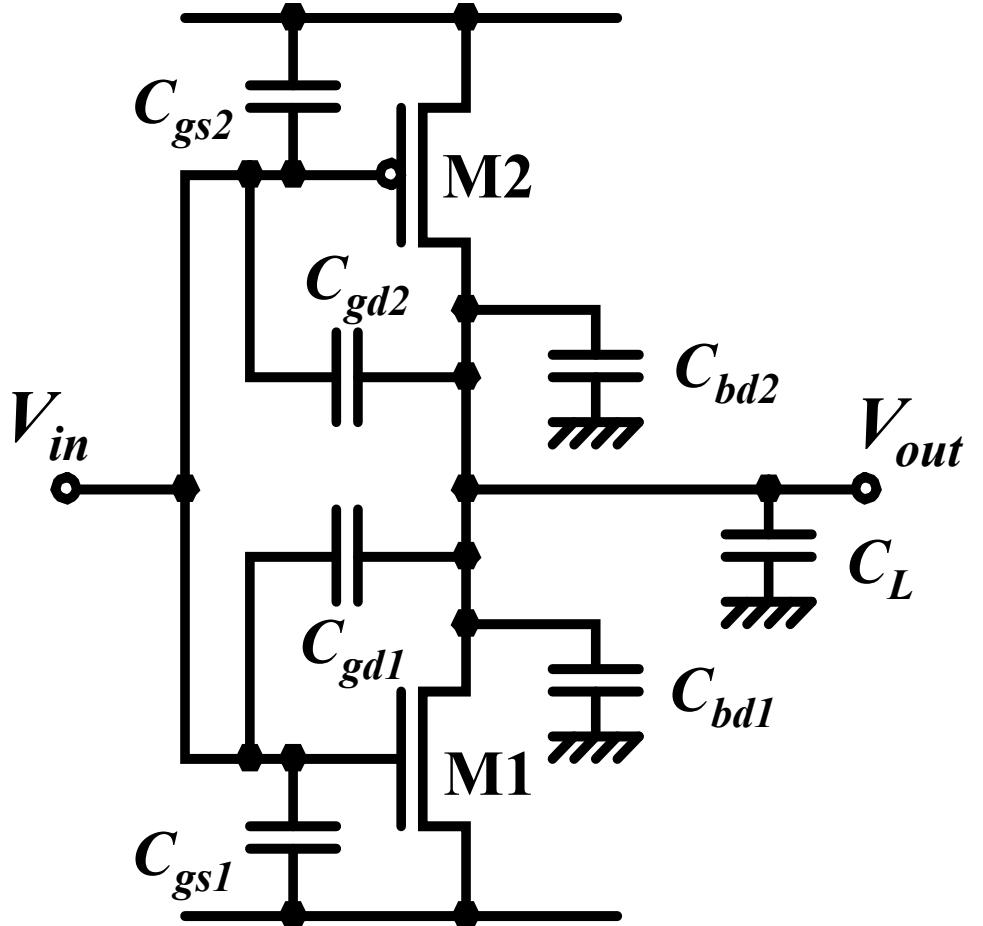
- Add together (no need to include  $C_{gs1}$  or  $C_{gs2}$ ) to get

$$C_T = C_{gd1} + C_{gd2} + C_{bd1} + C_{bd2} + C_L$$

which we will consider to be the load capacitance.

- The output conductance of this circuit is  $(g_{DS1} + g_{DS2})$  so the

bandwidth is:- 
$$\frac{(g_{DS1} + g_{DS2})}{2\pi C_T} \text{ Hz}$$



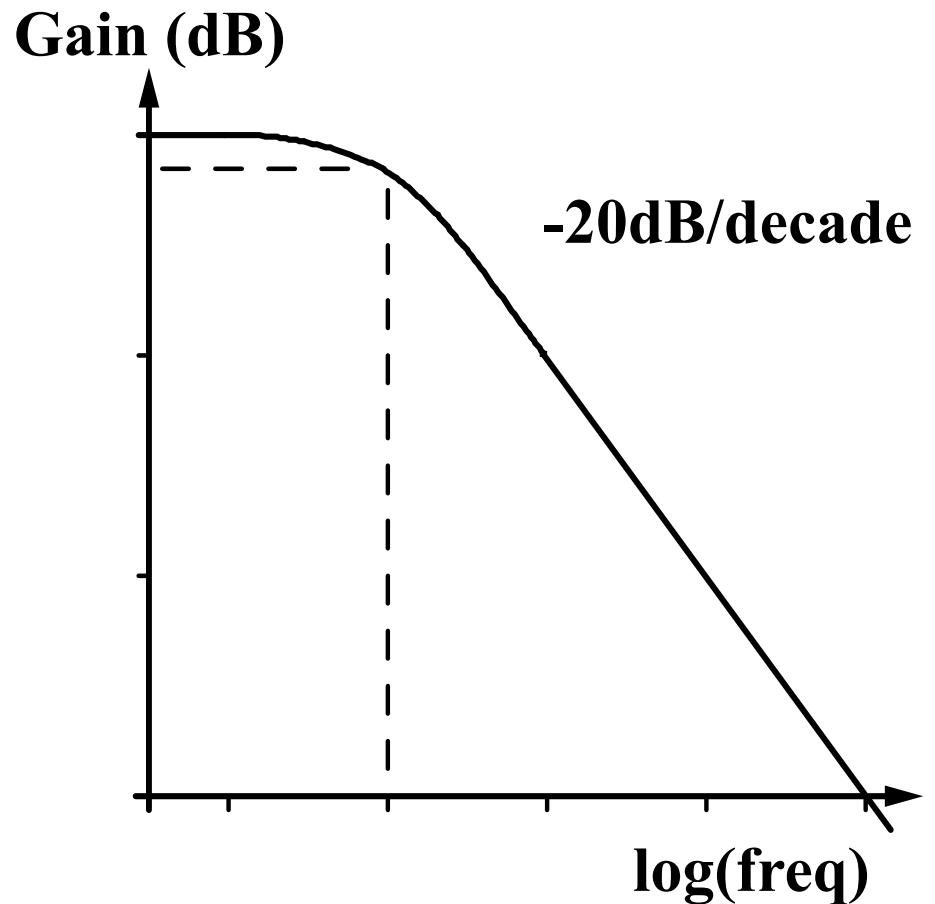
# CMOS Inverter Frequency Response

- DC Gain = 
$$-\frac{(g_{m1} + g_{m2})}{(g_{ds1} + g_{ds2})}$$

- 3dB point at 
$$\frac{(g_{ds1} + g_{ds2})}{C_T}$$

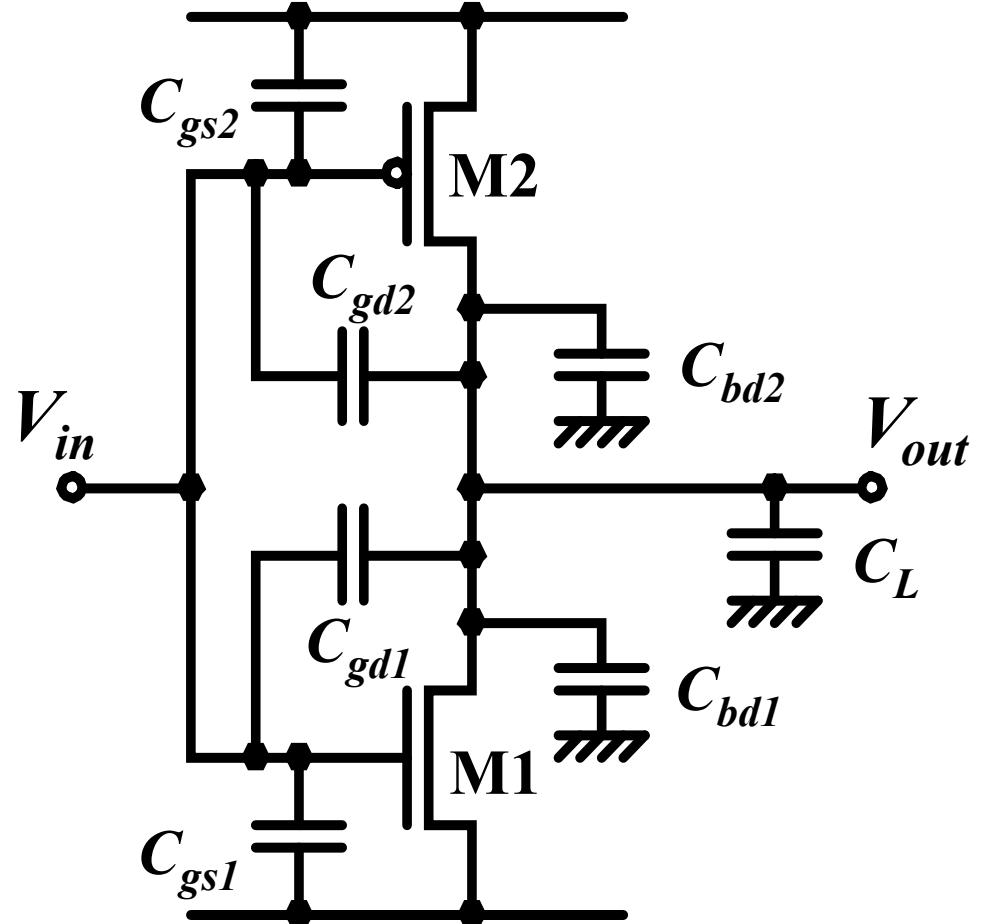
- Note Gain  $\propto \frac{1}{\sqrt{I_{DS}}}$

- Bandwidth  $\propto I_{DS}$

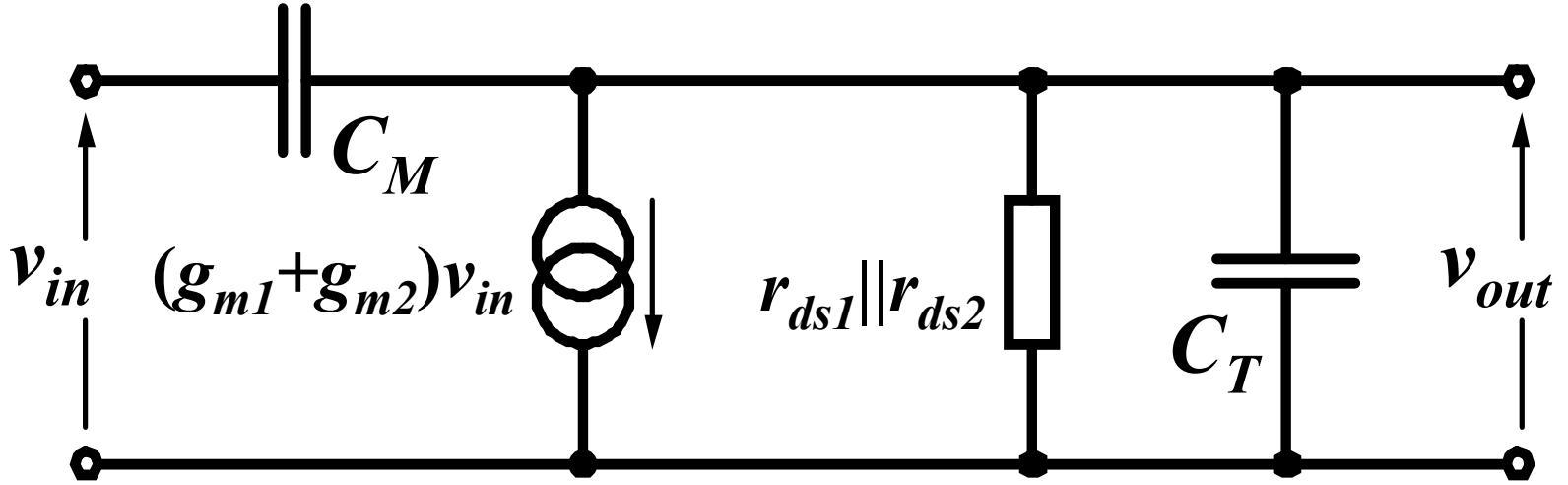


# CMOS Inverter - Analogue

- Note that  $C_{gd1}$  and  $C_{gd2}$  are connected between the amplifier I/P and O/P
- They *can* be considered part of the load cap,  $C_T$ , but have a more significant influence due to the *Miller Effect*



# CMOS Inverter - Analogue



- $C_M = C_{gd1} + C_{gd2}$  and the rest is as before
- Note the capacitor,  $C_M$ , is connected between the amplifier input and output

# Miller effect

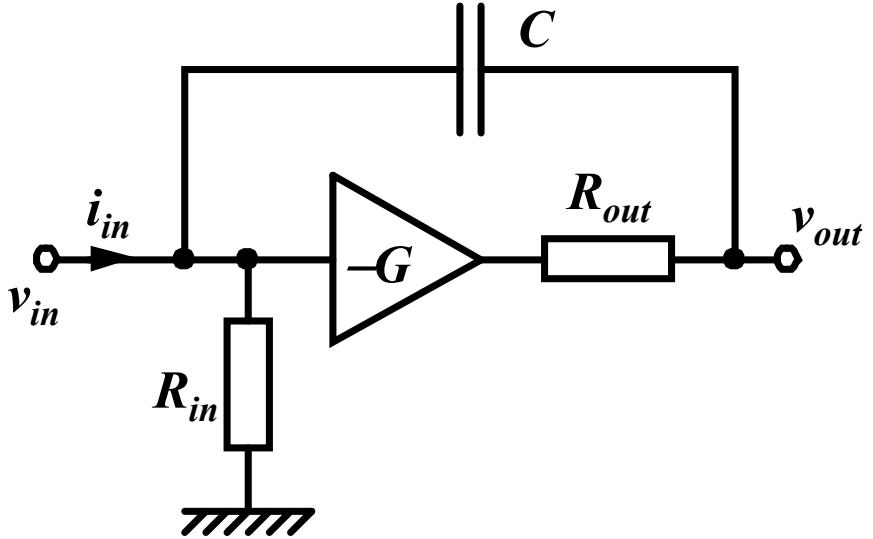
- Suppose that a capacitor,  $C$ , is connected between input and output of our model
- What is the new input impedance?
- Equations are:

- IP node:

$$i_{in} + \frac{0 - v_{in}}{R_{in}} + (v_{out} - v_{in})j\omega C = 0$$

- OP node:

$$\frac{(-Gv_{in} - v_{out})}{R_{out}} + (v_{in} - v_{out})j\omega C = 0$$



# Miller effect

- Eliminate  $v_{out}$  and solve for  $R_{in\_new} = v_{in}/i_{in}$  to

get:

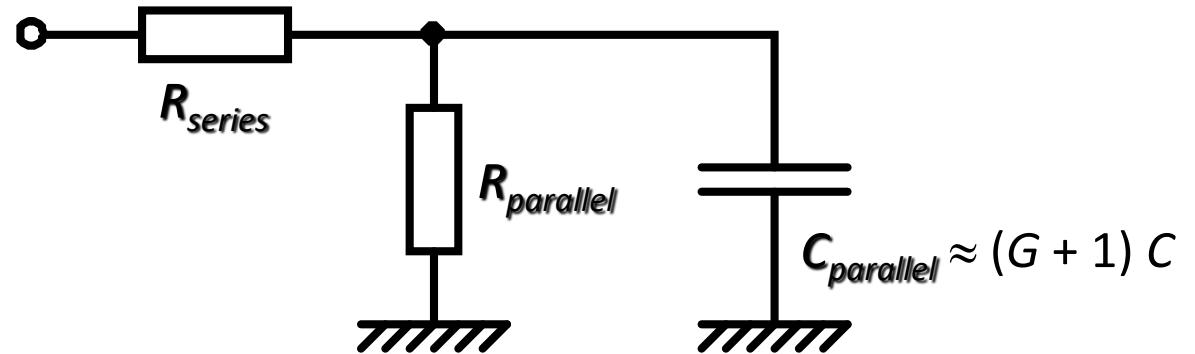
$$R_{in\_new} = \frac{R_{in}(1 + R_{out}Cj\omega)}{1 + (R_{out}C + R_{in}C(G+1))j\omega}$$

- We can show that this is equal to:

$$R_{in\_new} = R_{series} + \left( \frac{1}{R_{parallel}} + \frac{1}{1/j\omega C_{parallel}} \right)^{-1}$$

# Miller effect

- $R_{series} + \left( \frac{1}{R_{parallel}} + \frac{1}{1/j\omega C_{parallel}} \right)^{-1}$  has equivalent circuit

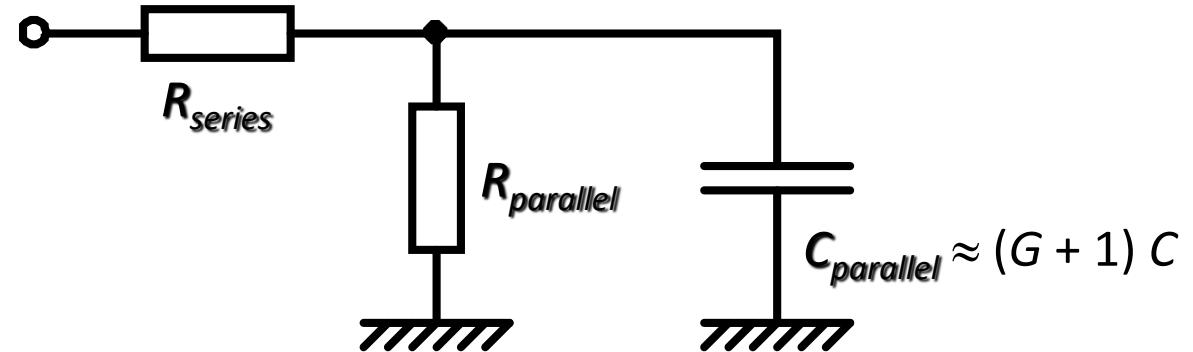


- with

$$C_{parallel} = \left( \frac{R_{out} + (G+1)R_{in}}{R_{in}} \right)^2 \frac{C}{G+1} \approx (G+1)C$$

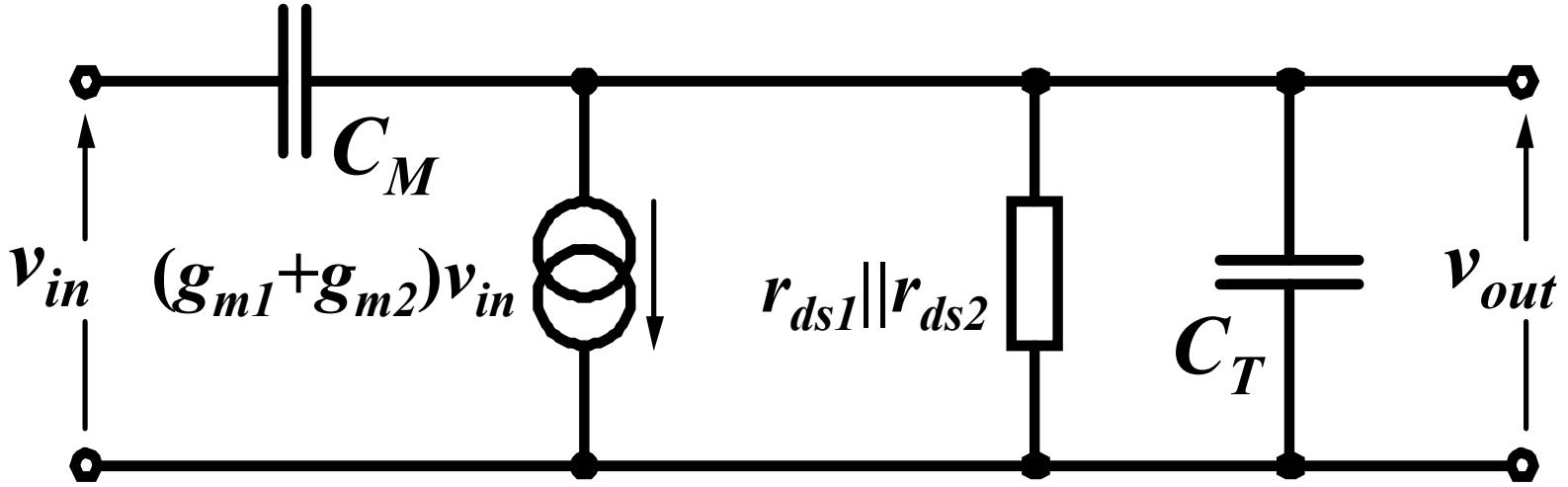
# Miller effect

- $R_{parallel} \approx R_{in}$ , just the original value
- $R_{series} \approx R_{out} / (G + 1)$ , relatively small



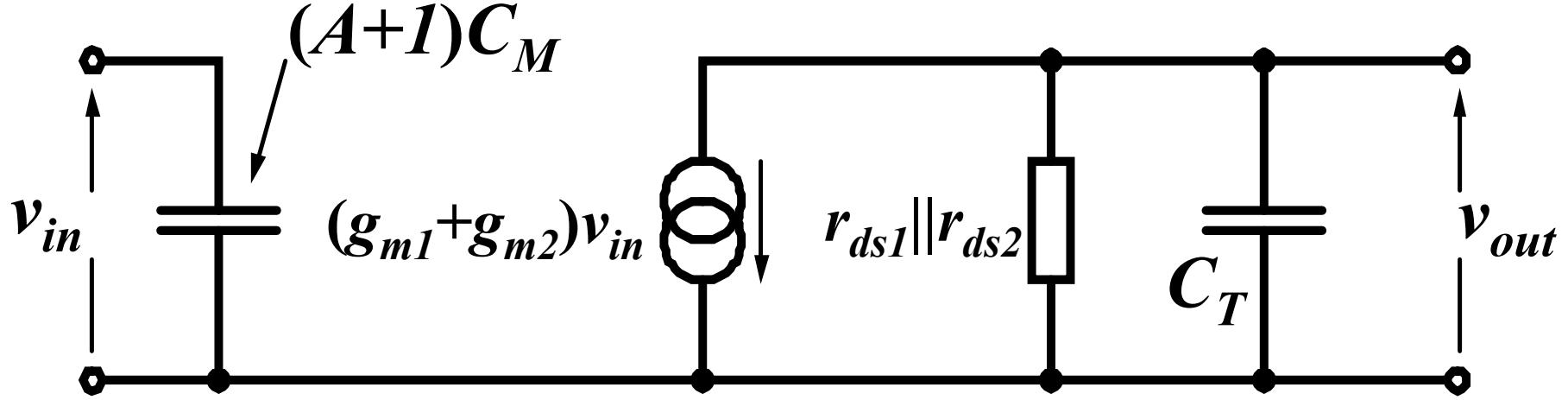
- Capacitor is a *major* problem for driving stage
- Can enormously reduce system bandwidth

# CMOS Inverter - Analogue



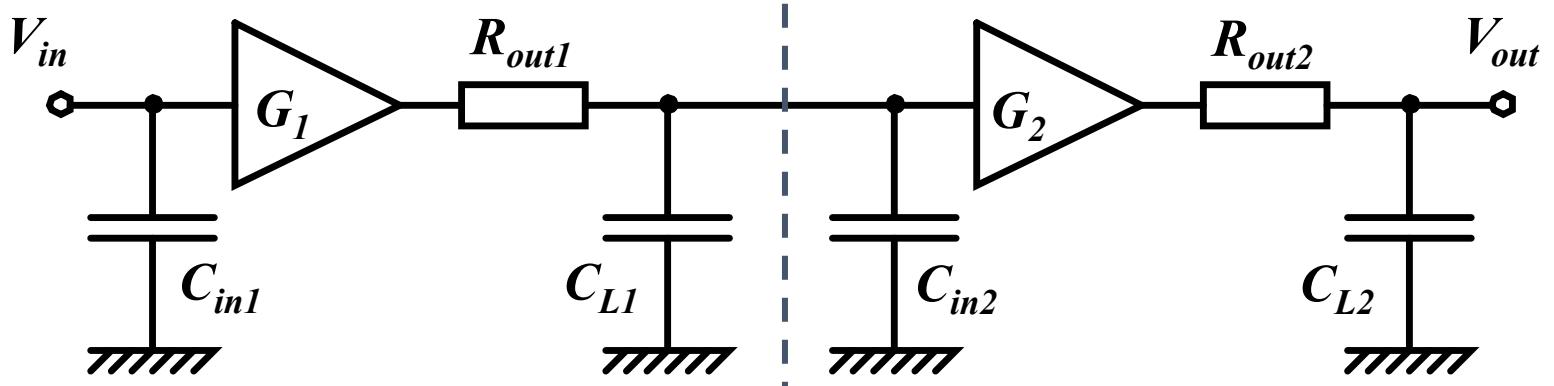
- $C_M = C_{gd1} + C_{gd2}$  - remainder of model unchanged
- The Miller Effect multiplies  $C_M$  by the amplifier gain and connects it from  $v_{in}$  to ground

# CMOS Inverter - Analogue



- Here “ $A$ ” is the amplifier gain, which is large.
- This “Miller Capacitance” is a big load on the previous stage and introduces an extra, significant, pole that can dominate the frequency response

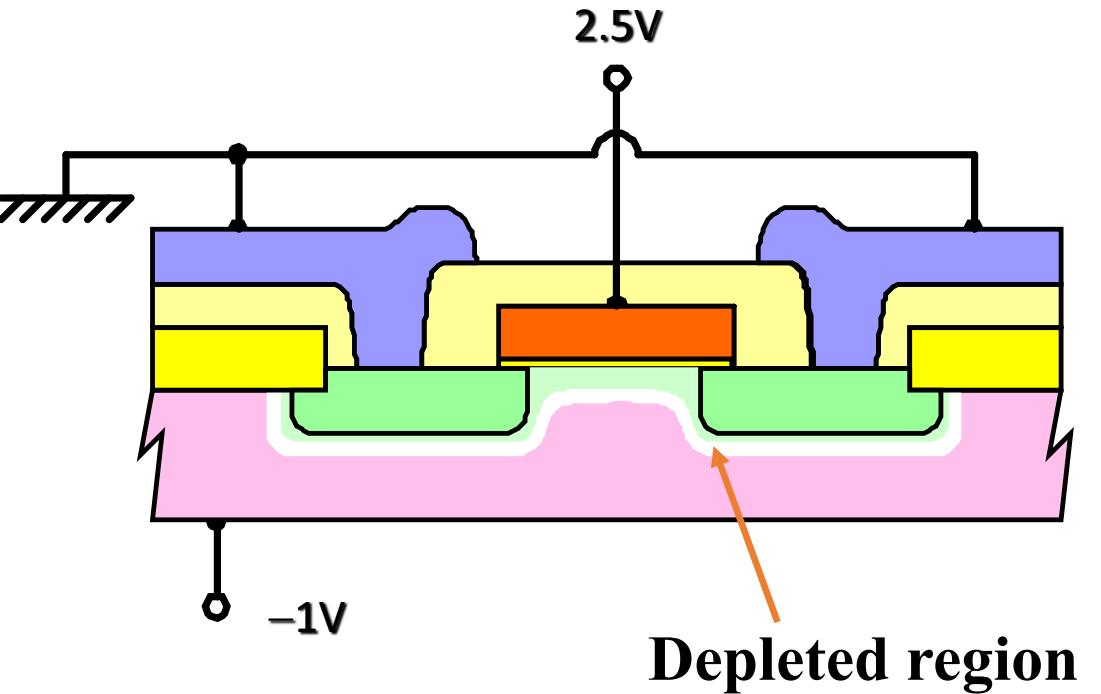
# Cascaded Amplifiers



- Here we see two amplifiers in cascade
- $C_{in1}$  is driven by  $v_{in}$  so is no problem
- Otherwise we see two low-pass filters
- $C_{in1}$  and  $C_{in2}$  will be increased by Miller effect

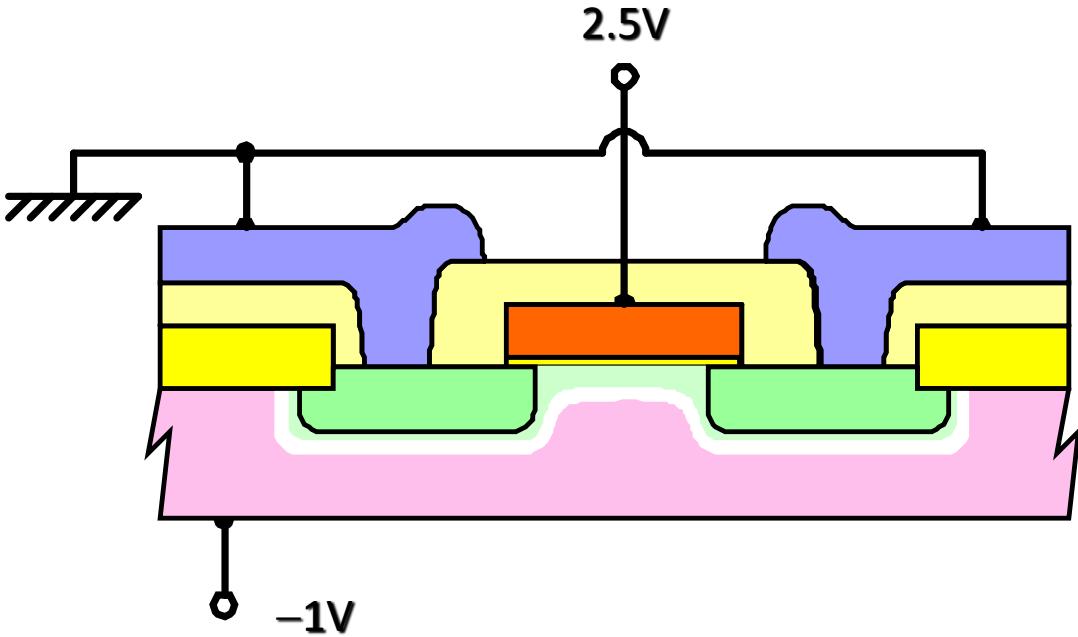
# Body effect

- Suppose that we set up a transistor in the usual way *but* we connect  $-1V$  to its substrate
- Then a depletion region will form between the reverse-biased source/substrate and drain/substrate
- It will also appear under the channel



# Body effect

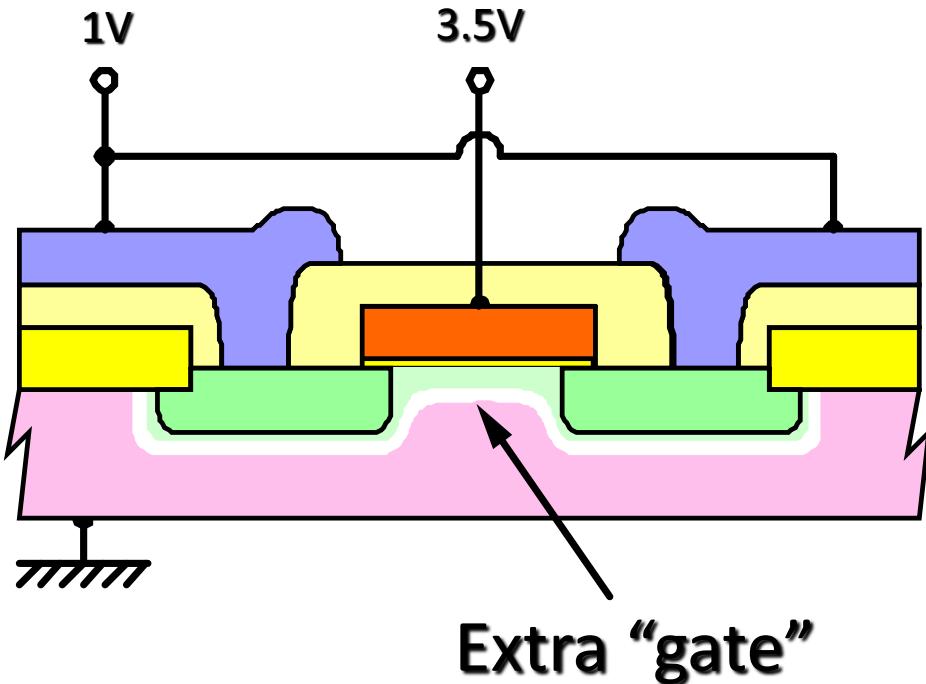
- Under the channel, but separated from it by an insulating depletion region is a “plate” at a potential of  $-1V$



- Gate at  $+2.5V$  trying to turn transistor ON, “plate” below trying to turn transistor OFF. The effect is similar to *increasing* the transistor threshold voltage

# Body effect

- This situation is identical - only the reference is lifted by 1V
- Source is *not grounded*
- Effect is still that of increasing the transistor threshold voltage



$$V_T = V_{T0} + \gamma \left( \sqrt{2|\phi_f| + V_{SB}} - \sqrt{2|\phi_f|} \right)$$

# Body effect

- The full story is:

$$V_T = V_{T0} + \gamma \left( \sqrt{2|\phi_f| + V_{SB}} - \sqrt{2|\phi_f|} \right)$$

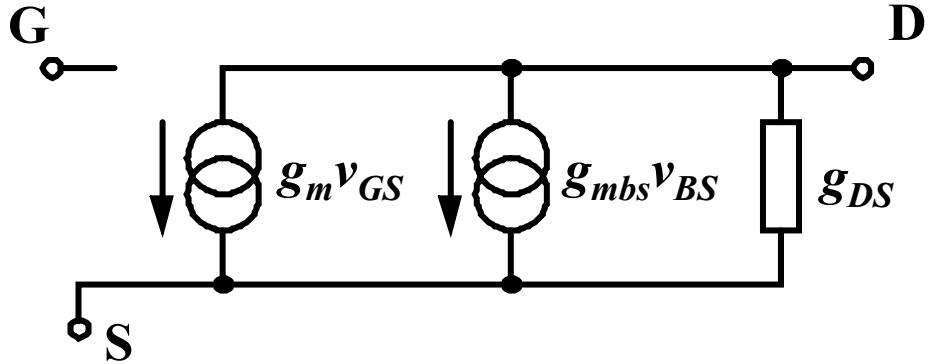
with

$$\phi_f = \frac{kT}{q} \ln \left( \frac{N_{SUB}}{n_i} \right) , \text{ often around } 0.35V$$

$$\gamma = \frac{1}{C_{ox}} \sqrt{2q\varepsilon_{Si} N_{SUB}} , \text{ often around } 0.5 \text{ V}^{\frac{1}{2}}$$

# Extended transistor model

- Here  $g_{mbs}$  has been included in the transistor model
- If  $V_{BS}$  is constant then  $v_{BS} = 0$  and the right-hand current source has no effect
- We need not use this extended model often, but sometimes it is very important



# Calculation of $g_{mbs}$

- To model body effect we include another current source,  $g_{mbs}$ , in the transistor model

- We have

$$g_{mbs} = \frac{dI_{DS}}{dV_{BS}} = -\frac{dI_{DS}}{dV_T} \frac{dV_T}{dV_{SB}}$$

- $\frac{dI_{DS}}{dV_T} = -\beta(V_{GS} - V_T)$  and  $\frac{dV_T}{dV_{SB}} = \frac{\gamma}{2\sqrt{2\phi_f + V_{SB}}}$

- Hence

$$g_{mbs} = \frac{\gamma\beta(V_{GS} - V_T)}{2\sqrt{2\phi_f + V_{SB}}} = g_m \frac{\gamma}{2\sqrt{2\phi_f + V_{SB}}}$$