



Electronic Information Displays – Route Map

CORE PROGRAMME

-  S1 Logistics
-  S2 Context
-  S3 LC Intro
-  S4 Passive Matrix
-  S5 Active Matrix Addr
-  S6 Active Matrix Tech
- S7 OLED Intro
- S8 OLED Elec
- S9 Microdisplays

GUEST PROGRAMME

- Travis AR VR
- Hands LC not display
- Khan Light Field
- Srivastava QD/QR
- McKendry MicroLED

S6 Active-Matrix Technology – Contents

Substrates

Amorphous Silicon

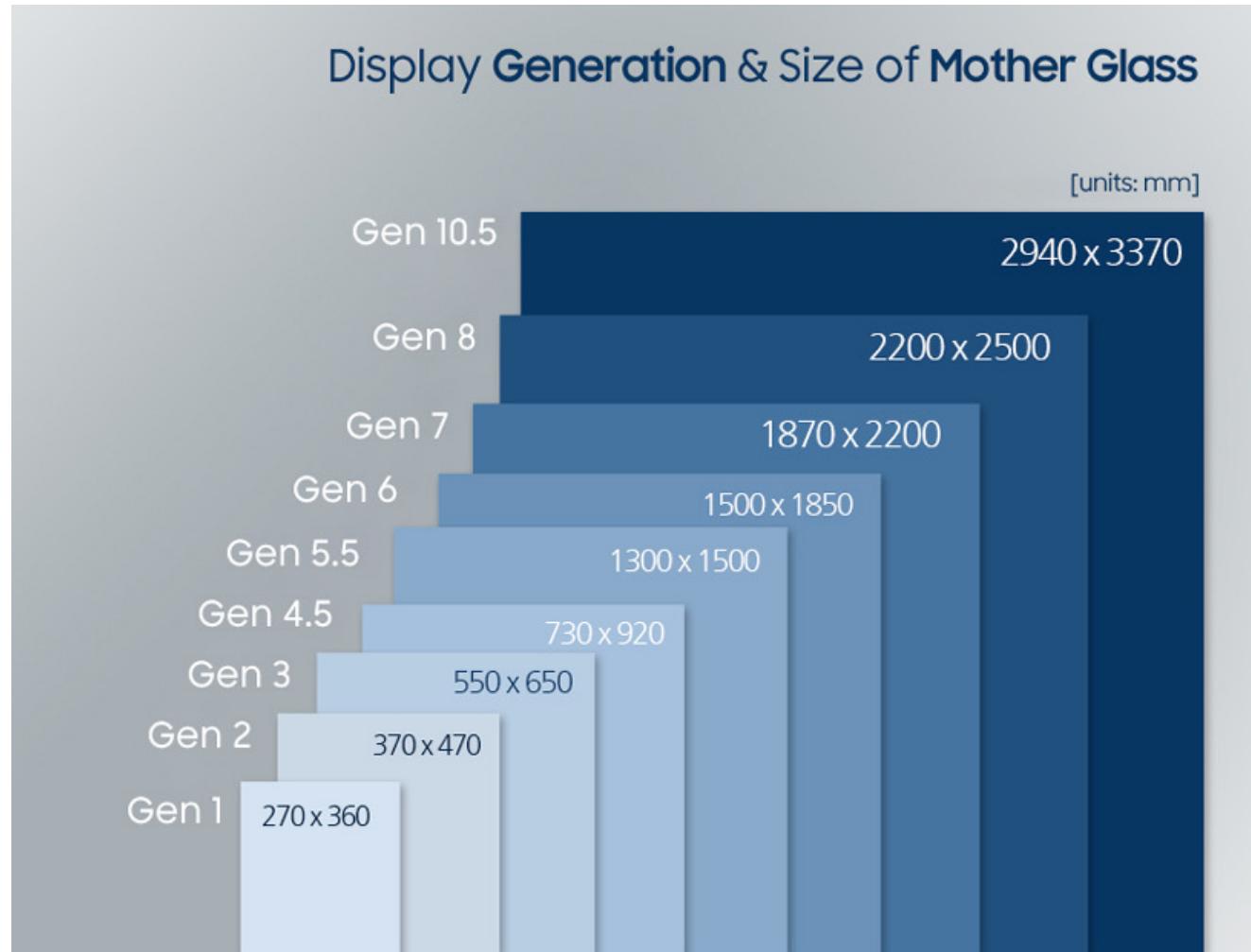
α -Si TFT device

TFT AMLCD Pixel

Back Channel Etched Process

Low-temp Poly Process

Evolution of Glass Substrate size

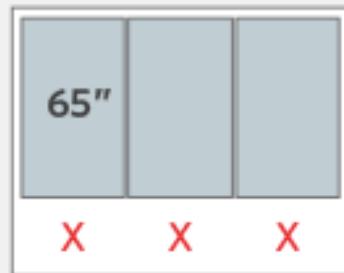


Revenue per Glass Generation

GEN 8.5



Most efficient for 55"



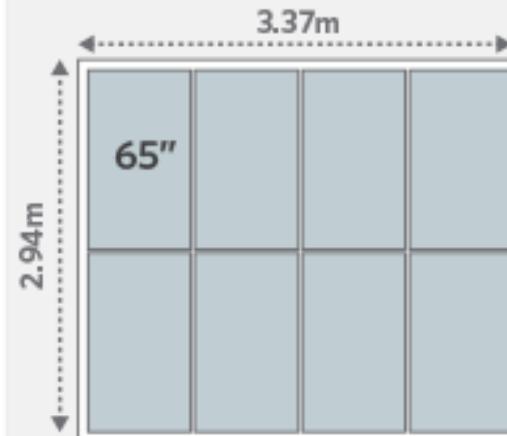
Not efficient for 60"+

55" UHD panel ASP: \$180

Revenue/substrate: \$1080

Revenue/area: **\$196/m²**

GEN 10+



Glass utilization
high for 65"

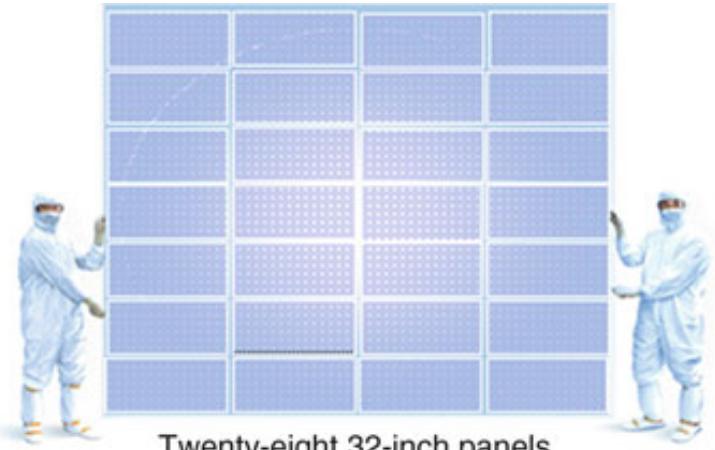
65" UHD panel ASP: \$290

Revenue/substrate: \$2320

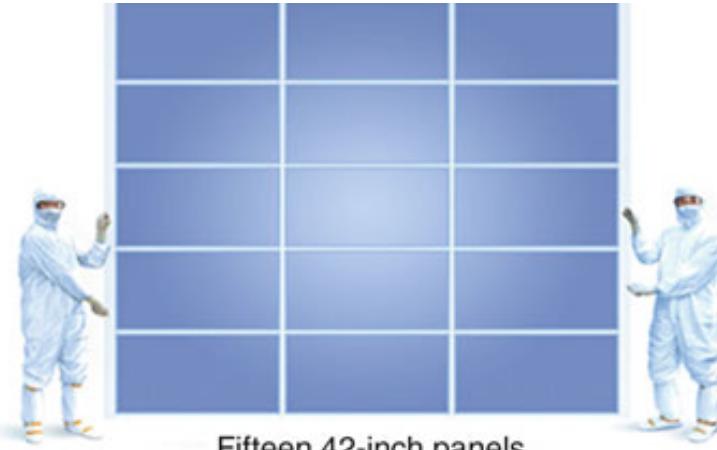
Revenue/area: **\$234/m²**

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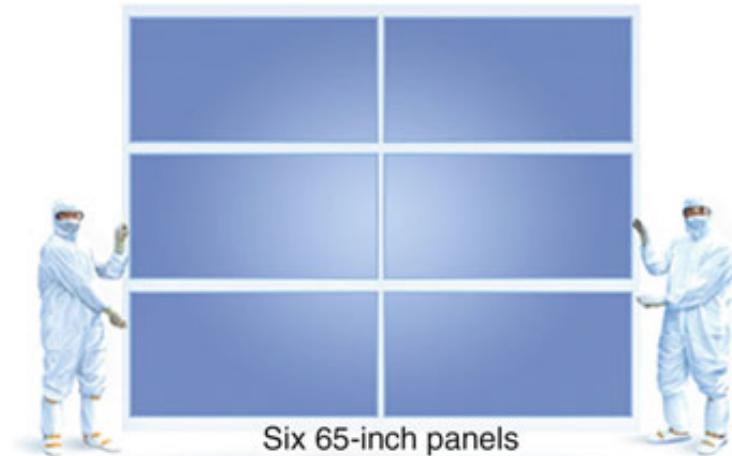
Gen 10 Substrate



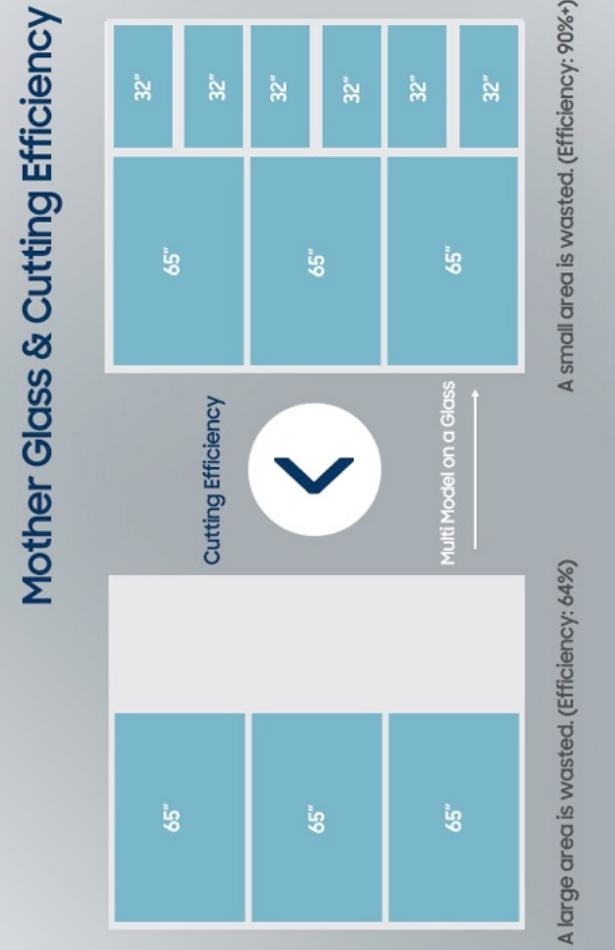
Twenty-eight 32-inch panels



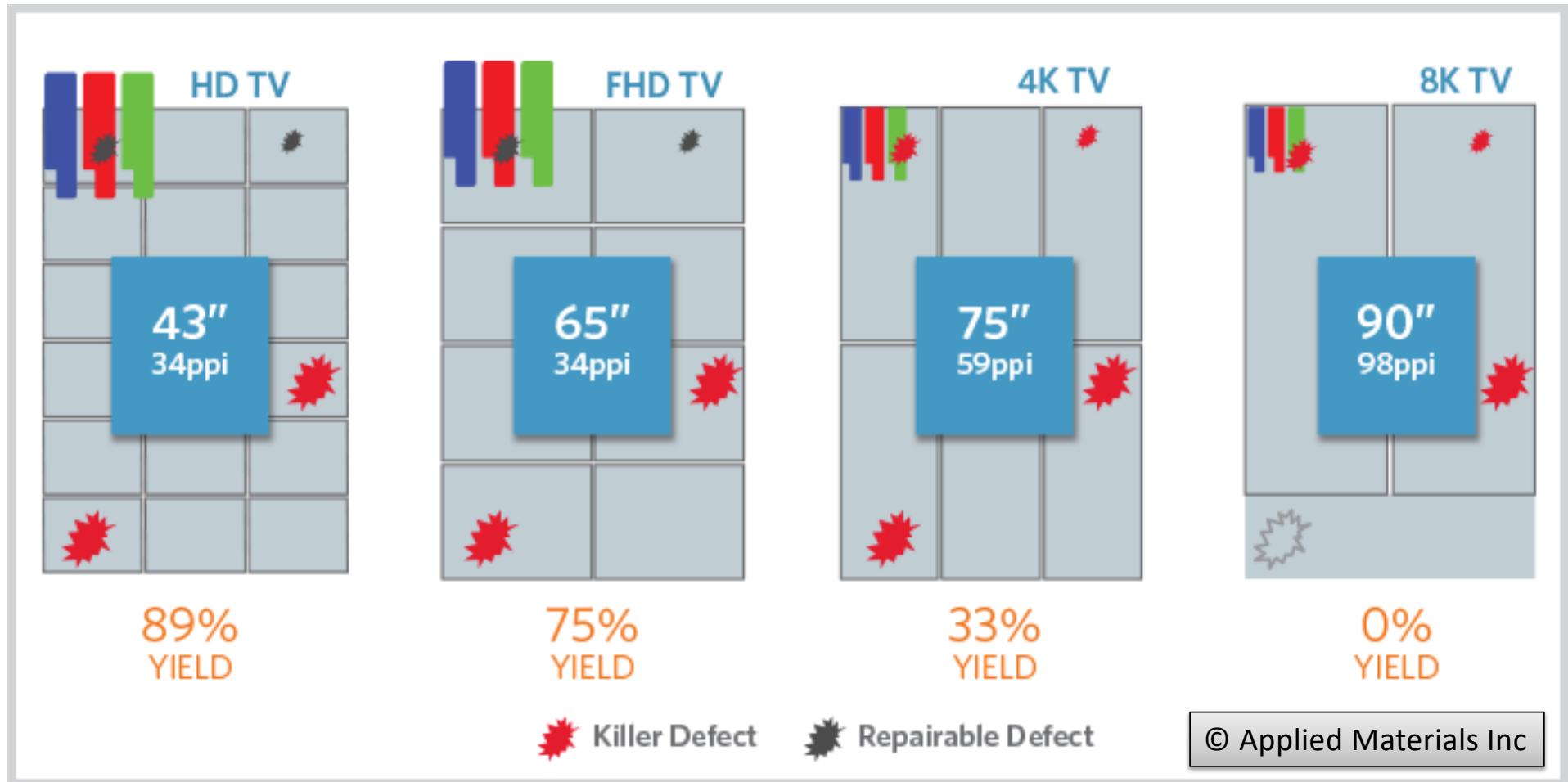
Fifteen 42-inch panels



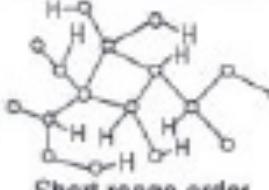
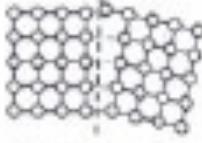
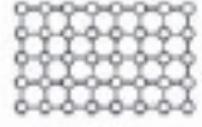
Six 65-inch panels



Evolution of Yield with Time



Qualitative comparison

	a-Si amorphous	poly-Si poly-crystal	c-Si single crystal
Field Effect Mobility μ (cm ² /Vs)	0.5 - 1.0	30 - 300	600 - 700
Crystal Structure	 Short range order H-termination	 Grain boundary	 Perfect
Application	Pixel Switching	Driver Circuit	Driver LSI

Qualitative Comparison of Backplane Technologies

PROPERTY	a-SI:H*	OXIDE	LTPS
Cost	thumb up	thumb up	thumb down
Scalability	thumb up	thumb up	thumb down
On current	thumb down	hand out	thumb up
Off current	hand out	thumb up	hand out
CMOS	thumb down	thumb down	thumb up

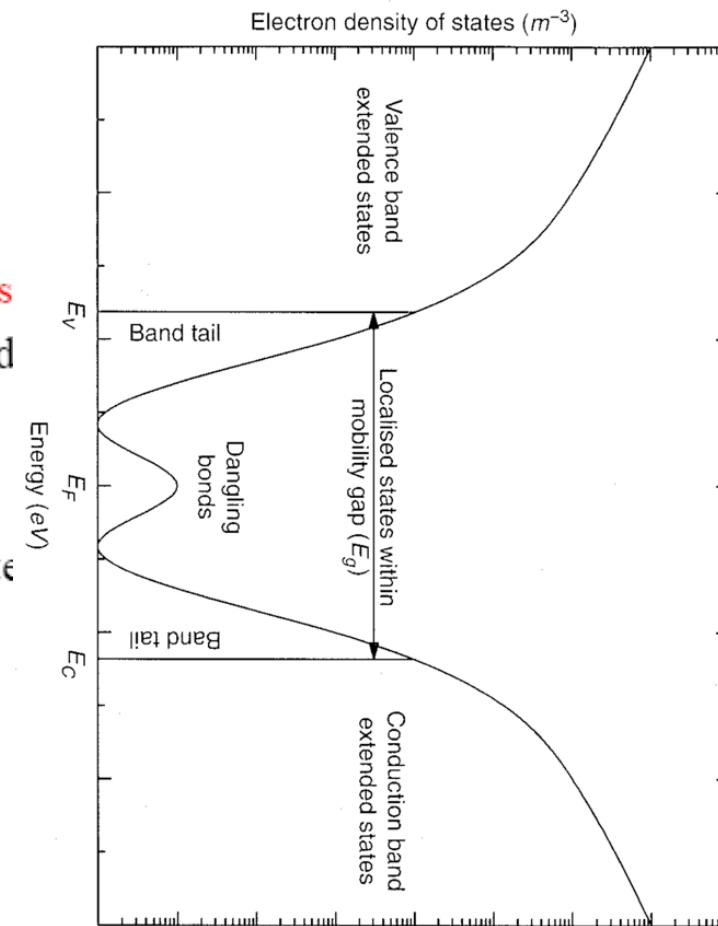
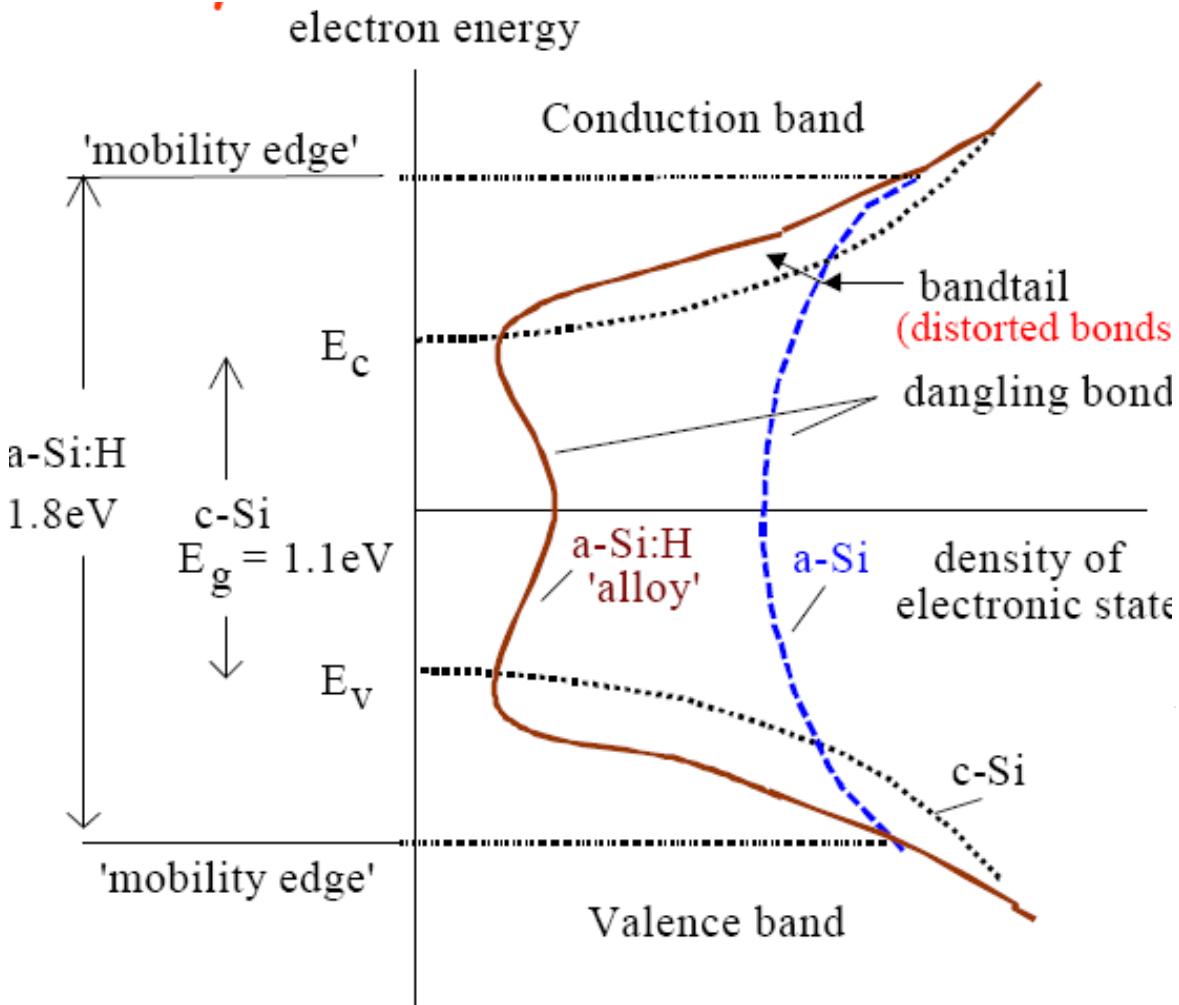
TFT Technology: Advancements and Opportunities for Improvement

John F. Wager

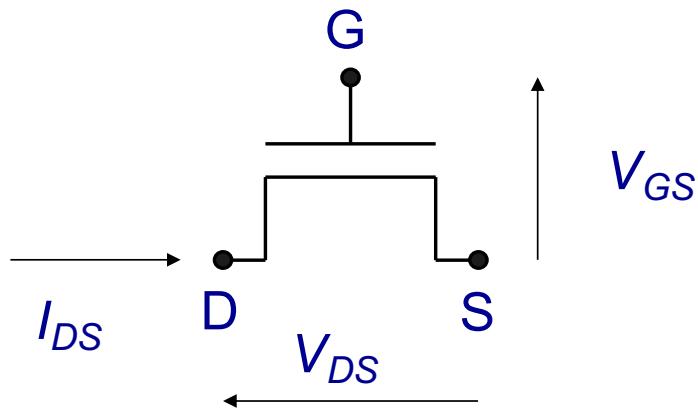
ID Magazine, March 2020

<https://doi.org/10.1002/msid.1098>

Density of states in a-Si

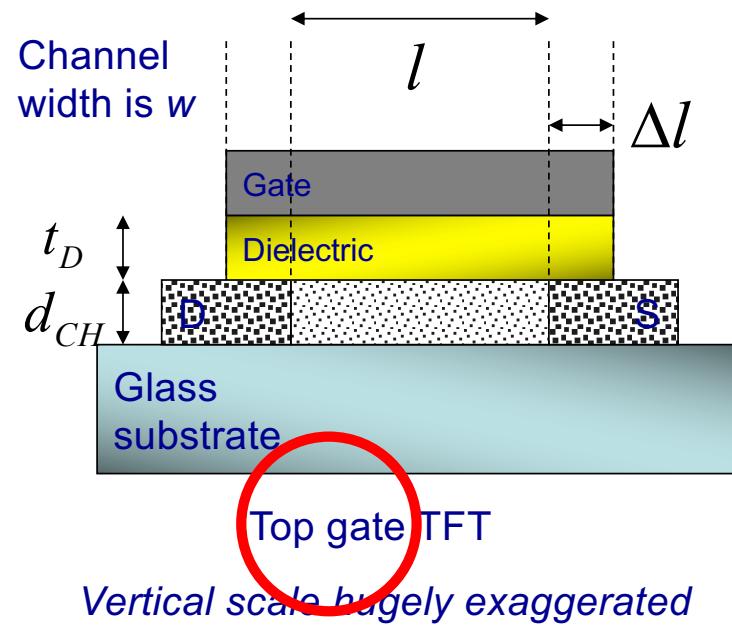


a-Si:H Thin Film Transistor



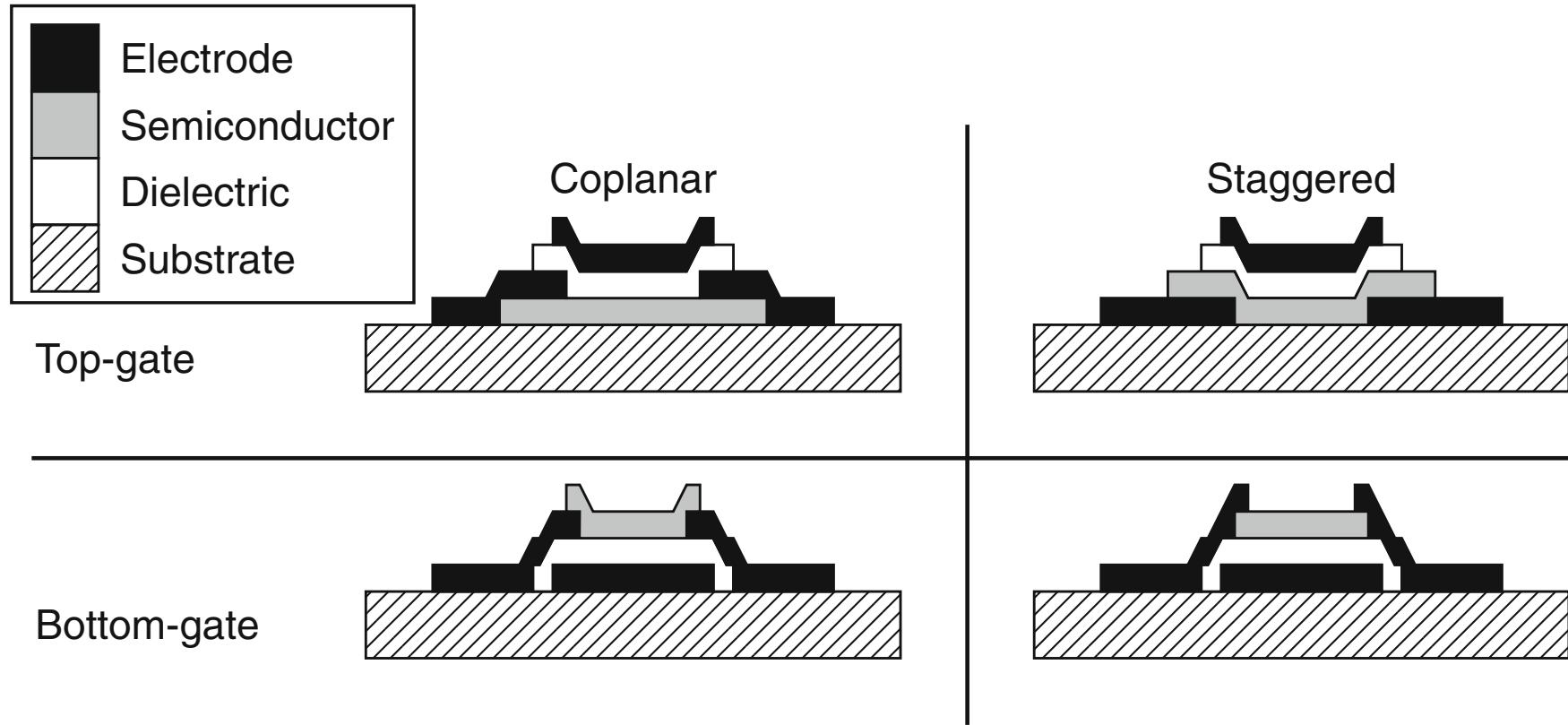
Some similarity in principle to
the operation of
a 3-terminal MOSFET
but

- Much larger dimensions
- Very different materials



MMXXII

Configurations for TFT on glass



Ideal TFT

$$V_{GS} < V_T \ . \ I_{DS} = 0$$

$$V_{GS} - V_T \geq V_{DS}, V_{GS} > V_T \ . \ I_{DS} = \mu C_0 (W/L) \left[(V_{GS} - V_T) V_{DS} - V_{DS}^2 / 2 \right]$$

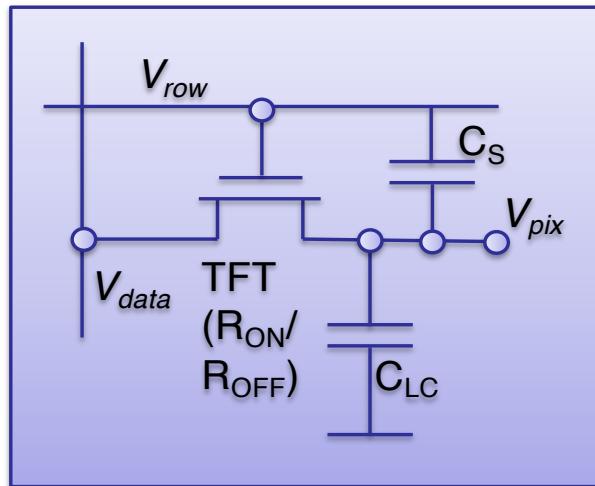
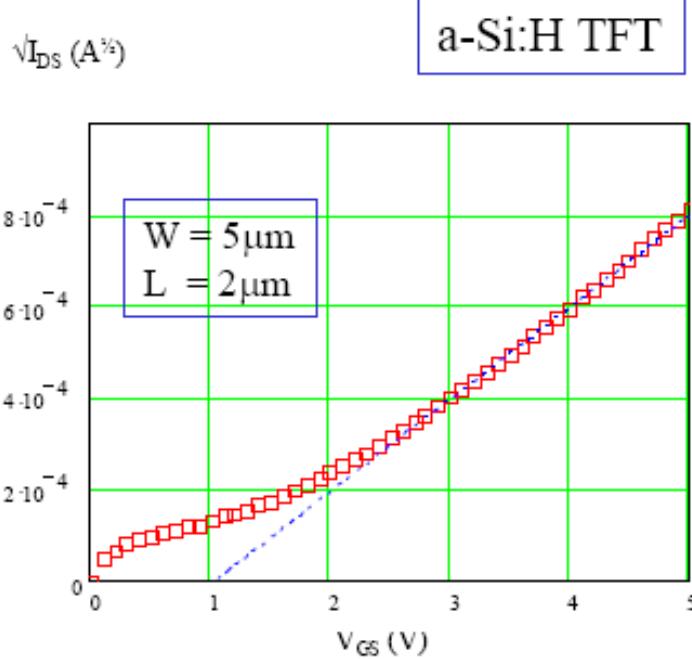
$$V_{GS} - V_T < V_{DS}, V_{GS} > V_T \ . \ I_{DS} = \frac{\mu C_0 (W/L)}{2} (V_{GS} - V_T)^2$$

$$\ . \ C_0 = \epsilon_0 \epsilon_R / t_D$$

$$\ . \ V_T = -en_0 d / C_G$$

Look very similar to I_{DS} equations for a MOSFET

Practical TFT



In practice

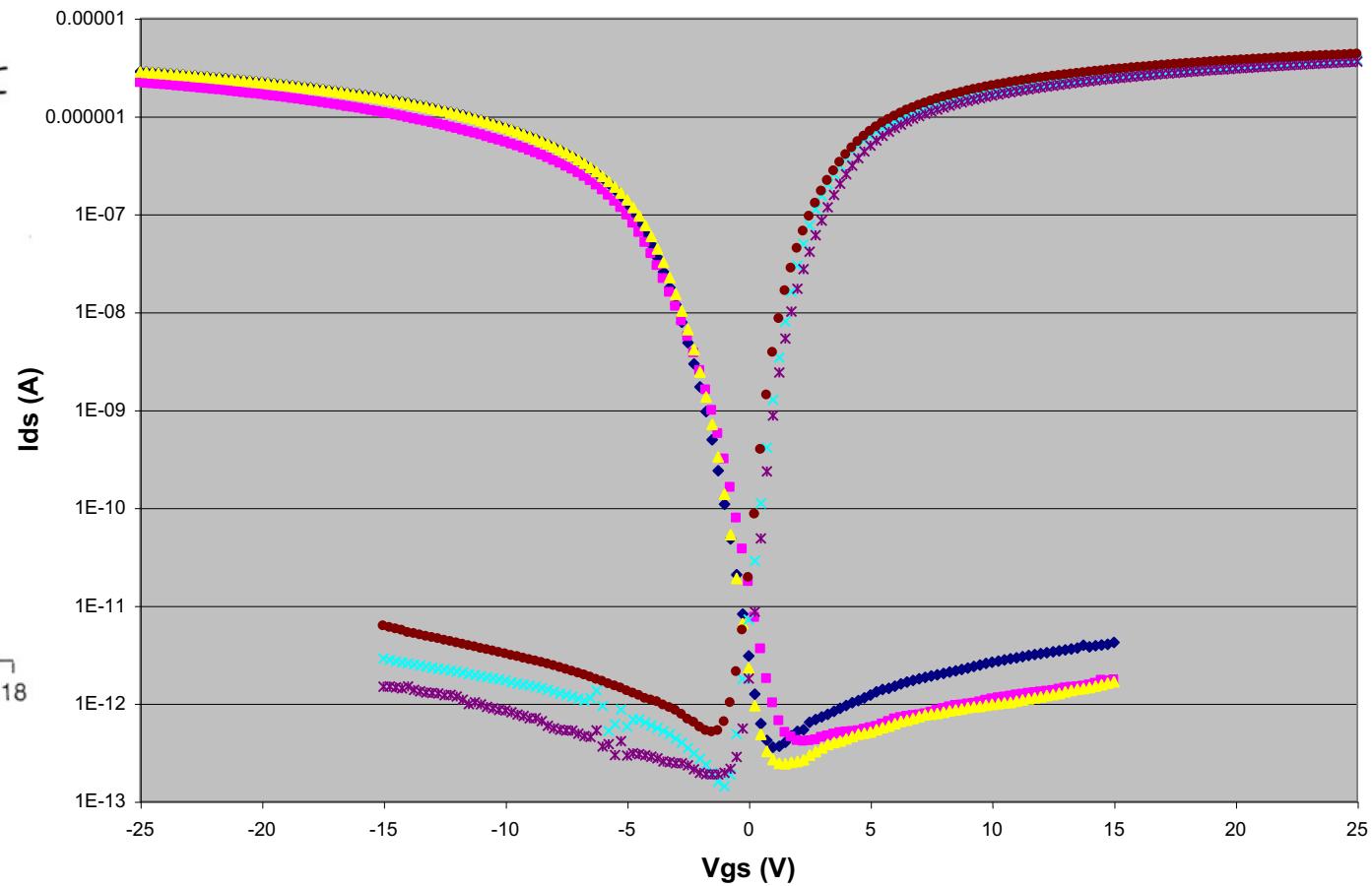
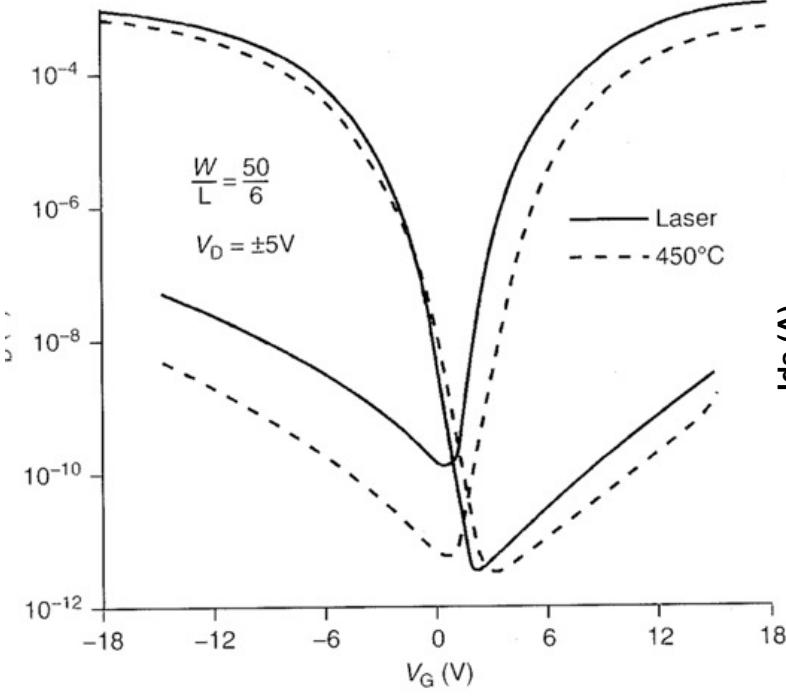
$$I_{OFF} = \frac{W}{L} \frac{V_{DS}}{R_{CH,OFF}}$$

and from

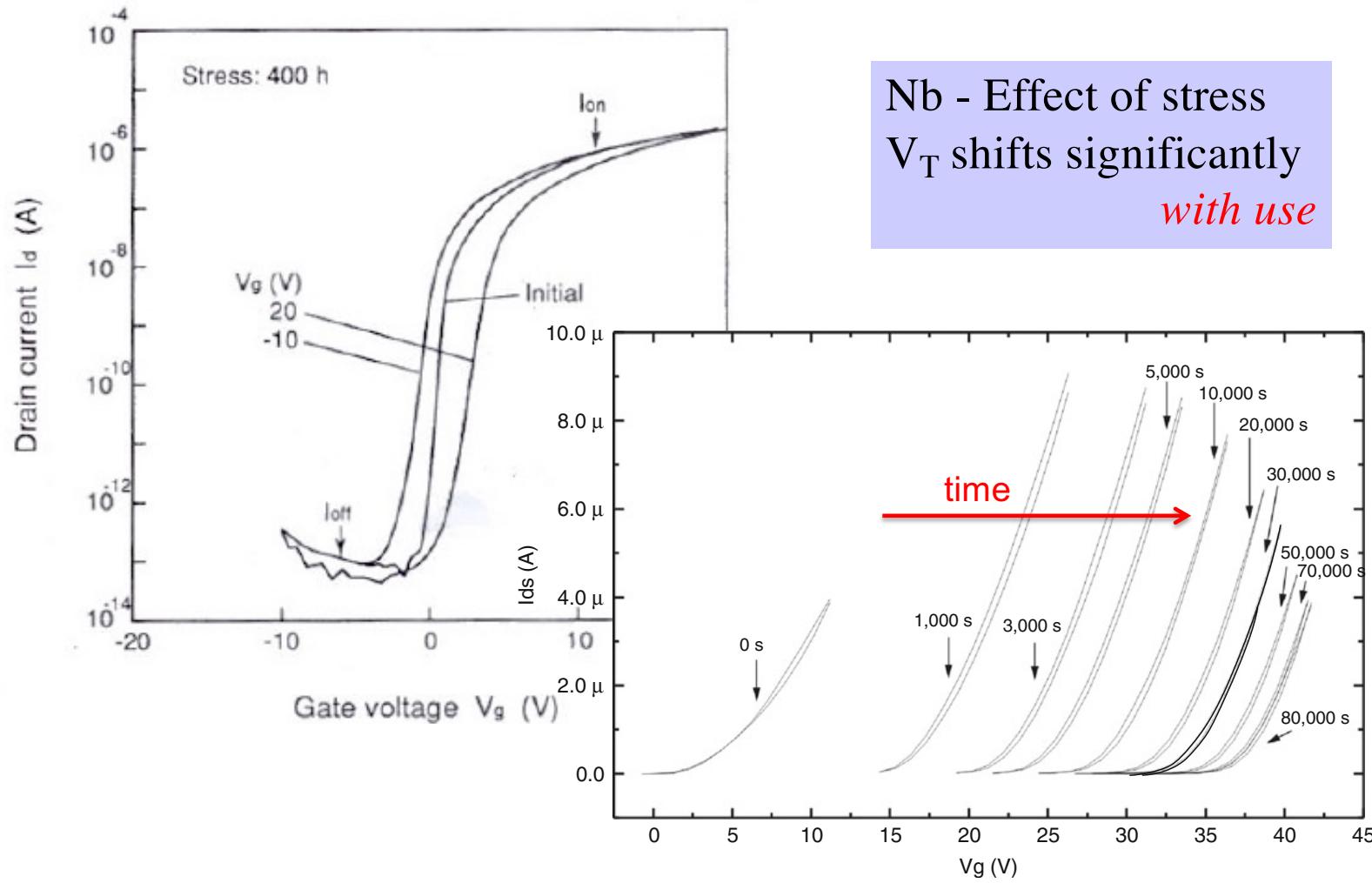
$$\sqrt{I_{DS}} = M(V_{GS} - V_T)$$

$$\mu = M^2 2 l d_{CH} / \epsilon_0 \epsilon_r w$$

Example poly-Si TFT Characteristics



Example α -Si TFT Characteristics



Nb - Effect of stress
 V_T shifts significantly
with use

Pixel constraints on TFT

$$T_{ROW_ADDRESS} = 5T_{RC}$$

$$T_{FRAME} / N = 5R_{ON}(C_{LC} + C_s)$$

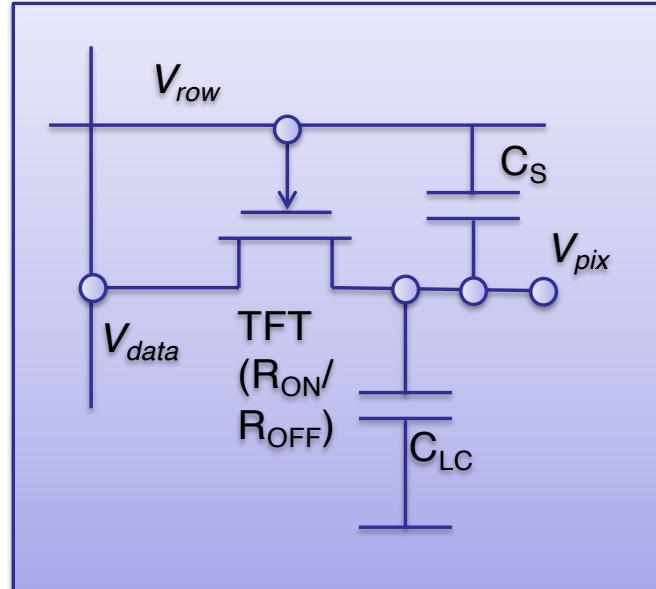
$$R_{ON} = \frac{T_{FRAME}}{5N(C_{LC} + C_s)}$$

ensures that C charges to within 1%

$$\begin{aligned} T_{OFF} &= R_{OFF}(C_{LC} + C_s) \\ &= T_{FRAME} / 0.01 \end{aligned}$$

$$R_{OFF} = \frac{100T_{frame}}{(C_{LC} + C_s)}$$

ensures that C leaks less than 1%



$$\frac{R_{OFF}}{R_{ON}} \geq 500N$$

ensures that the pixel voltage is within
2% of the intended value

Backplane Technology Comparison

Table 2 Comparison among representative TFTs. This table is modified from that taken from J. K. Jeong (Jeong 2007)

	a-Si:H TFT	Poly-Si TFT	TAOS TFT
Generation	>10G	6.5G(LTPS)/8G (HTPS)?	8.5G
Channel	a-Si:H	ELA LTPS/SPC HTPS	a-InGaZnO ₄
TFT mask steps (LCD/OLED)	4–6/6–7	5–9	4–6
Mobility (cm²/Vs)	<1	30–100 (or larger)	1–30 (100?)
TFT uniformity	Good	Poor/better	Good
Pixel TFT	NMOS	PMOS, CMOS	NMOS
Pixel circuit (OLED)	Complex (e.g., 4 T + 2C)	Complex (e.g., 5T + 2C)	Simple (2 T + 1C) in prototypes Several T in products
Cost/yield	Low/high	High/low	Low/high
TFT reliability	Poor	Good	Good
V_{th} shift	>30 V	<0.5 V	<1 V
Stability	Poor	Good	Better than a-Si Large negative ΔV_{th} by light illumination
Circuit integration	No	Yes	Yes
Process T	150–350 °C	250–550 °C	RT – 450 (600) °C
Display mode	LCD, e-paper	LCD, OLED	LCD, OLED, e-paper
Substrate	Glass, metal, plastic	Glass, metal, plastic	Glass, metal, plastic

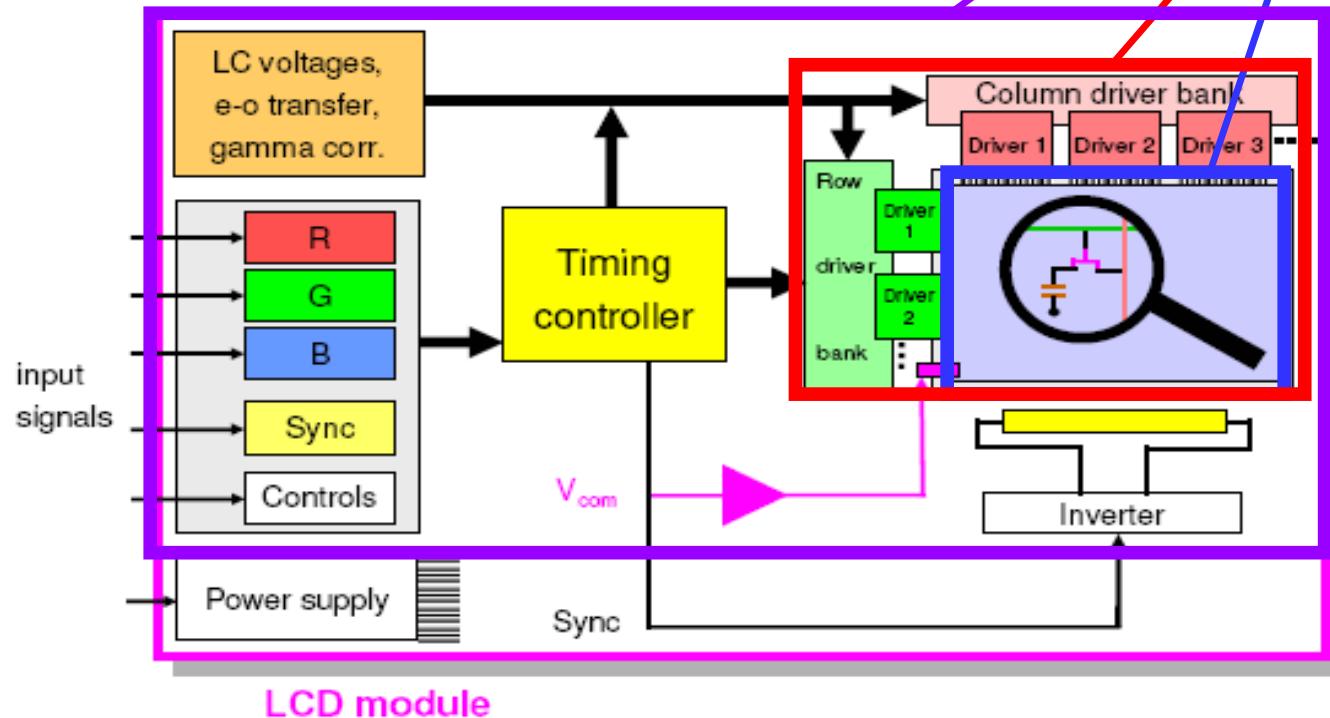
Intended for qualitative comparison

AM LCD Module (including backlight)

Integration on chip capability of CMOS for microdisplay

Integration on glass capability of LTPO

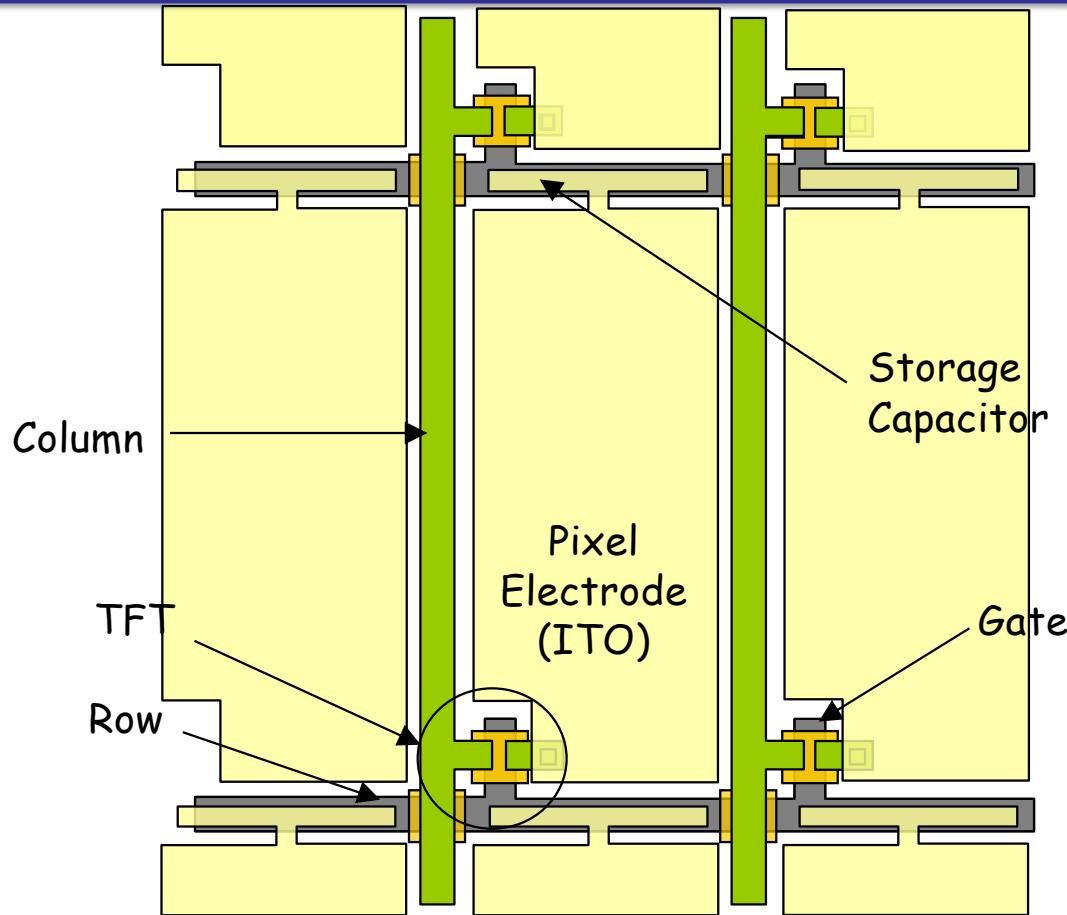
Integration on glass capability of amorphous silicon



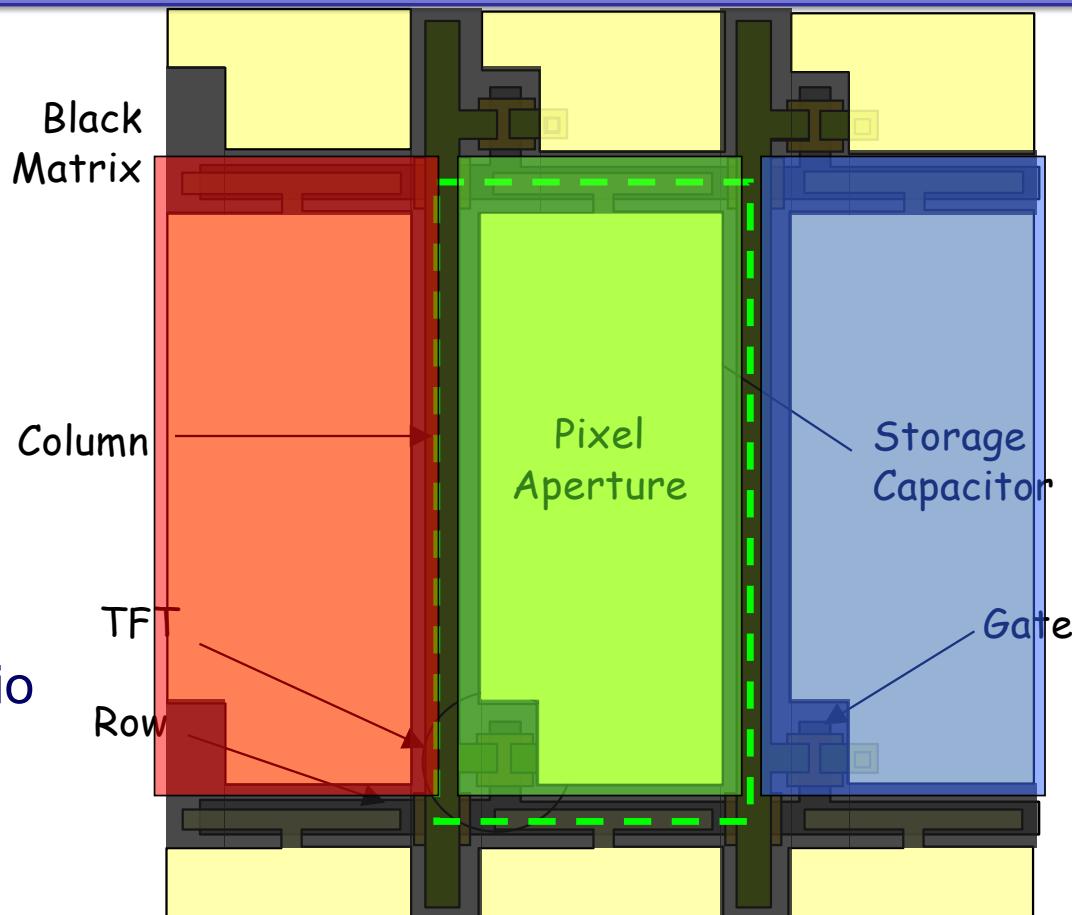
TFT AMLCD pixel layout

With all that area available in the pixel

-why only 1 TFT stuck in the corner of the pixel?



TFT AMLCD pixel layout



Maximize Aperture ratio
= aperture / footprint

Means

Maximize aperture

Means

Minimize circuitry & interconnect

a-Si:H TFT Active Plate Process

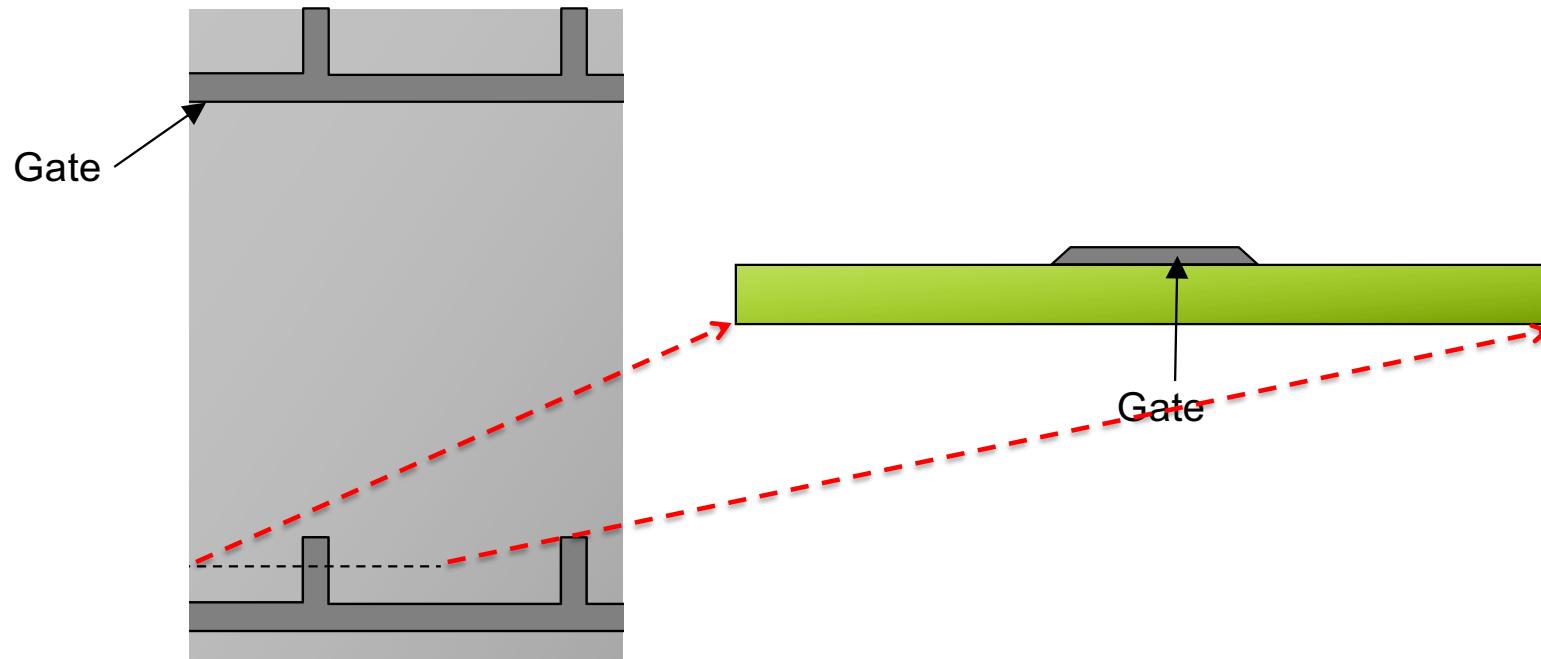
5 mask Back Channel Etched (BCE) TFT Process

- Classic standard in AMLCD industry
- Transmissive display
- Some manufacturers using 4 mask process
- Process split up into photo-lithography mask stages.

Mask 1: Gate

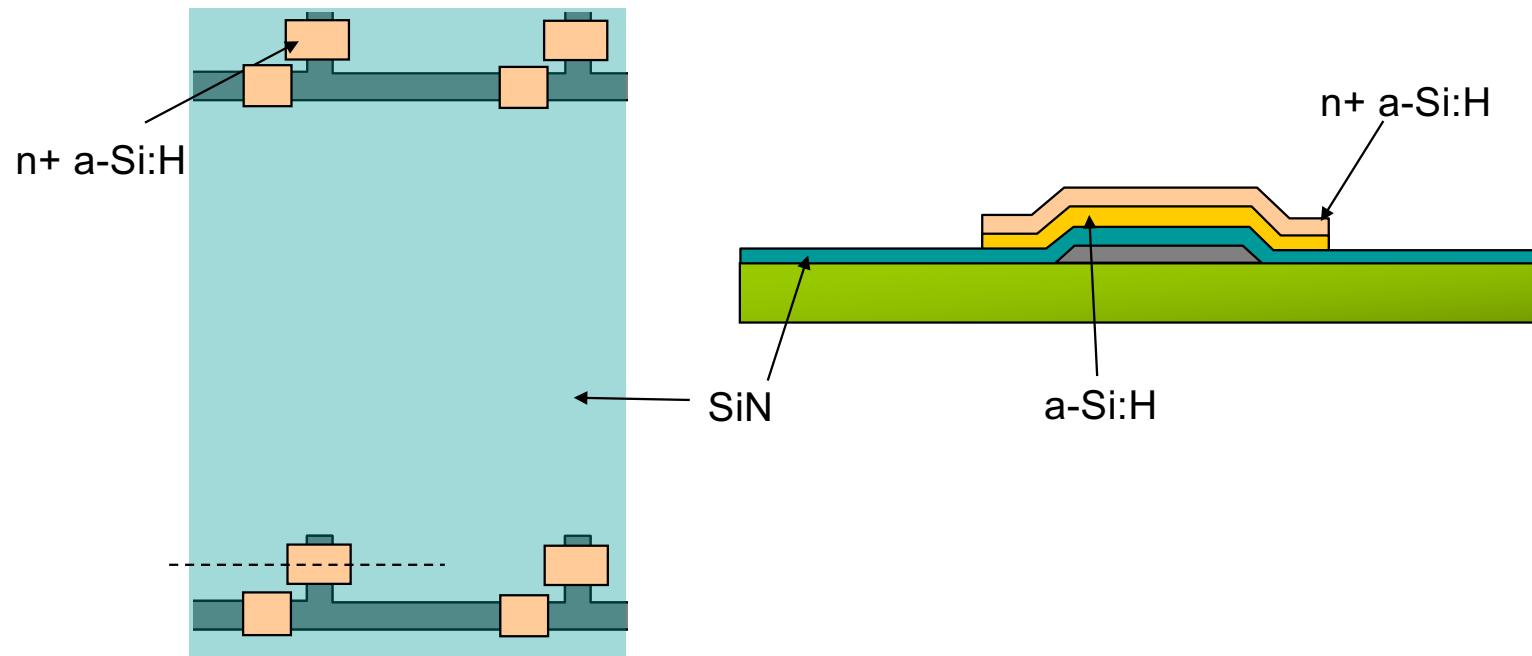
Deposit: Gate metal

Pattern & Etch: Gate metal



Mask 2: Amorphous Si

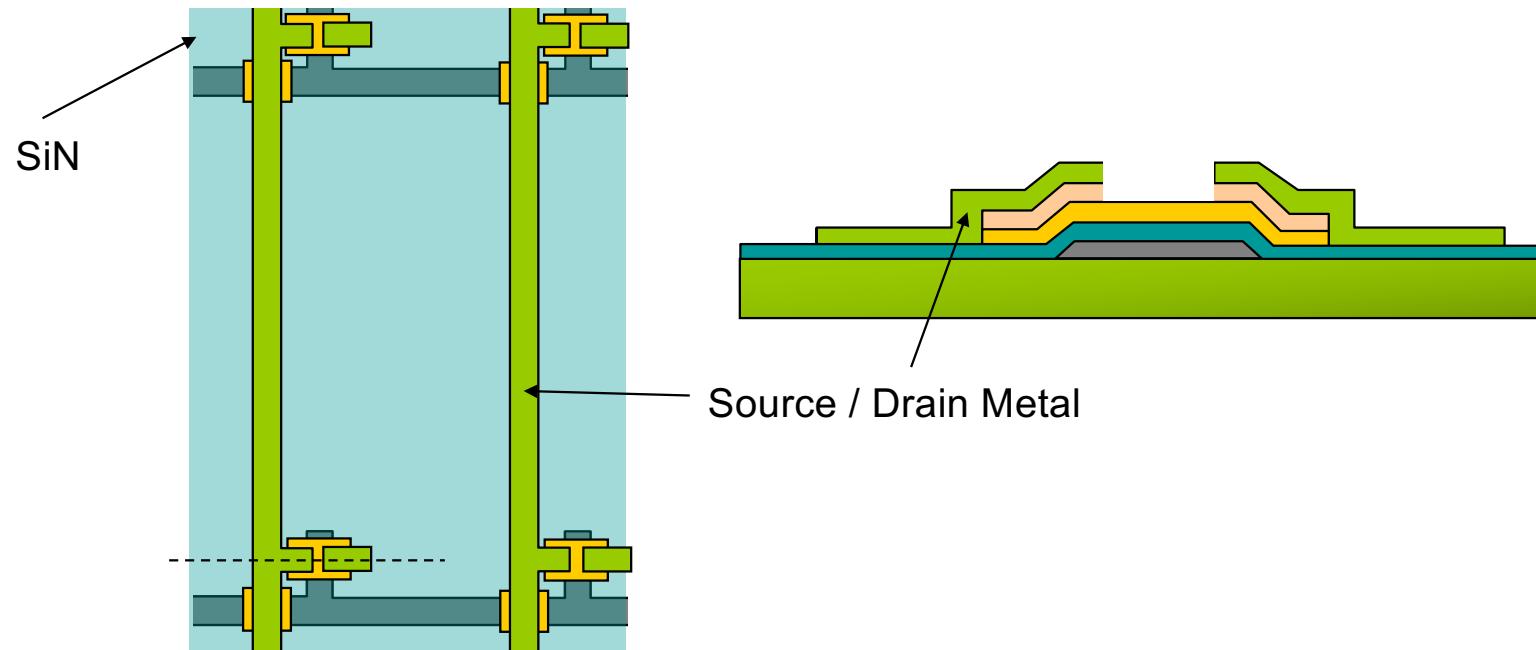
Deposit: SiN, a-Si:H & n+ a-Si:H
Pattern & Etch: n+ a-Si:H & a-Si:H



Mask 3: Source & Drain

Deposit: Source / Drain metal

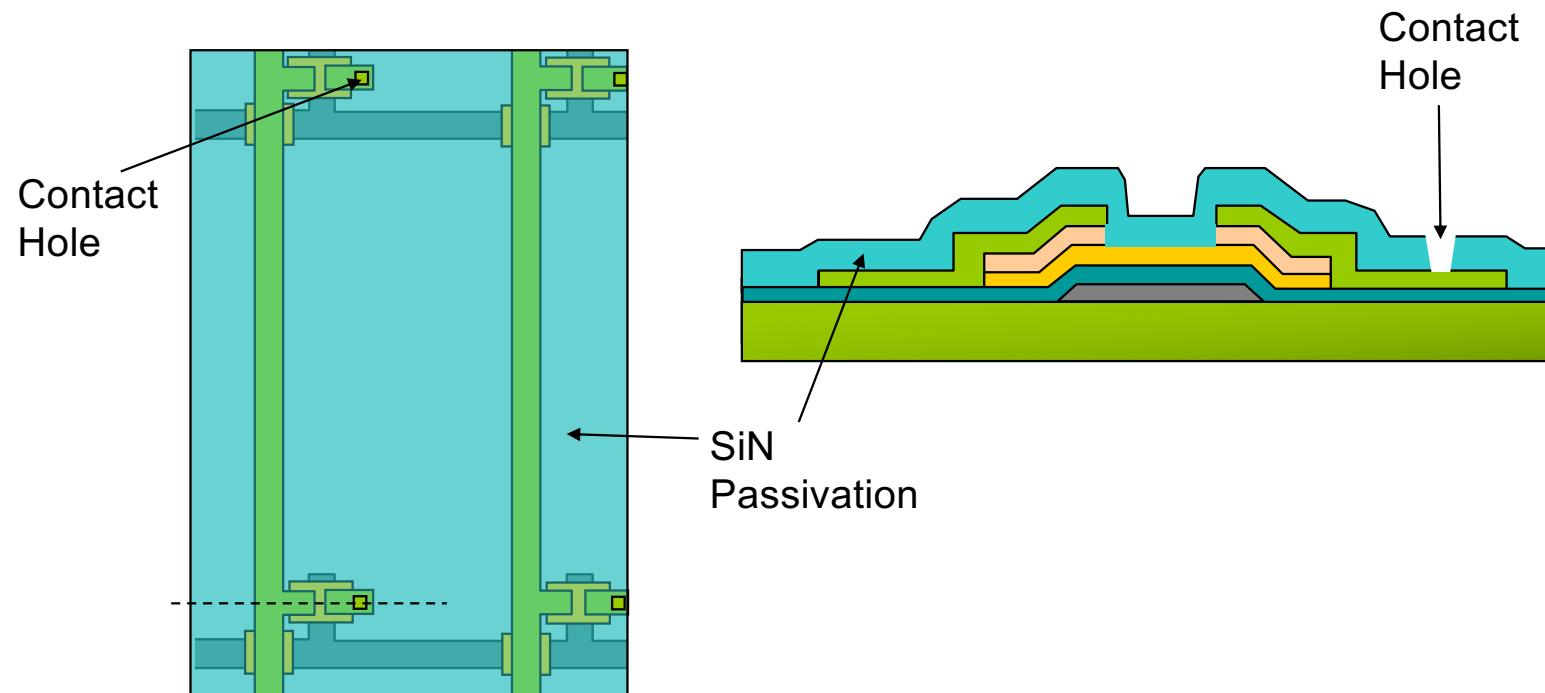
Pattern & Etch: Source / Drain metal & n+a-Si



Mask 4: Contact Hole

Deposit: SiN (Passivation)

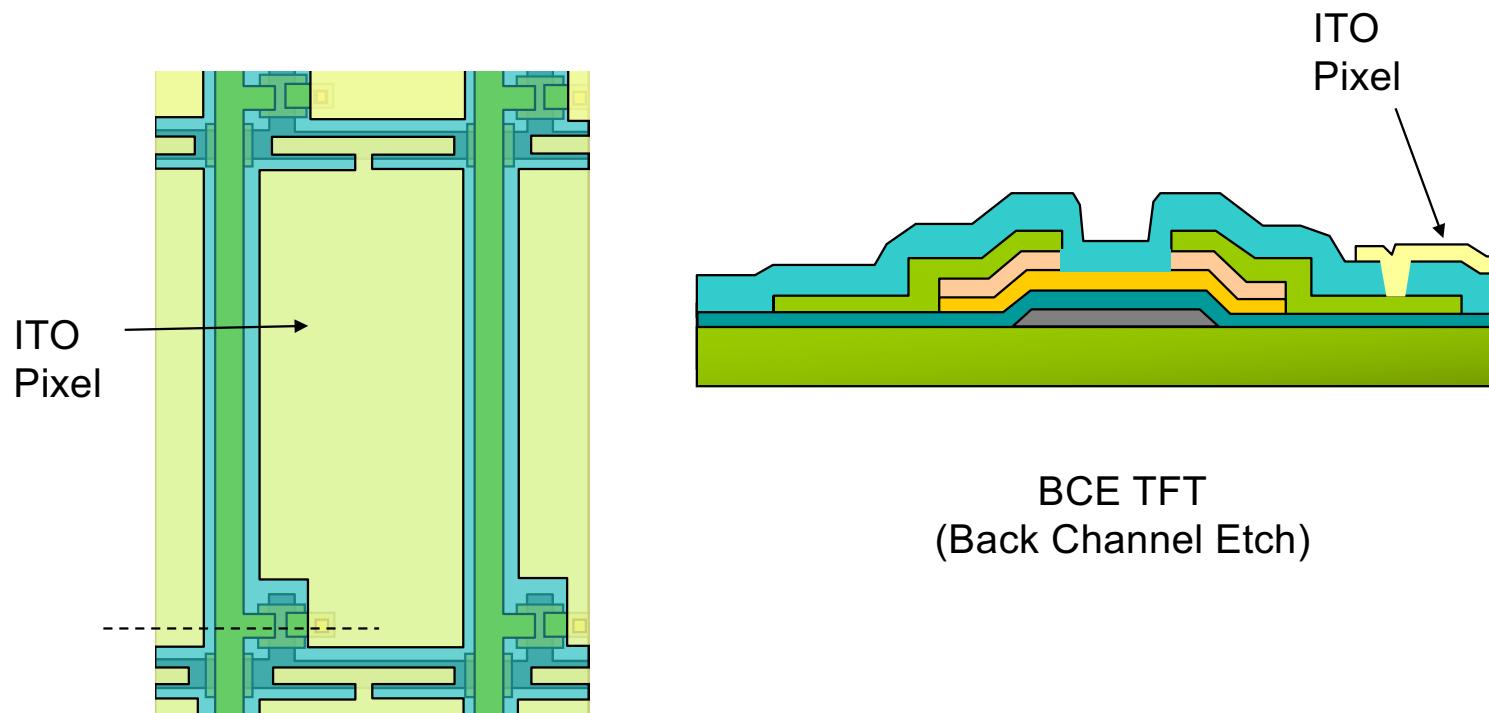
Pattern & Etch: SiN (Passivation) & Gate SiN



Mask 5: Pixel Electrode

Deposit: ITO (Transmissive)

Pattern & Etch: ITO



Polysilicon TFT

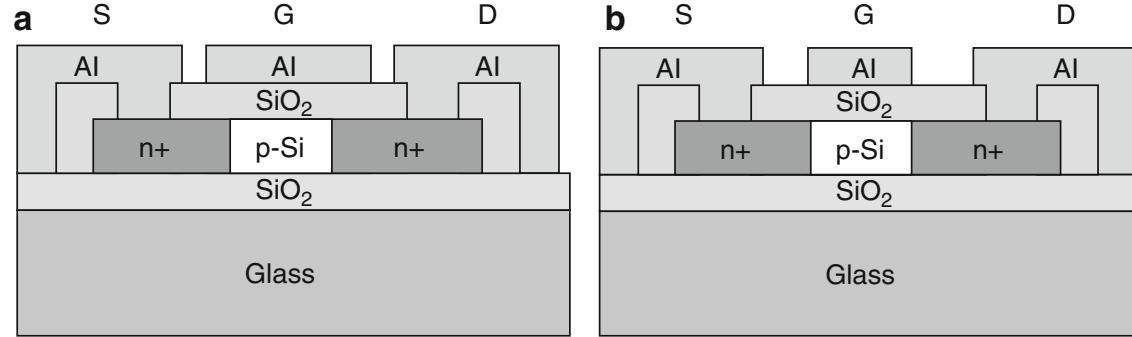


Fig. 6 Cross-sectional diagrams of poly-Si TFT architectures (a) non-self-aligned, (b) self-aligned

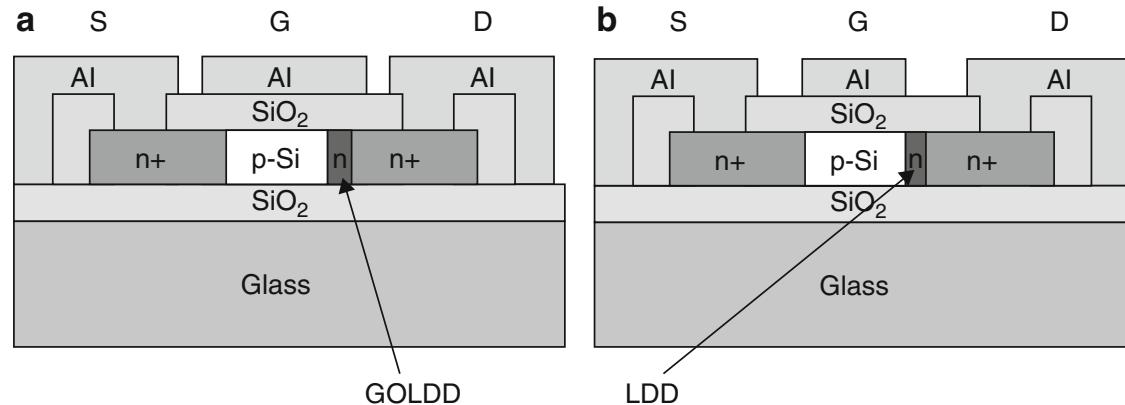


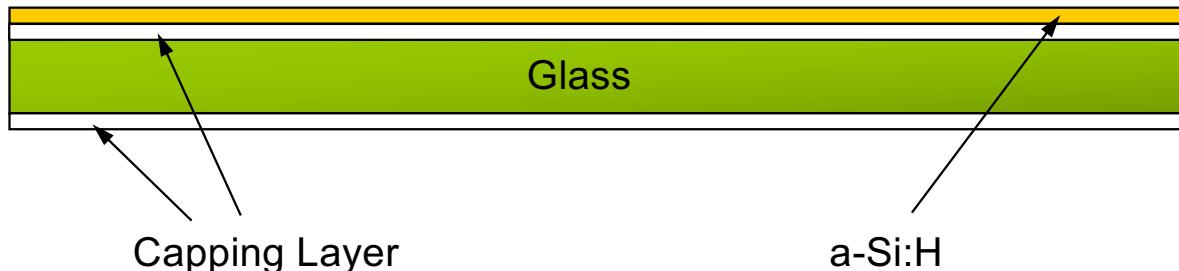
Fig. 10 Cross-sectional diagrams of field relief structures in self-aligned poly-Si TFTs: (a) gate overlapped LDD (GOLDD), (b) LDD

LTPS

- More complex process than for α -Si:H TFTs
 - Form p-Si from α -Si:H e.g. Excimer Laser Annealing
 - Forming both n-type & p-type devices (CMOS)

Deposit dielectric layers on front & back surface of glass & α -Si:H

- SiO_Y capping layers - prevents contamination from glass
 - acts as a heat buffer during laser crystallisation of α -Si:H



LTPS

Dehydrogenate – remove hydrogen from a-Si:H

- Otherwise explosive evolution of H₂ occurs during laser crystallisation
- Could badly damage a-Si/pSi surface
- ~8% H as deposited, < 3% after dehydrogenation

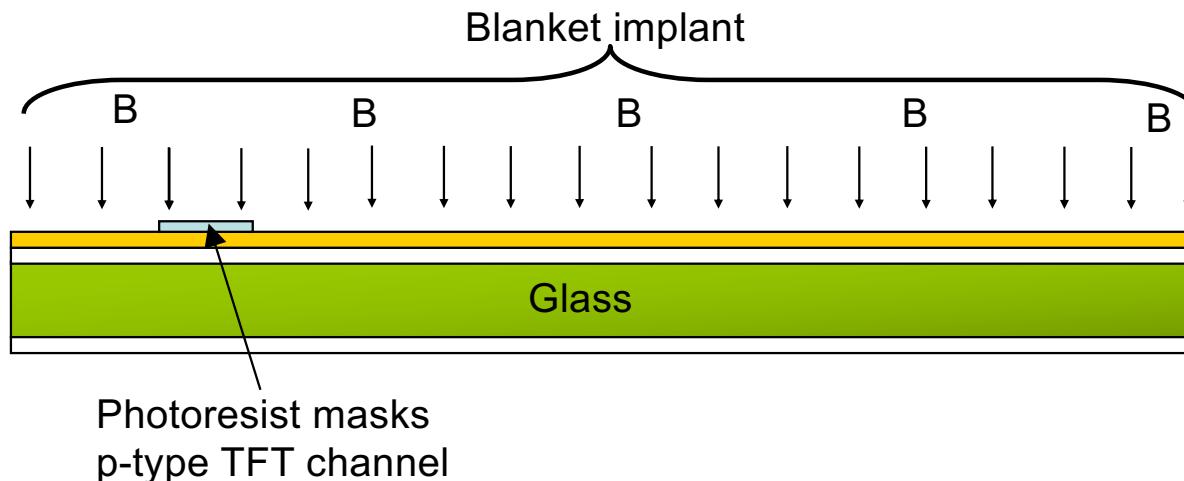


- Thermal anneal: 400°C – 450°C for ~1-2 hours, in pure N₂

Mask 1: Low Ion Implantation Dose

Adjustment of TFT threshold voltage V_t

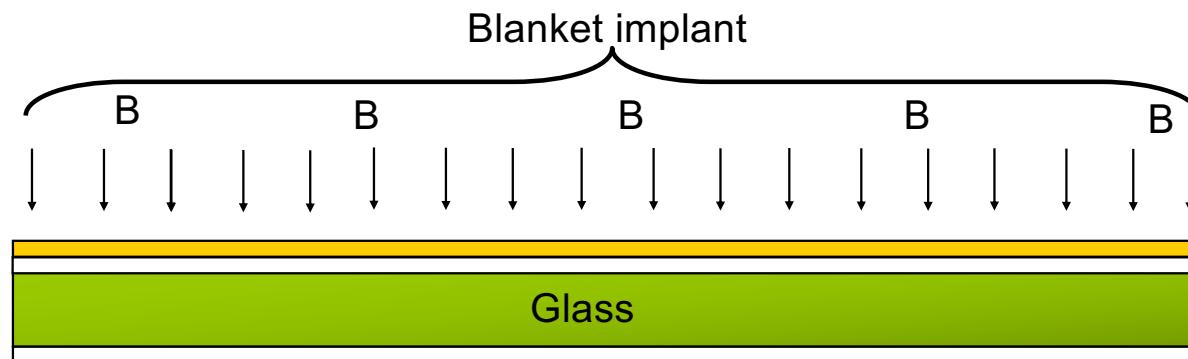
- Boron (B)
- Different adjustment required for n-type & p-type TFTs
- e.g. mask p-channel TFTs (in peripheral circuits) by photoresist



Blanket Implant

Blanket Ion Implantation

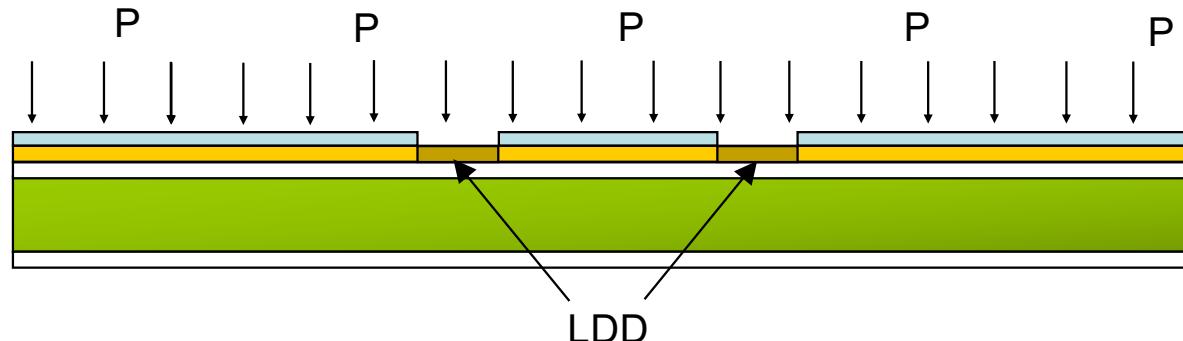
- Allows adjustment of both n-type & p-type TFT threshold voltages V_t
- B implant



Mask 2: Lightly Doped Drain (LDD)

n-type p-Si TFTs need LDD to reduce E-field

- Hot carrier injection – high electric field
- Causes high leakage current
- Not required for p-type



- LDD acts as a field relief region

Laser Crystallisation then Mask 3: PolySi Island

- Substrate cleaned – a-Si surface
- Excimer Laser Anneal
 - Crystallisation



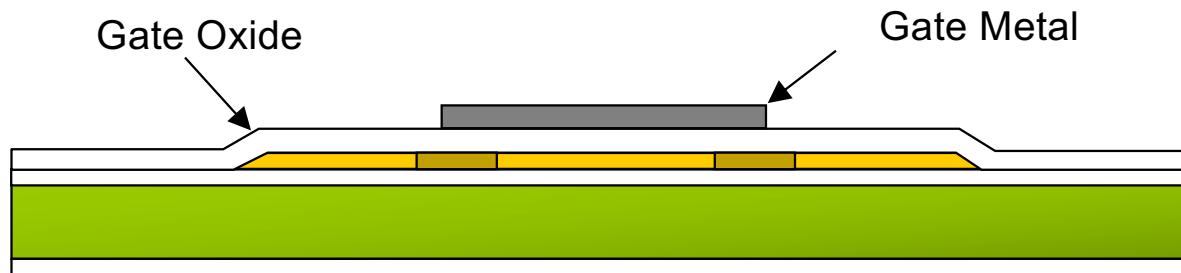
Dry etch to form p-Si islands



Mask 4: Gate

Gate oxide deposition

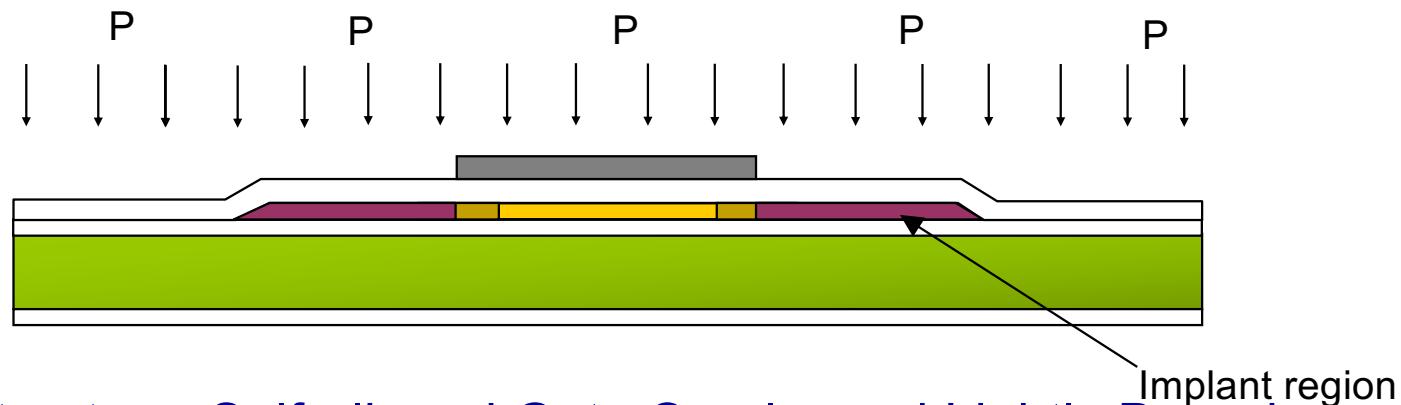
- Gate metal deposition
- Pattern (wet etch)



Mask 5: High Dose S/D Contacts (n-type)

High P implant for n-type TFTs

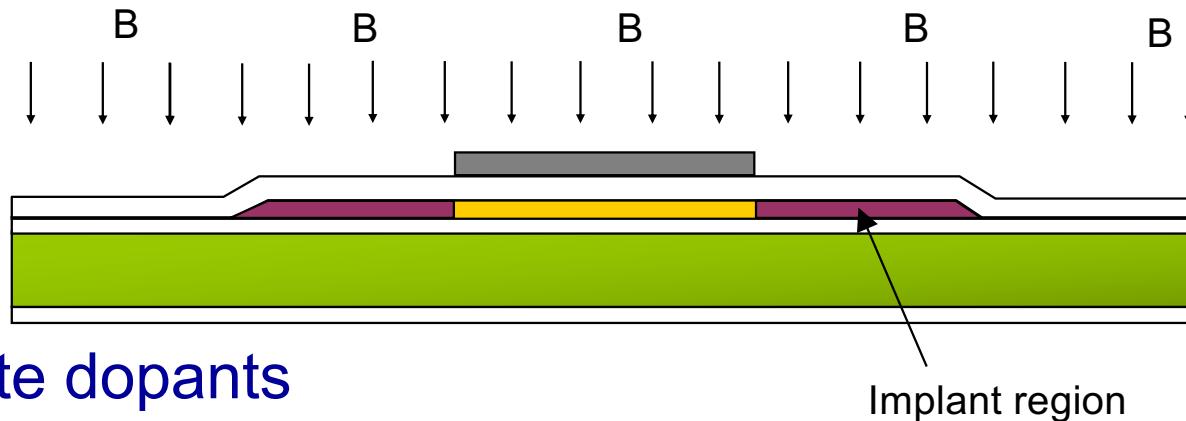
- Uses photoresist mask (not shown) – protects p-type TFTs
- Through gate oxide
- Forming self-aligned Source & Drain contacts



- Structure: Self-aligned Gate Overlapped Lightly Doped Drain (SA-GOLDD)

Mask 6: High Dose S/D Contacts (p-type) then Dopant Activation

- High B implant for p-type TFTs
 - Uses photoresist mask (not shown) – protects n-TFTs



Activate dopants

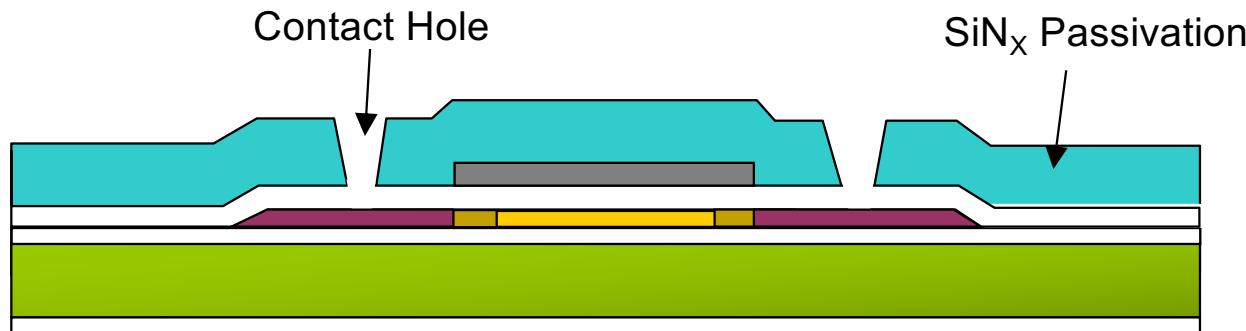
- Furnace: $\sim 450^{\circ}\text{C}$, 1- 2 hours in N_2/H_2
- Excimer Laser Anneal (ELA): Lower E than for crystall'n
 - Through gate oxide layer, do not want re-melting



Mask 7: Contact Holes to Source, Drain & Gate

Deposit SiN_X passivation layer

- Pattern & Etch down to implanted Source & drain regions
 - Wet or dry etch through SiN_X & gate oxide – sloped side walls preferred

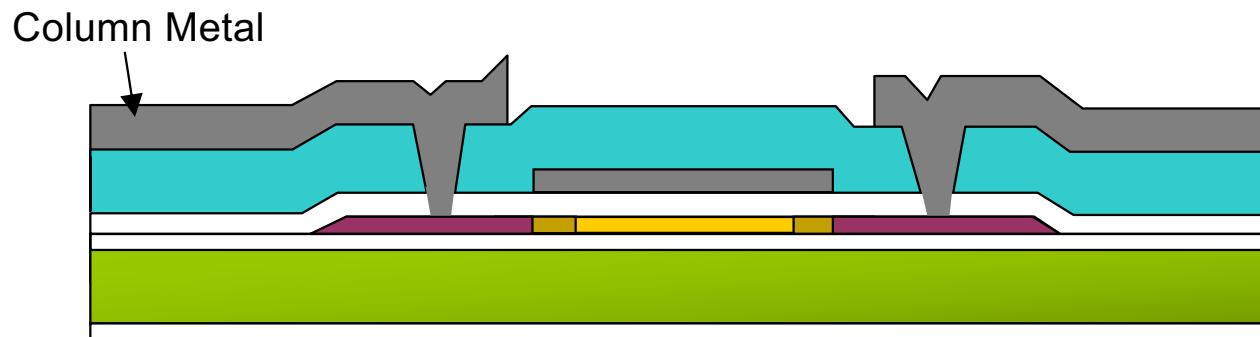


- Etch to gate metal at edge of display (not shown). Etching through SiN_X only required

Mask 8: Column Metal

Deposit Column Metal

- Pattern & Etch: wet etch

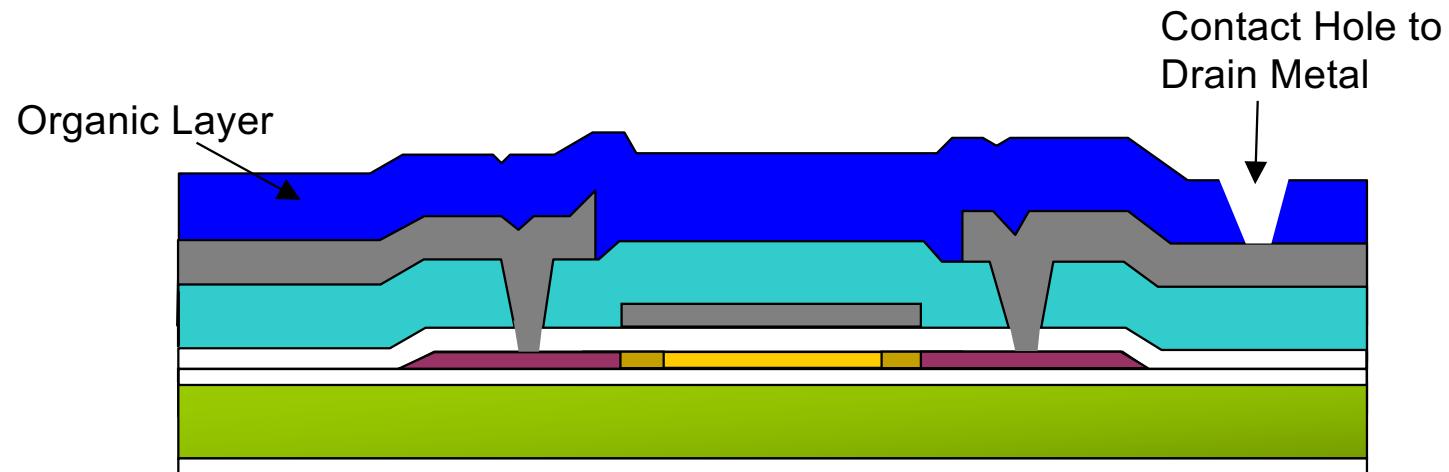


- Hydrogenation in N_2/H_2 , 1-2 hours, $\sim 300^\circ C$

Mask 9: Contact Hole

Thick organic layer

Pattern & Etch: possibly photosensitive

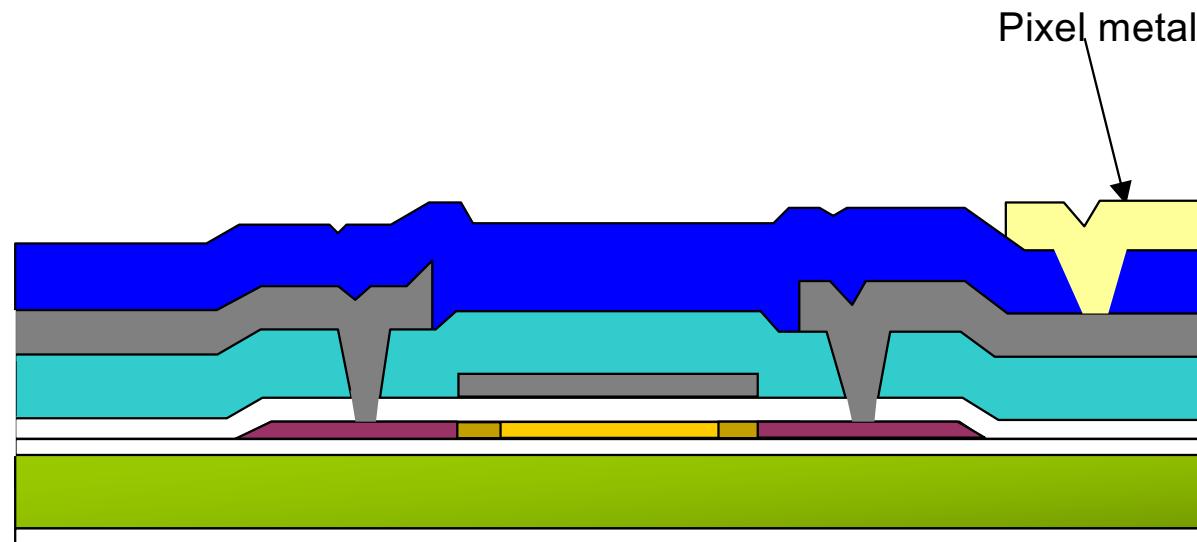


- Organic layer is cleared at edge of display over lead-ins

Mask 10: “Pixel”

Deposit ITO (transmissive)

– Pattern & Etch



IGZO – Top Gate vs Bottom Gate

