THE UNIVERSITY *of* EDINBURGH

Analogue IC Design

FET Amplifiers (Part1)

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FET I-V Summary

- *Shockley* 1st order transistor models (for nFET):

$$I_{ds} = \begin{cases} 0 & V_{gs} < V_t \quad \text{cutoff} \\ \beta\left(V_{gs} - V_t - V_{ds}/2\right)V_{ds} & V_{ds} < V_{gs} - V_t \quad \text{linear} \\ \frac{\beta}{2}\left(V_{gs} - V_t\right)^2 & V_{ds} > V_{gs} - V_t \quad \text{saturation} \end{cases}$$

nMOS I-V Summary

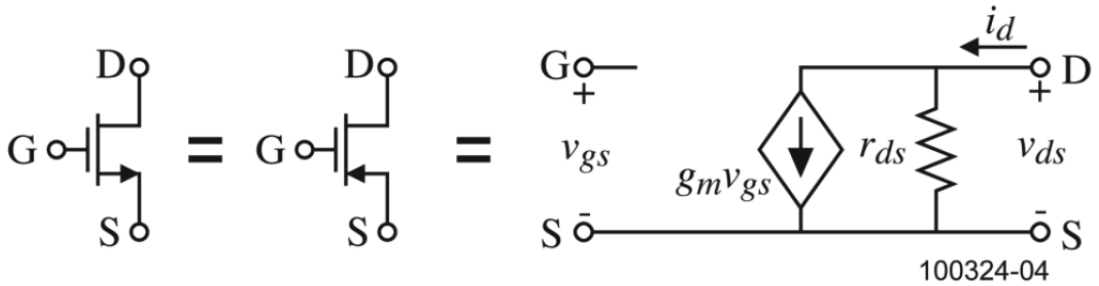
- Basic equations:

$$(v_{DS} \geq v_{GS} - V_T)$$

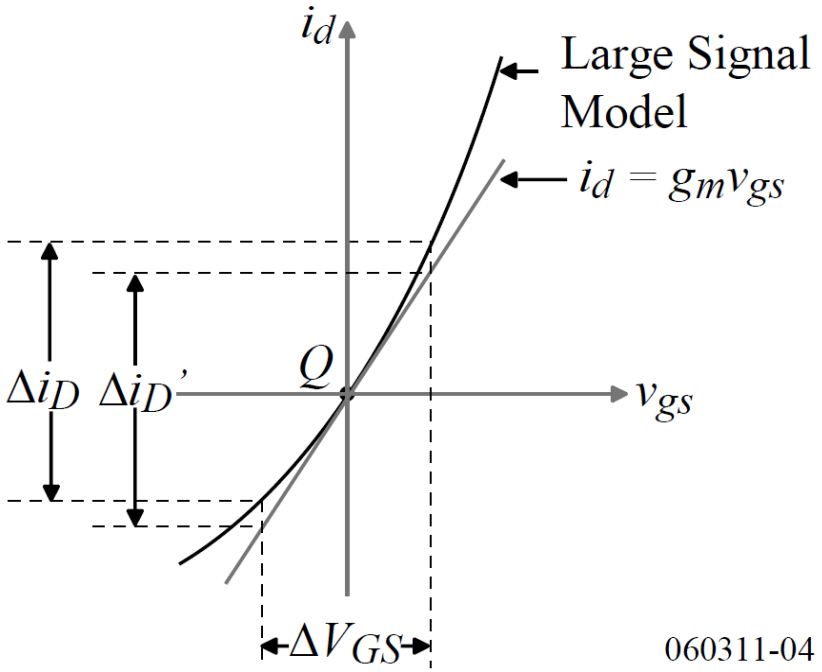
$$i_D = \frac{W\mu_o C_{ox}}{2L}(v_{GS} - V_T)^2(1 + \lambda v_{DS})$$

Transistor Model

- Transconductance for small signal analysis



$$g_m = \frac{\partial i_D}{\partial v_{GS}} = \sqrt{2K' \frac{W}{L} i_D (1 + \lambda v_{DS})}$$

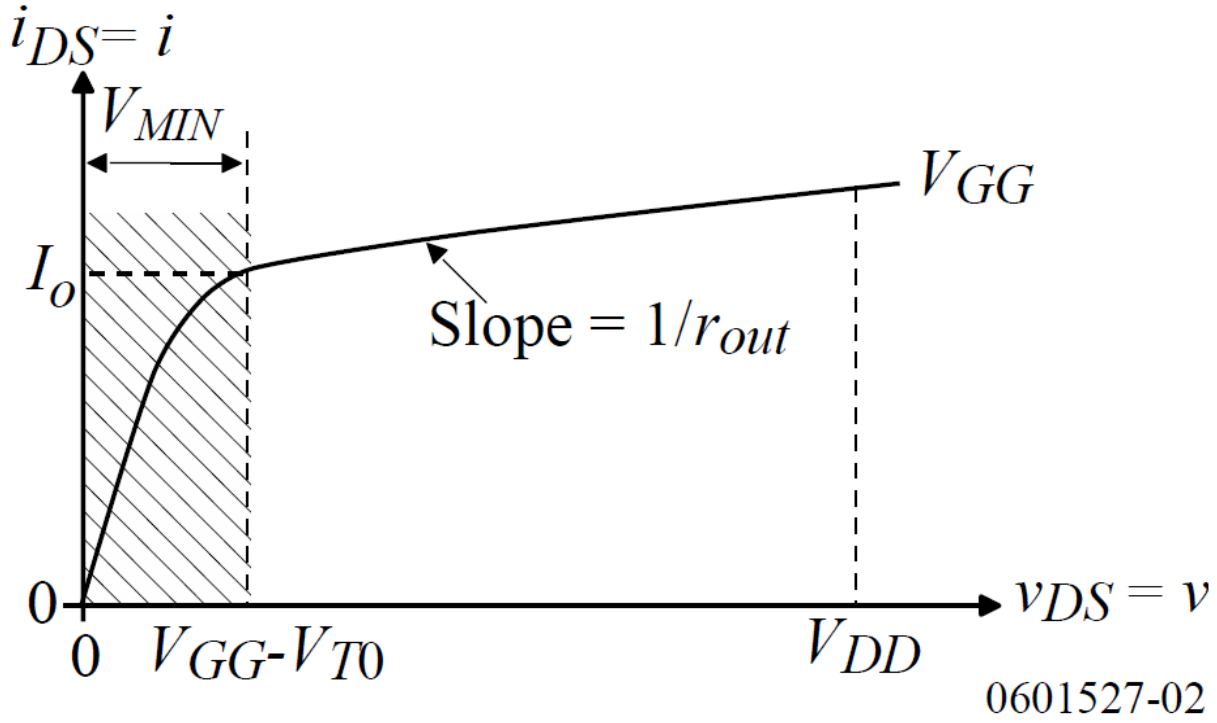


Transistor Model

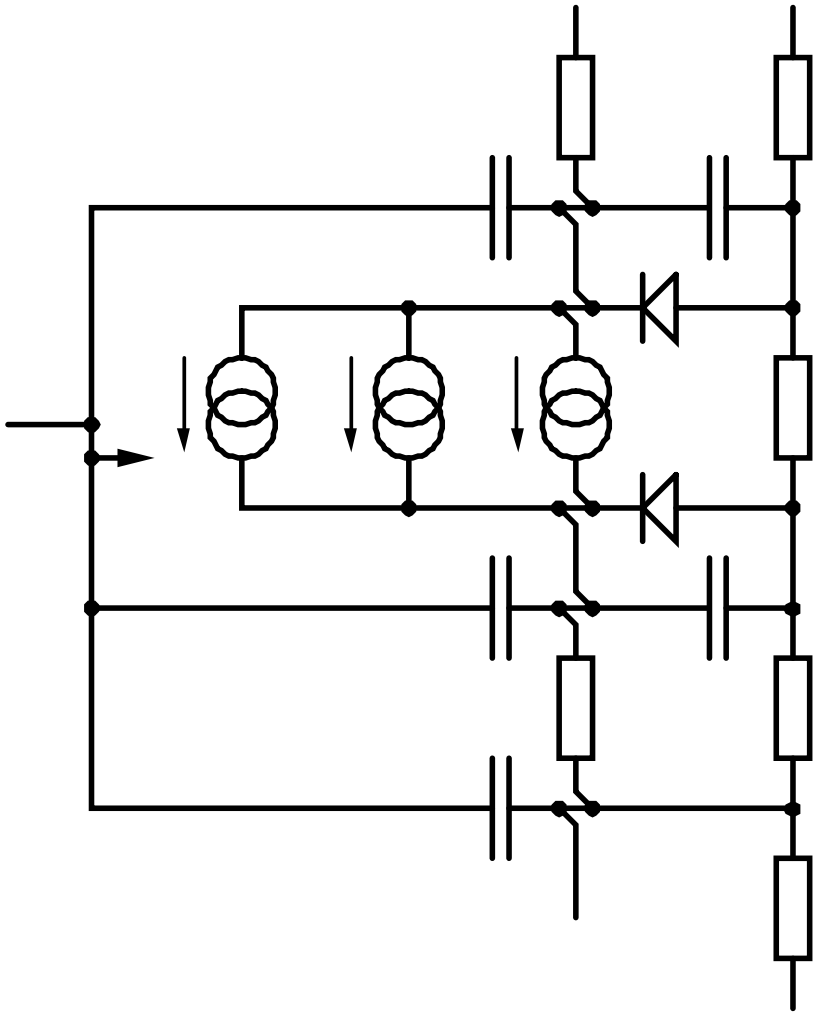
- nFET current source:

$$V_{MIN} = V_{DS}(\text{sat}) = V_{GS} - V_{T0}$$

$$r_{out} = \frac{1}{di_D/dv_{DS}} = \frac{1+\lambda V_{DS}}{\lambda I_D} \approx \frac{1}{\lambda I_D}$$



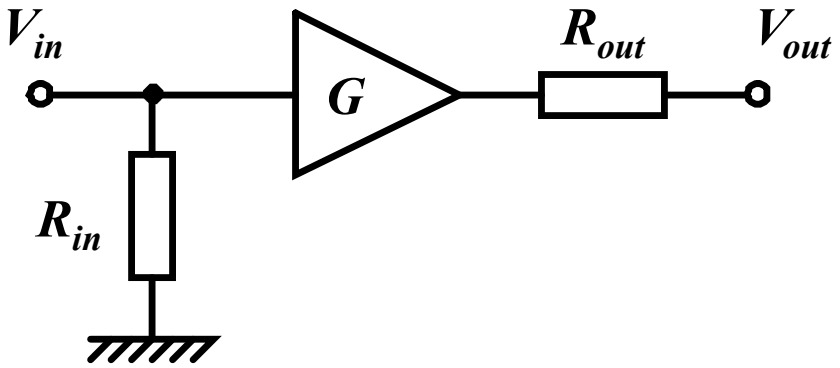
FYI - Better MOSFET Model



- $i_A = v_{GS} \times g_m$
  - the effect of the G-S voltage on i_{DS}
- $i_B = v_{DS} \times g_{DS}$
  - the effect of the D-S voltage on i_{DS}
- $i_C = v_{BS} \times g_{mbs}$
  - the effect of the b-s voltage on i_{DS} … the body effect

Basic Amplifier Model

- This is one of the most useful amplifier models
- R_{in} is the amplifier input impedance (usually infinite for MOS circuits)
- R_{out} is the amplifier output impedance
- G is the amplifier gain, usually negative
- This model, however, is incomplete when used with MOS circuits

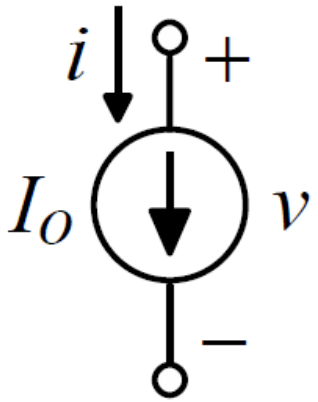


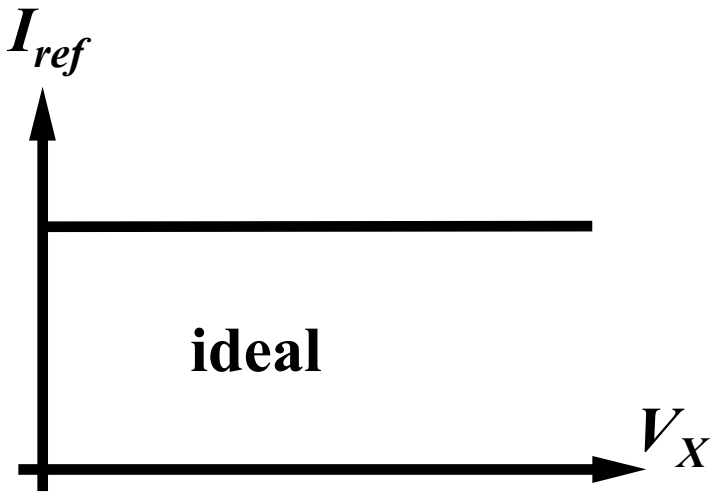
Using Small-Signal Models

- Small-Signal models are used for AC signals *only*
- First assume the DC biasing is OK and, using this, find g_m and g_{DS}
- Only interested in AC signals, so set all DC voltages equal to zero (zero is their *AC* component)
- Large (decoupling) capacitors become short-circuits
- Substitute the small-signal model for any FETS in the circuit, connection for connection
- Analyse using Ohm's Law and Kirchhoff's Laws

Current Source

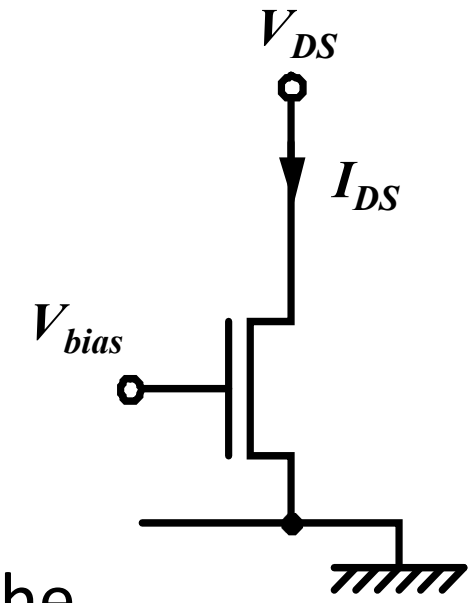
- An ideal current source
- Fixed current I_0
- I_{ref} is independent of V_x





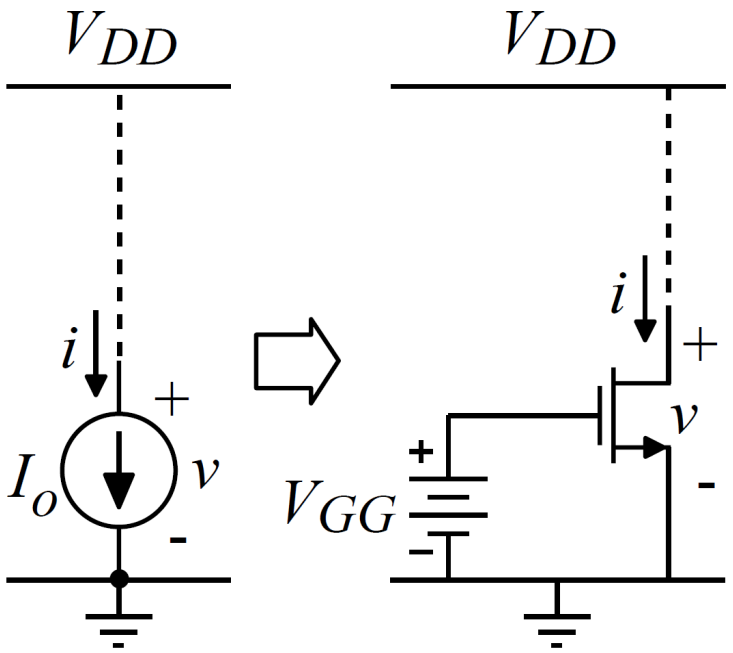
Brief Introduction to Current Sources/Sinks

- NB: Terms current “source” and “sink” will be used interchangeably!
- A current source is a device through which a fixed current flows irrespective of the voltage across it
- A perfect current source is not realisable, but, a single FET in saturation is a fair approximation
- Make $V_{bias} = V_T + \Delta V$ and make $V_{DS} > \Delta V$ to keep the transistor in saturation

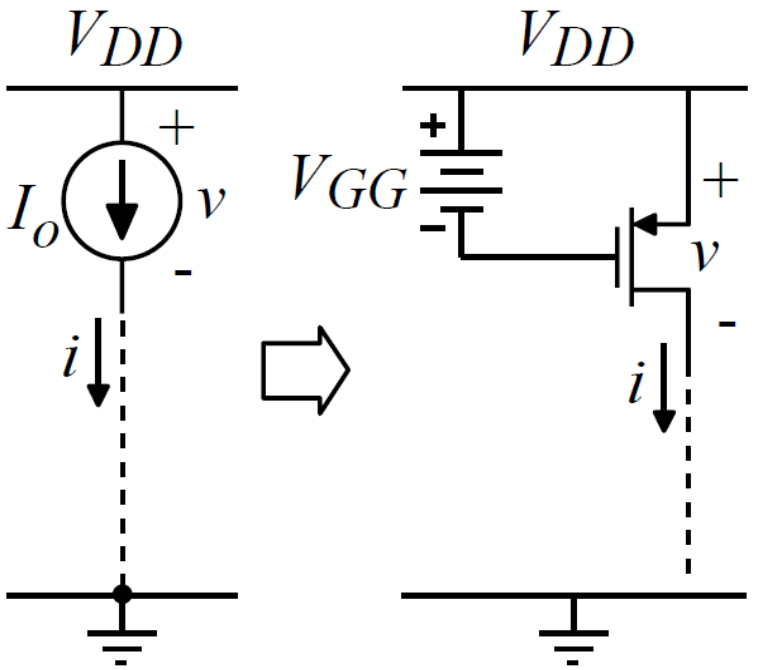


Current Source

- nFET and pFET as current source
- Both are called “current sources”!



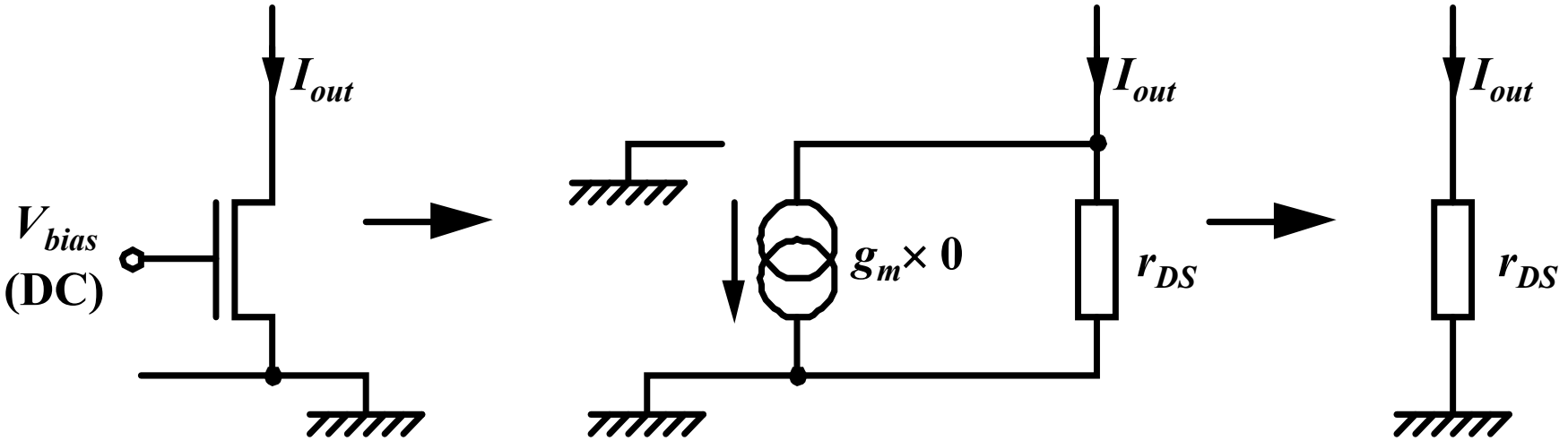
Current Sink



Current Source

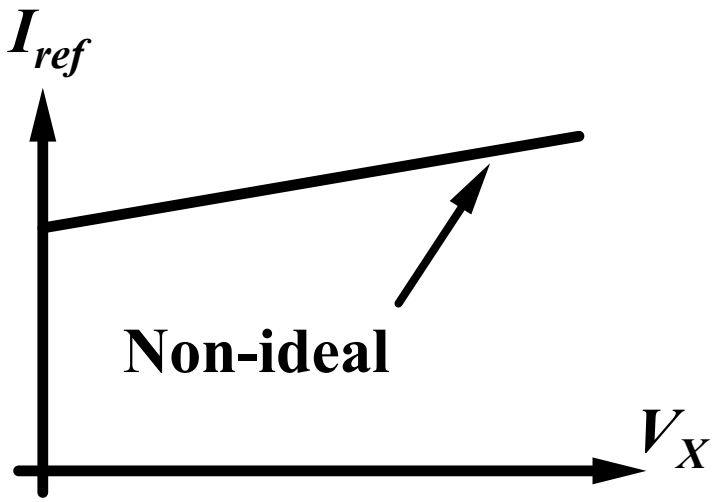
Current Source

- The output impedance of a perfect current source is infinite
- The output impedance of a single FET current source is r_{DS}, as shown below



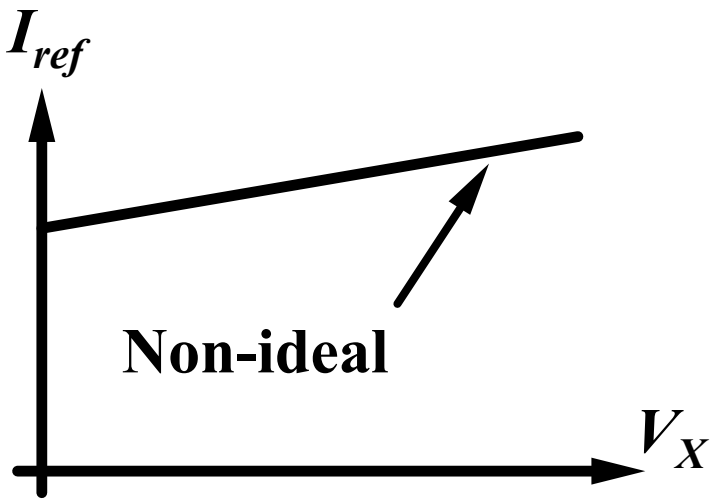
Current Source

- nFET and pFET as current source
- The current/voltage graph should be horizontal, but it has a slopes, hence a resistance



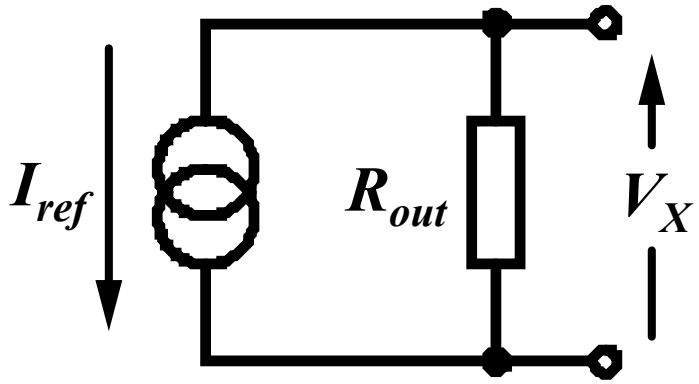
Current Source

- A realisable “current source” will supply *approximately* the same current, I_{ref}, but the output current will rise slightly with the voltage across it, V_X.
- The current/voltage graph should be horizontal, but it slopes up, as shown.



Intro to Current Sources

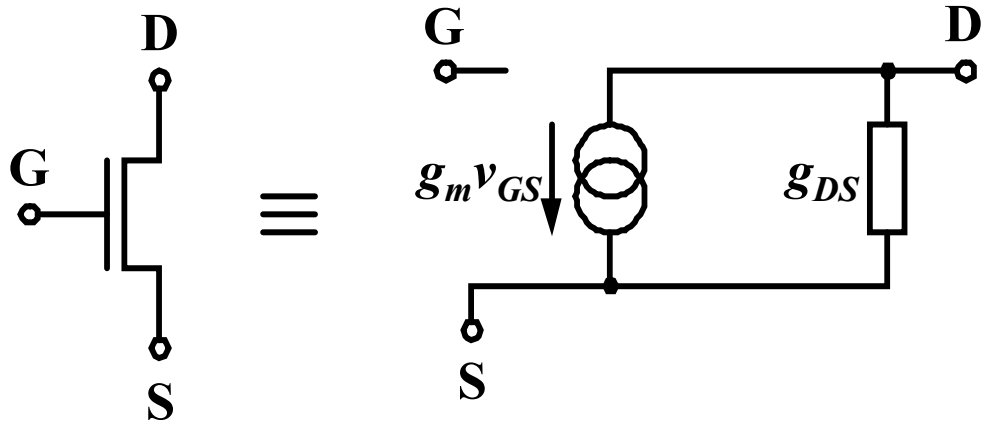
- The model of such a current source, comprising an ideal current source and a resistor, is shown here. The resistor, R_{out}, models the non-ideality.



- Clearly, as V_X rises, more current flows through R_{out} so modelling the realisable "current source".
- Clearly, the realisable "current source" tends towards the ideal as R_{out} tends to infinity.

Transistor Model

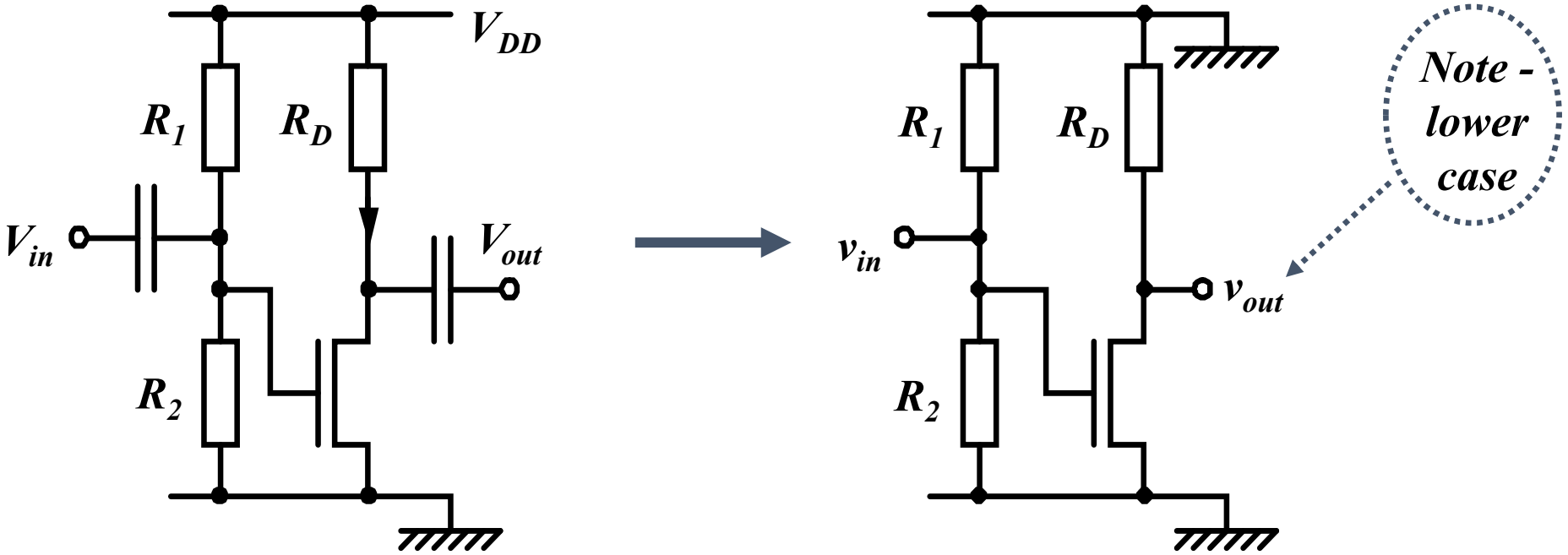
- A FET is a non-linear device and we want to replace it with a *linear* model
- The *small-signal model* normally used is shown here



- Note that the gate does not appear to be connected. The gate draws no current; only the *voltage* V_{GS} matters
- The drain current comes (mainly) from the dependent current source of value $g_m v_{GS}$
- The variations in I_{DS} with V_{DS} are modelled by $g_{DS} = 1/r_{DS}$

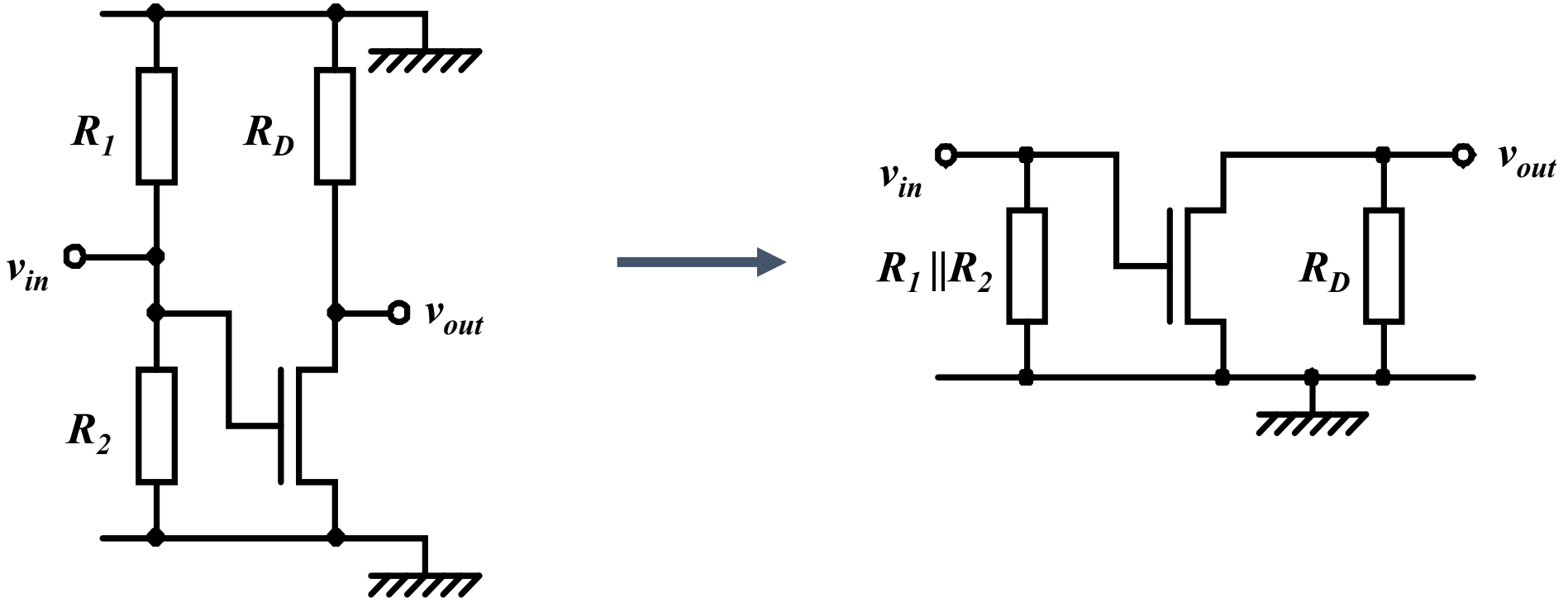
Example of Small-Signal Analysis

- 1/ Replace all DC supplies by AC zero
- 2/ Replace all decoupling capacitors by short-circuits



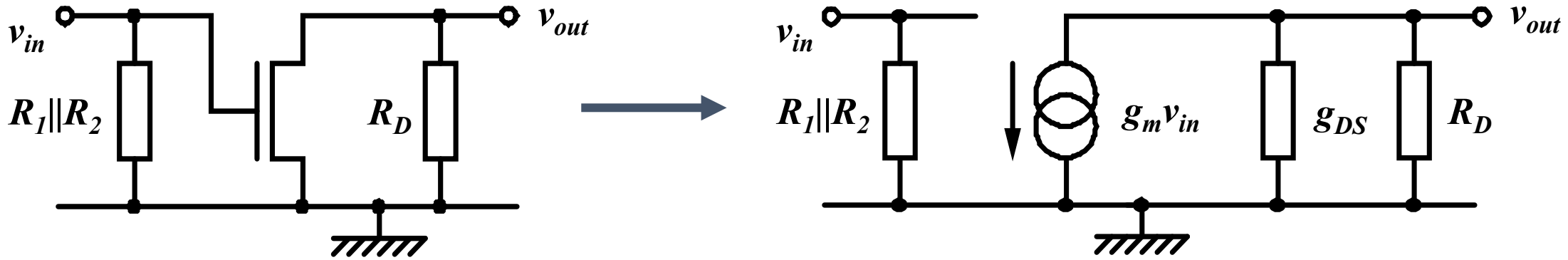
Example of Small-Signal Analysis

- 3/ Redraw to have a single ground rail
- 4/ R_1 and R_2 are in parallel so can be replaced by a single component



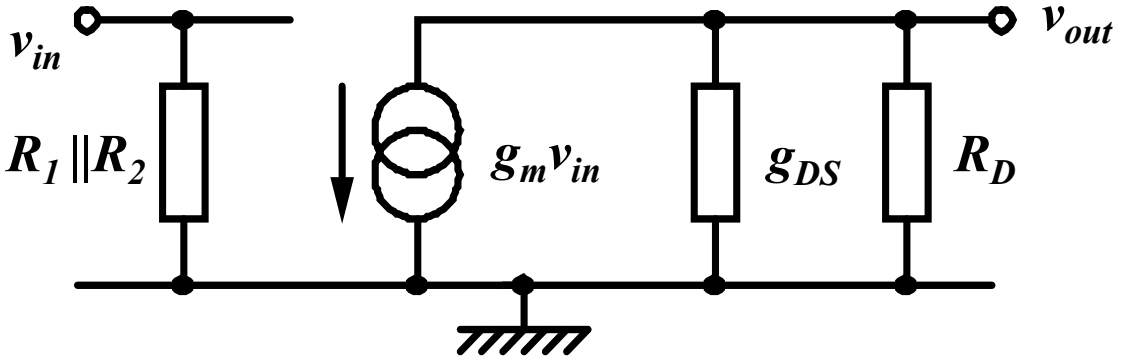
Example of Small-Signal Analysis

- 5/ Substitute the small-signal model of the FET, terminal by terminal
- 6/ Analyse using Ohm's and Kirchhoff's Laws
- v_{in} is an AC voltage source so R_1 and R_2 don't matter



Example of Small-Signal Analysis

- All current comes from current source and must go through the parallel combination of g_{DS} and R_D

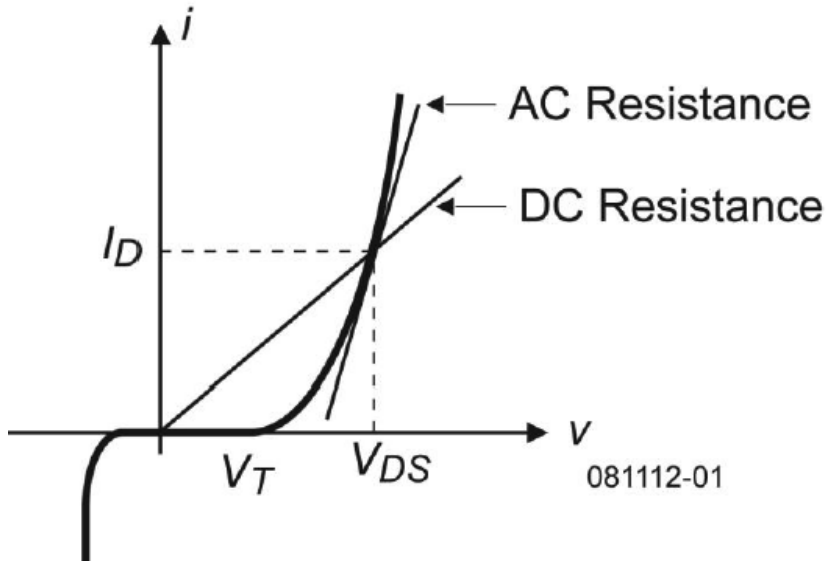


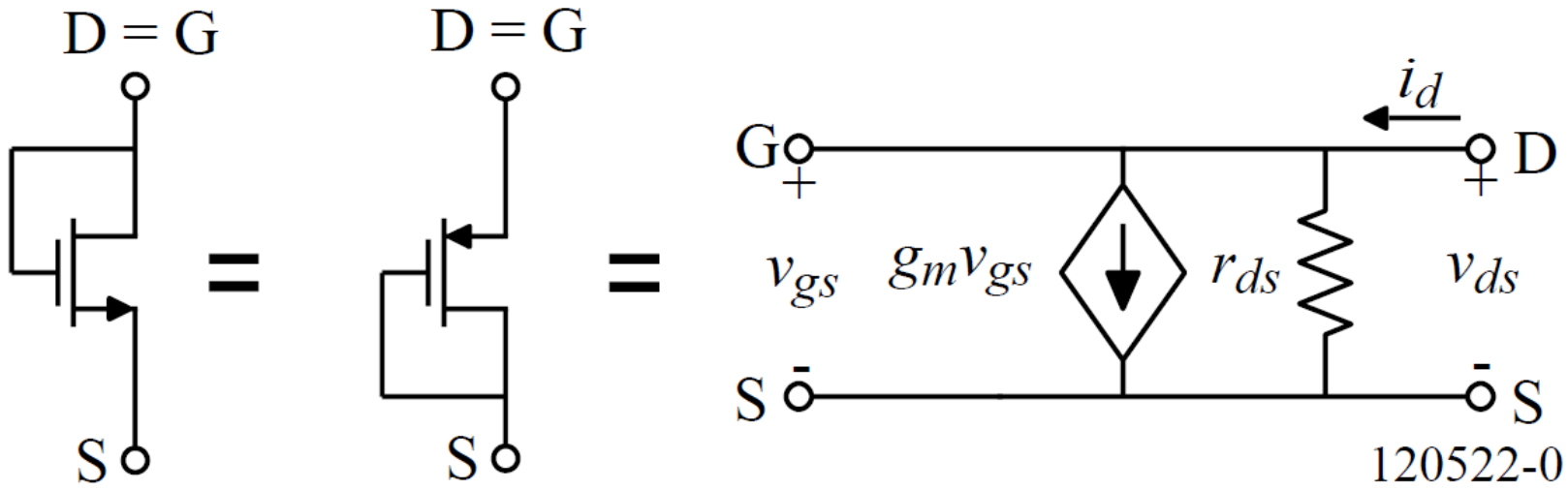
- Let $G_D = 1/R_D$. Then the parallel combination has conductance $g_{DS} + G_D$. The current is $g_m v_{in}$ so

$$v_{out} = -\left(\frac{g_m v_{in}}{g_{DS} + G_D}\right) \Rightarrow \frac{v_{out}}{v_{in}} = -\left(\frac{g_m}{g_{DS} + G_D}\right)$$

Diode connected FET

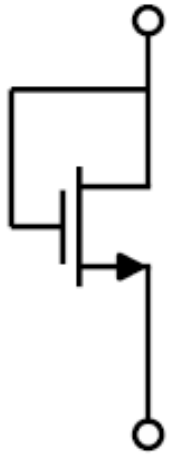
- Diode counted FETs:
- Non-linear “active resistor”





Diode connected FET

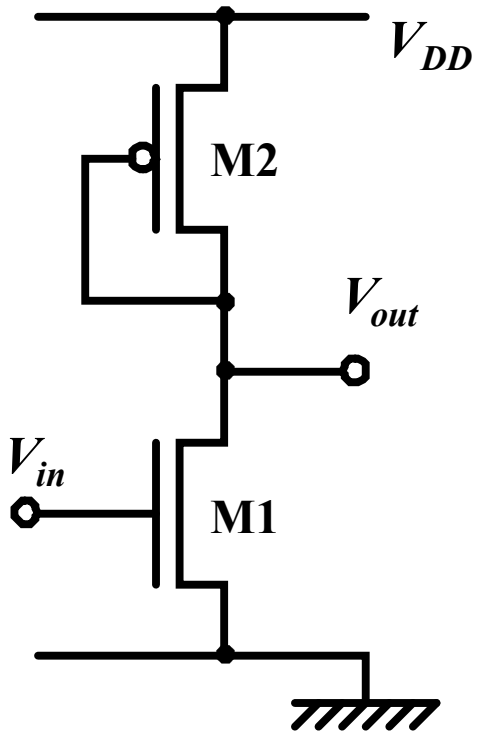
- Always in saturation



$$\text{AC resistance} = \frac{v_{ds}}{i_d} = \frac{1}{g_m + g_{ds}} \approx \frac{1}{g_m}$$

Inverter with Diode-Connected active load

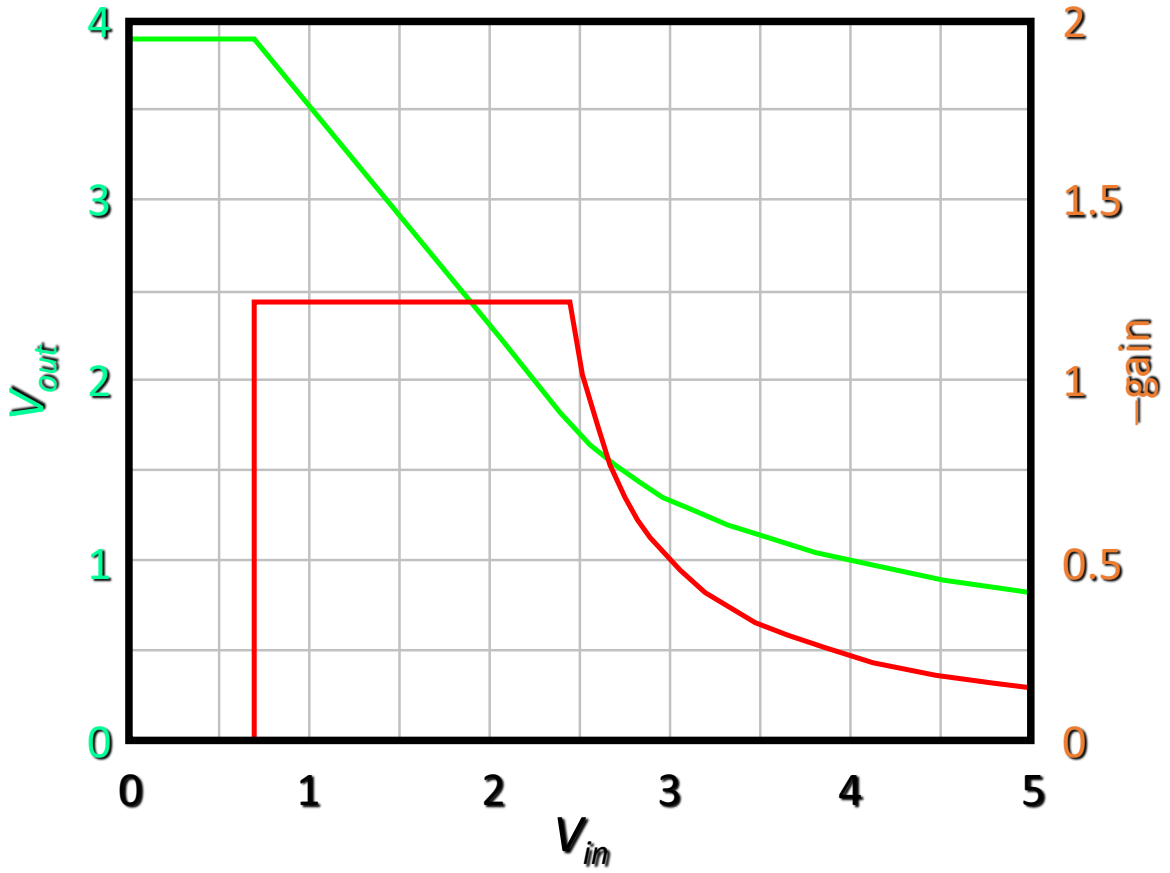
- Replace resistor with active device
- *Much* smaller
- Unfortunately M2 “fights” M1
  - as V_{out} falls M2 tries even harder to drag it back up
- Gain tends to be low



Inverter with Diode-Connected active load

- $(W/L)_1 = 20/2.5$
- $(W/L)_2 = 33.5/2.5$ (same current as 5kΩ resistor)
- $V_{out(max)} = V_{DD} + V_{TP}$
- As V_{in} rises M1 and M2 saturated, then M1 moves into linear region and gain falls

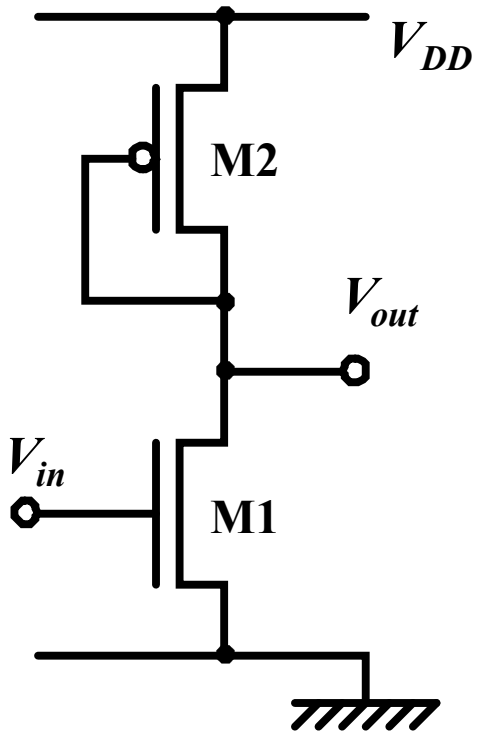
–ve



Inverter with Diode-Connected active load

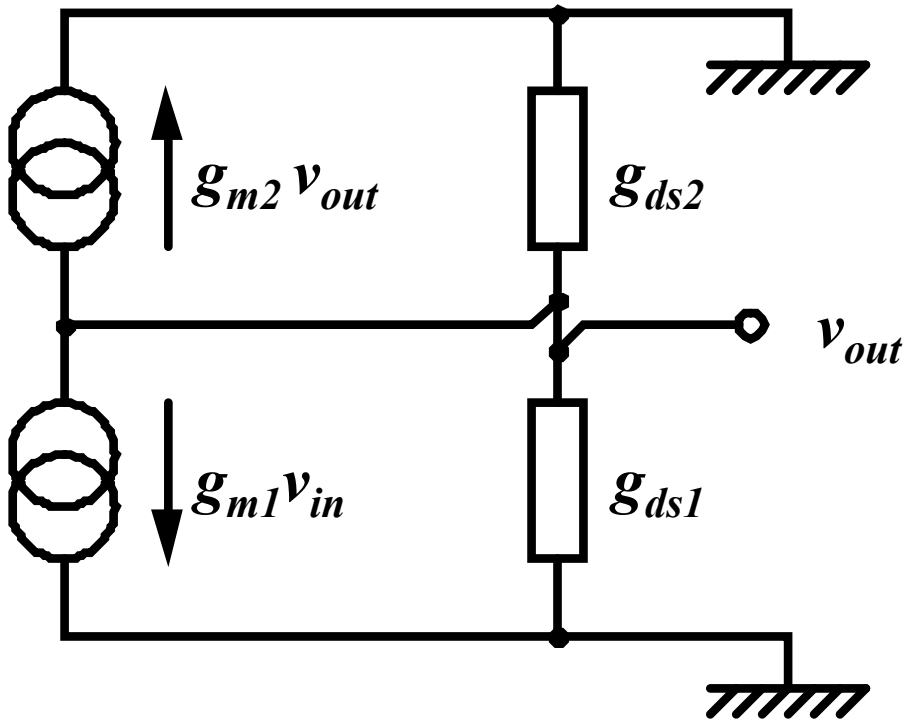
- OK, so M2 was a stupid size
- Make it much weaker so the gain, (β_1 /β_2), rises

- We could not increase the resistance of a resistive load as it would become huge. No problem with a FET



Inverter with Diode-Connected active load

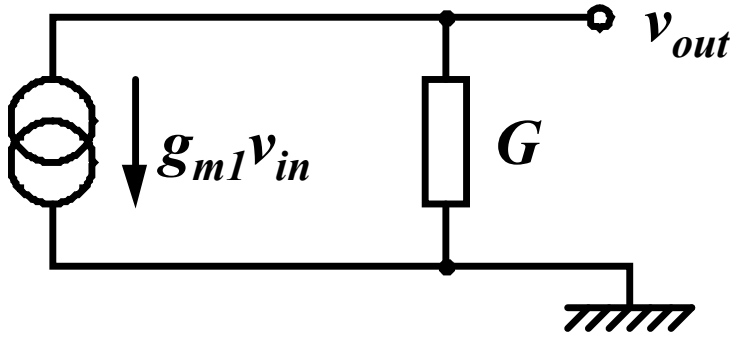
- Shown here is the first-stage small-signal model of the active-load inverter
- Note that the $g_{m2}v_{out}$ current source, connected from v_{out} to ground, is just a resistor of value g_{m2}



Inverter with Diode-Connected active load

- Let $G = g_{m2} + g_{DS1} + g_{DS2}$
- Then

$$\frac{v_{out}}{v_{in}} = -\left(\frac{g_{m1}}{g_{m2} + g_{DS1} + g_{DS2}}\right)$$



- This is approximately equal to $-g_{m1}/g_{m2}$ which is equal to

$$-\sqrt{2\beta_1 I_{DS1}} / \sqrt{2\beta_2 I_{DS2}} = -\sqrt{\beta_1/\beta_2}$$

$$Gain, A_v = -\sqrt{\frac{\beta_1}{\beta_2}} = -\sqrt{\frac{\mu_n \left(\frac{W}{L}\right)_1}{\mu_p \left(\frac{W}{L}\right)_2}}$$

Inverter with Diode-Connected active load

- Limitations of Diode-Connected Active Load:

- So, the gain is a relatively weak function (because of square root) of the device dimensions.
- For high gain, then the device will have disproportionately wide or long transistors.
- This will result in large input or load capacitance.
- Large capacitance limits/reduces bandwidth.

Inverter with Diode-Connected active load

Limitations of Diode-Connected Active Load

Also, $I_{D1} = I_{D2}$

$$\therefore \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_{in} - V_{t1})^2 = \frac{1}{2}\mu_p C_{ox}\left(\frac{W}{L}\right)_2 (V_{GS2} - V_{t2})^2$$

$$\Rightarrow \sqrt{\frac{\mu_n\left(\frac{W}{L}\right)_1}{\mu_p\left(\frac{W}{L}\right)_2}} = \frac{|V_{GS2} - V_{t2}|}{V_{in} - V_{t1}} = \mathbf{Av} \qquad (V_{GS2} = V_{DD} - V_{out})$$

Thus,

$$\mathbf{Av} = \frac{|V_{ov2}|}{V_{ov1}}$$

Inverter with Diode-Connected active load

Limitations of Diode-Connected Active Load

So, for high gain, overdrive voltage of M2 has to much bigger than that of M1.

$$V_{GS2} = V_{ov2} + V_{t2}$$

High $V_{ov2} \Rightarrow$ high V_{GS2}

- High V_{GS2} (DC bias point) will lead to distortion in the output signal or limit the output signal swing without distortion.

Key points

- A MOS transistor converts input voltage to output current via g_m
- The output current is converted to output volts via the load resistance, R_L
- Therefore $Gain = g_m \times R_L$
- This is a key result!!

Key points

- The output impedance of a MOS circuit is R_L
- The output impedance is always a key component of the circuit's bandwidth
- Roughly $Bandwidth = 1/(R_L C_L)$
  where C_L is the load capacitance (and there is always a load capacitance)
- Another key result!

Key points

- We have $Gain = g_m \times R_L$

  and $Bandwidth = 1/(R_L C_L)$
- The Gain-Bandwidth product (GBW) of the circuit is a measure of its "goodness"
- $GBW = (g_m \times R_L) \times [1/(R_L C_L)] = g_m / C_L$
  so we see that *GBW* depends only on g_m and C_L

Requirements for a “good” load

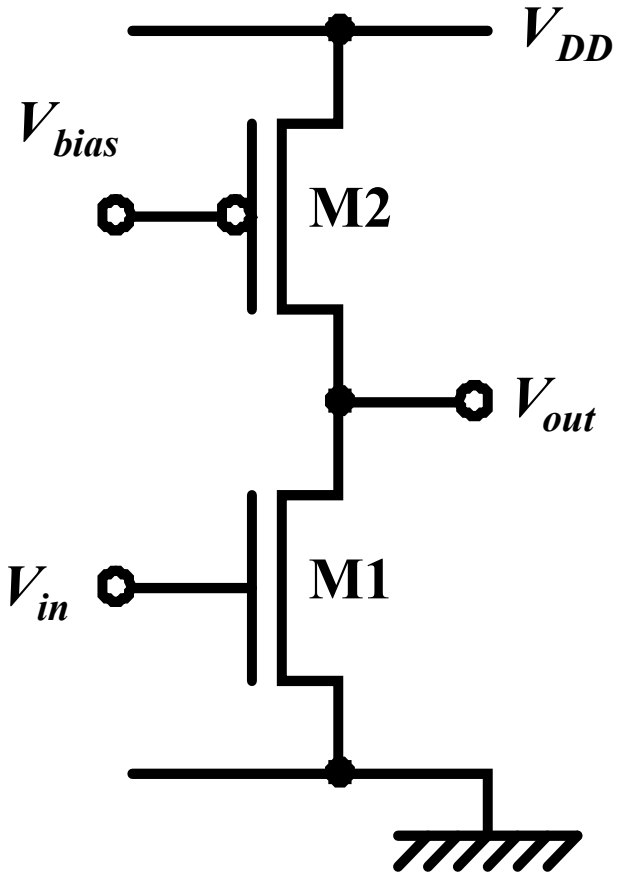
- For resistive load we had

$$\frac{v_{out}}{v_{in}} = -\left(\frac{g_m}{g_{DS} + G_D}\right)$$

- For high gain we need G_D *small*, so R_D *high*
- … but we need the load to be physically small
- … and we need a reasonable DC bias current
- Strangely enough, this is actually possible! What we need is a current source

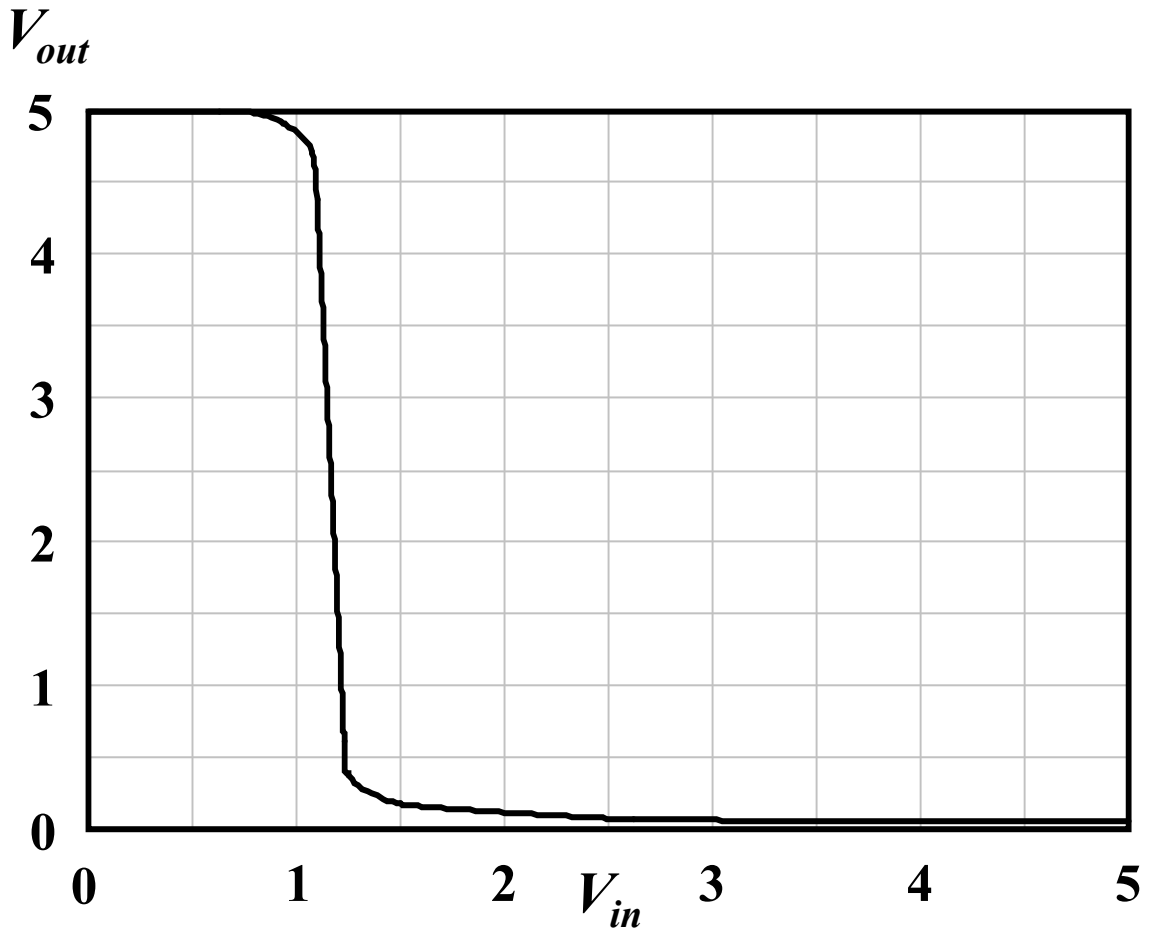
Single Transistor Amplifier - Current Source Load

- Very suitable for integration - single load transistor takes little area on IC
- M2 is half a P-Channel current mirror. V_{bias} comes from the other side
- M2 must be in saturation and M1 is best operated in saturation
- The gain of this circuit can be quite high



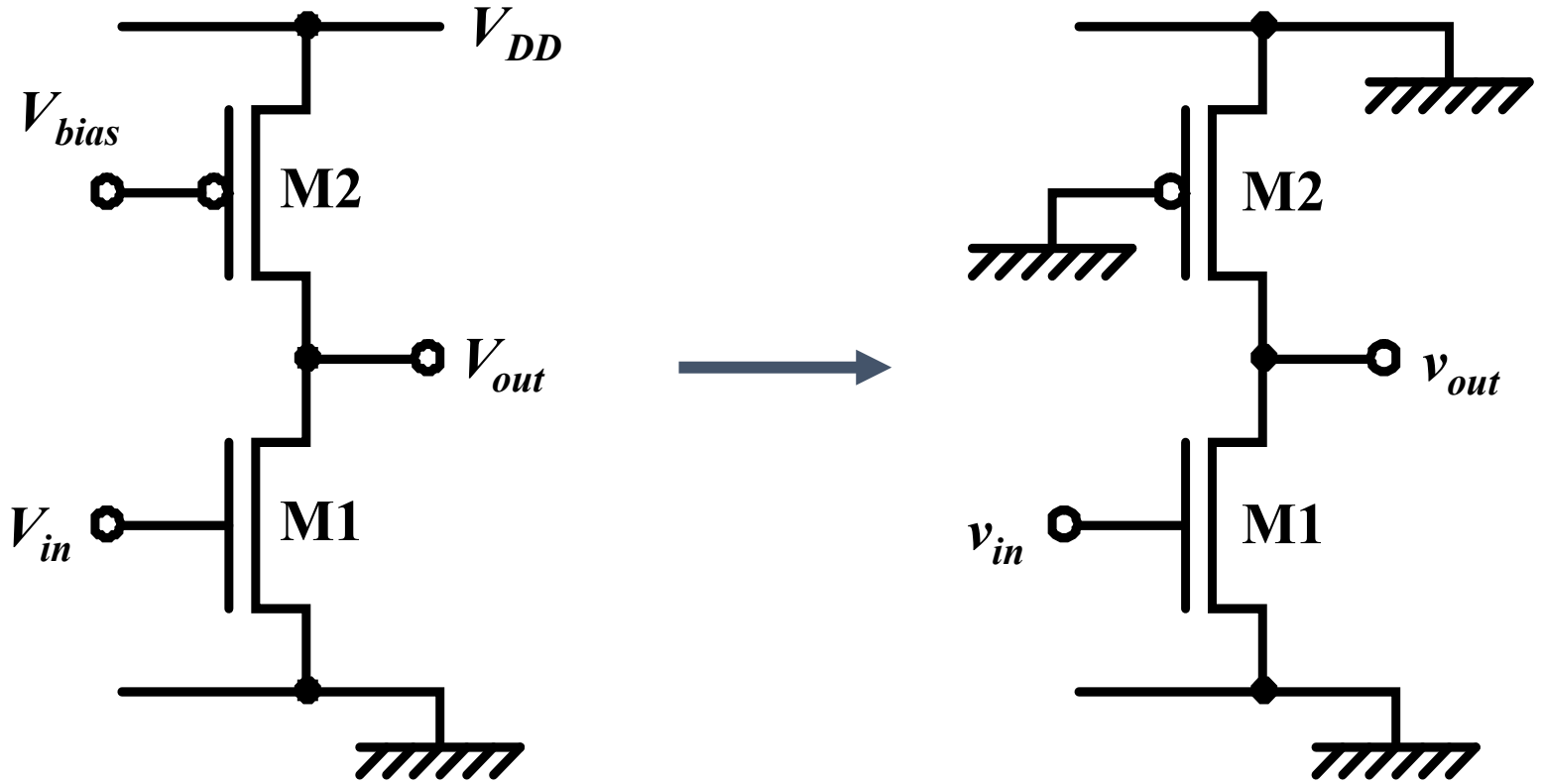
Single Transistor Amplifier - Current Source Load

- High-gain region always a good bit below $V_{in} = V_{DD}/2$
- Maximum current limited by current source load



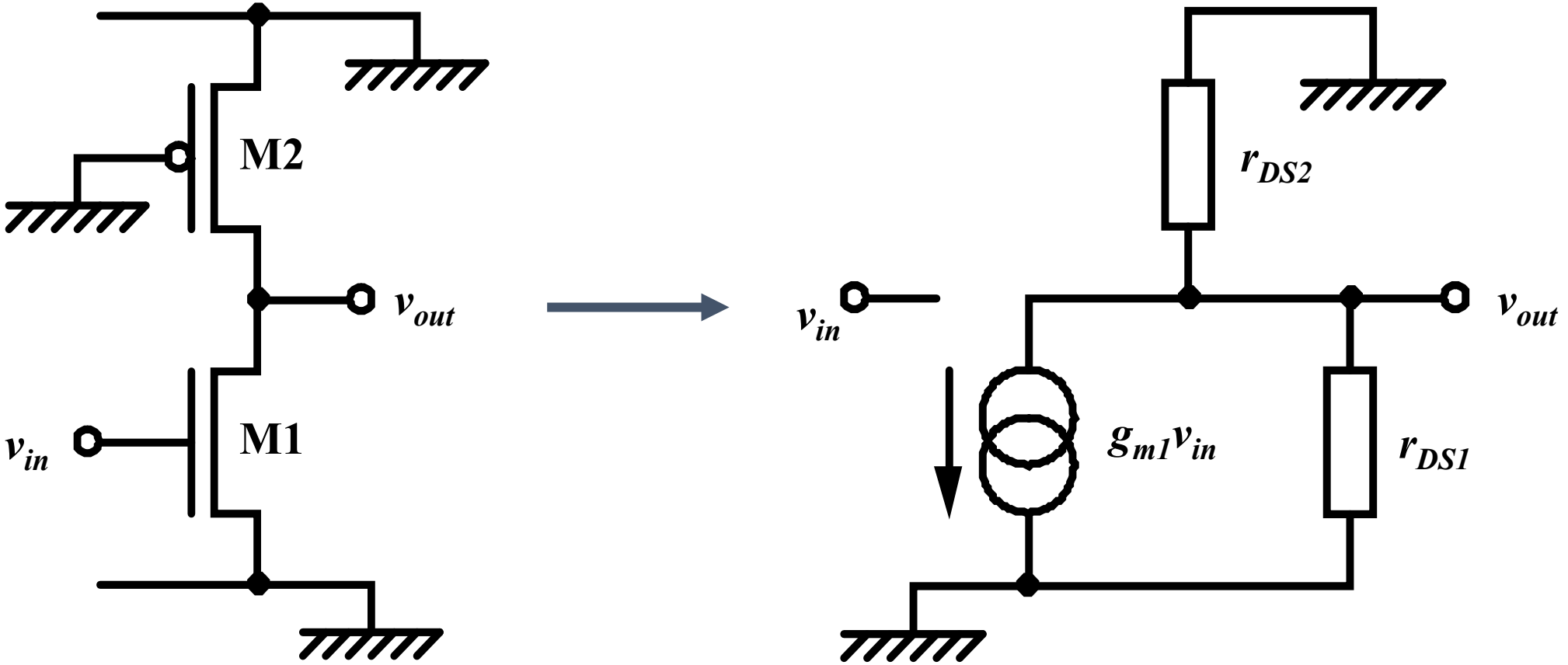
Single Transistor Amplifier - Current Source Load

- Now let us look at the small-signal model
- First set to zero DC bias voltages (including V_{bias})



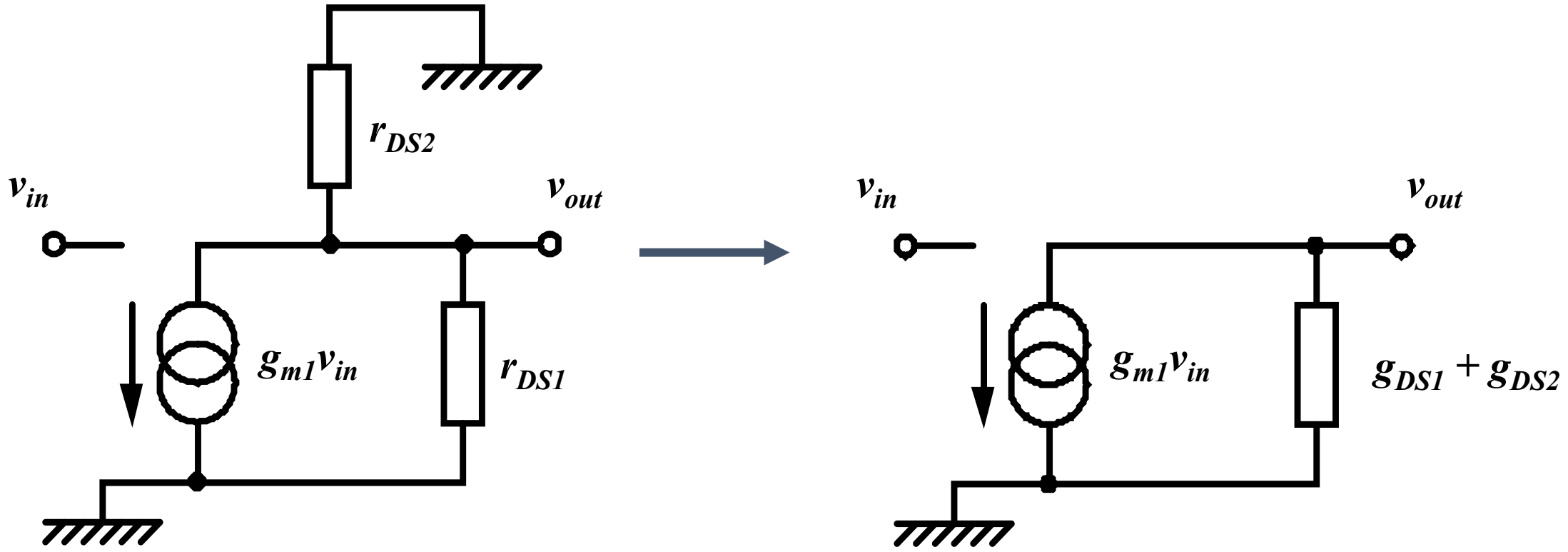
Single Transistor Amplifier - Current Source Load

- Substitute the small-signal models for the FETs



Single Transistor Amplifier - Current Source Load

- Redraw to make clearer, merging the two resistors



Single Transistor Amplifier - Current Source Load

- Now we see that all the current must go through the resistor.

Hence:

$$\frac{v_{out}}{v_{in}} = \frac{-g_{m1}}{g_{DS1}+g_{DS2}} = \frac{-\sqrt{2\beta_1}\sqrt{I_{DS}}}{I_{DS}\left(\lambda_N+\lambda_P\right)}$$

- Note that the gain is *inversely* proportional to $\sqrt{I_{DS}}$

- Clearly the output impedance is equal to $(g_{DS1} + g_{DS2})^{-1}$