



THE UNIVERSITY *of* EDINBURGH

Analogue IC Design

Introduction to chip design

Sep – Dec 2022

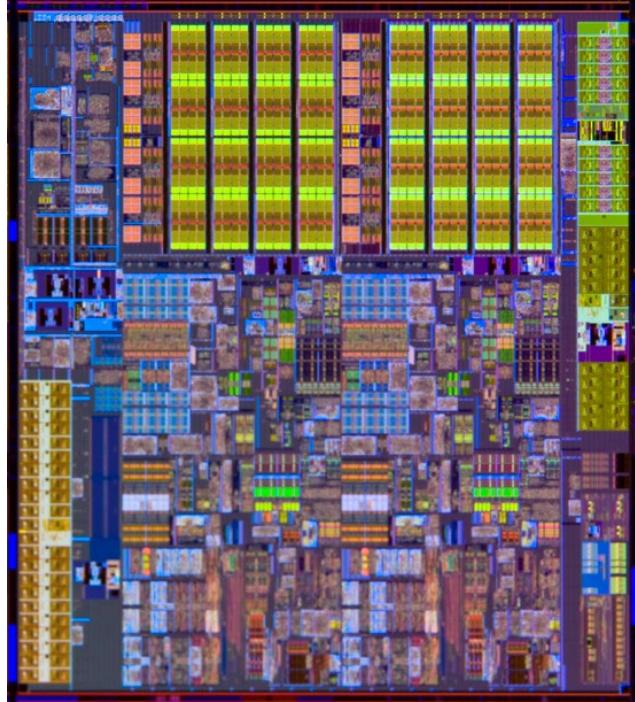
Dr Danial Chitnis

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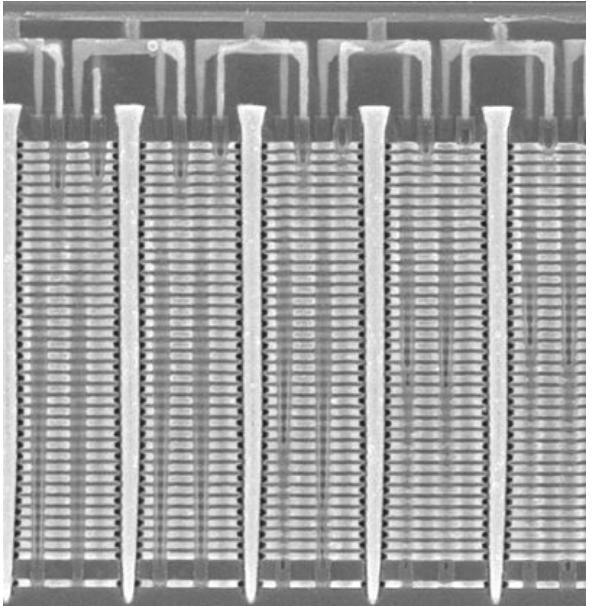
Contents

- Transistors
- Layout
- Design Rules
- Packaging
- Power
- Transistor models
- Non-ideal effects

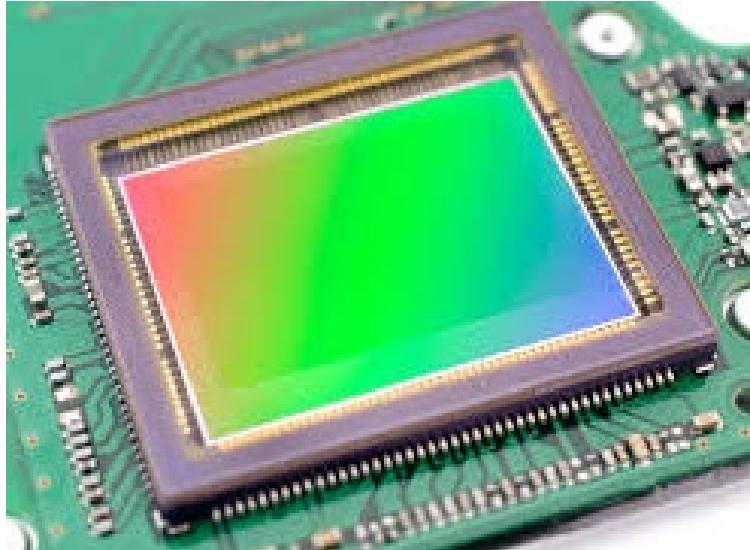
Our progress in the past three decades...



Microprocessors



Memory

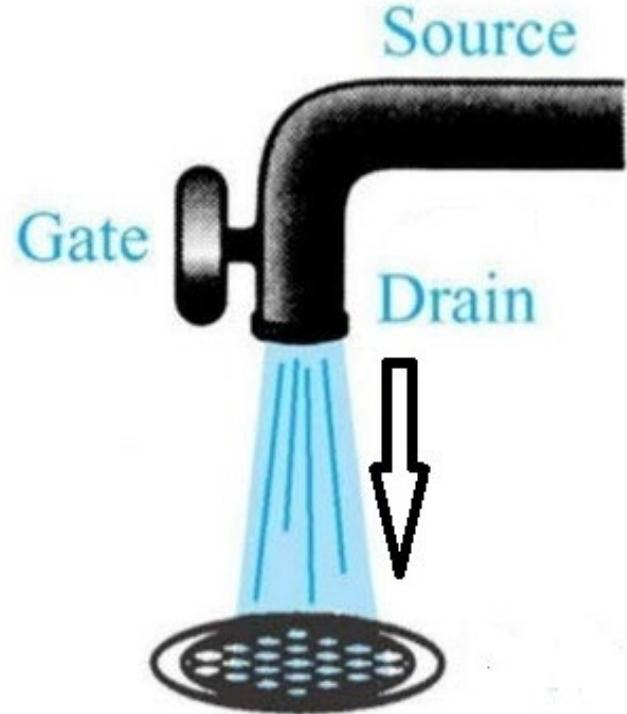


CMOS
Image Sensors

Back to today...

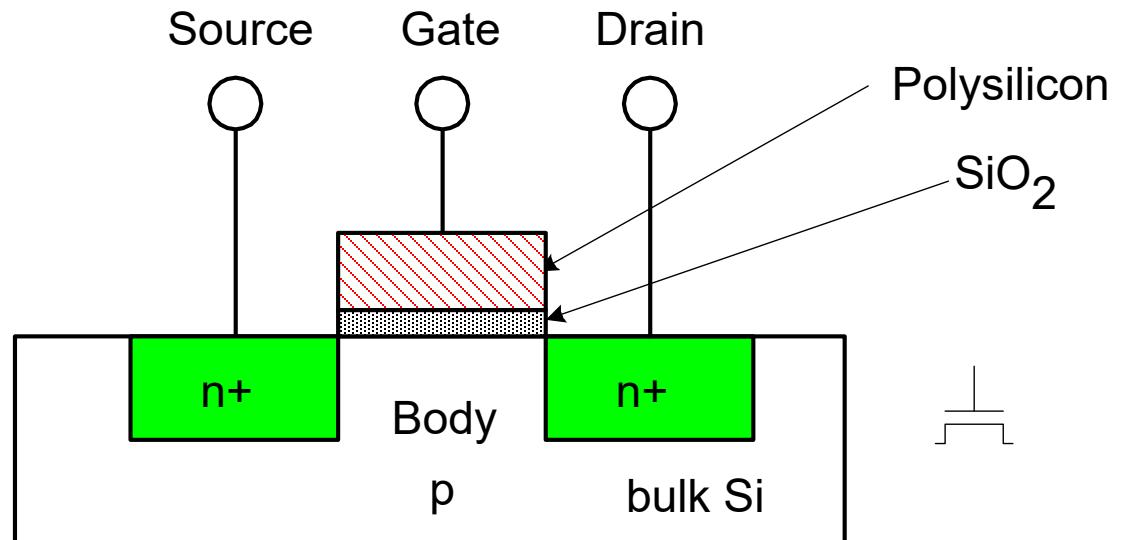
Transistors

- What is a transistor?
- Is it a switch or is it an amplifier?
- Tap analogy
- It consume energy only when the gate is changed



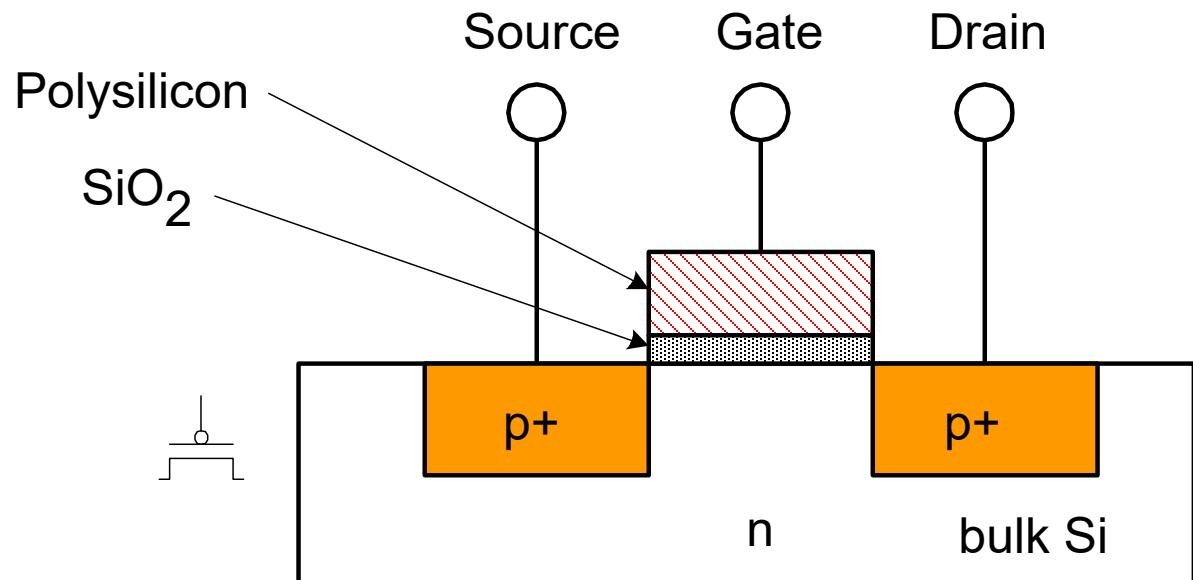
Transistors

- Four terminals: gate, source, drain, body
- Symbol shows gate, source, drain
 - Usually omits body
 - Source and drain are logically indistinguishable



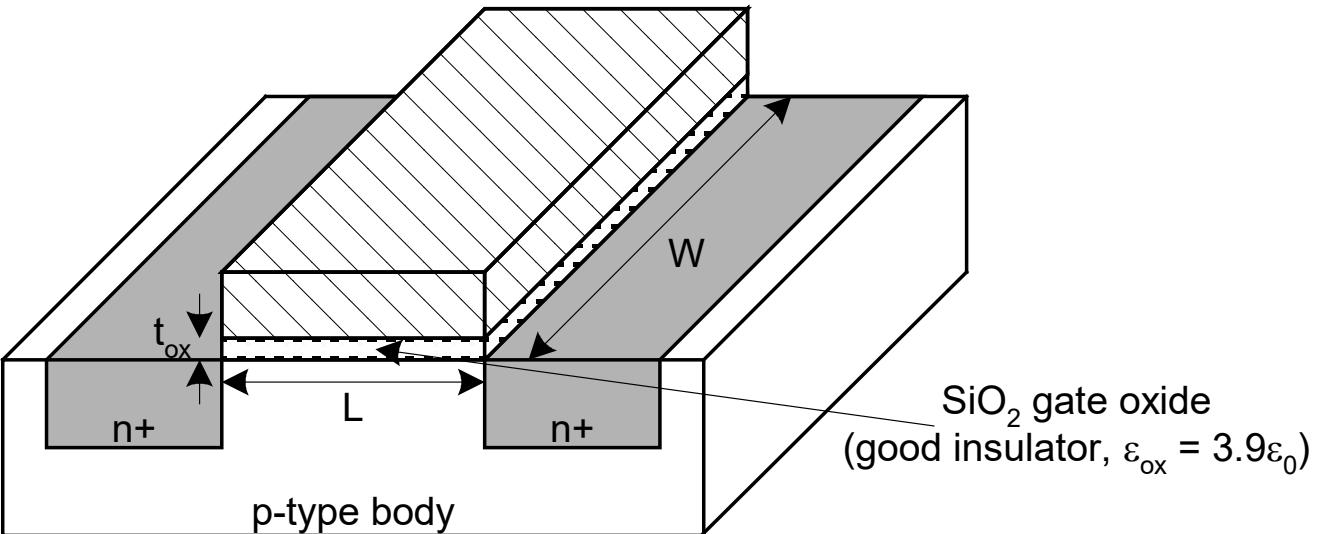
Transistors

- Similar, but doping and voltages reversed
 - Body tied to high voltage (V_{DD})
 - Gate low: transistor ON
 - Gate high: transistor OFF
 - Bubble indicates inverted behavior



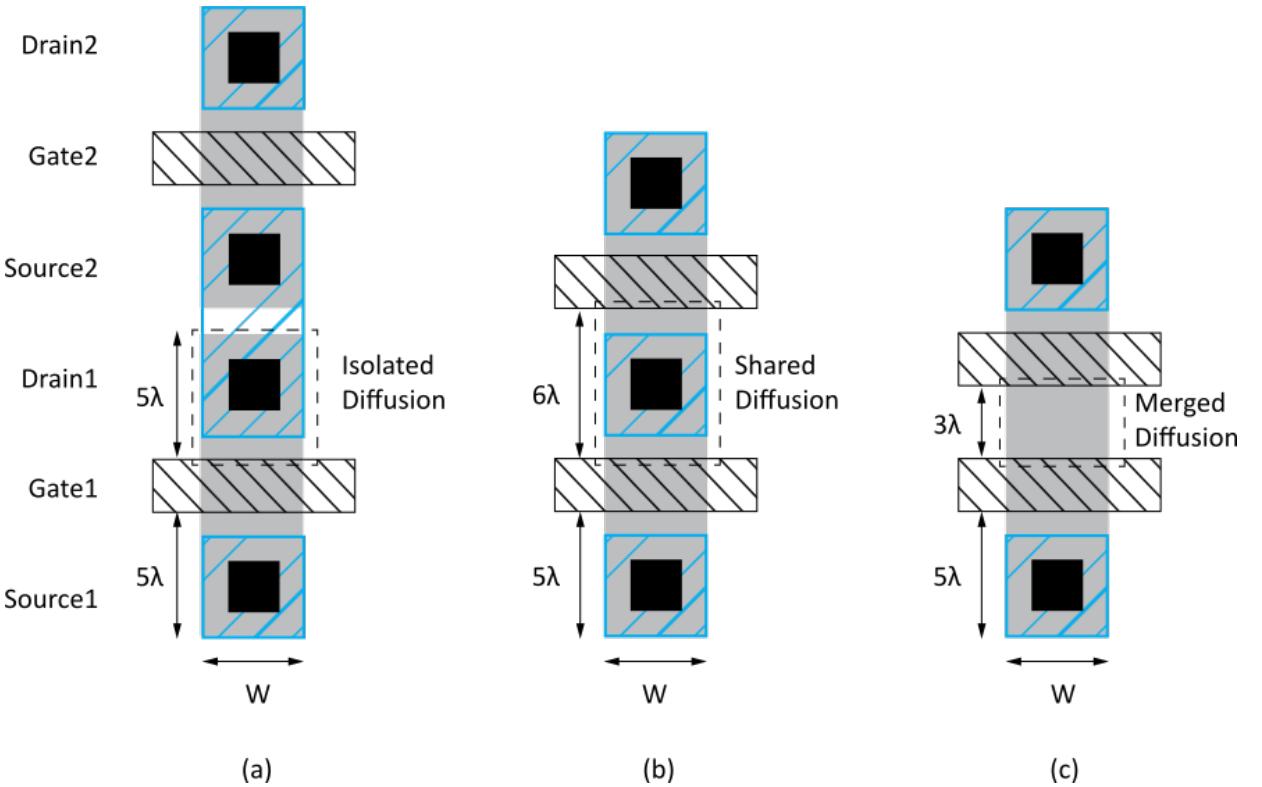
Transistors

- Important to remember transistor is a 3D structure



Transistors

- Top layout view
- Transistors may share diffusion areas

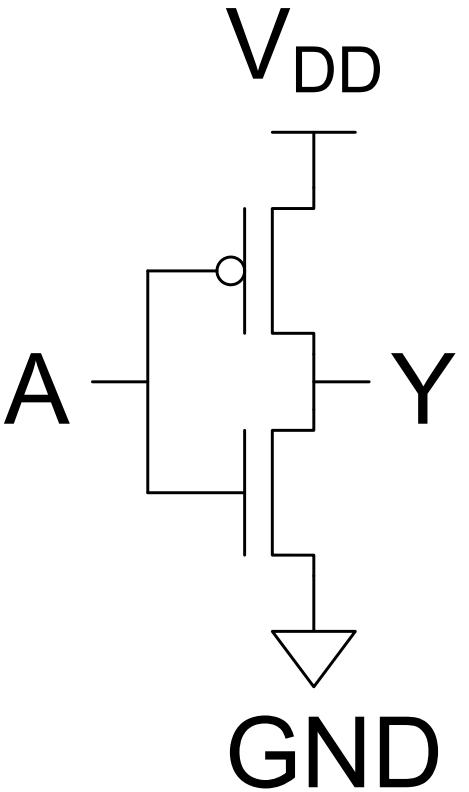
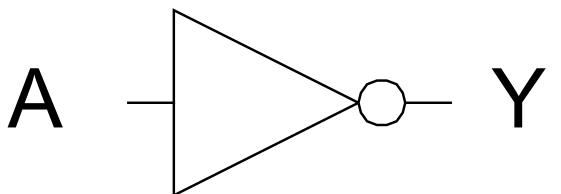


CMOS Fabrication

- CMOS transistors are fabricated on silicon wafer
- Lithography process similar to printing press
- On each step, different materials are deposited or etched
- Easiest to understand by viewing both top and cross-section of wafer in a simplified manufacturing process

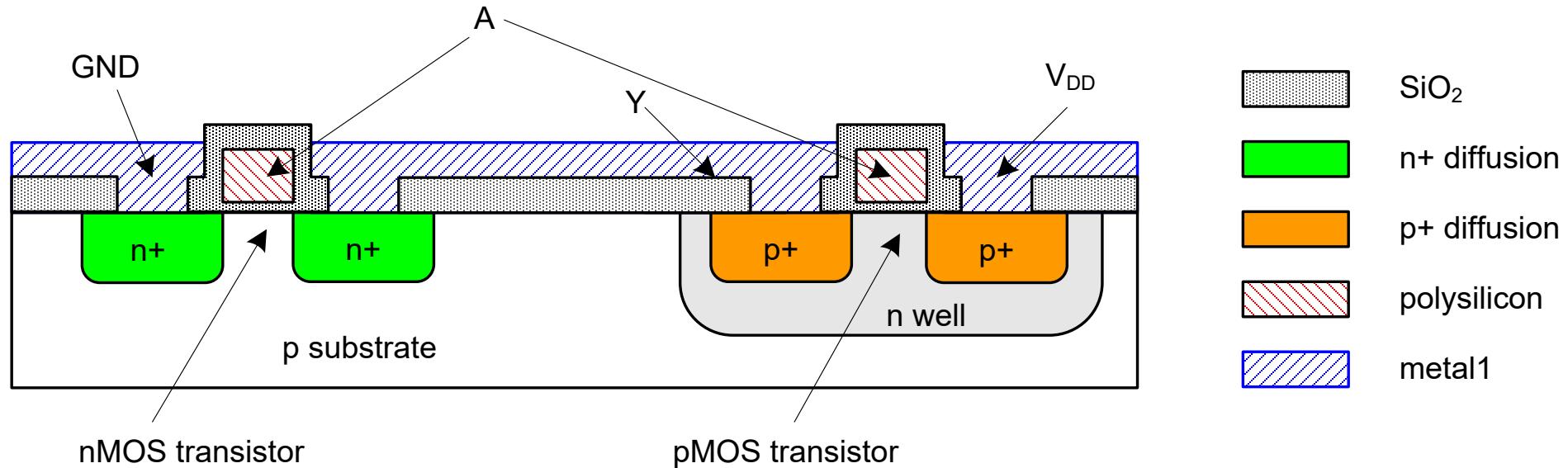
CMOS Inverter

A	Y
0	1
1	0



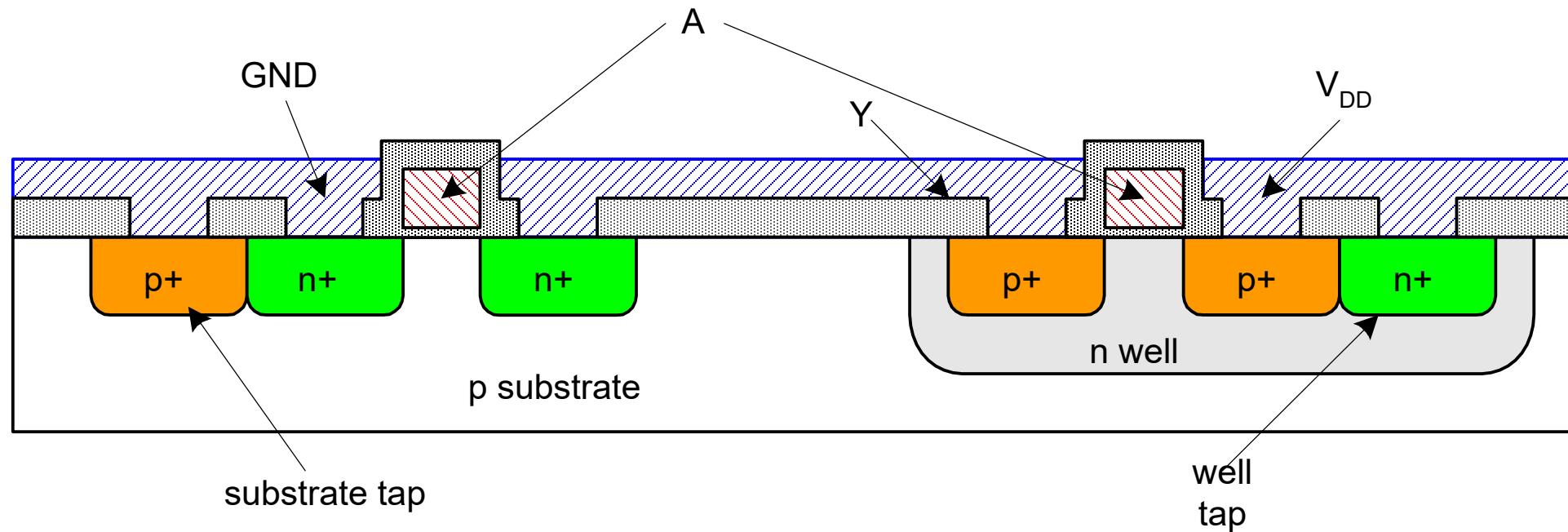
Inverter Cross-section

- Typically use p-type substrate for nMOS transistors
- Requires n-well for body of pMOS transistors
 - So pMOS p-type source/drain doesn't short to p-type substrate



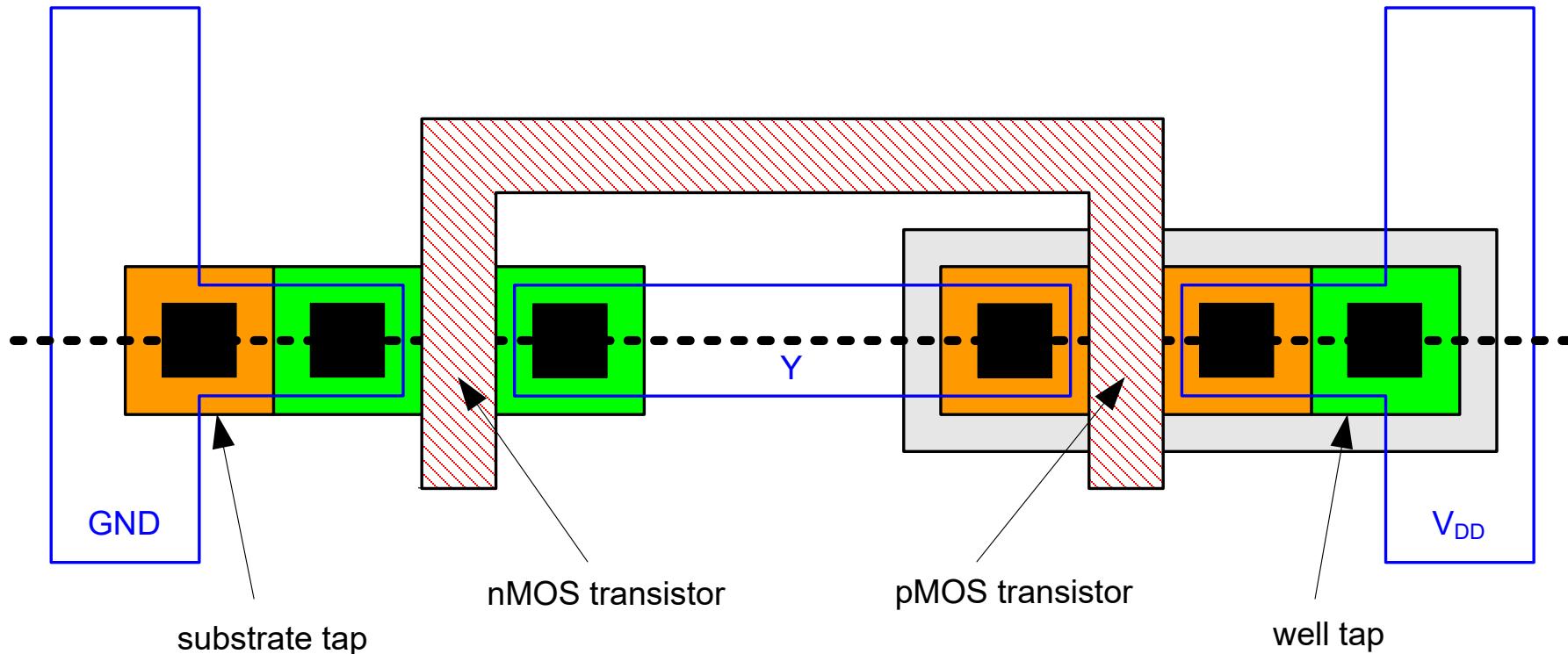
Well and Substrate Taps

- Substrate must be tied to GND and n-well to V_{DD}
- Metal to lightly doped semiconductor forms poor connection called Schottky Diode
- Use heavily doped well and substrate contacts/taps



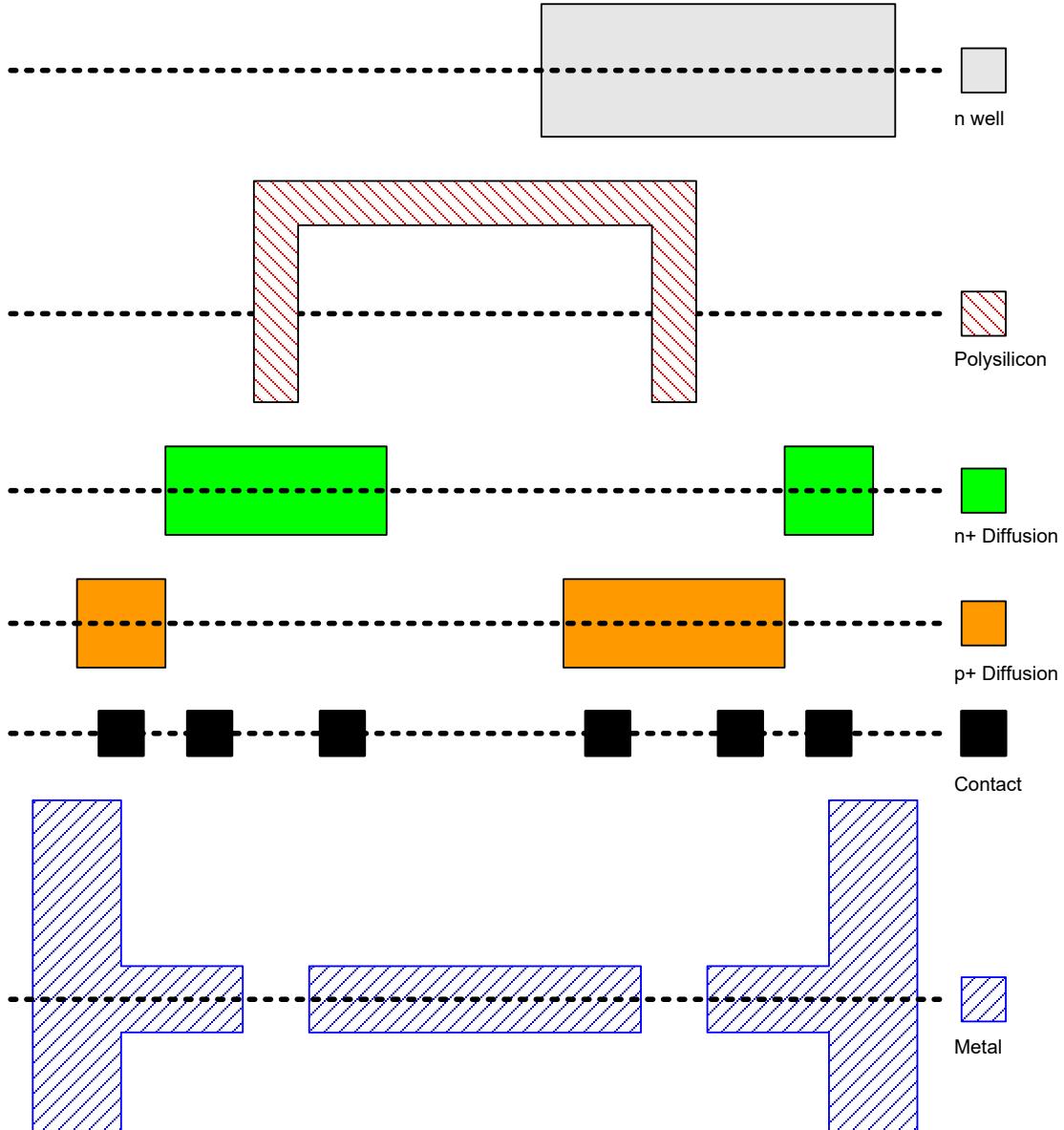
Inverter Mask Set

- Transistors and wires are defined by *masks*
- Cross-section taken along dashed line



Detailed Mask Views

- Six masks
 - n-well
 - Polysilicon
 - n+ diffusion
 - p+ diffusion
 - Contact
 - Metal



Fabrication

- Chips are built in huge factories called fabs
- Contain clean rooms as large as football fields, costing billions of dollars



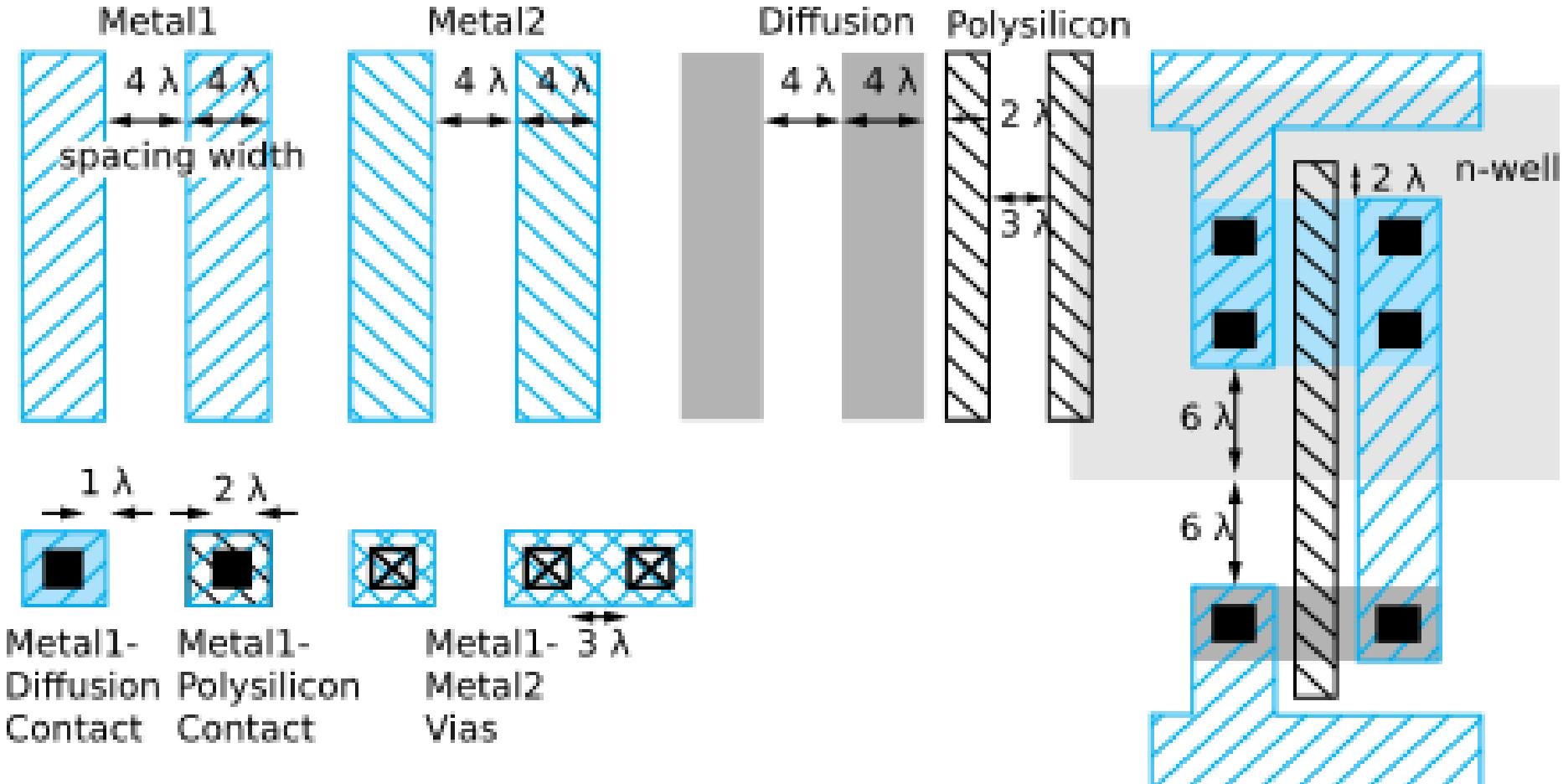
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Layout

- Chips are specified with a set of masks
- Minimum dimensions of masks determine transistor size (and hence speed, cost, and power)
- Feature size f = distance between source and drain
 - Set by minimum width of polysilicon
- Feature size improves 30% every 3 years or so
- Normalize for feature size when describing design rules
- Express rules in terms of $\lambda = f/2$
 - E.g., $\lambda = 0.3 \mu\text{m}$ in $0.6 \mu\text{m}$ process

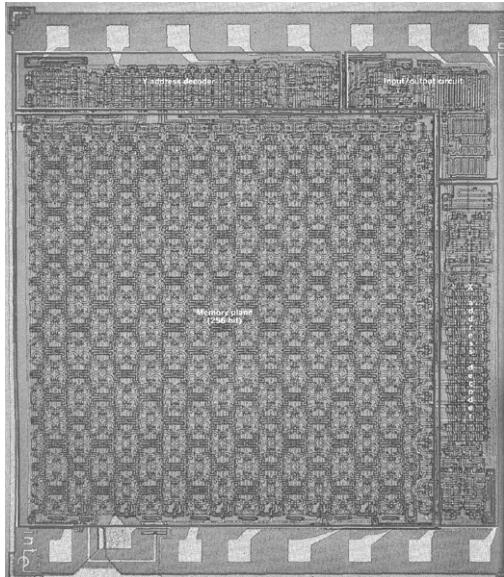
Simplified Design Rules

- Conservative rules to get you started



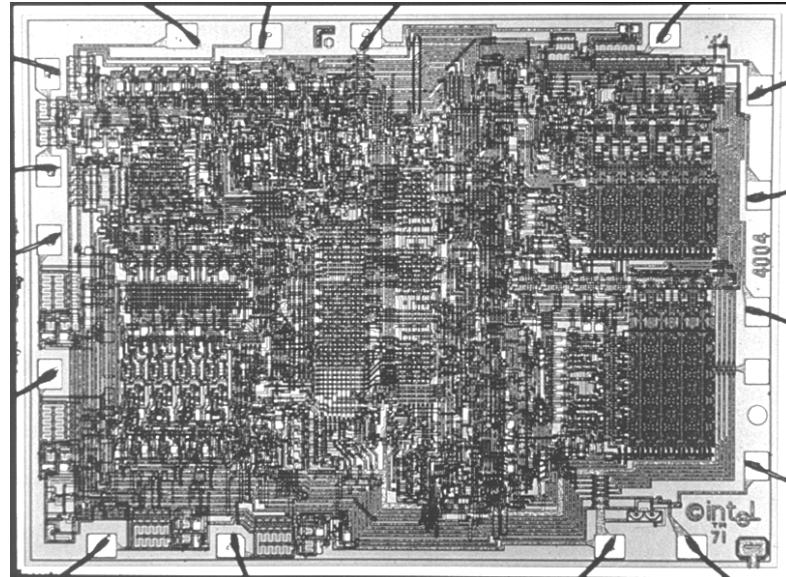
MOS Integrated Circuits

- 1970's processes usually had only nMOS transistors
 - Inexpensive, but consumed power while idle



[Vadasz69]
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Intel 1101 256-bit SRAM



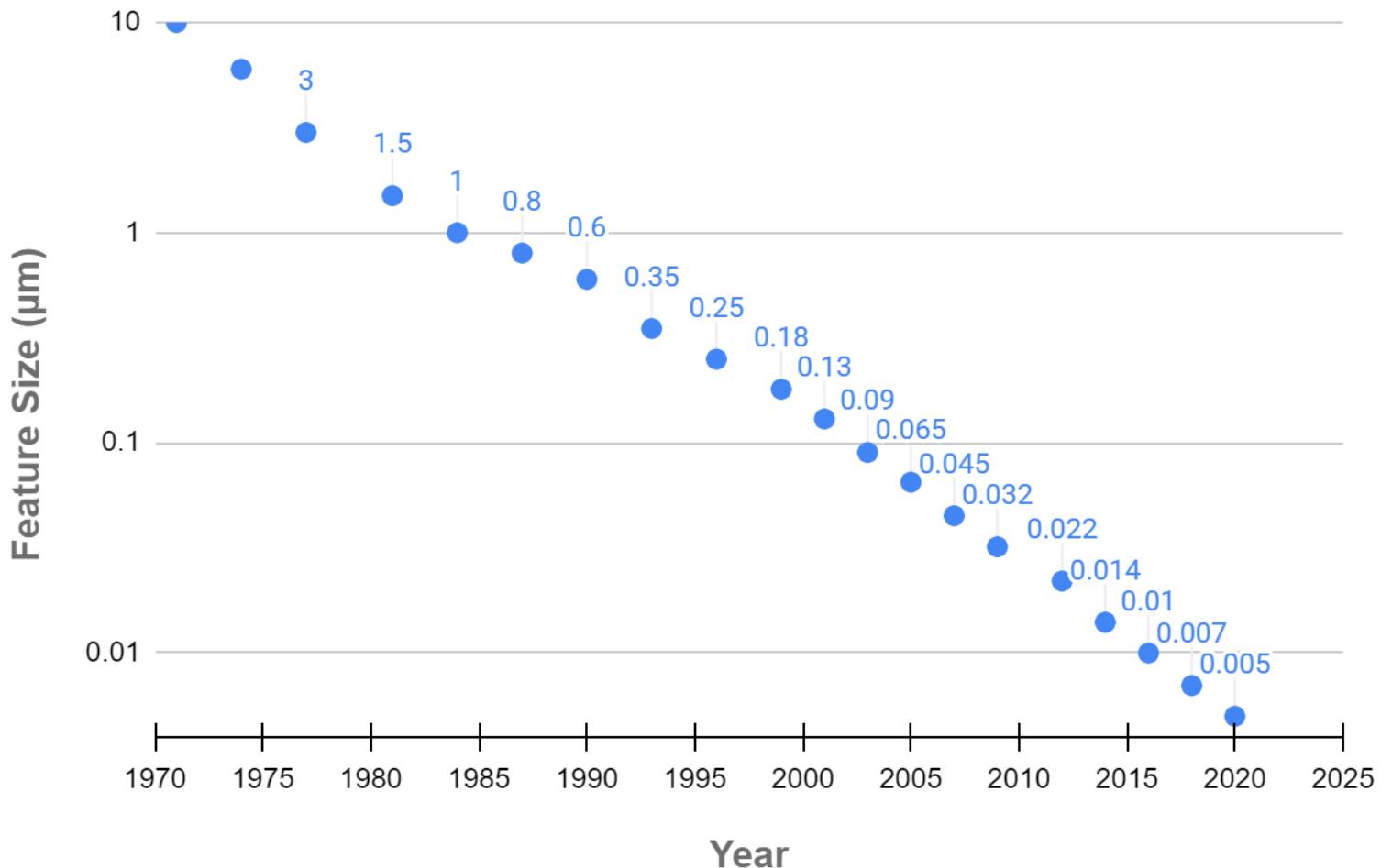
Intel
Museum.
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Intel 4004 4-bit μ Proc

- 1980s-present: CMOS processes for low idle power

Feature Size

- Minimum feature size shrinking 30% every 2-3 years



Clock Speeds

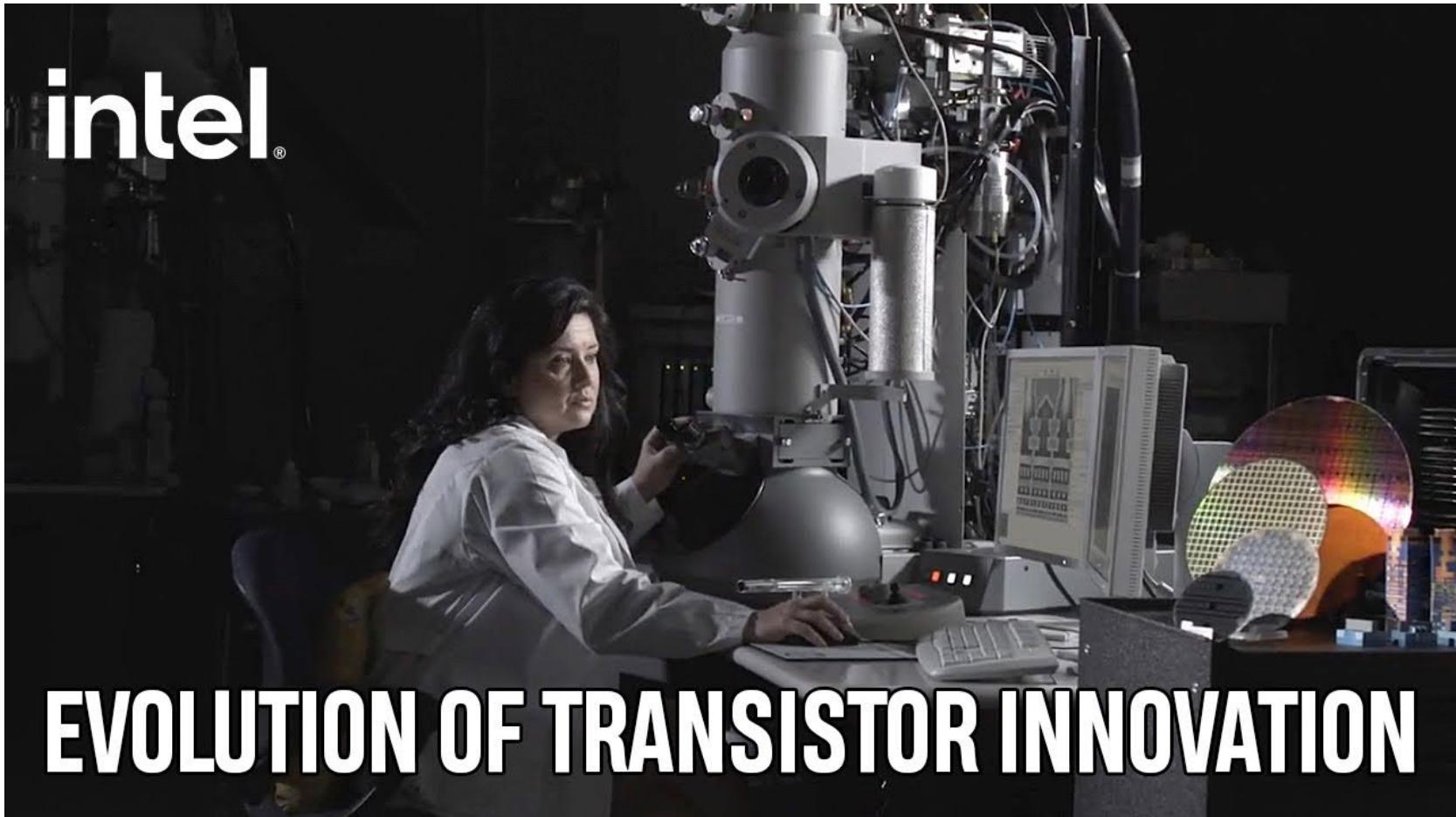
- Many other factors grow exponentially
 - E.g., clock frequency, processor performance

Year	Clock Speed (Hz)	Processor name
1971	740K	4004
1972	500K	8008
1982	6M	80186
1982	8M	80188
1993	66M	Pentium
1999	600M	Pentium III
2000	2G	Pentium 4
2006	2.33G	Core 2 Duo
2008	3.2G	Core i7
2011	2.67G	Xeon E7
2013	4.4G	Intel "Haswell"

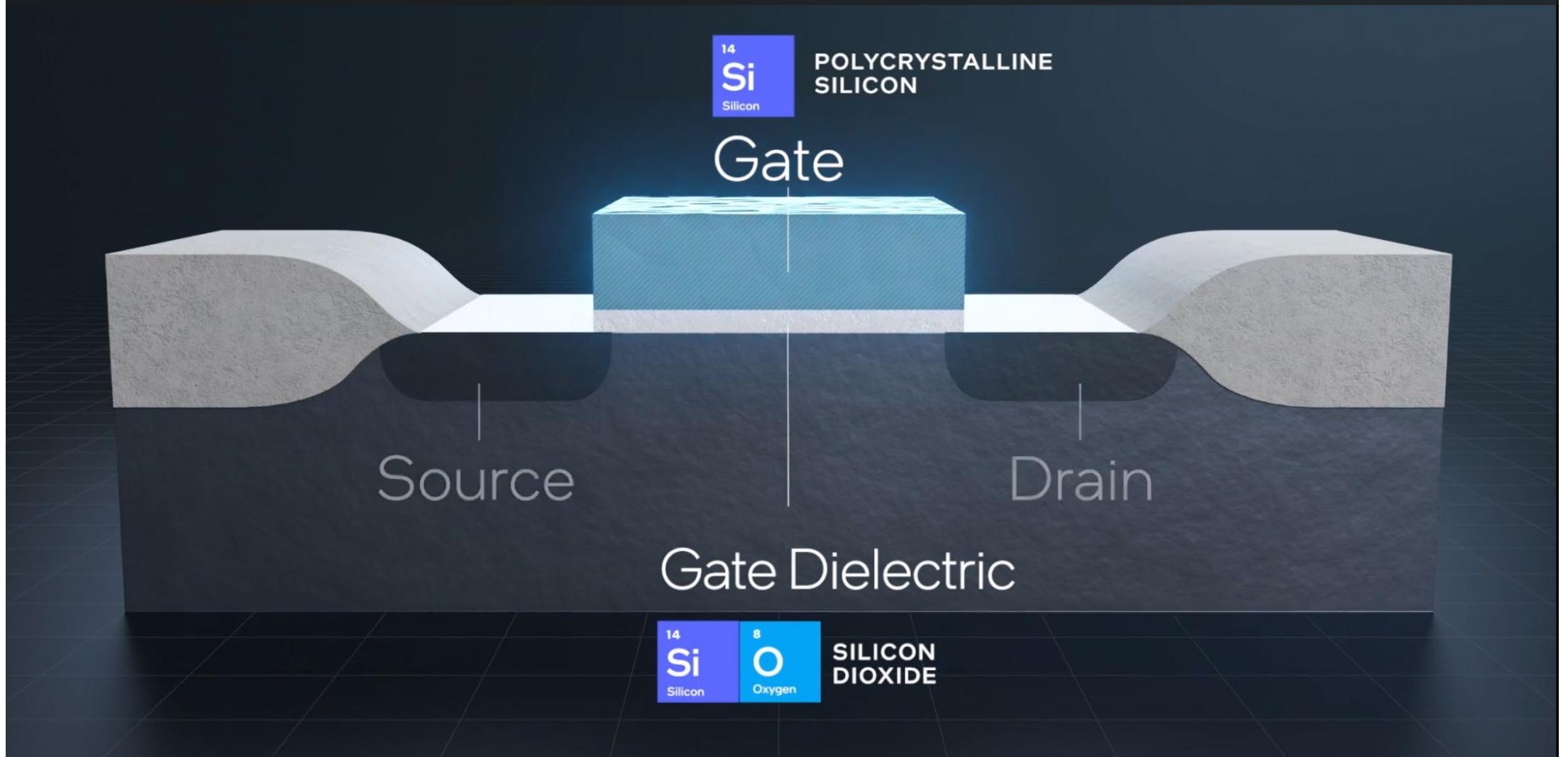
Intel Processors, year and clock speed

Intel's Video

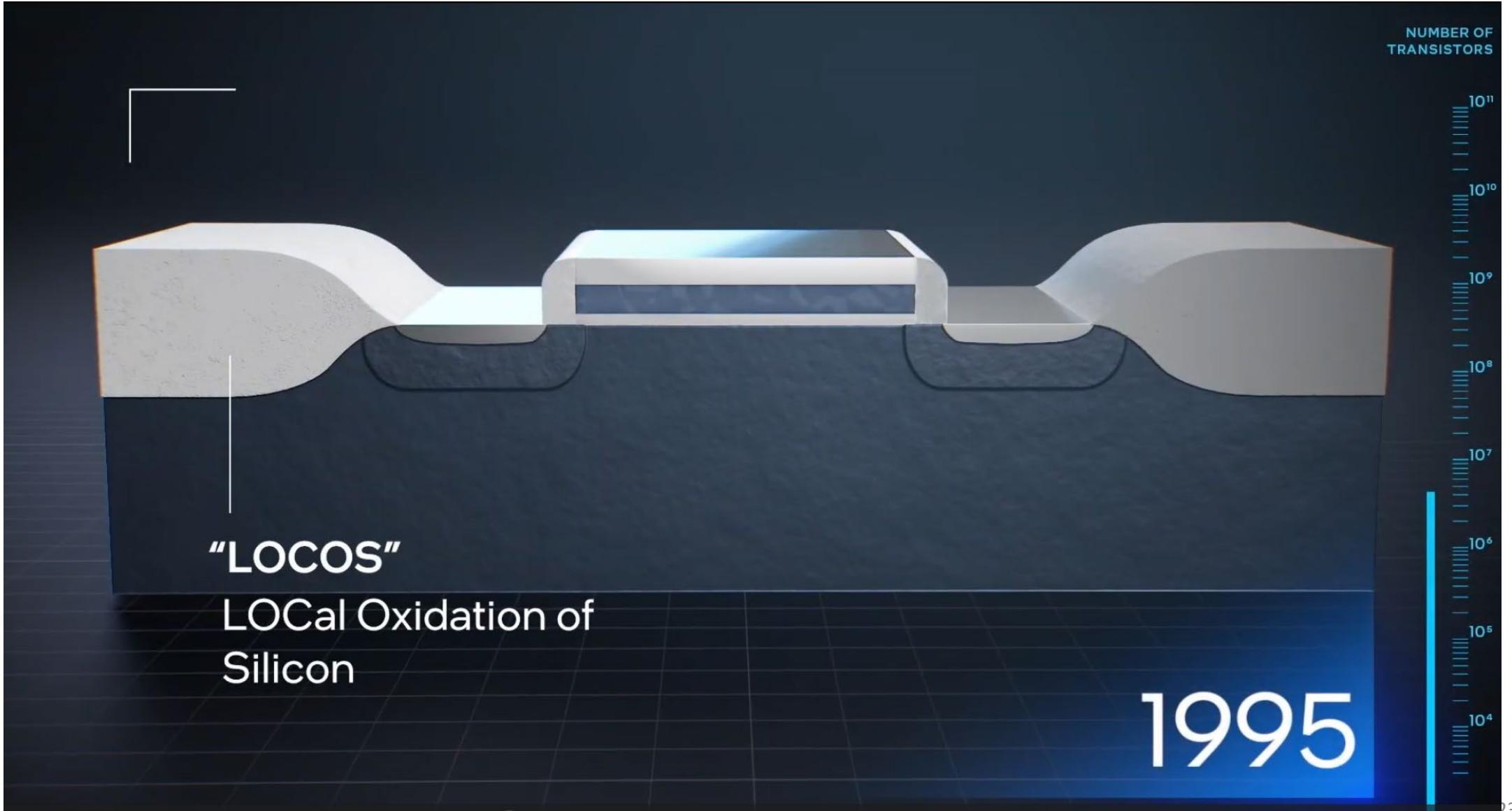
- Intel video (<https://youtu.be/Z7M8etXUEUU>)

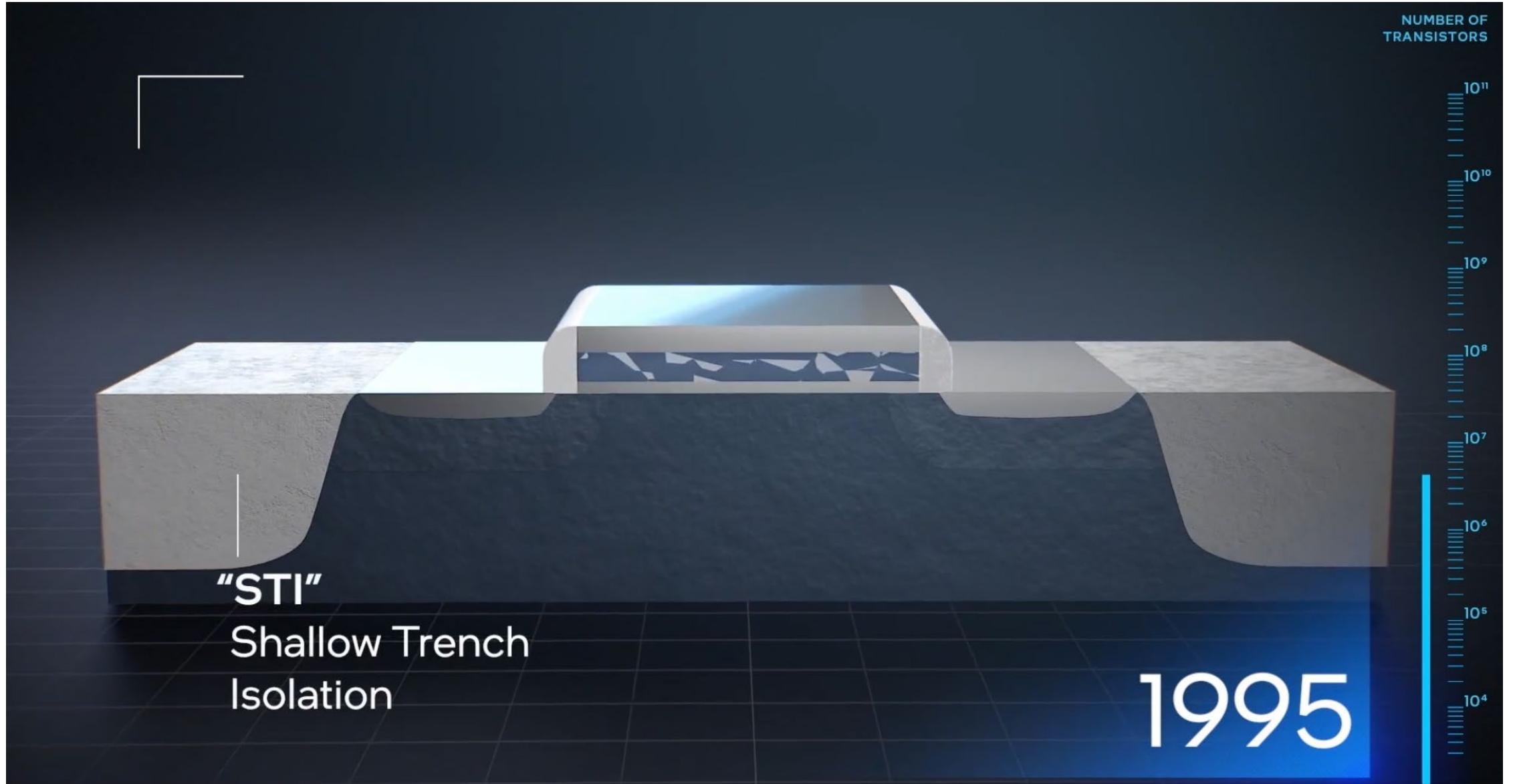


Transistor

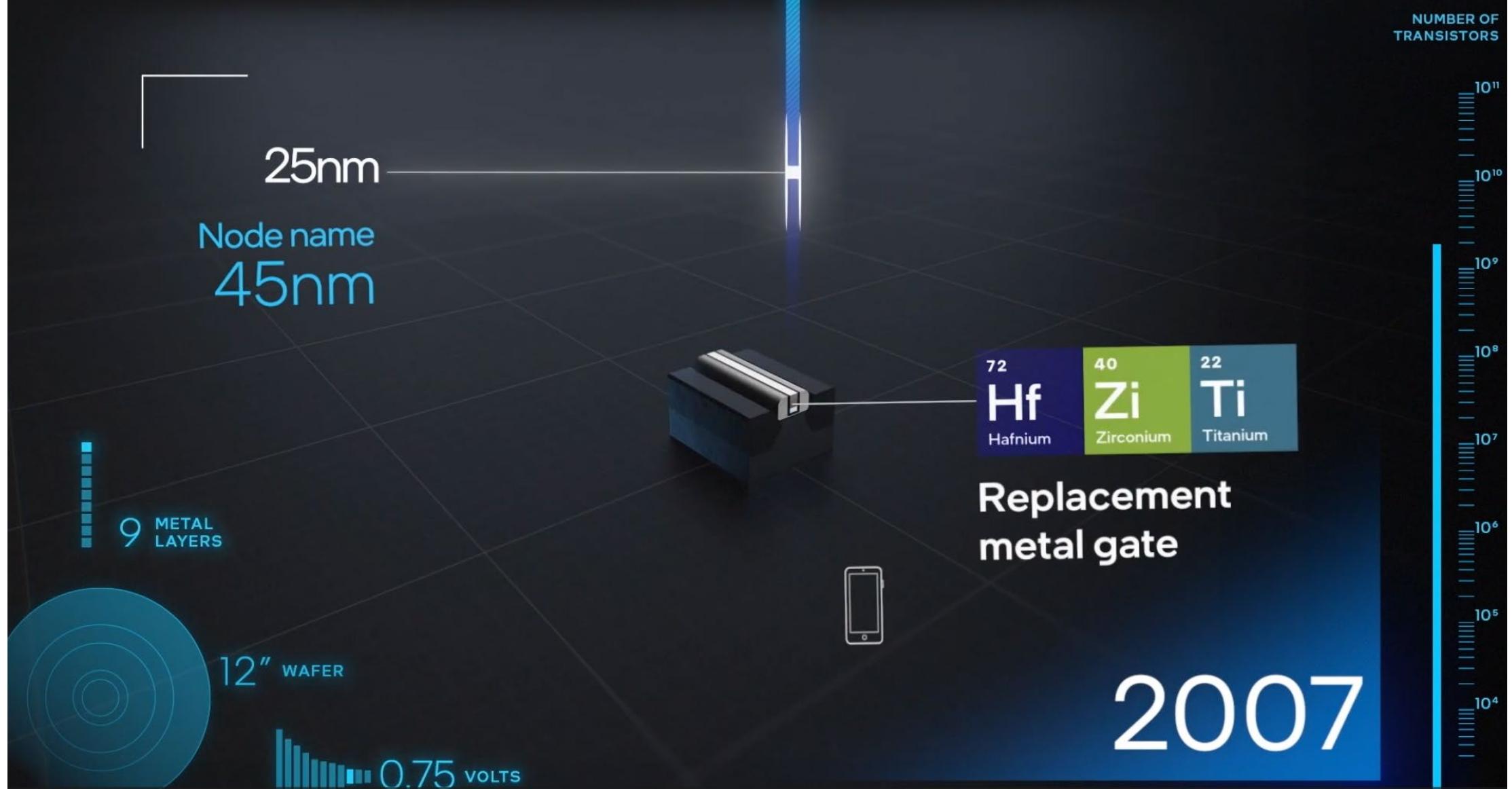


LOCOS

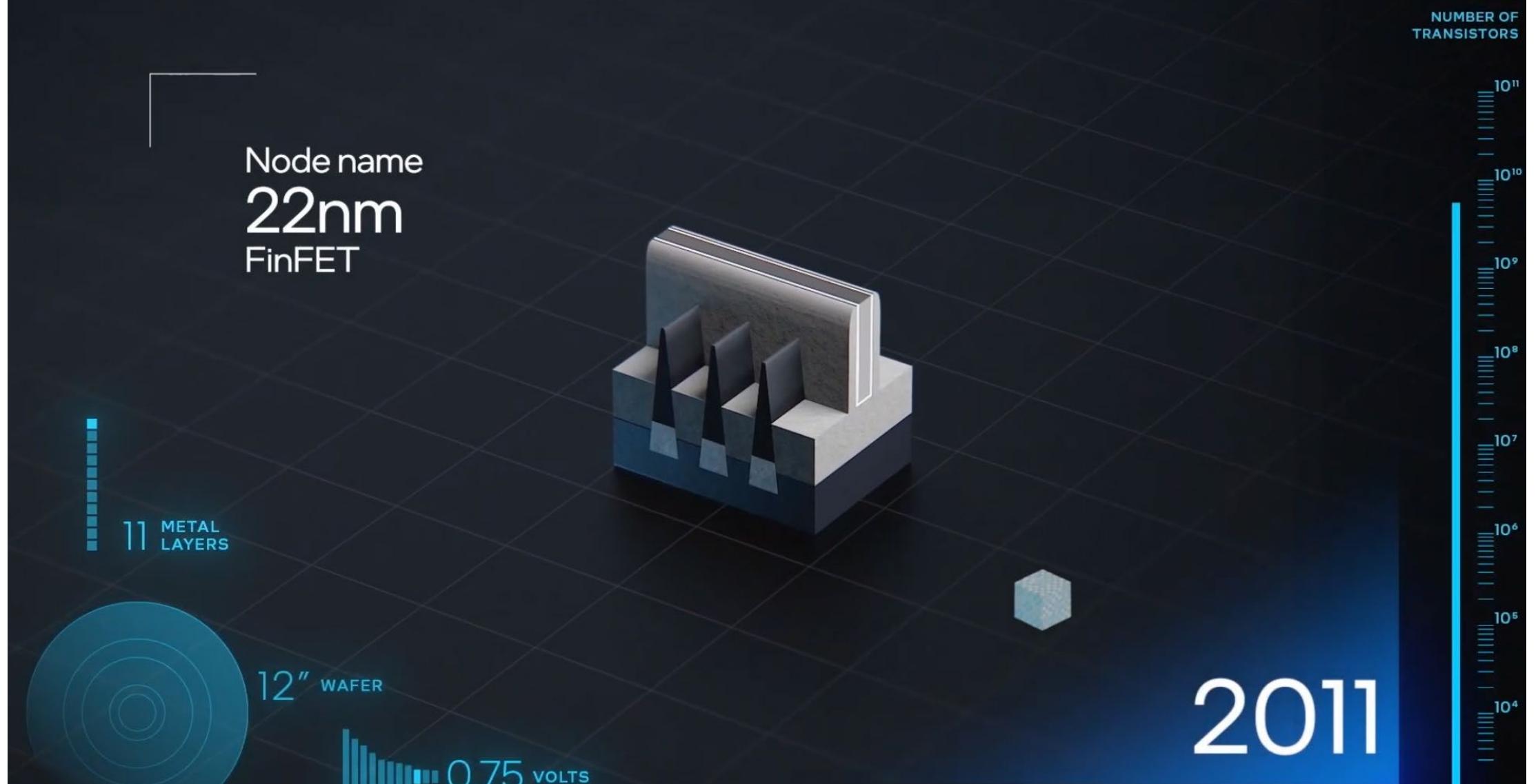




High-K/Metal Gate



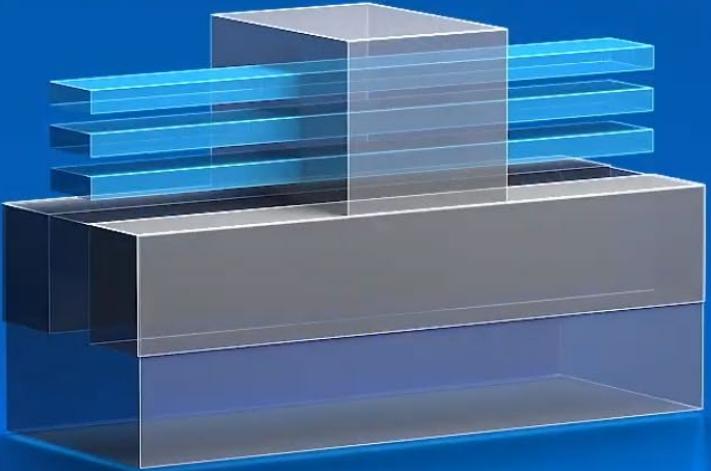
FinFET



RibbonFET

Intel
20A

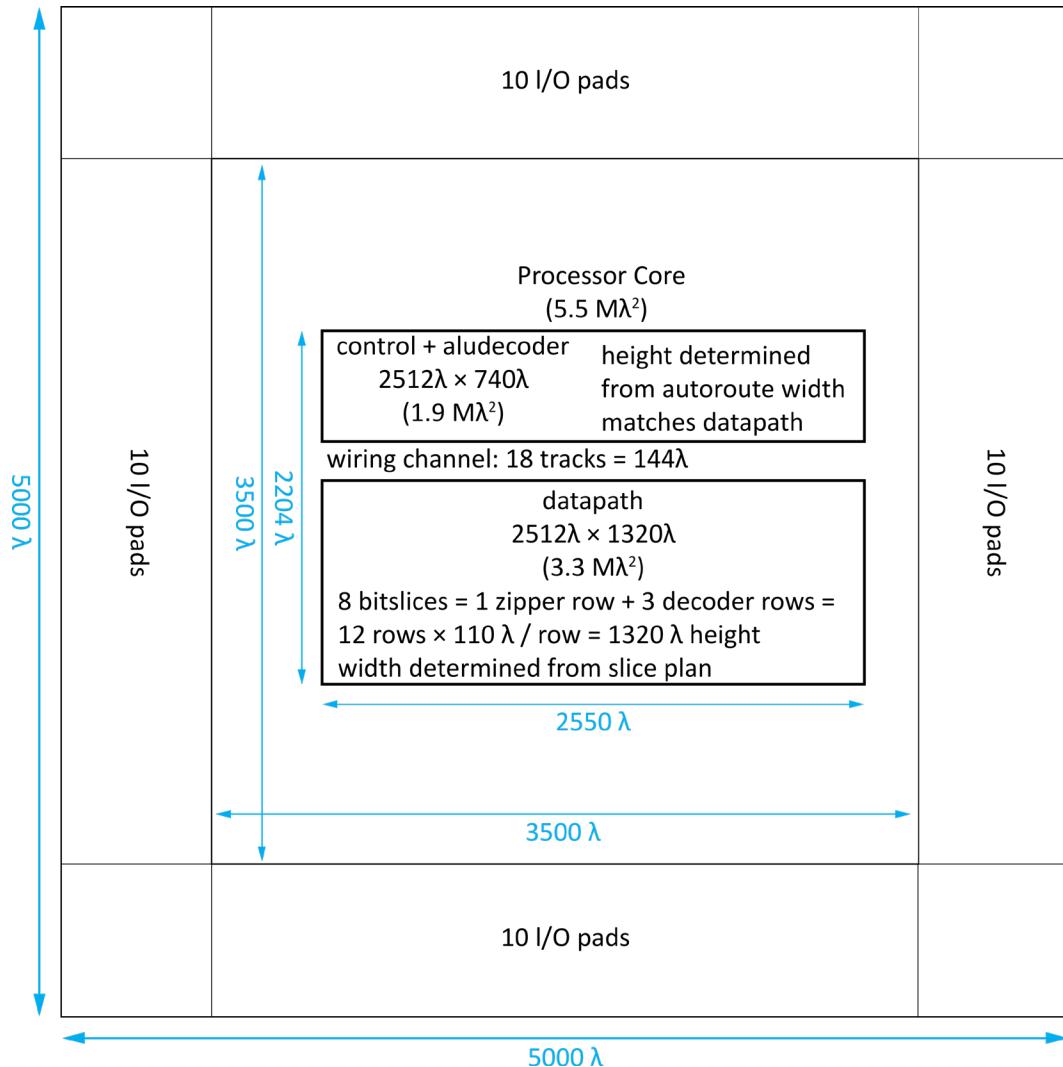
Gate-all-around
RibbonFET



Modern Design Rules

- Rules are expressed in nanometers, not λ
- Lithography becomes difficult when feature size is less than the wavelength of light
- At 16 nm and below, design rules are highly restrictive
 - Layers have preferred directions, and no bends are allowed
 - Only certain widths are allowed
 - Minimum area of each rectangle
 - Complex rules for power busses
 - Thousands of design rules
 - Layout becomes the domain of full-time experts
- But the principles of layout remain valid

Simplified Processor Floorplan

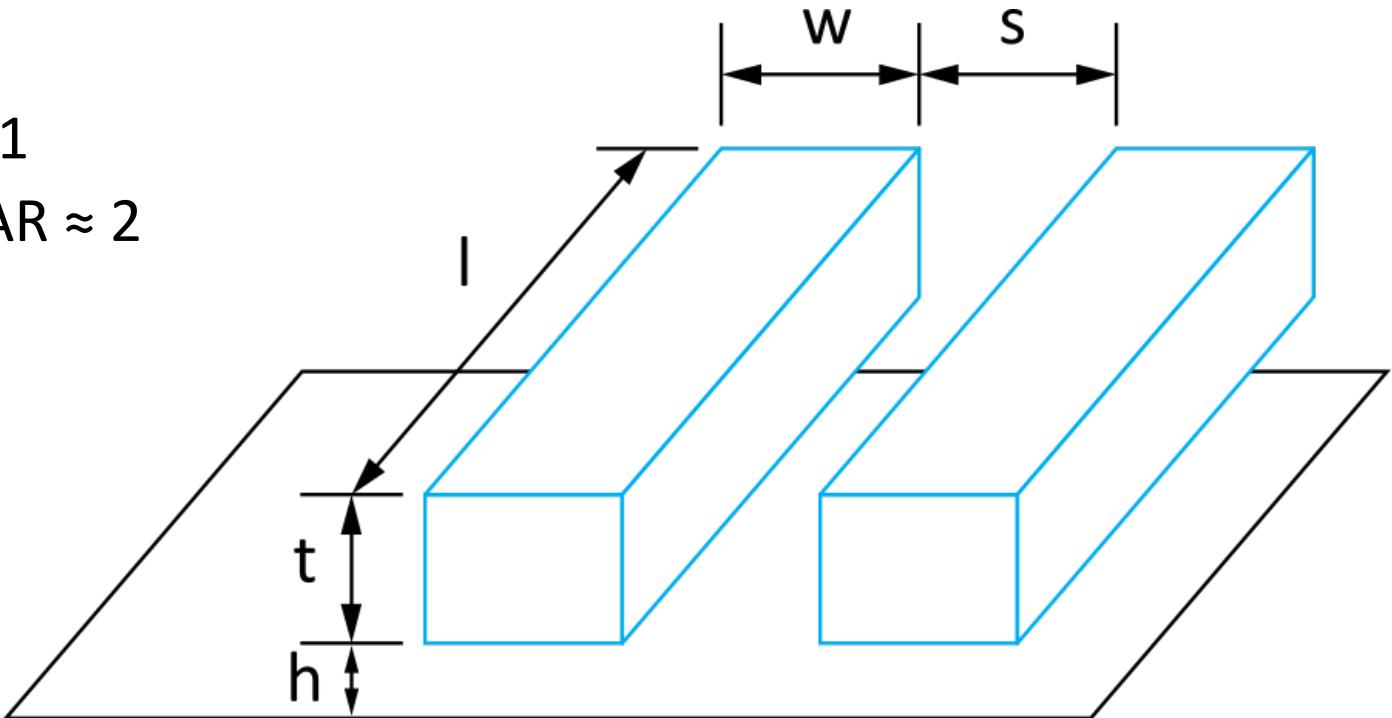


Wires

- Chips are mostly made of wires called *interconnect*
 - In stick diagram, wires set size
 - Transistors are little things under the wires
 - Many layers of wires
- Wires are as important as transistors
 - Speed
 - Power
 - Noise
- Alternating layers run orthogonally

Wires

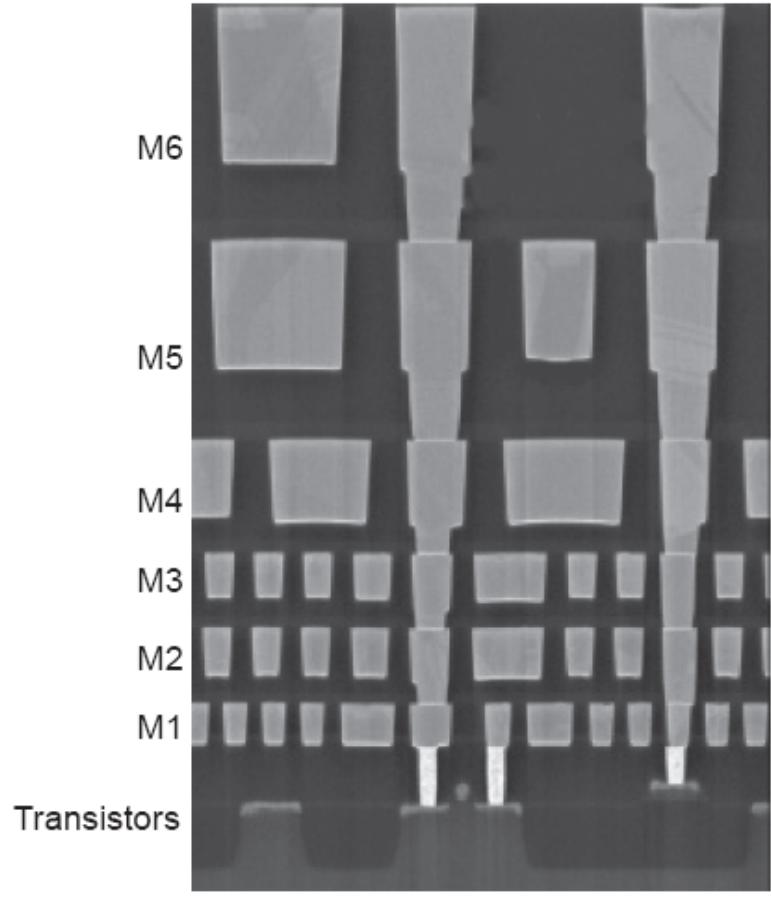
- Pitch = $w + s$
- Aspect ratio: $AR = t/w$
 - Old processes had $AR \ll 1$
 - Modern processes have $AR \approx 2$
 - Pack in many skinny wires



Layer Stack

- AMI 0.6 μm process has 3 metal layers
 - M1 for within-cell routing
 - M2 for vertical routing between cells
 - M3 for horizontal routing between cells
- Modern processes use 6-10+ metal layers
 - M1: thin, narrow ($< 3\lambda$)
 - High-density cells
 - Mid-layers
 - Thicker and wider (density vs. speed)
 - Top layers: thickest
 - For V_{DD} , GND, clk

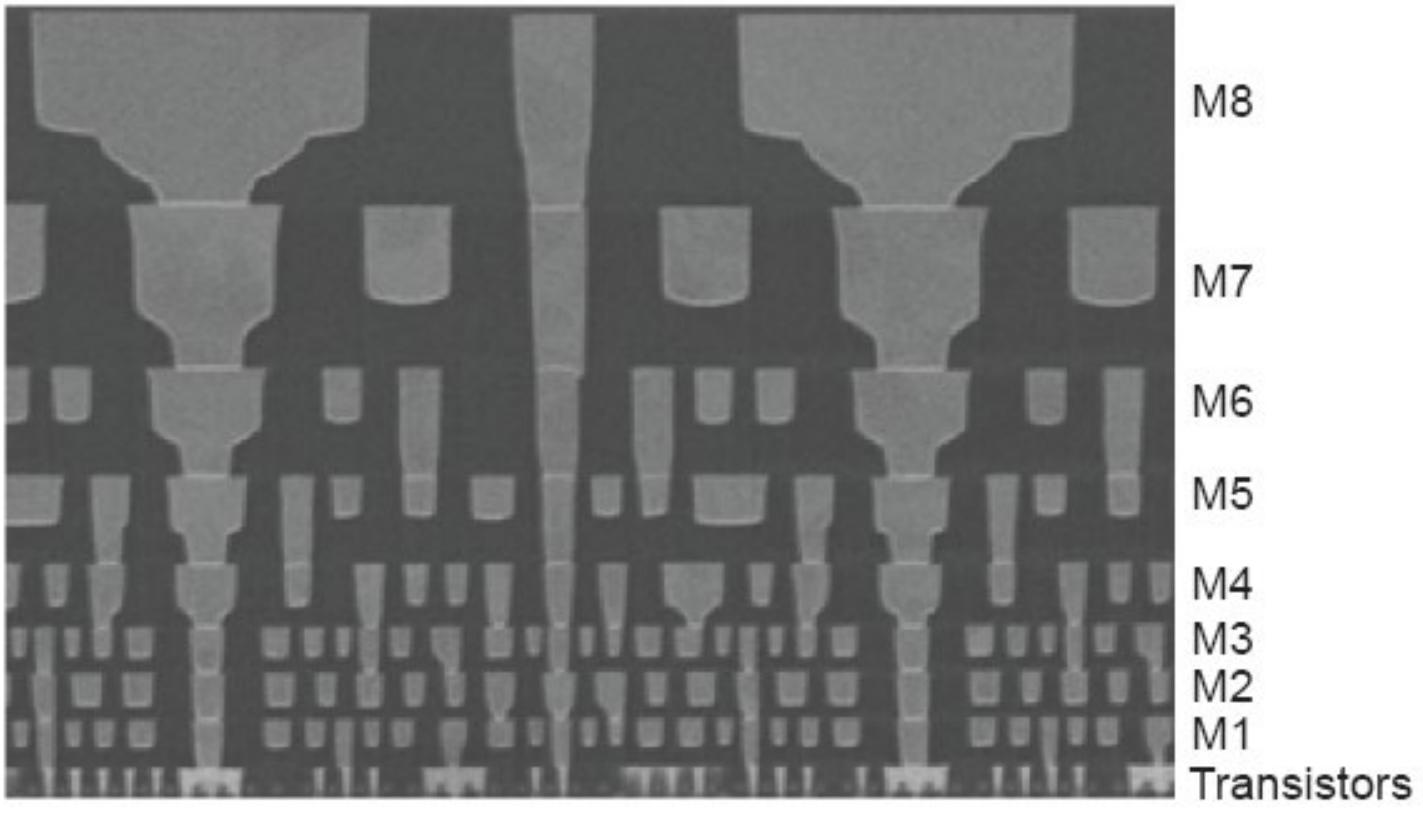
Layer Stack - Example



Intel 90 nm Stack

[Thompson02]

$1 \mu\text{m}$



Intel 45 nm Stack

[Moon08]

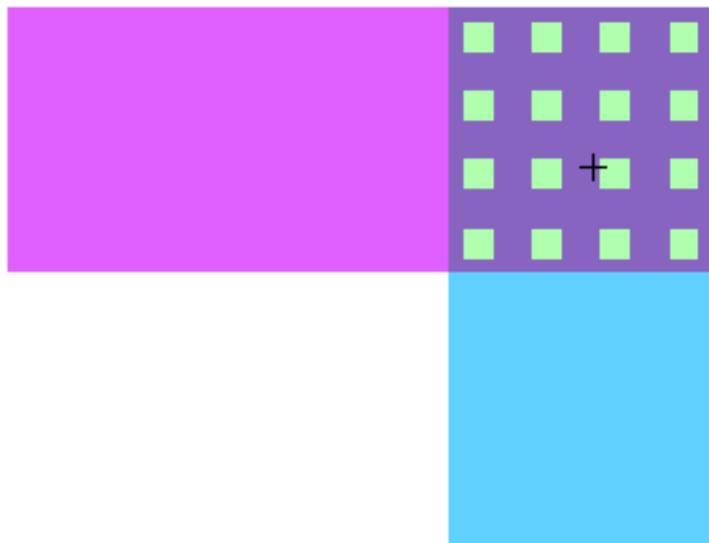
Choice of Metals

- Until 180 nm generation, most wires were aluminum
- Contemporary processes normally use copper
 - Cu atoms diffuse into silicon and damage FETs
 - Must be surrounded by a diffusion barrier

Metal	Bulk resistivity ($\mu\Omega \cdot \text{cm}$)
Silver (Ag)	1.6
Copper (Cu)	1.7
Gold (Au)	2.2
Aluminum (Al)	2.8
Tungsten (W)	5.3
Titanium (Ti)	43.0

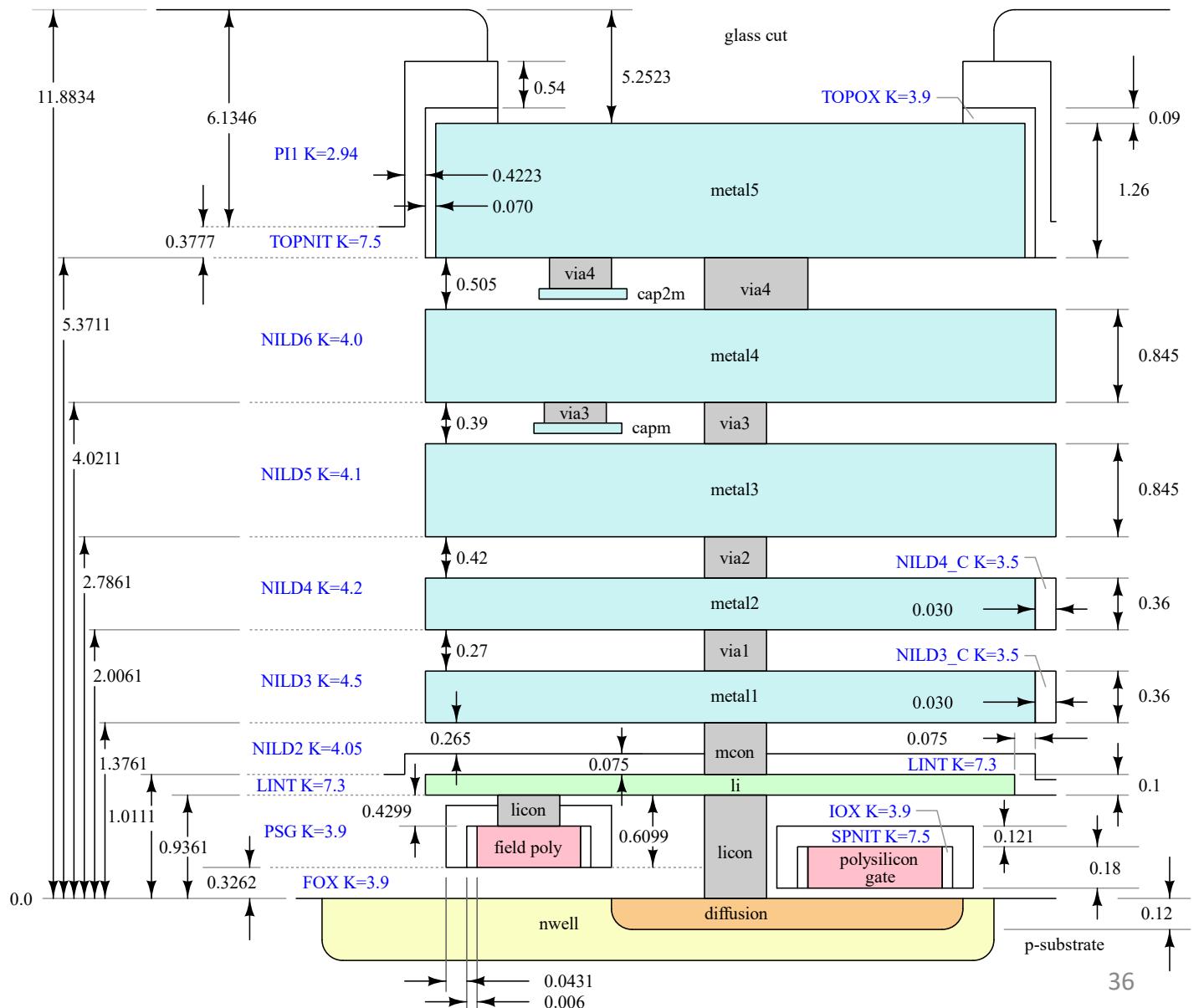
Contacts Resistance

- Contacts and vias also have 2-20 Ω
- Use many contacts for lower R
 - Many small contacts for current crowding around periphery



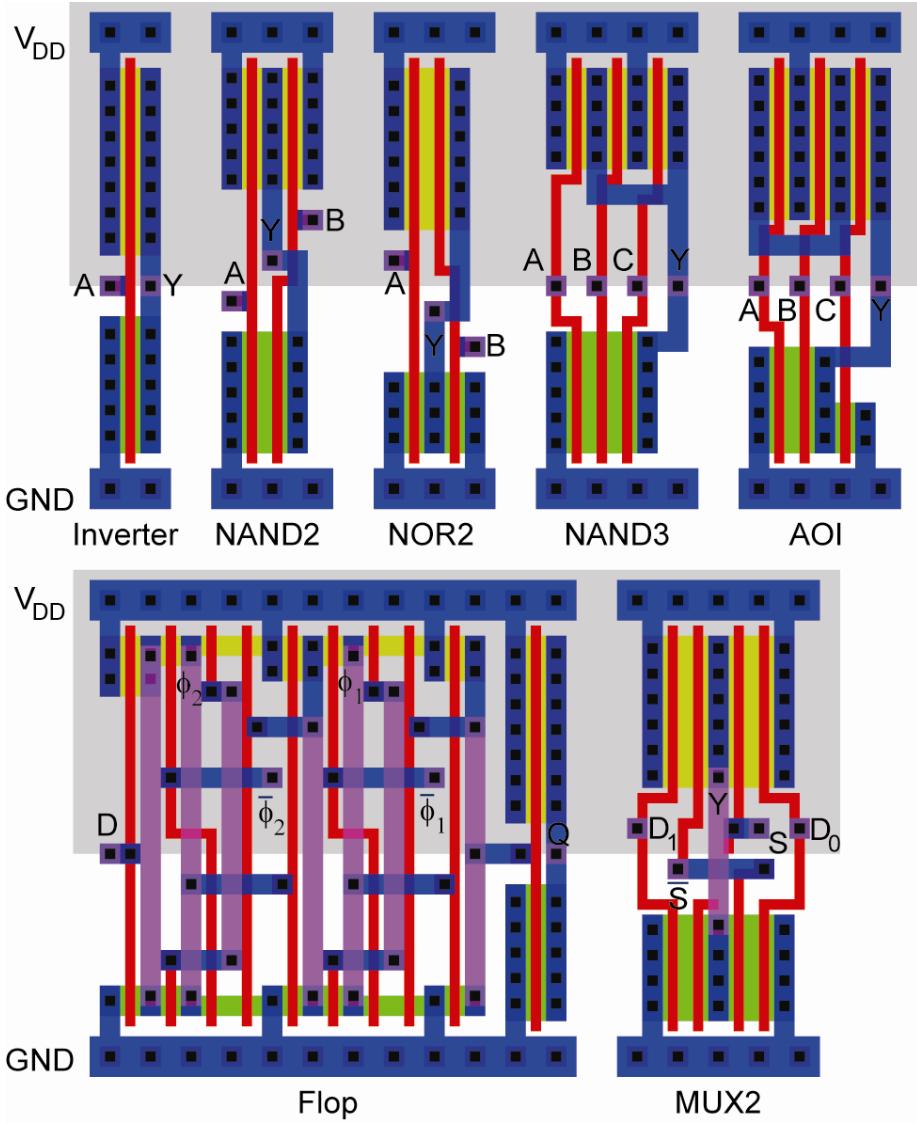
PDK Example

- Skywater: an open-source process development kit
- CMOS 130nm
- Design rules publicly available online
- Apartment analogy
 - Metals are above ground
 - Diffusion are in the basement



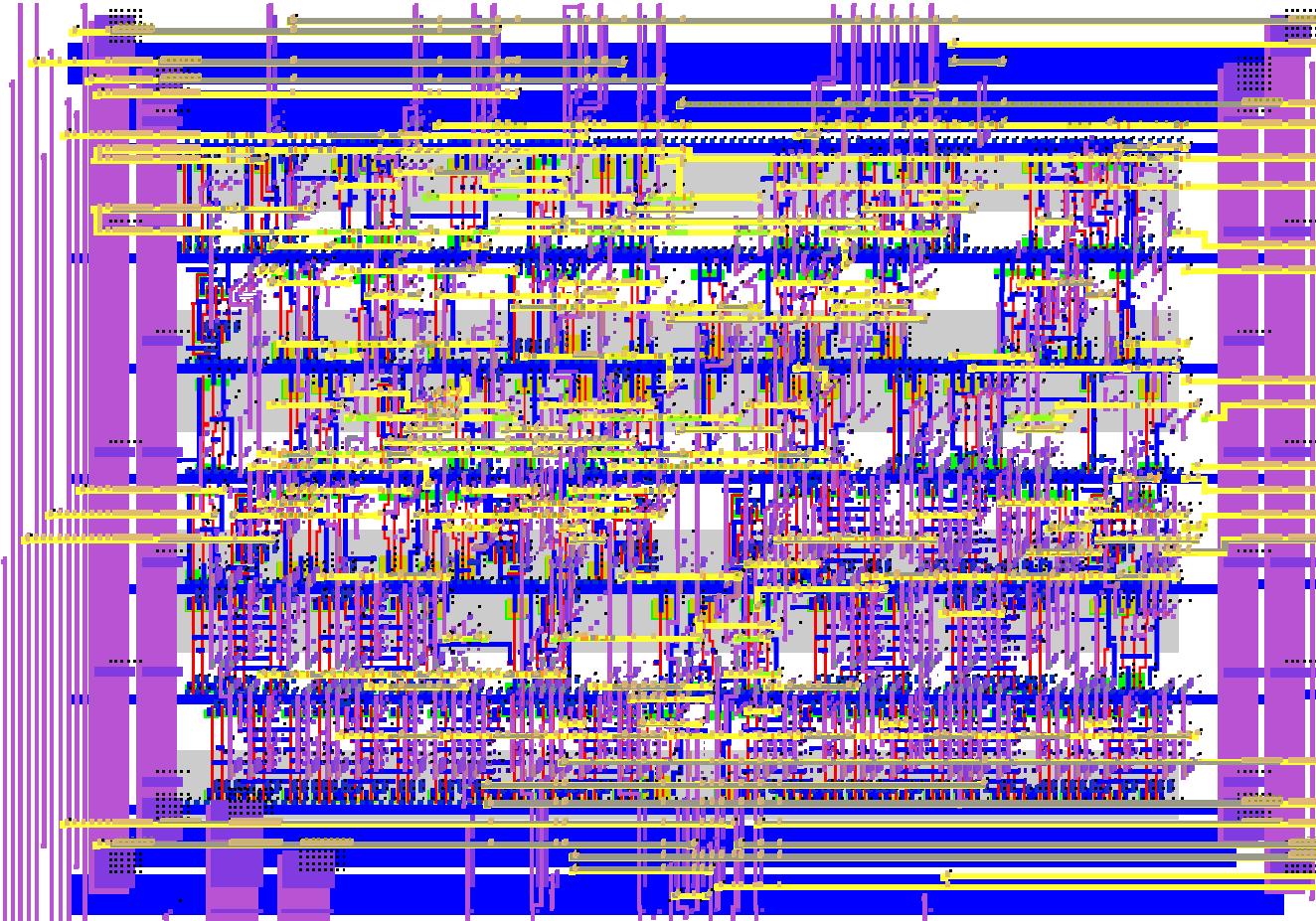
Standard Cells

- Uniform cell height
- Uniform well height
- M1 V_{DD} and GND rails
- M2 Access to I/Os
- Well/substrate taps
- Exploits regularity

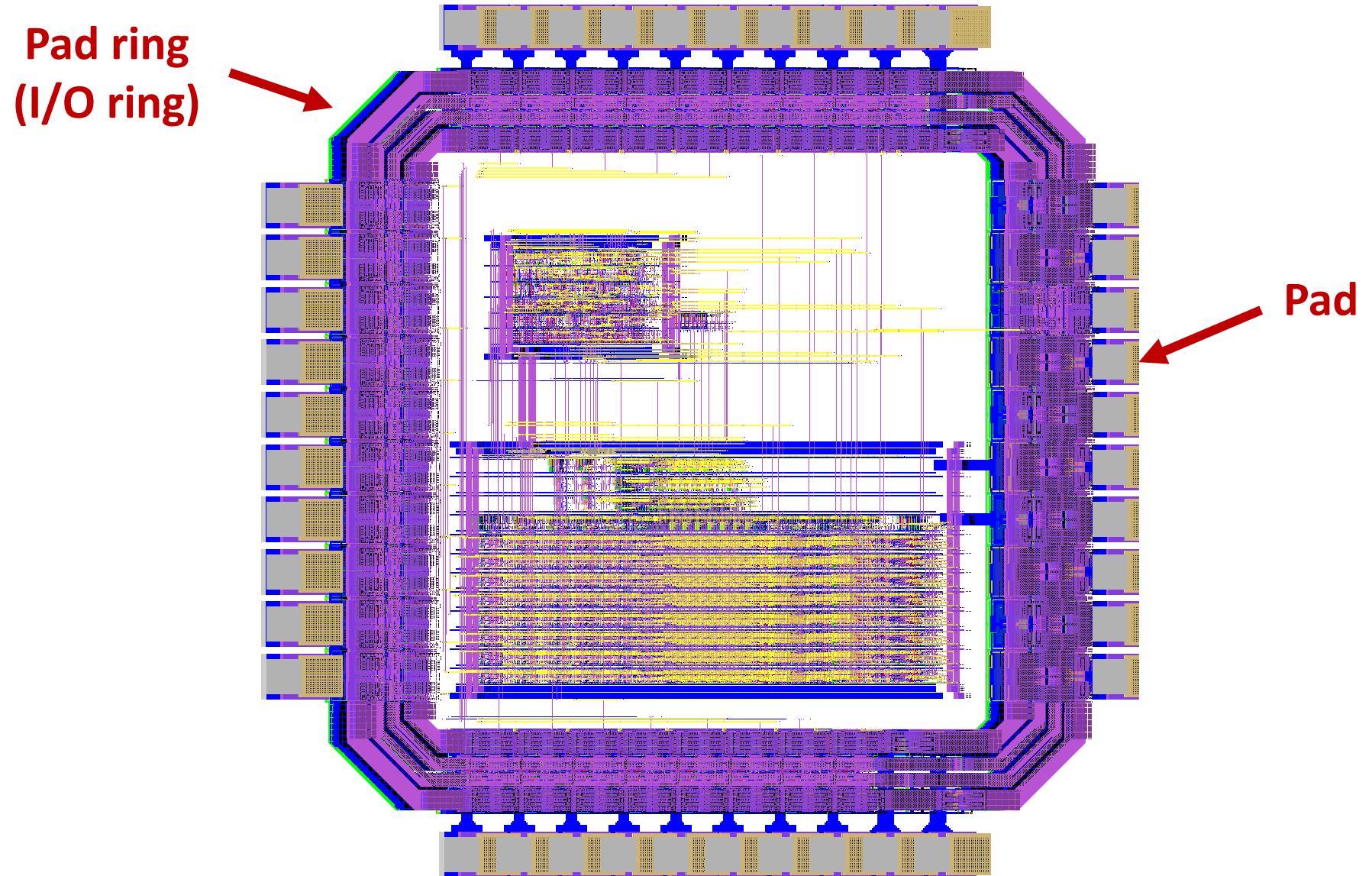


Block-Level Layout

- Synthesize HDL into gate-level netlist
- Place & Route using standard cell library

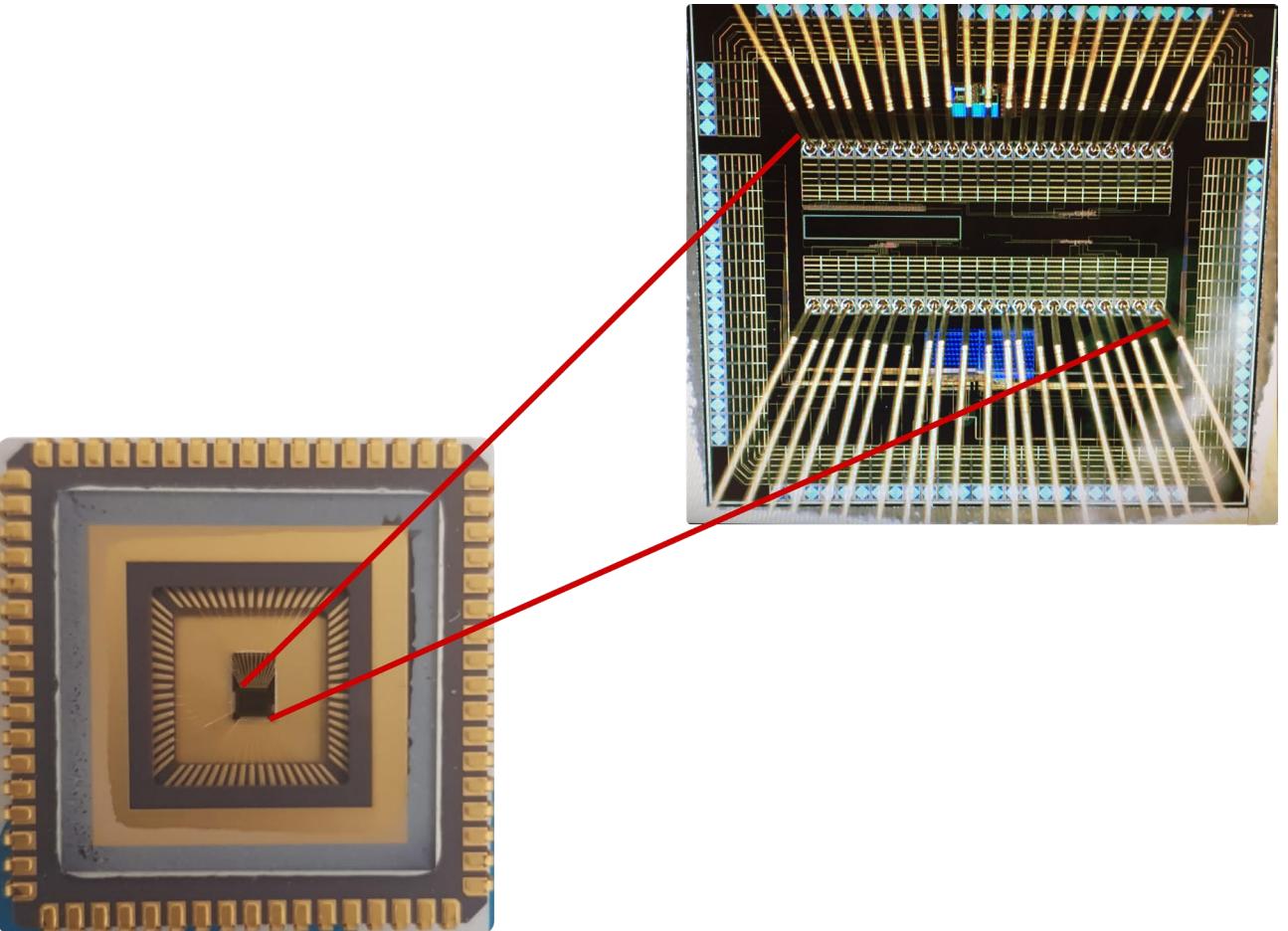


Full-Chip Layout



Packaging

- Tapeout final layout
- Fabrication
 - 6, 8, 12" wafers
 - Optimized for throughput, not latency (10 weeks!)
 - Cut into individual dice
- Packaging
 - Bond gold wires from die I/O pads to package

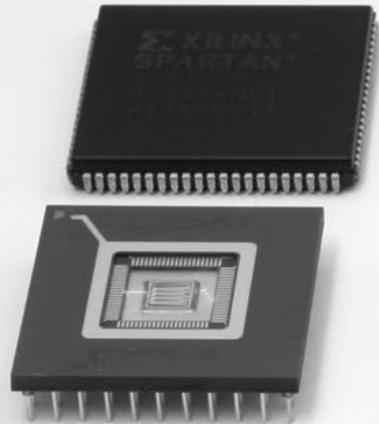


Packaging

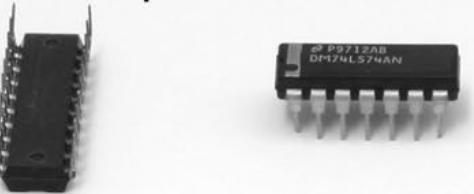
- Package functions
 - Electrical connection of signals and power from chip to board
 - Little delay or distortion
 - Mechanical connection of chip to board
 - Removes heat produced on chip
 - Protects chip from mechanical damage
 - Compatible with thermal expansion
 - Inexpensive to manufacture and test

Package Types

84-pin PLCC



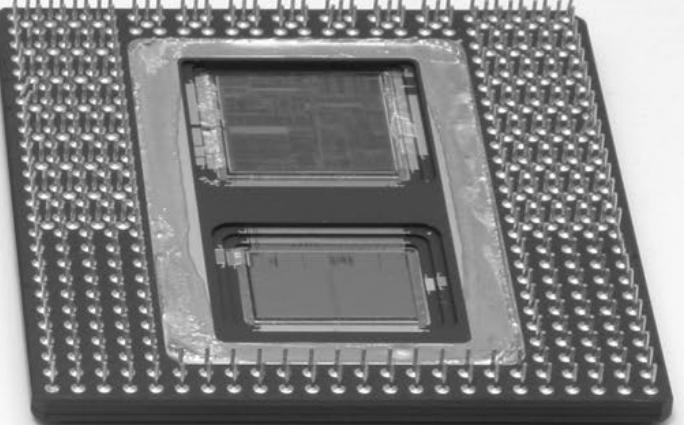
14-pin DIP



44-pin PLCC



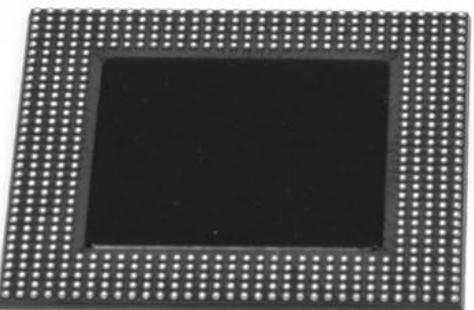
387-pin PGA Multichip Module



84-pin PGA



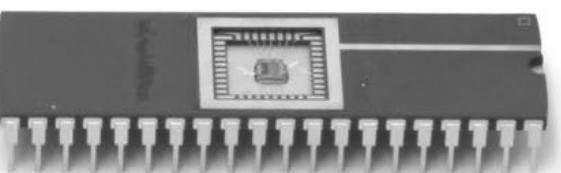
280-pin QFP



86-pin TSOP



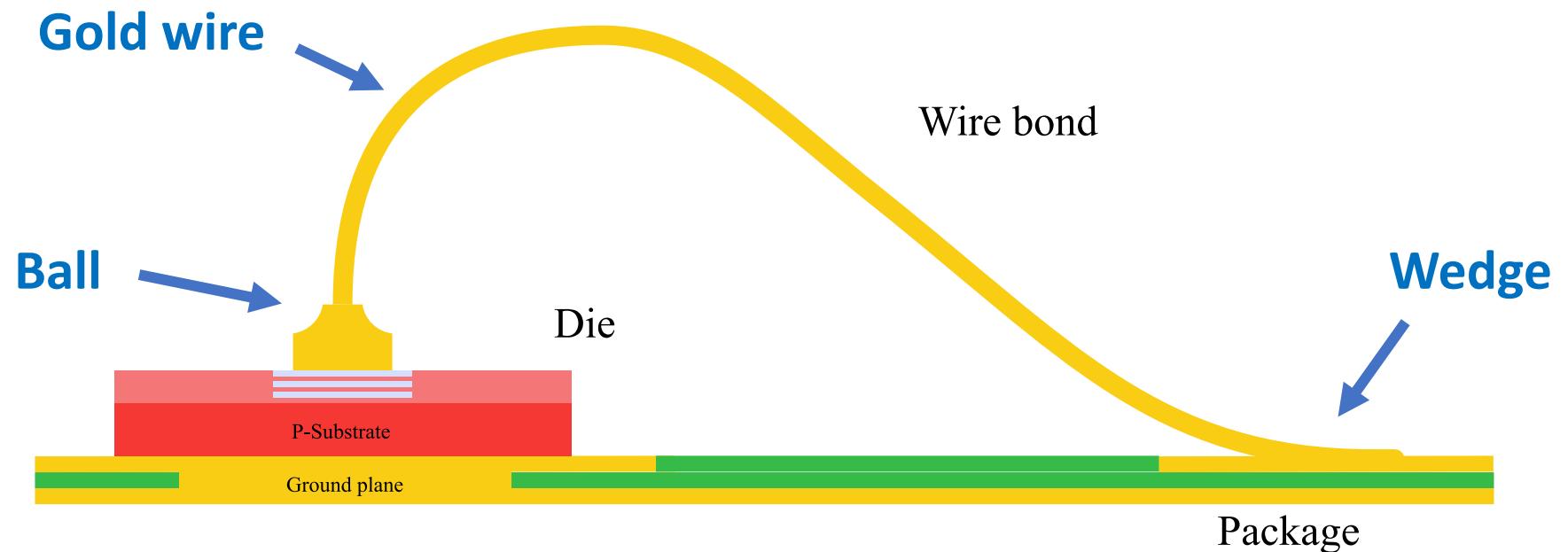
40-pin DIP



560-pin BGA

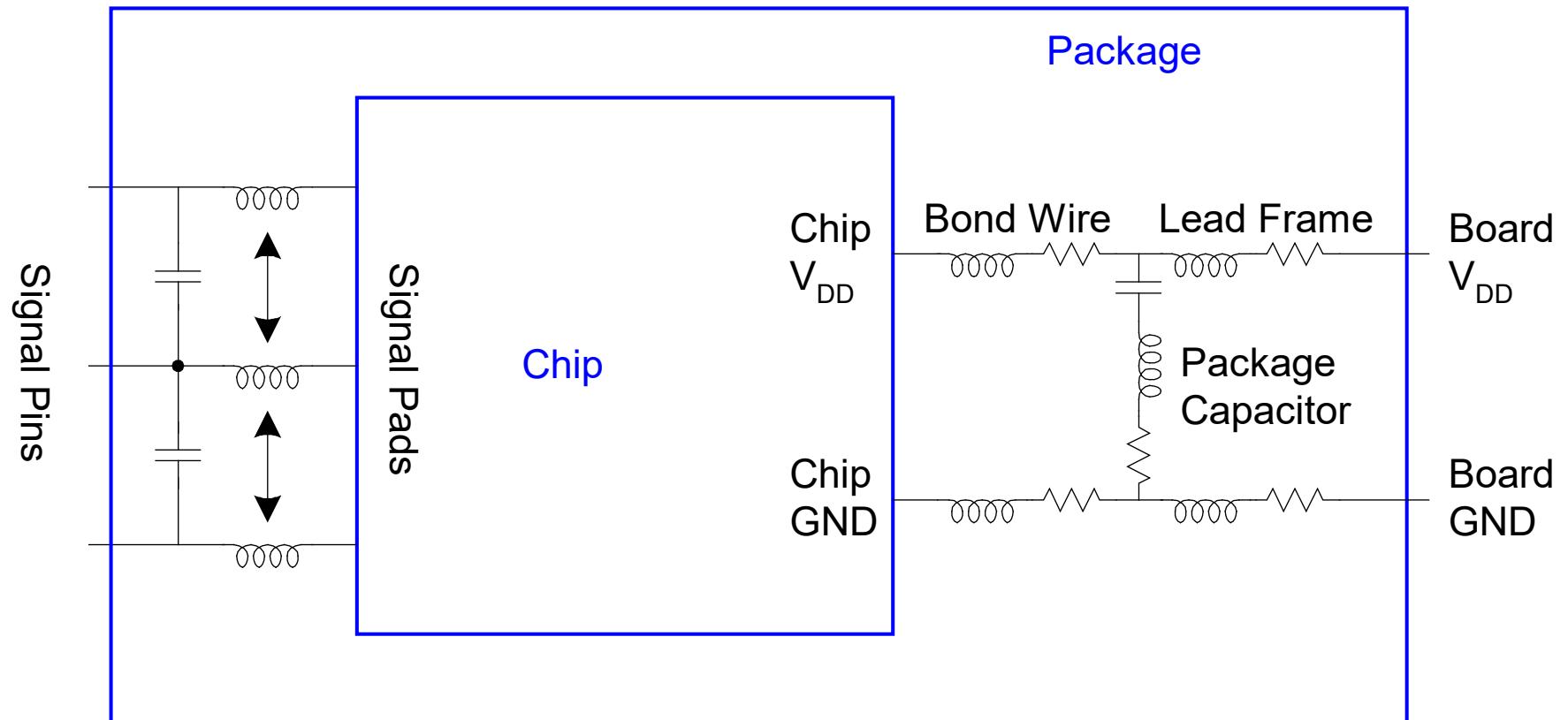
Bonding wires

- Provide connection between the pad on the chip and the pad on the package
- Ball-Wedge gold wire for low currents
- Wedge-Wedge aluminum for high currents



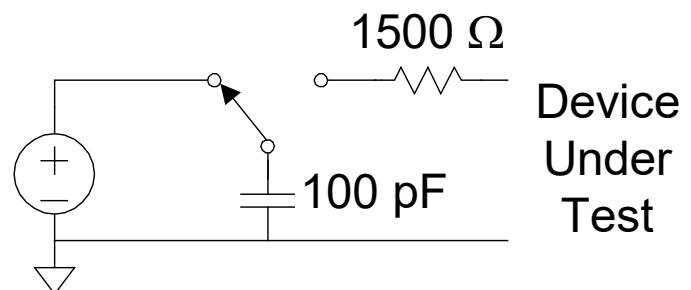
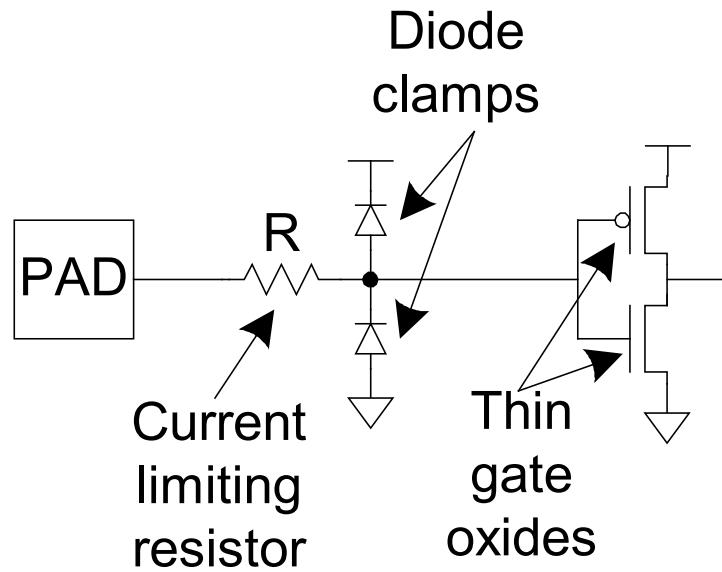
Package Parasitic

- Use many V_{DD} , GND in parallel
 - Inductance, I_{DD}



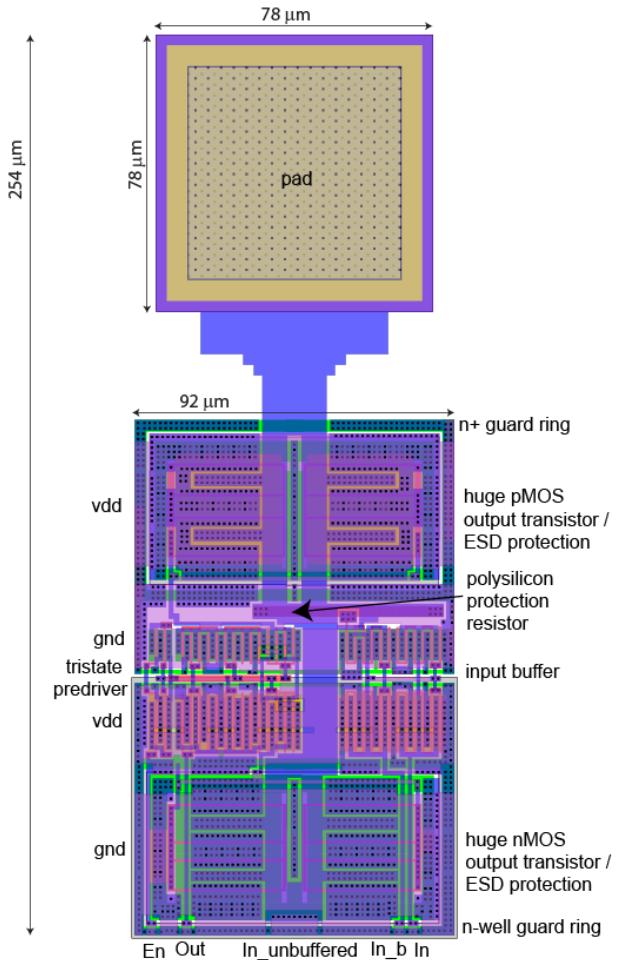
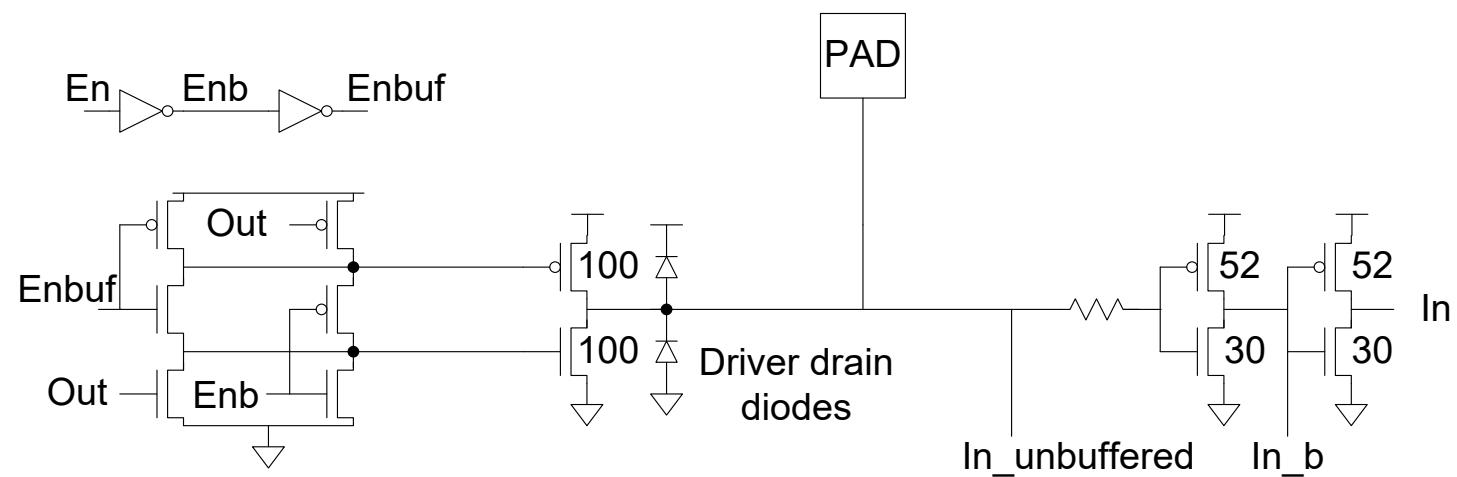
ESD Protection

- Static electricity builds up on your body
 - Shock delivered to a chip can fry thin gates
 - Must dissipate this energy in protection circuits before it reaches the gates
- ESD protection circuits
 - Current limiting resistor
 - Diode clamps
- ESD testing
 - Human body model
 - Views human as charged capacitor



I/O Pads

- 0.6 μm three-metal process
 - Similar I/O drivers
 - Big driver transistors provide ESD protection
 - Guard rings around driver

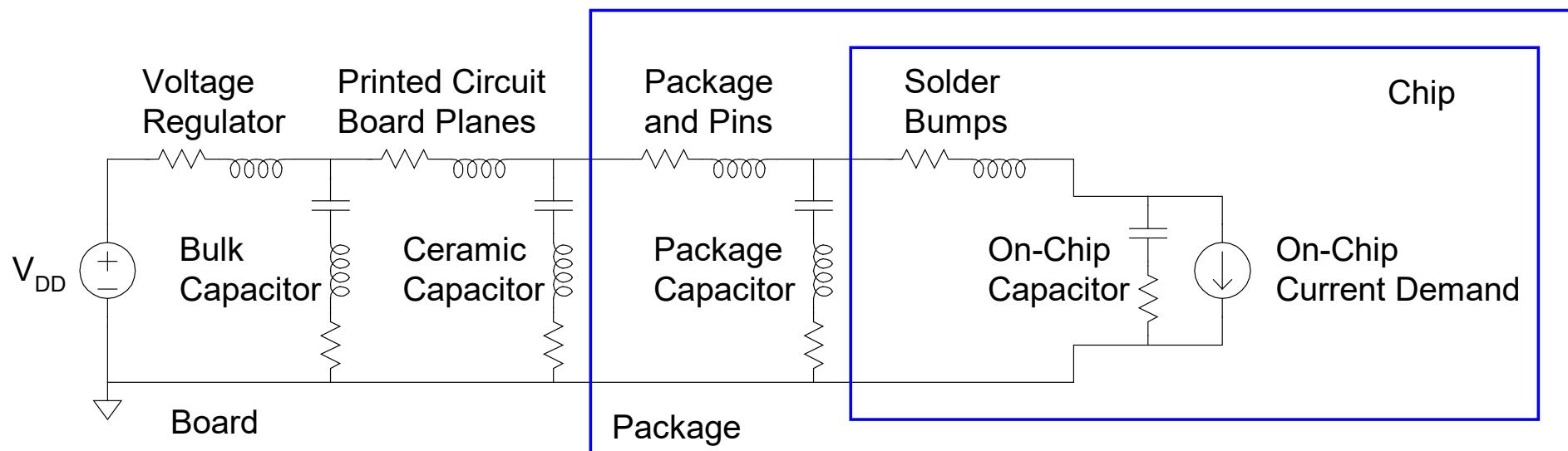


Power Distribution

- Power Distribution Network functions
 - Carry current from pads to transistors on chip
 - Maintain stable voltage with low noise
 - Provide average and peak power demands
 - Provide current return paths for signals
 - Avoid electromigration & self-heating wearout
 - Consume little chip area and wire
 - Easy to lay out

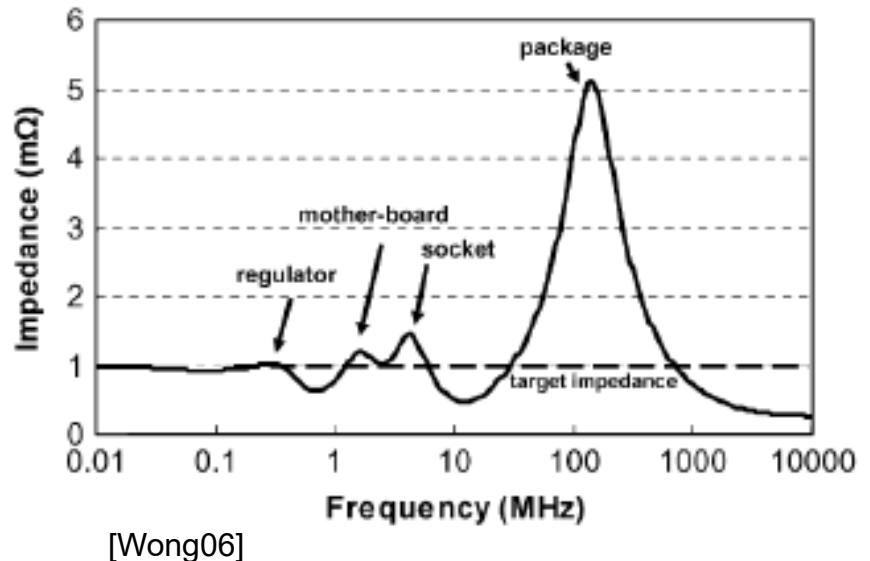
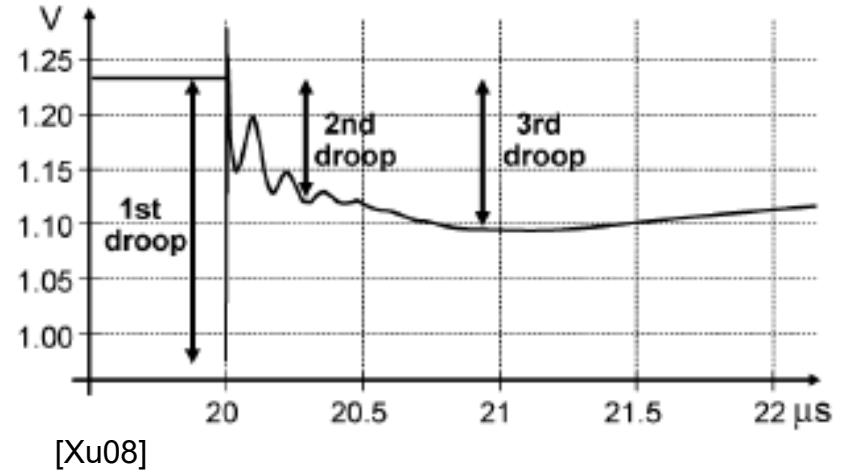
Power System Model

- Power comes from regulator on system board
 - Board and package add parasitic R and L
 - Bypass capacitors help stabilize supply voltage
 - But capacitors also have parasitic R and L
- Simulate system for time and frequency responses



Example: Pentium 4

- Power supply impedance for Pentium4
 - Spike near 100 MHz caused by package inductance L
- Step response to sudden supply current chain
 - 1st droop: on-chip bypass caps
 - 2nd droop: package capacitance
 - 3rd droop: board capacitance



[Wong06]

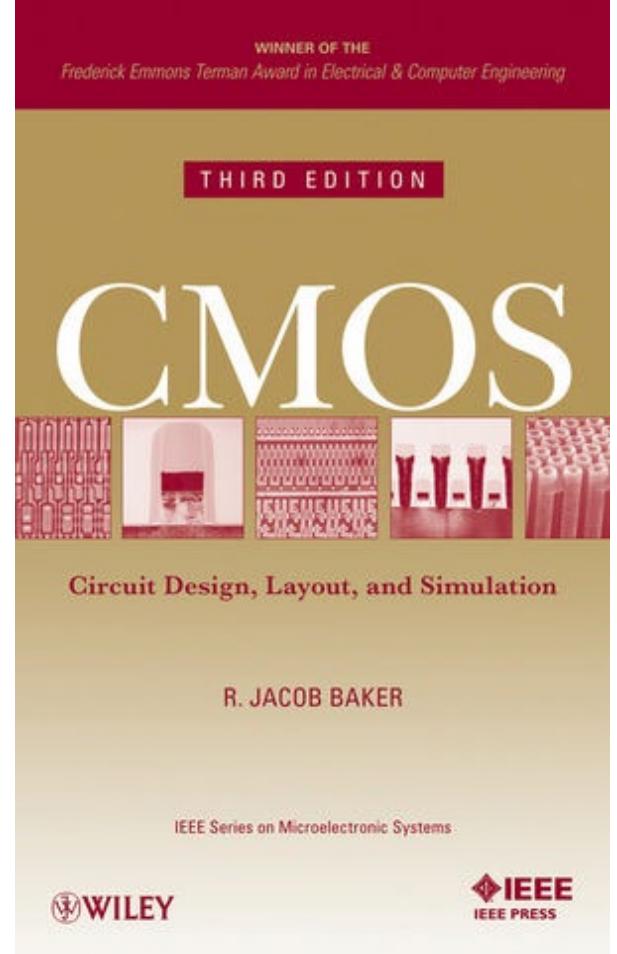
More info on fab

- LTT video: <https://www.youtube.com/watch?v=2ehSCWoaOqQ>



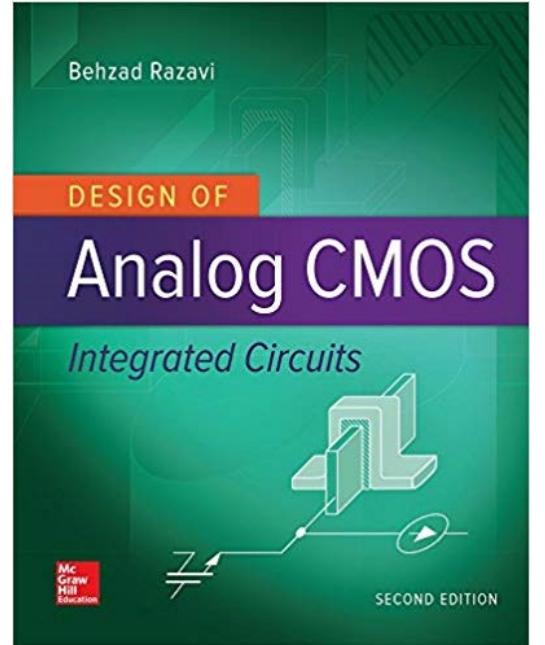
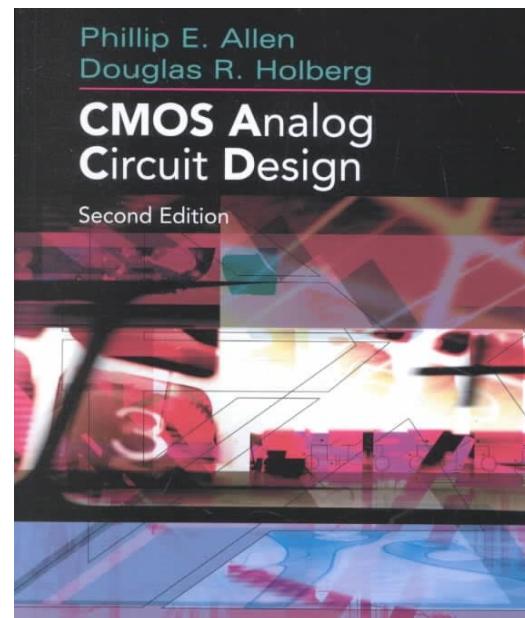
Reference material

- CMOS: Circuit Design, Layout, and Simulation, Third Edition
- By R. Jacob Baker
- Online access via UoE library
- <https://onlinelibrary.wiley.com/doi/book/10.1002/9780470891179>
- If out of UoE network, then login via Shibboleth
- See <http://cmosedu.com> for more material



Reference material

- Design of Analog CMOS Integrated Circuits,
by Behzad Razavi
- CMOS Analog Circuit Design,
By P. Allen, D. Holberg



Chip Images

- Let's see few real-world examples