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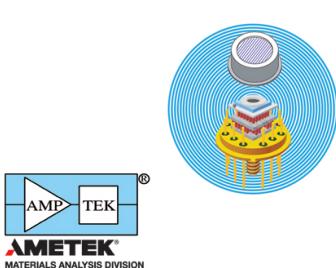
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Room-temperature single dopant atom quantum dot transistors in silicon, formed by field-emission scanning probe lithography

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Electrical operation of room-temperature (RT) single dopant atom quantum dot (QD) transistors, based on phosphorous atoms isolated within nanoscale SiO₂ tunnel barriers, is presented. In contrast to single dopant transistors in silicon, where the QD potential well is shallow and device operation limited to cryogenic temperature, here, a deep (~ 2 eV) potential well allows electron confinement at RT. Our transistors use ~ 10 nm size scale Si/SiO₂/Si point-contact tunnel junctions, defined by scanning probe lithography and geometric oxidation. “Coulomb diamond” charge stability plots are measured at 290 K, with QD addition energy ~ 0.3 eV. Theoretical simulation gives a QD size of similar order to the phosphorous atom separation ~ 2 nm. Extraction of energy states predicts an anharmonic QD potential, fitted using a Morse oscillator-like potential. The results extend single-atom transistor operation to RT, enable tunneling spectroscopy of impurity atoms in insulators, and allow the energy landscape for P atoms in SiO₂ to be determined. *Published by AIP Publishing.*

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I. INTRODUCTION

Single dopant transistors in silicon (Si),^{1–12} where the device electrical characteristics are controlled by discrete electron energy states associated with individual dopant atoms, reduce the active element in electronic devices to the one- or few-atom level. These devices are of great promise for the implementation of quantum nanoelectronic circuits,¹² fabrication of spin-qubits in Si for quantum computation,^{13,14} and probing the physics of a single or a few impurity atoms in semiconductors.¹⁵ Single-dopant transistors may be defined using nanoscale Si field-effect transistors (1–9) such as Si nanowire (NW) FETs⁷ or FinFETs,⁵ where the doping concentration and FET channel dimensions are chosen to be such that one or only a few dopant atoms exist at some point along the Si channel.⁵ The dopants then form single atom quantum dots (QDs), measurable at cryogenic or milli-Kelvin (mK) temperatures near the device threshold voltage. Resonant tunneling and Coulomb charging effects are then observed, associated with the electron states lying within the shallow (~ 100 meV or less⁵) potential well of single donor (phosphorous⁶ or arsenic¹) or acceptor (boron⁸) atoms. Some influence of the stochastic variation in dopant number and location can persist even at room temperature (RT).⁵ Single-atom electronic devices operating with one and two tunnel coupled dopants,^{16,17} electron charge pumping through two dopants,¹⁸ and spin-qubit devices have now all been demonstrated.^{13,14}

At present, control over the electronic states in the shallow potential well of a donor or acceptor impurity atom in a Si FET channel has provided the main route for single-atom electronics, as the channel can retain good conductivity at cryogenic temperatures and the impurity states couple strongly, via resonant tunneling, to the conduction path.¹² In contrast, the electronic states of impurity atoms embedded within an insulator are poorly understood, as the measurement of these is more complex due to lower conductivity of the insulator, disorder within the insulator, and difficulty in tunnel coupling to these states.¹² In the case of a distribution of impurity atoms where trapped charges interact over length scales spanning multiple impurities, a Coulomb glass can also form.^{19,20} This creates a universal Coulomb gap, pinned at the Fermi energy, which may prevent full electrical control over the impurity states. However, an impurity atom lying within an insulator has the major advantage of creating a very deep potential well, where depth $D_e \gg k_B T = 25$ meV at RT. The electronic states in the well can then be measured at RT, raising the possibility of practical, RT nanoelectronic application. A larger number of electronic states may also exist within the well, compared to only 2–3 states observed in shallow Si donor potential wells.⁵ At present, the cryogenic temperature measurements of resonant tunneling and single electron charging effects have been reported for impurities within insulators. In an early work, the measurements of resonant tunneling via sodium (Na) impurities in large area silicon dioxide (SiO₂) gate capacitor structures were reported.²¹ Coulomb charging effects have also been reported, for impurity atoms embedded within double barrier heterostructure resonant tunneling diodes in Group III–V materials.²²

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Fabricating devices to allow single or a few dopant atoms to be controlled requires high resolution lithography, typically electron beam lithography (EBL), scanning probe lithography (SPL), or the state-of-the-art optical lithography techniques used in complementary metal oxide semiconductor (CMOS) transistor nanofabrication.⁵ For fast prototyping of devices or for physics investigations using devices fabricated in the laboratory, EBL and SPL techniques are often more suitable. However, these are both serial writing techniques, and it is recognised that high resolution is accompanied by a significant decrease in throughput.²³ Fortunately, in many research-oriented devices, the high-resolution features are localised in small areas, enabling the device pattern to be split via a mix-and-match lithography approach.²⁴ A diverse range of SPL techniques have been developed, using both STM²⁵ and atomic force microscopy (AFM)²⁶ modes. The probe is used to create secondary effects, which in combination with other processes, lead to the efficient removal or deposition of materials. These can be mechanical, thermal, electrostatic and chemical processes, or hybrid versions of these.^{27–31} In our earlier work, high resolution structures, aligned to optically pre-patterned substrates, were defined using field-emission scanning probe lithography (FE-SPL).³² Such a method can be used to facilitate lithography in ultra-thin (~ 10 nm) resist layers, with pattern transfer into Si/SiO₂/Si substrates via cryogenic etching.³³ Control terminals such as side-gates can then be placed very close to the device channel or QD, leading to an improved gate control of device current.

This paper reports the electrical operation of RT point-contact (PC) QD single-electron transistors (SETs) based on phosphorous dopant atoms embedded within nanoscale SiO₂ tunnel junctions. In contrast to single dopant atom transistors in silicon, where the QD potential well is shallow and device operation limited to cryogenic temperature, here, a deep ($\sim 2\text{--}3$ eV) potential well allows electron confinement at RT. The devices are fabricated in a heavily P doped ($\sim 10^{20}/\text{cm}^3$), *n*-type silicon-on-insulator (SOI) material. A side-gated point-contact geometry is used,³⁴ with a narrow ~ 10 nm scale “neck” defined by scanning probe lithography (SPL). The use of SPL provides the required nanoscale lithographic resolution, and limits damage to the sample, e.g., by substrate charge trapping or damage caused by high-energy electrons, as may occur in more traditional methods such as EBL. Oxidation of the point-contact, combined with pre-defined device geometry, allows complete oxidation of the “neck” region only via a “geometric oxidation” process,³⁴ creating a nanoscale SiO₂ tunnel junction with embedded P impurity atoms, lying between Si source/drain regions. RT ($=290$ K) single-electron charge stability plots show Coulomb diamonds arranged in groups. Each group may be associated with a specific QD. The electrically extracted QD size is ~ 2 nm, similar to the impurity separation, suggesting that P atoms from the heavy doping create the QDs. The experimental characteristics are investigated further by simulation, allowing extraction of energy states, and hence the underlying energy potential. This is found to be anharmonic and is modeled using a Morse oscillator like potential. Our results extend the operation of single-atom transistor operation from cryogenic temperatures to RT, provide the tunneling

spectroscopy of P impurity atoms in SiO₂ insulators, and allow the energy landscape for these impurity atoms to be determined.

II. FABRICATION

The point-contact transistor devices were fabricated using optical and scanning probe lithography on a <100> oriented SOI wafer consisting of a *p*-type ($9\text{--}15\ \Omega\text{ cm}$) substrate, a buried oxide (BOx) layer 25 nm thick, and an ultrathin (12 ± 1 nm) *p*-type device layer ($9\text{--}15\ \Omega\text{ cm}$). The top silicon layer was then doped by phosphorous ion implantation with a dose of $2 \times 10^{15}\ \text{cm}^{-2}$ at 2 keV, giving a maximum *n*-doping of $5\text{--}6 \times 10^{20}\ \text{atoms}/\text{cm}^3$. This top silicon layer was then patterned by optical lithography to give a 4×4 array of device fabrication areas [Fig. 1(a)]. Each area consisted of a central square “mesa” [Fig. 1(b)]. Three different mesa sizes were used (30 μm , 50 μm , and 100 μm sides) [Fig. 1(b)]. Each device mesa connected to 12 surrounding contact pad areas, with registration marks to guide subsequent SPL [Fig. 1(c)]. SPL device patterns were etched into the top silicon down to the BOx layer within the mesa regions [Fig. 1(d)], with the devices linking to the contact pad lines. In our chip layout, the central mesa region between the four devices is not electrically connected and therefore may be “floating” in potential. Any charge on this would shift the electrical characteristics by a constant amount. Furthermore, as the floating region is relatively large, this charge may also be lost to the substrate if any leakage path exists across the BOx layer. For this work, chip sizes of 15×15 mm were used.

High-resolution lithography was undertaken using field emission (FE)-SPL. In this technique, low energy electrons (20–100 eV) are emitted by field emission from an ultra-sharp tip (typical radius 4–10 nm) on a scanning probe,^{35–38} with a bias voltage applied between sample and tip. An enhancement of the electric field at the tip enables the emitted electrons to follow a Fowler-Nordheim dependency.³⁹ The use of low electron energy and intensity avoids problems such as defect generation or charge trapping that can occur with high-energy beams. An active (self-sensing and self-actuated) cantilever was used for FE-SPL,^{40,41} enabling atomic force microscopy (AFM) to be employed for both alignment and inspection.^{42,43} The FE-SPL was undertaken using a thermomechanically actuated, piezoresistive cantilever technology.⁴⁴ A rigid cross-beam support could facilitate an average movement error of 80 nm for a series of 100 μm steps across 100 mm, with a resolution of 10 nm. Using this equipment, by a variation of exposure doses, it was possible to obtain line widths from 5 to 100 nm, gratings with half pitch values of 7 nm, and dots with sizes < 10 nm.^{2,42–44} A resist layer of calixarene was used, with a thickness of 12–17 nm. Line exposures were made using the calixarene in a positive self-development mode, which facilitated the direct removal of line widths from 200 nm for large separation lines, down to 10 nm when defining the inner core of the QD device in high resolution. Prior to exposure of the device structure, calibration of the requisite calixarene dose level was undertaken, to ensure that the optimum exposure conditions were used.

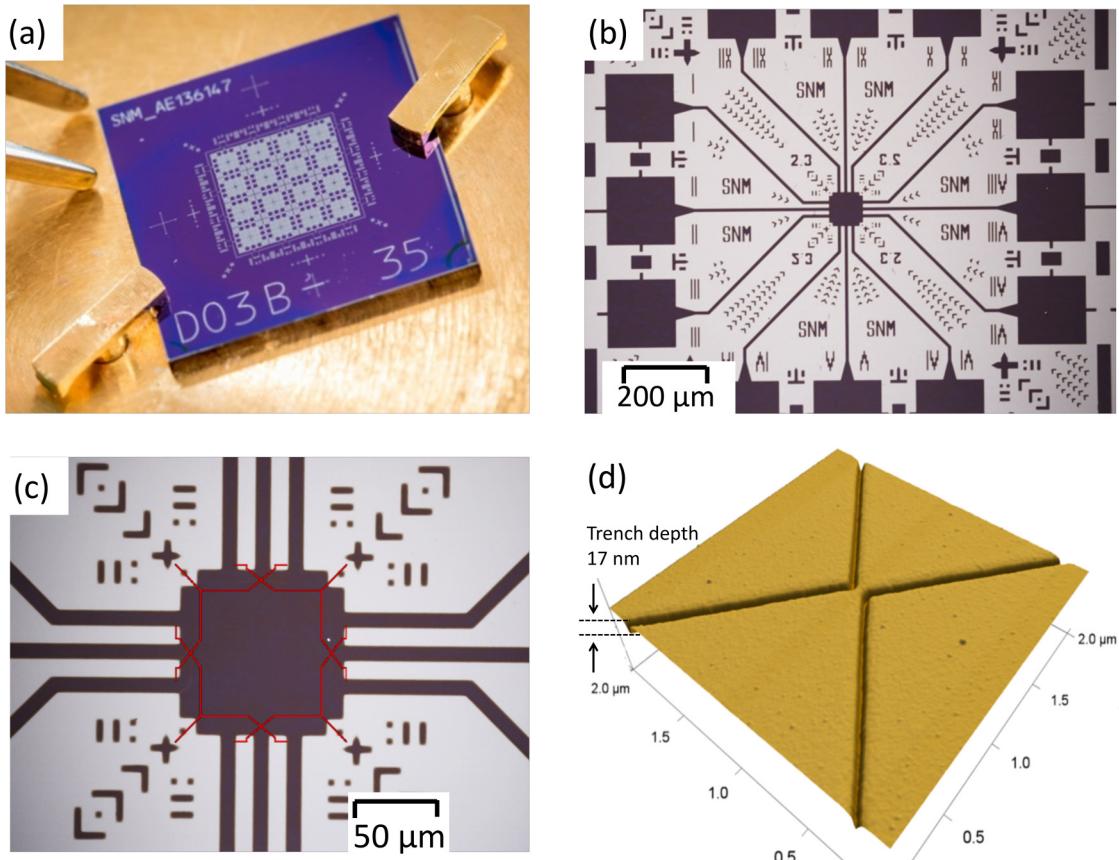


FIG. 1. (a) Overall view of a 15×15 mm chip used for device fabrication. A 4×4 array of square device fabrication regions was defined by optical lithography in the top Si, by etching into the BOx layer. (b) Optical micrograph of a single device fabrication area, with a central mesa region for subsequent SPL, surrounded by interconnects leading to 12 contact pad regions. (c) Higher resolution optical micrograph with overlaid FE-SPL exposure patterns for four devices. (d) AFM image of a point-contact QD device before oxidation, where the etched lines are defined by FE-SPL and cryogenic RIE. Here, the source and drain regions lead from bottom-left to top-right, and the side-gates lead from top-left to bottom-right. The etch depth obtained from an AFM line scan is 17 nm.

High resolution atomic force microscopy images of the silicon neck of three point-contact QD transistors, prior to oxidation are shown in Figs. 2(a)–2(c). These show devices with nominal neck widths ~ 50 nm, ~ 35 nm, and ~ 20 nm, respectively. Images include the effect of tip convolution of the AFM tip of radius ~ 10 nm. This implies that the actual neck widths are less, ~ 30 nm, ~ 15 nm, and <10 nm, respectively. Figures 2(d)–2(f) show the AFM scans from a second set of comparable devices, with associated line scans across the two gates (top to bottom) and point-contact regions of the device. The nominal widths of the devices are indicated, as measured between the blue dots in each line scan. Device pattern transfer into the silicon, to replicate the nanoscale features lithographically generated in ultra-thin (10–20 nm) resist, was achieved using anisotropic cryogenic reactive ion etching (RIE) based on SF_6/O_2 chemistry.³³ With this technique, the thin resists used for the high-resolution FE-SPL can be effective as barriers for the etching. The increased sticking probabilities at low temperatures (i.e., below 170 K) facilitate the formation of a passivation layer by the reactants (SiO_xF_y). This is constantly removed by the sputtering that occurs from the energetic ions impacting mainly perpendicular to the bottom surface, thus resulting in an anisotropic etching of the silicon.⁴⁵ Etching was undertaken using an Oxford Instruments ICP PlasmaPro 100 Cobra tool with a

3 kW/2 MHz ICP source and a 300 W/13.56 MHz platen r.f. power generator. Gas flows of 10 sccm and 2 sccm were used for the SF_6 and O_2 , respectively. The system uses liquid nitrogen as coolant and helium “backside” cooling for thermal contact between the sample and the temperature-controlled sample holder. The sample was cooled to 150 K with the process undertaken at a pressure of 5 mTorr. Using this technique, precise pattern transfer of sub-20 nm patterns with high aspect ratios has been shown, with etch depths of 80 nm.⁴⁶ A small undercut occurs during etching, leading to a reduction in point-contact height for the narrowest neck widths [Figs. 2(c) and 2(f)]. This reduces the volume of the point-contact region even further, helping to isolate only a few dopants within this region.

Thermal oxidation at 900 °C for 15 min was used to grow a SiO_2 layer of ~ 15 nm on the Si surfaces of the device. As the point-contact “neck” defined by FE-SPL was only ~ 10 nm in width and, for the narrowest necks [Fig. 2(f)], <10 nm in height, this process completely oxidised the neck, forming the device “core,” a nanoscale SiO_2 tunnel junction with embedded P dopant atoms.³⁴ The included angle defined at the tips of both of the triangular source/drain regions of the point-contact (Fig. 2) was $\sim 90^\circ$, larger than in our previous work on EBL defined point-contacts.³⁴ The larger included angle led to sharply closing

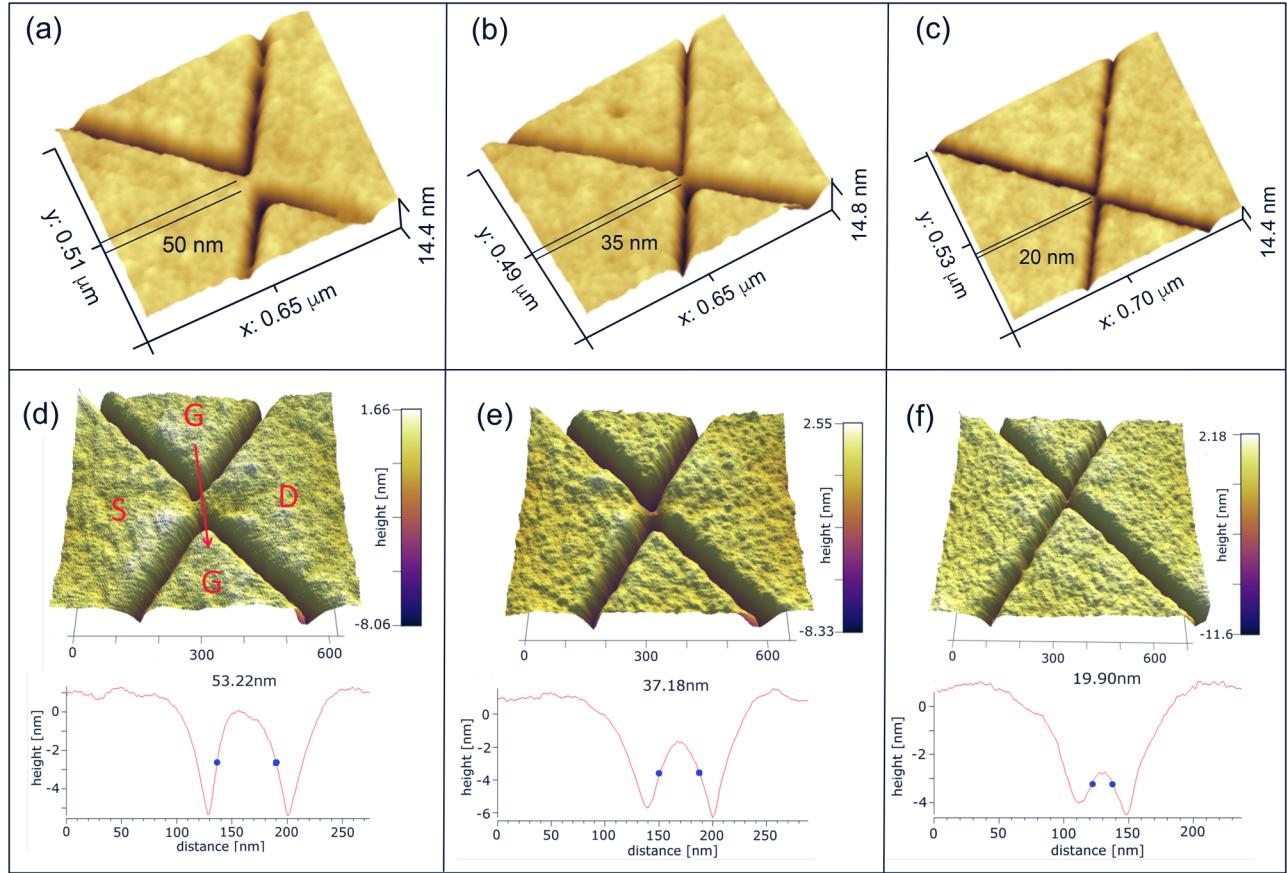


FIG. 2. [(a)–(c)] High resolution, pre-oxidation AFM micrographs of three point-contact QD transistors, with neck regions ~ 50 nm, ~ 35 nm, and ~ 20 nm in width, respectively. Images include the effect of convolution of the ~ 10 nm radius AFM tip. [(d)–(f)] AFM scans from a second set of comparable devices, with associated line scans across the two gates (top to bottom) and point-contact regions of the device. The nominal widths of the devices are indicated, as measured between the blue dots in each line scan.

device “walls” and hence a narrower SiO_2 neck region. The tunnel barrier width was then reduced while retaining good conductivity at the tips of the triangular source/drain regions. Contact windows remote to the device core were opened using a specific mask pattern, and a “burst” dip in 49% hydrofluoric acid (HF) was applied to ensure a clean surface for ohmic contacts. These were formed using an optical lift-off, with a deposition of ~ 20 nm thickness of Cr followed by ~ 200 nm of Al.

III. ELECTRICAL CHARACTERISATION AND SIMULATION

Figures 3(a) and 3(b) show the room temperature (RT = 290 K) log drain-source current (I_{ds}) vs. drain-source (V_{ds}) and gate-source (V_{gs}) voltage of point-contact (PC) transistors (Devices “A” and “B,” estimated to be ~ 10 nm \times ~ 7 nm in cross-section). The biasing for the device is shown schematically in Fig. 3(c). Here, discrete electronic states $E_0 - E_n$ are tunnel coupled to the source and drain electrodes and capacitively coupled to the gate electrode, via lumped “effective” capacitances C_1 , C_2 , and C_g , which model the capacitive environment. In Fig. 3(a), for low values of $|V_{ds}|$, a series of diamond-shaped low current (<10 pA) regions are observed. These features, resembling Coulomb diamonds,^{47–49} change in size along both V_{ds} and V_{gs} axes, forming patterns

as V_{gs} varies. We now group the diamonds (groups a_1-a_7 , b_1-b_5 , and c_1-c_4), based on successively decreasing or increasing diamond sizes. Here, in group b , the diamond sizes increase and then decrease as V_{gs} increases. In group a , the diamonds show a decrease in size from a_3-a_7 for negative values of V_{ds} ; however, smearing of the diamonds into each other, particularly for positive V_{ds} , leads to less clear behavior for diamonds a_1-a_4 . For group c , the size increases for diamonds c_1-c_3 . The presence of groups of diamonds with similar trends implies that the underlying electronic states are not completely random in energy. Qualitatively similar behavior is seen in other devices [Dev. B, Fig. 3(b)]. Figure 3(d) shows the selected traces of I_{ds} vs. V_{gs} , at constant values of V_{ds} , extracted from the data of Fig. 3(a). I_{ds} oscillates strongly with V_{gs} , and a sub-threshold current region is observed for $V_{gs} < -1.5$ V and low V_{ds} magnitude. The current oscillations vary strongly in peak height for $V_{gs} > -1.5$ V, following the rise and fall of the diamond region sizes in Fig. 3(a). Finally, Fig. 3(e) shows the selected traces of I_{ds} vs. V_{ds} , at constant values of V_{gs} . The slope of the traces in the low $|V_{ds}|$ region is modulated periodically with V_{gs} , corresponding to the current oscillations in Fig. 3(d). Results are shown only for RT, as the diamond shapes in the characteristics change with reducing temperature, due to the increasing influence at lower temperatures of additional potential barriers along the current path, reported in detail in

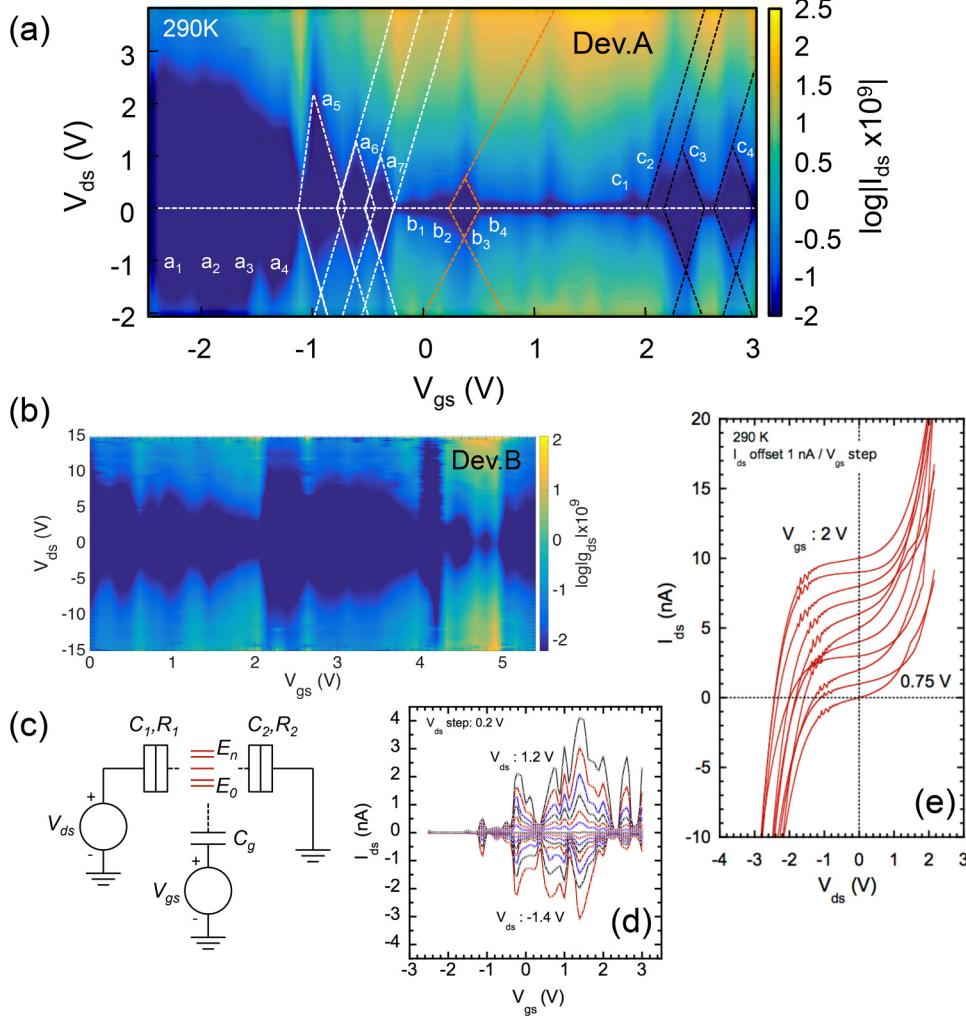


FIG. 3. (a) Room temperature (RT = 290 K) electrical characteristics of a point-contact QD transistor. Log drain-source current (I_{ds}) vs. drain source (V_{ds}) and gate (V_{gs}) voltage for a point-contact transistor, Device “A.” (b) Log (I_{ds}) vs. (V_{ds}) and (V_{gs}) characteristics of a second transistor, Device “B.” (c) Schematic circuit diagram for the transistor, showing the discrete energy states E_n on the QD, separated by energy gaps ΔE_n . (d) Selected traces of I_{ds} vs. V_{gs} , at specific and constant values of V_{ds} from -1.4 V to $+1.2$ V, extracted from the data of Fig. 3(a). Strong RT oscillations occur in I_{ds} with V_{gs} . (e) Selected traces of I_{ds} vs. V_{ds} , at specific and constant values of V_{gs} from 0.75 V to 2 V.

our previous work.³⁴ A similar effect, with series potential barriers along the current path, leads to the high threshold value of V_{ds} for current flow in Dev. B even at RT [Fig. 3(b)], while in Dev. A [Fig. 3(a)], the effect of any series potential barriers at RT is minimised for $V_{gs} > -1.5$ V.

The existence of diamond-like regions in the characteristics of Fig. 3(a) typically implies the presence of discrete energy states E_n near the Fermi energy, separated by energy gaps ΔE_n [Fig. 3(c)]. As V_{gs} is varied, these states are swept past the source Fermi energy E_{FS} due to electrostatic coupling to the gate across the gate capacitor C_g , and resonant tunneling of electrons occurs across the states. A current peak occurs when a given state is in resonance with E_{FS} , and a valley occurs when E_{FS} lies in-between a pair of states. As varying V_{ds} can also change the states in energy, due to coupling across the tunnel junctions with capacitance (resistance) C_1 (R_1) and C_2 (R_2) [Fig. 3(c)], this leads to diamond-like regions in a plot of I_{ds} vs. V_{ds} , V_{gs} , with each diamond associated with a pair of states (E_n , E_{n+1}). Typically, the presence of diamond-like features is associated with the “Coulomb diamonds”^{47–49} in the physically defined “island” of a single-electron transistor (SET) or quantum dot (QD). Here the energy gap $\Delta E_n = E_{n+1} - E_n$ between a pair of states is created by a combination of the quantum confinement energy (E_{kn}) and single-electron charging energy ($E_{cn} = e^2/C_t$, where $C_t =$

$C_1 + C_2 + C_g$ is the total capacitance of the state) for each state, $\Delta E_n = E_{kn,n+1} - E_{kn} + E_{cn}$.⁴⁹ However, more generally, any distribution of discrete energy states separated by energy gaps, where the states are coupled to, and can be shifted in energy by drain and gate voltages in a transistor configuration, will lead to diamond-like features in the electrical characteristics. Within a crystal, these states may be confined by potentials defining island regions with different material morphology, by impurity atoms, or by a distribution of defect states; however, these states must not be pinned in energy if diamond-like features are to be observed.

The capacitive network surrounding the states determines leverage of the bias voltages on the energy of the states, and hence the width and height of the diamonds in the electrical characteristics. Assuming similar tunnel barriers, $C_1 = C_2 = C$, where $V_{ds}/2$ drops across each barrier, a realistic assumption when a strong Coulomb staircase is not observed, and ignoring any additional series voltage drops in the contact regions, the maximum diamond height along the V_{ds} axis is $\Delta V_{ds} = \Delta E_n/e$. Here, ΔE_n is the separation in energy of the corresponding pair of states n and $n+1$. Similarly, the maximum diamond width along the V_{gs} axis is $\Delta V_{gs} = [(2C + C_g)/C_g]\Delta E_n/e$. This leads to values of $\Delta V_{ds} < \Delta V_{gs}$. For the case $C_g \ll C$, $\Delta V_{gs} = (2C/C_g)\Delta V_{ds}$, which is often the case in SETs and QD transistors where the gate is placed at a distance from the QD. If

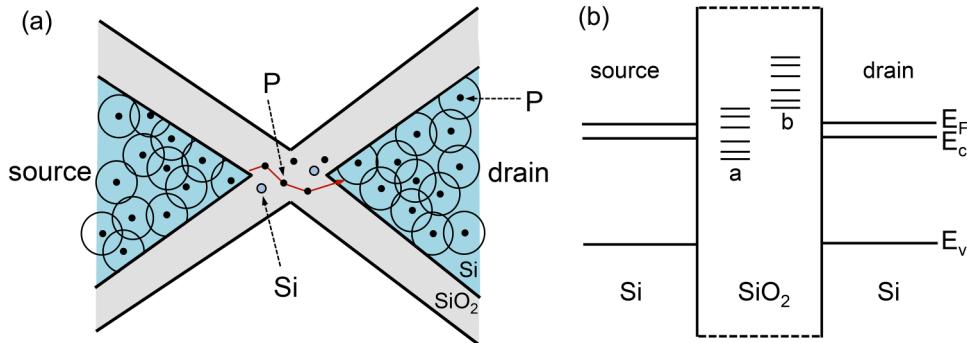


FIG. 4. (a) Schematic diagram of the point contact QD transistor. Thermal oxidation of the device (grey area) leads to complete oxidation only of the point-contact neck. This forms a ~ 10 nm scale SiO_2 tunnel junction at the neck, sandwiched by triangular Si regions (shaded blue). The P dopant atoms are shown as black dots. In the Si regions, the P atoms act as donors, with overlapping Bohr electron orbits (black circles), such that these regions conduct at RT. The P atoms in the SiO_2 neck are isolated and can form QDs. Electron transport can occur via tunneling along a path (red line) through the isolated dopant states. The average separation between the P donor atoms is ~ 2 nm. (b) Schematic representation of the energy diagram across the point-contact region. The source and drain Si regions are degenerately doped, with E_F above E_c . P atoms in the SiO_2 neck can form QDs. Energy states for two QDs, "a" and "b," are shown schematically.

$C_g > C$, ΔV_{ds} can approach but not exceed ΔV_{gs} in value, and observation of the case $\Delta V_{ds} > \Delta V_{gs}$ implies that a substantial portion of V_{ds} drops external to the QD, e.g., in contact resistances or other, series QDs. In the data of Dev. A [Fig. 3(a)], $\Delta V_{ds} \sim \Delta V_{gs}$ (group "b") or $\Delta V_{ds} > \Delta V_{gs}$ (group "a"). This suggests that in Dev. A, C_g may be relatively large and that additional, significant series potential drops exist. This picture is supported by the data for $V_{gs} < -1.5$ V, where additionally, the widths of the diamonds a_1-a_4 along the V_{ds} axis do not reduce to zero, implying that additional potential barriers/voltage drops exist along the conduction path. However, these additional potential barriers can be modulated by V_{gs} , as seen by the increase in current above a threshold voltage for current oscillations, at $V_{gs} \sim -1.5$ V. For $V_{gs} > -1.5$ V, the effect of any additional potential barrier is minimised. Finally, for Dev. B [Fig. 3(b)], for most of the diamond-like features, $\Delta V_{ds} \gg \Delta V_{gs}$ and the diamond width along V_{ds} cannot be reduced to zero, implying a stronger effect from additional potential barriers in this device.

Figure 4 shows a schematic diagram of the PC point contact transistor. Thermal oxidation of the device [grey area, Fig. 4(a)] leads to complete oxidation only of the PC neck, leading to a ~ 10 nm scale SiO_2 neck, sandwiched by triangular Si regions [blue areas, Fig. 4(a)]. As the Si is heavily doped n -type with P ($> 10^{20}/\text{cm}^3$), well above the metal/insulator threshold, the un-oxidised Si regions are conductive and form a Fermi sea at RT. Here, the P atoms are shown as black dots, and the majority of the donor electron Bohr orbits (black circles) overlap. The average separation between the P donor atoms in these regions is ~ 2 nm, and the effect of spatial disorder in the donor locations is likely to be significant only at the tip of each triangular Si region. In contrast, the SiO_2 PC neck forms a potential barrier region with the P doping atoms acting only as embedded impurity atoms (~ 15 P atoms/ $5 \times 5 \times 5$ nm^3 region), which may form sites through some of which electron tunneling can occur [Fig. 3(b)]. Further sources for tunneling sites are any Si rich regions within the SiO_2 , forming Si nanocrystals (blue circles in neck region) embedded within the SiO_2 ,⁵⁰ and these may or may not contain P atoms.

Phosphorous atoms embedded in SiO_2 do not behave as shallow electron donors, as in Si . Given the wide band gap in SiO_2 (~ 9.7 eV), depending on whether a P impurity atom is bonded to a Si or O atom, or lies interstitially (possible, given segregation in a heavily doped material), various energy states are possible.^{51,52} If the P atom bonds to a Si atom, it may act as a large ionization energy (~ 0.7 eV) electron donor into the SiO_2 conduction band, ~ 4 eV above the conduction band/Fermi energy E_F in the Si regions. In contrast, if the P atom bonds to an O atom, it creates a near mid-gap state at an energy ~ 3.7 eV above the valence band in the SiO_2 . For interstitial P atoms, states are likely to lie near mid-gap. Electron transport across the SiO_2 neck can occur via tunneling along a path through these states [Fig. 4(a)], if they lie in an energy range close to E_F [Fig. 4(b)]. During the tunneling process, it may also be possible to charge these states. An energy gap $E_g > k_B T = 25.6$ meV between a pair of states ($T = 290$ K) would lead to observation of a diamond-like region in the electrical characteristics. Here, the outer shell configuration for neutral P ($3s^2 3p^3$)⁵³ implies that up to 3 extra electrons can be added to the $3p$ states or up to 5 electrons removed from the normally filled states. Bonding of the P atom to Si , O or a further P atom changes the occupancy of the states.

The electrical characteristics of Fig. 3(a) are now simulated within a QD framework, using a single-electron tunneling simulator, "CAMSET."^{54,55} Here, the master equation for tunneling across a QD is solved,^{47,48} given effective capacitances C_1 , C_2 , C_g surrounding the QD [Fig. 3(c)], and the density of states (DOS) on the QD. The capacitive network determines the value of charging energy E_{cn} and the bias voltage leverage on the energy states, and the DOS corresponds to the confinement energy E_{kn} . The approach used is to fit the widths of the diamonds in various groups in Fig. 3(a) along V_{gs} only, by adjusting the values of the parameters C_1 , C_2 , C_g and E_{kn} . As additional voltage drops can occur along the tunneling path in series with the QD, we do not fit the height of the diamonds along V_{ds} . Furthermore, while the simulation extracts values for ΔE_n , as we do not know the exact size of the QD, it is difficult to calculate

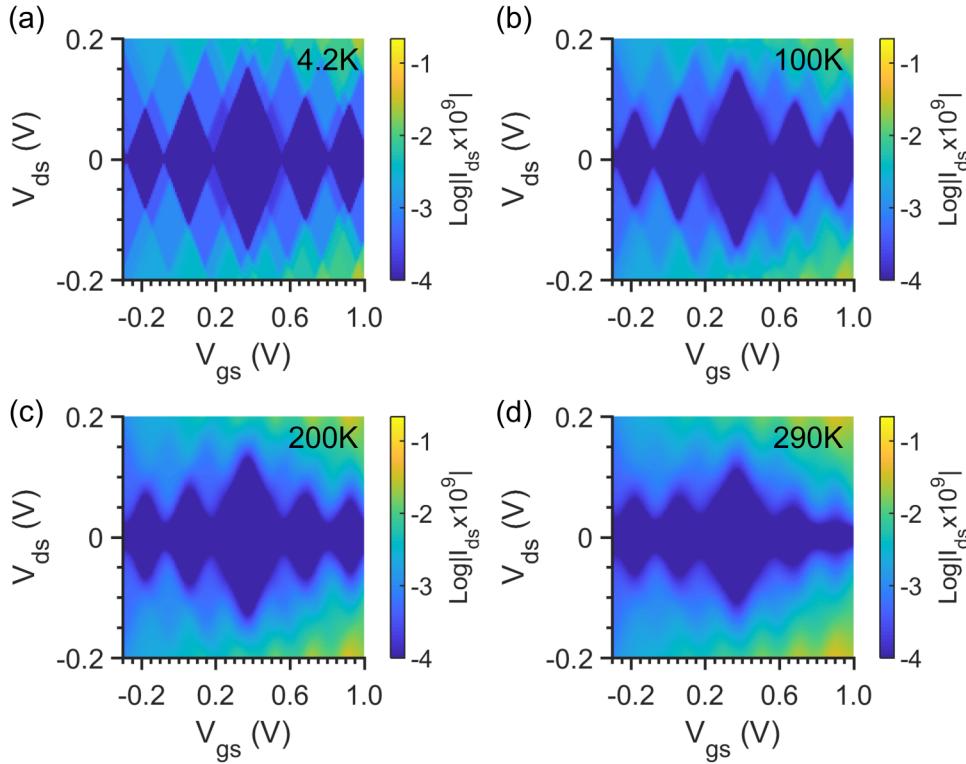


FIG. 5. Simulation of the electrical characteristics of Fig. 3(a), using a single-electron tunneling simulator, “CAMSET.” The master equation for tunnelling across a QD is solved, given effective capacitances C_1 , C_2 , C_g surrounding the QD [Fig. 3(c)], and the density of states (DOS) on the QD. The widths of the diamonds in various groups in Fig. 3(a) are obtained by adjusting the values of the parameters C_1 , C_2 , C_g , and E_{kn} . The simulation shows $\log I_{ds}$ (color scale) vs. V_{ds} , V_{gs} for the five diamonds of group “b” in Fig. 3(a). Results are shown for temperature (a) 4.2 K, (b) 100 K, (c) 200 K, and (d) 290 K (RT). The simulation results for the lower temperatures are presented to allow sharp diamond edges to be resolved, as thermally-assisted tunneling reduces.

precisely the relative influence of E_{cn} and E_{kn} within a given energy gap ΔE_n .

Figure 5 shows the simulation results for the five diamonds of group “b” [Fig. 3(a)], at various temperatures from RT = 290 K to 4.2 K. Here, simulation results for the lower temperatures are presented to better resolve the diamonds due to reduced thermal smearing. Similarly, Fig. 6 shows

simulation results for the diamonds of group “a.” In the case of group “b” (Fig. 5), the diamonds are seen to increase and then decrease in width/height as V_{gs} increases, similar to the experimental data of Fig. 3(a). Adjusting the energy spacing between states ΔE_n by increasing and then reducing this allows simulation of this effect. Finally, in the case of group “a” diamonds (Fig. 6), the trend is of mainly decreasing

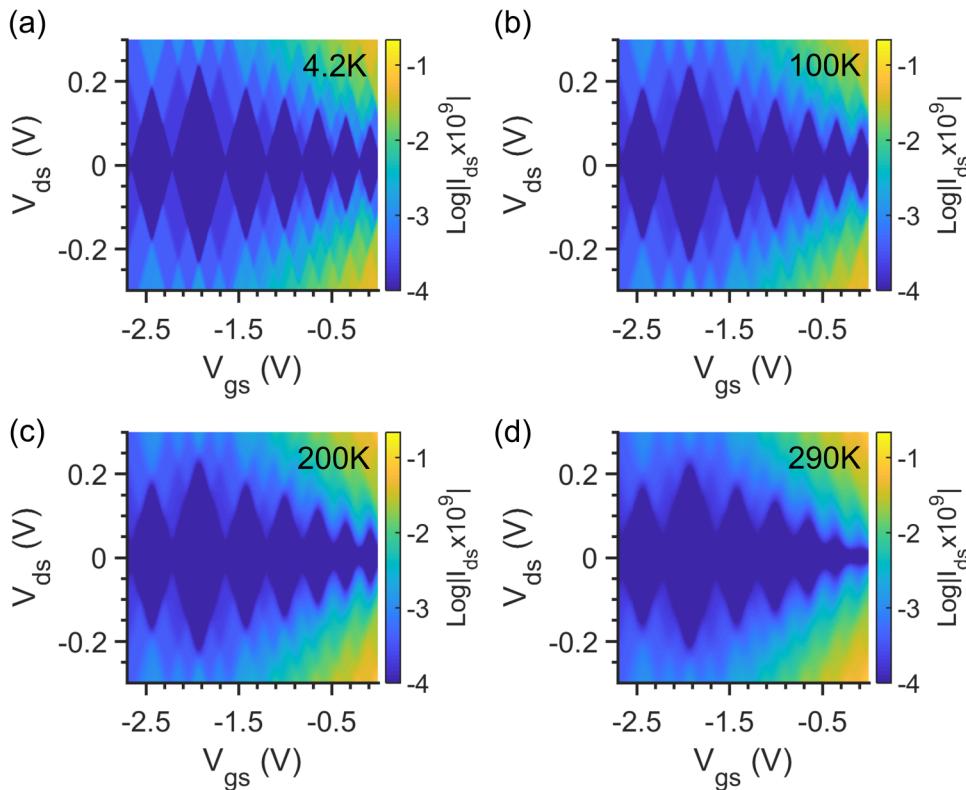


FIG. 6. CAMSET simulation for $\log I_{ds}$ (color scale) vs. V_{ds} , V_{gs} for the diamonds shown in group “a” in Fig. 3(a). Results are shown for temperatures (a) 4.2 K, (b) 100 K, (c) 200 K, and (d) 290 K (RT). For the simulations of both Figs. 5 and 6, the increase and subsequent decrease in width/height of the diamonds with increasing V_{gs} , seen in the experimental data of Fig. 3(a), is modeled by increasing/reducing the energy spacing ΔE_n between states in the simulation.

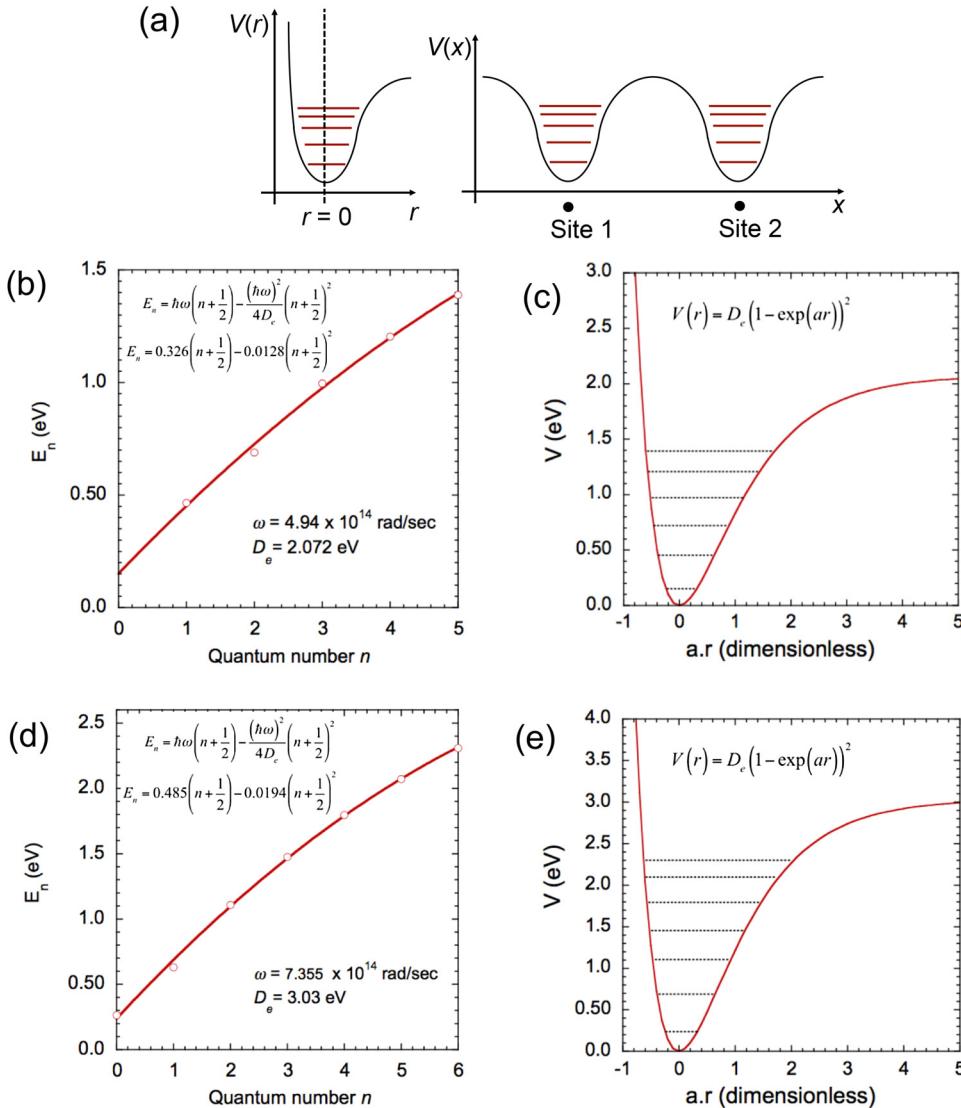


FIG. 7. (a) Schematic representation of two possible anharmonic potential wells. The left figure shows an asymmetric Morse-like energy potential, with a hard wall for $r < 0$ and an anharmonic part for $r \gg 0$. The right figure shows two symmetric, inverted “bell-like” potentials centred at dopant sites 1 and 2. A harmonic part exists for each well near the centre of the well, and anharmonic parts away from the centre. (b) Plot of energy states E_n (open circles) vs. quantum number n for the diamonds in group “b” [Fig. 3(a)], using the simulation results shown in Fig. 5. E_n is fitted (red line) using the energy states for an anharmonic Morse-like energy potential (equation for E_n given in figure). The well-depth energy parameter $D_e = 2.07$ eV and angular frequency $\omega = 4.94 \times 10^{14}$ rad/s. (c) Potential well $V(r)$ for the energy states of (b), using the anharmonic Morse-like energy potential (equation for $V(r)$ given in figure). (d) is a repeat of (b), but for the diamonds of group “a.” Here, $D_e = 3.03$ eV, implying a deeper well, and $\omega = 7.355 \times 10^{14}$ rad/s, implying a narrower well. (e) is a repeat of (c), but for the energy states of (d).

diamond size, with an increase only from the first diamond (centred at $V_{gs} \sim -2.5$ V) to the second diamond (centred at $V_{gs} \sim -2$ V). Furthermore, the increasing value of $|V_{ds}|$ needed for current flow, below threshold gate voltage $V_{gs} < -1.5$ V in the experimental data [Fig. 3(a)], is not simulated. While this prevents the diamond regions from reducing periodically to zero height along V_{ds} in the experimental data, this does not occur in the simulation, which extracts only the QD like behavior. The tendency of the device to turn off at negative voltages is caused by field effect transistor like behavior in our n -type device, where negative voltage creates a series potential barrier reducing current flow.

IV. DISCUSSION

The simulation results (Figs. 5 and 6) allow extraction of ΔE_n and hence the corresponding energy states E_n for the diamonds in group “a” and “b.” Figures 7(b) and 7(d) show the plots of E_n vs. quantum number n for group “b” and “a” diamonds, respectively, where ΔE_n increases and then reduces as n increases. It is possible to use the extracted values of ΔE_n to estimate the order of magnitude of the size of the potential well holding the states. A simple approximation is

used assuming a spherical QD, where $\Delta E_n = E_c + \Delta E_k$, where $E_c = e^2/C_t = e^2/(4\pi\epsilon\epsilon_0 r)$ and $E_k \sim \pi^2\hbar^2/2mr^2$.³⁴ For the diamond b_3 [Fig. 3(a)], solving the quadratic equation in r for the extracted value of $\Delta E_n = 0.31$ eV gives $r \sim 1.8$ nm, $E_c \sim 0.2$ eV, and $E_k \sim 0.11$ eV. Here, E_c and E_k are $\gg k_B T = 25$ meV at 290 K, supporting the observation of RT operation. Regarding the value $r \sim 1.8$ nm, while this is well above the interatomic spacing in Si/SiO₂, it is of similar scale to the average P donor separation ~ 2 nm and corresponds to a QD diameter ~ 3.6 nm, close to twice the donor separation. This suggests that the origin of the potential wells holding the states is likely to be associated with a more spatially isolated P donor or a cluster of P donor impurities.

We now consider the shape of the effective potential well underlying the behavior of the Coulomb diamonds observed in our data. For simplicity, we assume that the potential well shape is comparatively “hard,” i.e., perturbation of the potential as electrons are added to the well can be neglected, and we do not perform a self-consistent calculation of the potential.⁵⁶ This assumption may be reasonable as in our case, the walls of the potential well are likely to be defined by the SiO₂ environment holding an embedded P impurity atom, or a cluster of P or Si atoms, which forms the

site for E_n . For a quasi-hard potential well shape, the increasing/reducing trend in ΔE_n cannot be explained by a square well (ΔE_n would increase), a harmonic potential (constant ΔE_n), or a purely atomic $1/r$ potential (ΔE_n would reduce). However, a mixed potential, where at low energy, a steep walled or quasi-rectangular well exists, and at higher energy the well opens out, in a manner similar to a $1/r$ potential, can result in initially increasing and then decreasing diamond sizes. Anharmonic asymmetric, or inverted “bell-like,” effective potentials [Fig. 7(a)] can lead to the trends observed in ΔE_n . Here, an increase in ΔE_n is caused by an increase in $\Delta E_{kn} = E_{k,n+1} - E_{kn}$ deep in the well, and a decrease in ΔE_n as both ΔE_{kn} and E_{cn} decrease as the potential well diameter increases towards the top of the well. We approximate this situation using a simple model based on an asymmetric Morse-like energy potential⁵⁷ [left figure, Fig. 7(a)], where a hard wall exists for $r < 0$ and an anharmonic part for $r \gg 0$. The right figure shows two symmetric, inverted “bell-like” potentials centred at dopant sites 1 and 2. A harmonic part exists for each well near the centre of the well and anharmonic parts away from this. We now use the Morse-like energy potential,⁵⁷ $V(r) = D_e(1 - \exp(ar))^2$, to model our data. Here, the energy parameter D_e determines the depth of the well, and the inverse length a determines the width. Typically, the Morse potential is used to model vibrational states in diatomic molecules;⁵⁷ however, this also provides a convenient means to incorporate anharmonicity. The potential has the advantage of straightforward expressions for the

energy states, $E_n = \hbar\omega\left(n + \frac{1}{2}\right) - \frac{(\hbar\omega)^2}{4D_e}\left(n + \frac{1}{2}\right)^2$, allowing extraction of D_e and angular frequency ω . Here, the energy separation between the bottom of the well and the ground state (E_0) can be smaller than that between the first excited state and the ground state ($E_1 - E_0$) if $\frac{(\hbar\omega)^2}{4D_e} \ll \hbar\omega$. As n increases, the second term in the expression for E_n becomes more significant, leading to a reduction in the energy state separations. Furthermore, given the possibility of more than one potential well contributing to the electrical characteristics [e.g., as shown in Fig. 4(b)], variation in the location in energy of the bottom of the potential well, and hence of the associated ladder of states [e.g., as shown in Fig. 4(b)], can result in both increasing and decreasing sets of diamonds. Here, a set of diamonds of reducing size as V_{gs} increases, associated with states lying higher up in a potential well, may then transition to a set of diamonds of increasing size, associated with the lowest two states in a Morse potential, or with a steeper and non-Morse like potential deep in the well. Figures 7(b) and 7(d) show fits (red lines) to the extracted values of E_n , which give, for group “b” (group “a”), $D_e = 2.07$ eV (3.03 eV) and $\omega = 4.94 \times 10^{14}$ rad/s (7.355×10^{14} rad/s). The corresponding equations for the energy states in group “b” and “a” are $E_n = 0.326\left(n + \frac{1}{2}\right) - 0.0128\left(n + \frac{1}{2}\right)^2$ and $E_n = 0.485\left(n + \frac{1}{2}\right) - 0.0194\left(n + \frac{1}{2}\right)^2$, respectively.

Figures 7(c) and 7(e) show the plots of our effective potential $V(r)$ vs. ar for these values of D_e . It is seen that the well for

group “a” is deeper than that for group “b,” consistent with the clearer diamonds, with lower thermal smearing, observed for group “a” [Fig. 3(a)].

The origin of anharmonic effective potentials of the types shown in Fig. 7(a) is now considered. The possibility that the potential is localised on a site consisting of a P impurity atom, or on a Si cluster/nanocrystal, embedded within SiO_2 , is considered first. Here, the potential sides are likely to be “quasi-hard,” as exists for the $r < 0$ part in a Morse-like potential [Fig. 7(a) left]. However, interaction of this P atom/Si cluster with other nearby P atoms/Si clusters may lower the intermediate potential to create the anharmonic part, $r \gg 0$. The potential itself may be created either by a charged impurity or by the charge configuration of the environment. For the case where the potential site lies within a 1-D chain of P atoms/Si clusters, anharmonic parts may exist away from the centre of each well [Fig. 7(a) right], creating softer “saddle” potentials intermediate to the sites along the chain. However, if the ends of the chain terminate within the SiO_2 region, the final potential will be Morse-like. Anharmonicity can also arise from the effect of the high electric fields within the point-contact with applied drain- and gate-source voltages, and the interaction of these with the electric field pre-existing in the SiO_2 region due to its charge configuration. Finally, we consider further the situation where the potential is centred on a P atom or a cluster associated with P atoms. While the presence of Si rich clusters in the SiO_2 cannot be eliminated in our devices, a potential well associated with interacting P doping atoms embedded in the SiO_2 is more likely. This view is supported by (i) the very high doping level ($>10^{20}/\text{cm}^3$), implying that ~ 10 or more P impurities are present in the SiO_2 tunnel barrier, (ii) the estimate of the QD size, which corresponds well to the average separation between P impurity atoms, (iii) the existence of 8 electron states (partially filled) for the outer most shell of each P atom, some of which can then participate in the tunneling/charging process, and (iv) results from our previous work, where statistics on the observation of RT Coulomb diamonds in similar devices could be associated with material morphology and not the device geometry.³⁴ Argument (iii), the 8 electrons available for the P atom outer shell, may also be contrasted to the alternative possibility of defect states in SiO_2 as the origin of our data. These can either be empty or occupied by one electron. A series of states, grouped with the correct increasing/reducing value of energy separation, would then be necessary to explain the multiple diamonds seen in our data, less likely given the random nature of defect states.

Finally, we comment on the possibility that a portion of the Si point-contact region remains unoxidised. For example, the device structure in Fig. 2(f) has the unoxidised point-contact height reduced by ~ 3 nm due to an undercut of this area during isolation trench etching. The height of the remaining Si region is ~ 9 nm, and a subsequent oxidation to grow a ~ 15 nm SiO_2 layer may still leave an ultra-thin Si layer a few nanometre thick unoxidised. If this layer is continuous and incorporates P dopant atoms, then it would form a parallel, resistive conduction path and prevent observation of QDs within the SiO_2 region, with the device behaving as

a resistor. In contrast, if this layer is discontinuous, such a layer has been shown to form isolated Si nanocrystal QDs.⁵⁸ These QDs, particularly if they incorporate P dopants and are small enough, can then also contribute to the RT Coulomb diamond characteristics.

V. SUMMARY

This paper discussed the electrical operation of RT point-contact QD transistors where the QDs were associated with phosphorous dopant atoms embedded within nanoscale SiO₂ tunnel junctions. In contrast to single dopant atom transistors in silicon, where the QD potential well is shallow and device operation limited to cryogenic temperature, here, a deep (~2–3 eV) potential well allows electron confinement at RT. The devices were fabricated using FE-SPL on a heavily P doped (~10²⁰/cm³), *n*-type silicon-on-insulator (SOI) material. The devices used a ~10 nm scale SiO₂ point-contact lying between larger source and drain regions, with two side gates to control the point-contact tunnel current. The use of SPL provided the required nanoscale lithographic resolution while limiting the damage to the sample, as may occur in more traditional methods such as EBL. The potential associated with P impurity atoms, embedded within the SiO₂, defined ultra-small, few nanometre scale QDs. RT single-electron charge stability plots showed Coulomb diamonds arranged in groups, with each group associated with a specific QD. The electrically extracted QD size was ~2 nm, similar to the impurity separation. This suggested that segregated P atoms or clusters from the heavy doping created the QDs. The experimental characteristics were investigated further by simulation, allowing extraction of energy states, and hence the underlying energy potential. This was found to be anharmonic and could be modeled using a Morse oscillator-like potential. Our results demonstrate that it is possible to extend single-atom transistor operation to RT and that tunneling spectroscopy may be used to measure the electronic energy states and potential well shape associated with single or small numbers of impurity atoms, isolated within a nanoscale insulator.

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