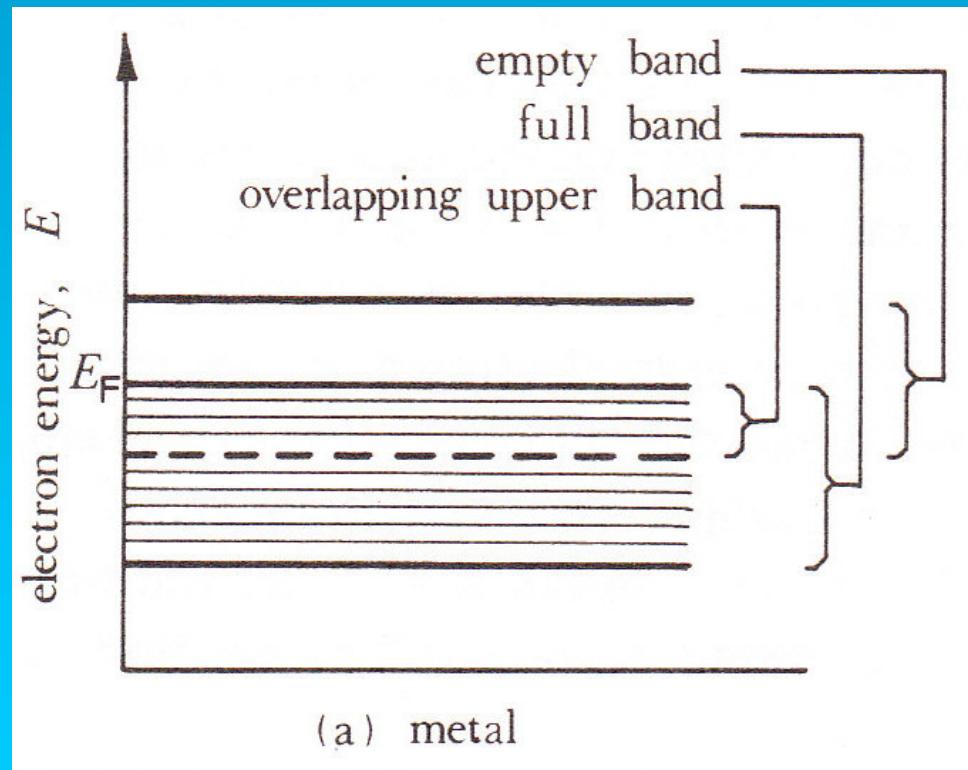
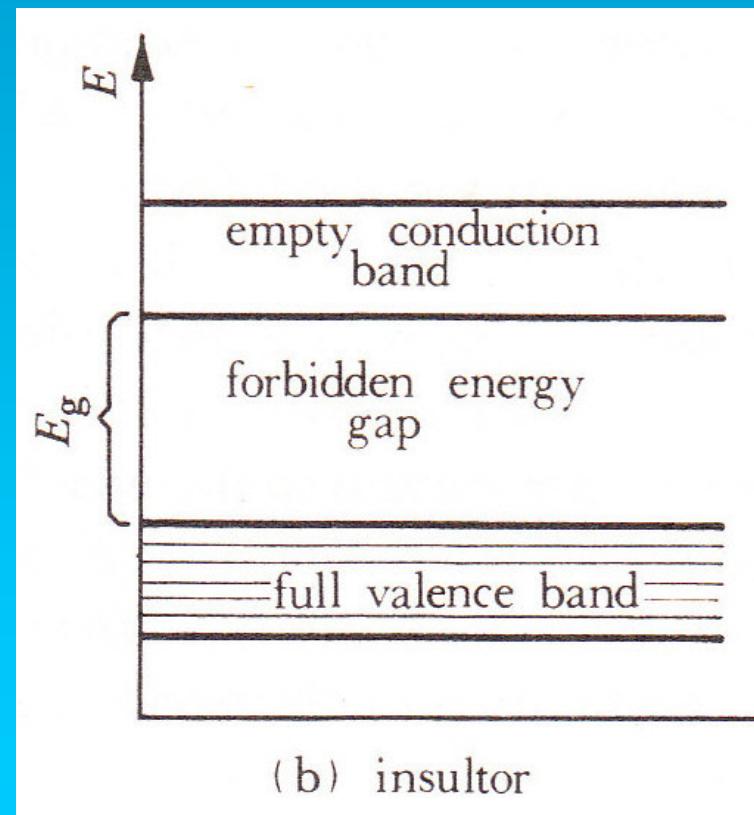


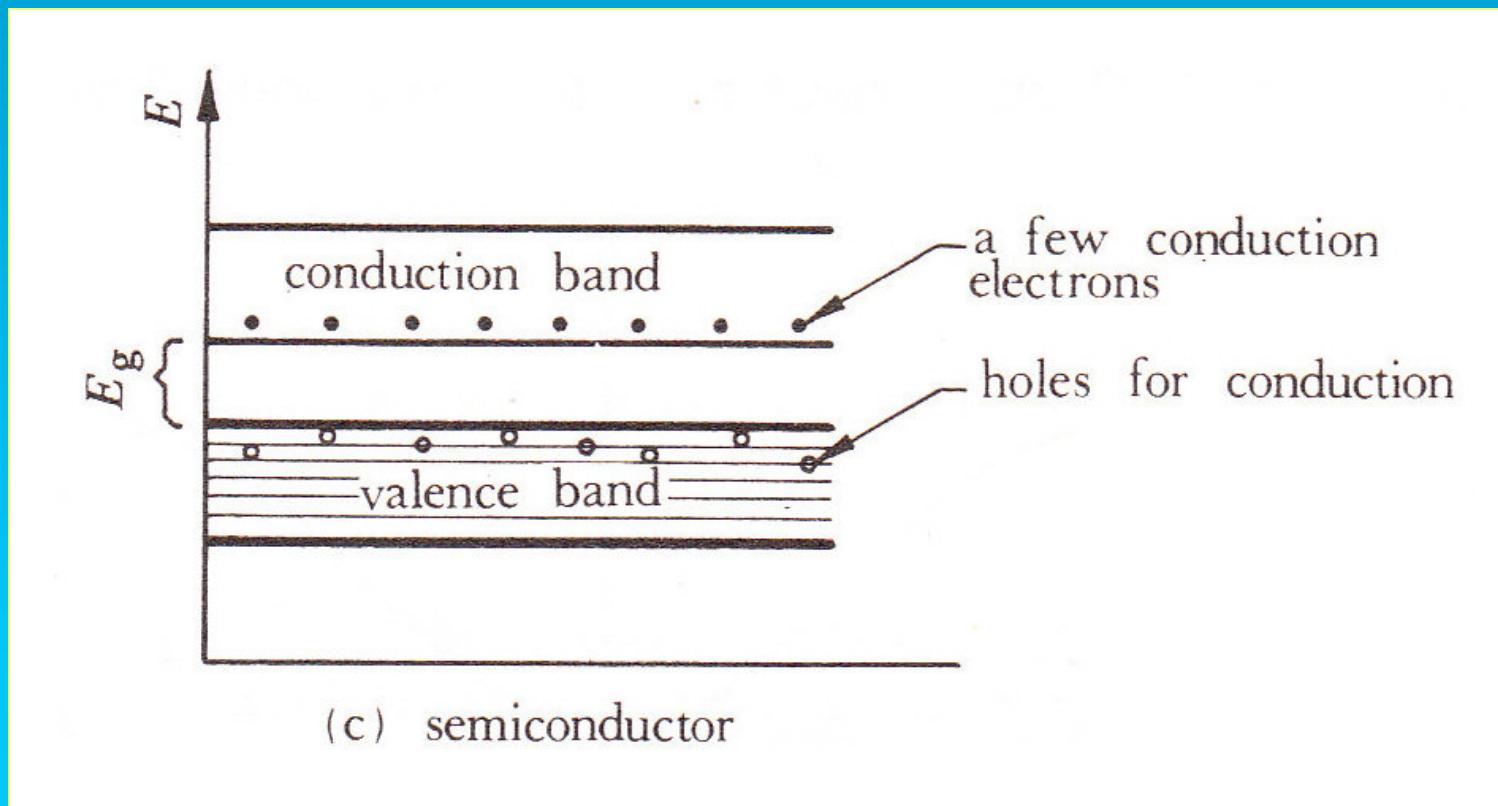
# Metal



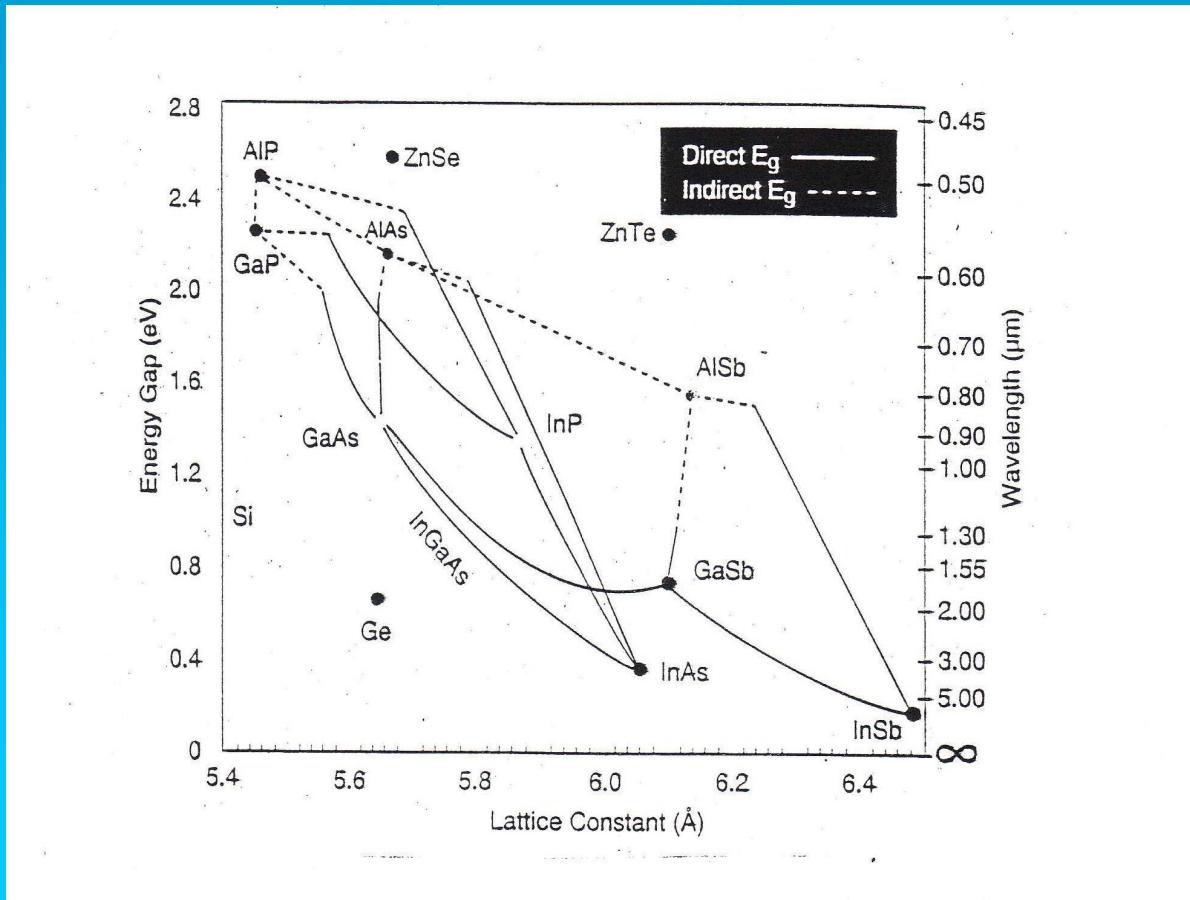
# Insulator



# Semiconductor



# Rosetta Stone in Bandgap Engineering



- Effective mass
- Electron and hole mobility

# Semiconductor heterojunction

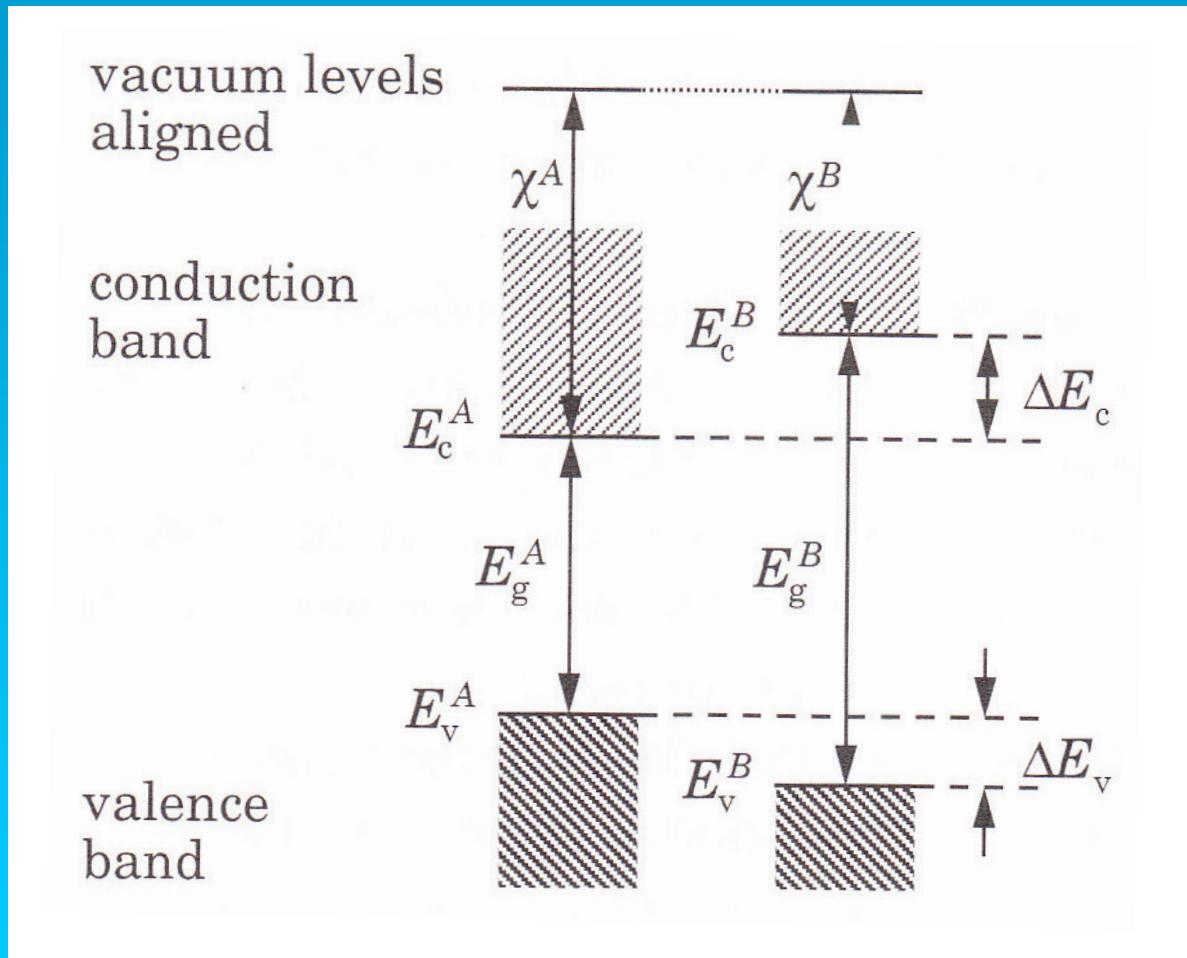
A junction between p-type and n-type layers in the same material is called a homojunction. A junction between two different materials is called a heterojunction. Heterojunctions are widely used in GaAs, InP and Si based electronic devices. They are also widely used in optoelectronic devices. The whole point of growing heterostructures is the opportunity that they offer to manipulate the behaviour of electrons and holes through band engineering.

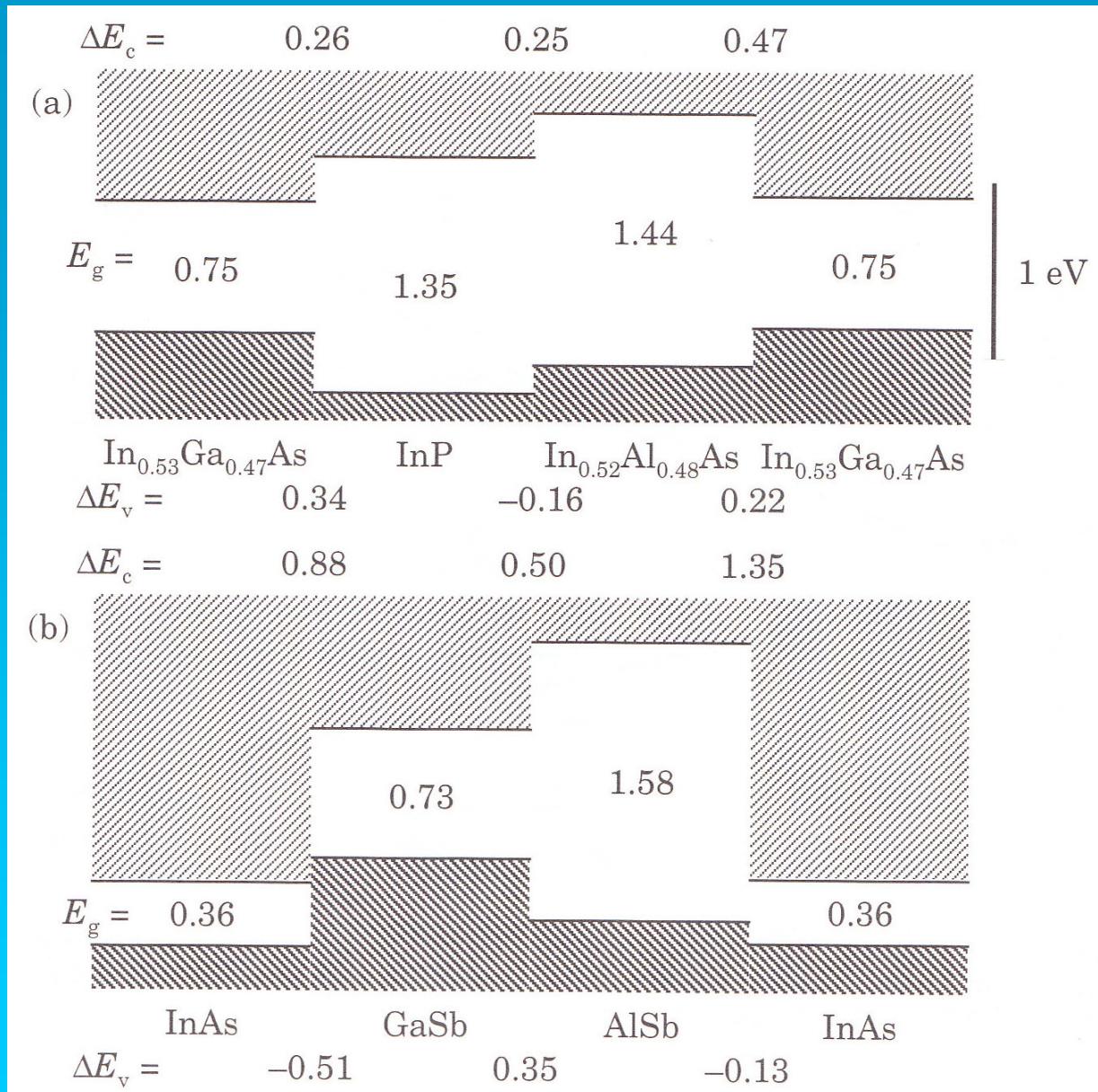
- It is shown that different materials have different band-gaps, now we need to look in more detail at the conduction and valence bands themselves,  $E_c$  and  $E_v$ . Consider a heterojunction between two materials A and B, with  $E_g^A < E_g^B$

# Anderson's rule

This is based on the electron affinity  $\chi$  of the materials, the energy required to take an electron from the bottom of the  $E_c$  to the vacuum level where it can escape from the crystal. The electron affinity is nearly independent of the position of the Fermi level, unlike the work function, which is measured from the Fermi level and therefore depends strongly on doping.

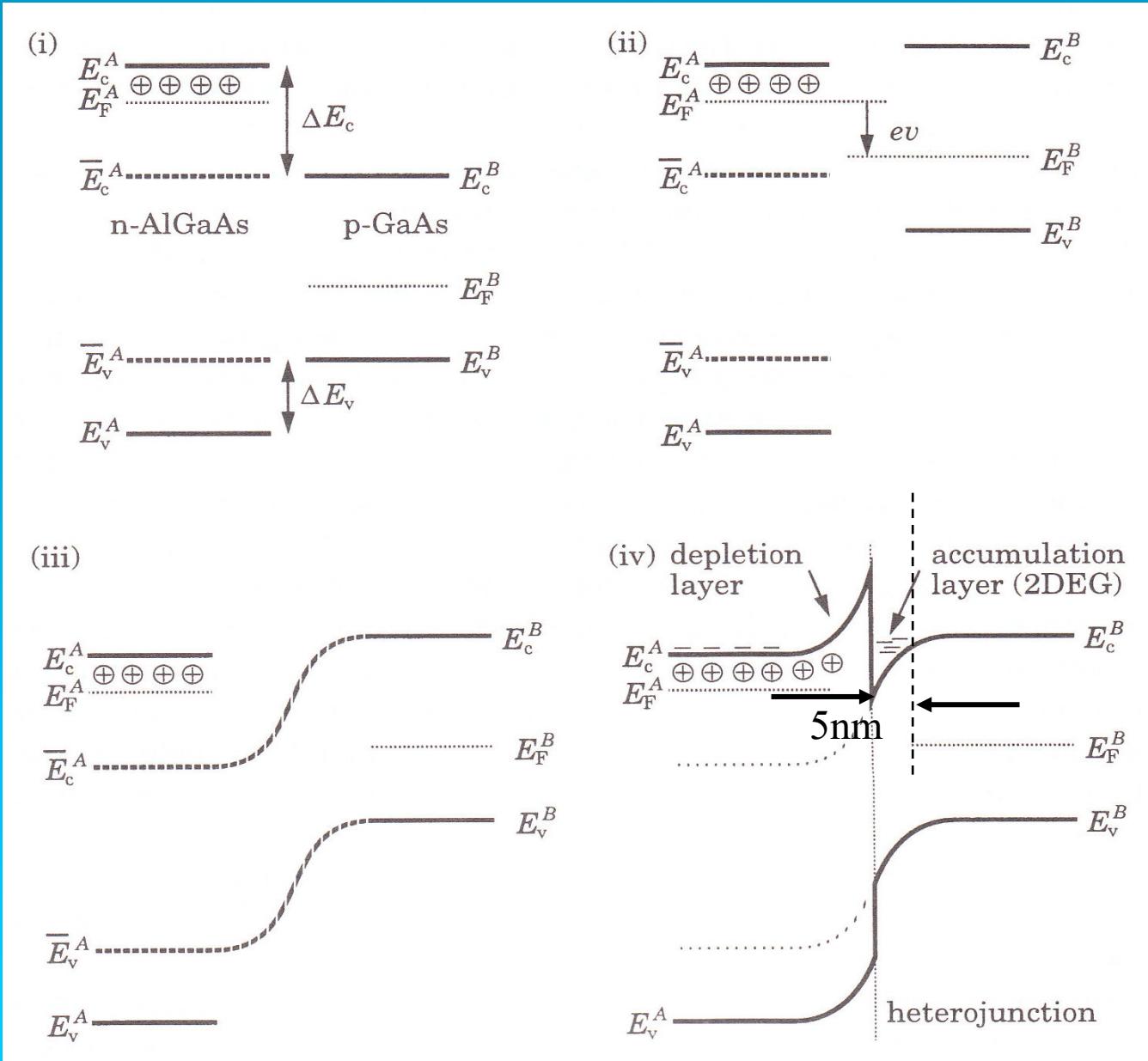
- Anderson's rule states that the vacuum levels of the two materials of a heterojunction should be lined up. This shows immediately that  $\Delta E_c = E_c^B - E_c^A = \chi^A - \chi^B$ .
- e.g. GaAs has  $\chi = 4.07\text{eV}$  and  $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$  has  $\chi = 3.74\text{eV}$ , predicting  $\Delta E_c = 0.33\text{eV}$





# Construction of band diagrams – taking into account of doping

In constructing semiconductor band diagrams, take into account the doping of the material, which will determine where the Fermi level lies and the band discontinuity, if one is aligning two different materials.



# Procedures

- Start with flat band in each material, with the bands in their natural alignment and the Fermi levels set by the doping on each side.
- Align the Fermi levels. Assume there is a positive bias  $v$  applied to the side B.
- Join  $E_c^A$  (bar) to  $E_c^B$  and  $E_v^A$  (bar) to  $E_v^B$ .
- Restore  $E_c^A$  on side A and  $E_v^A$ .

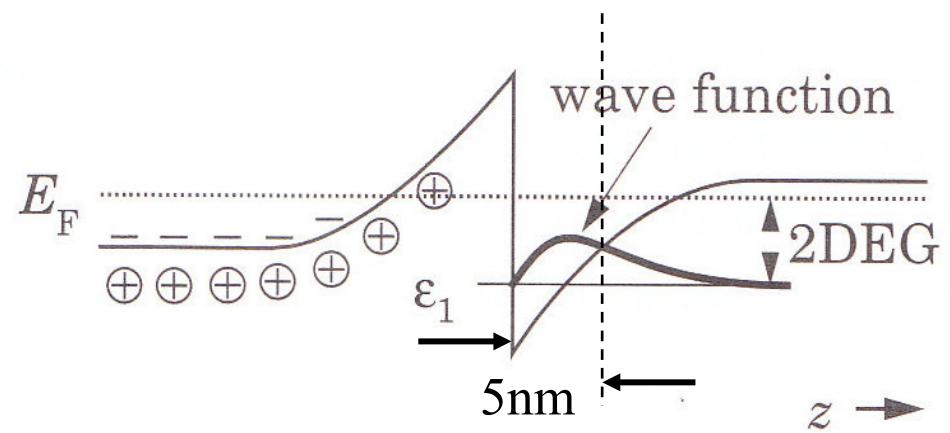
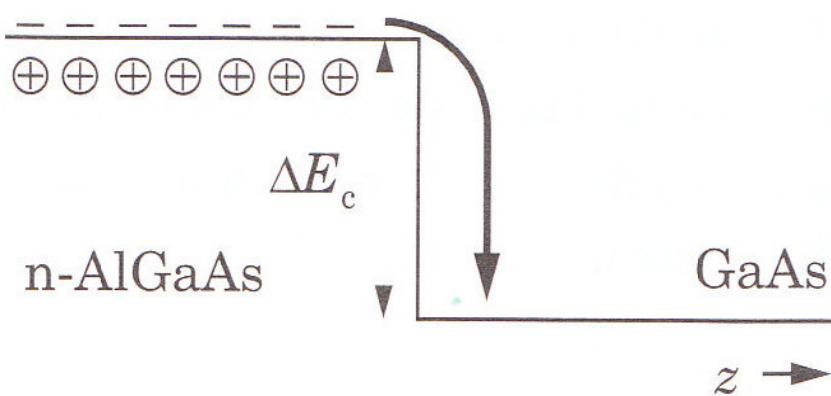
# High Electron Mobility Transistors (HEMT)

Main reasons for their superior behaviour

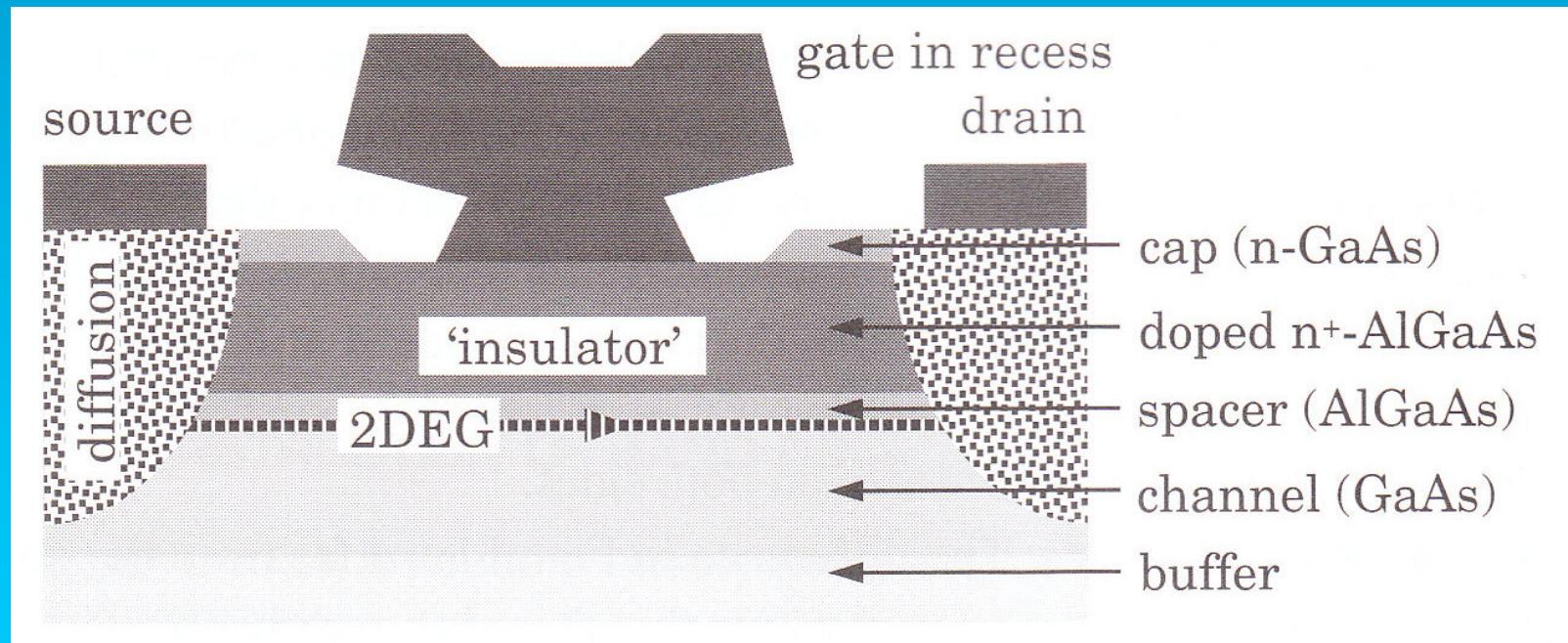
# Exploit design of material properties

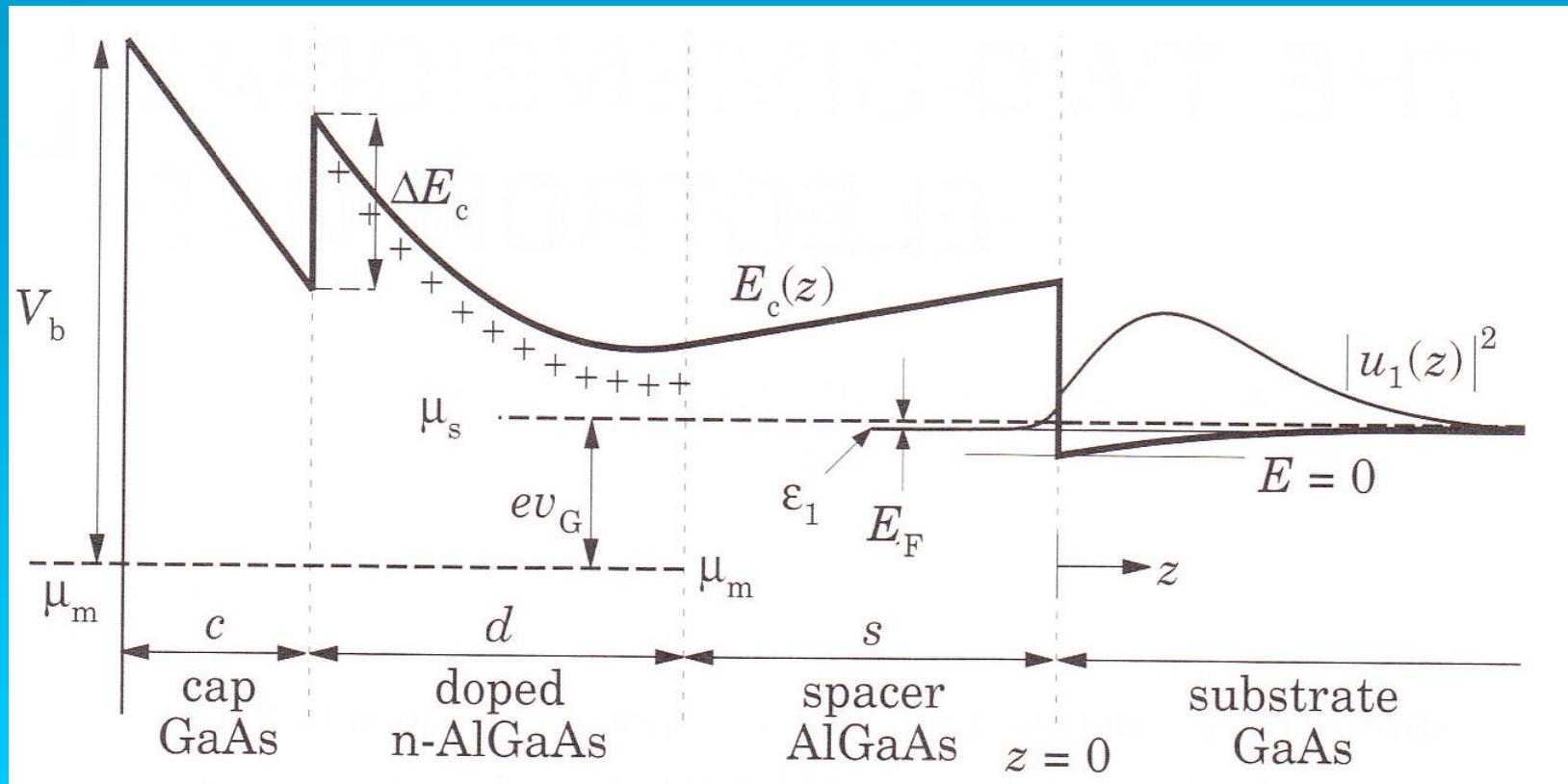
- High mobility due to reduced scattering because the donors are spatially separated from the carrier channel
- Can control gain by optimising carrier density, or space layer thickness, or distance between gate and channel
- Can choose material with a small effective mass – higher intrinsic carrier mobility

# Modulation doping



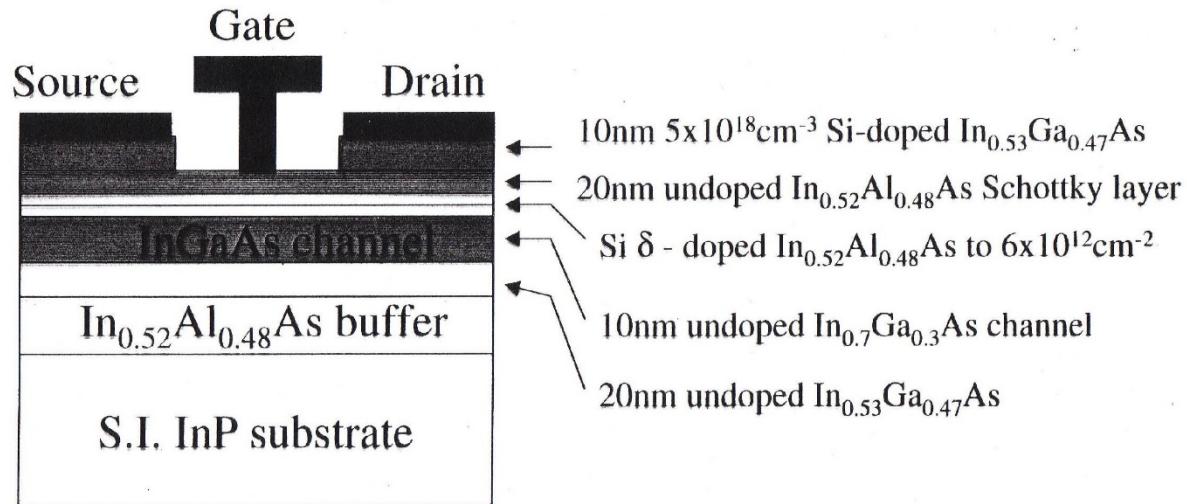
# GaAs/AlGaAs HEMT





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## **Application of reactive ion etching to the fabrication of 0.2micron gate length InP high electron mobility transistors**

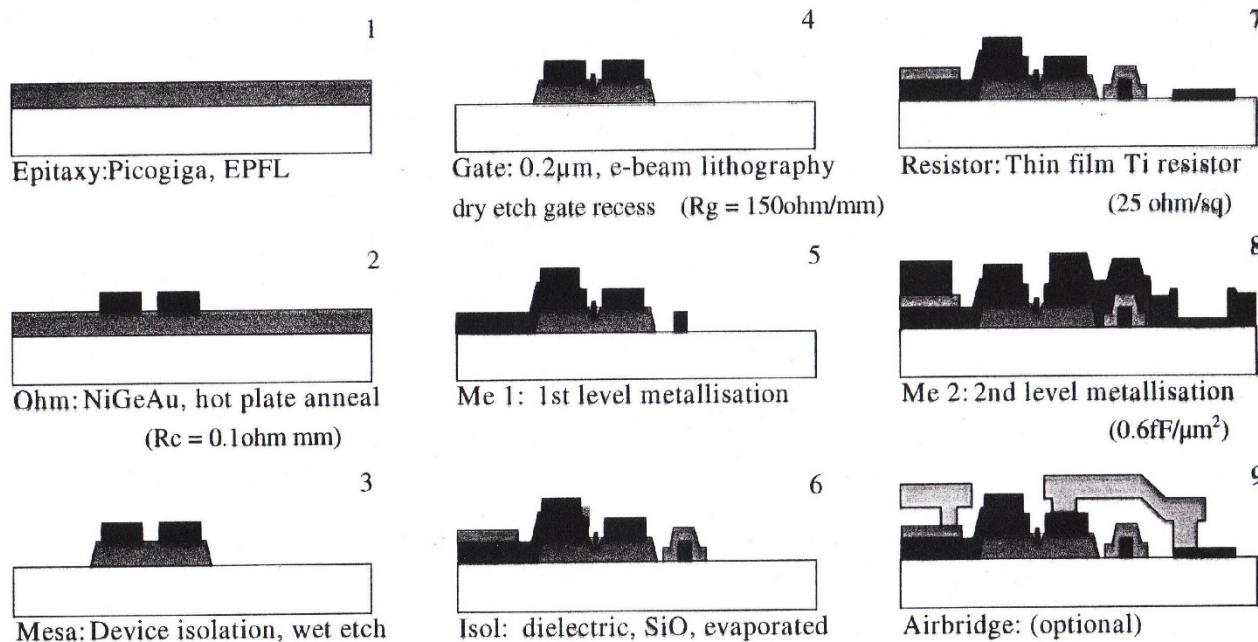


Room temp. mobility  
13,000 cm<sup>2</sup>/Vs

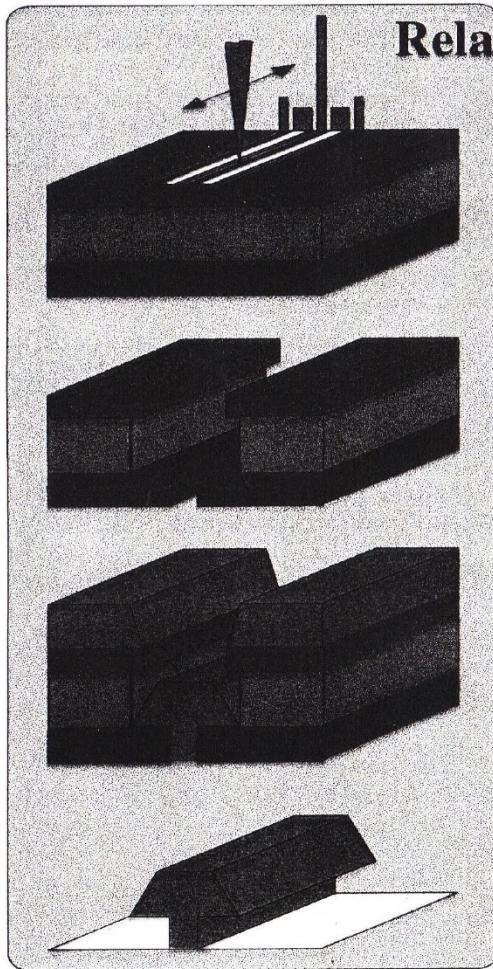
Carrier density  
 $3.2 \times 10^{12} \text{ cm}^{-2}$

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# Process schematic for MMIC



# T-gate fabrication

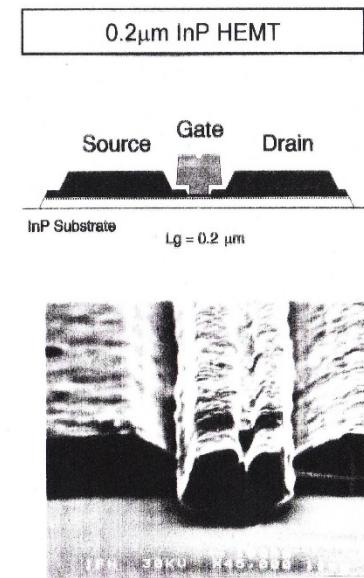


**e-beam exposure**  
**PMMA/P(MMA-MAA)/**  
**PMMA at 30kV, 100pA**

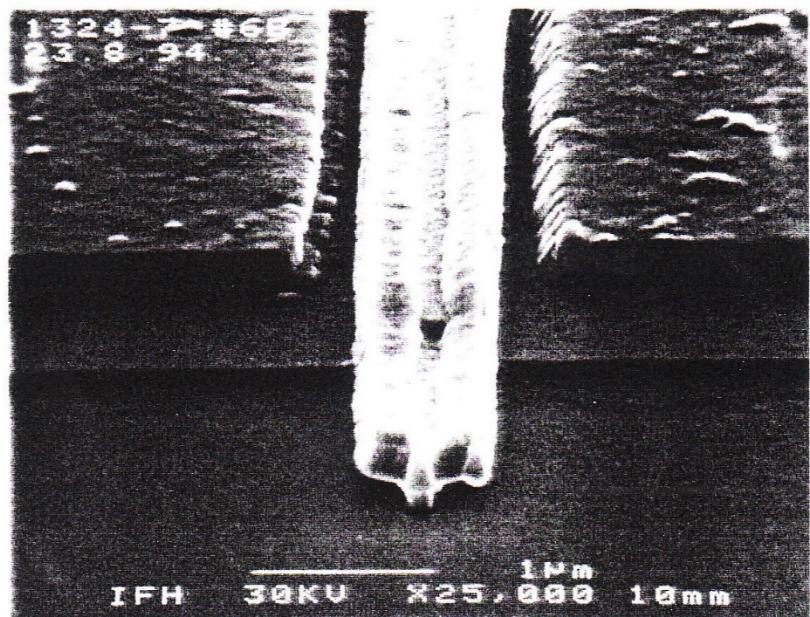
**Development**  
**1:3, MIBK:IPA**  
**Single development**

**Metallisation**  
**Ti/Au, 20/250nm**

**T-gate structure**  
**Standard lift-off process**

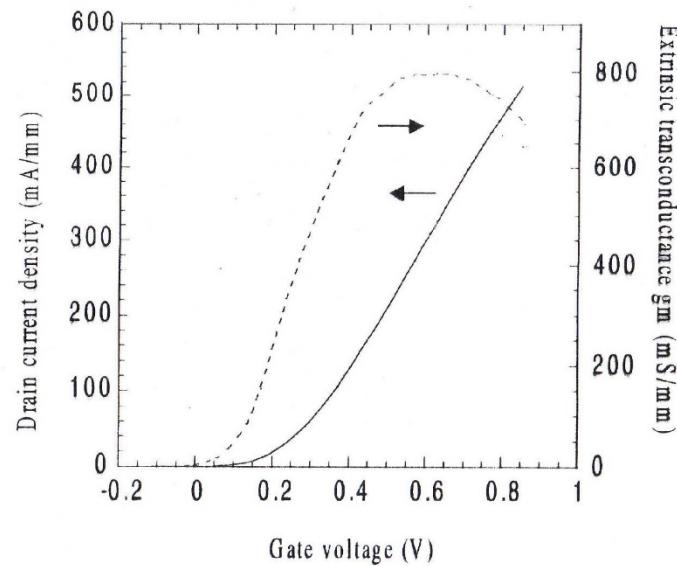
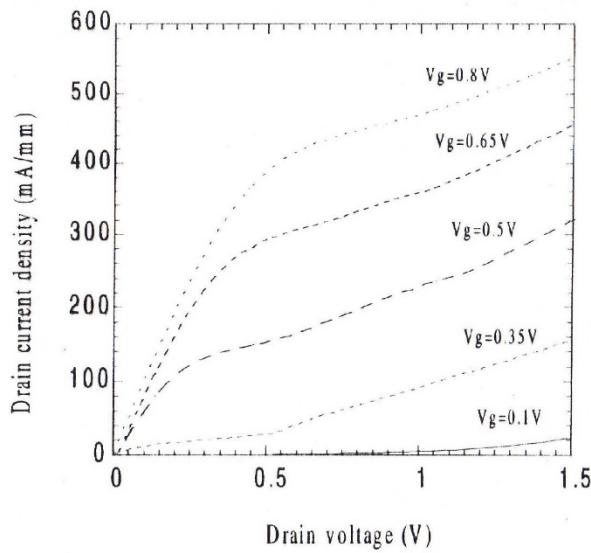


SEM Micrograph of an 0.2 $\mu$ m Transistor



InP HEMT, 1.4 $\mu$ m source-drain  
0.2 $\mu$ m gate-length

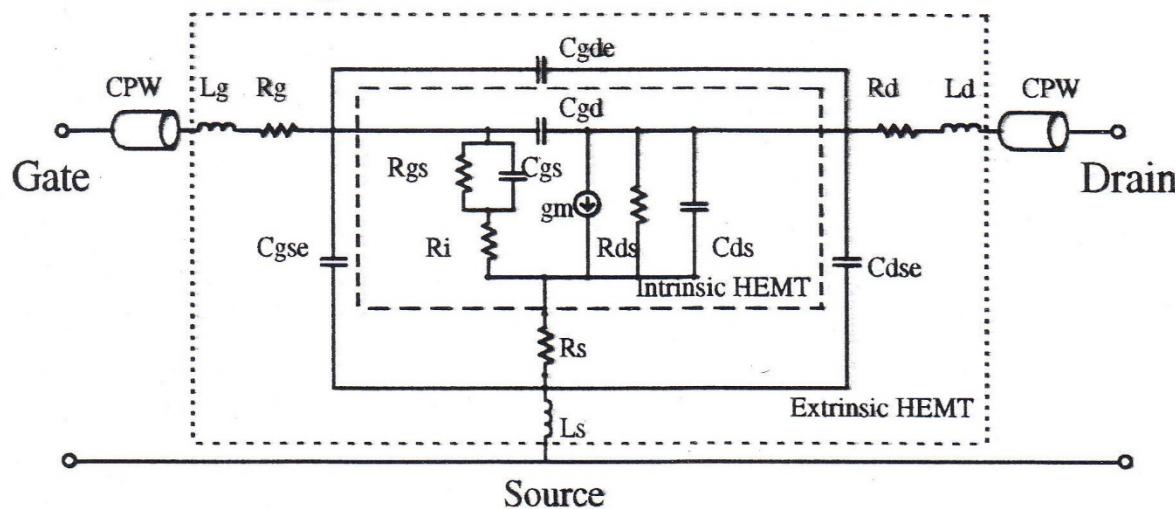
## Typical dc characteristics for the enhancement mode FETs



- Threshold voltage at  $\sim 0.1V$
- Extrinsic transconductance  $\sim 800mS/mm$
- Non-saturation of output conductance

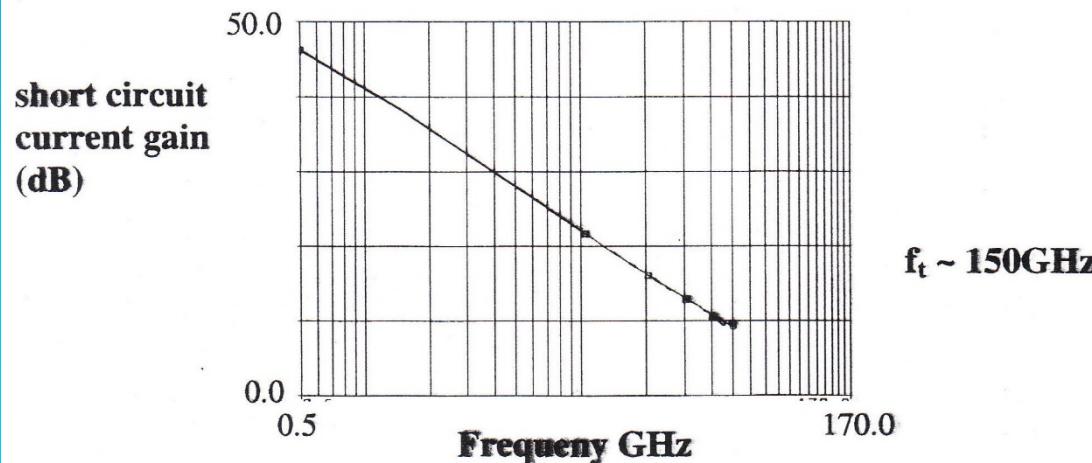
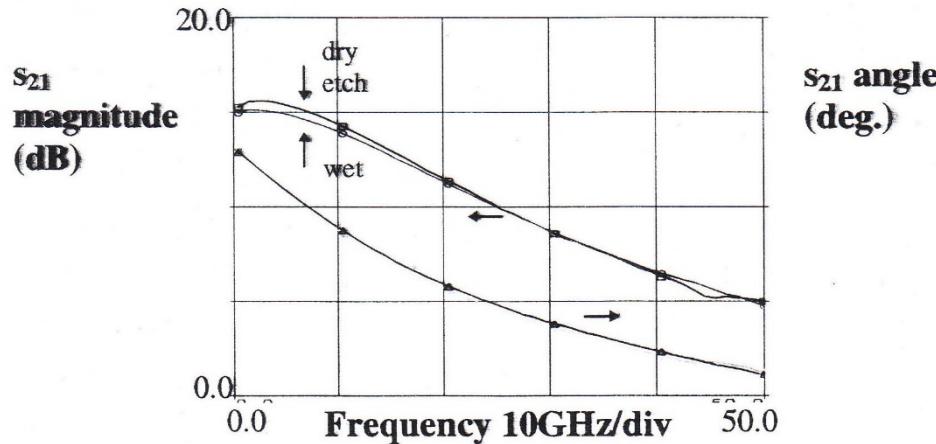
# High frequency performance

- small signal model

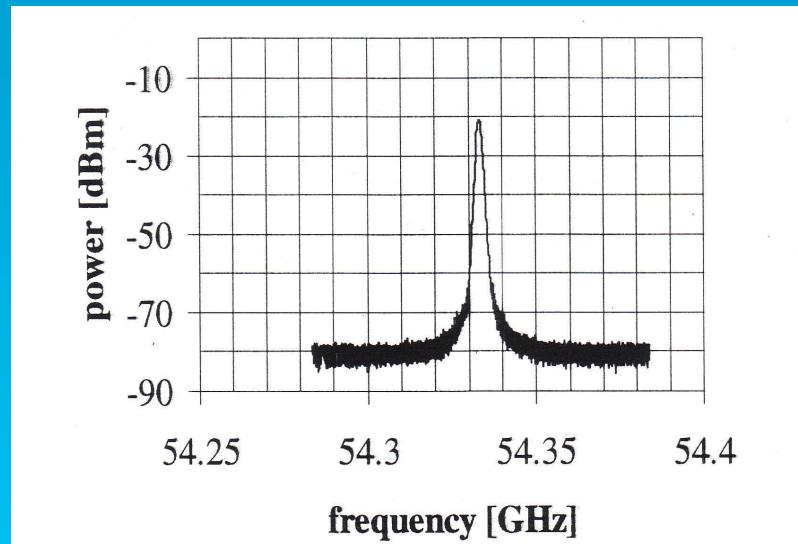
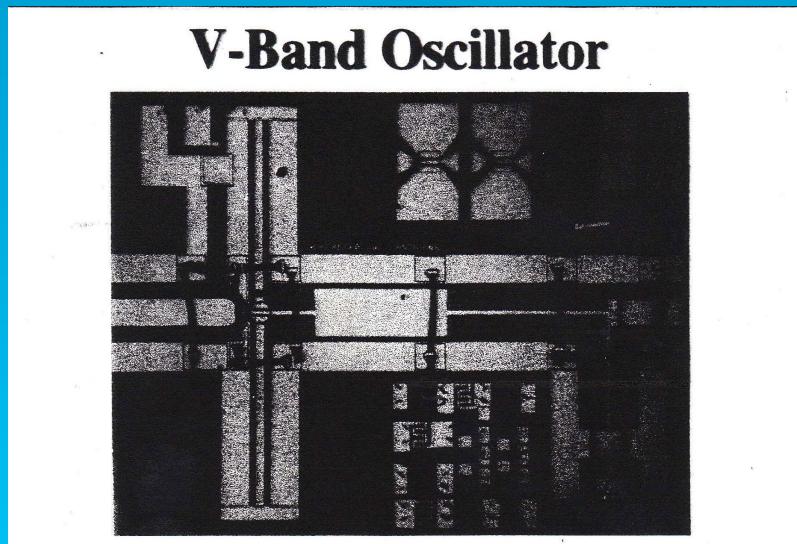


# High frequency performance

- wet (modelled) and dry etch

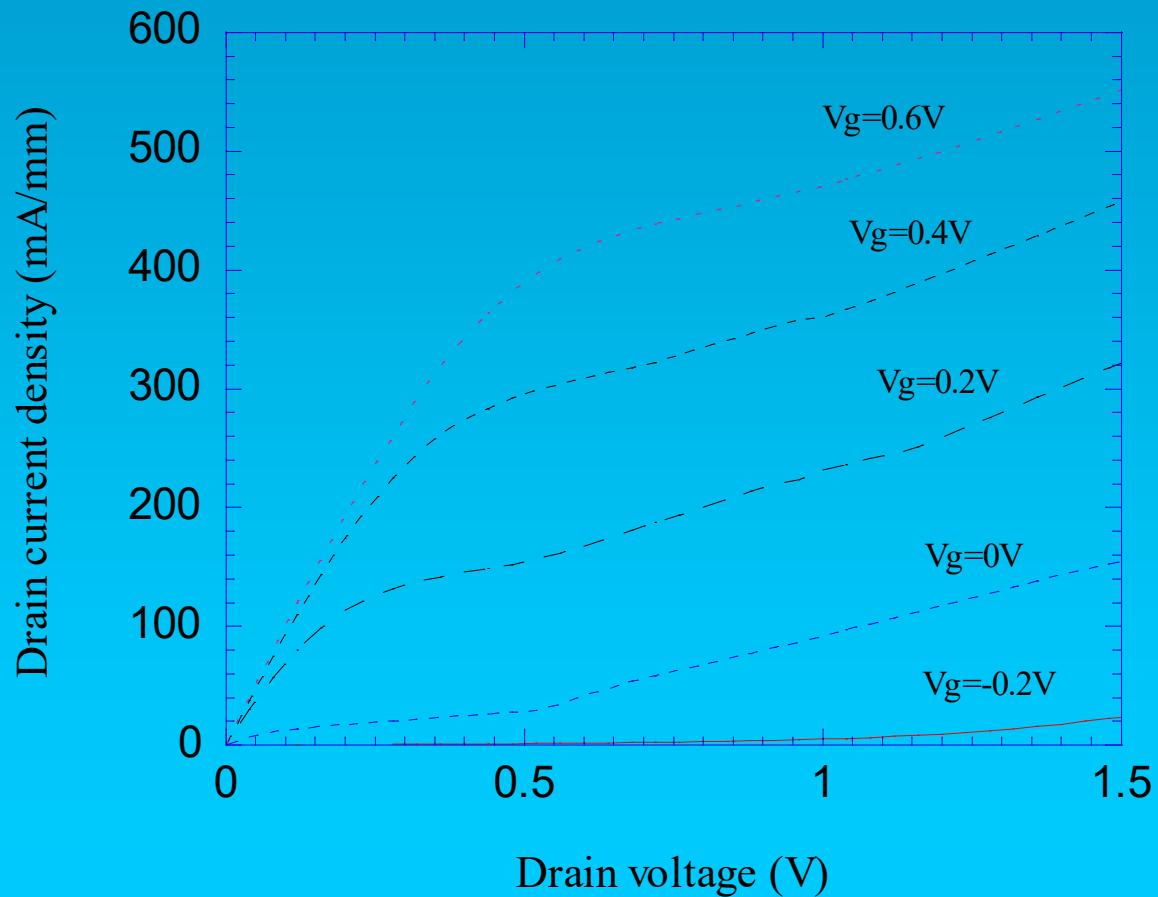


# High frequency performance

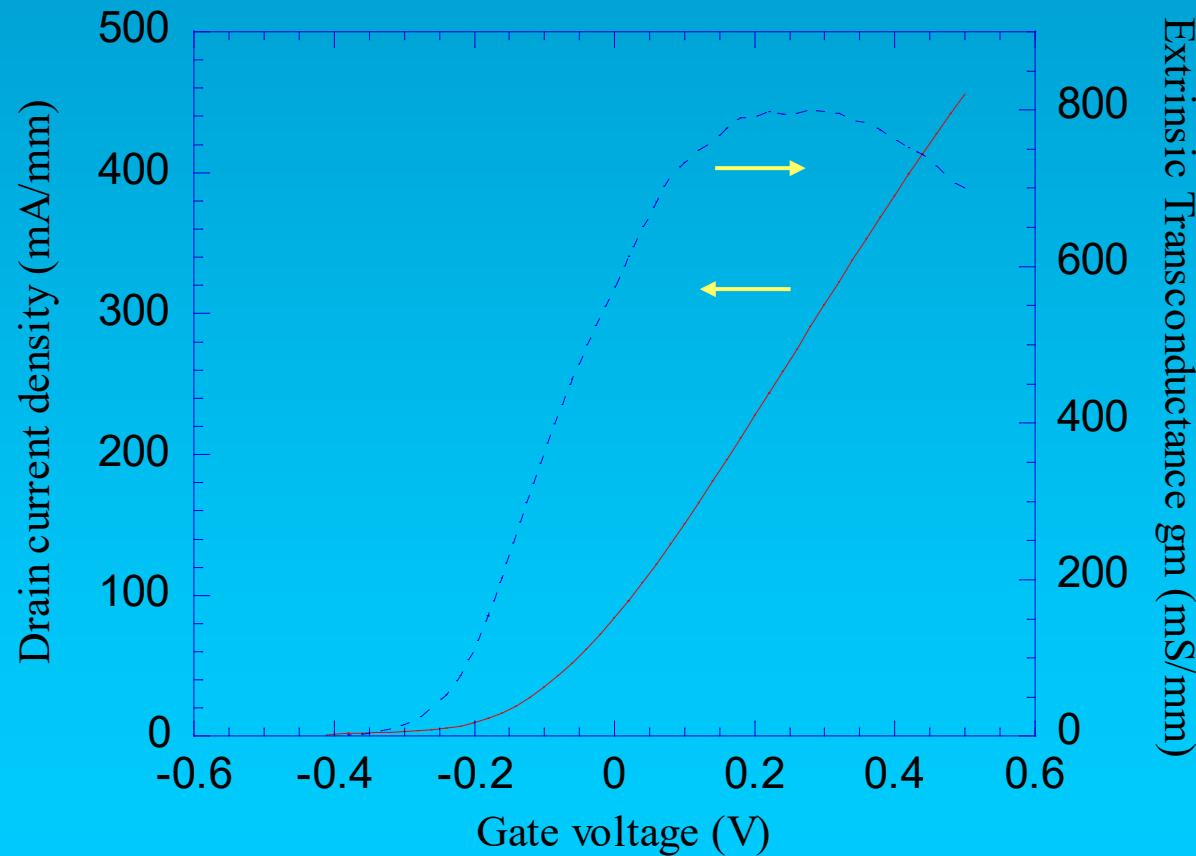


Output power 4dBm  
Phase noise  $\sim -115$  dBc/Hz @ 10MHz

# $I_d$ - $V_d$ characteristics



# $I_d$ and $g_m$ versus $V_g$ characteristics



Important equations :

$$g_m = g_i / (1 + g_i R_s)$$

where  $g_m$  is the extrinsic transconductance,  $g_i$  is the intrinsic transconductance and  $R_s$  is the source resistance.

$$g_m = \partial I_d / \partial V_G$$

$$g_i = (q\mu n) / L \left\{ 1 + [q\mu n \cdot d / \epsilon v_s L]^2 \right\}^{1/2}$$

where  $q$  is the electronic charge,  $n$  is the electron density,  $\mu$  is the carrier mobility,  $v_s$  is the carrier saturation velocity,  $L$  is the gate length of the device.

Note that  $d = d_d + d_i$

where  $d_d$  is the thickness of the doped AlGaAs layer and  $d_i$  is the spacer layer thickness.

Decreasing  $d$  may improve the device performance because of a large charge transfer across the heterointerface - increase in  $n$ , even though the maximum value of the low field mobility -  $\mu$ , decreases with decreasing  $d$ .

The maximum transconductance increases with increasing threshold voltage, with increasing doping of the AlGaAs layer and with decreasing space thickness. The reason for this is that all these factors bring the channel closer to the gate.

- By gate recess
- Figure of merit for high frequency performance :
- $f_T = g_m(\max) / (C_g + C_i)$

where  $C_g$  is the gate capacitance and  $C_i$  is the interconnect and fringing capacitance.

- By making T-shaped gates – decreases the RC time constant for switching