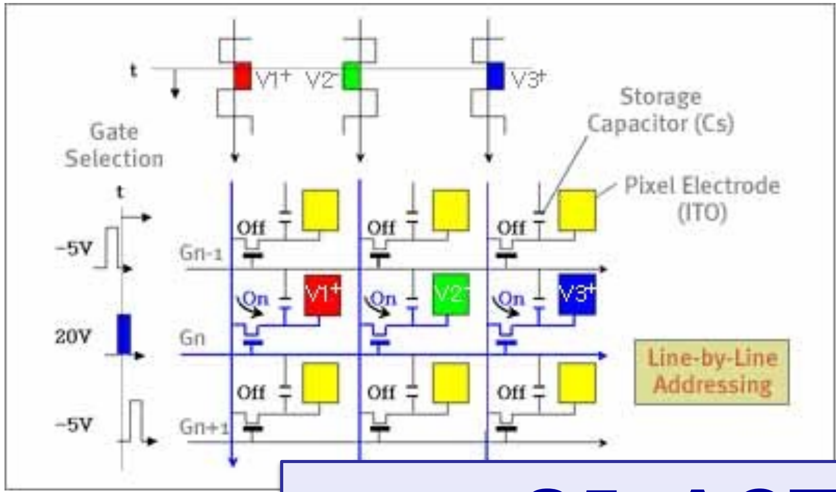
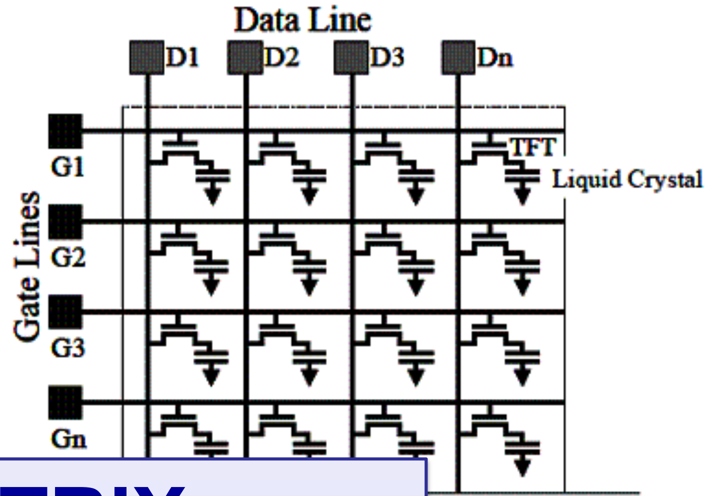




S5. ACTIVE MATRIX LCD ADDRESSING AND ELECTRONICS

Why AM Aim of AM Principles

Electronic subsystems

Timing Waveforms Kickback

Why active matrix addressing?

REVIEW CONSTRAINTS OF PM ADDRESSING

Passive matrix is

- (In principle) simple
- Uses low-tech, low-cost backplane technology

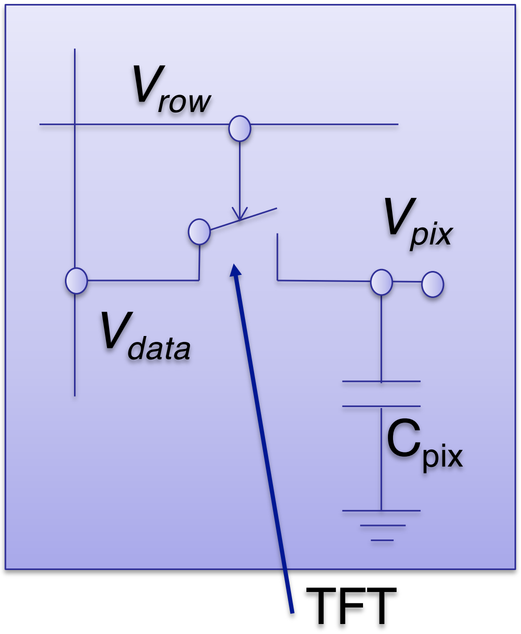
But due to low duty cycle and crosstalk

- Requires very sophisticated drive waveforms
- Still cannot drive very large numbers of rows
  - Each row of pixels is “intentionally” addressed for at most 1/n of the frame time (where n = number of rows)
  - Each row of pixels is subject to the data signals that drive the other rows of pixels (for (n-1)/n of the frame time)

The Aim of Active Matrix Addressing

The aim of AM Addressing is to overcome the limitations of PM Addressing by

- Increasing the duty cycle
  - Putting the drive signal into the pixel electrode during a line-addressing time <u>and</u> keeping it there for all or most of the frame time
- Reducing cross-talk
  - Isolating the pixel electrode from the effect of signals driving pixels in other rows
- In short we need a non-linear element in each pixel
  - In practice this is frequently implemented as a "sample-and-hold" circuit as show



Active Matrix

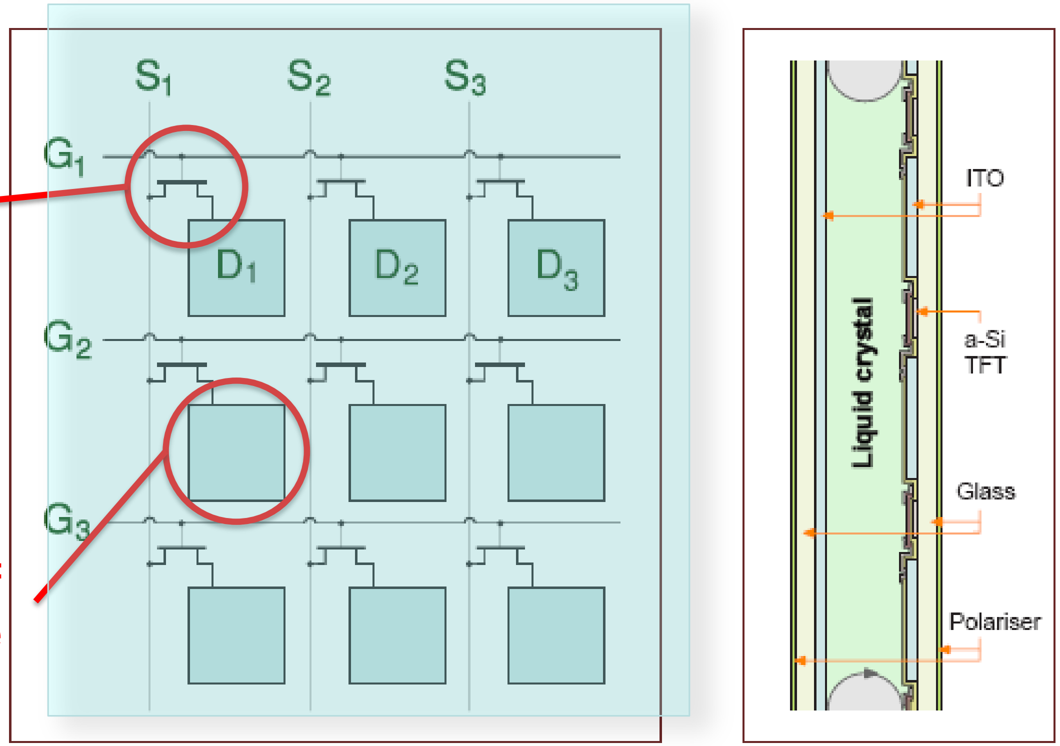
Row and column electrodes on active (back) substrate

Common electrode on front substrate

Switch = TFT

- Active switch and storage element per pixel isolates electronic addressing of pixel from drive EO element
- Per row / column
  - One driver
  - One connecting wire

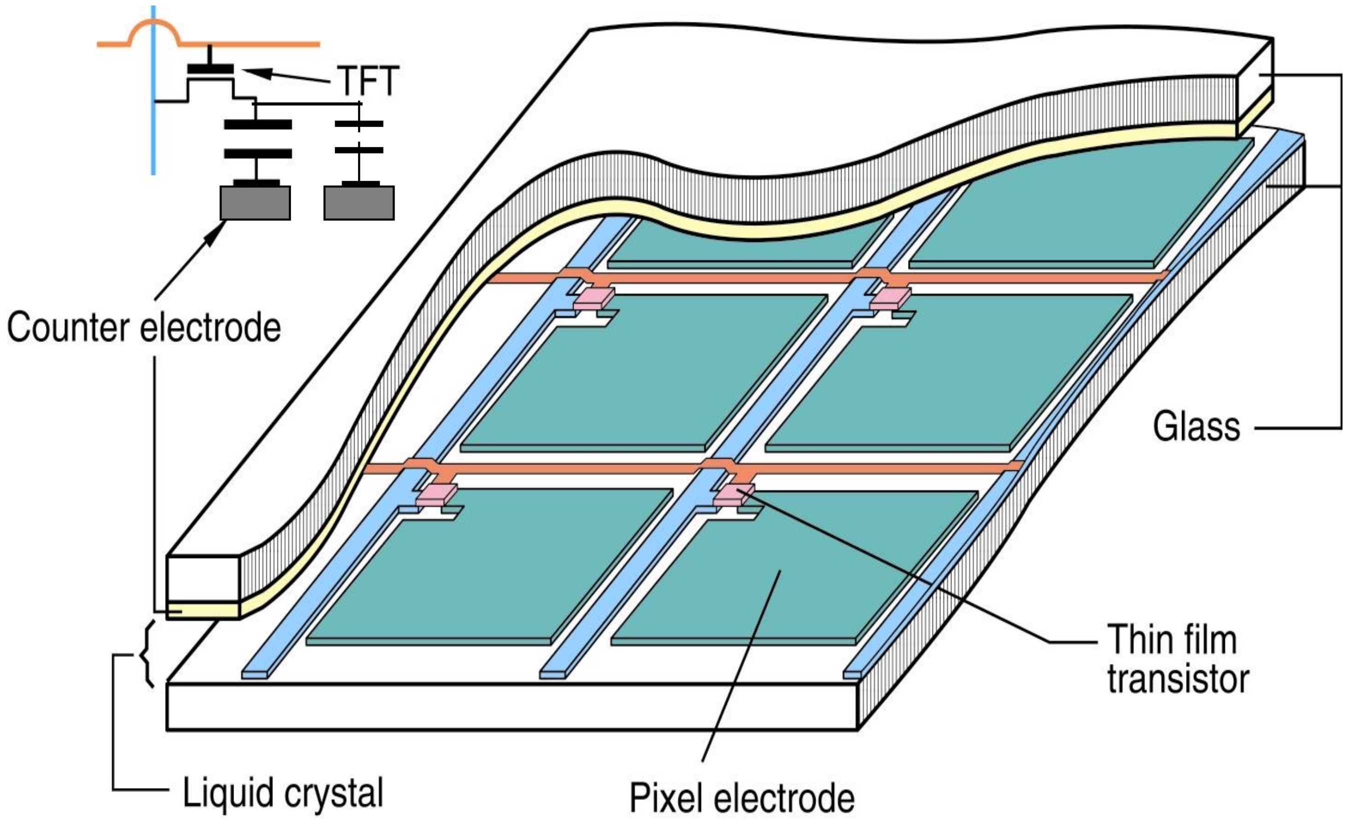
Storage Cap = pixel electrode



- MxN pixels requires only M+N drivers

Active matrix LC display

TFT-LCD Exploded View

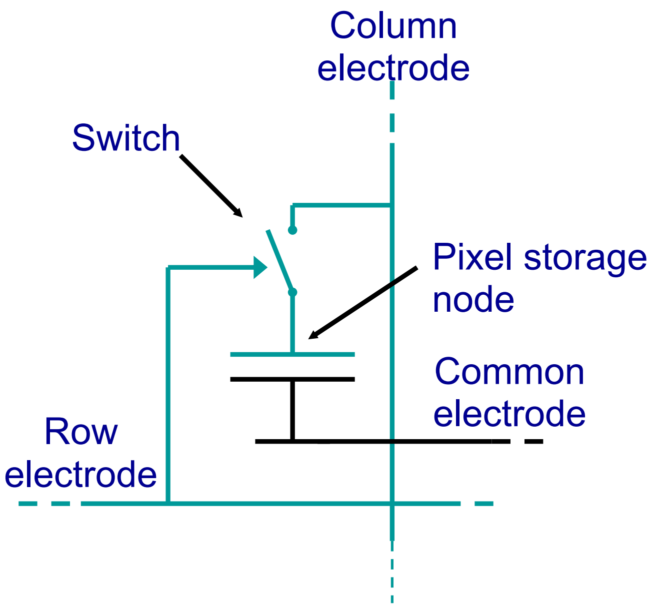


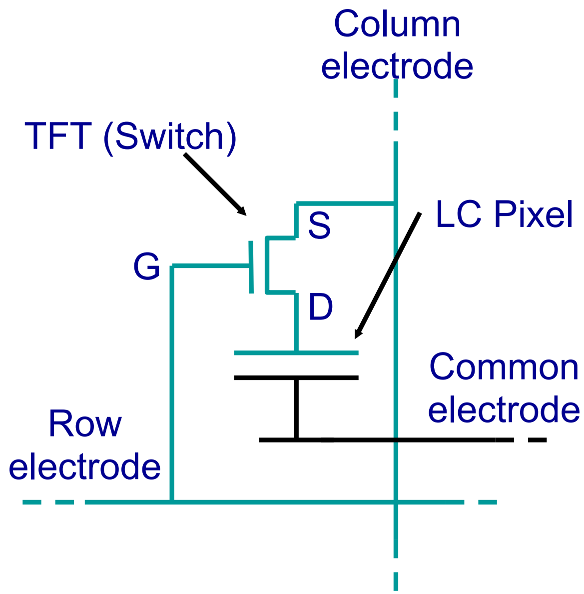
Active Matrix Technologies

AM **technology** =
content of ***NEXT*** lecture

- **LCD**
  - **Active Matrix**
    - **TFT**
      - **LC on Si (LCoS)**
      - **α-Si TFT**
      - **HT Poly-Si TFT**
      - **LT Poly-Si (LTPS) TFT**
      - **Organic / plastic TFT**
      - **IGZO TFT (Indium Gallium Zinc oxide)**
    - **MIM**
      - **Thin Film Diode (TFD)**
  - **Passive Matrix**

AM Pixel Circuit



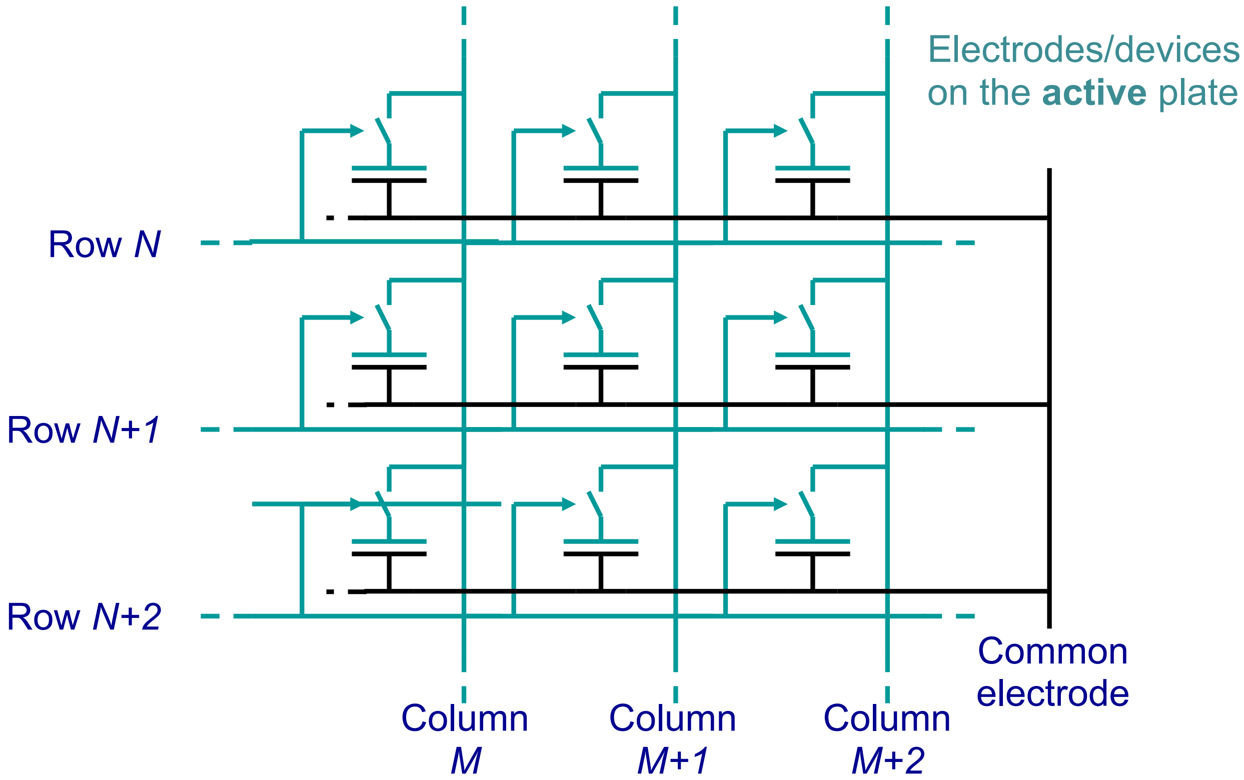


Active Matrix Addressing

- Reduces crosstalk
- Simplifies addressing waveforms
- Increases pixel drive time from 1/N of field time to ~ field time
- Allows more rows of pixels

DM-MJR

Active Matrix Structure



Row Sequential Addressing 1/5

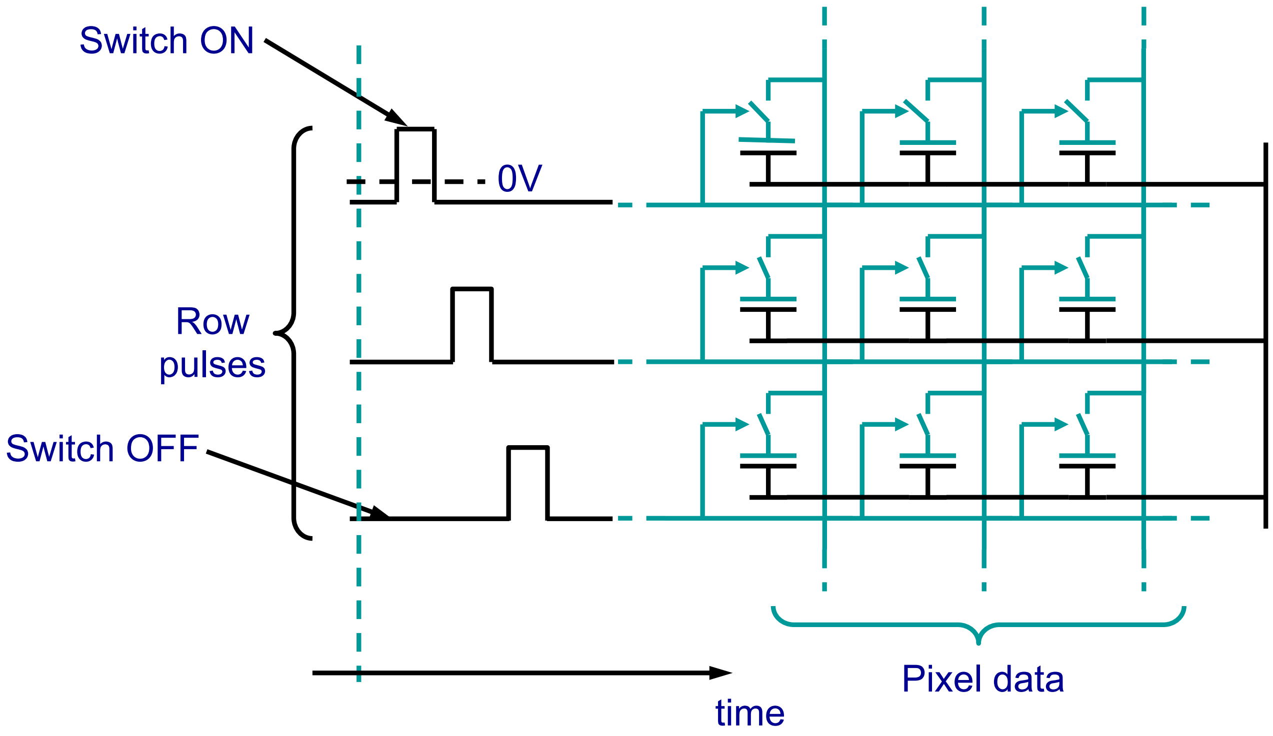
Each row of pixels is addressed in sequence

Pixel data is applied to the column electrodes

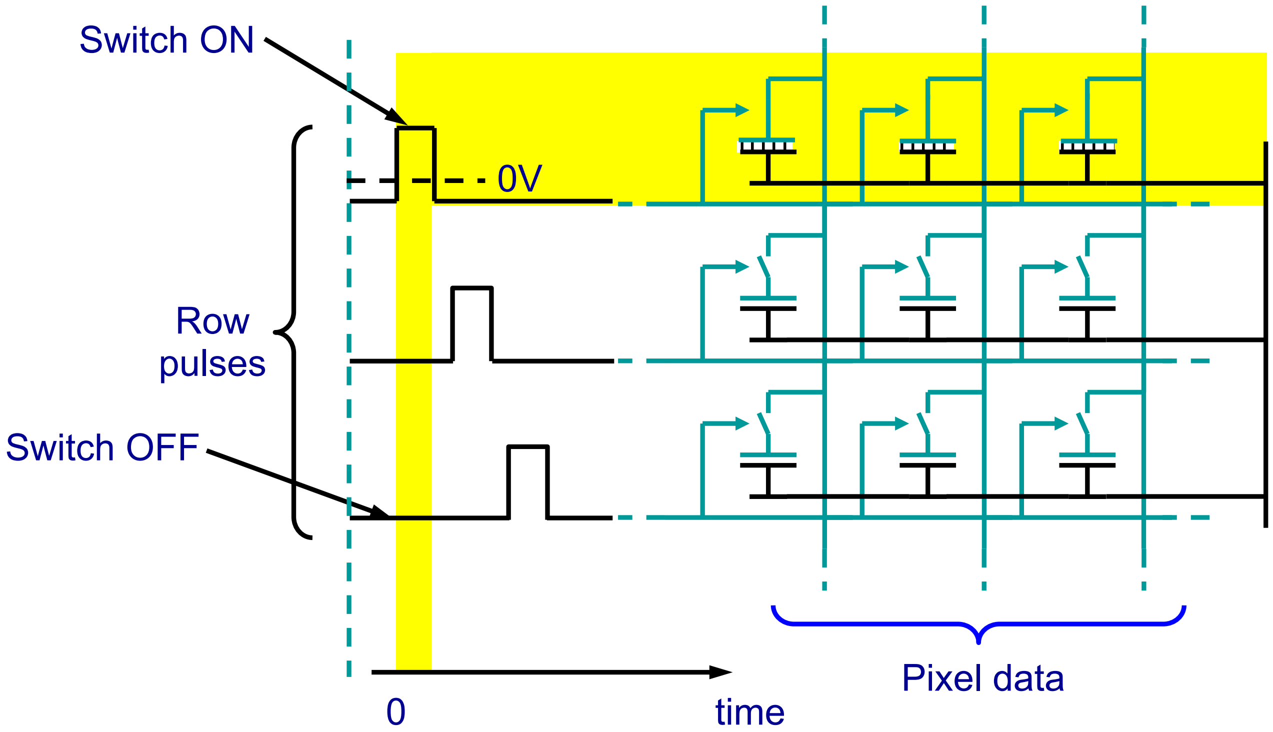
Column data is transferred into a row of pixels
- Achieved by applying a pulse to the row electrode
- Closes the switches (turns the TFTs on)
- Charges up the pixel capacitance, C_{LC}

When pixel is charged the TFT switch is opened
- Pixel capacitance is isolated
- Charge remains on pixel

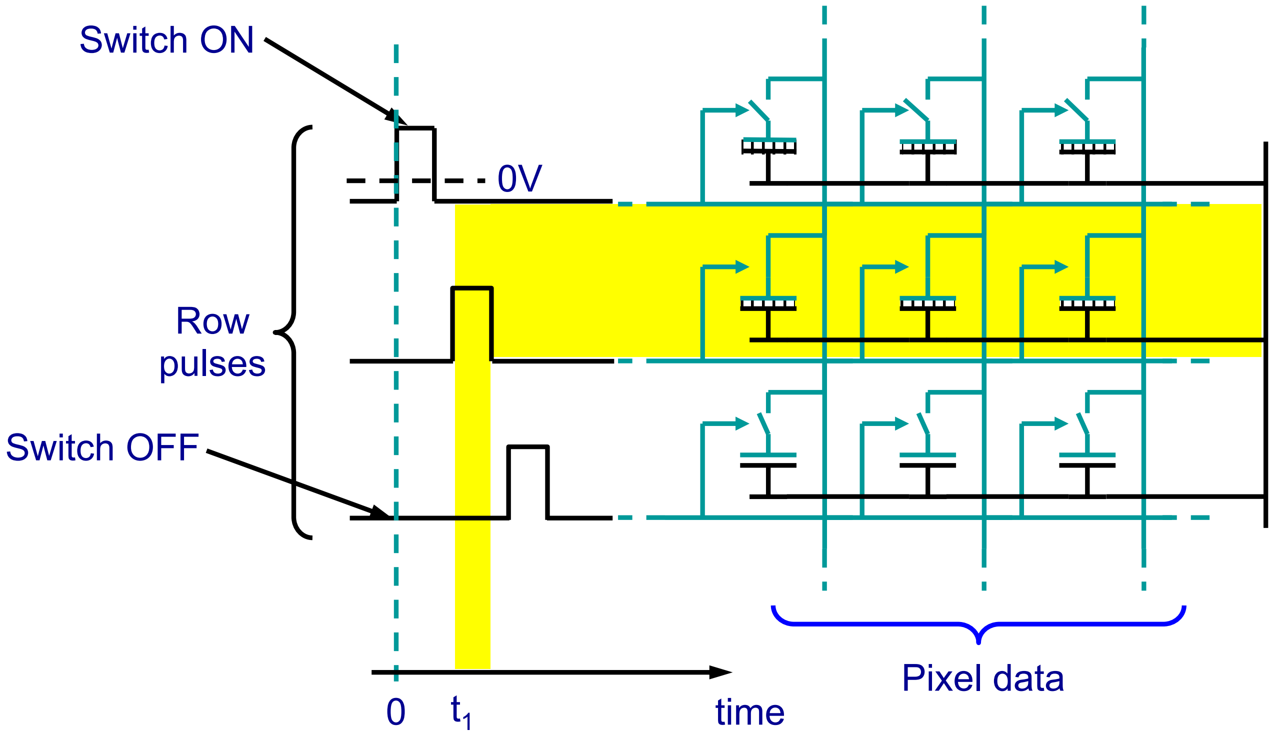
Row Sequential Addressing 2/5



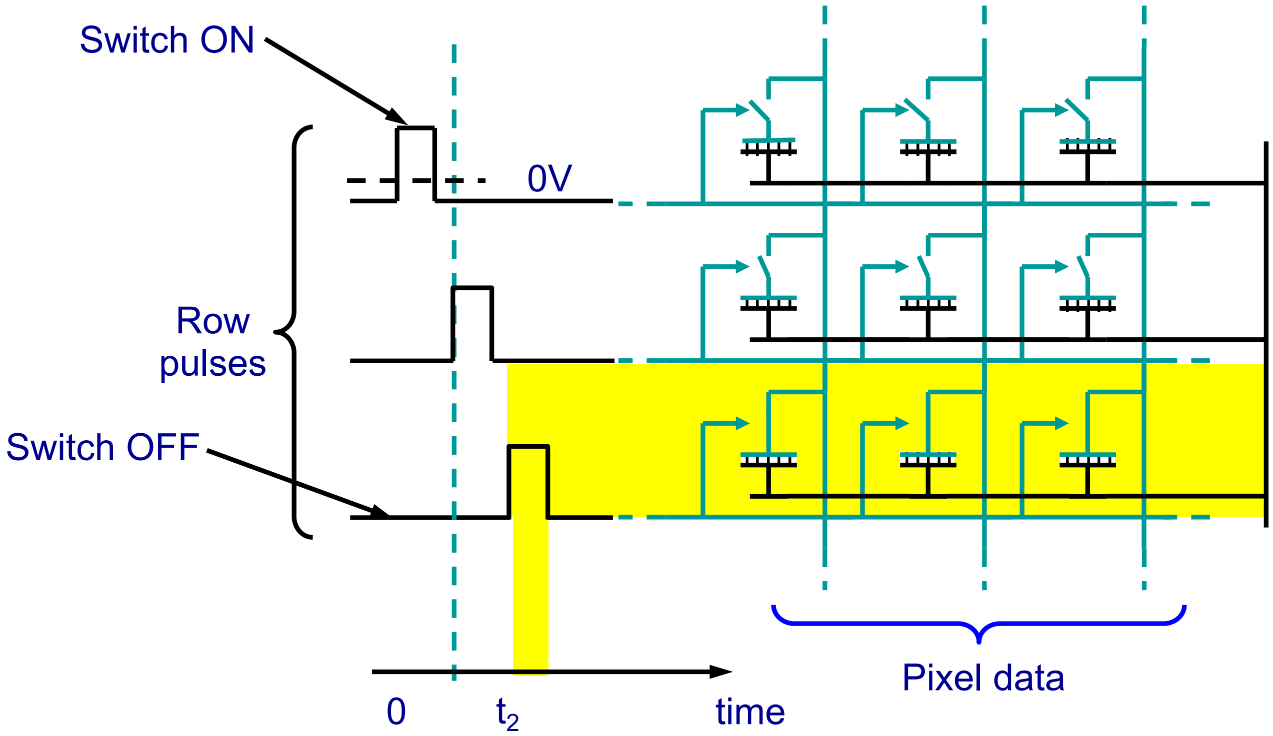
Row Sequential Addressing 3/5



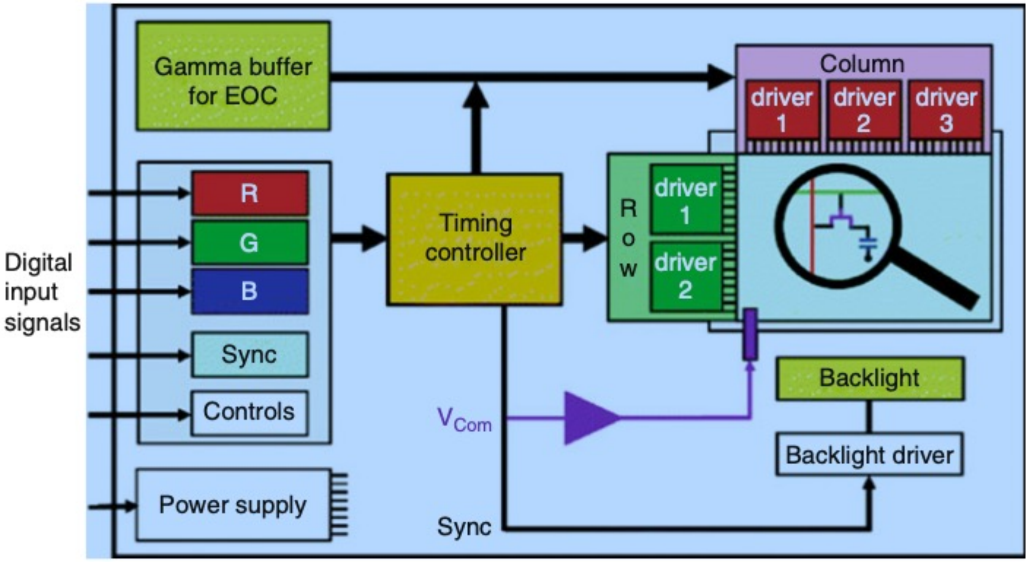
Row Sequential Addressing 4/5



Row Sequential Addressing 5/5



AM LCD Module (including backlight)



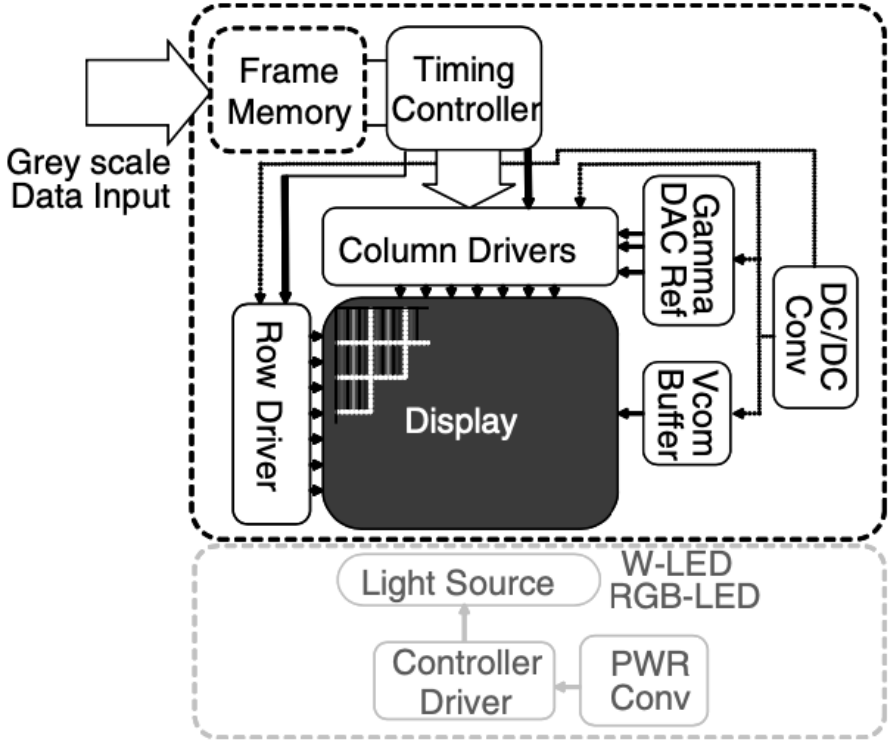


Figure 9.3 The major functions within an Active Matrix LCD

Panel Interface Timing

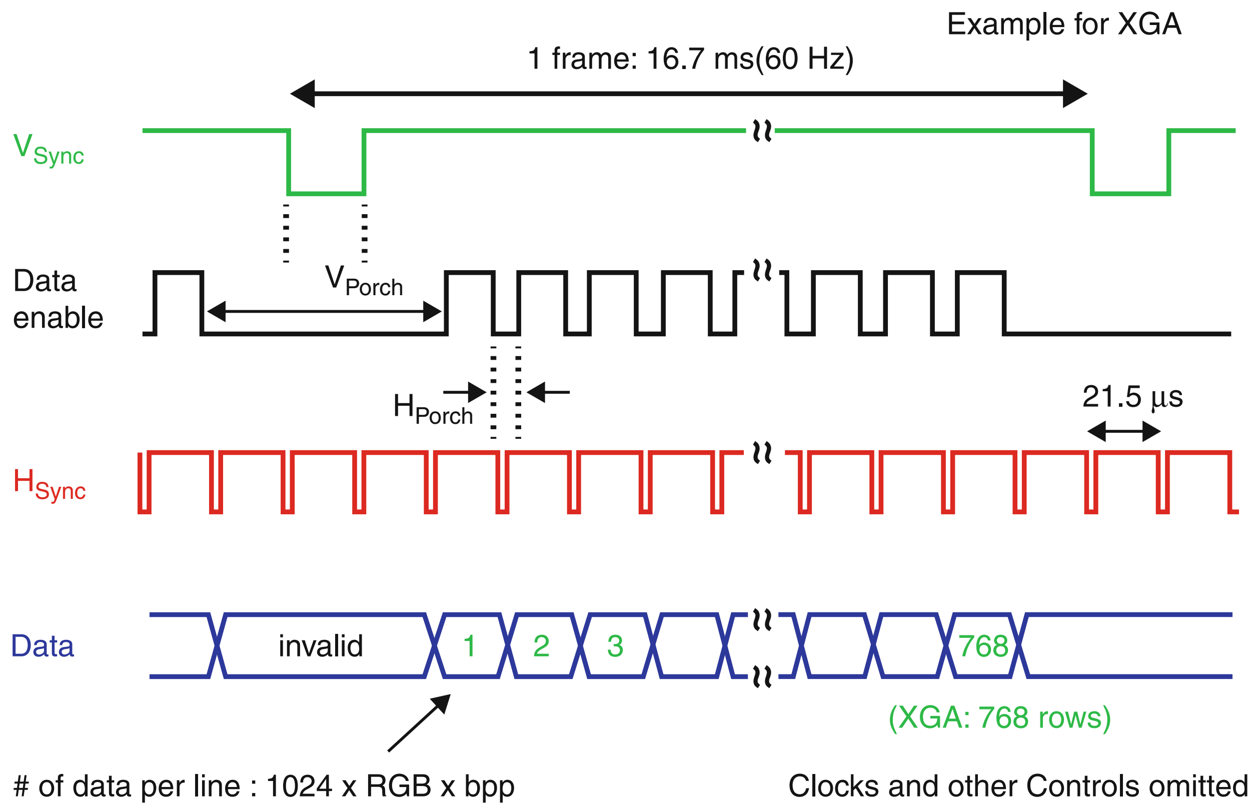


Fig. 2 Typical example of parallel panel interface timing which is practically the same for Timing Controller data input (for details see section "Timing Controller and Intrapanel Interface")

LCD Timing Controller

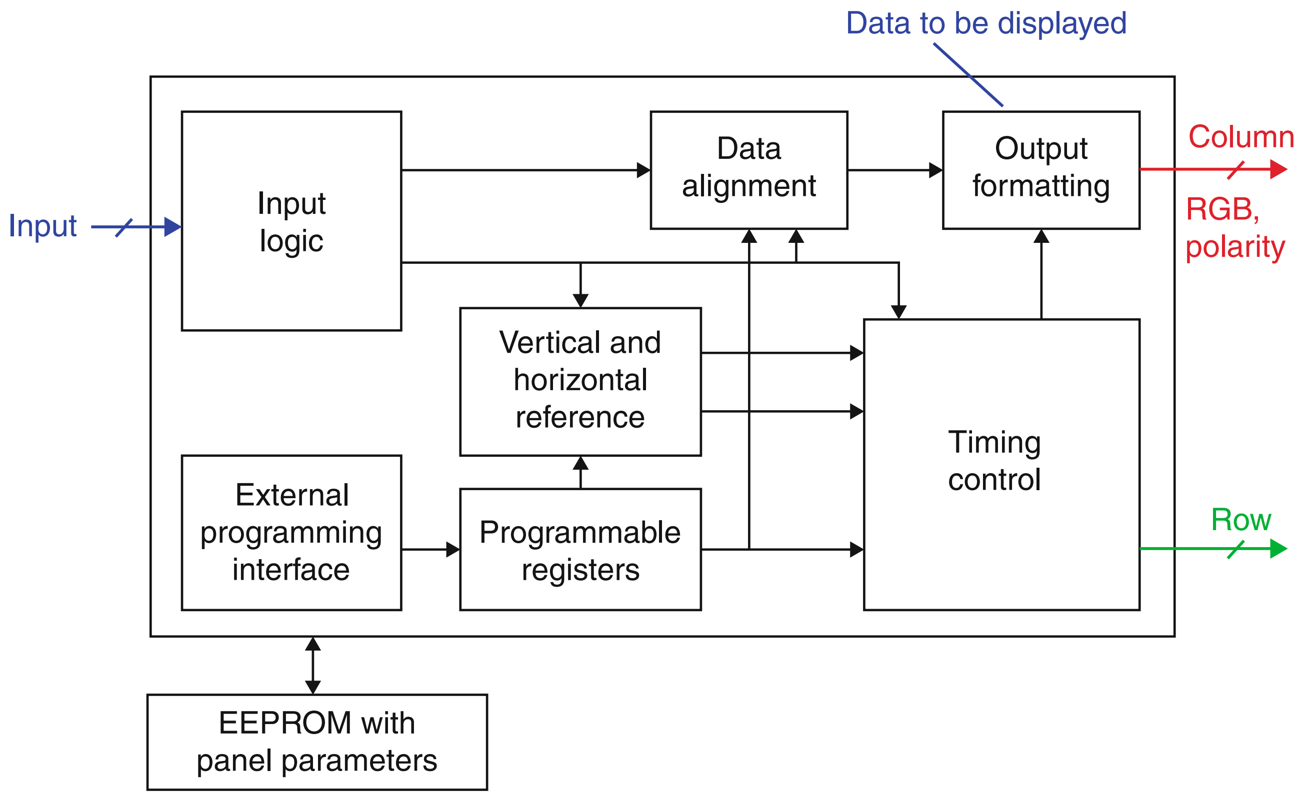
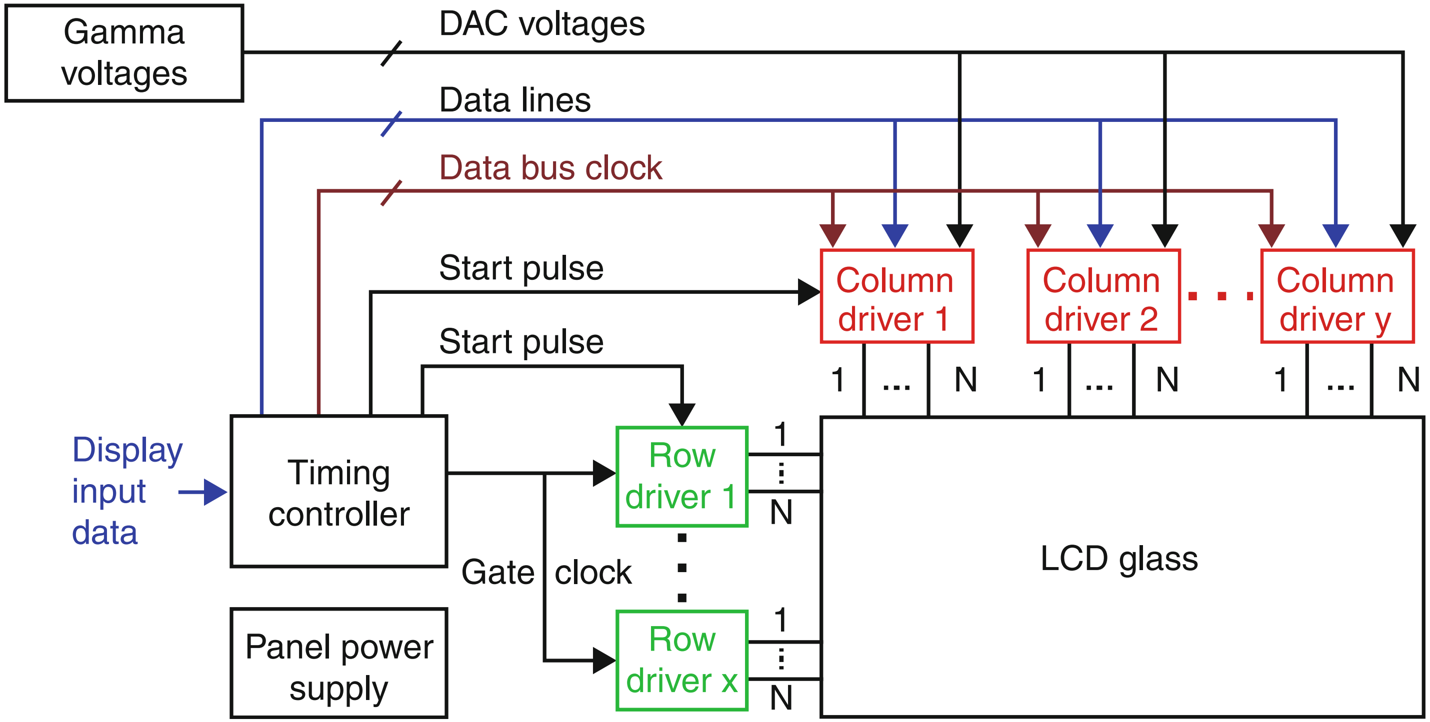
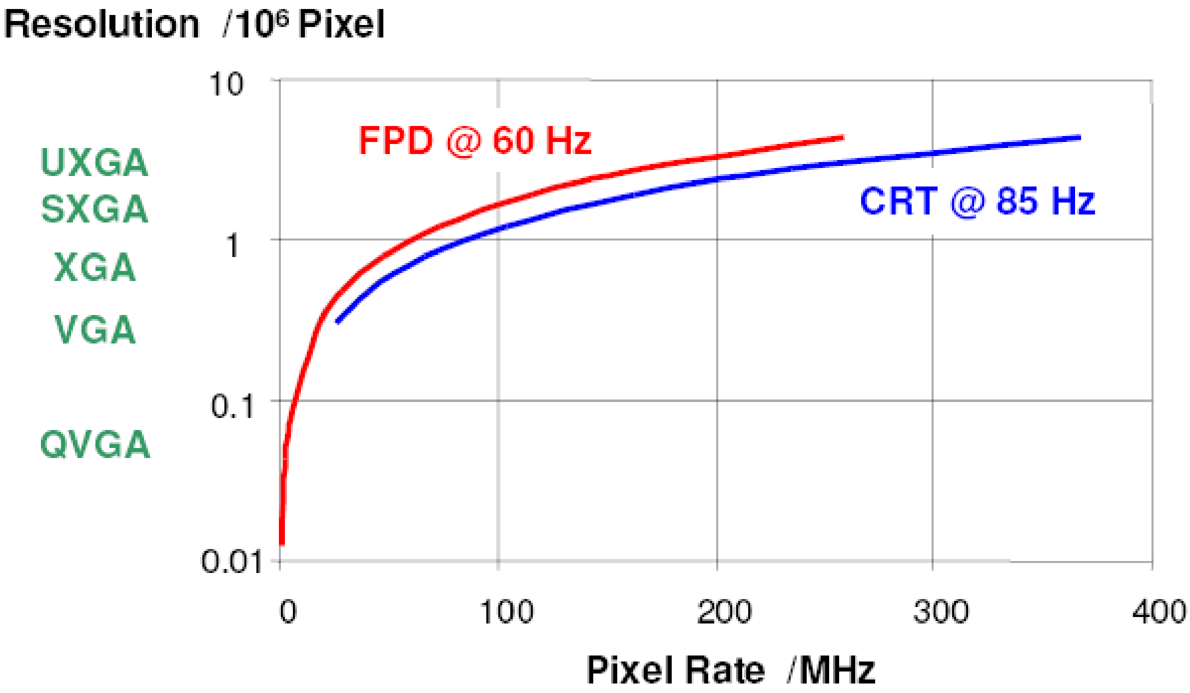


Fig. 4 Simplified block diagram of an LCD Timing Controller with its inputs and outputs

Panel Electronics



Data Rates



Pixel frequency	= Resolution x Frame frequency	(limit for parallel interfacing)
Data rate	= Pixel frequency x RGB x Colour depth	(limit for serial interfacing)

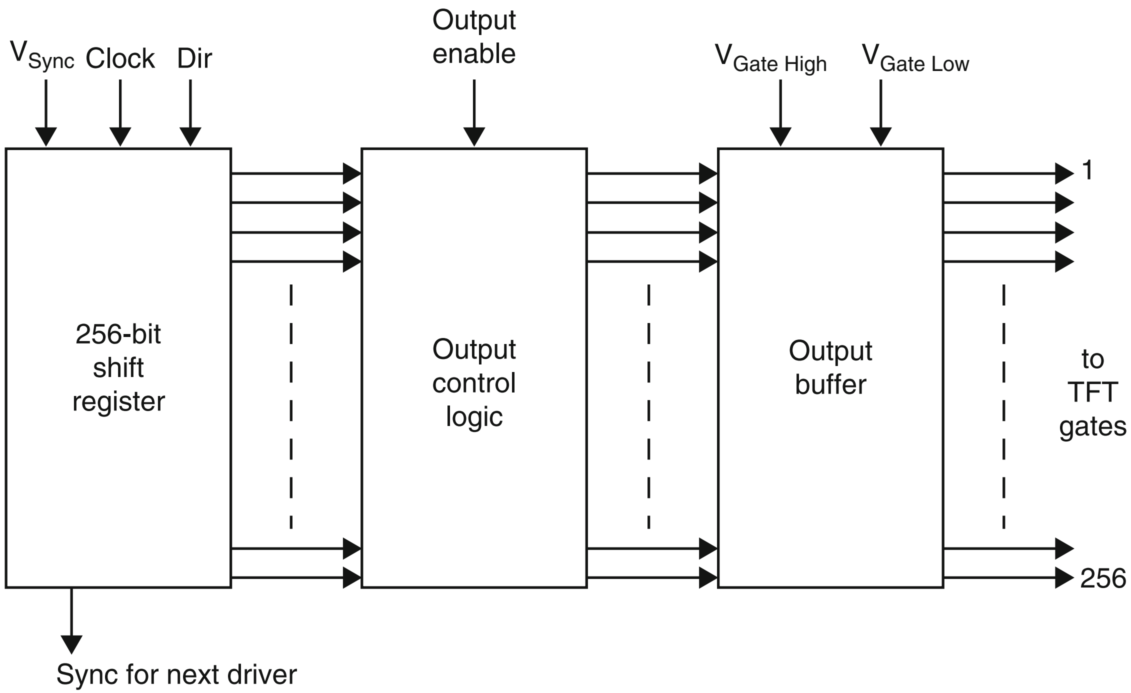
Row Driver and Timing

Shift register passes token

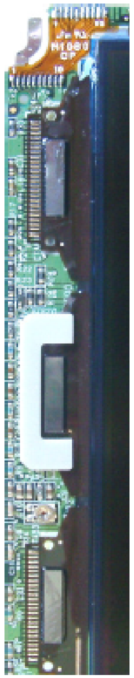
Token determines which row is active

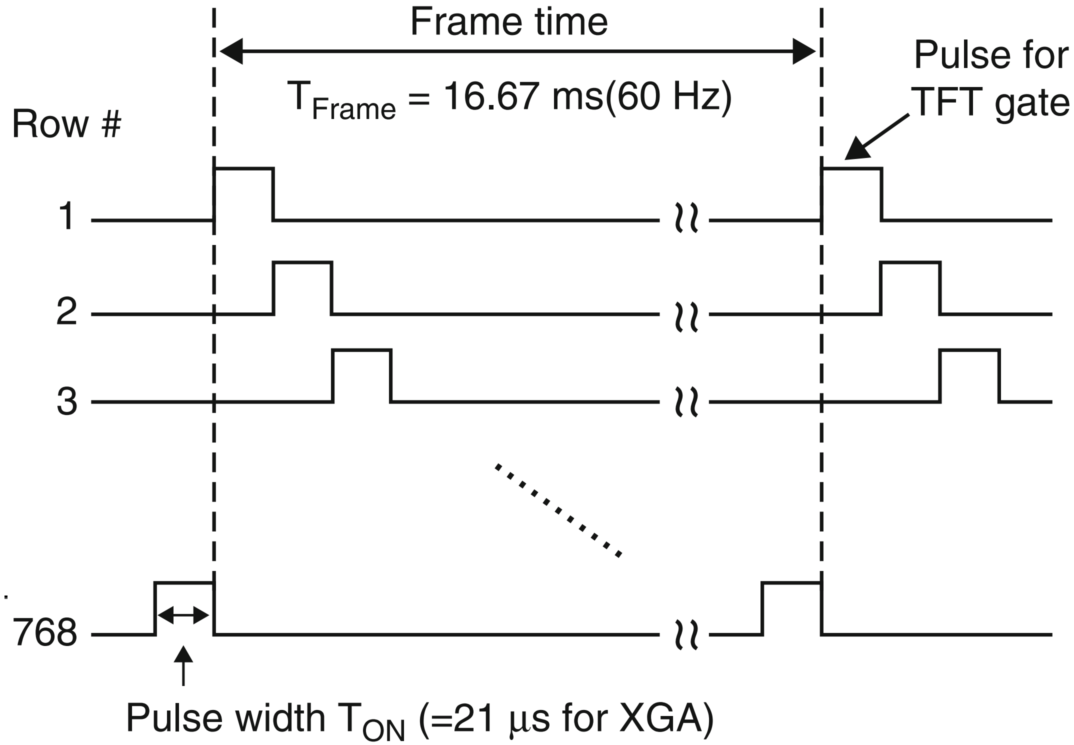
Dir sets scan direction

Output enable cuts gate voltage before next line to prevent cross-talk

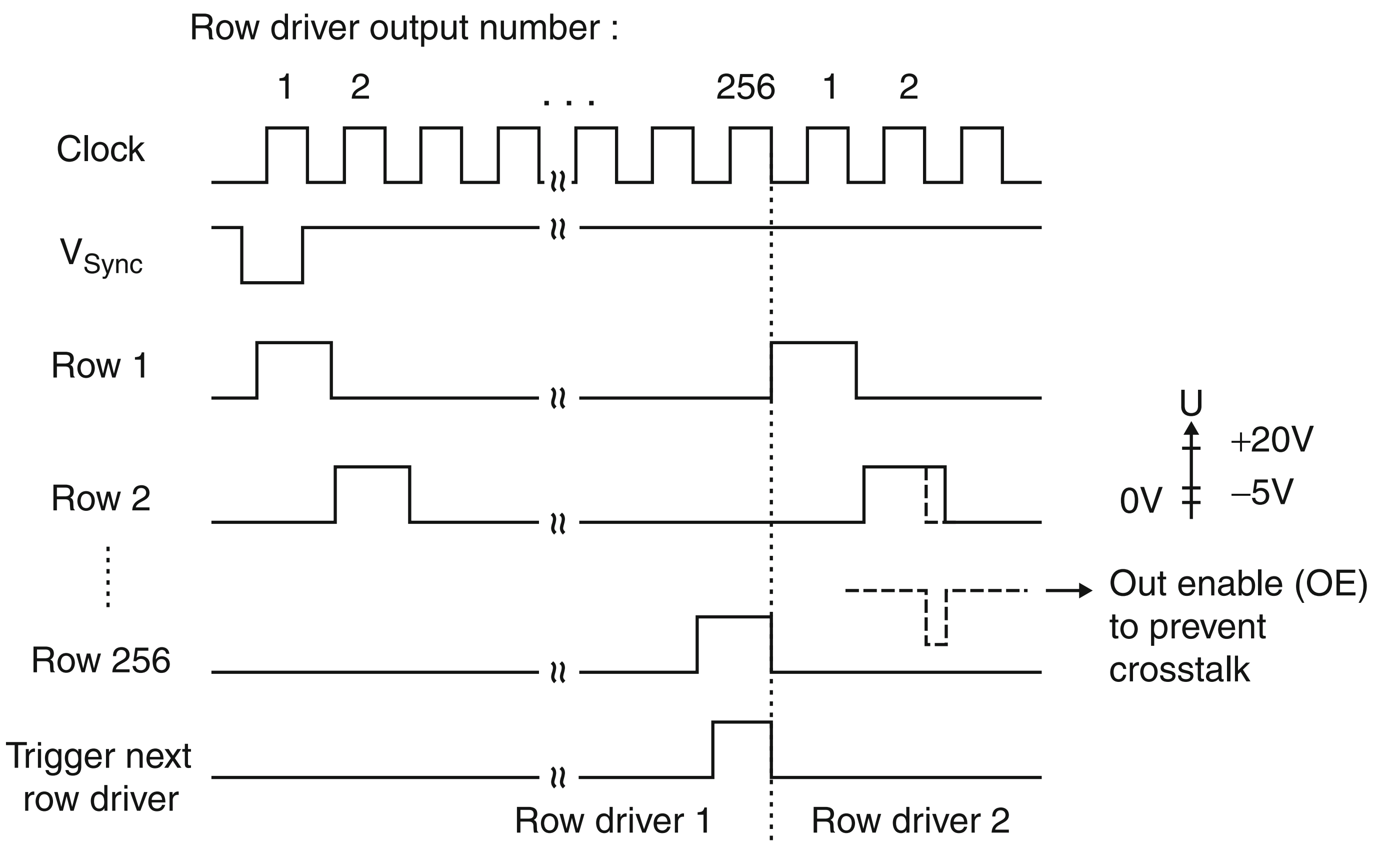


Row Driver Timing Diagram





Row Driver Timing Diagram



Example Column Driver

Example shown is

- Digital in, analog out

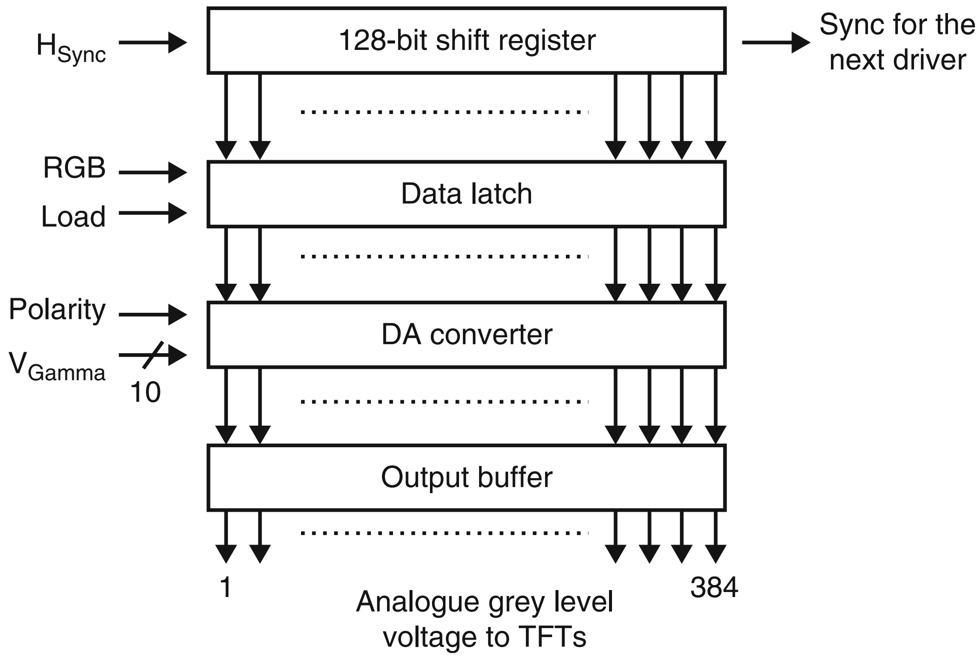
Could also be

- Digital in, digital out
- Analog in, analog out

Polarity for inversion

V_{gamma} for EO TF

Clocks etc not shown



Column driver timing diagram

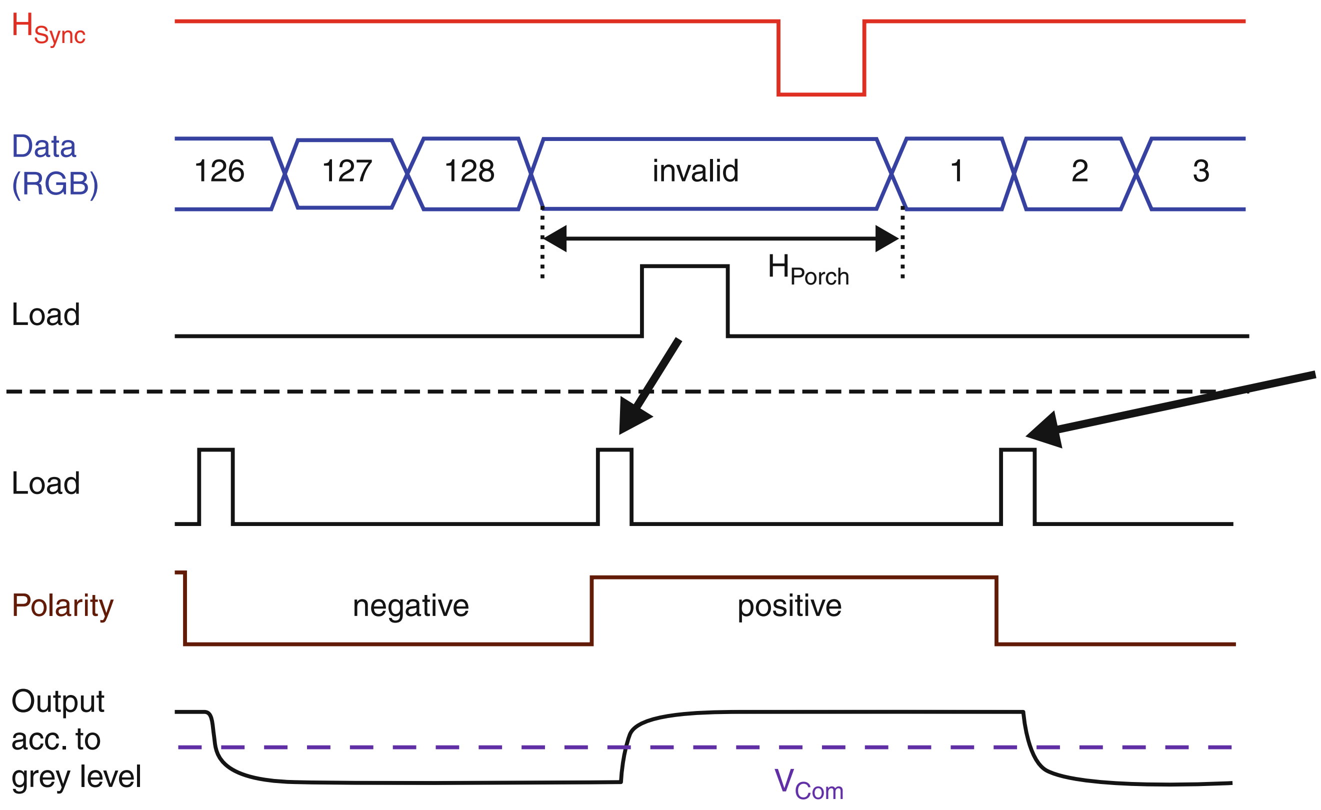
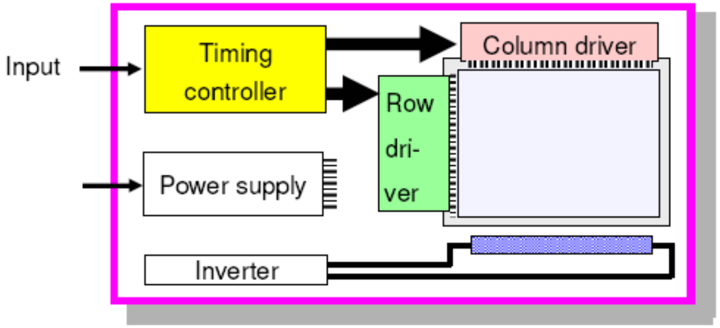


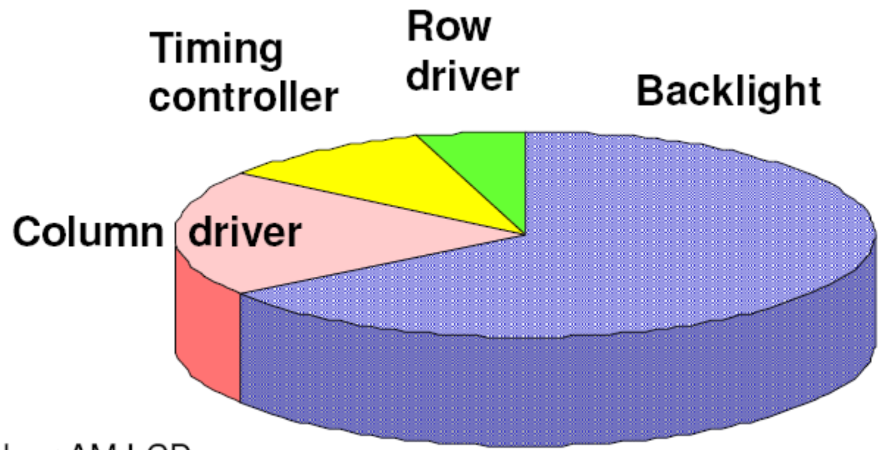
Fig. 11 Typical timing diagram (clock and some control signals omitted) of an XGA AMLCD column driver

Power Budget



LCD module

Electronics draw ~ 1/3
of total power consumption !



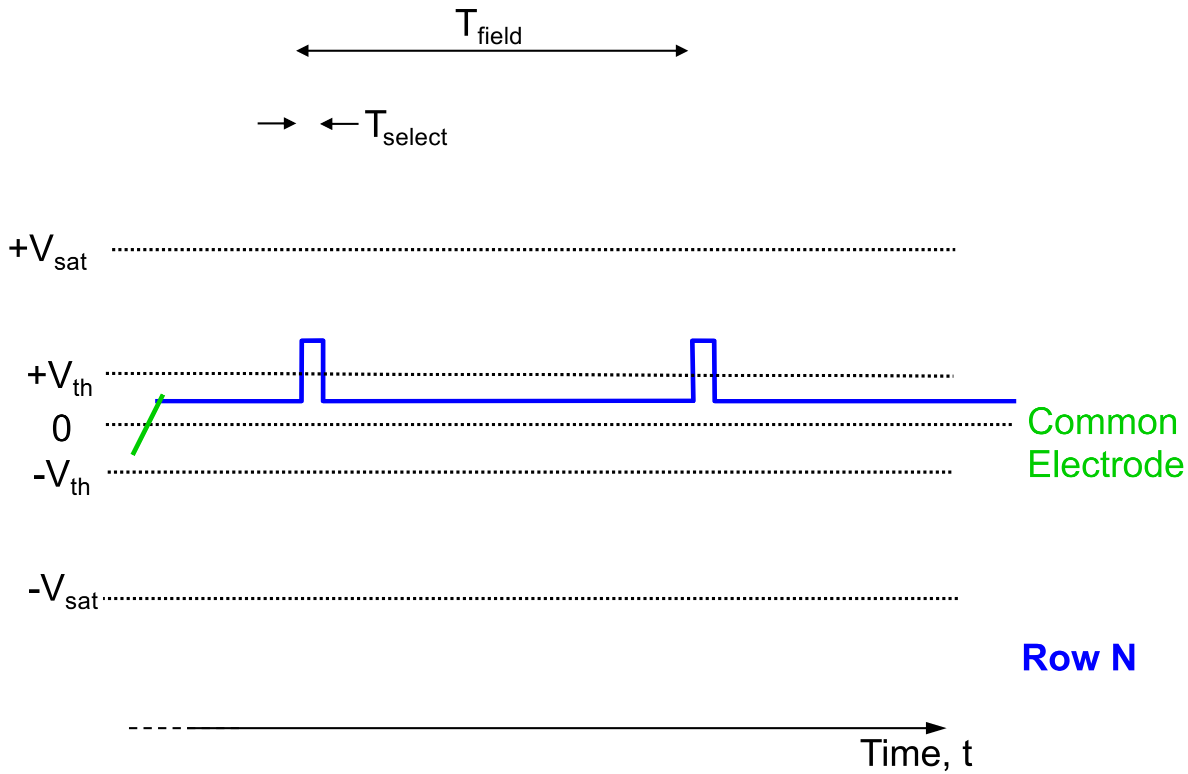
Example for 10.4" VGA Colour AM LCD

Row/Column Waveforms

Voltage levels of the LC & Common Electrode

Row/Column Waveforms

Consider Nth row



Row/Column Waveforms

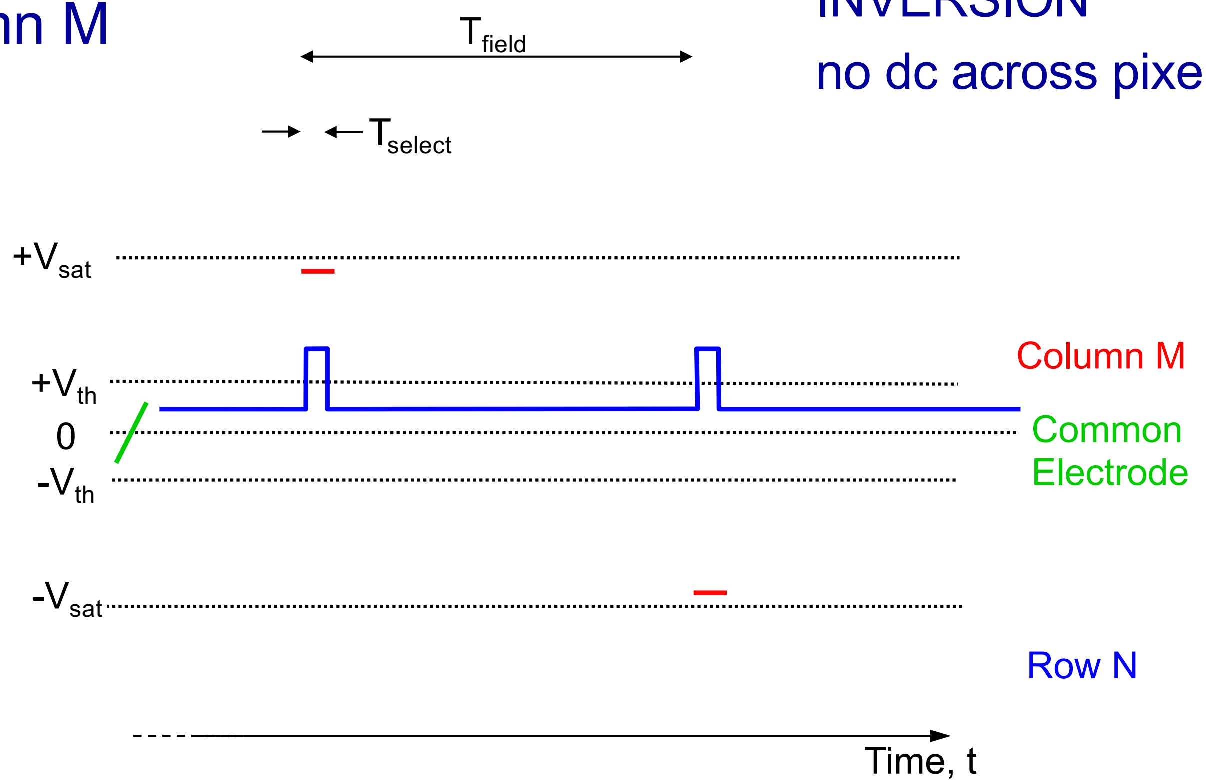
Apply voltage to

Column M

+ve & -ve voltage

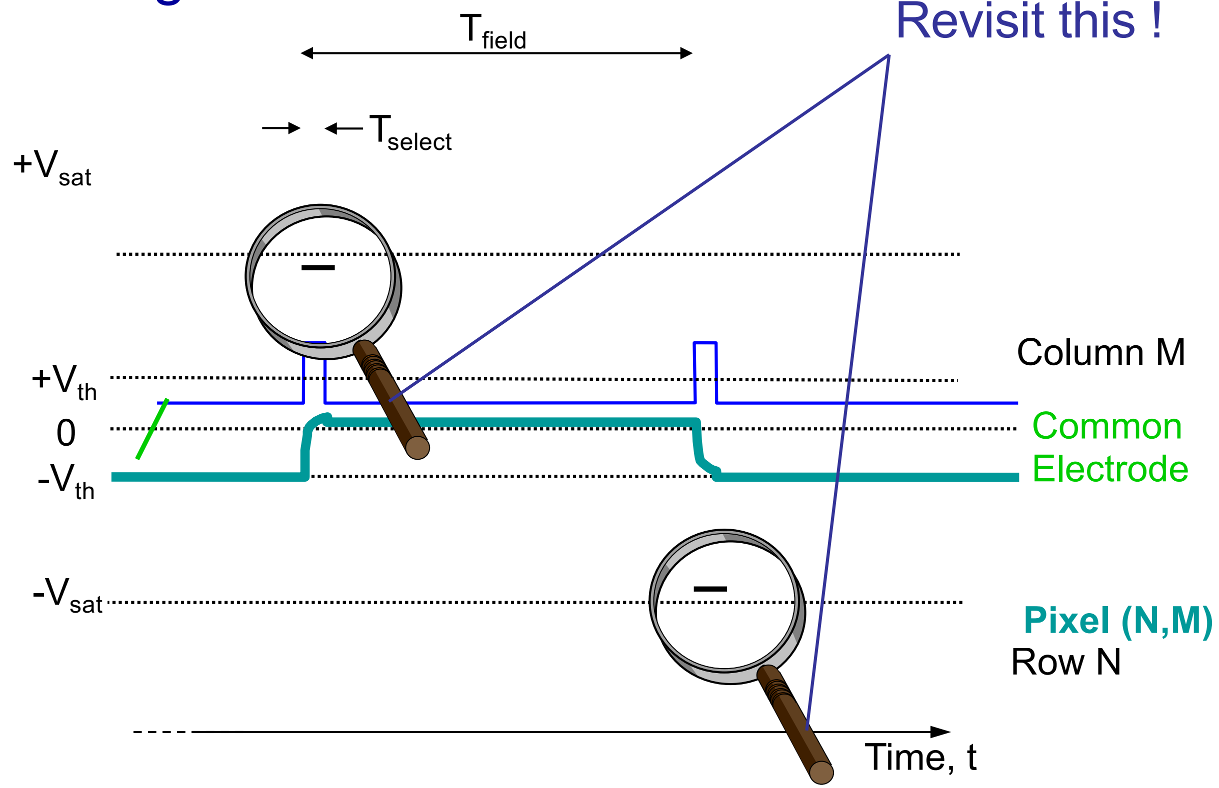
INVERSION

no dc across pixel

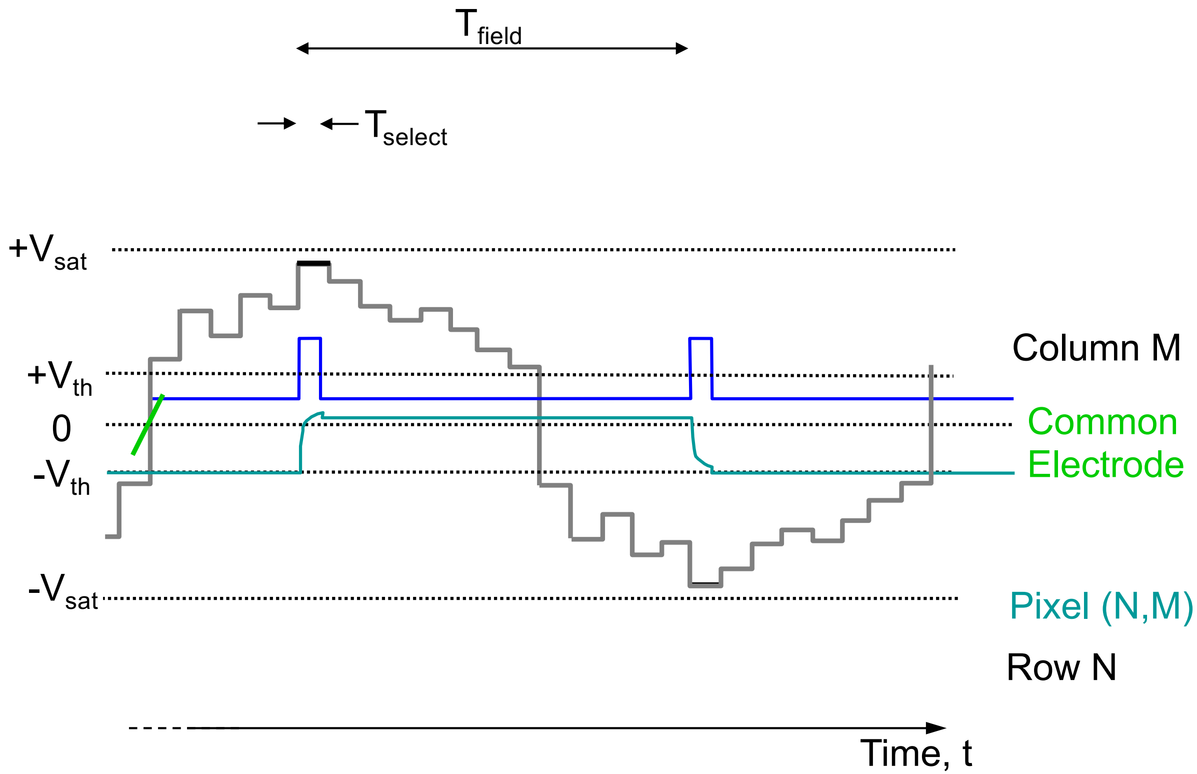


Row/Column Waveforms

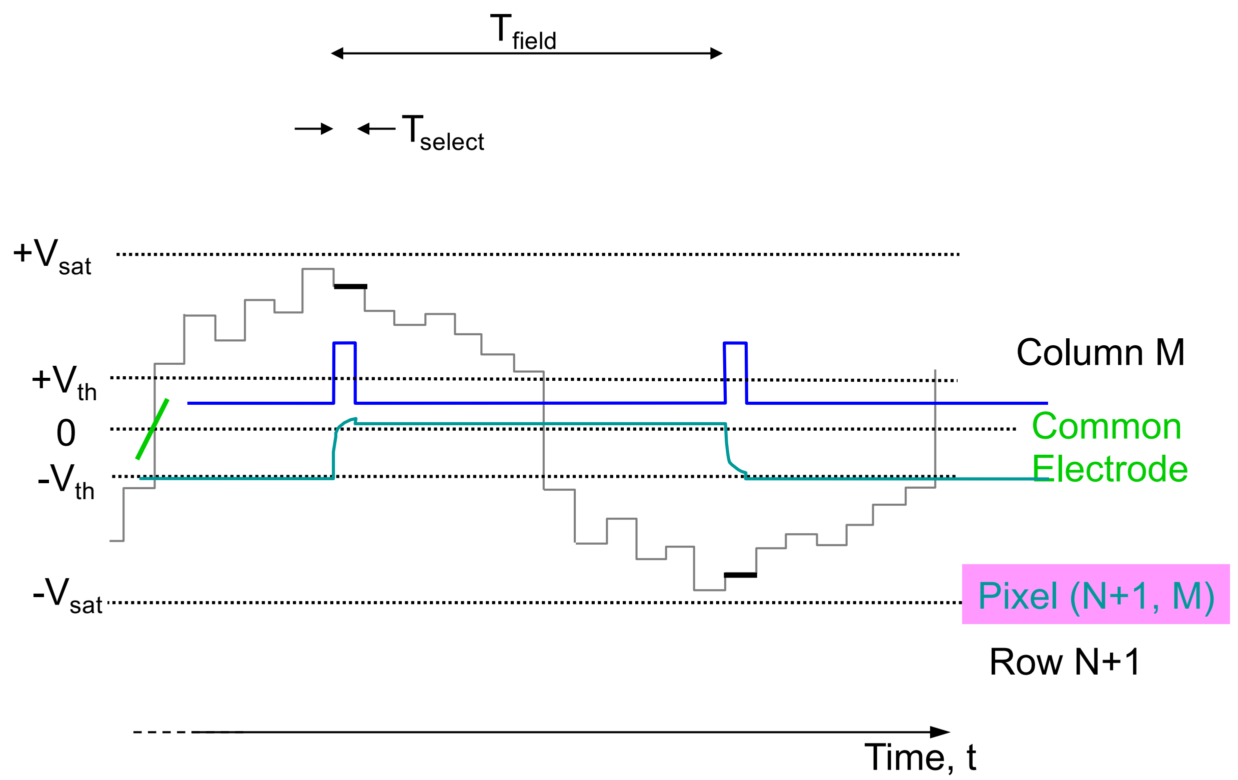
Pixel Voltage



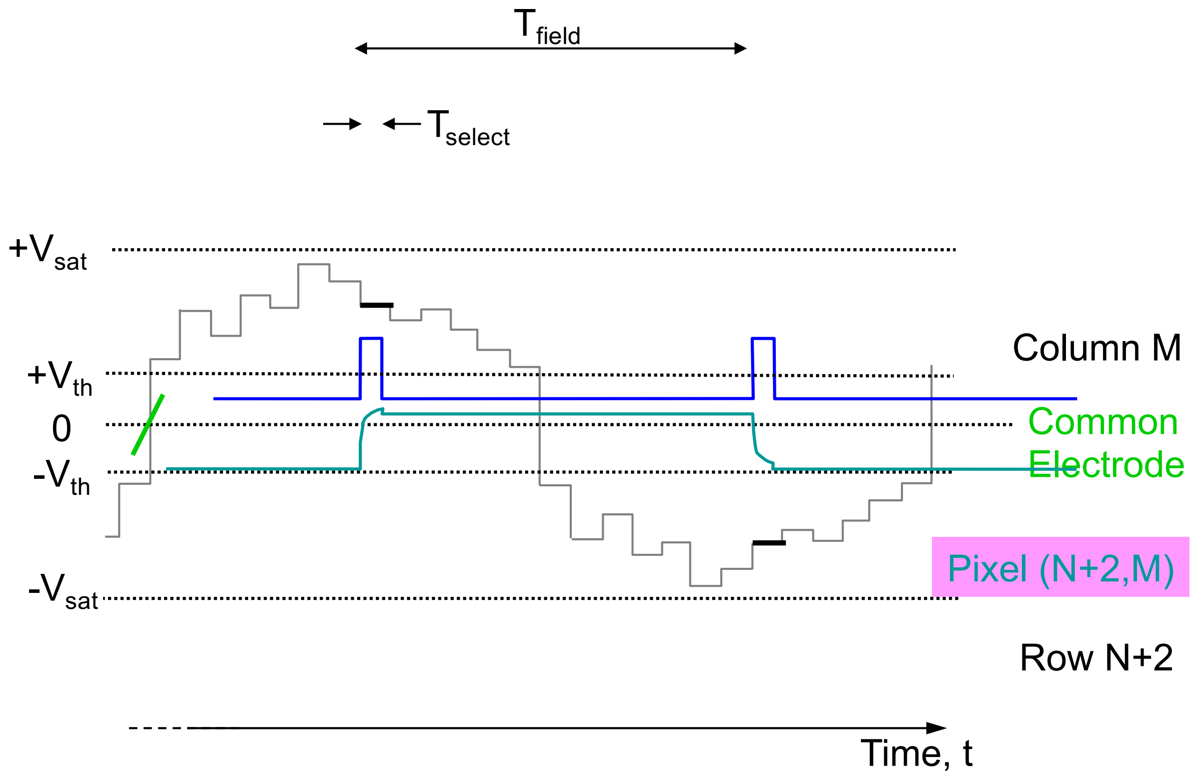
Row/Column Waveforms



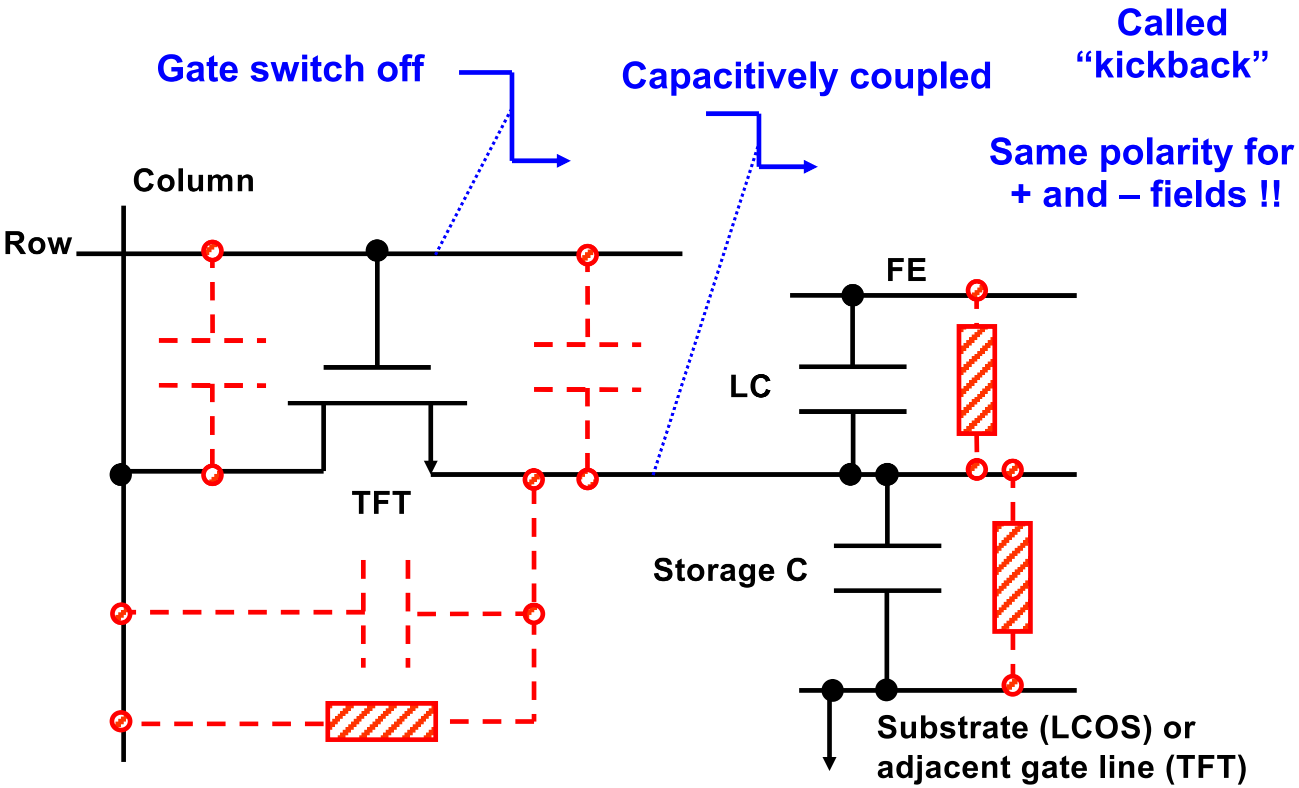
Row/Column Waveforms



Row/Column Waveforms

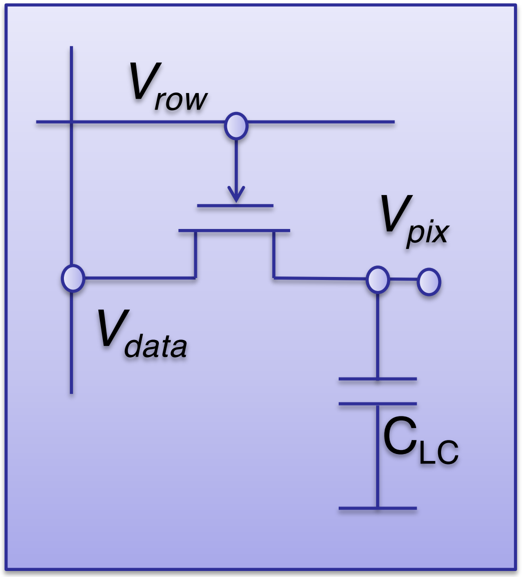


1xTFT, 1xC pixel – circuit schematic



Black / solid is designed-in"   Red / dashed is "parasitic"

Kickback – the issue



TFT

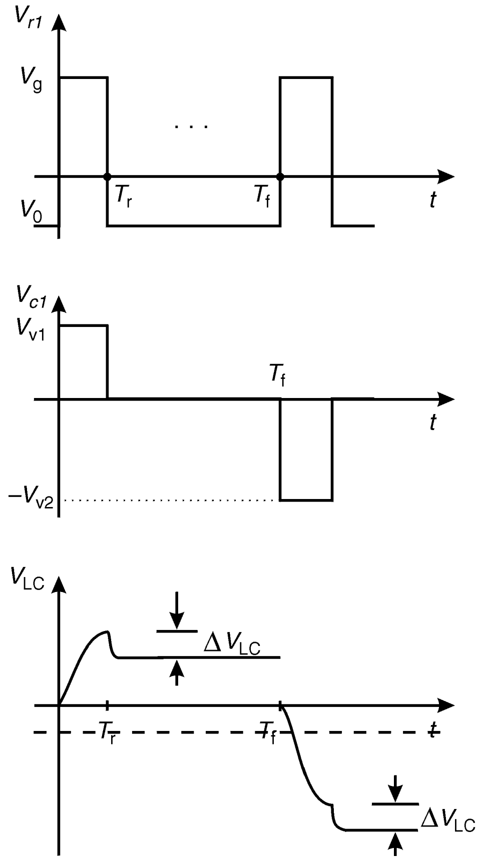


Figure 14.5 The gate impulses and their effect on the pixel voltage V_p

Kickback – the problem

Cause

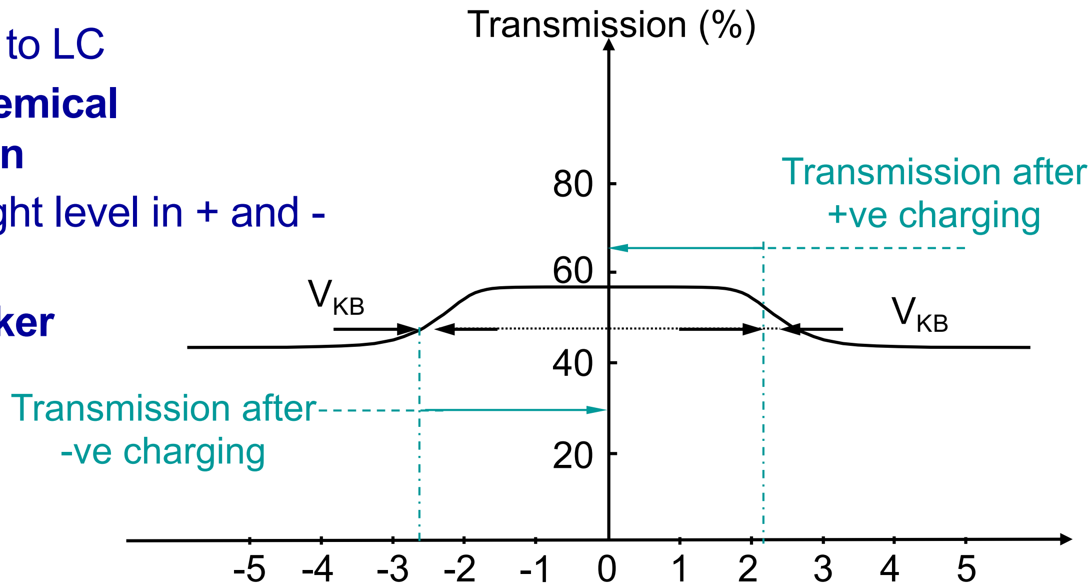
- Gate drain overlap capacitance
- Gate turn-off edge

Effects

Asymmetry of + and – field drive voltages

- Net d.c. signal to LC
  - **Electro-chemical degradation**
- Inequality of light level in + and - fields
  - **Visible flicker**

Exaggerated !

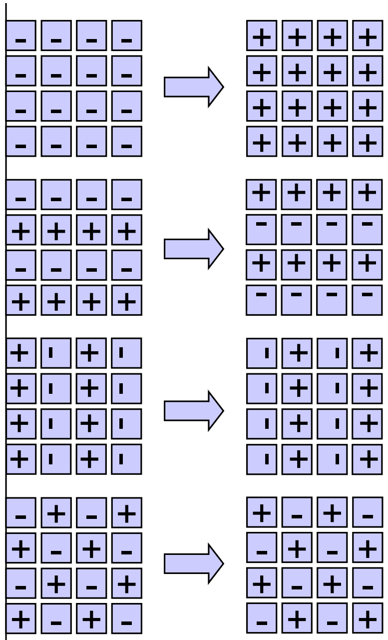


Kickback - solution

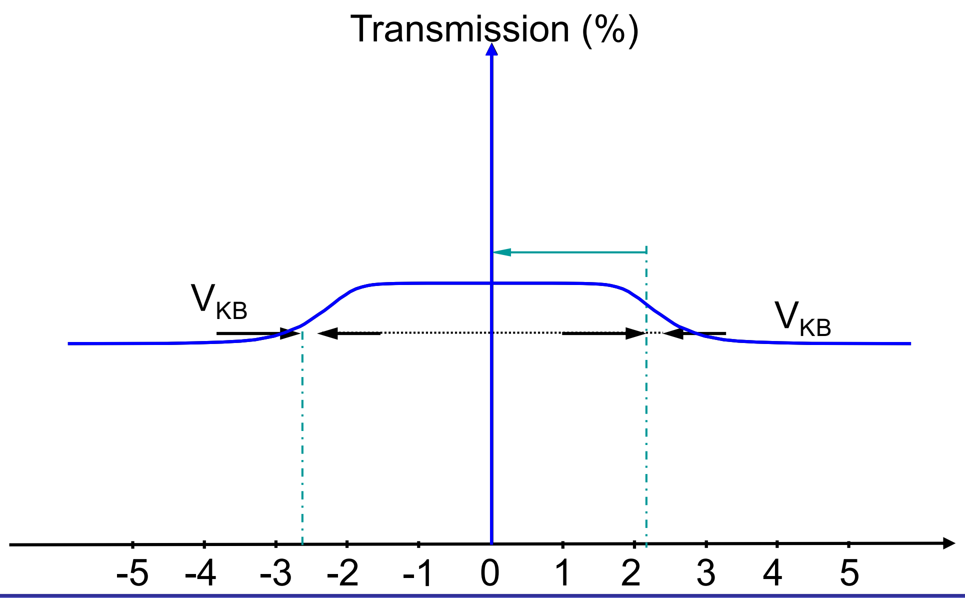
Improvements

Bias the common electrode to re-balance the symmetry

- DC balance not by field but by row, column or pixel



Exaggerated !



External Sources of Information

Handbook of Visual Display Technology **3rd Edition 2020**

https://link.springer.com/referencework/10.1007/978-3-642-35947-7

Not 1st edition 2012
Not 2nd edition 2016

Part X Fundamentals of Driving

Active Matrix Driving *Blankenbach*

Acknowledgement – some Figures taken from the above source

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Chapter 9 Advances in Mobile Display Driver Electronics

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