Depletion and enhancement mode InP high electron mobility transistors fabricated by a dry gate recess process

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Abstract

We report depletion and enhancement mode InP high electron mobility transistors (HEMTs) fabricated using CH_4/H_2 selective dry etch gate recess process. Under the etching conditions developed, the process has a $In_{0.7}Ga_{0.3}As$ to $In_{0.52}Al_{0.48}As$ selectivity of 130. The dc threshold voltages of the devices fabricated in this way increase from –1.3V to 0.1V as a function of dry etch time, with an extrinsic transconductance of 520mS/mm in the depletion mode and 800mS/mm in enhancement mode. The devices exhibit an extrapolated cut-off frequencies of 150GHz. This work demonstrates the potential of the use of dry etching as a gate recess technology for the future development of high frequency InP-based circuits.

Introduction

Depletion mode high electron mobility transistors (HEMTs) based in lattice matched InP material have been under intense investigation for the past years. These transistors possess superior device performance compared to their III-V counter parts due to the large conduction band offset at the heterointerface; the small electron effective mass and the high electron effective velocity in the InGaAs channel. On the other hand, for future high speed digital circuits applications, enhancement mode devices are essential building blocks because of their simple implementation and low power dissipation. Few successful efforts have been reported in the fabrication of such transistors operating in the enhancement mode regime [1-4]. However, such methods require buried-gate structures that are difficult to implement in applications. In this paper, we present a dry gate recess method using CH_4/H_2 that has been found to shift the threshold voltage of devices, and hence, from depletion to enhancement mode. This technique is commensurate with current processing technologies [5].

Experiments

The device and material structure are illustrated in figure 1. From top to bottom, the heterostructure consists of the following layers: a 10nm $5x10^{18}cm^{-3}$ Si-doped $In_{0.53}Ga_{0.47}As$ layer, 5nm undoped InGaAs, 20nm undoped $In_{0.52}Al_{0.48}As$ Schottky layer, Si pulsed doped to 6×10^{12} cm^{-2}, 5nm undoped InAlAs spacer, 10nm undoped pseudomorphic $In_{0.7}Ga_{0.3}As$ channel, 20nm undoped $In_{0.53}Ga_{0.47}As$ layer, 250nm InAlAs buffer, all on a semi-insulating InP substrate. This material has a room temperature mobility of $13,000cm^2/Vs$ and a carrier density of $3.2 \times 10^{12}cm^{-2}$. Dry gate recessing of the top highly doped InGaAs layer to form HEMT devices has been performed in

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an Integrated Plasma Limited dry etcher equipped with a load lock. A CH_4/H_2 gas mixture, with a ratio of 7.5sccm:82.5sccm, 36mTorr pressure, 0.079W/cm^2 power density, resulting in -190V dc bias has been employed. Under these conditions, an $In_{0.53}Ga_{0.47}As$ etch rate of 8nm/min. and a selectivity of $In_{0.52}Al_{0.48}As$ to $In_{0.53}Ga_{0.47}As$ of 130 have been achieved [6]. Microwave transistors with 0.2μm gate lengths have been fabricated using mix and match electron beam and optical lithography. Ohmic contacts have optimised contact resistance of 0.1ohm-mm. Gates of T-shape is formed by depositing Ti/Au on a tri-level resist layer before lift-off. Figure 2 shows a mushroom gate on top of the InP heterostructure. Details of the device fabrication procedure have been described elsewhere [7]. In the present experiments, devices have been processed with dry gate recess duration ranging between 3 minutes and 9 minutes. All devices have been subjected to a short 10s wet etch to remove an Al and In rich layer prior to gate deposition [7]. dc measurements of the HEMTs have been performed using a Keithley test set while microwave measurements up to 50GHz are taken using a HP 8510C network analyser.

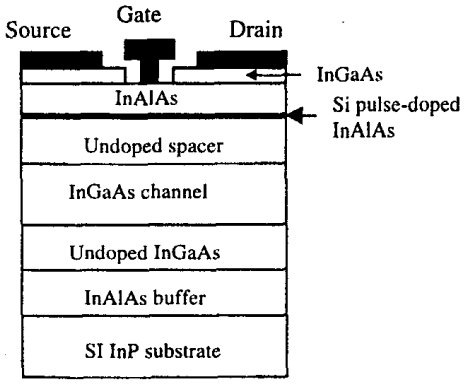

Figure 1 Device and material structure (not to scale)

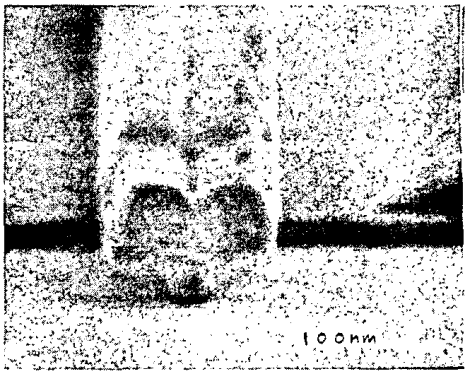

Figure 2 Scanning electron micrograph of a 0.2μm gate on InP heterostructure

Results and Discussion

Using the fabrication technology described above, changes in the dc parameters as a function of dry etch time have been observed. Table 1 shows a summary of the dc characteristics of the HEMTs.

Dry etch time	g_{mmax} (mS/mm)	I_{dss} (mA/mm)	V_{th} (V)
3mins.	520	604	-1.3
6mins.	650	135	-0.7
8mins.	740	48	-0.2
9mins.	800	0	0.1

Table 1 Summary of dc characteristics of CH_4/H_2 gate recessed InP HEMT transistors.

In particular, we observe a systematic shift to more positive threshold voltages accompanied by a decrease in the saturated drain current and an increase in the measured g_{mmax}. After 9 minutes etching, the threshold voltage is 0.1V which results in an enhancement mode device with an extrinsic transconductance of 800mS/mm. Figures 3 and 4 show the typical transfer and output characteristics of such a device.

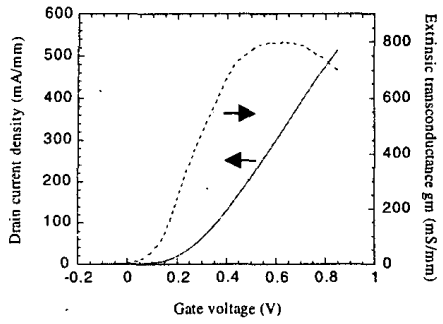

Figure 3 dc transfer characteristics of InP HEMTs after dry etching for 9 minutes

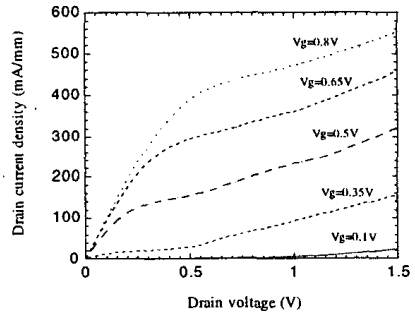

Figure 4 dc output characteristics of InP HEMTs after dry etching for 9 minutes.

A shift in the dc characteristics as a function of dry (over)etch time has been reported previously [7]. But only with the present pulse-doped material are enhancement mode FETs demonstrated. This reflects the importance of tailoring device material design for the desired performance.

The observation of depletion and enhancement device operation in the present InP heterostructure material may be explained by the accurate control of the effective gate to channel distance. Two possible mechanisms may be responsible for the observed shift of the dc parameters: i) etch-induced effects without physically removing material; ii) overetching physically removes material at a controlled rate.

It is well known that low energy ion bombardment induces depletion in the underlying unetched material, the size of which changes as a function of dry etch time [8]. The existence of such a layer may alter the band structure underneath the gate significantly. This could be a primary cause for the shift in the threshold voltage of our HEMT devices. It is possible that the presence of dry etch-induced effects allows the effective positioning of the gate extremely close to the channel, without destroying the room temperature properties of the two dimensional electron gas, thus permitting the fabrication of enhancement devices with very high transconductance. Recent studies in the low frequency noise behaviour of similar dry gate recessed HEMTs reveal the possible existence of trap passivation under the gate area during etching [9], and a decrease in the source resistance of dry etched devices [10]. These effects were attributed to the cause of the improved low frequency noise behaviour compared to the wet etched devices. Such effects may be related to depletion. However, the detail mechanisms for etch-induced depletion effects remain unclear. Comparison of the source resistances measured from our depletion and enhancement mode devices did not reveal dramatic differences $\approx$ 0.8Ωmm. We note that the commonly observed "kink" in InP-based HEMTs [11] is evident in the output characteristics of our devices.

The possibility of physically removing the InAlAs because of the overetch time cannot be ruled out. However, with a selectivity of 130, this would happen at a phenomenally slow rate, and suggests the likelihood of the influence of etch-induced effects on the observed device parameter change.

Nonetheless, the ability to control device characteristics by varying the dry etch time has important implications in the fabrication and design of future high speed digital circuits.

A typical short circuit current gain of the enhancement mode devices is shown in figure 5. A cut-off frequency of 150GHz can be extrapolated which demonstrates the excellent performance of these devices at microwave frequencies.

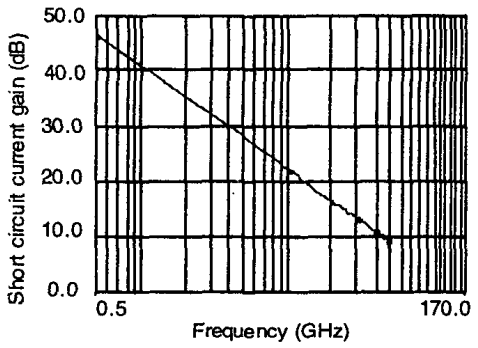

Figure 5 Short circuit current gain as a function of frequency for CH_4/H_2 gate recessed enhancement mode InP HEMTs

In summary, using CH_4/H_2 as a selective dry gate recess process, we have fabricated 0.2μm gate length depletion and enhancement mode InP HEMTs. The detailed mechanisms that cause the shift in dc characteristics of our devices are not well understood at present. Nevertheless, these devices exhibit excellent extrinsic transconductances from 520mS/mm to 800mS/mm and short circuit current gain cut-off frequencies of 150GHz.

Acknowledgements

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