



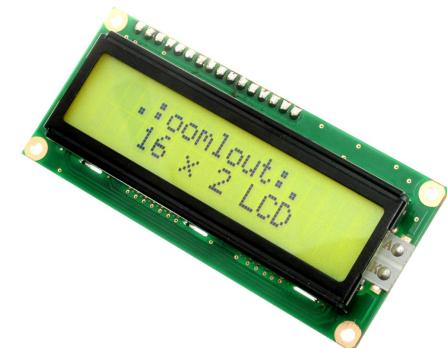
SECTION 1

ELECTRONIC INFORMATION

DISPLAYS - AN OVERVIEW

Electronic Display - Definition

Wikipedia. An electronic **display device** is an output device for presentation of information for visual or tactile reception, acquired, stored, or transmitted in various forms. When the input information is supplied as an electrical signal, the display is called *electronic display*.



www.answers.com

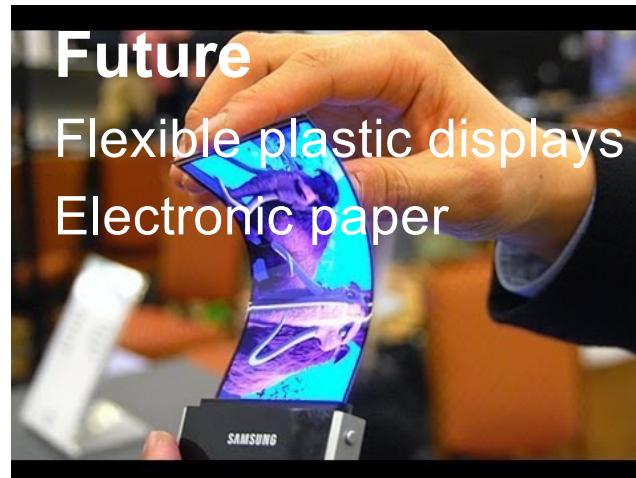
An electronic **display device** is an electronic component used to convert electric signals into visual imagery in real time suitable for direct interpretation by a human operator

Display paradigms

Historical
CRT = Cube



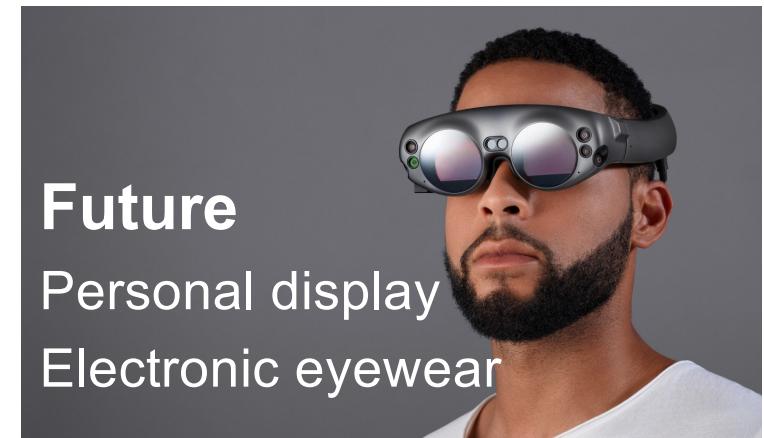
Future
Flexible plastic displays
Electronic paper



Current
LCD, OLED
Flat, thin, mostly rigid



Future
Personal display
Electronic eyewear



Three questions for you ...

My assertions

Today, in 2022, electronic displays are everywhere

They have permeated all parts of our lives

We could not function (so well / at all*) without them

My questions

Since waking up this morning

How many electronic display screens have you looked at ?

How many times have you looked at an electronic display ?

How many minutes have you spent looking ?

* Delete as appropriate

Ubiquity of Electronic Displays

Electronic displays are everywhere

- Home
- Office
- Car, bus
- Person
- Pub
- Railway station, airport

Content is continuously becoming more

- Complex
- Colourful
- Video-oriented
- Engaging



Goal of advanced electronic displays

Definition of the ideal electronic display

- An electronic display on which a viewed image is indistinguishable from reality

Not possible!

Goal of today's advanced displays

- To come as close as possible to the ideal display given practical restrictions
- Size, weight, power consumption, cost etc

*Thought
Experiment!*

A fundamental issue

The real world is
3-DIMENSIONAL
CONTINUOUS &
UNLIMITED in
SPACE
TIME
COLOR
BRIGHTNESS

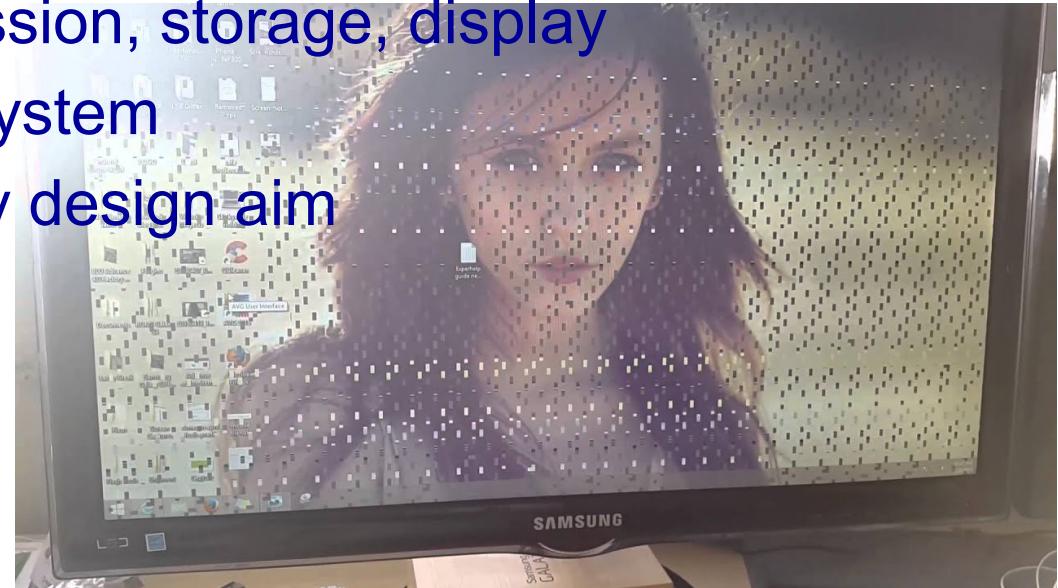
Look around you!

Almost all
Electronic Displays are
PLANAR (2-D)
DISCRETE &
LIMITED in
SPACE (pixels)
TIME (frames)
COLOR (shades)
BRIGHTNESS (grey levels)

Visual artifacts

Definition - artefacts are unwanted visible effects that distort faithful reproduction, reduce realism or otherwise detract from the users enjoyment of the content being viewed

- **artefacts** can derive from any part (or combination of parts) of the system – capture, transmission, storage, display
- **artefacts** exist in every display system
- Minimization of **artefacts** is a key design aim



Display System Functional Blocks

Generate / receive Image Data



Store Image Data

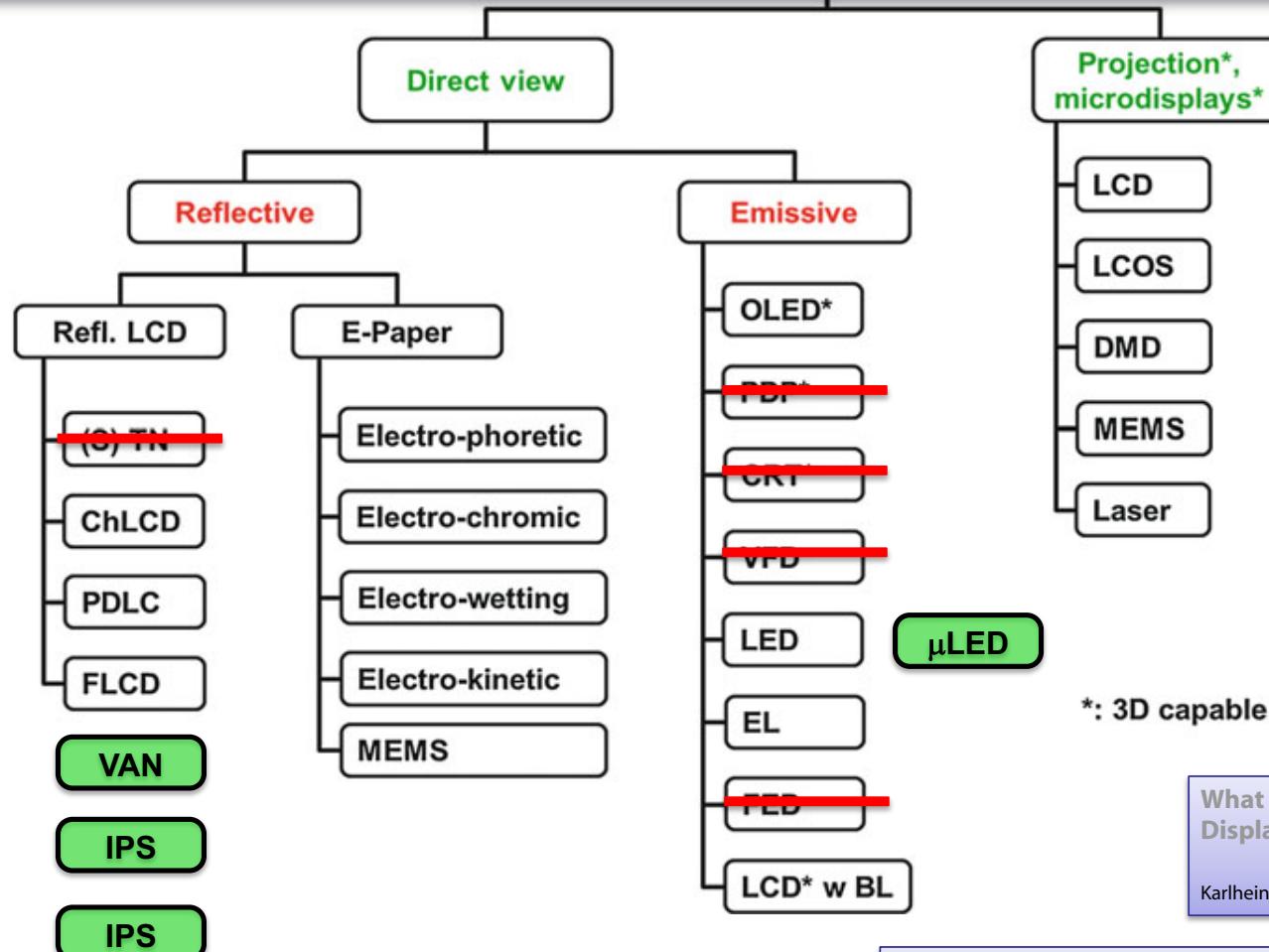
Transmit Image Signal

Convert Image Signal

Display Image Signal



Display technologies

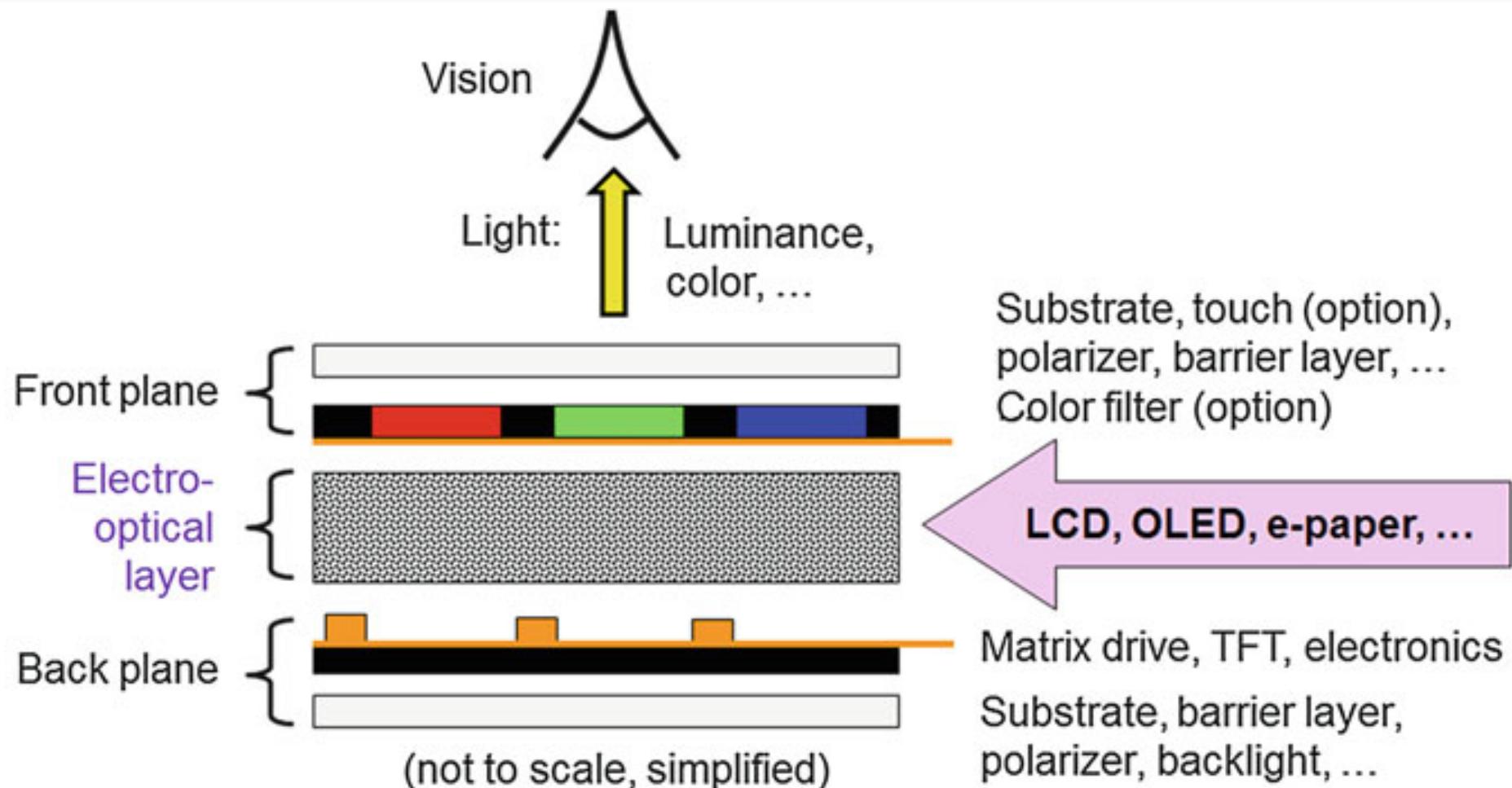


What is a Display? An Introduction to Visual Displays and Display Systems

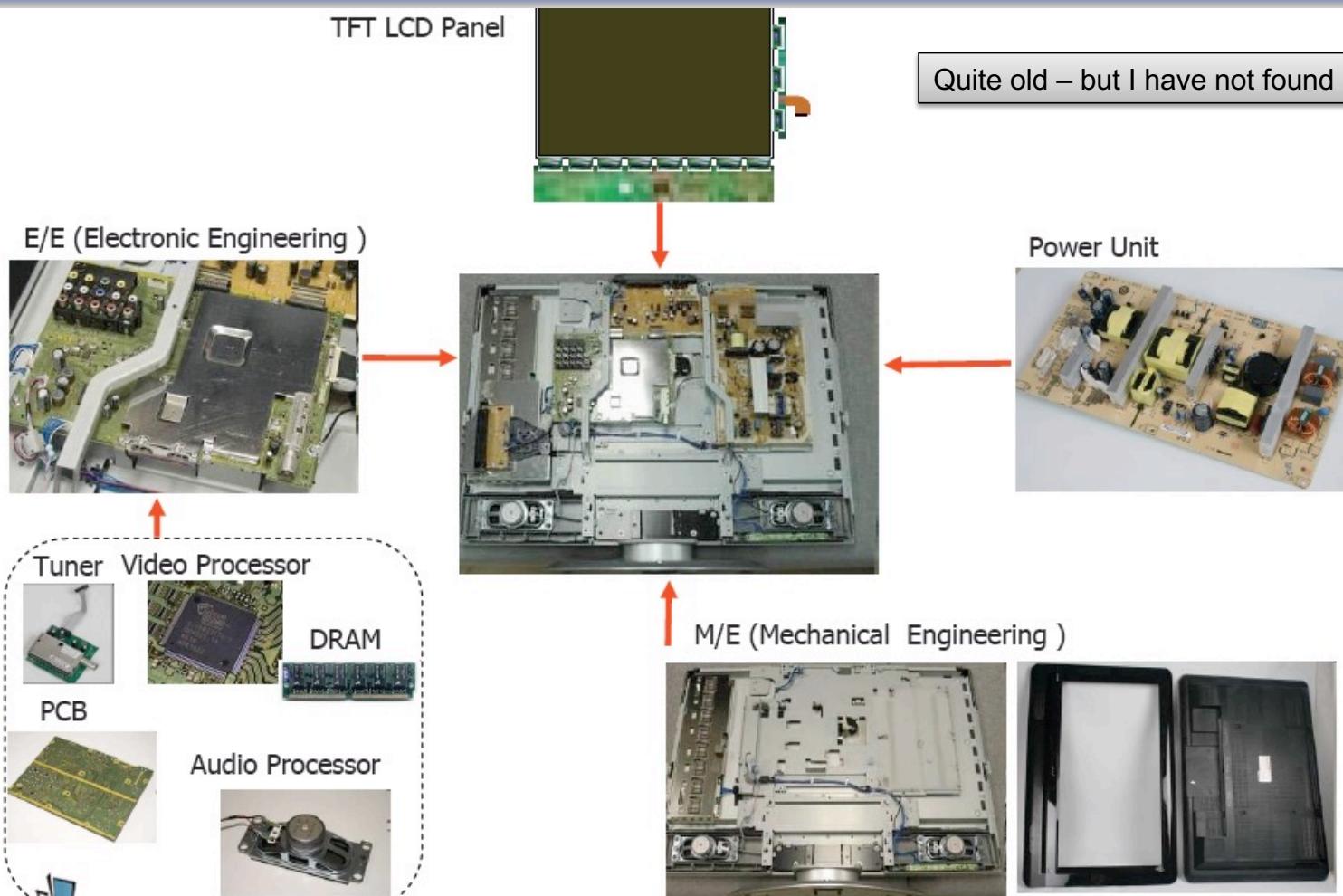
Karlheinz Blankenbach

Suggestion - Go home and look up all the acronyms

Display Panel - Component Parts



TFT LCD TV breakdown



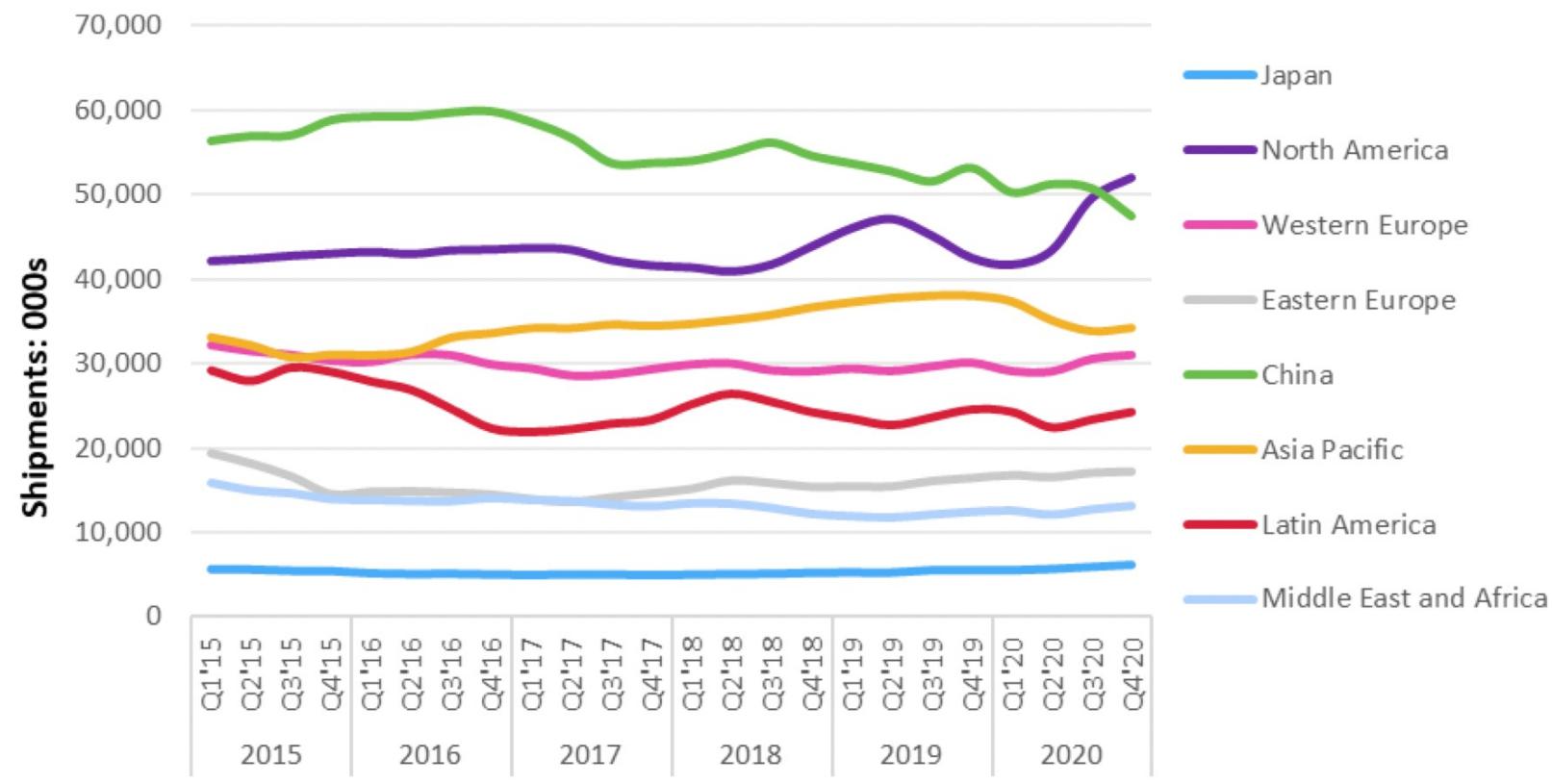
Domestic flat panel tv

LCD and OLED!
LED?



Domestic Flat Panel tv Market

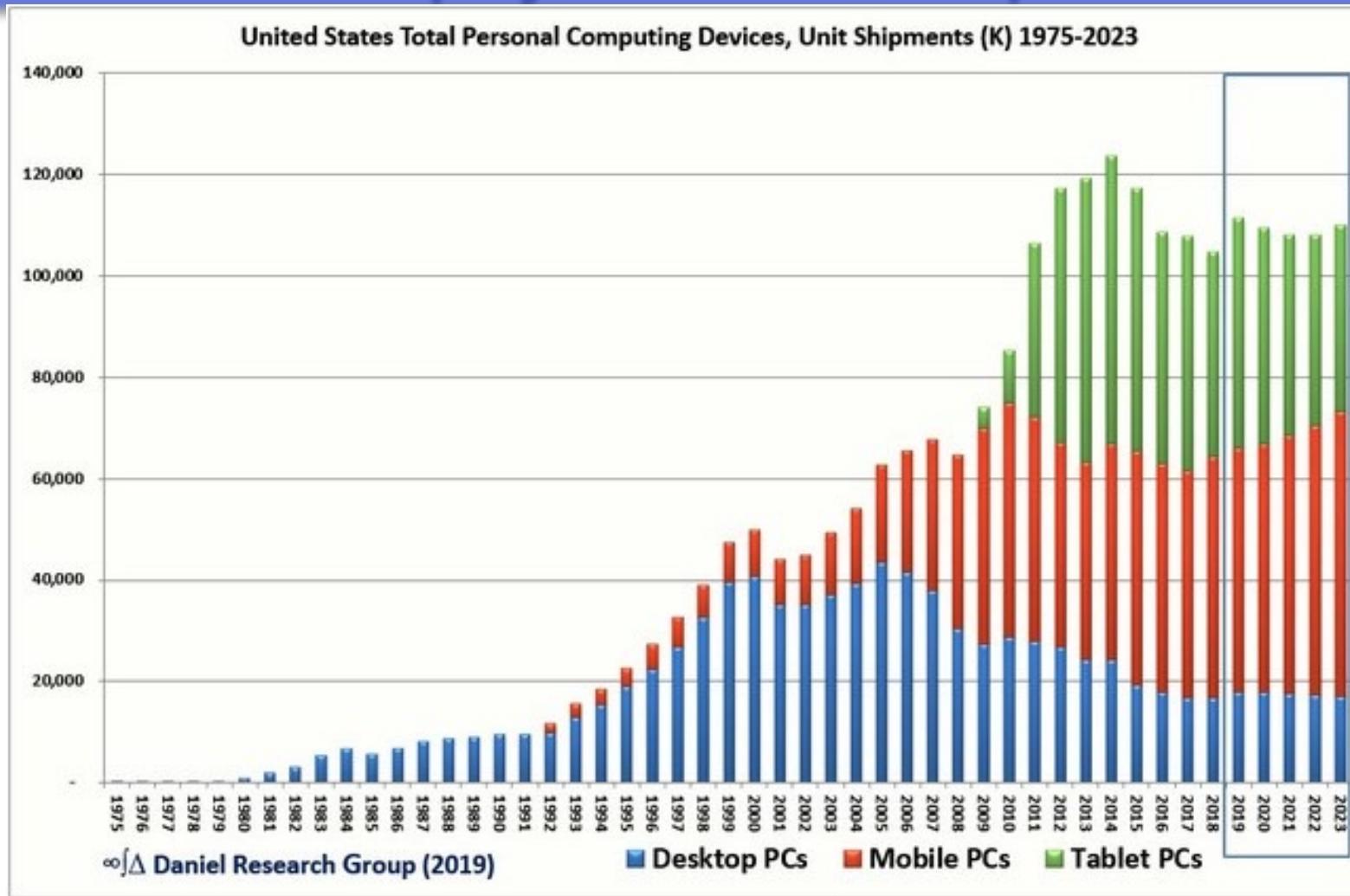
TV shipment history (rolling four quarters)



Source: Omdia

© 2021 Omdia

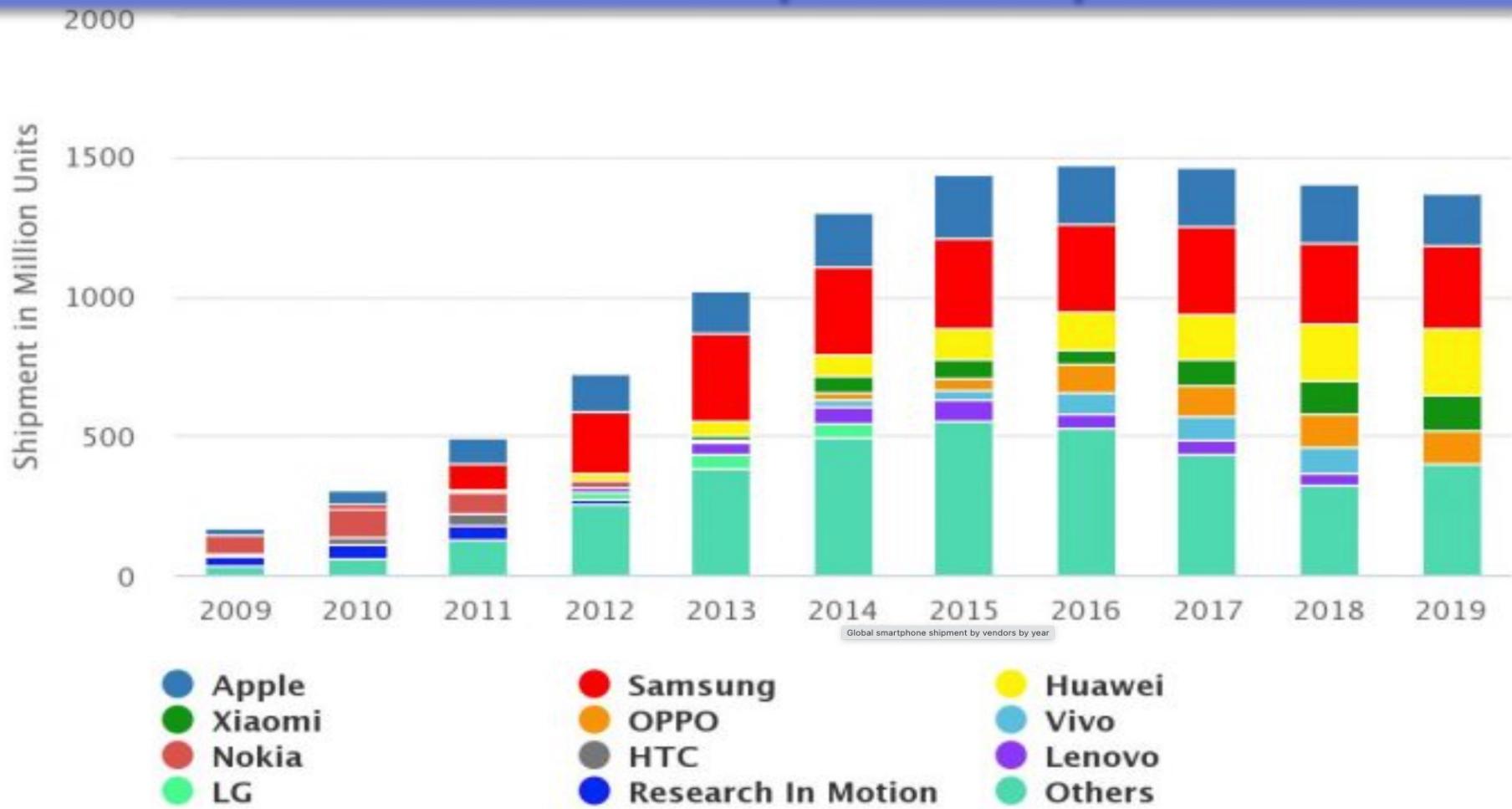
Display Markets - Computer



Mobile phones, GPS, Games



Worldwide Smartphone Shipments



© Dazeinfo / Data Source: IDC

WW SM TFT LCD ASP Trend

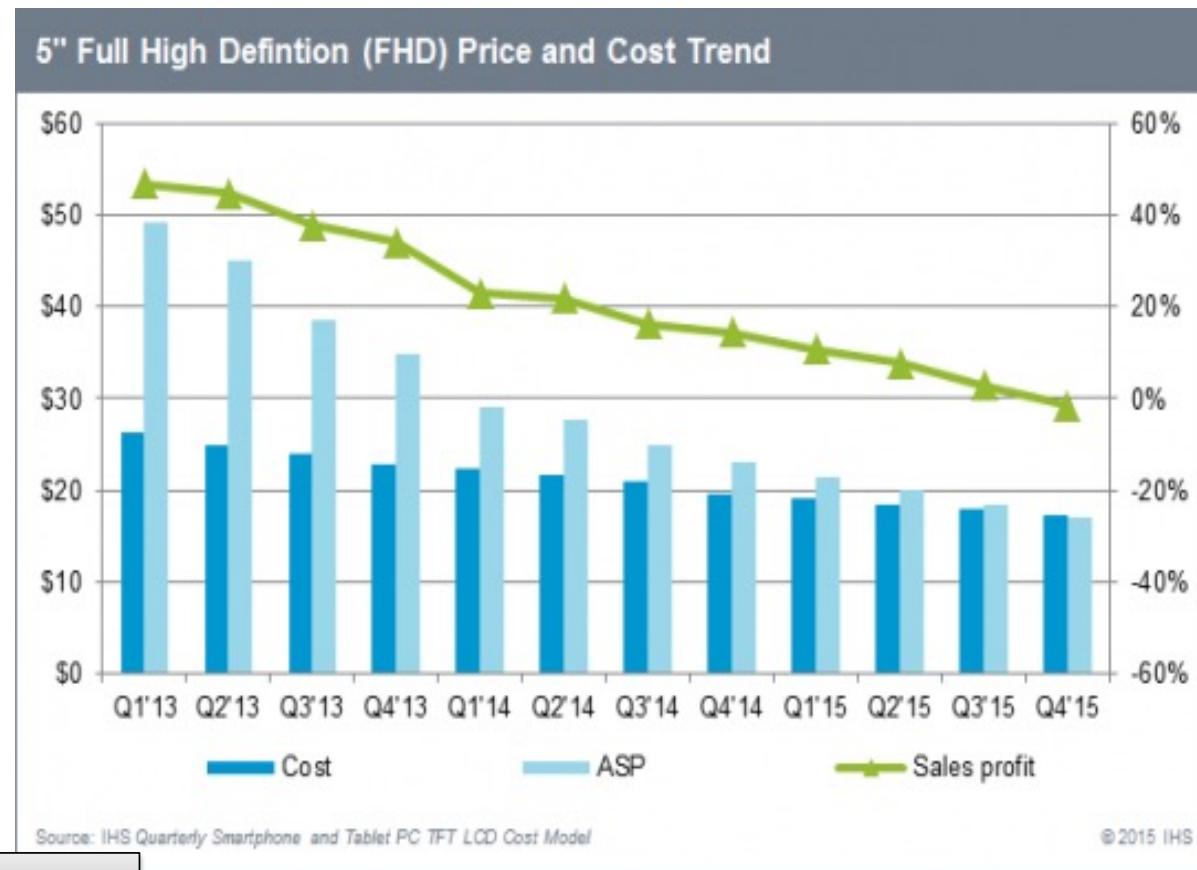
Underlying reason is

- Price erosion
- Like most consumer electronics

Manufacturers must constantly

- Grow volume
- Increase yield
- Reduce overheads

to thrive / survive



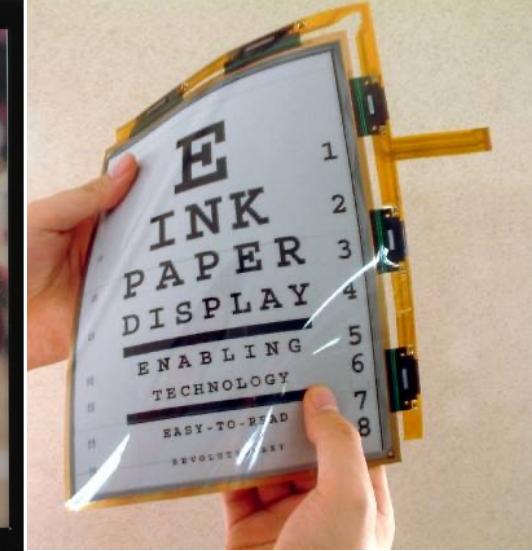
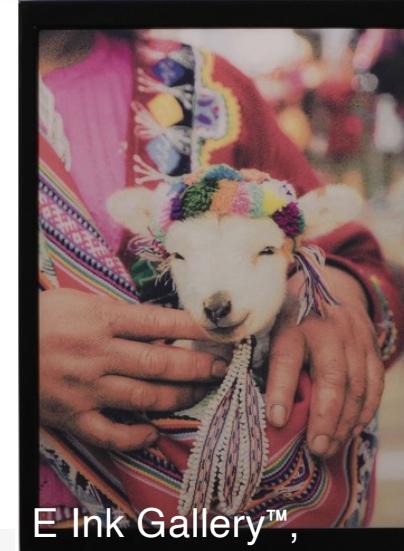
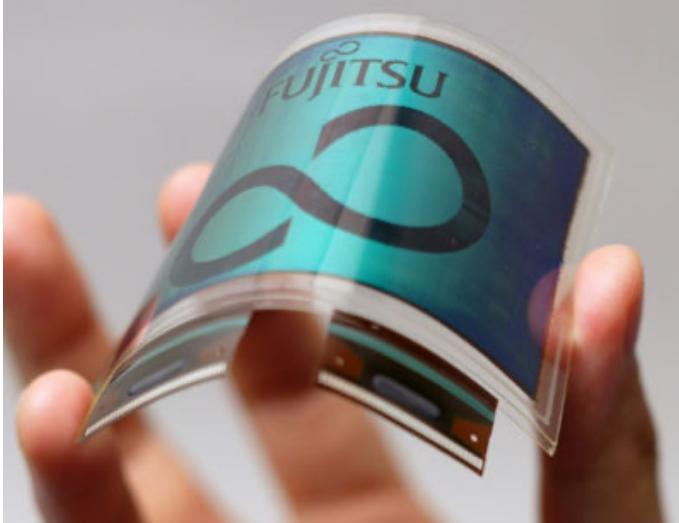
Historical figures that indicate trends

AR/VR HMD – Emerging Market



VARJO XR-3

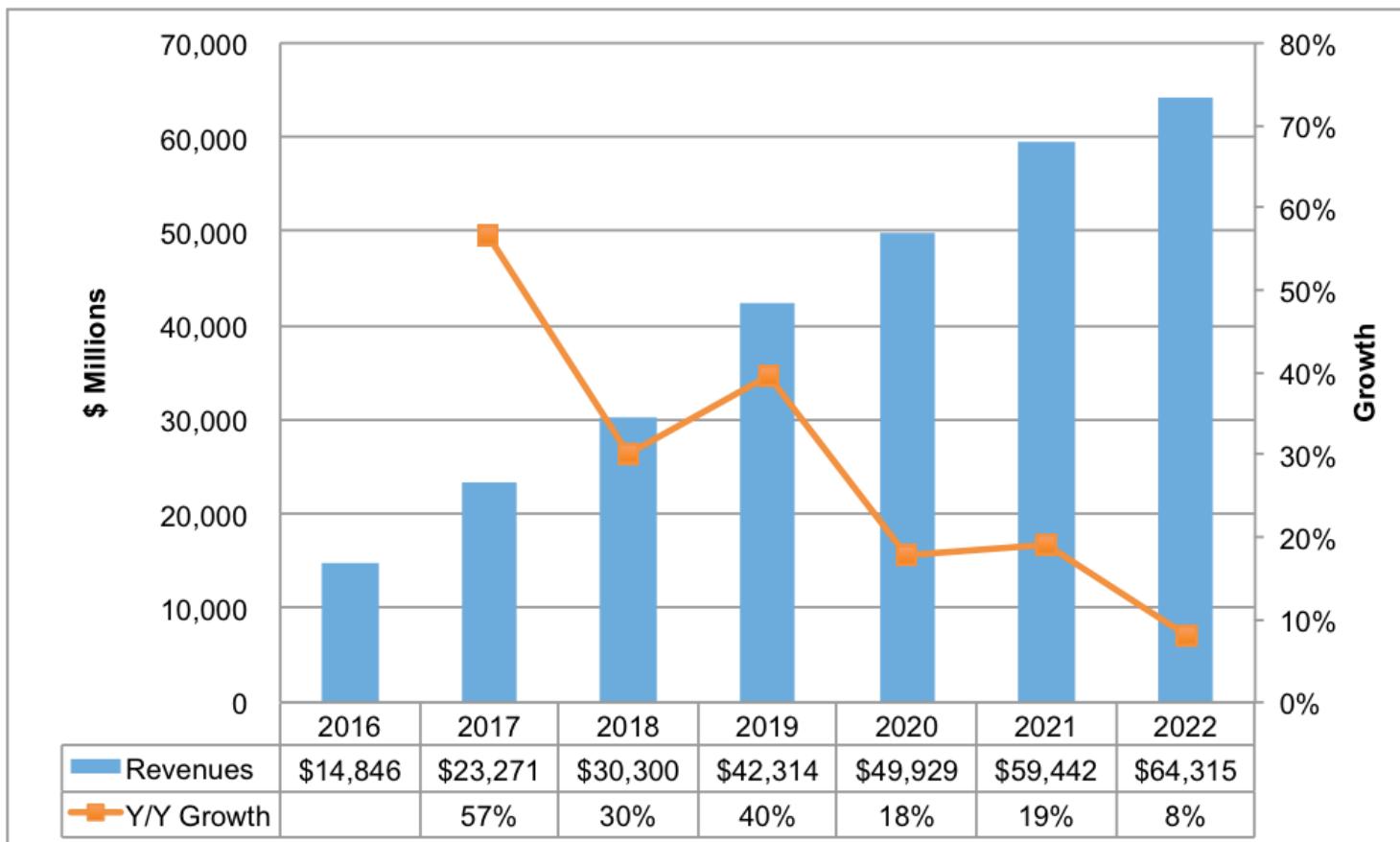
Flexible & Organic



E Ink Gallery™,
based on the Advanced Color ePaper (ACeP™) is a high quality, full color reflective display. In the ACeP™ system, the ink can produce full color at every pixel, without the use of a color filter array (CFA).

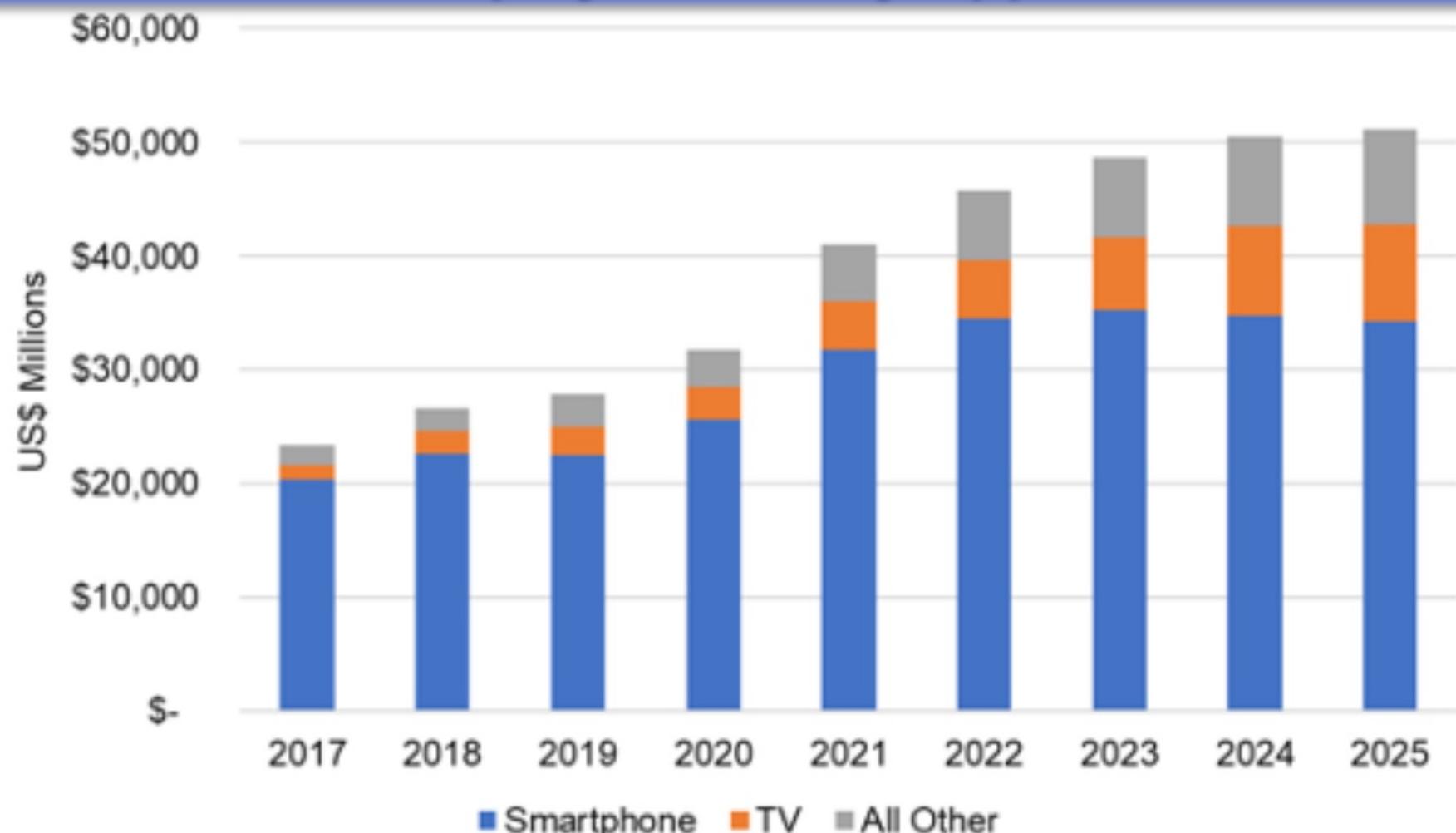


OLED Display Market Forecast



Source – DSCC via Display Daily

OLED Display Panels by Application



Comparing display pixels and sensor array pixels

The main reason that electronic display pixels
are completely unlike image sensor pixels
is because ...



Display System Design

The greatest challenge of display **system** design derives from the fact that...

... no matter how faithful, repeatable and reliable the electronics, electro-optics, backlighting etc is ...

SECTION 3

LIQUID CRYSTAL DISPLAYS

AN INTRODUCTION

MATERIALS, CONCEPTS & ELECTRO-OPTICS

Liquid Crystal Displays (2nd Edition)

Ernst Leuder. Pub Wiley / SID, Ch2, pp3-20.

Handbook of Visual Display Technology (2nd Edition)

Pub Springer 2016

[Twisted Nematic and Supertwisted
Nematic LCDs](#)

Peter Raynes
Pages 2077-2090

[Optics of Liquid Crystals and Liquid
Crystal Displays](#)

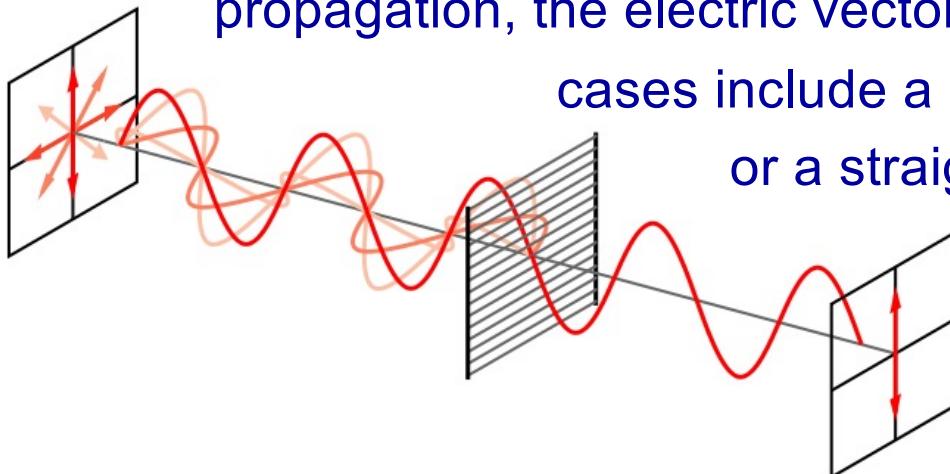
Philip W. Benzie, Steve J. Elston
Pages 1979-2002

Polarized Light

Visible light is a form of Electro-Magnetic Radiation (EMR) with wavelength in the region 390 - 750 nm (790 – 400 THz).

EMR has both electric and magnetic field components, which stand in a fixed ratio of intensity to each other, and which oscillate in phase perpendicular to each other and perpendicular to the direction of energy and wave propagation.

When projected on to the plane normal to the direction of propagation, the electric vector traces an ellipse. Special cases include a circle (circularly polarized) or a straight line (linearly polarized)

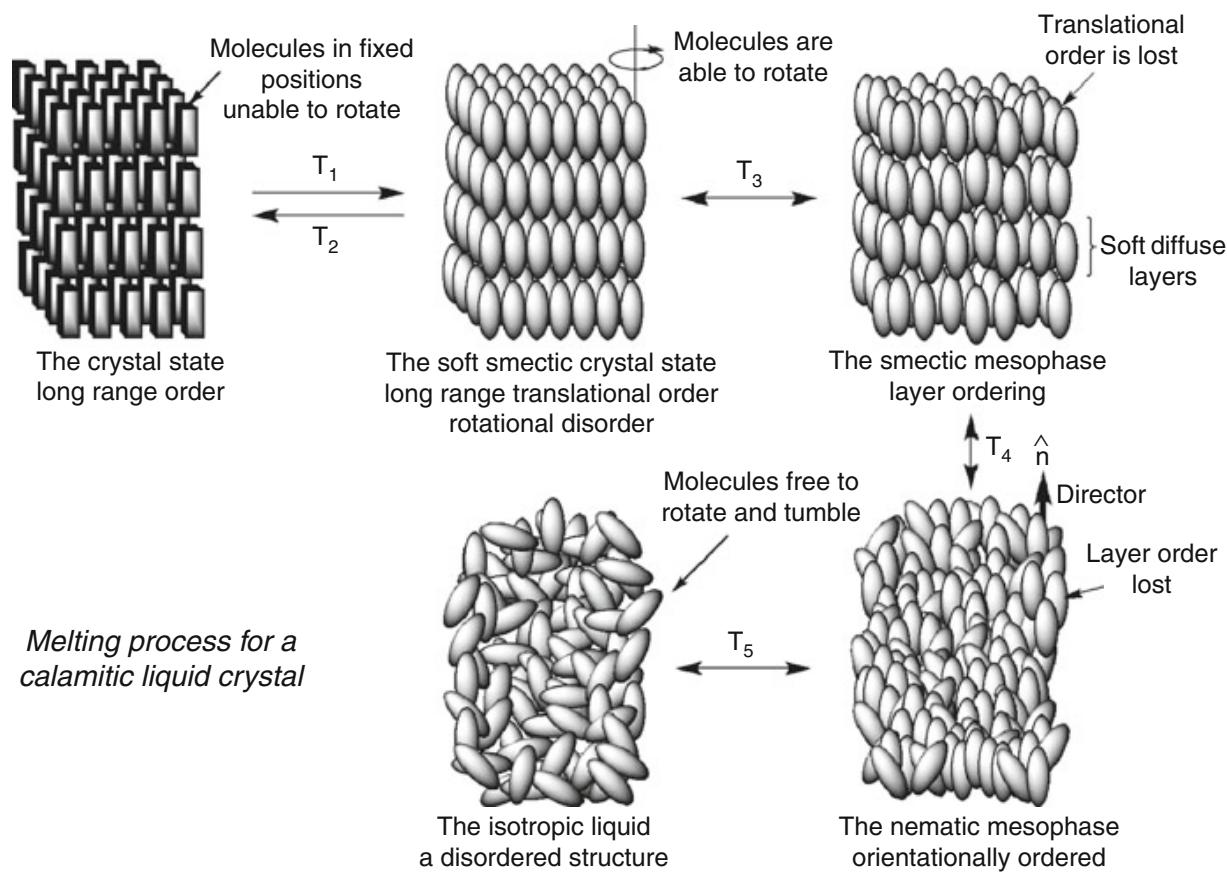


[Animation – plane polarized wave](#)
[Animation - circular polarized light](#)

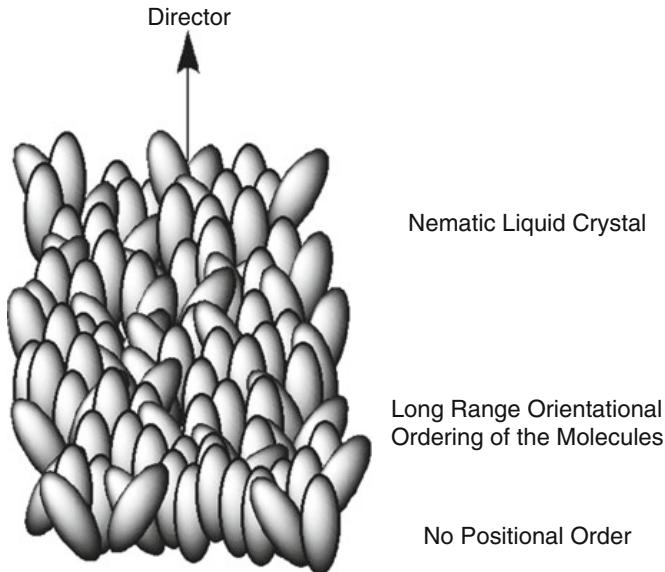
Definition – Liquid Crystal

The term “**liquid crystal**” describes a group of meso-phases between solid crystal and isotropic liquid that exist for a number of organic molecular materials.

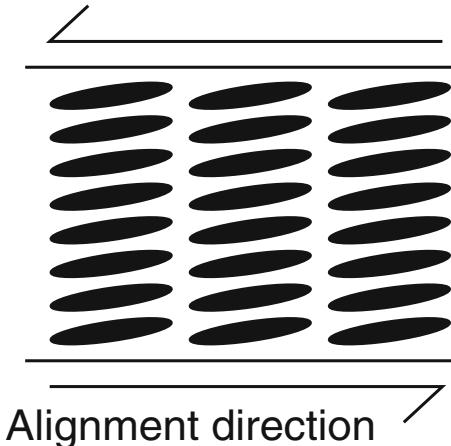
A liquid crystal material is a material that exhibits one or more of these meso-phases.



Definition – Liquid Crystal



b Fréedericksz cell



LC molecules are usually of a particular shape – rod-like (used in LCDs) or disk-like (used for other purposes)

When captured in a thin layer between two flat plates the LC materials can often be “aligned” by surface forces.

An applied electric field can then alter the LC alignment to provide a visible effect (brightness change, colour change).

LC Molecules and Polarizability

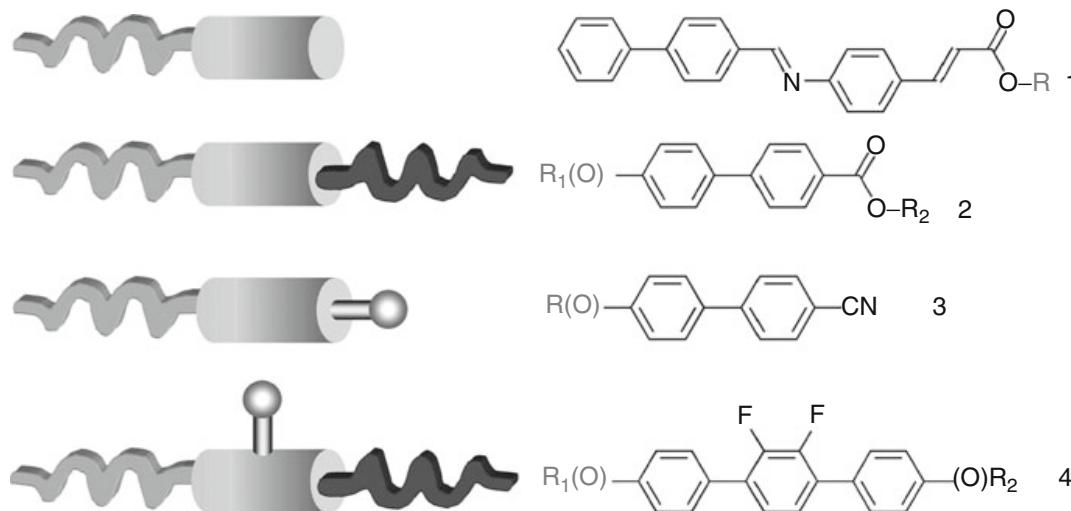
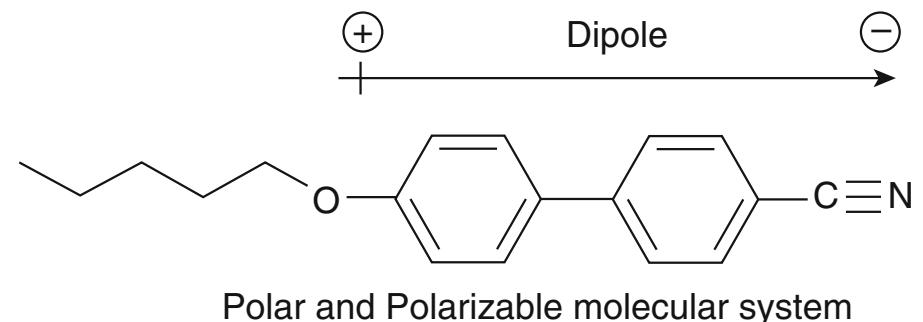
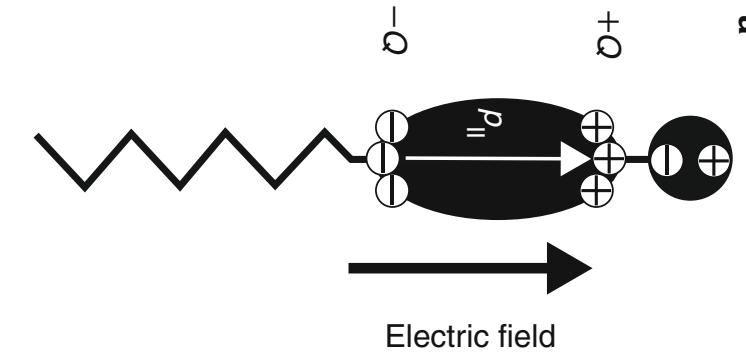


Fig. 12 Typical material design for rodlike liquid crystals (Gray et al. 1973, 1989; Gray and Harrison 1971; Goodby and Gray 1976a). Materials 3 and 4 show the design of liquid crystals found in display devices



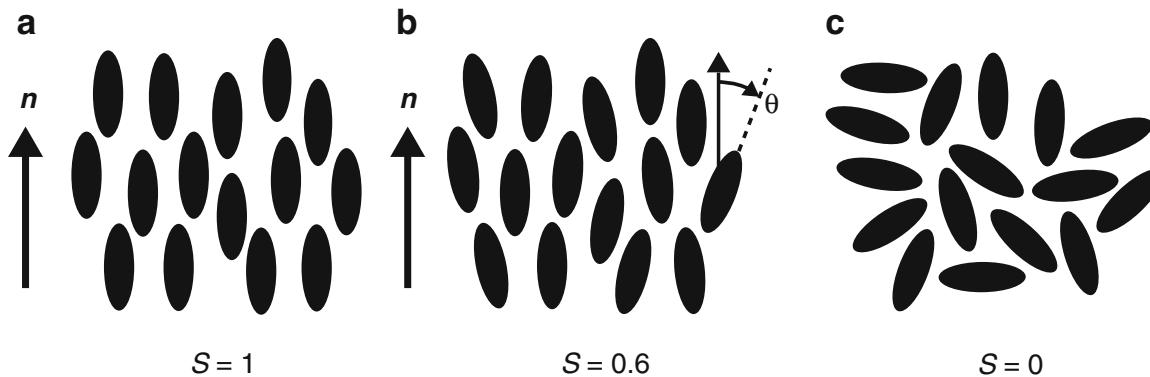
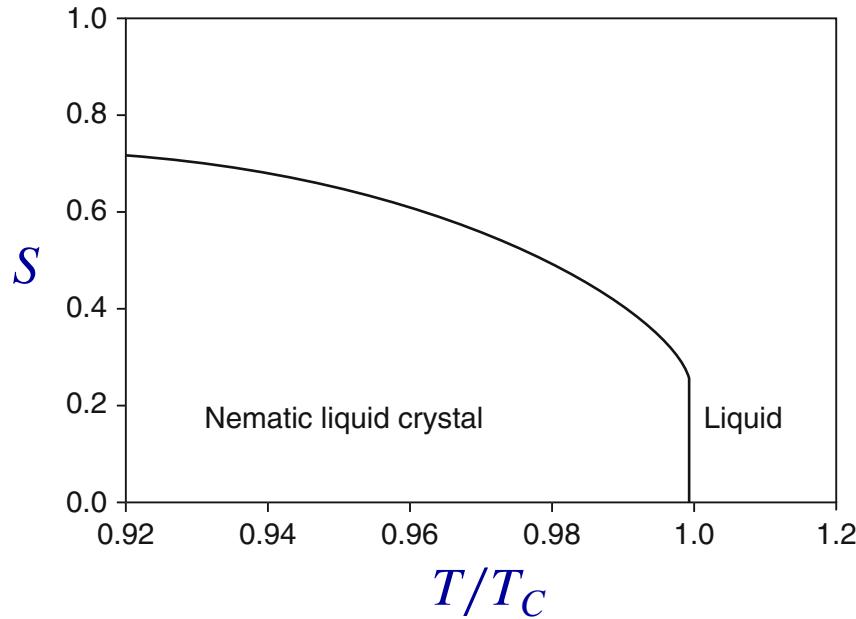
Order Parameter

The Order parameter S is a measure of how mutually well-aligned the molecules are.

$$S = \frac{1}{2} (3 \cos^2 \theta - 1)$$

where

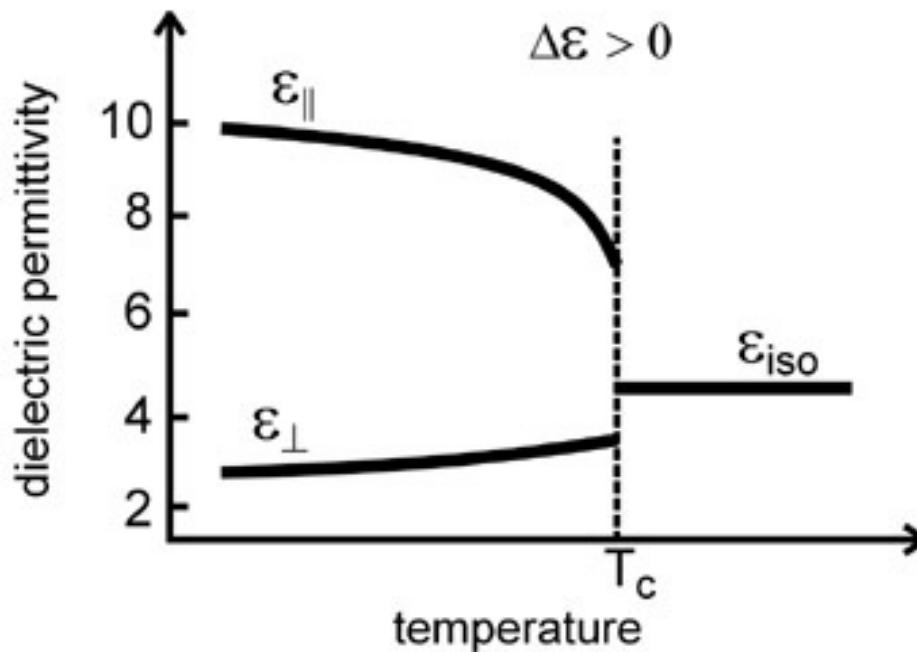
$$S = (1 - T/T_C)^b$$



Dielectric Permittivity

Dielectric properties of LCs are related to the response of LC molecules to the application of an electric field.

Permittivity ϵ is a physical quantity that describes how an electric field affects and is affected by a dielectric medium and is determined by the ability of a material to polarize in response to an applied electric field.



Dielectric Anisotropy and LC switching

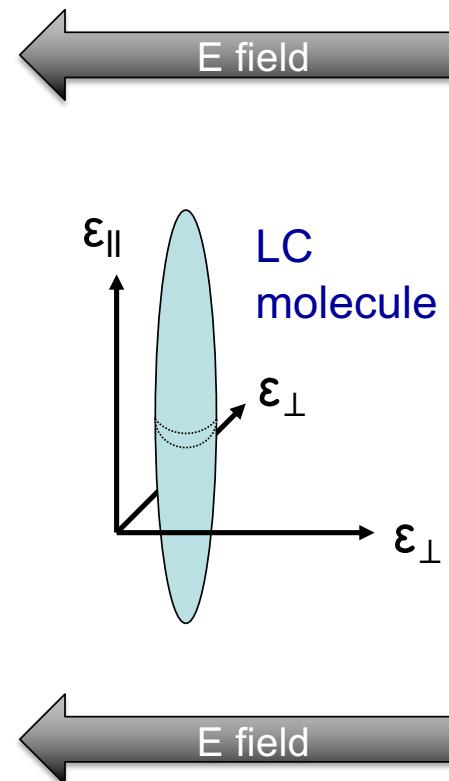
The dielectric anisotropy

$$\Delta\epsilon = \epsilon_{||} - \epsilon_{\perp}$$

can take positive and negative values.

If an electric field is applied orthogonal to its director the liquid crystal will tend to rotate to align the director with the electric field assuming that the director and the dipole moment (more precisely the larger component of the dielectric anisotropy) are essentially co-linear.

In LCs with a positive (*negative*) dielectric anisotropy will align the director parallel (*perpendicular*) to the applied electric field



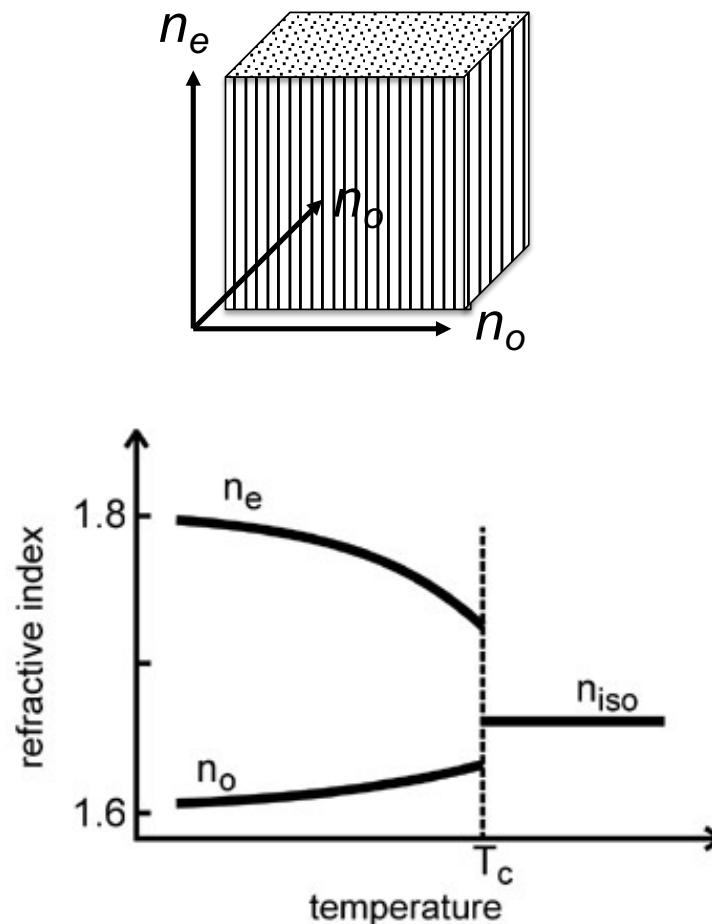
Animated example of positive →

Birefringence (Optical Anisotropy)

Birefringence is the optical property of a material having a refractive index that depends on the polarization and propagation direction of light. Optically anisotropic materials are said to be **birefringent**. The birefringence is often quantified by the maximum difference in refractive index within the material.

A **birefringent** material is one in which the refractive index along one axis (extra-ordinary) is different to that along the other two (ordinary) perpendicular axes.

Many LC configurations exhibit switchable birefringence.



LC Materials

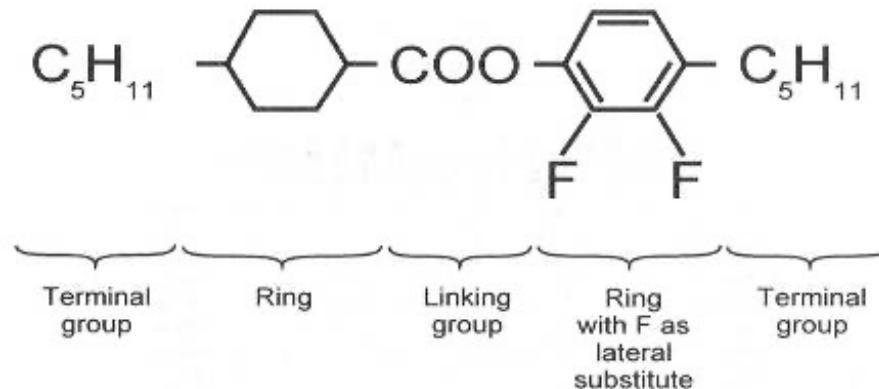
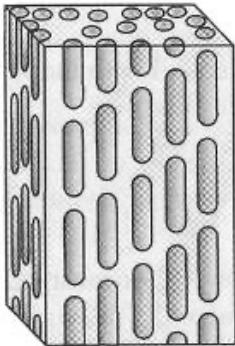


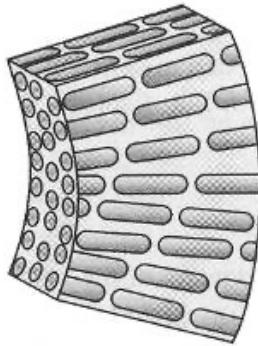
Table 2.2 Properties of nematic LC materials with a wide temperature range

	MLC-1380000	MLC-13800100	MLC-1390000	MLC-13900100
Transition temp.				
smectic-nematic	< -40°C	< -40°C	< -40°C	< -40°C
Clearing pt T_c	110°C	111°C	110.5°C	110.5°C
Rotational				
viscosity, 20°C	228 mPas	151 mPas	235 mPas	167 mPas
$\Delta\epsilon$ 1 kHz, 20°C	+8.9	+5.0	+8.3	+5.2
$n_0 = n_{\perp}$	1.4720	1.4832	1.4816	1.4906
$n_e = n_{ }$	1.5622	1.5735	1.5888	1.5987
Δn	+0.0902	+0.0903	+0.1073	+0.1081

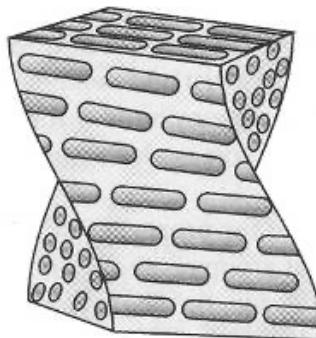
Properties of LCs



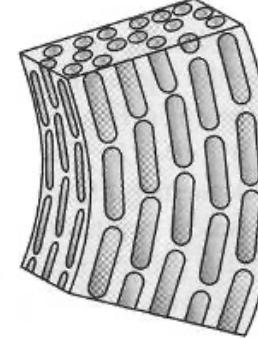
Equilibrium configuration



Elastic constant K_{11}
(a)

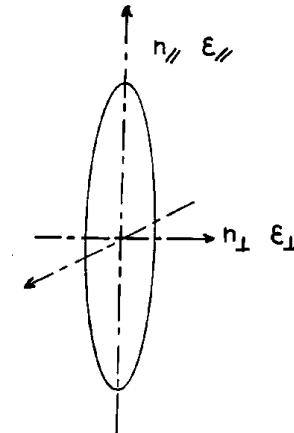


Elastic constant K_{22}
(b)



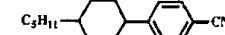
Elastic constant K_{33}
(c)

- (a) Splay
- (b) Twist
- (c) Bend

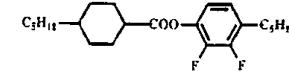


Dielectric anisotropy

$$\Delta\epsilon = \epsilon_{\parallel} - \epsilon_{\perp}$$



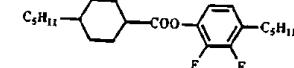
$$\epsilon_{\parallel} = 17.7 \quad \epsilon_{\perp} = 4.8 \quad \Delta\epsilon = +12.9$$



$$\epsilon_{\parallel} = 3.5 \quad \epsilon_{\perp} = 5.6 \quad \Delta\epsilon = -2.1$$

Birefringence

$$\Delta n = n_{\parallel} - n_{\perp}$$



$$n_e = 1.529 \quad n_o = 1.472 \quad \Delta n = 0.057$$

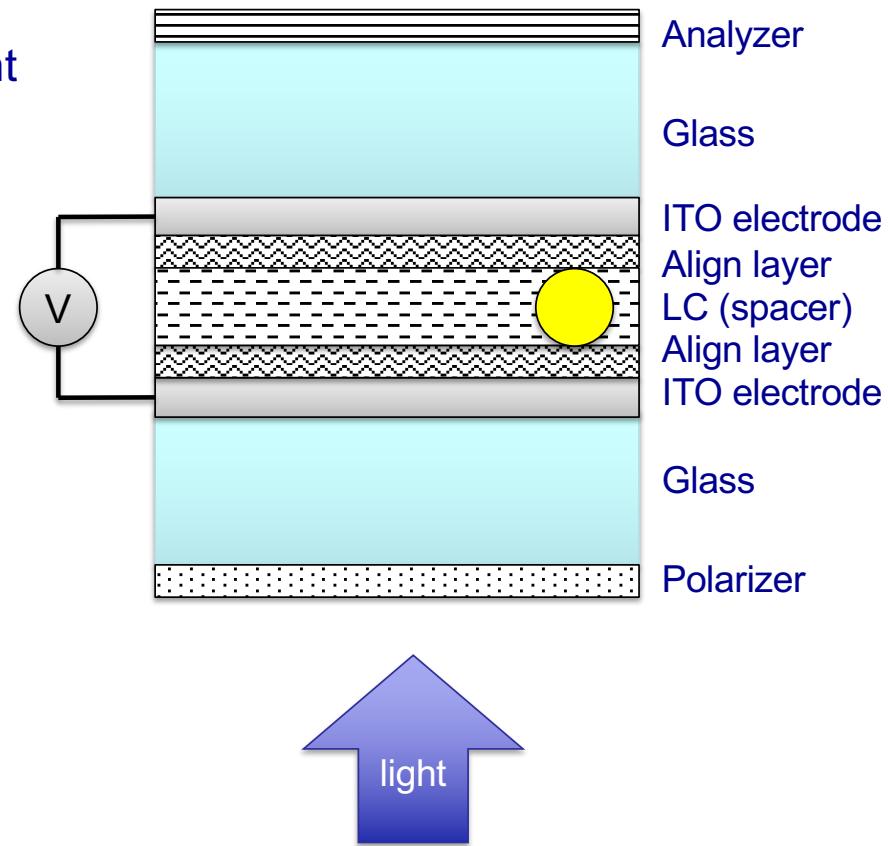
Nematic LC – typical properties

Parameter	Symbol	<u>Typical value</u>	Comments
Clearing point	T_{Cl}	80 °C	Max operating temperature
Sm-N transition	T_{S-N}	-40 °C	Min operating temperature
Optical Anisotropy	$\Delta n = n_e - n_o$	1.562 - 1.477 = 0.085	Determines optical performance
Dielectric Anisotropy	$\Delta \epsilon = \epsilon_{\parallel} - \epsilon_{\perp}$	10.5 - 3.5 = 7	Determines response to E field
Threshold Voltage TN cell	$V_{th,10}$	1.6 V	Voltage at 10% trans (NB mode)
Elastic Constants	K_{11}, K_{22}, K_{33}	10^{-11} N	Important for response time
Rotl Viscosity at 20°C	η_r	100 mPa.s	Important for response time

Basic LC cell

Details

- LC layer <1 to several μm thick
- Thickness uniformity is important
- Alignment layer is mechanical / chemical
- Indium Tin Oxide (ITO) is a **transparent conductive material**
- In a modern LCD there are very many additional features
- Anti-Reflection layers
- Circular polarizer
- Compensation layer(s) to aid viewing angle
- RGB Colour filters layer, etc

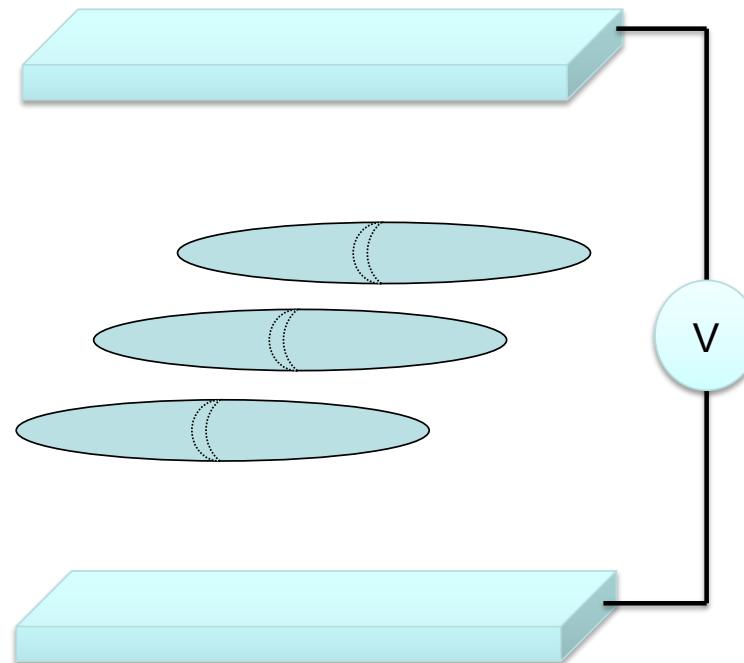


Freedericksz Transition

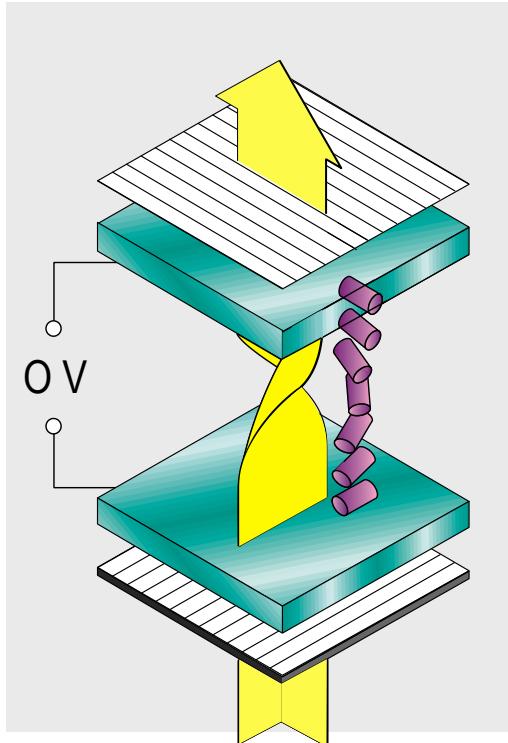
Recall the dielectric anisotropy in LCs

$$\Delta\epsilon = \epsilon_{||} - \epsilon_{\perp}$$

If then an electric field is applied orthogonal to the director the liquid crystal will tend to rotate to align the director with the electric field assuming that the director and the dipole moment (more precisely the larger component of the dielectric anisotropy) are essentially co-linear. The reorientation starts in the middle where there is little surface interaction.

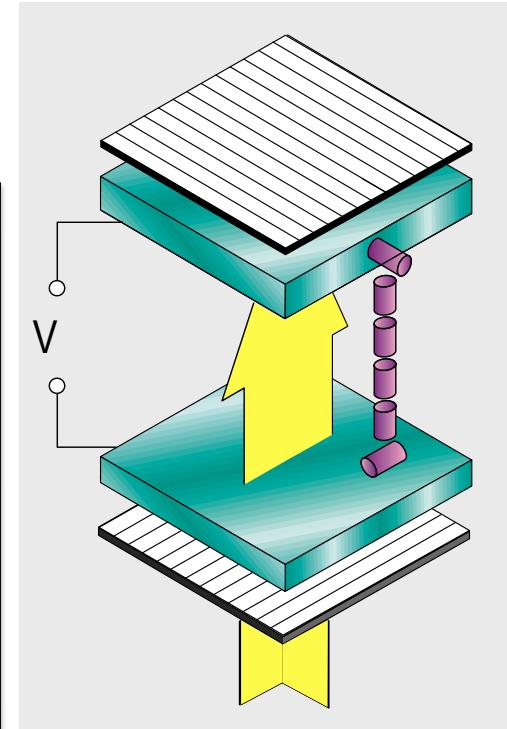


Twisted Nematic (TN) Effect



Crossed polarizers
Drive voltage = zero
Twisted Nematic LC
Light passes through

Nematic LC responds slowly ($>>\text{ms}$) to the RMS value of a medium frequency ($>\text{kHz}$) ac drive waveform



Intermediate voltage
Some light passes

Crossed polarizers
Drive voltage = V_{max}
LC untwisted
Light blocked

Aside on real LCDs

It is relatively straightforward to explain the principle of how an LC cell operates (i.e., how to make a single cell of LC go dark or bright).

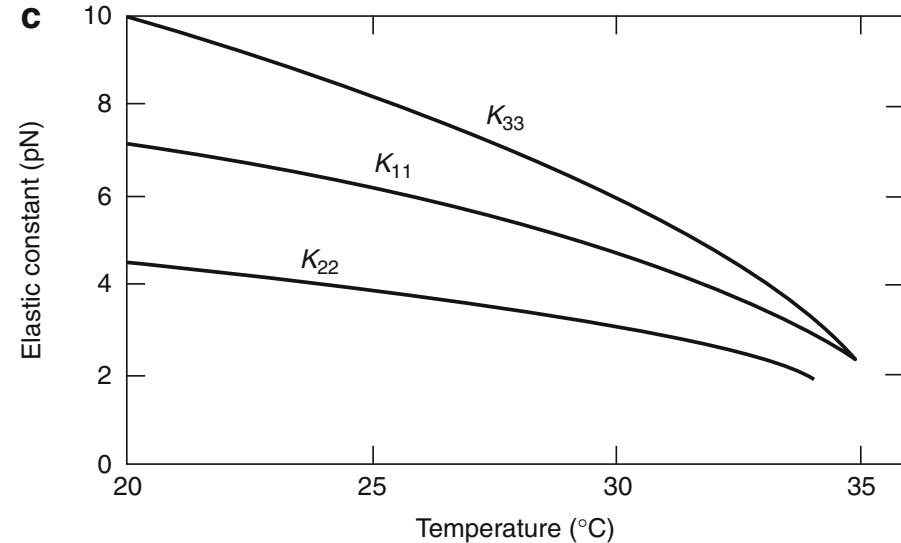
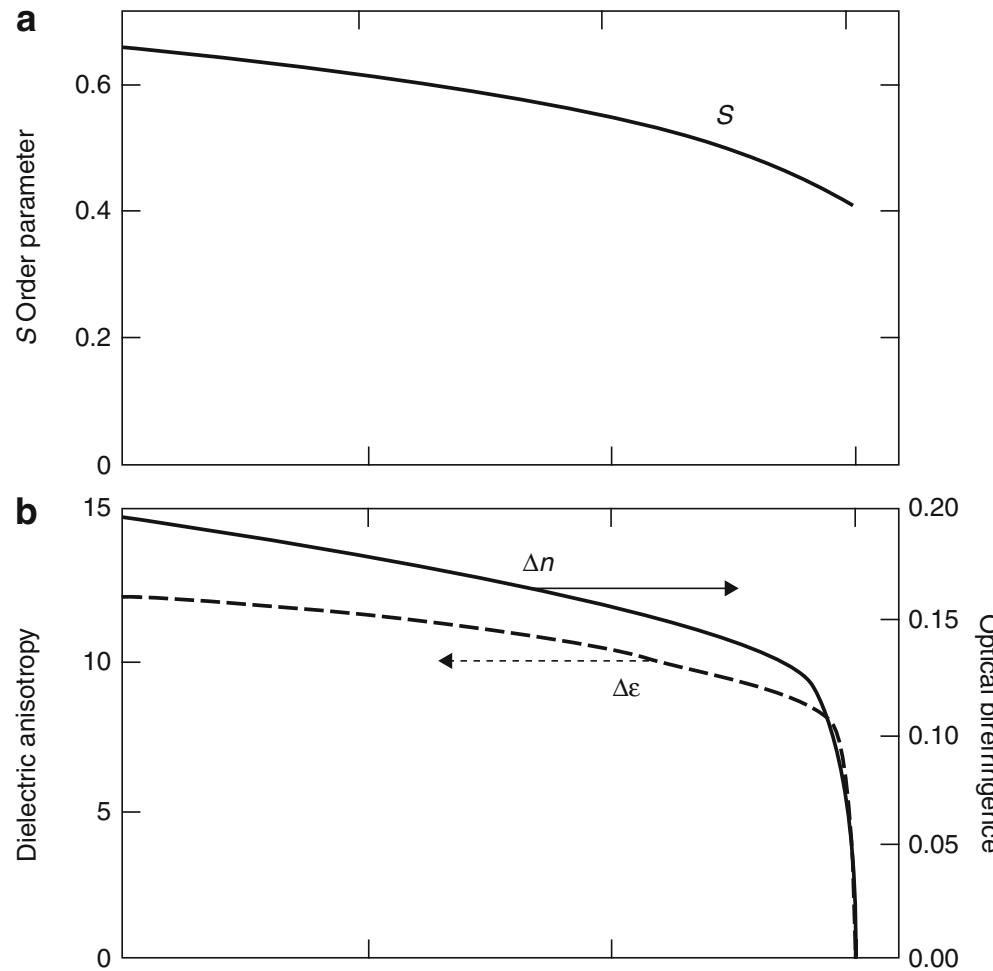
Making a high definition high performance LCD that works well is much more challenging

- Many small close pixels
- Colour (ie wide range of wavelengths)
- Wide viewing angle
- Large temperature range
- High brightness
- High contrast ratio, etc.

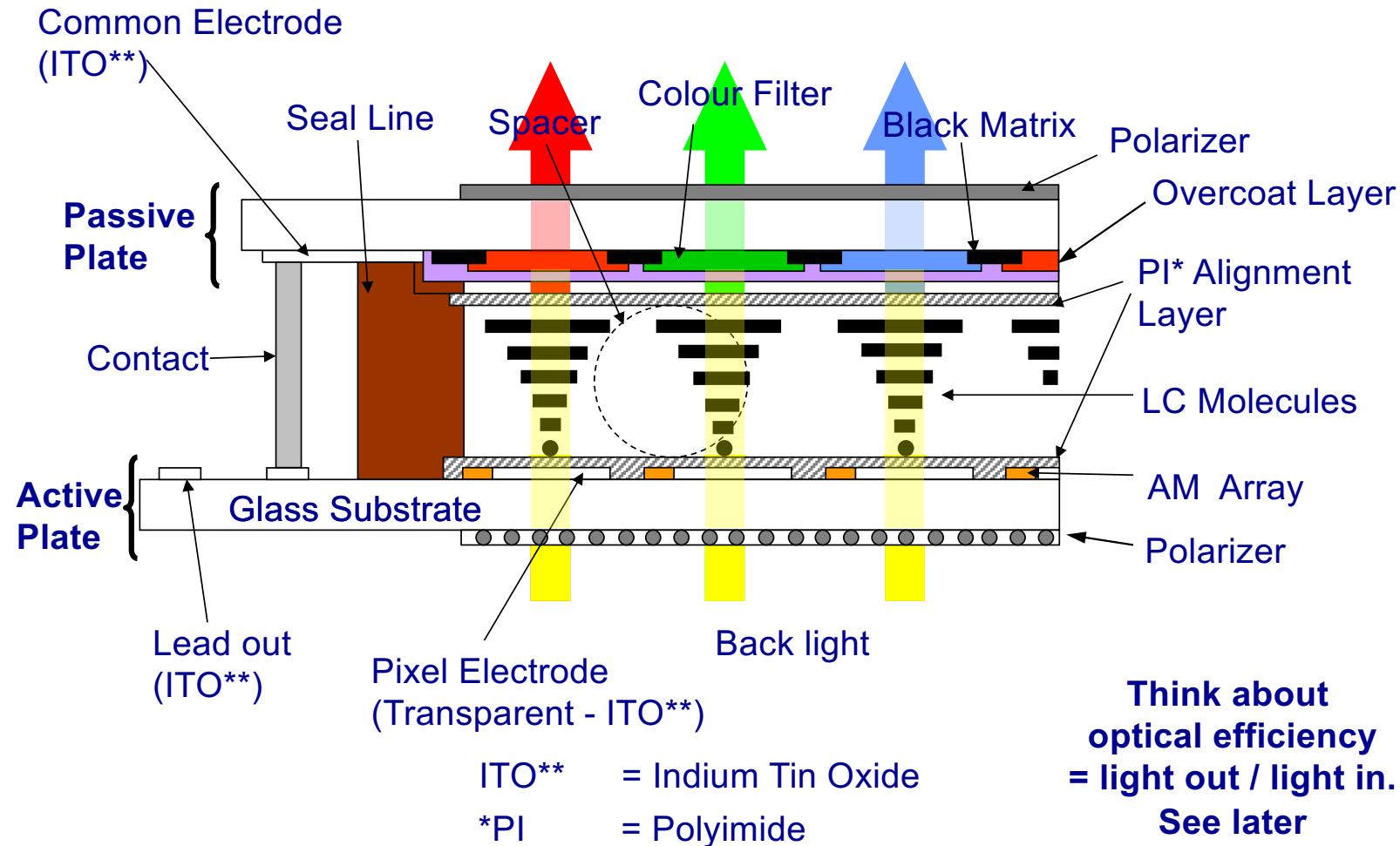
Much of that detail is beyond the scope of this course.



Effect of Temperature



Transmissive AMLCD Overview

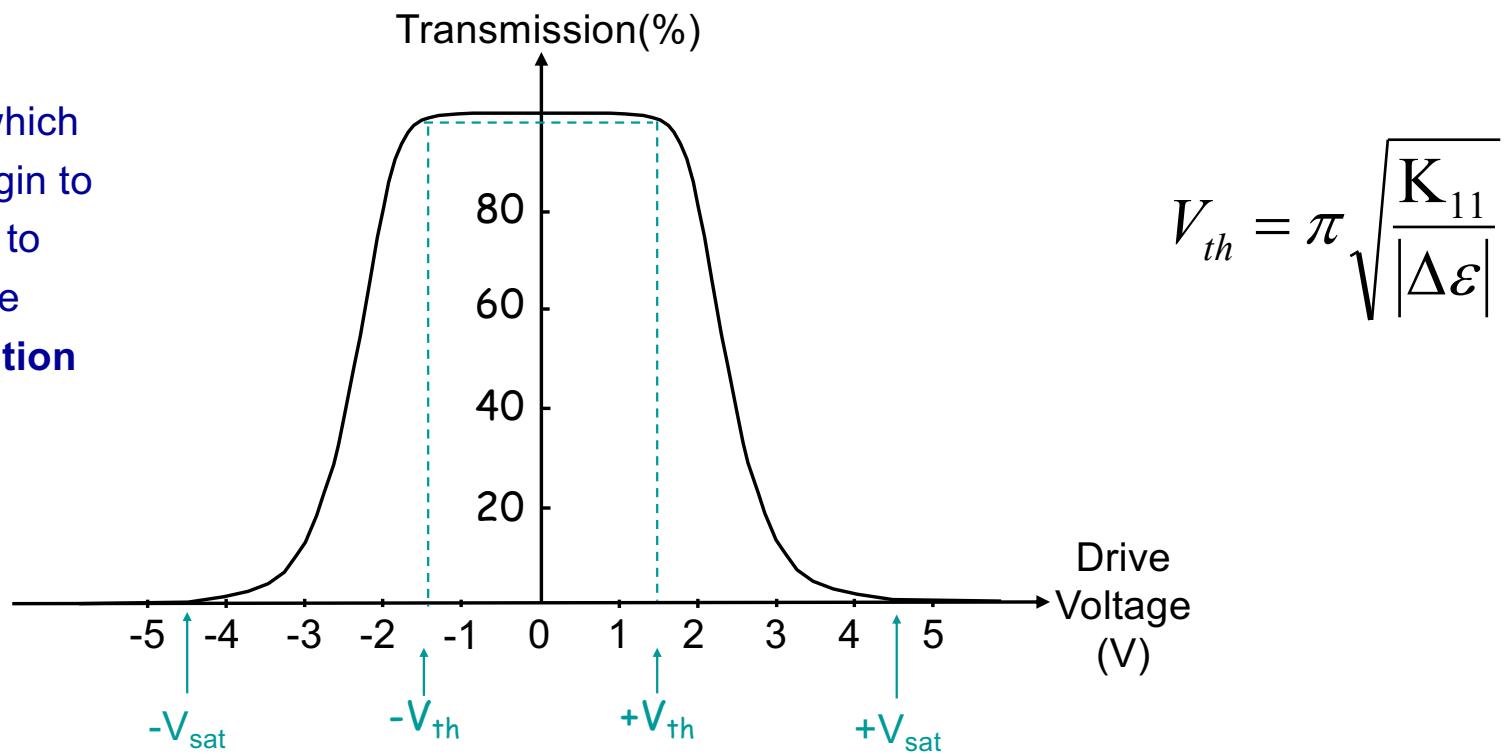


TN LC Transmission-Voltage Curve

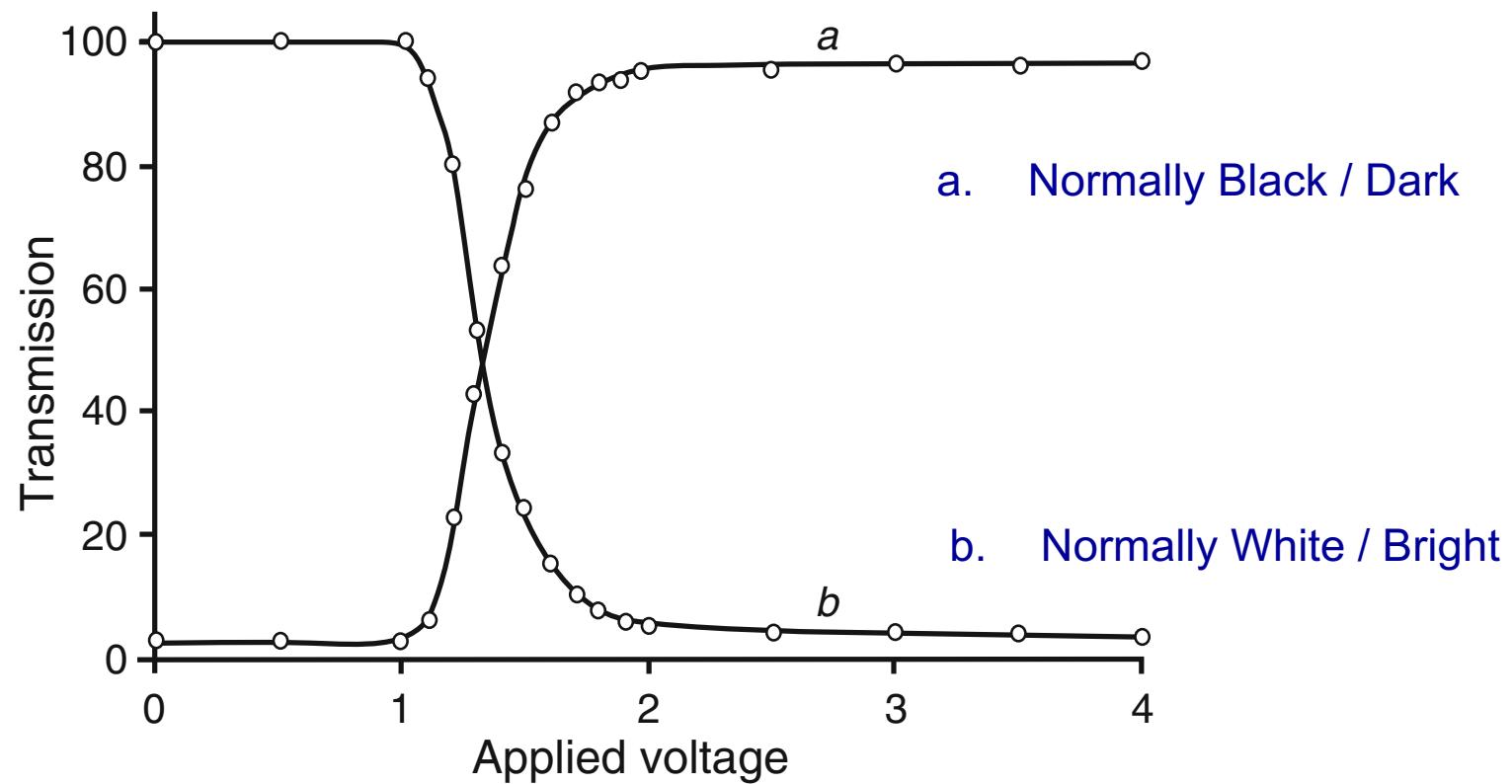
Typical TN LC material with crossed polarizers...

Same effect for +ve & -ve voltages ! Important for inversion drive schemes.

The critical point at which the LC molecules begin to re-orient in response to an E-field is called the **Freedericksz Transition**



TN LC Transmission-Voltage Curve



Some Characteristics of LC devices

Steady-state response

- Detail follows – a few to a few 10's of Volts

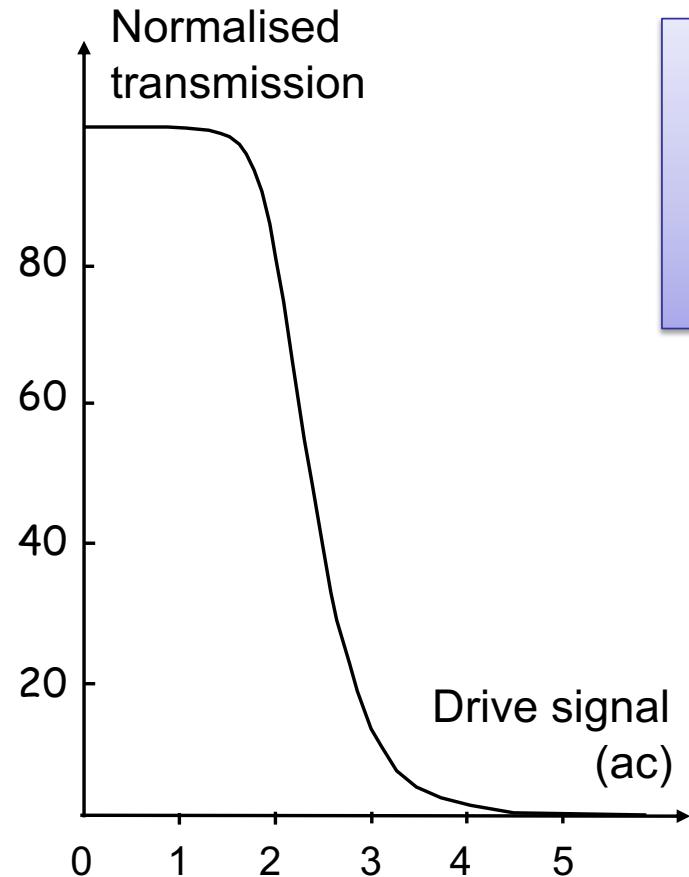
Response speed

- **Nematic** – analog response ~ ms
- (**Ferroelectric** – binary (bistable) response ~ μ s)

Other

- dc balance requirement
 - Long-term V d.c. causes electro-chemical degradation
 - Require a.c. drive for long lifetime
- Temperature limitations
 - At very low T, LC freezes solid
 - At very high T, LC melts to anisotropic liquid
 - In between, properties (e.g. switch speed) vary significantly

LC Switching Time



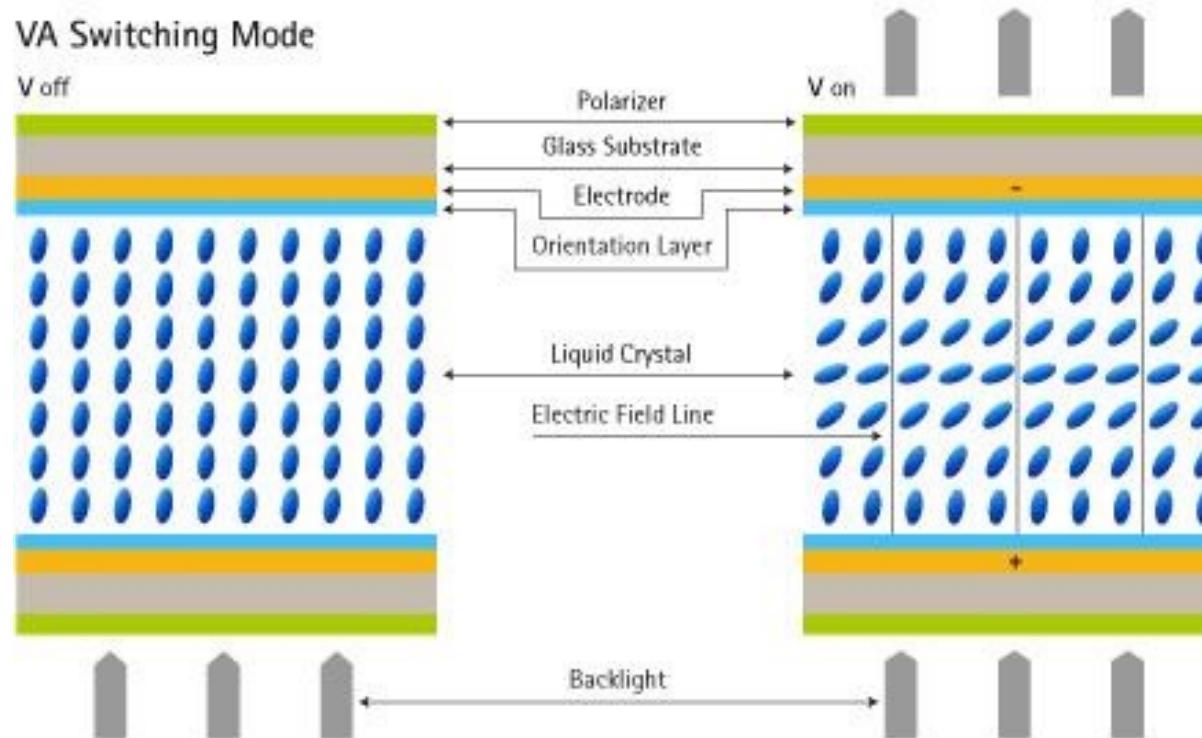
$$T_{rise} = \frac{\eta_r d^2}{\pi^2 K_{11}} \frac{1}{\left(\frac{\Delta\epsilon}{\pi^2 K_{11}} (V_1 - V_{th})^2 - 1 \right)}$$

$$T_{fall} = \frac{\eta_r d^2}{\pi^2 K_{11}}$$

Vertically Aligned LC

In vertical alignment (VA) LCDs, homeotropic liquid crystals – i.e. those aligned normal to the substrate surface – are switched parallel to the glass substrate by the application of an electric field which is normal to the substrate.

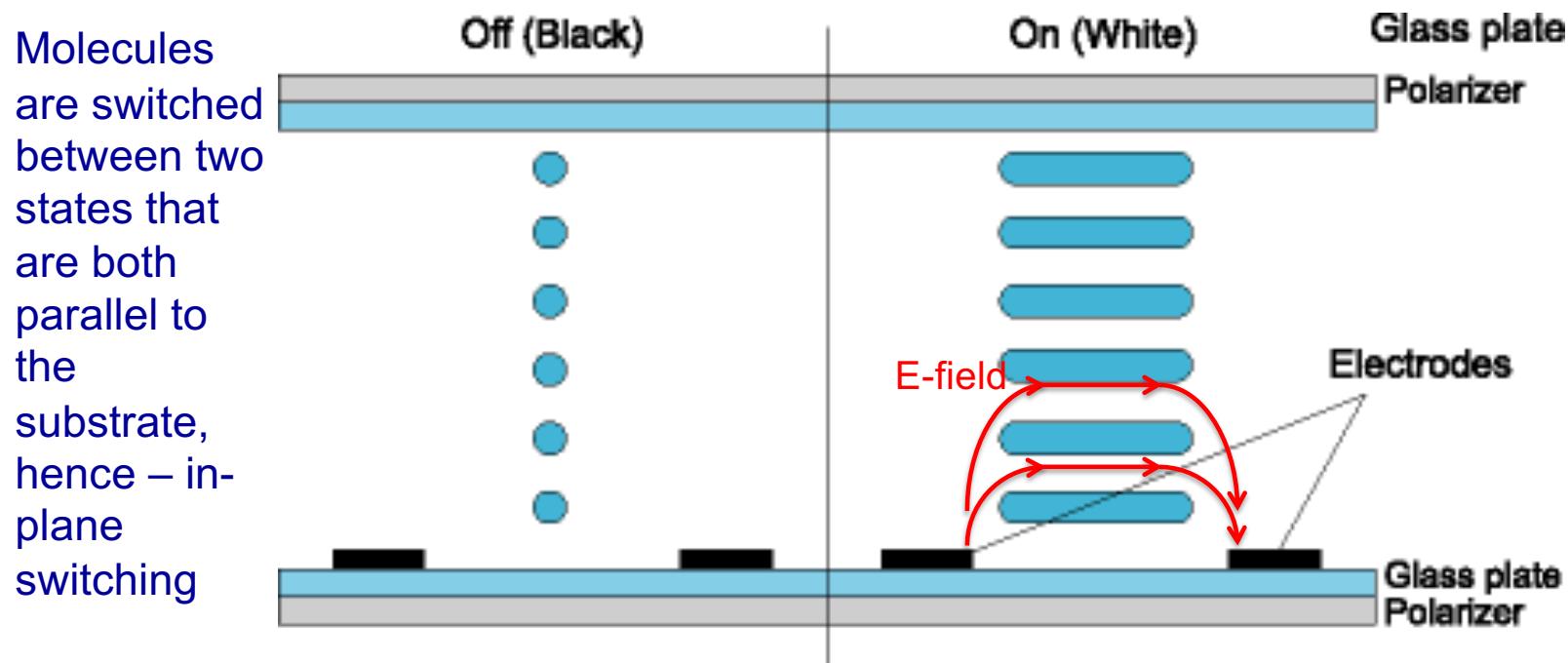
This requires liquid crystal mixtures with negative dielectric anisotropy which are aligned perpendicular to the electric field.



In-Plane Switching (IPS) LC

The IPS (in-plane switching) configuration puts the electrodes whose electrical fields are used to switch the LC molecules are only found on one of the two substrates in the form of strip electrodes.

The resulting electrical field is inhomogeneous and mostly aligned parallel to the substrate surface in the first approximation.



SECTION 4

LIQUID CRYSTAL DISPLAY – PASSIVE MATRIX ADDRESSING

Liquid Crystal Displays (3rd Edition)

Ernst Leuder. Pub Wiley / SID 2022

Ch2 Passive Matrix Addressing of TN Displays

Handbook of Visual Display Technology (2nd Edition)

Pub Springer 2016

[Direct Drive, Multiplex, and Passive Matrix](#)

Karlheinz Blankenbach, Andreas Hudak, Michael Jentsch

Pages 621-644

Objective and Contents

Objective

Introduce passive matrix (PM) addressing for LCDs of medium definition, complexity, performance and price

Usually monochrome or simple colour alphanumeric panels

Understand the constraints of PM LCD.

Contents

Review of background

Explanation of PM addressing

Derivation of Alt and Pleshko Criteria

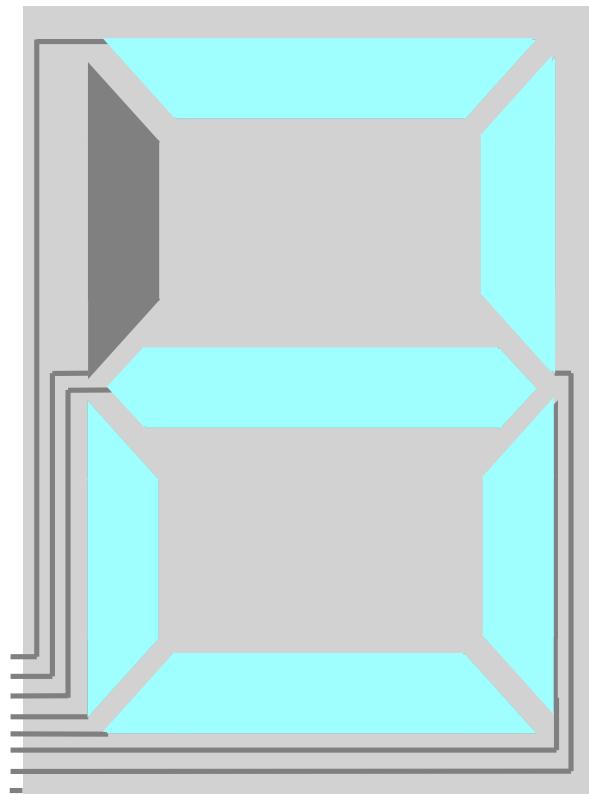
- leads to significant constraints of PM

Workarounds

Summary

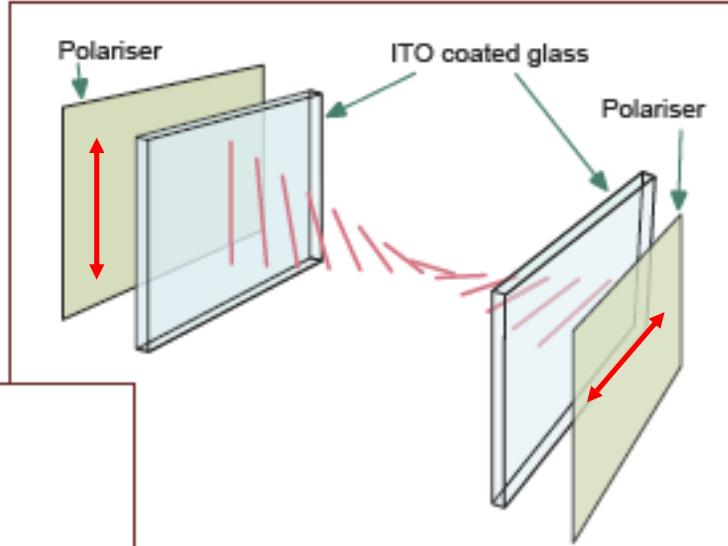
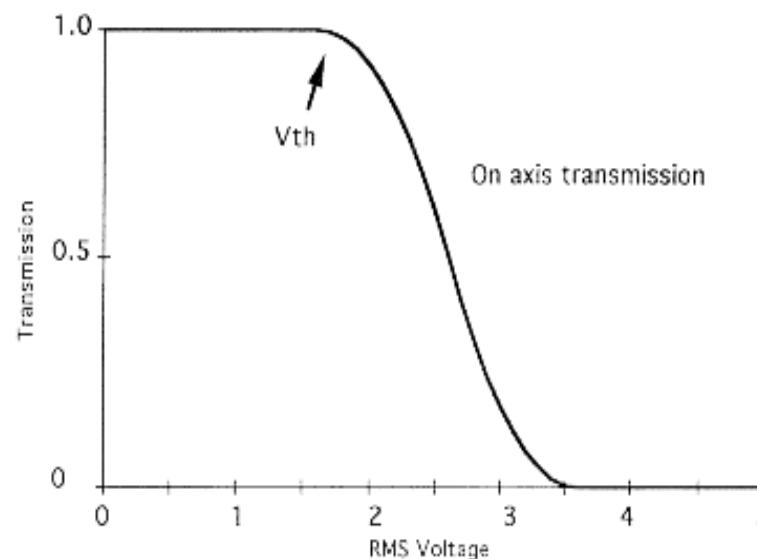
Direct Drive

- Common (or front) electrode
- Patterned (or back) electrode
- Per display segment
 - One driver
 - One connecting wire
- For higher pixel count displays this quickly becomes unmanageable



Revision – TNLC Config & Response

Electro-optic response of Liquid Crystal Display



Q. What if the polarisers are aligned parallel?

Threshold Voltage – Twisted Nematic

General (i.e., parallel) nematic LC

$$E_C = \frac{\pi}{d} \left(\frac{K_{11}}{|\Delta\epsilon|} \right)^{0.5}$$

$$V_{th} = \pi \left(\frac{K_{11}}{|\Delta\epsilon|} \right)^{0.5}$$

Where d = LC thickness

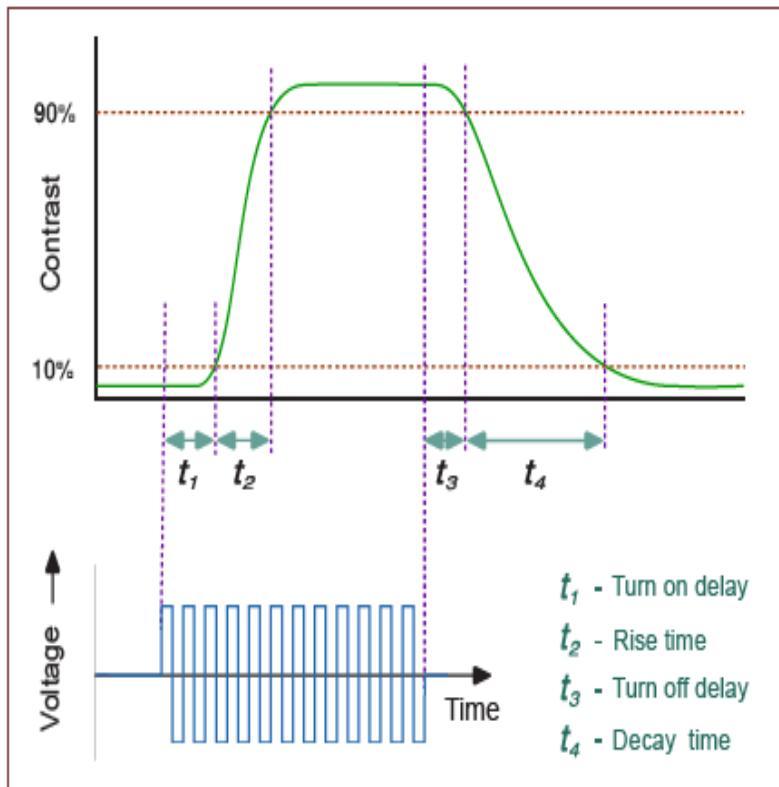
All the K_{11} K_{22} K_{33} etc
are defined in Section 3

Twisted nematic LC

$$V_{th} = \pi \left(\frac{K_{11} + (K_{33} - 2K_{22})/4}{|\Delta\epsilon|} \right)^{0.5}$$

Nb. It's the voltage!
(not the E field?)

Switching Time – twisted nematic



Switching time constants for LC material

Rise (**drive**) time

– Typical 20 – 80 ms*

$$\tau_r = \frac{\eta_r d^2}{\epsilon_0 |\Delta \epsilon| V^2 - \left(K_{11} + \frac{K_{33} - 2K_{22}}{4} \right) \pi^2}$$

Fall / decay (**relax**) time

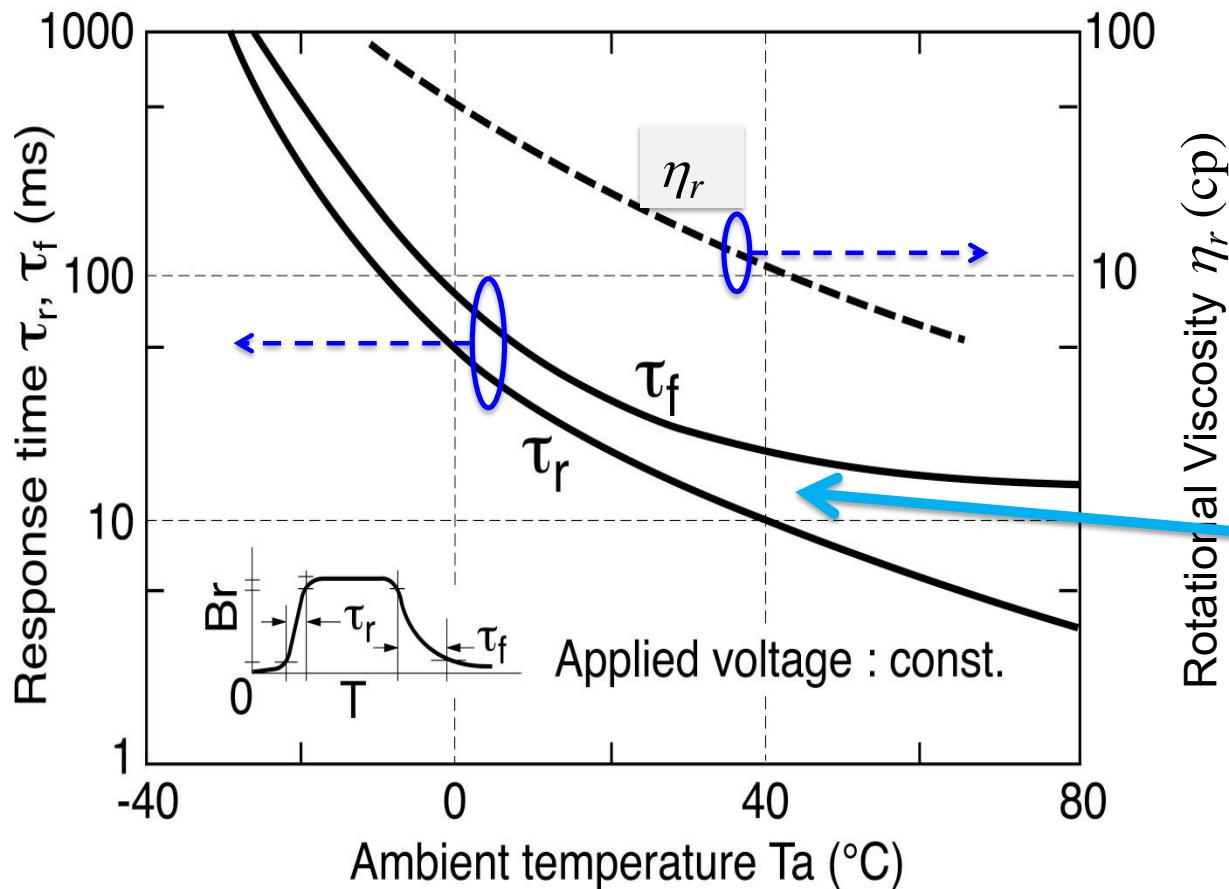
– Typical 60 – 150ms*

$$\tau_f = \frac{\eta_r d^2}{\left(K_{11} + \frac{K_{33} - 2K_{22}}{4} \right) \pi^2}$$

Both very temperature dependent

* Want slow for active matrix

Response Time Characteristic

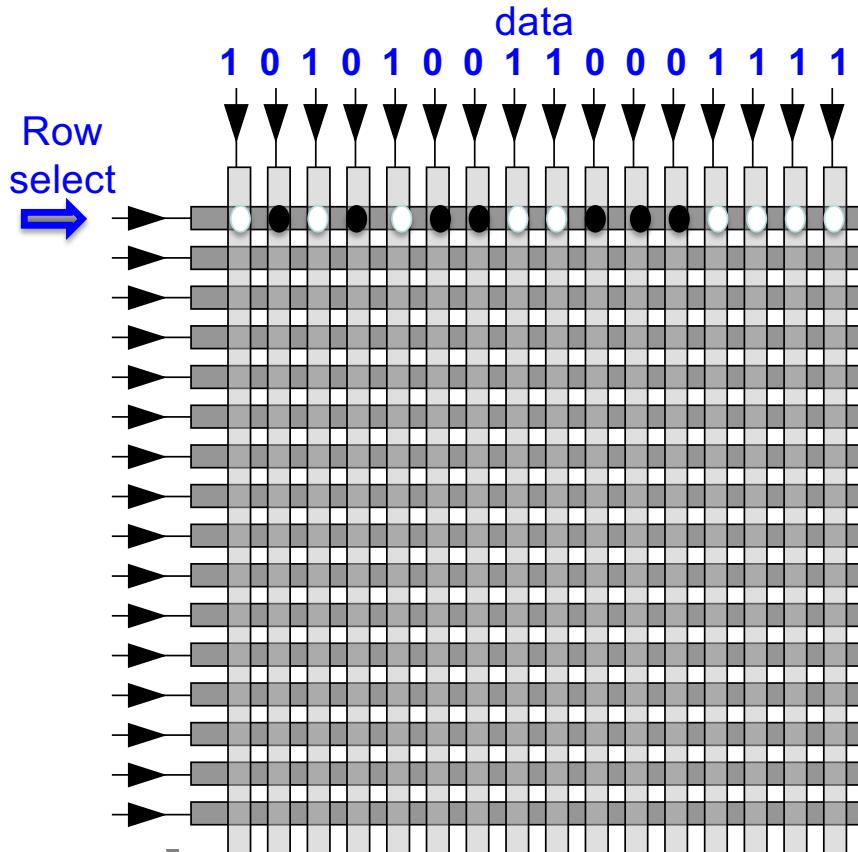


Suggests electronic driving force stronger than mechanical restoring force

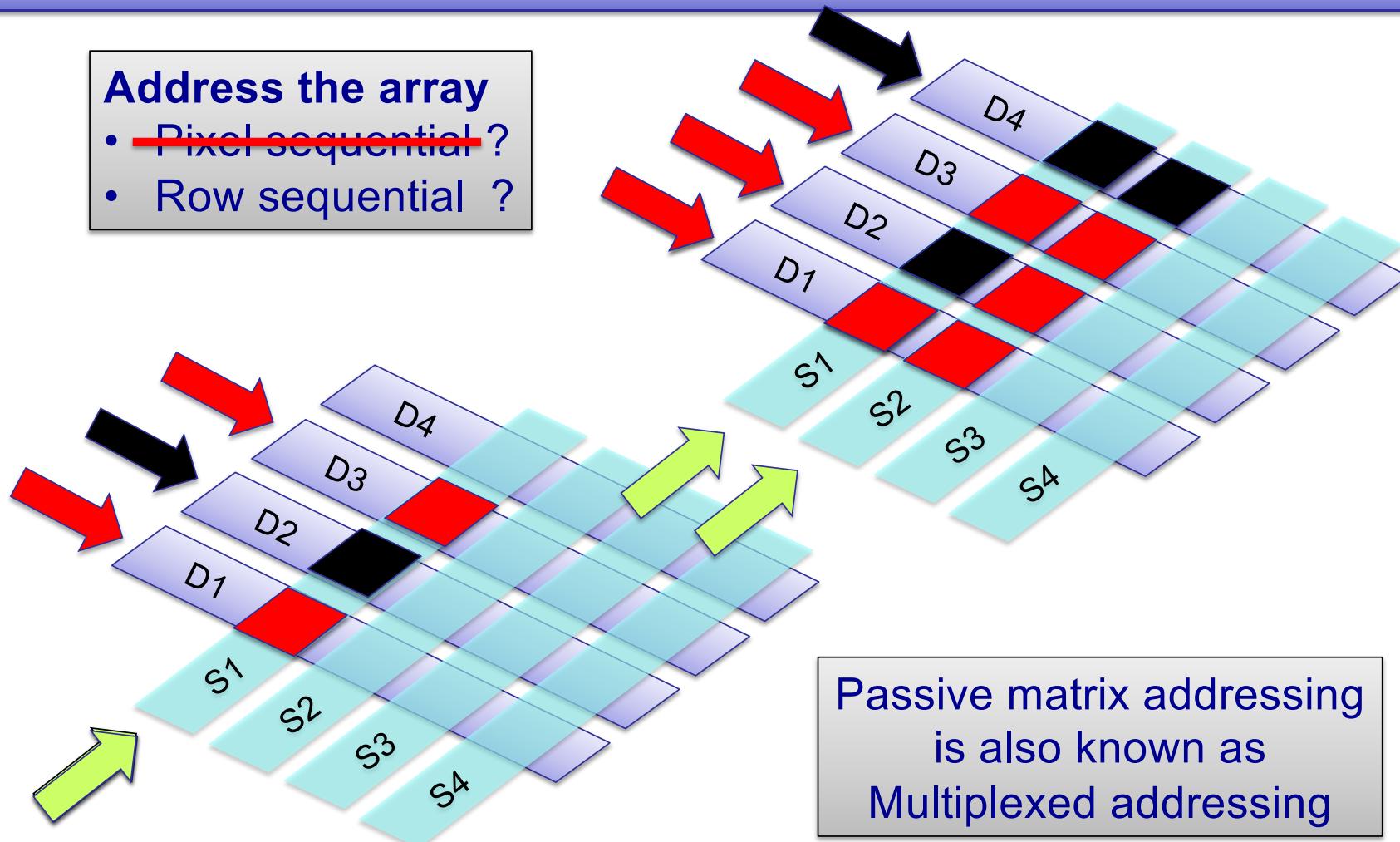
Passive Matrix

Q. Does it matter?

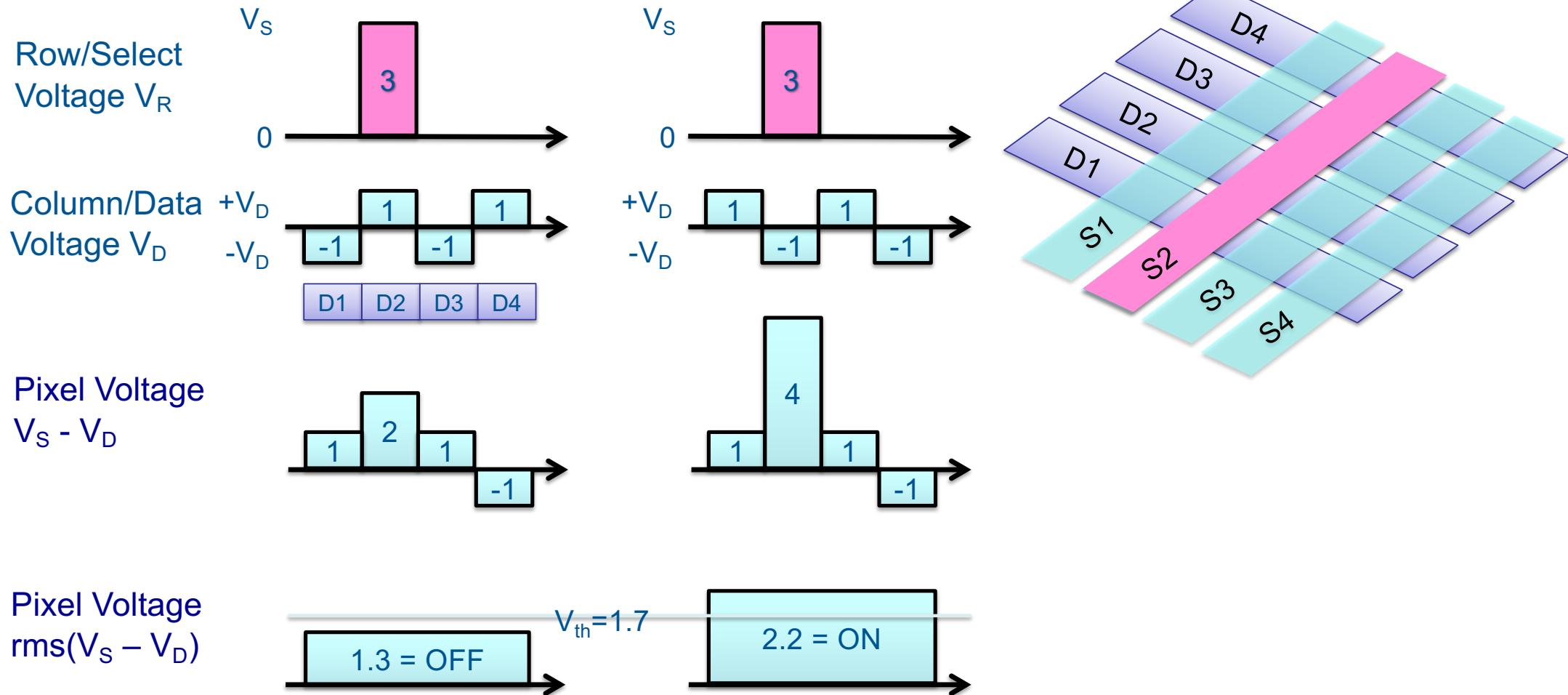
- Back electrode is vertical columns
- Front electrode is horizontal rows
- Per row / column
 - One driver
 - One connecting wire
- $M \times N$ pixels requires only $M+N$ drivers

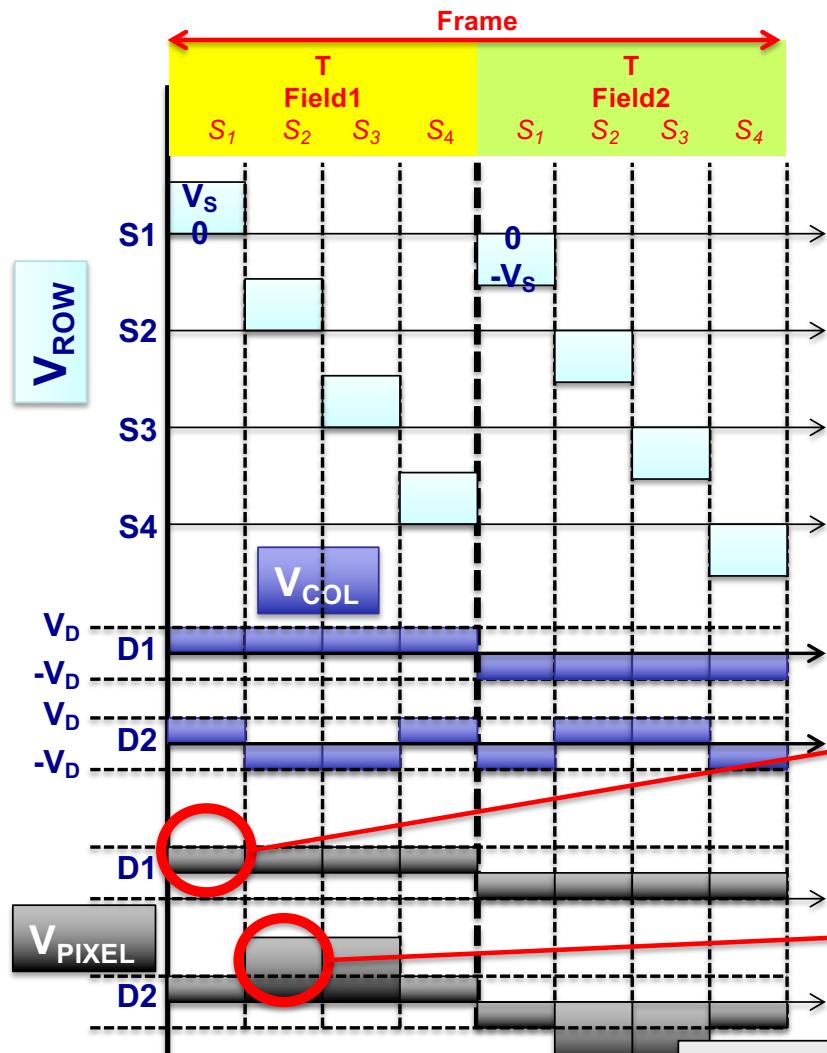


Passive Matrix Pixel Array



Single Pixel Response and Drive Waveform



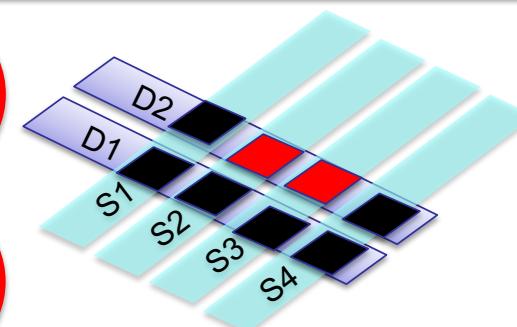


Example of Array Addressing Waveforms

$$V_{ROW} = 0, V_s$$

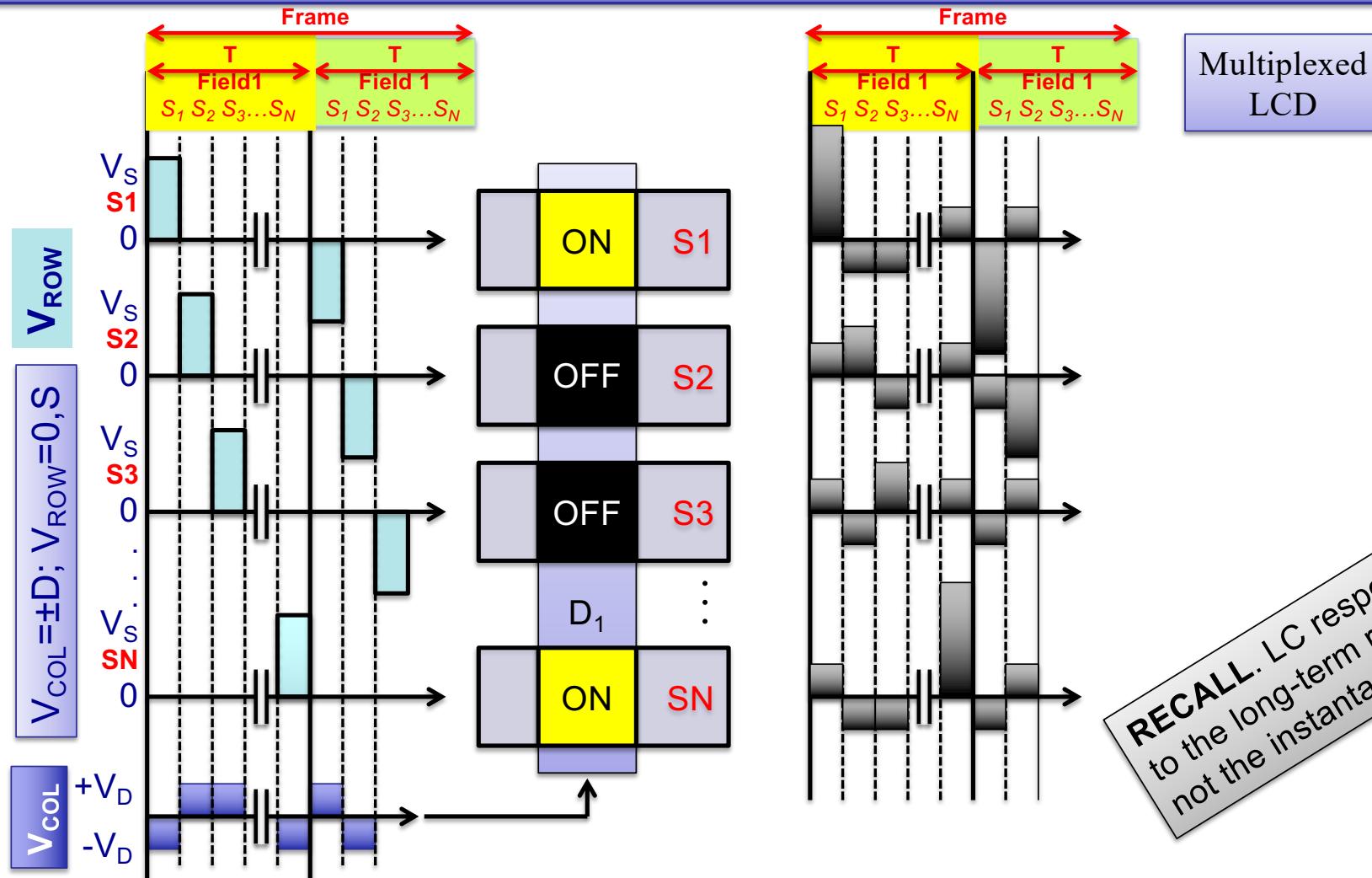
$$V_{COL} = \pm V_D$$

$$V_{PIXEL} = V_s \pm V_D \text{ (addressed)} \\ 0 \pm V_D \text{ (not-addressed)}$$



The purpose of Field 2 is to repeat Field 1 with all signals reverse polarity to achieve dc balancing

Example of Array Addressing Waveforms



RECALL. LC responds slowly to the long-term rms voltage, not the instantaneous value

Alt and Pleshko Criteria (1)

ON pixel

N rows means
the line time is T/N
where T is the frame time

- If the pixel is **ON**
the voltage it “sees” is
- $V_S + V_D$ for $1/N$ of the time
 - $\pm V_D$ for $(N-1)/N$ of the time

Define $\eta = 1/N$

Sometimes use η

V_{on} is the rms voltage experienced by an on pixel

$$V_{PIX,RMS} = \left[\frac{1}{T} \int_0^T [V(t)]^2 dt \right]^{1/2}$$

$$V_{on}^2 = \frac{1}{T} \int_0^{T/N} (V_S + V_D)^2 dt + \frac{1}{T} \int_{T/N}^T V_D^2 dt$$

$$V_{on}^2 = \frac{1}{T} \left[(V_S + V_D)^2 [t]_0^{T/N} + V_D^2 [t]_{T/N}^T \right]$$

$$= \frac{1}{T} \left[(V_S + V_D)^2 \frac{T}{N} + V_D^2 (N-1) \frac{T}{N} \right]$$

$$V_{on} = \left[\frac{(V_S + V_D)^2 + V_D^2(N-1)}{N} \right]^{1/2}$$

cf Slide 10 **ON**

$$\left[\frac{4^2 + 3}{4} \right]^{\frac{1}{2}} = \sqrt{4.75} = 2.2$$

Alt and Pleshko Criteria (2)

OFF pixel

N rows means
the line time is T/N
where T is the frame time
If the pixel is **OFF**
the voltage it “sees” is

- $V_s - V_d$ for $1/N$ of the time
- $\pm V_d$ for $(N-1)/N$ of the time

Define $\eta = 1/N$
Sometimes use η

V_{off} is the rms voltage experienced by an off pixel

$$V_{PIX,RMS} = \left[\frac{1}{T} \int_0^T [V(t)]^2 dt \right]^{1/2}$$

$$V_{off}^2 = \frac{1}{T} \int_0^{T/N} (V_s - V_d)^2 dt + \frac{1}{T} \int_{T/N}^T V_d^2 dt$$

$$V_{off}^2 = \frac{1}{T} \left[(V_s - V_d)^2 [t]_0^{T/N} + V_d^2 [t]_{T/N}^T \right]$$

$$= \frac{1}{T} \left[(V_s - V_d)^2 \frac{T}{N} + V_d^2 (N-1) \frac{T}{N} \right]$$

$$V_{off} = \left[\frac{(V_s - V_d)^2 + V_d^2 (N-1)}{N} \right]^{1/2}$$

cf Slide 10 **OFF**

$$\left[\frac{2^2 + 3}{4} \right]^{\frac{1}{2}} = \sqrt{1.75} = 1.3$$

Alt and Pleshko Criteria (3)

$$\frac{V_{on}}{V_{off}} = \left[\frac{(V_S + V_D)^2 + V_D^2(N-1)}{(V_S - V_D)^2 + V_D^2(N-1)} \right]^{1/2} = \left[\frac{\left[(V_S/V_D) + 1 \right]^2 + (N-1)}{\left[(V_S/V_D) - 1 \right]^2 + (N-1)} \right]^{1/2}$$

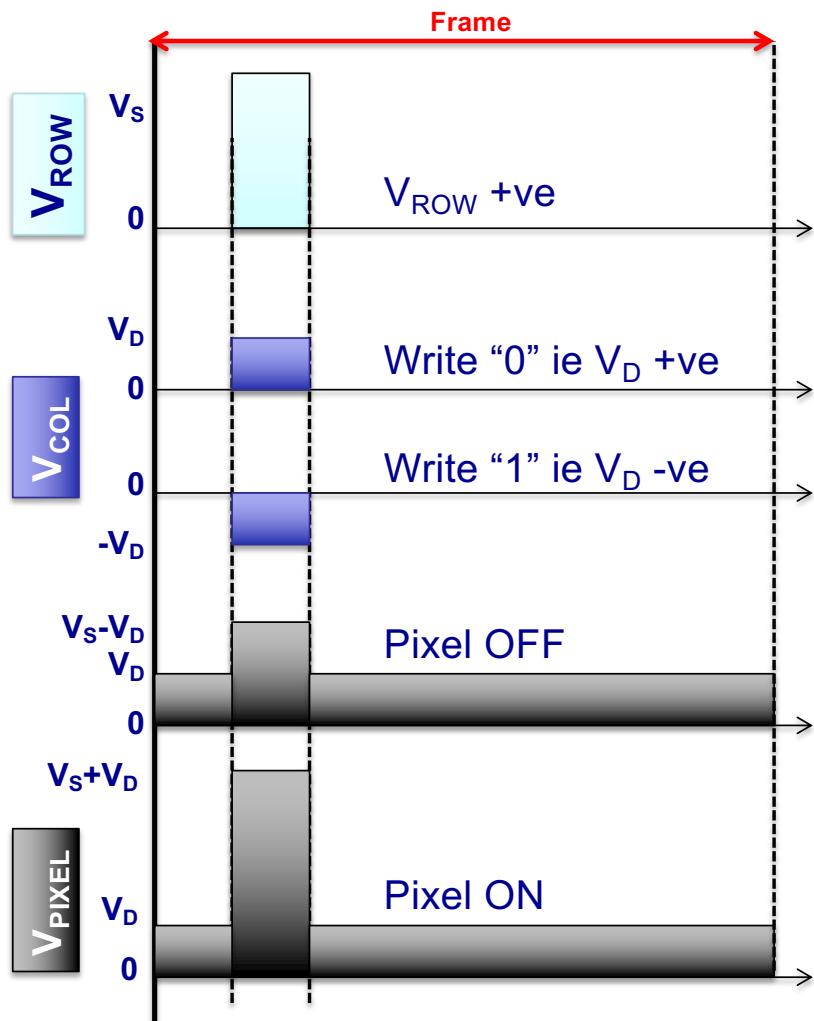
Now pose

$$u = V_S/V_D \Rightarrow \frac{V_{on}}{V_{off}} = \left[\frac{(u+1)^2 + N-1}{(u-1)^2 + N-1} \right]^{1/2} \quad \left(\frac{f}{g} \right)' = \frac{f'g - g'f}{g^2}$$

$$\frac{d}{du} \left(\frac{V_{on}}{V_{off}} \right) = 0 \Rightarrow u = \sqrt{N} = V_S/V_D$$

$$\left(\frac{V_{on}}{V_{off}} \right)_{\max} = \sqrt{\frac{\sqrt{N} + 1}{\sqrt{N} - 1}}$$

**Iron Law of
multiplexing for LCDs**



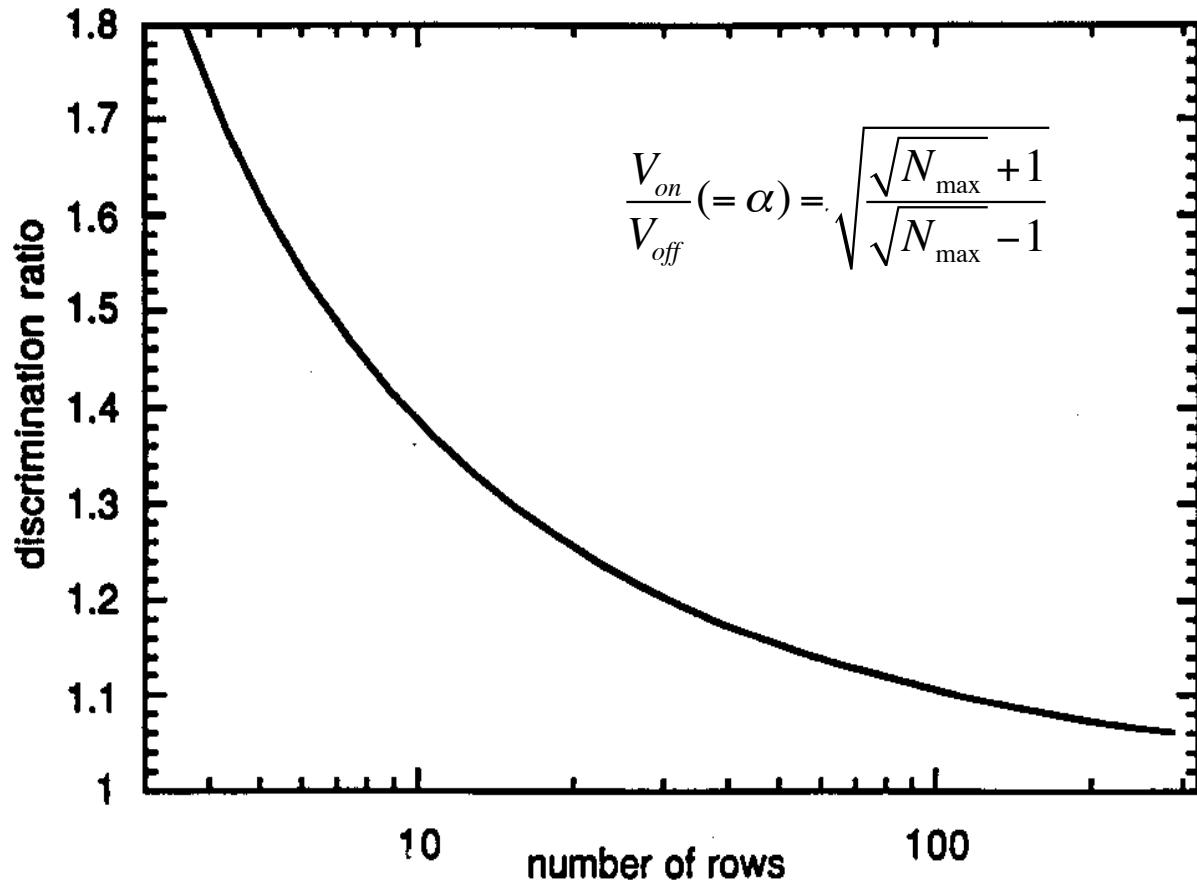
Signal to Single Pixel of $M \times N$ array for ON/OFF

Over a whole field- or frame-time -

$$V_{off}^2 = \frac{1}{N} (V_s - V_D)^2 + \frac{(N-1)}{N} V_D^2$$

$$V_{on}^2 = \frac{1}{N} (V_s + V_D)^2 + \frac{(N-1)}{N} V_D^2$$

V_{on}/V_{off} vs N (# rows) for multiplexed LCD



Alt-Pleshko Limit for Passive-Matrix Displays

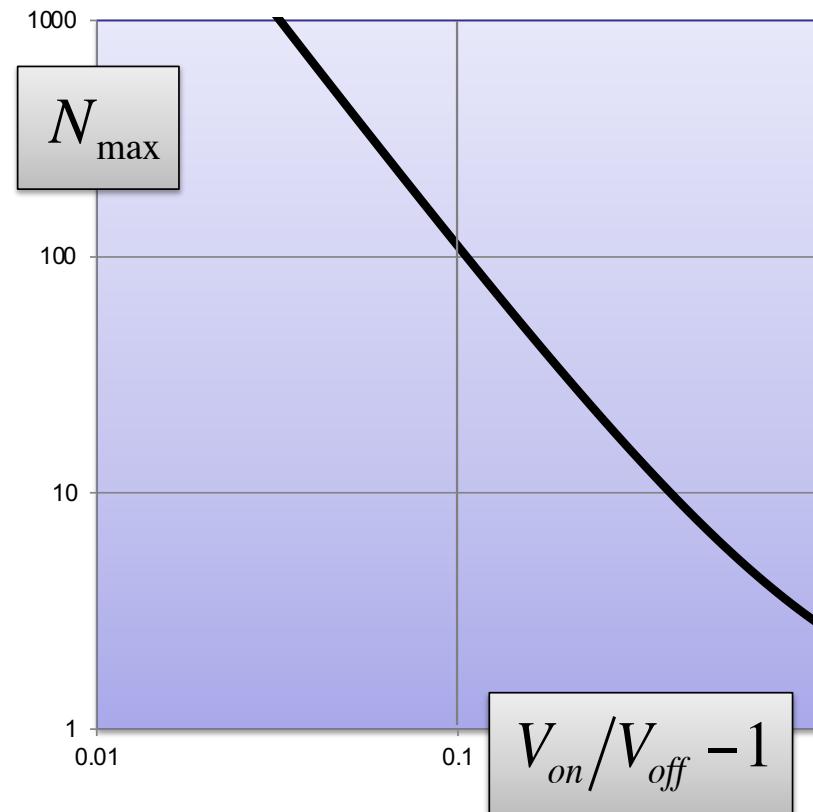
How many lines can we address?

$$\left(\frac{V_{on}}{V_{off}} \right)_{\max} = \sqrt{\frac{\sqrt{N} + 1}{\sqrt{N} - 1}}$$

Solving for N (See tutorial)

$$N_{\max} = \left(\frac{V_{on}^2 + V_{off}^2}{V_{on}^2 + V_{off}^2 - 1} \right)^2$$

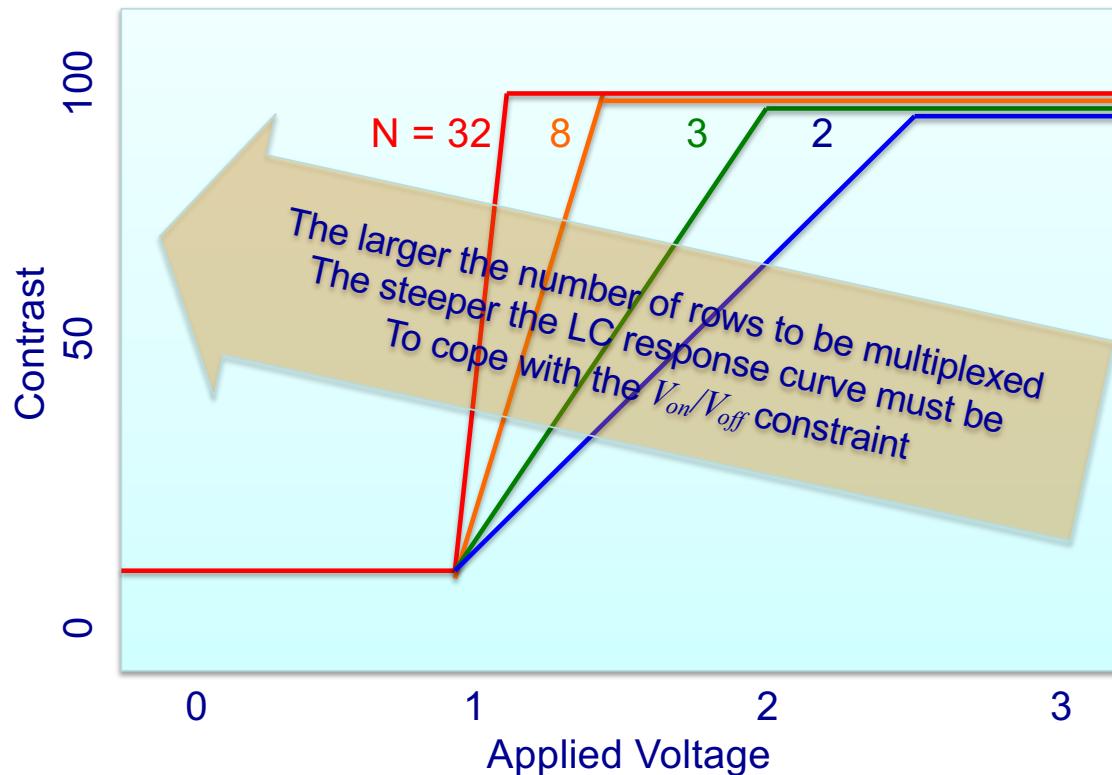
$$N_{\max} = \left(\frac{V_{on}^2 / V_{off}^2 + 1}{V_{on}^2 / V_{off}^2 - 1} \right)^2$$



Scanning limitations

$$\left(\frac{V_{on}}{V_{off}}\right)_{\max} = \sqrt{\frac{\sqrt{N} + 1}{\sqrt{N} - 1}}$$

N _{max}	V _{on} /V _{off}
2	2.41
3	1.93
4	1.73
8	1.45
16	1.29
32	1.20
100	1.10



Contrast loss when N increases

$$\alpha_{\max} = \sqrt{\frac{\sqrt{N} + 1}{\sqrt{N} - 1}}$$

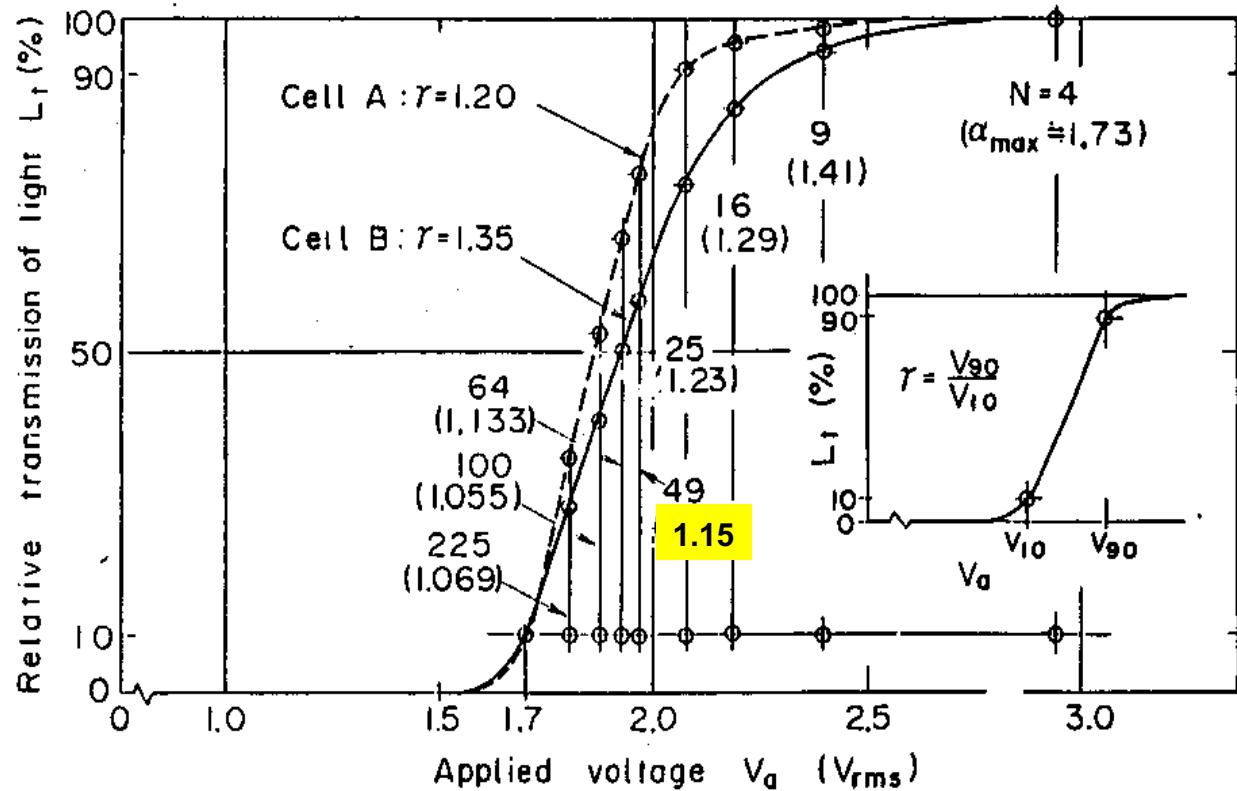
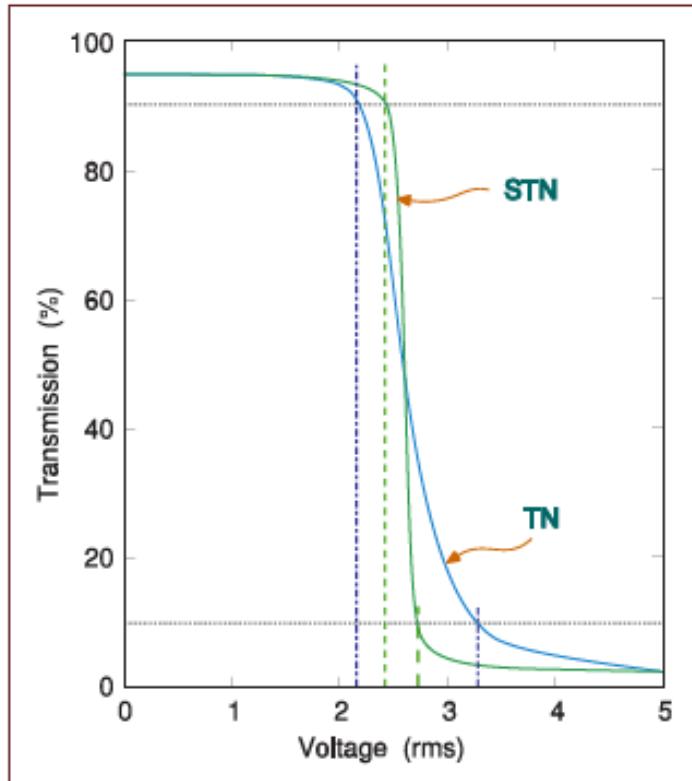


Fig. 4.9. Relation between light transmission ranges and number of scanning electrodes of two liquid crystal display panels.

Beating A&P - Super Twist Nematic LC



TN
90° twist
 $V_{10}/V_{90} = 1.6$

STN
180° - 270° twist
 $V_{10}/V_{90} = 1.06$

**Improved STN
LC material**

IMPORTANT
 $V_{90} = V_{OFF}$
 $V_{10} = V_{ON}$

Super Twist Nematic (STN) has much steeper response than regular TN
This allows many more rows to be addressed (see slide 21)

Beating A&P - Dual Scan Addressing

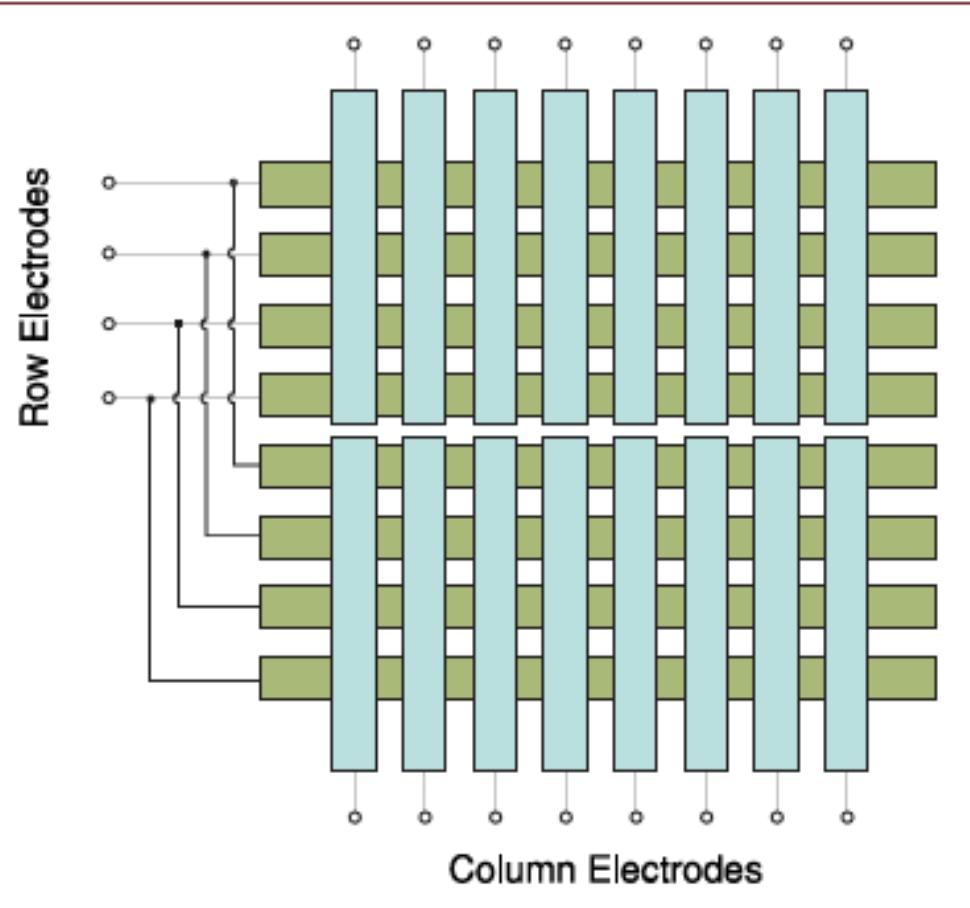
Address pixel matrix as follows

- One half of rows from top
- Other half from bottom

ie

2 half-matrices
each of $N/2$ rows
 $= M \times N/2$ pixels

Multi-line addressing is another potential solution
but is not covered here



Matrix layout for doubled vertical resolution

Passive Matrix LCD

Advantages of passive matrix

- more lines than segmented
- Lower cost substrate than active matrix

Disadvantages of passive matrix

- Limited number of lines of definition
- As number of lines rises
 - Limited contrast as more lines
 - Crosstalk between pixels
 - More stringent requirements on drive waveforms
 - Severe requirements on LC materials

Passive Matrix Addressing - Summary

Review

- Explanation of PM addressing
- Derivation of Alt and Pleshko Criteria leading to
- Significant constraints of PM
- Work-arounds
- Summary



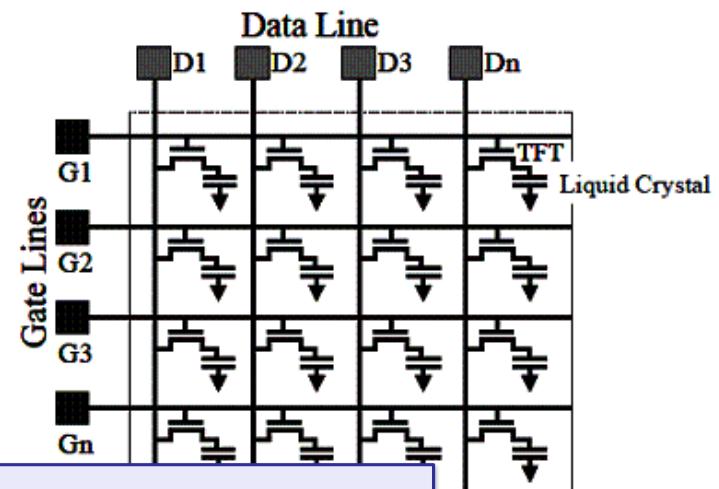
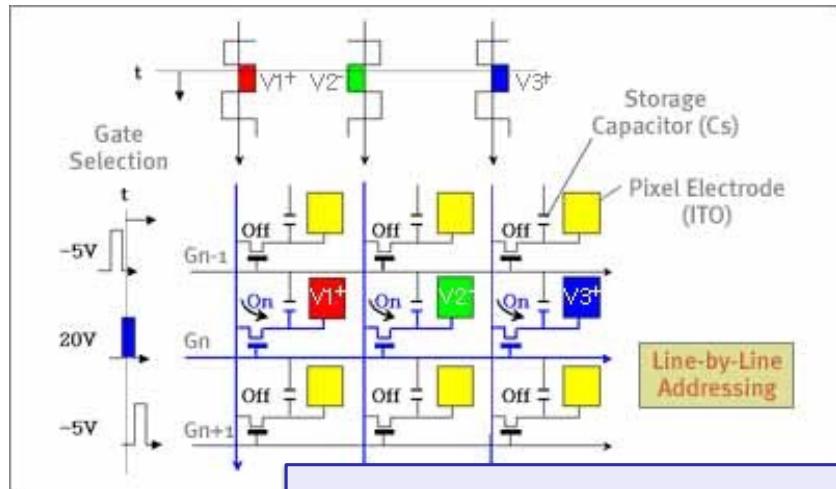
Comment

- Today's lecture has introduced some quite new concepts
- Please take time to familiarise yourself and absorb the new material

Additional Resources

- HBVDT is limited on analysis of PM LCD
- I have loaded Chapter 2 of Lueder (2022) on to Learn
 - *I strongly recommend that you study it*

Next lecture – Active Matrix (AM) LCD



S5. ACTIVE MATRIX LCD ADDRESSING AND ELECTRONICS

Why AM

Aim of AM

Principles

Electronic subsystems

Timing

Waveforms

Kickback

Why active matrix addressing?

REVIEW CONSTRAINTS OF PM ADDRESSING

Passive matrix is

- (In principle) simple
- Uses low-tech, low-cost backplane technology

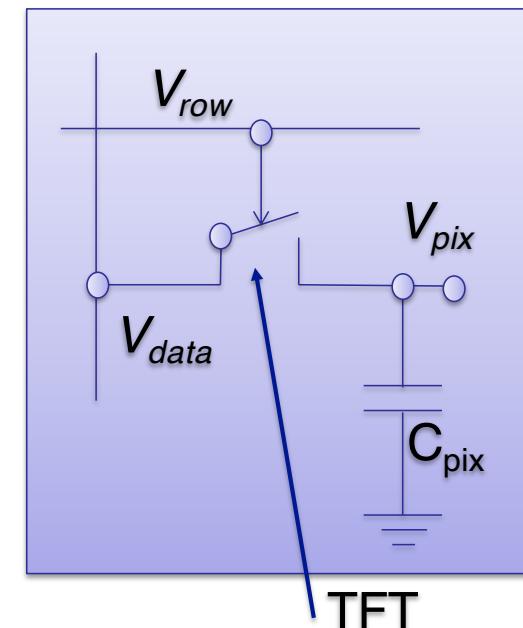
But due to low duty cycle and crosstalk

- Requires very sophisticated drive waveforms
- Still cannot drive very large numbers of rows
 - Each row of pixels is “intentionally” addressed for at most $1/n$ of the frame time (where n = number of rows)
 - Each row of pixels is subject to the data signals that drive the other rows of pixels (for $(n-1)/n$ of the frame time)

The Aim of Active Matrix Addressing

The aim of AM Addressing is to overcome the limitations of PM Addressing by

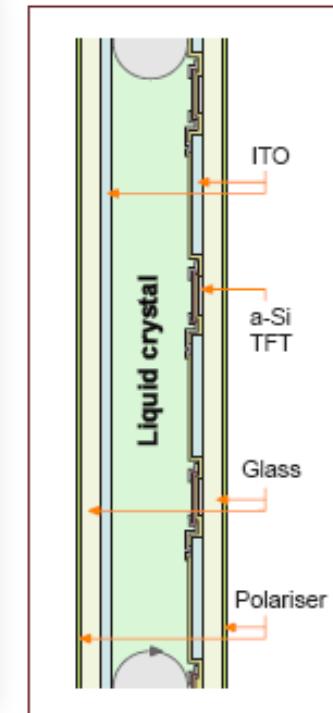
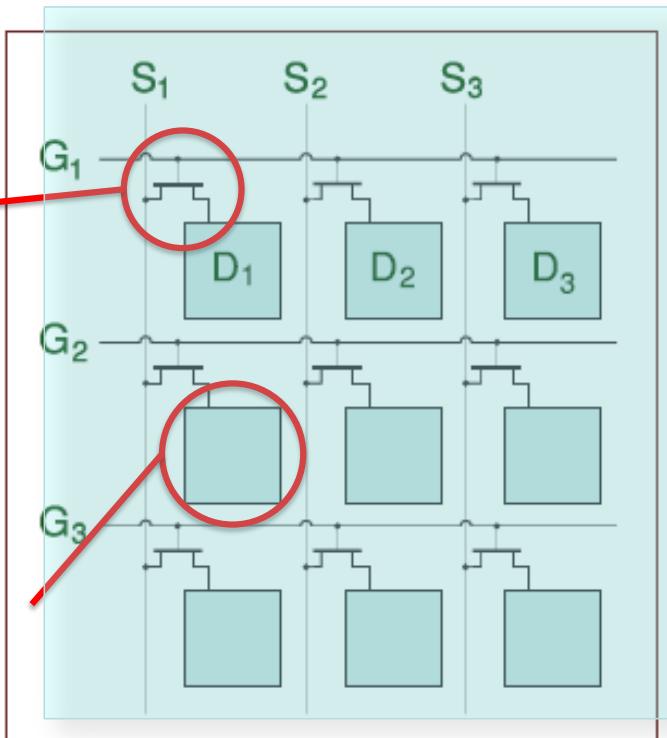
- Increasing the duty cycle
 - Putting the drive signal into the pixel electrode during a line-addressing time and keeping it there for all or most of the frame time
- Reducing cross-talk
 - Isolating the pixel electrode from the effect of signals driving pixels in other rows
- In short we need a non-linear element in each pixel
 - In practice this is frequently implemented as a “sample-and-hold” circuit as show



Active Matrix

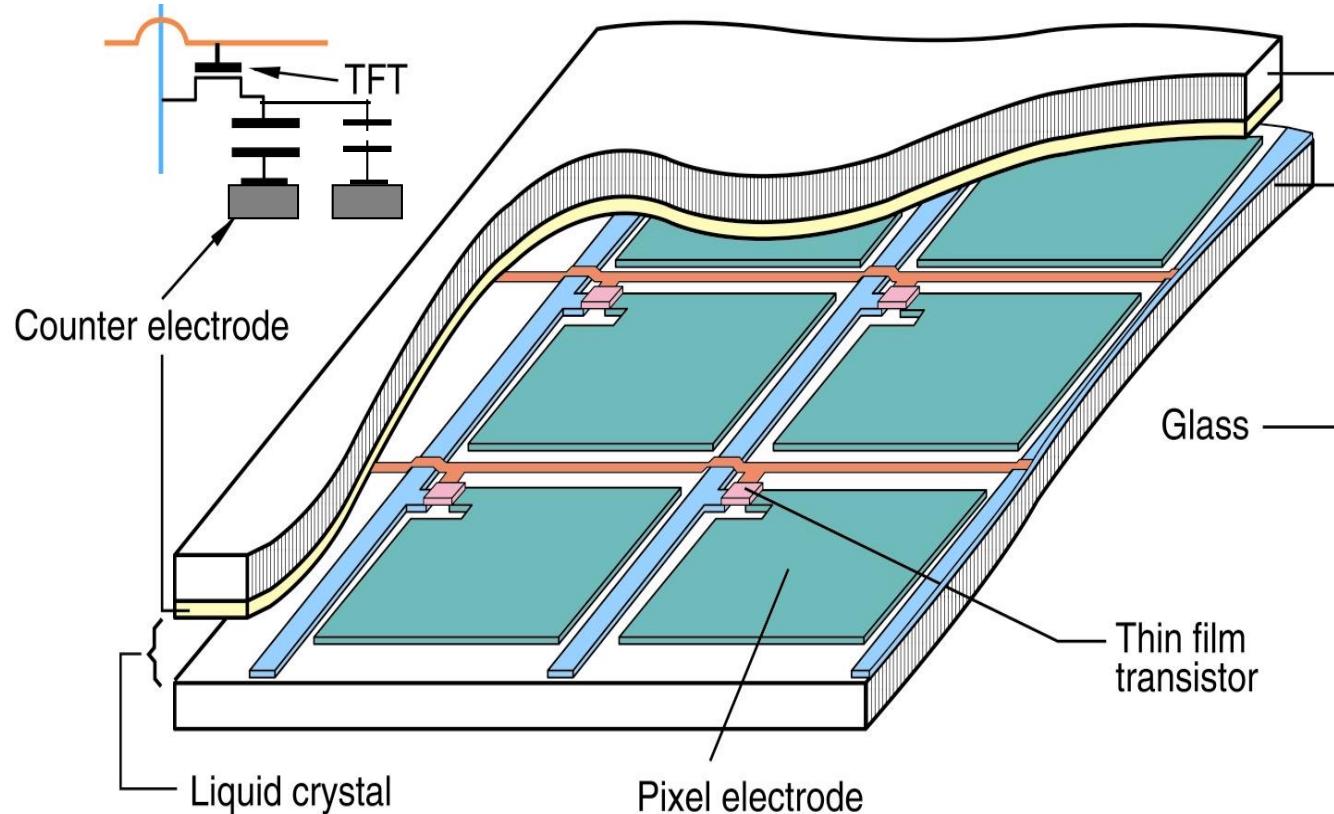
Row and column electrodes on active (back) substrate
Common electrode on front substrate
Switch = TFT

- Active switch and storage element per pixel isolates electronic addressing of pixel from drive EO element
- Per row / column Storage Cap =
 - One driver pixel electrode
 - One connecting wire
- $M \times N$ pixels requires only $M+N$ drivers



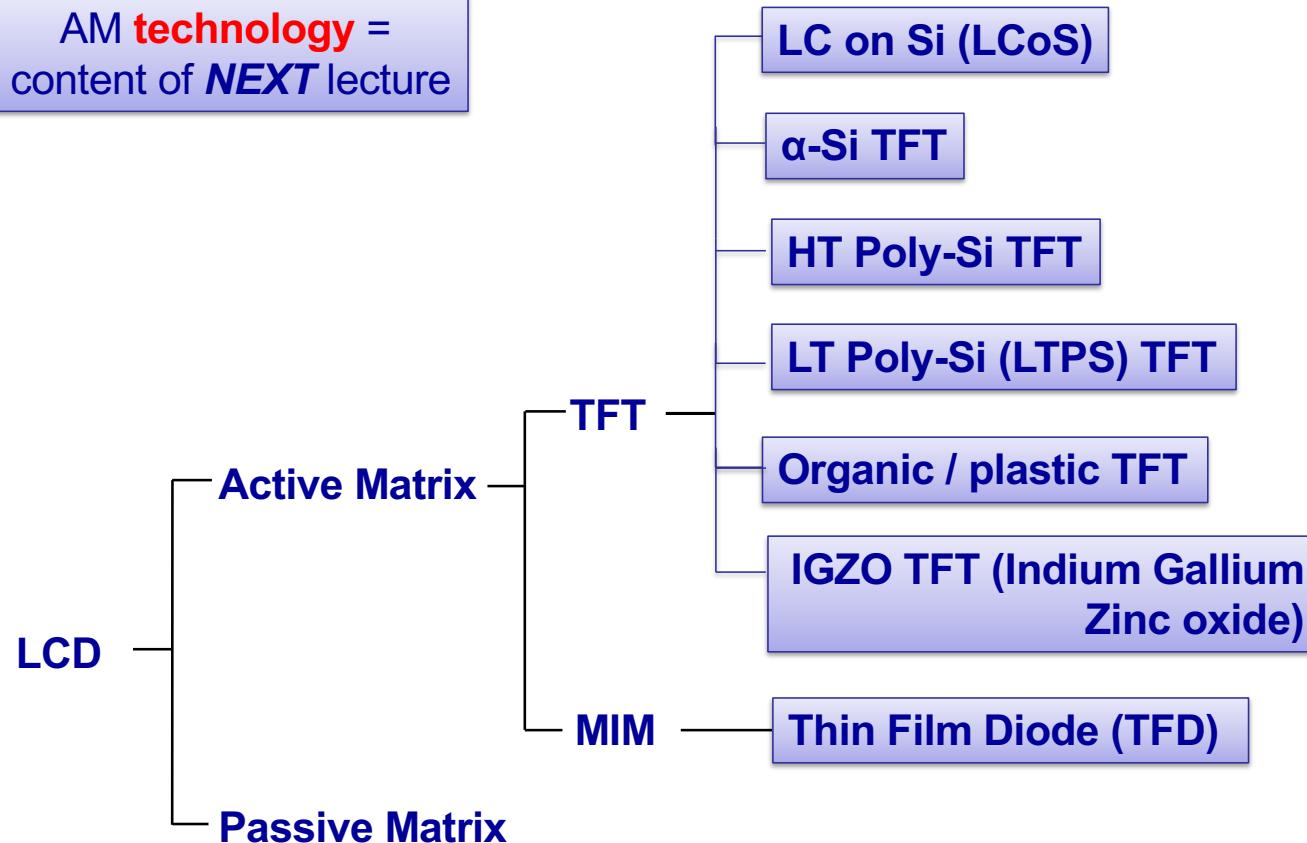
Active matrix LC display

TFT-LCD Exploded View

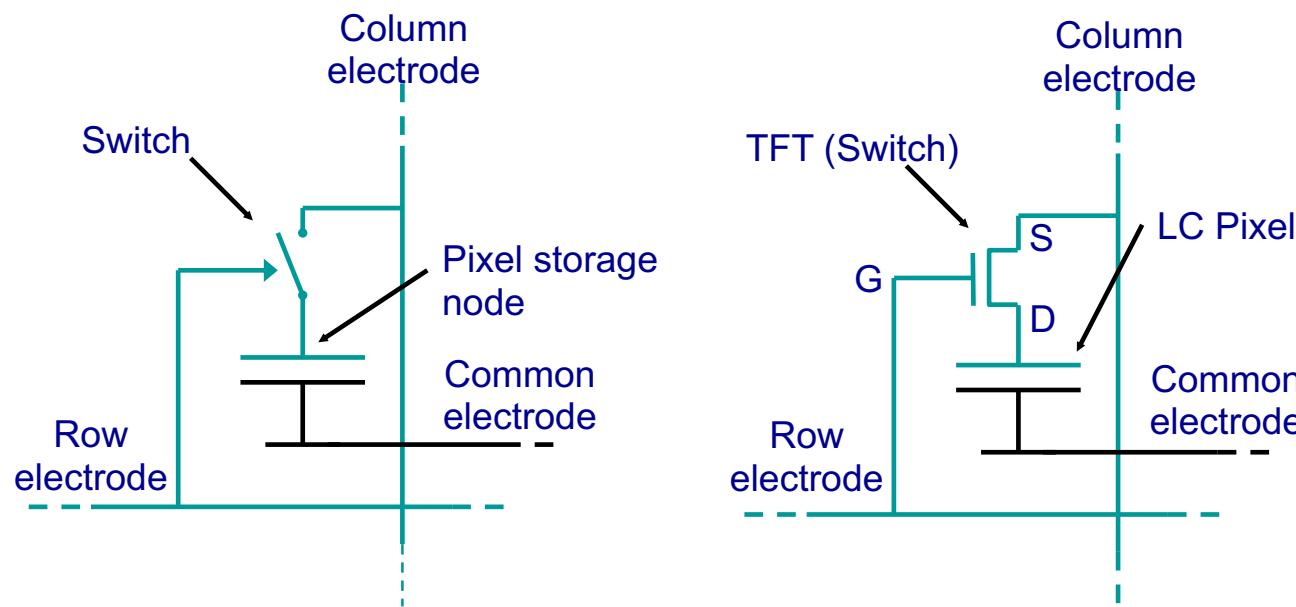


Active Matrix Technologies

AM technology =
content of **NEXT** lecture



AM Pixel Circuit

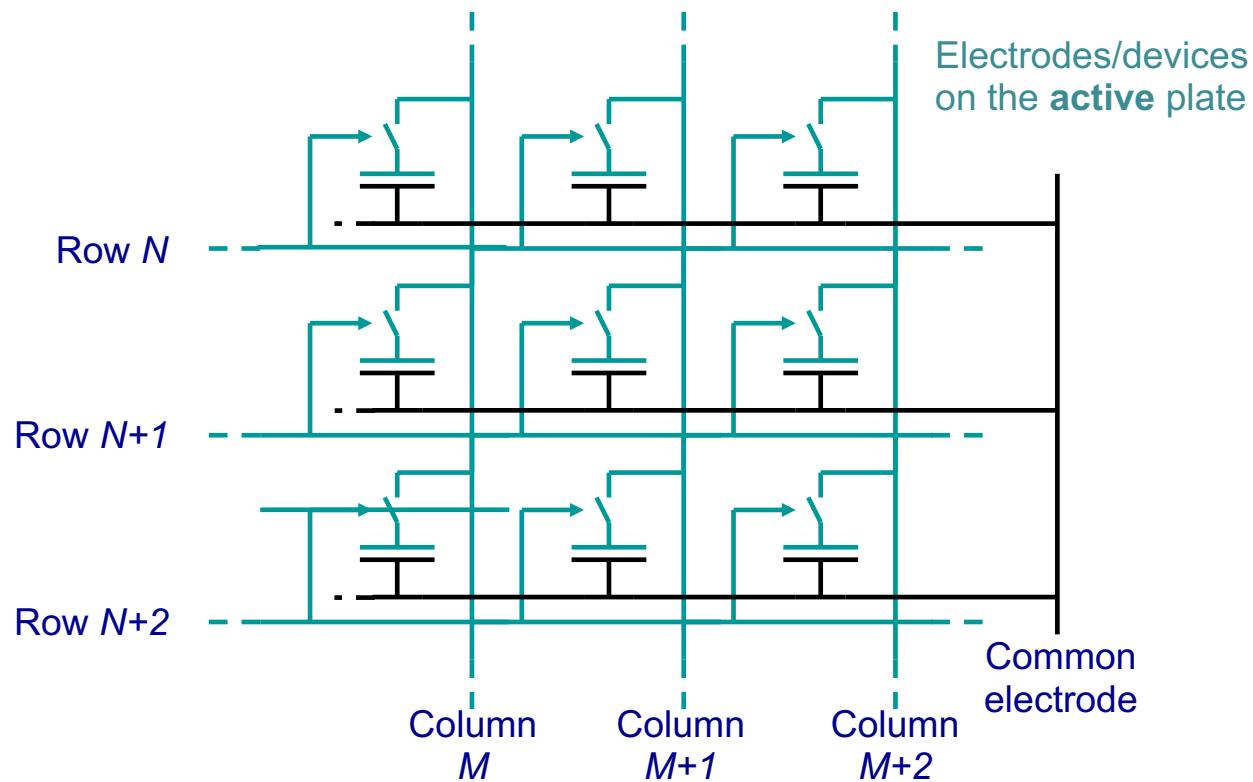


Active Matrix Addressing

- Reduces crosstalk
- Simplifies addressing waveforms
- Increases pixel drive time from $1/N$ of field time to \sim field time
- Allows more rows of pixels

DM-MJR

Active Matrix Structure



Row Sequential Addressing 1/5

Each row of pixels is addressed in sequence

Pixel data is applied to the column electrodes

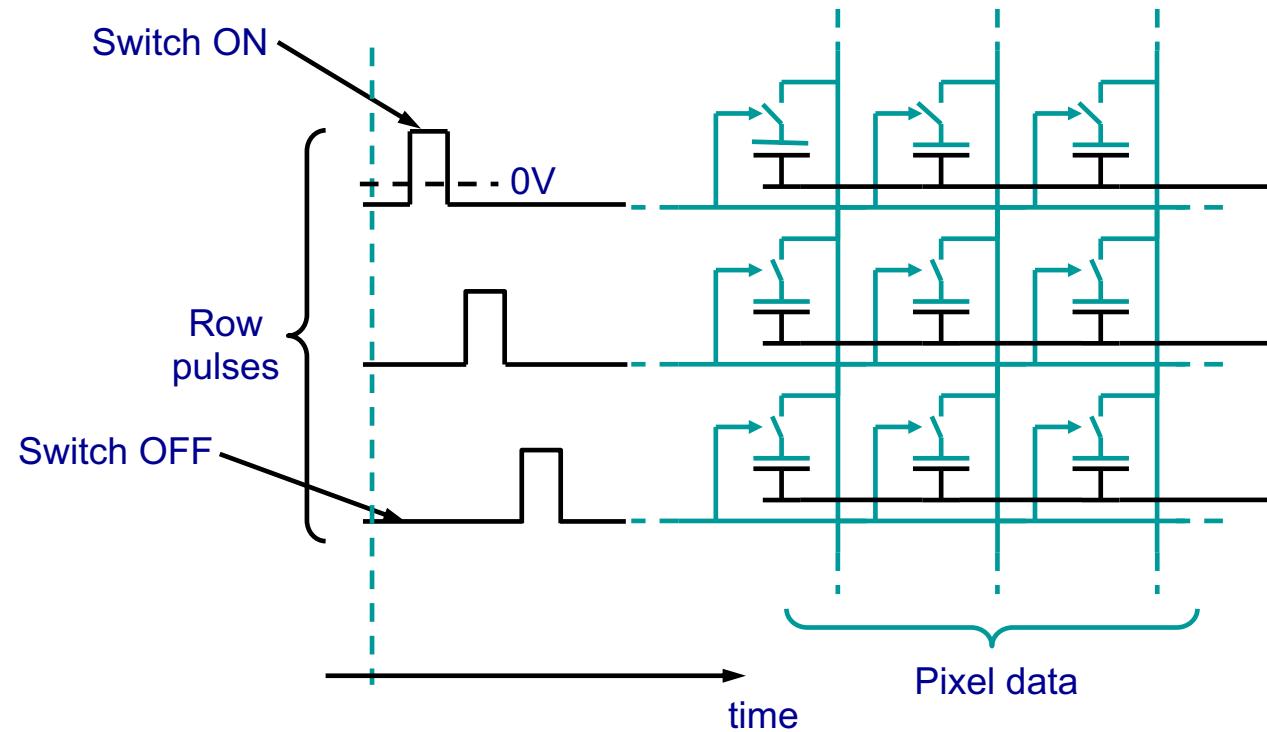
Column data is transferred into a row of pixels

- Achieved by applying a pulse to the row electrode
- Closes the switches (turns the TFTs on)
- Charges up the pixel capacitance, C_{LC}

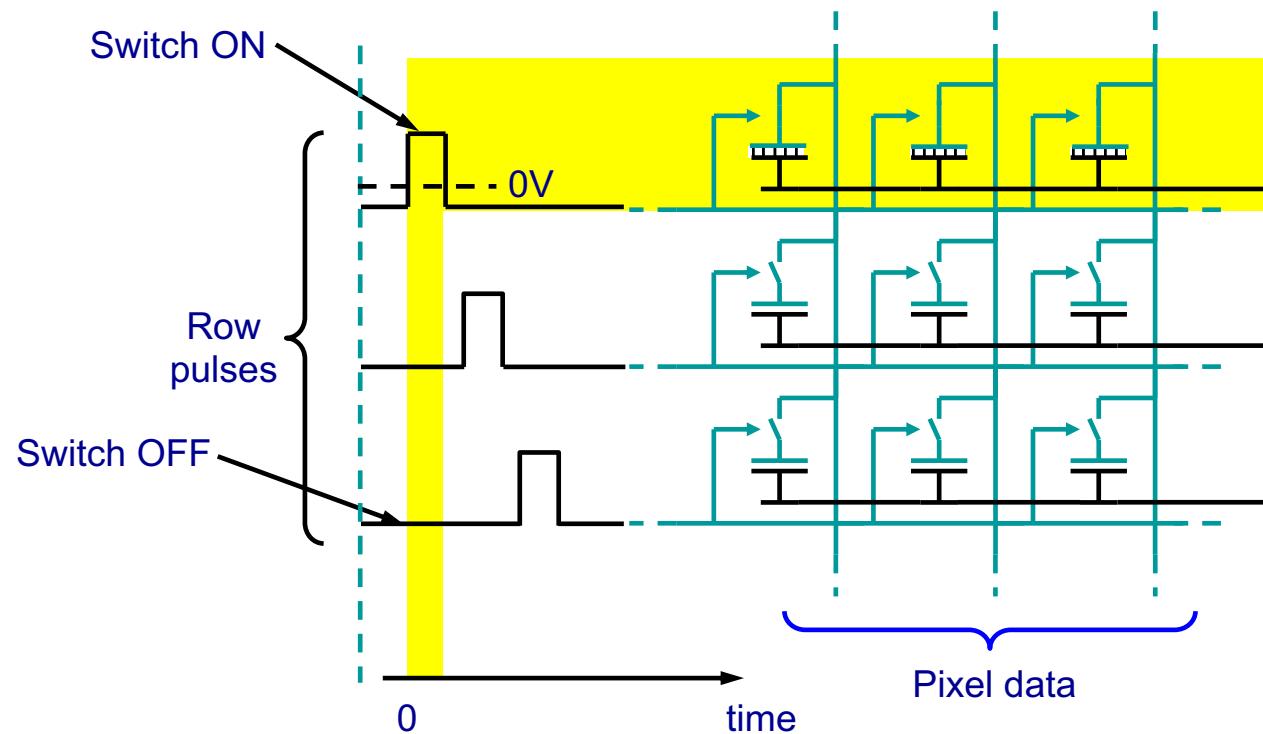
When pixel is charged the TFT switch is opened

- Pixel capacitance is isolated
- Charge remains on pixel

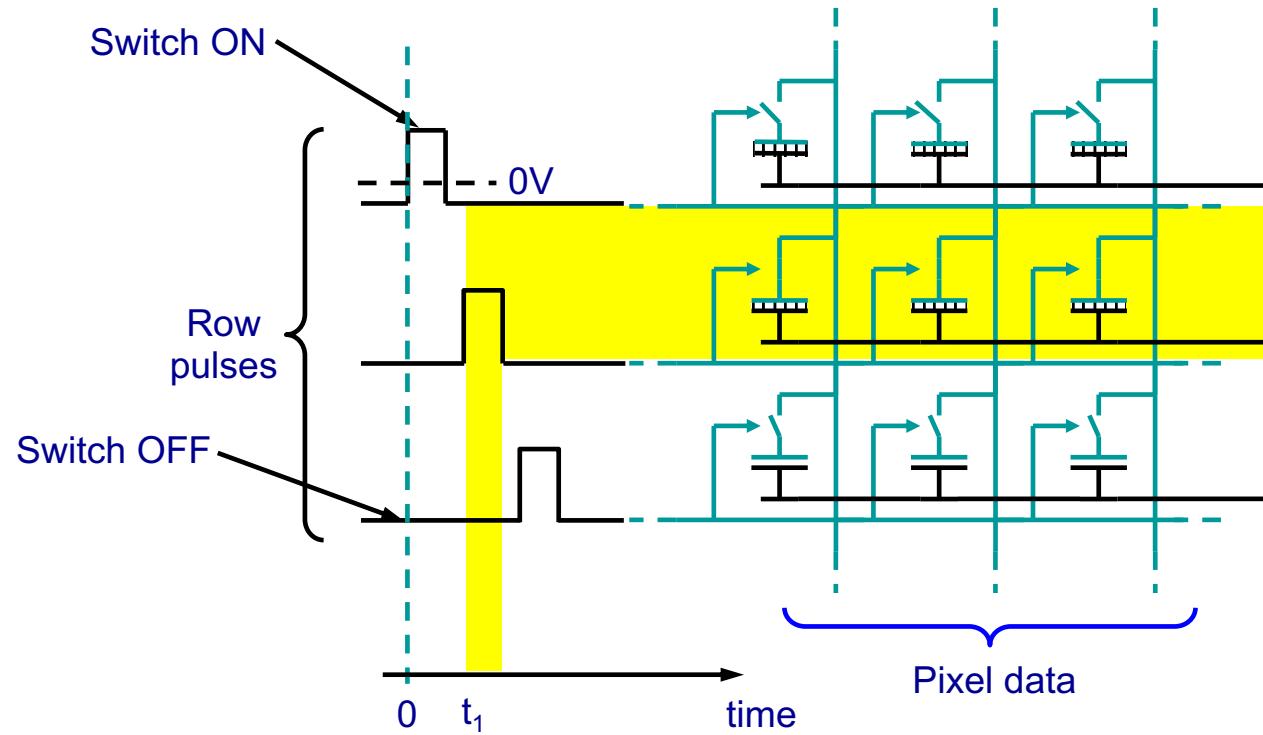
Row Sequential Addressing 2/5



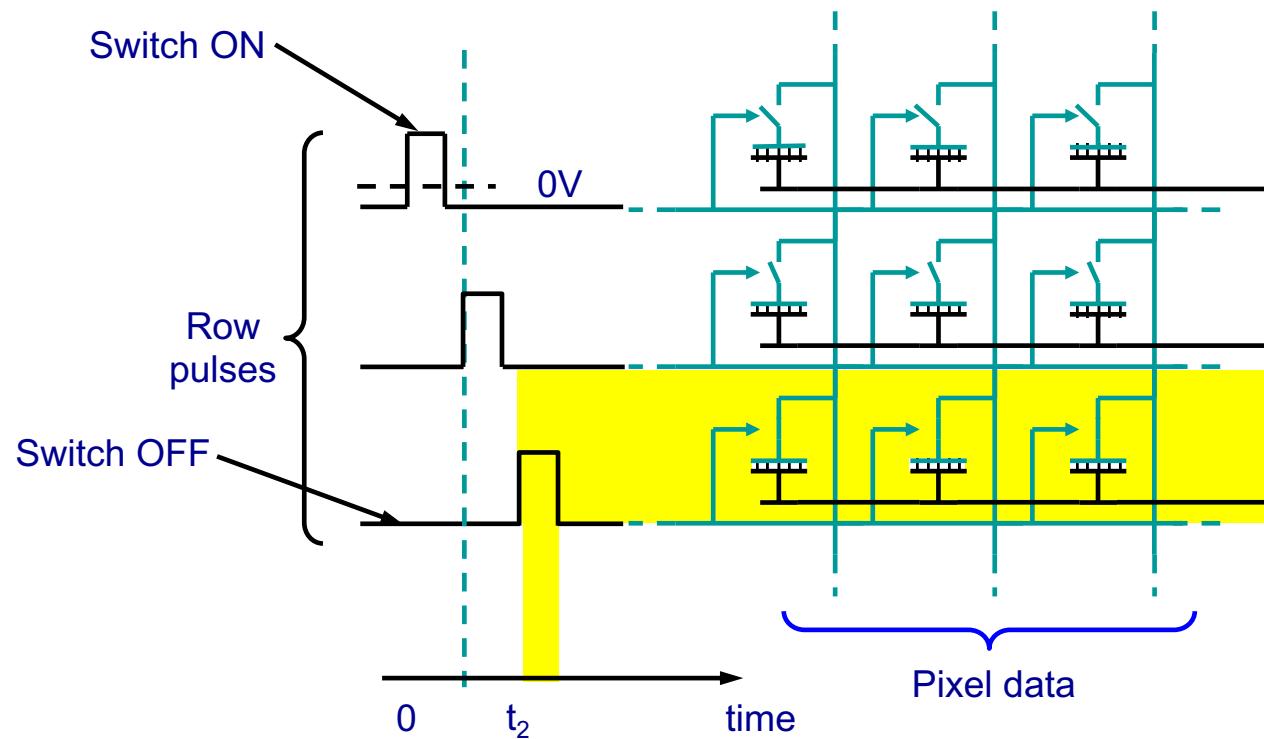
Row Sequential Addressing 3/5



Row Sequential Addressing 4/5



Row Sequential Addressing 5/5



AM LCD Module (including backlight)

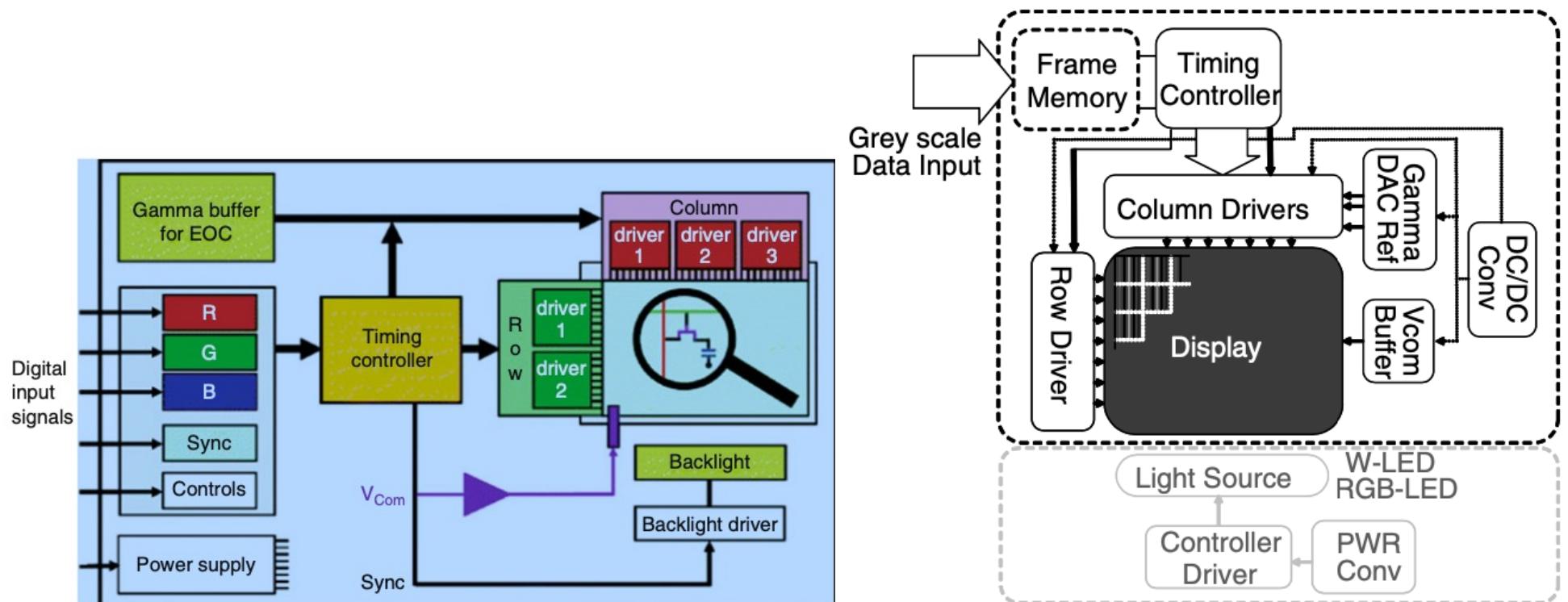


Figure 9.3 The major functions within an Active Matrix LCD

Panel Interface Timing

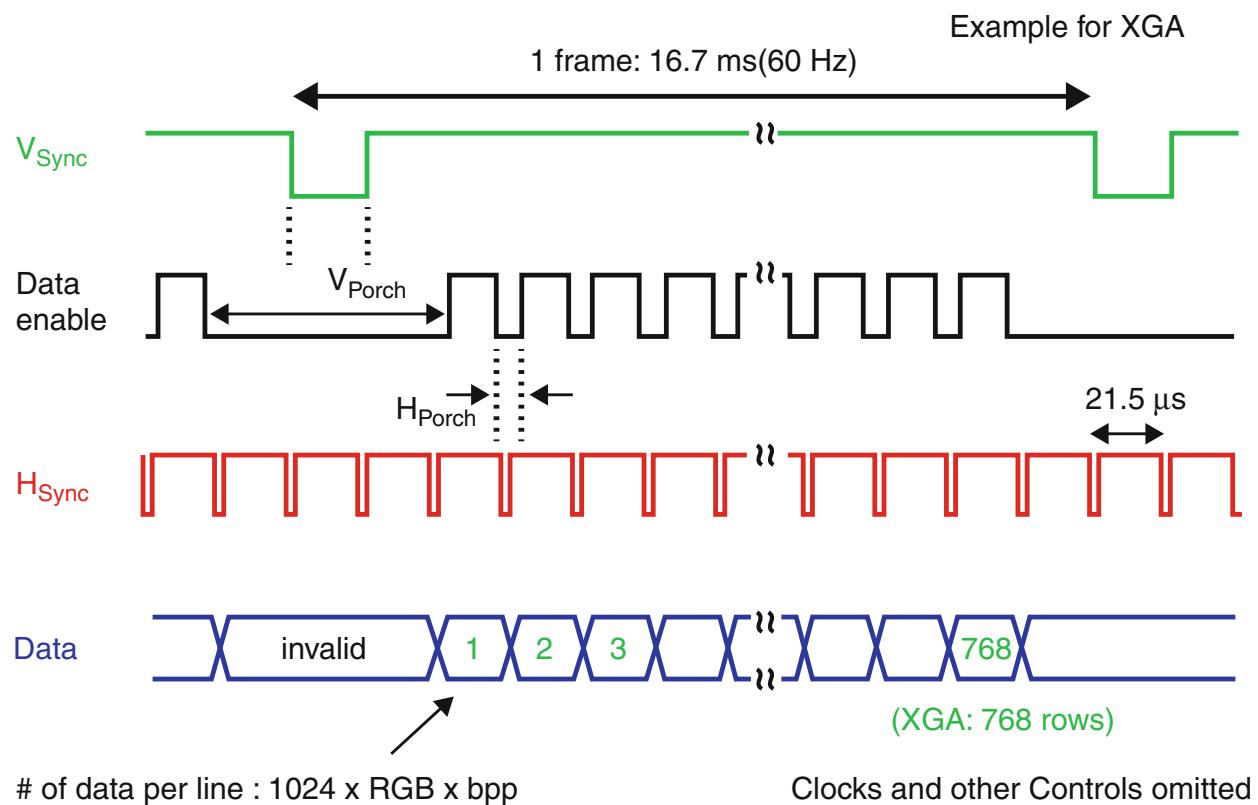


Fig. 2 Typical example of parallel panel interface timing which is practically the same for Timing Controller data input (for details see section “[Timing Controller and Intrapanel Interface](#)”)

LCD Timing Controller

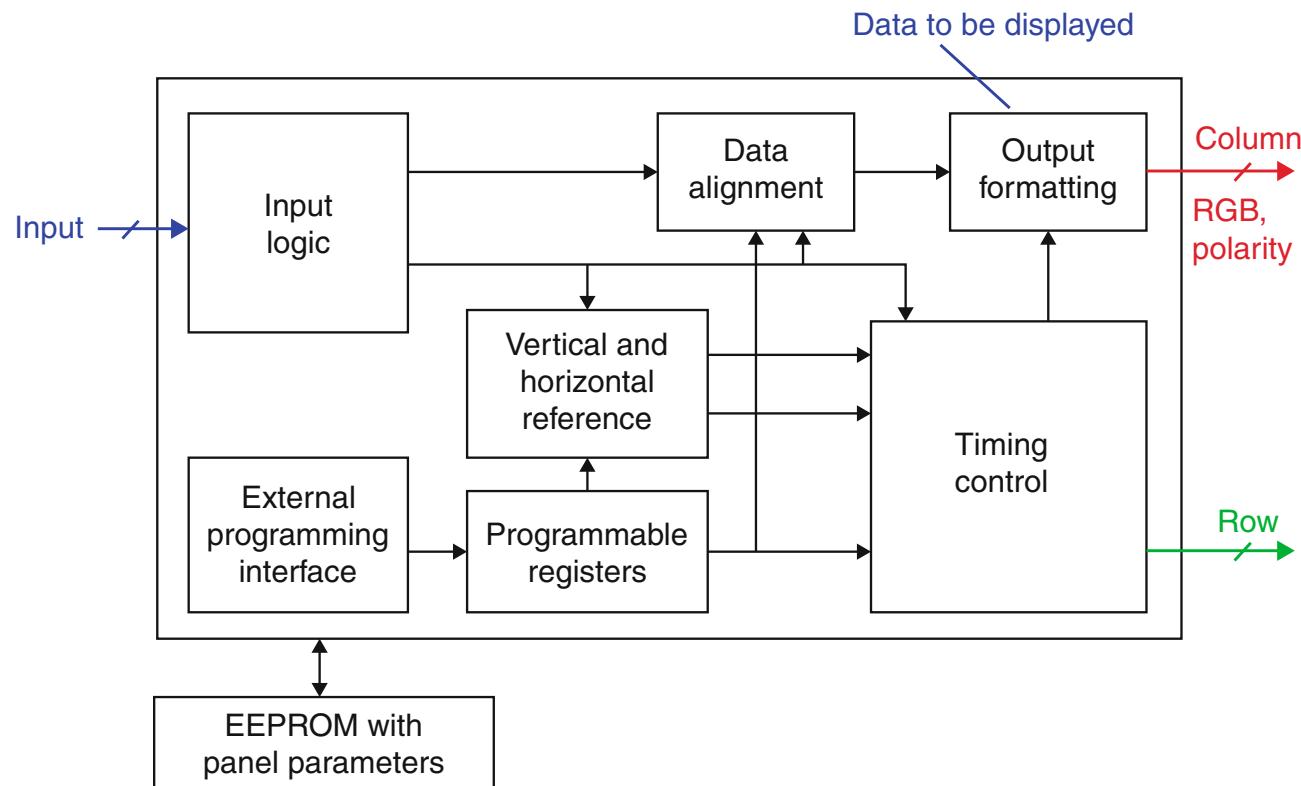
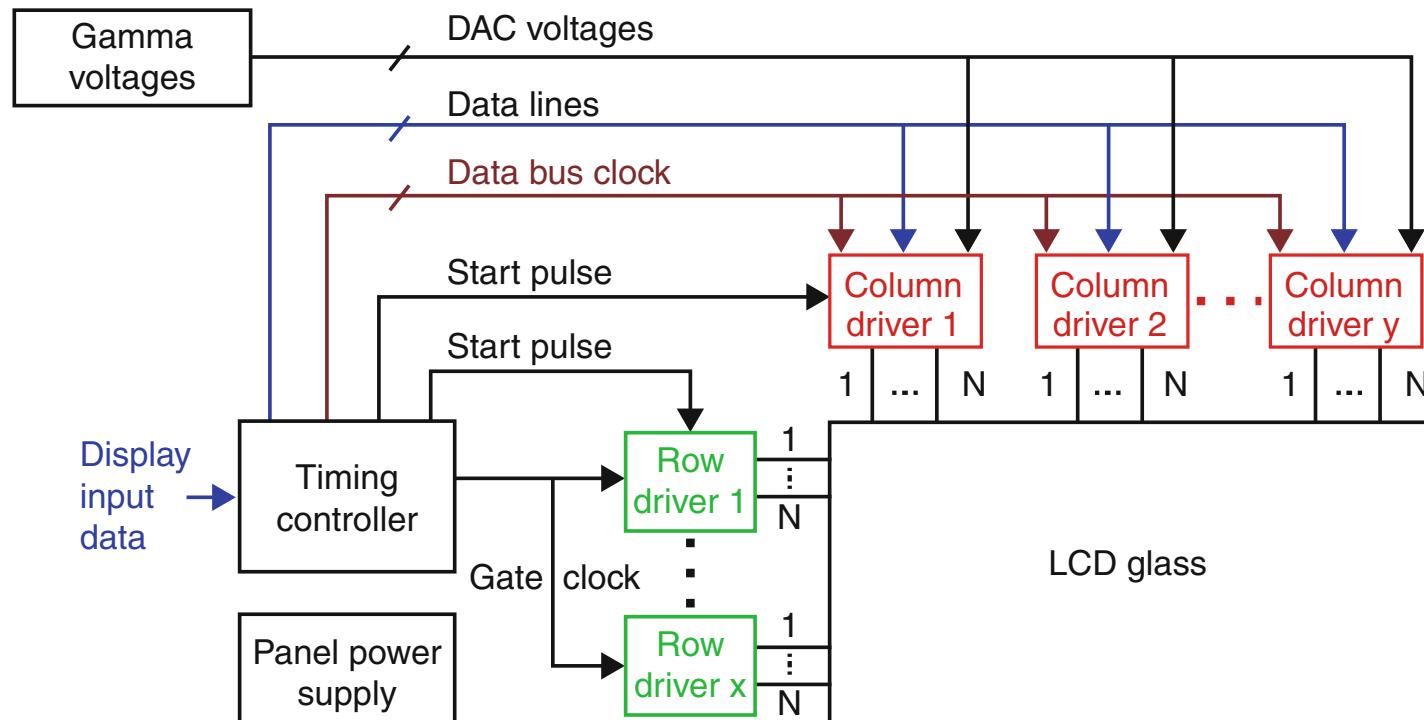
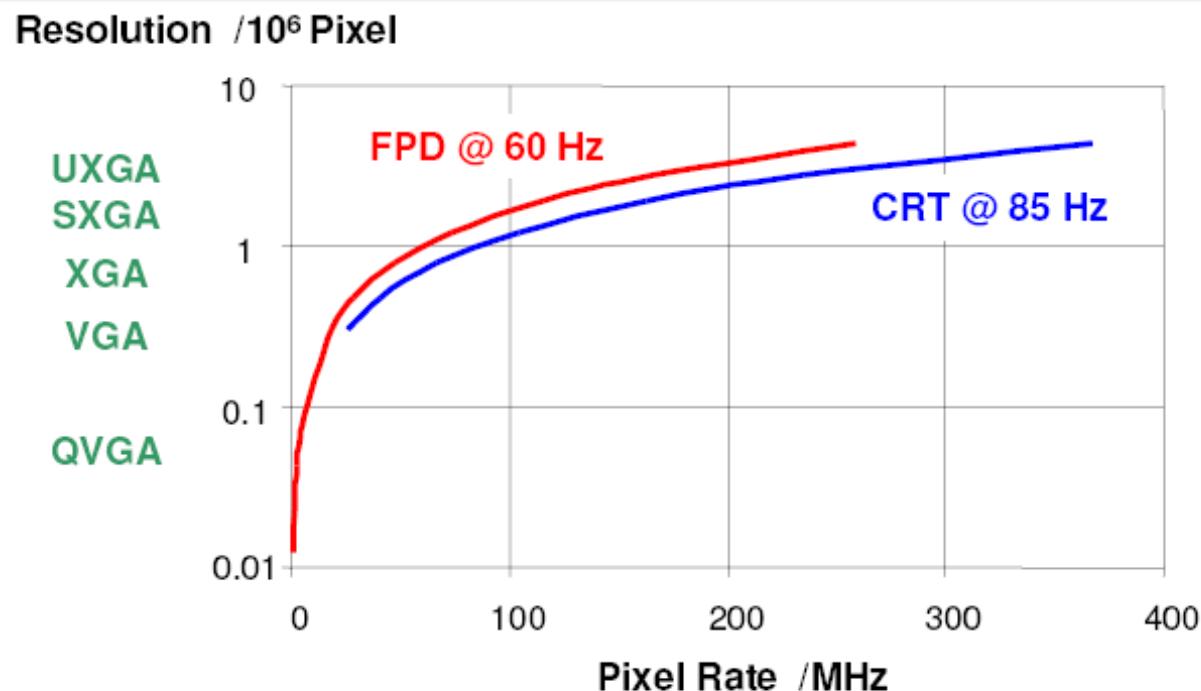


Fig. 4 Simplified block diagram of an LCD Timing Controller with its inputs and outputs

Panel Electronics



Data Rates



Pixel frequency = Resolution x Frame frequency (limit for parallel interfacing)

Data rate = Pixel frequency x RGB x Colour depth (limit for serial interfacing)

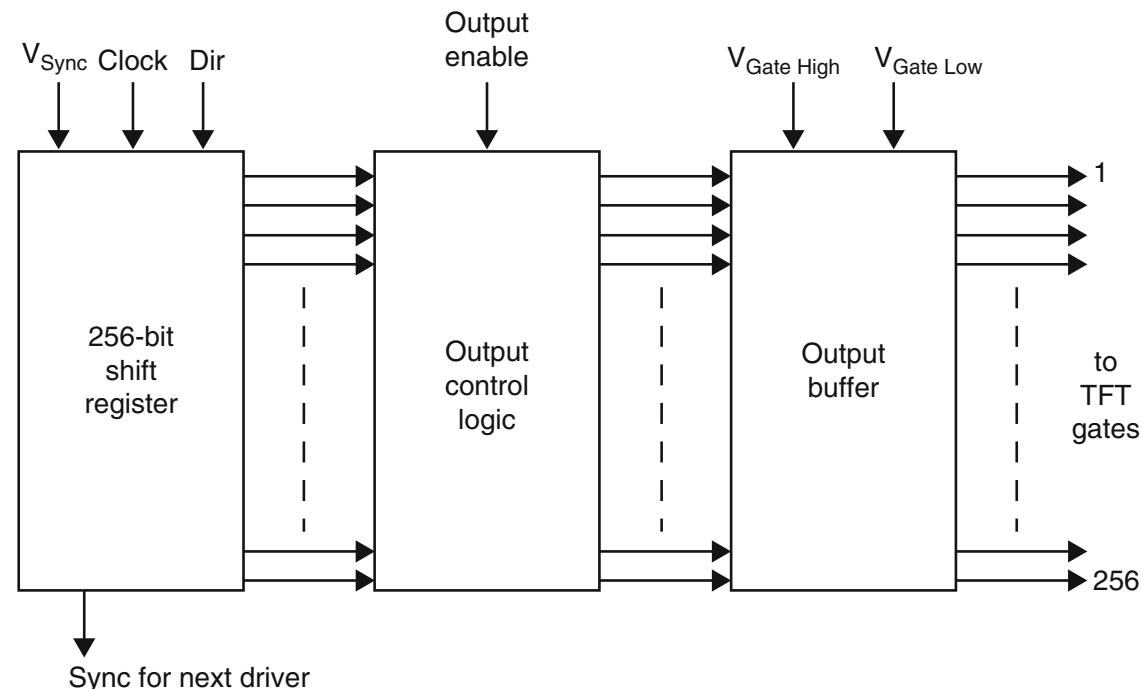
Row Driver and Timing

Shift register passes token

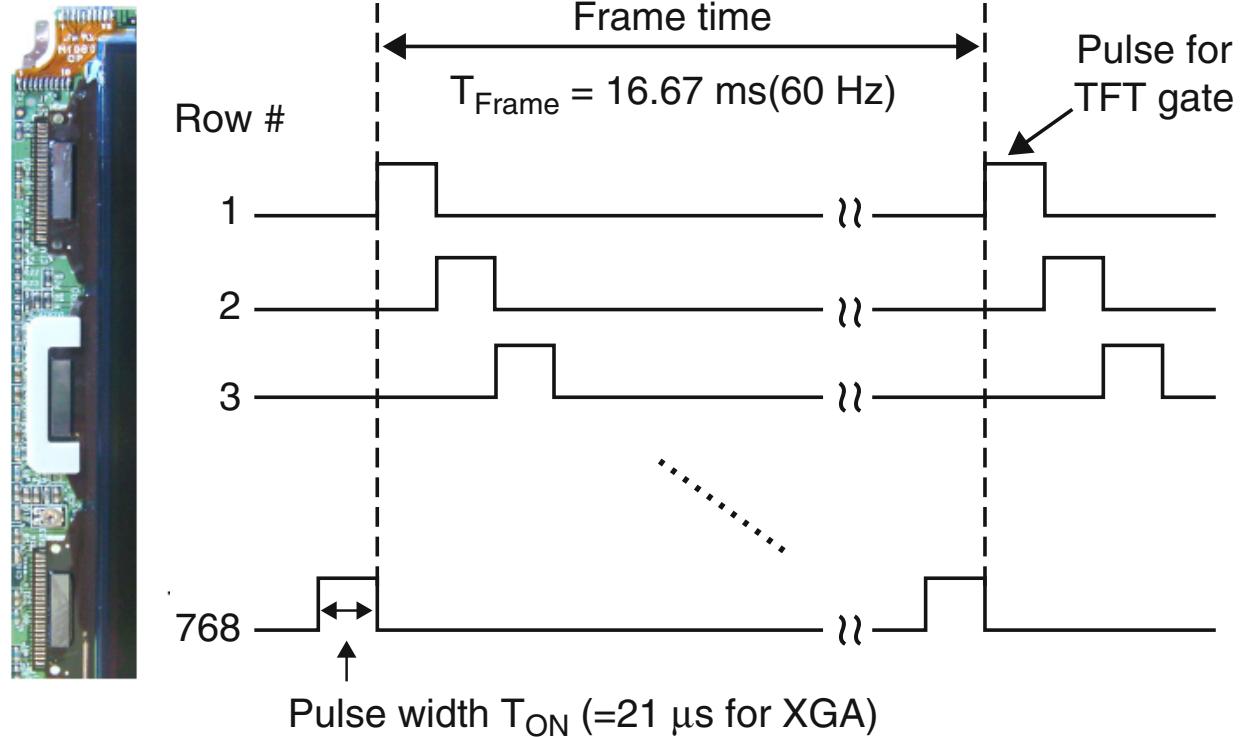
Token determines which row is active

Dir sets scan direction

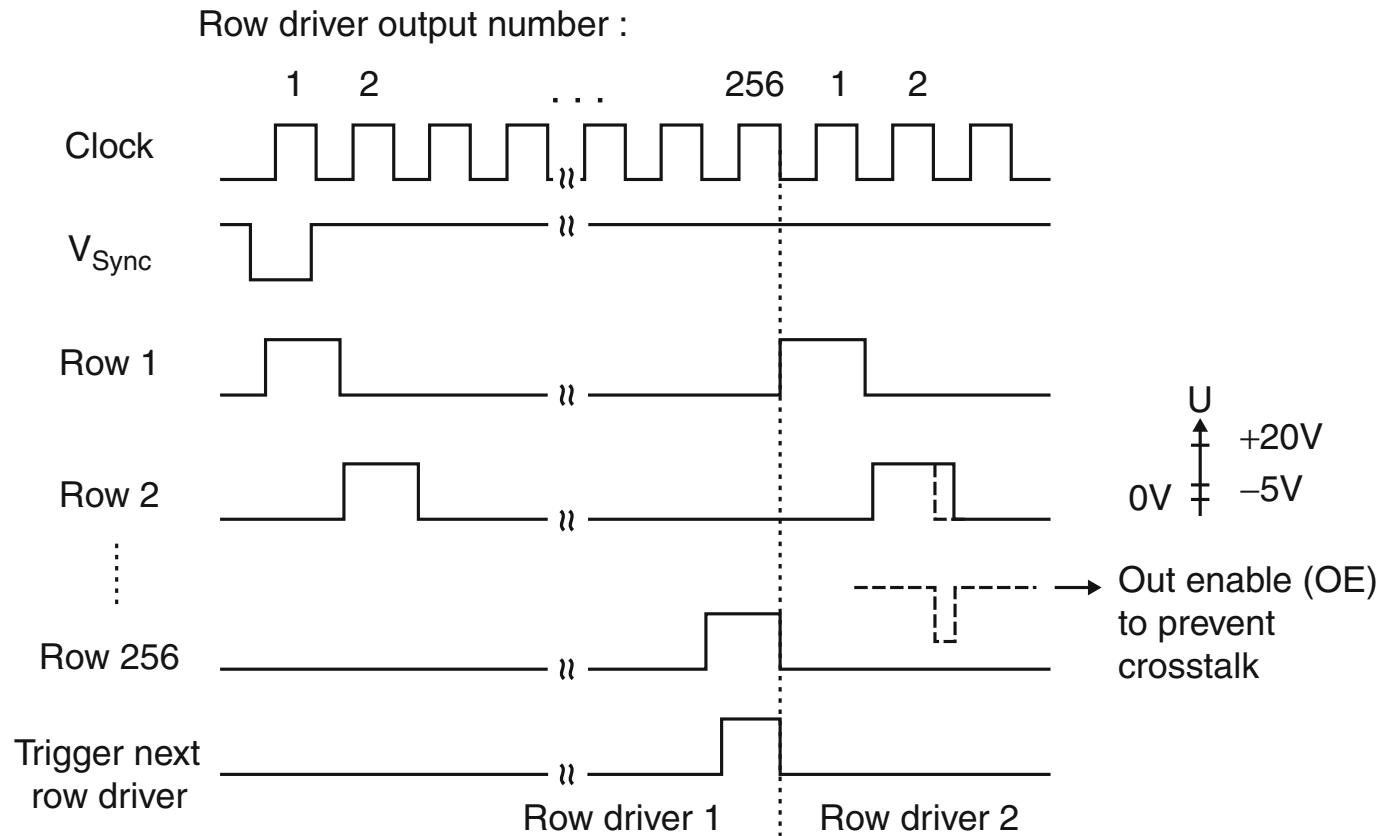
Output enable cuts gate voltage before next line to prevent cross-talk



Row Driver Timing Diagram



Row Driver Timing Diagram



Example Column Driver

Example shown is

- Digital in, analog out

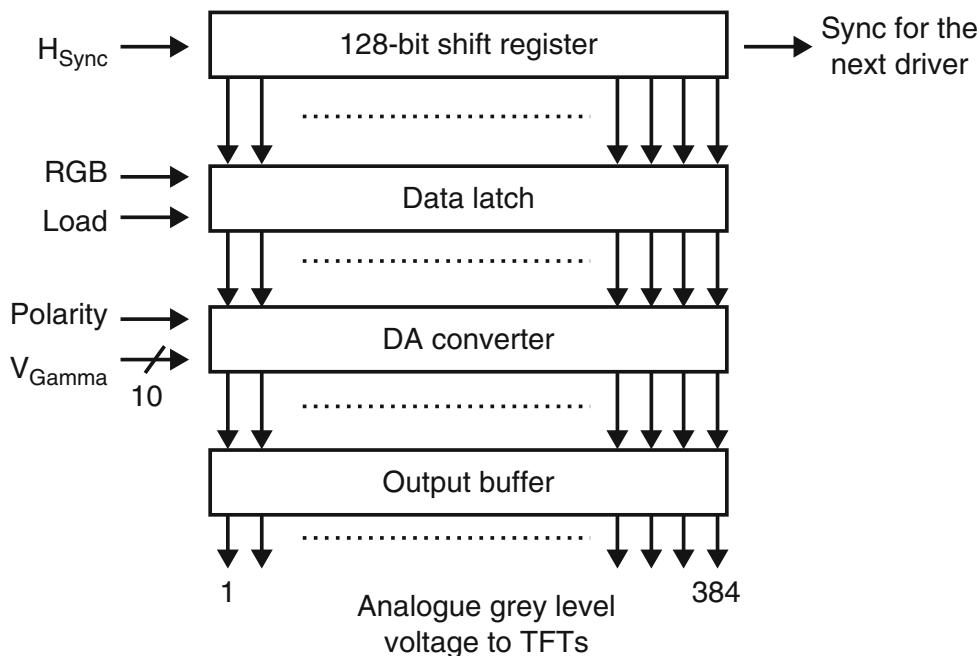
Could also be

- Digital in, digital out
- Analog in, analog out

Polarity for inversion

V_{gamma} for EO TF

Clocks etc not shown



Column driver timing diagram

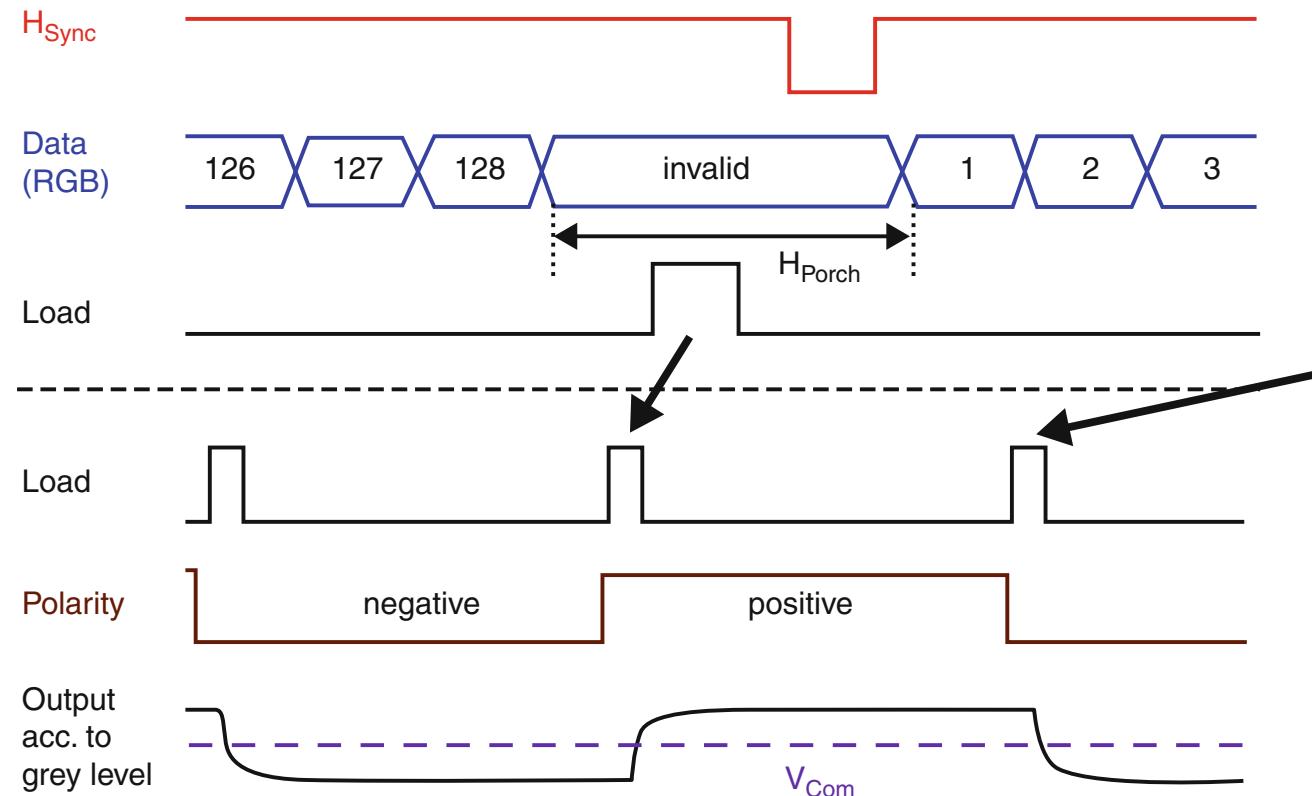
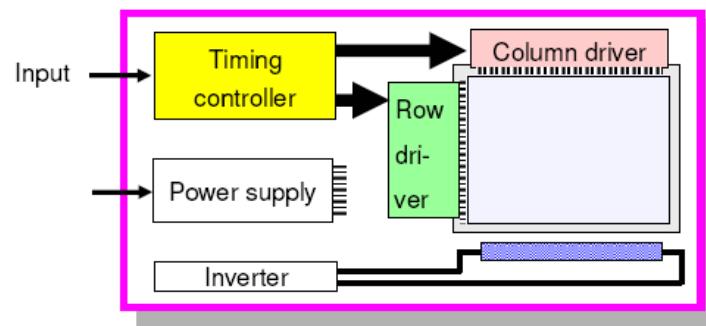


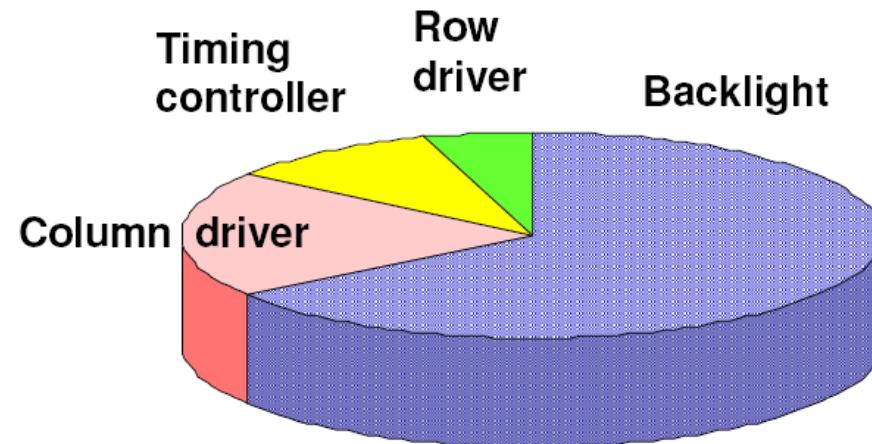
Fig. 11 Typical timing diagram (clock and some control signals omitted) of an XGA AMLCD column driver

Power Budget



LCD module

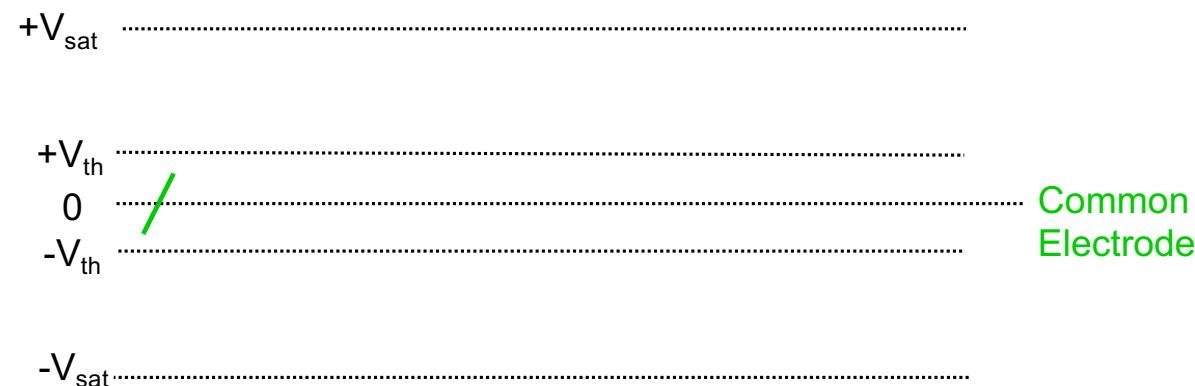
Electronics draw ~ 1/3
of total power consumption !



Example for 10.4" VGA Colour AM LCD

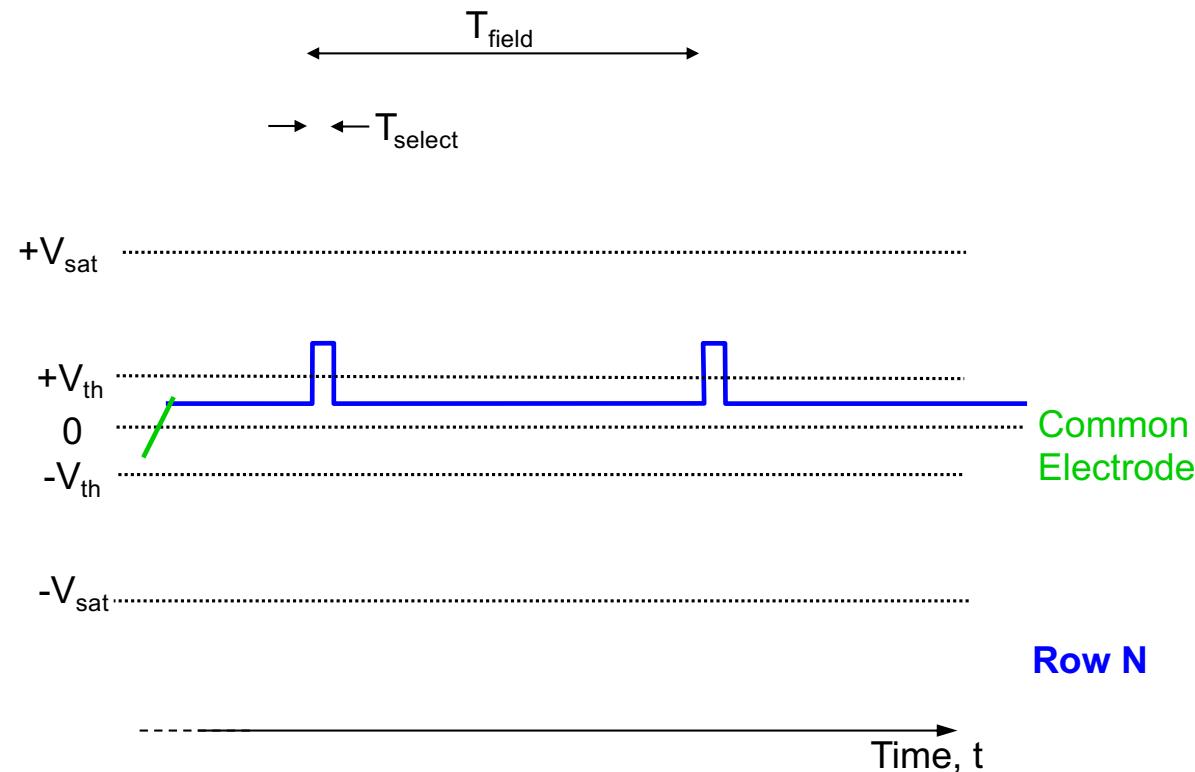
Row/Column Waveforms

Voltage levels of the LC & Common Electrode



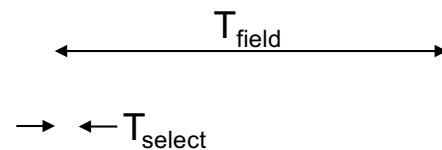
Row/Column Waveforms

Consider Nth row

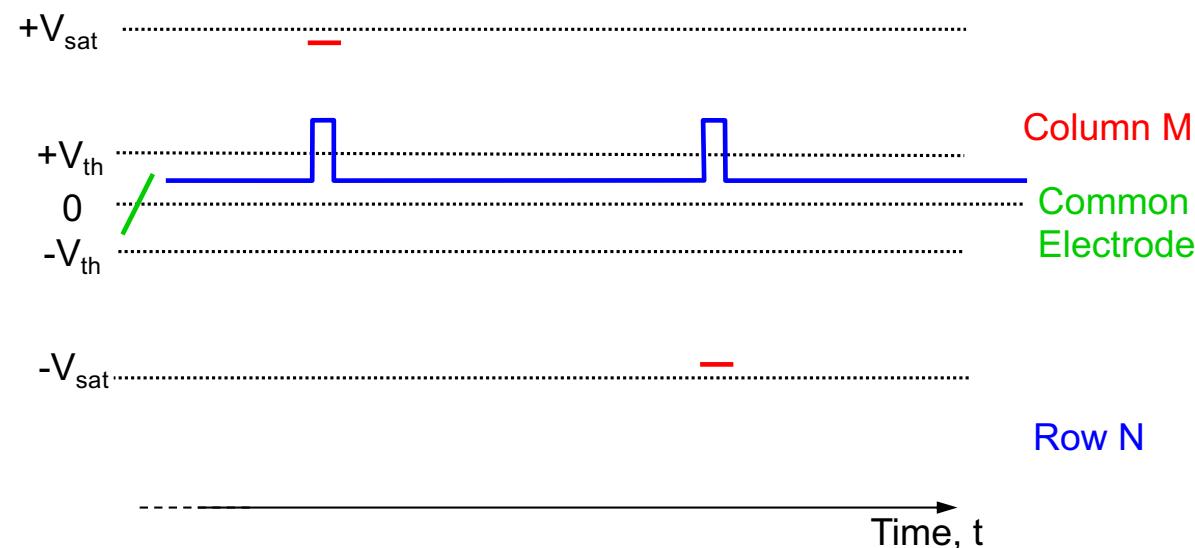


Row/Column Waveforms

Apply voltage to
Column M

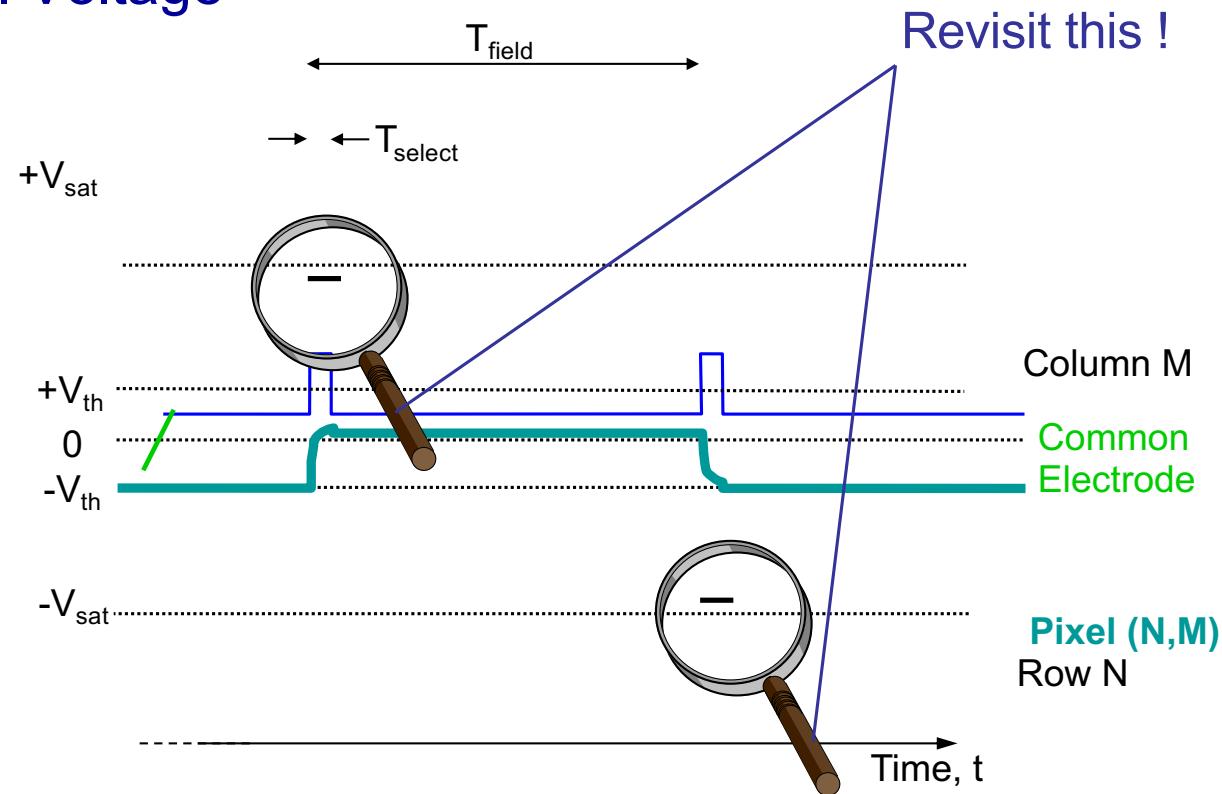


+ve & -ve voltage
INVERSION
no dc across pixel

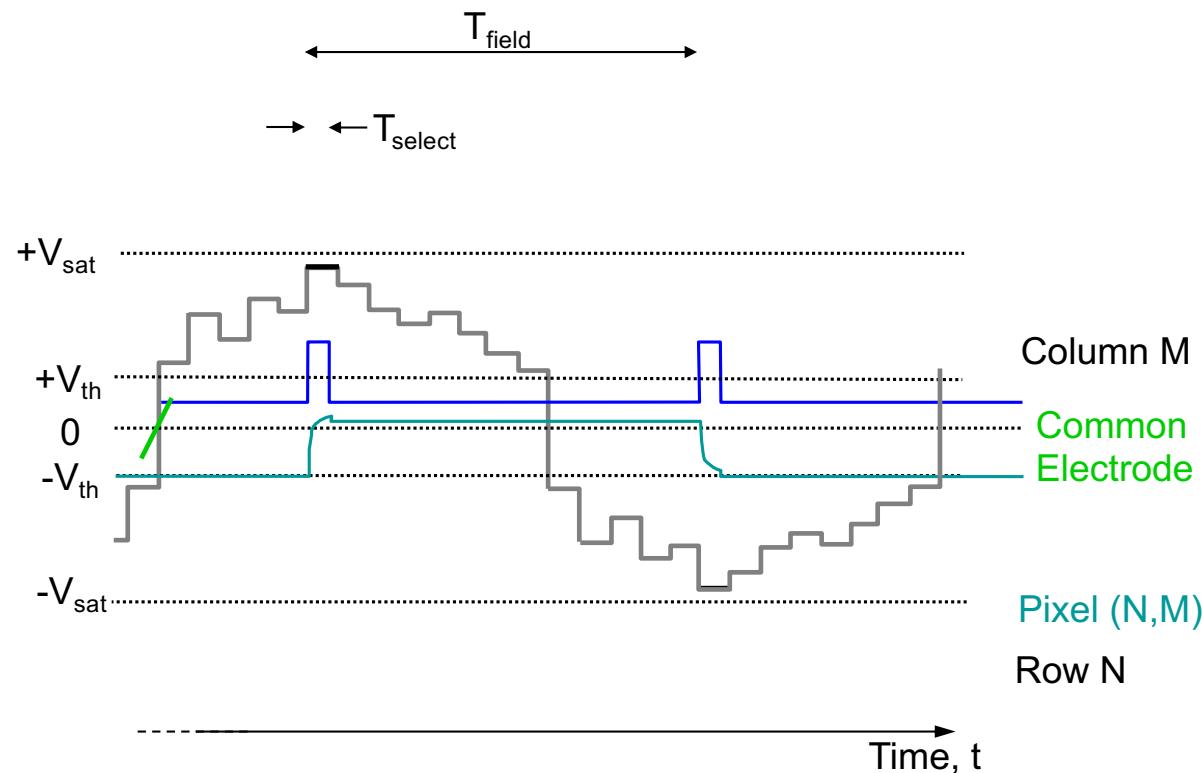


Row/Column Waveforms

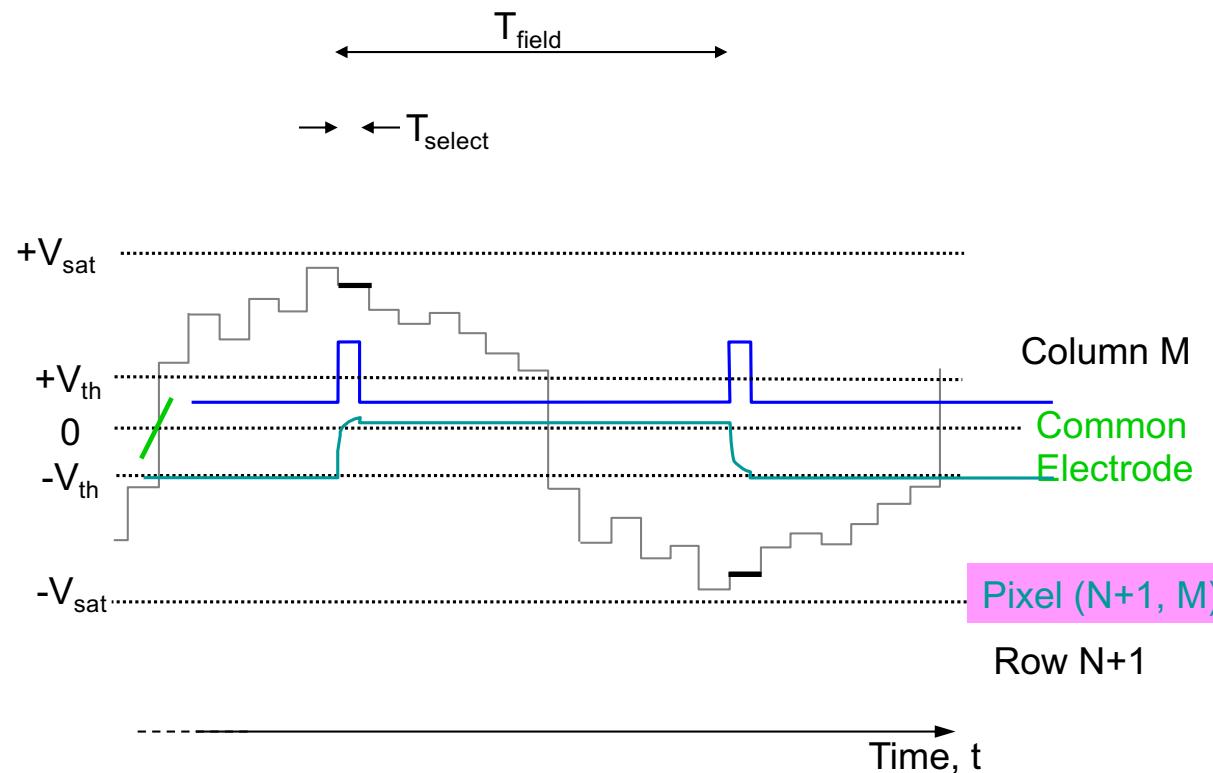
Pixel Voltage



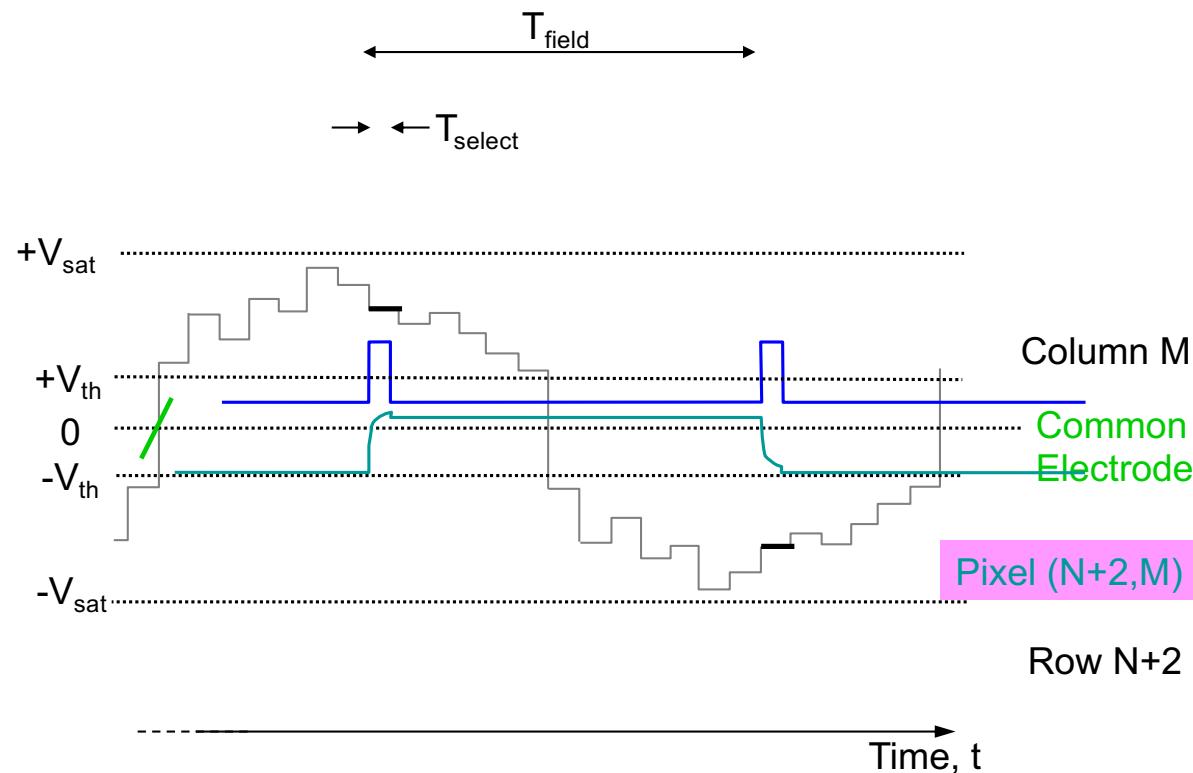
Row/Column Waveforms



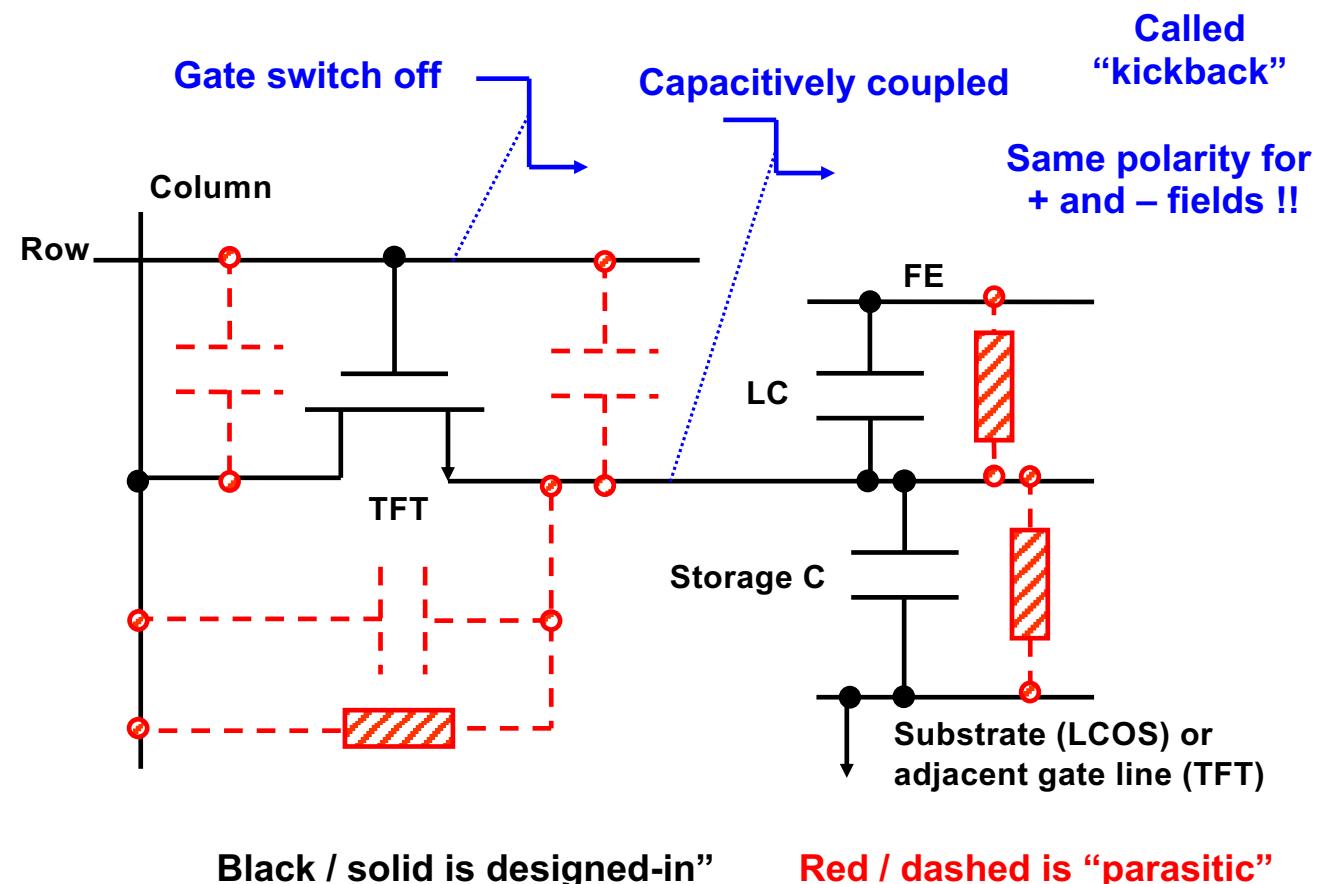
Row/Column Waveforms



Row/Column Waveforms



1xTFT, 1xC pixel – circuit schematic



Kickback – the issue

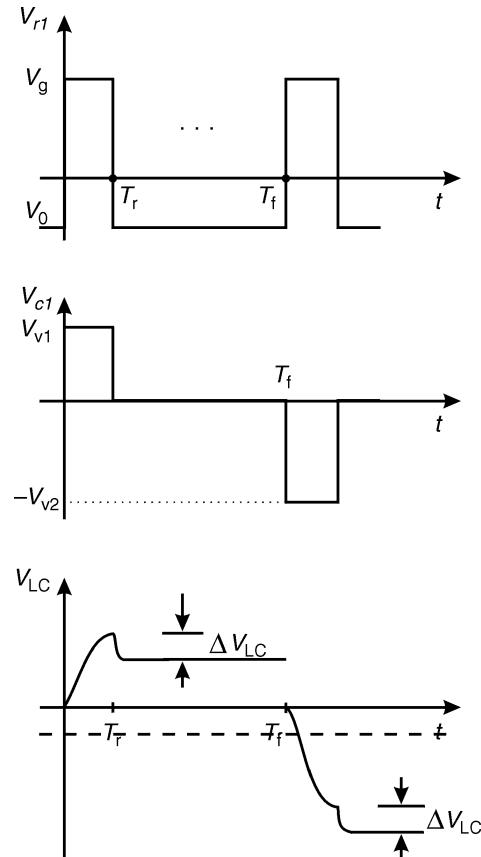
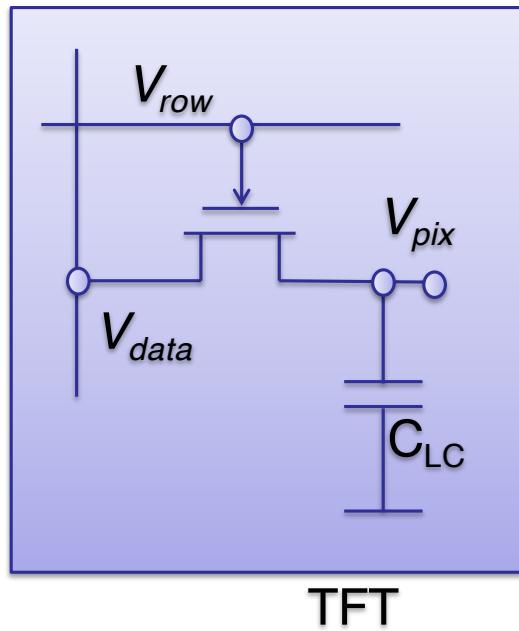


Figure 14.5 The gate impulses and their effect on the pixel voltage V_p

Kickback – the problem

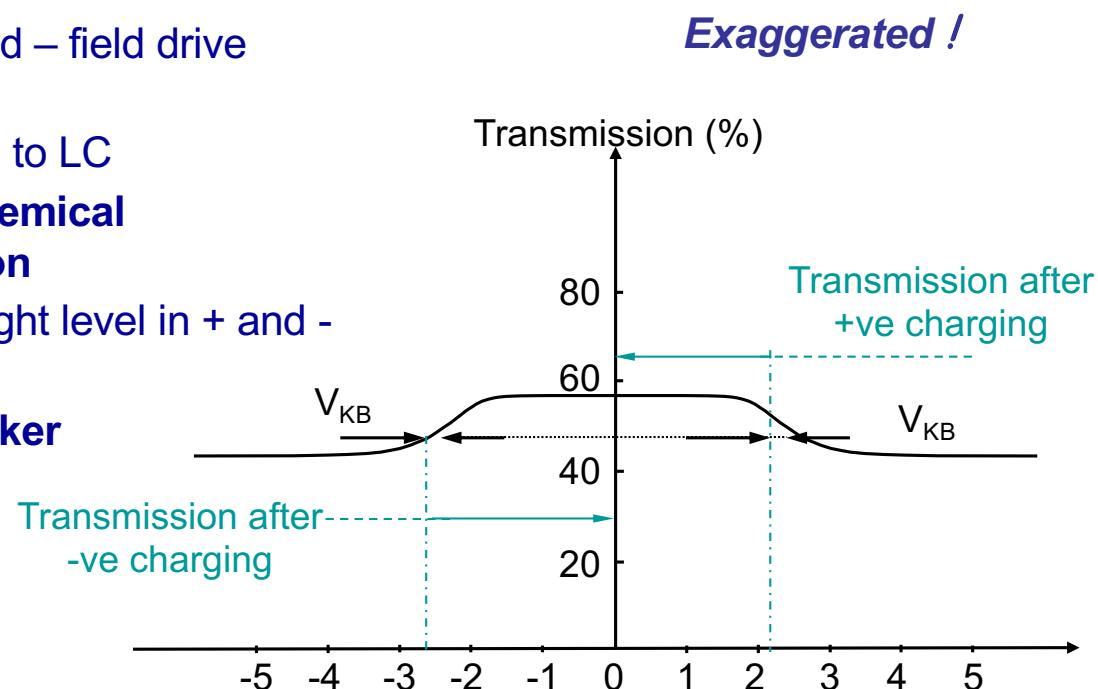
Cause

- Gate drain overlap capacitance
- Gate turn-off edge

Effects

Asymmetry of + and – field drive voltages

- Net d.c. signal to LC
 - **Electro-chemical degradation**
- Inequality of light level in + and - fields
 - **Visible flicker**

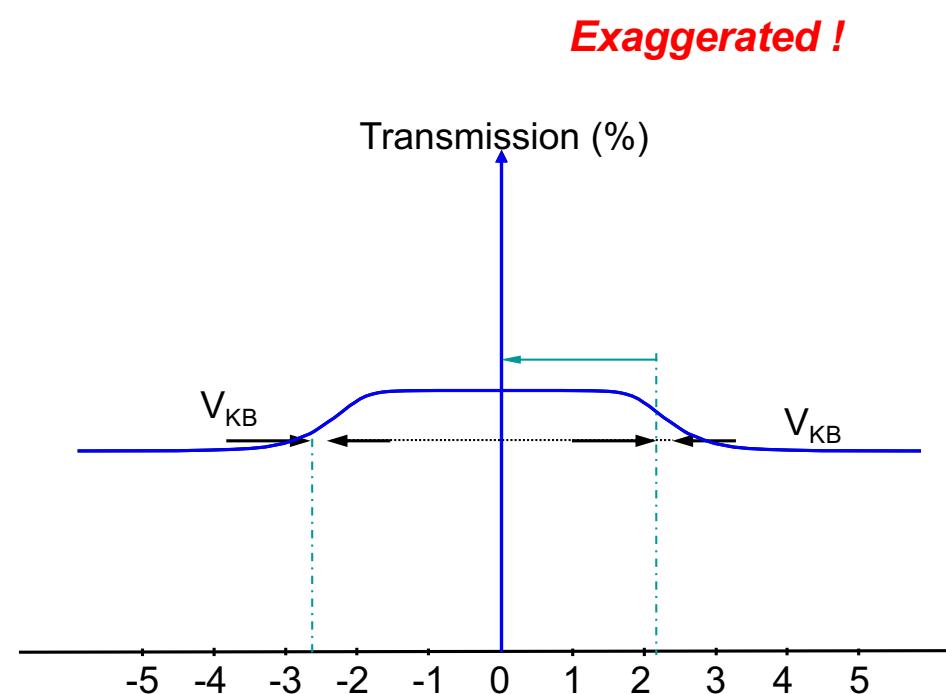
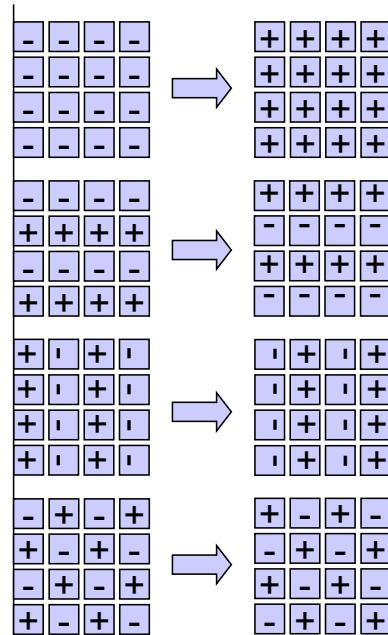


Kickback - solution

Improvements

Bias the common electrode to re-balance the symmetry

- DC balance not by field but by row, column or pixel



External Sources of Information

Handbook of Visual Display Technology **3rd Edition 2020**

<https://link.springer.com/referencework/10.1007/978-3-642-35947-7>

Part X Fundamentals of Driving

Active Matrix Driving *Blankenbach*

Acknowledgement – some Figures taken from the above source

Not 1st edition 2012
Not 2nd edition 2016

Mobile Displays: Technology and Applications.

Ed A. K. Bhowmik, Z. Li, and P. J. Bos © 2008 John Wiley & Sons, Ltd. ISBN: 978-0-470-72374-6

Chapter 9 Advances in Mobile Display Driver Electronics

James E. Schuessler , National Semiconductor, Santa Clara, California, USA



Electronic Information Displays – Route Map

CORE PROGRAMME

-  S1 Logistics
-  S2 Context
-  S3 LC Intro
-  S4 Passive Matrix
-  S5 Active Matrix Addr
-  S6 Active Matrix Tech
- S7 OLED Intro
- S8 OLED Elec
- S9 Microdisplays

GUEST PROGRAMME

- Travis AR VR
- Hands LC not display
- Khan Light Field
- Srivastava QD/QR
- McKendry MicroLED

S6 Active-Matrix Technology – Contents

Substrates

Amorphous Silicon

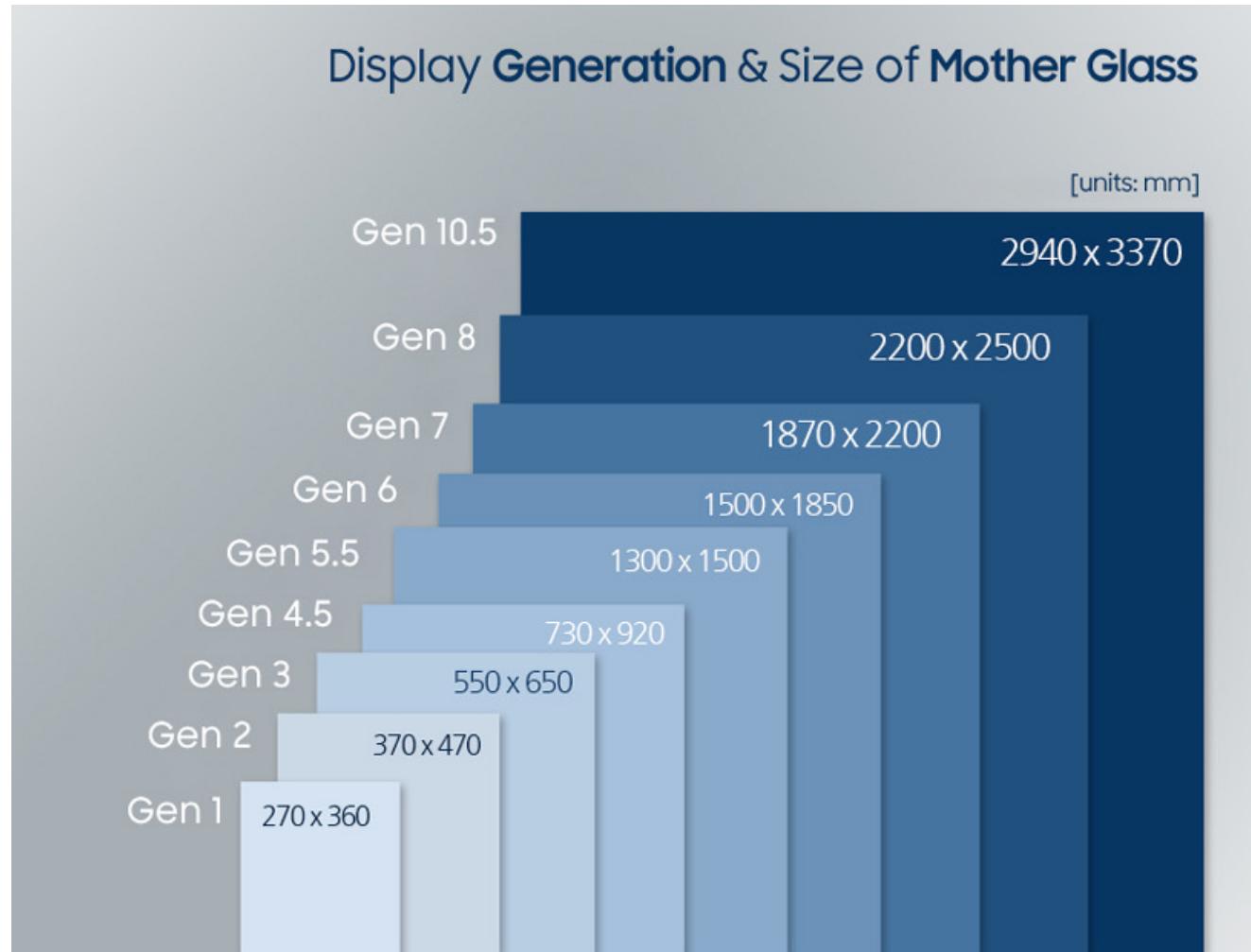
α -Si TFT device

TFT AMLCD Pixel

Back Channel Etched Process

Low-temp Poly Process

Evolution of Glass Substrate size

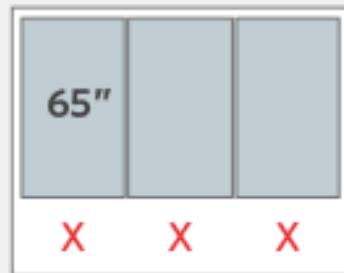


Revenue per Glass Generation

GEN 8.5



Most efficient for 55"



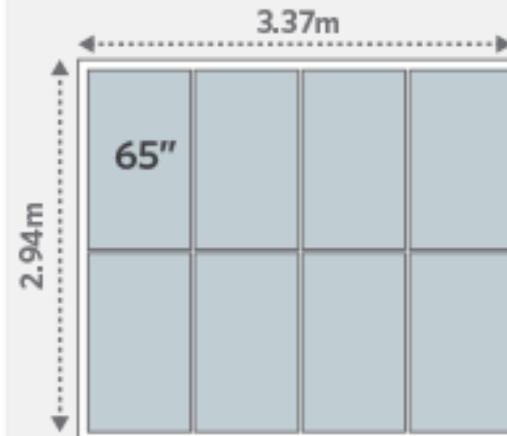
Not efficient for 60"+

55" UHD panel ASP: \$180

Revenue/substrate: \$1080

Revenue/area: **\$196/m²**

GEN 10+



Glass utilization
high for 65"

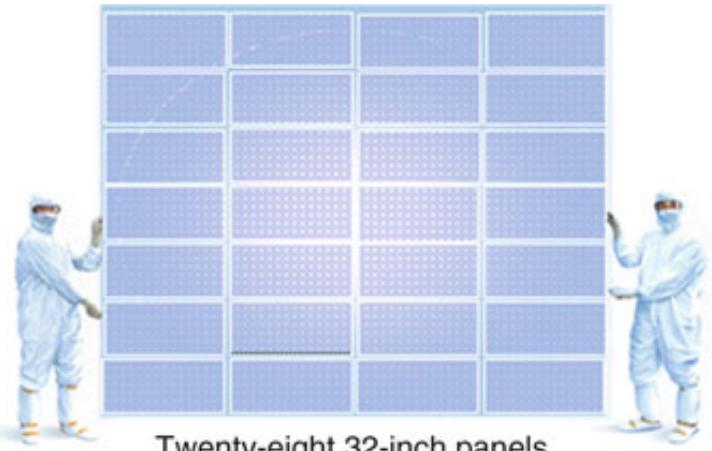
65" UHD panel ASP: \$290

Revenue/substrate: \$2320

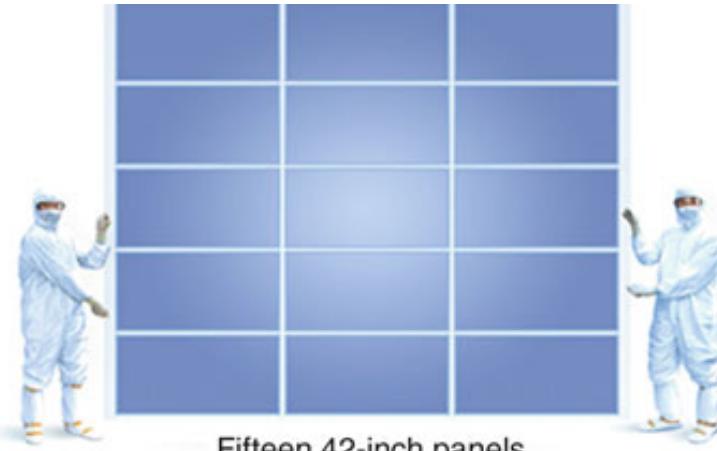
Revenue/area: **\$234/m²**

© Applied Materials Inc

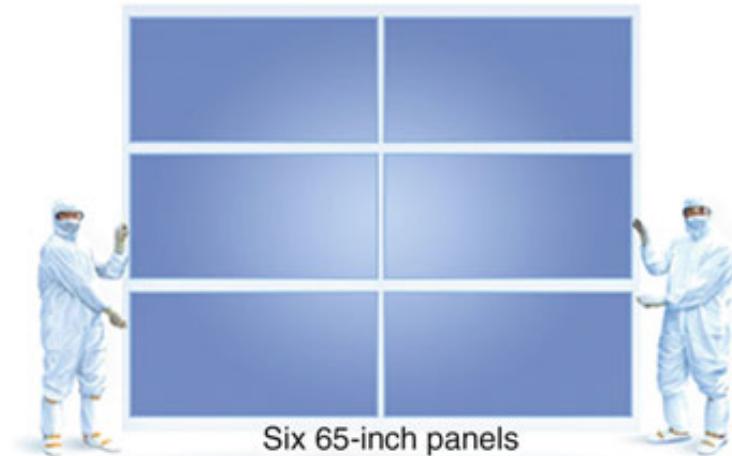
Gen 10 Substrate



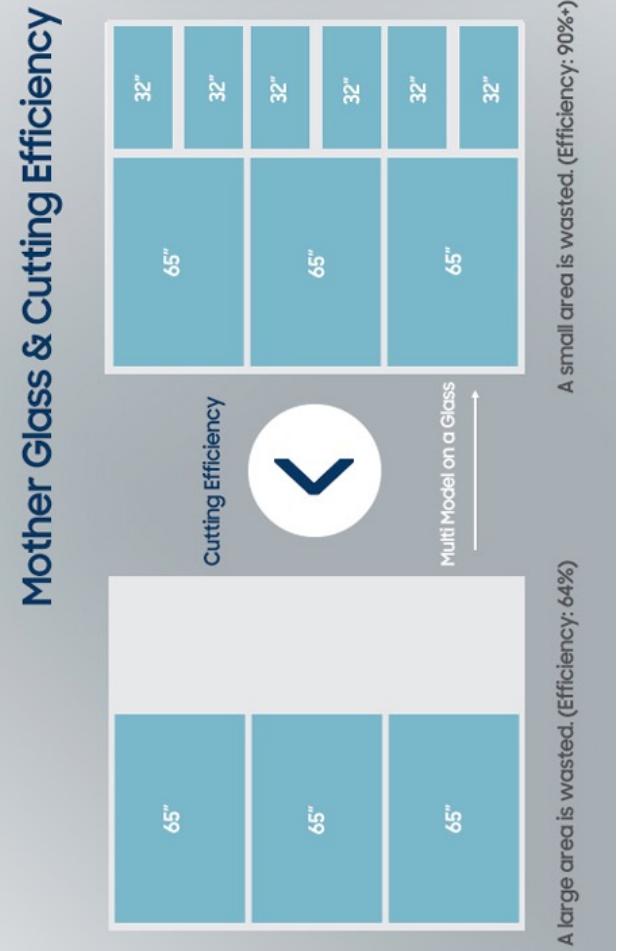
Twenty-eight 32-inch panels



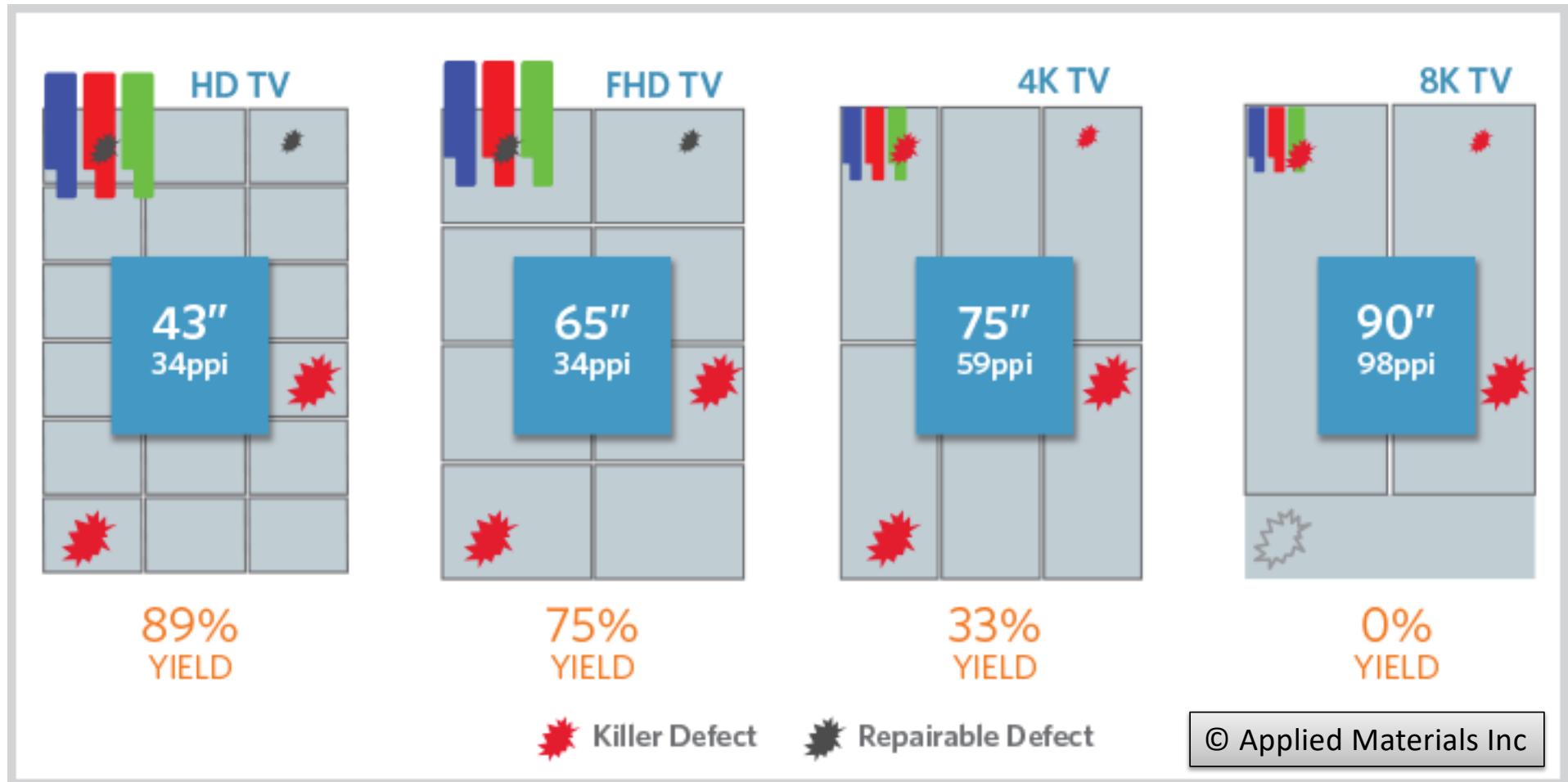
Fifteen 42-inch panels



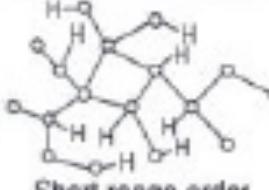
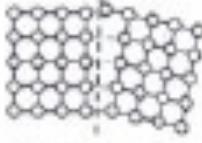
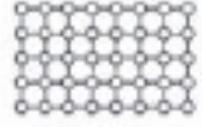
Six 65-inch panels



Evolution of Yield with Time



Qualitative comparison

	a-Si amorphous	poly-Si poly-crystal	c-Si single crystal
Field Effect Mobility μ (cm ² /Vs)	0.5 - 1.0	30 - 300	600 - 700
Crystal Structure	 Short range order H-termination	 Grain boundary	 Perfect
Application	Pixel Switching	Driver Circuit	Driver LSI

Qualitative Comparison of Backplane Technologies

PROPERTY	a-SI:H*	OXIDE	LTPS
Cost	thumb up	thumb up	thumb down
Scalability	thumb up	thumb up	thumb down
On current	thumb down	hand out	thumb up
Off current	hand out	thumb up	hand out
CMOS	thumb down	thumb down	thumb up

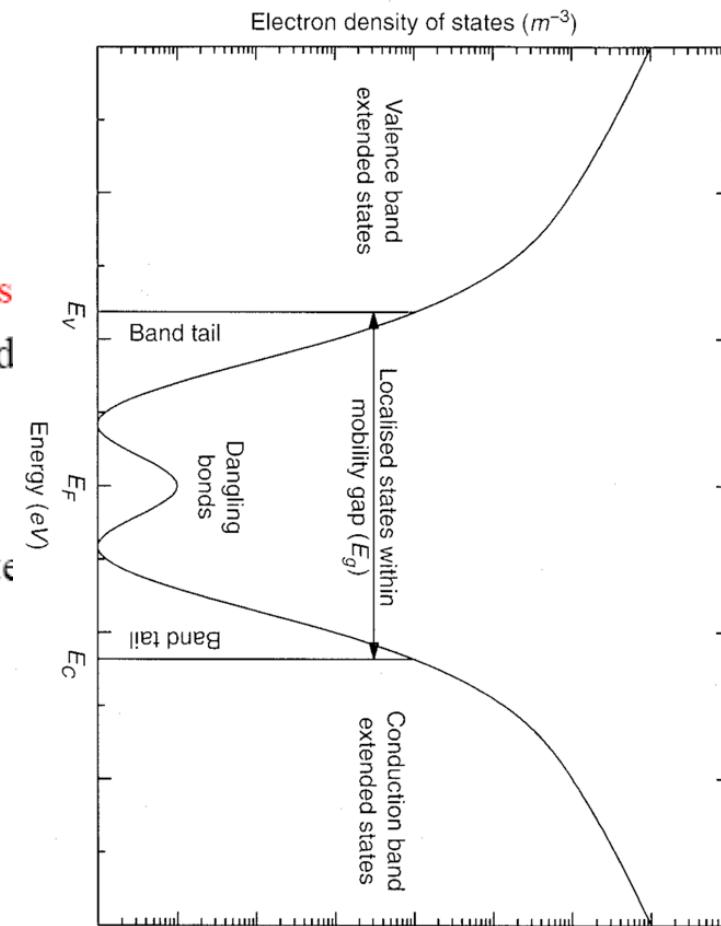
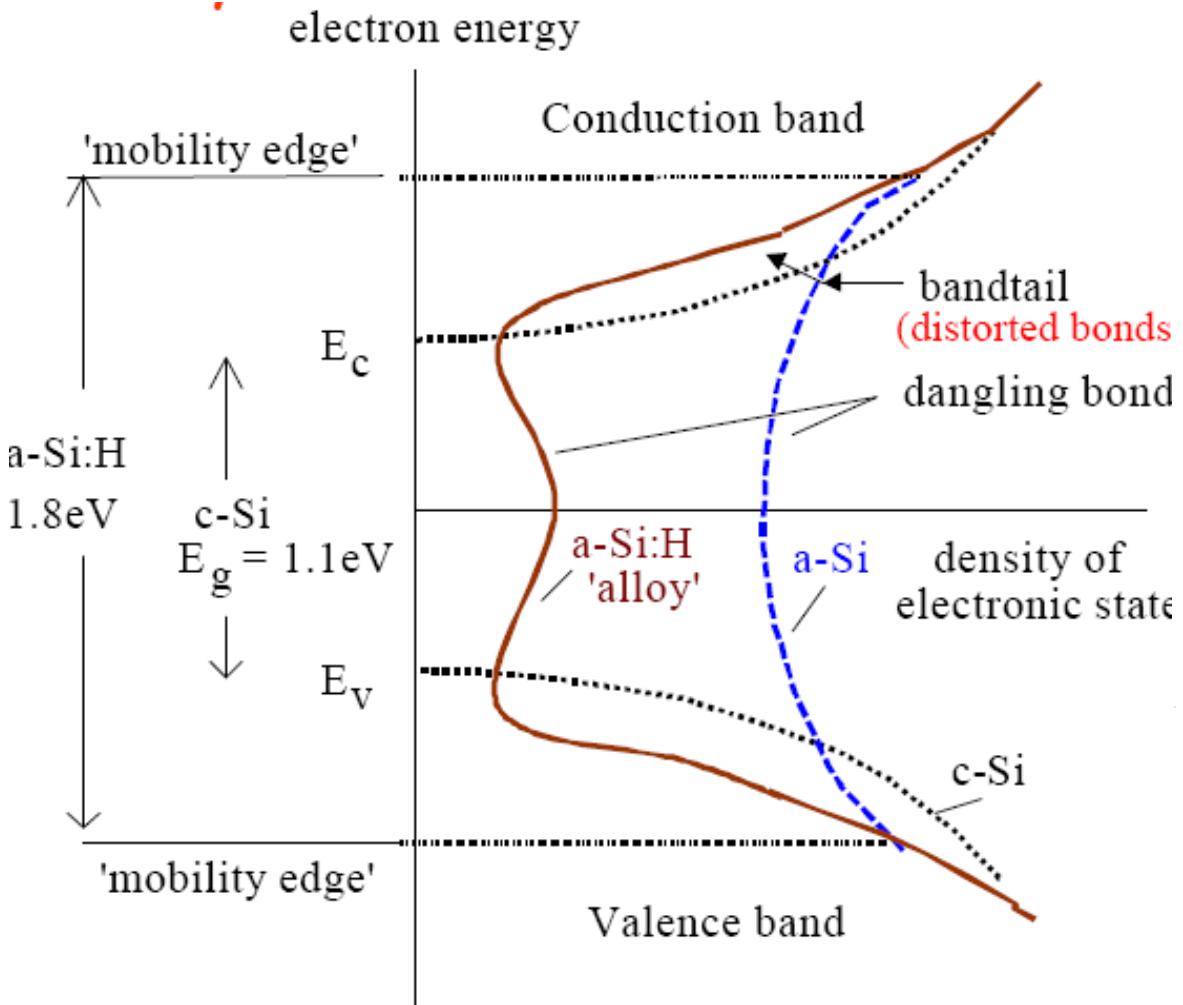
TFT Technology: Advancements and Opportunities for Improvement

John F. Wager

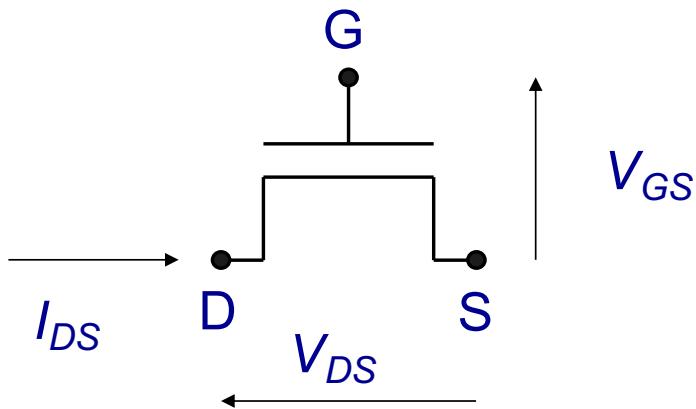
ID Magazine, March 2020

<https://doi.org/10.1002/msid.1098>

Density of states in a-Si

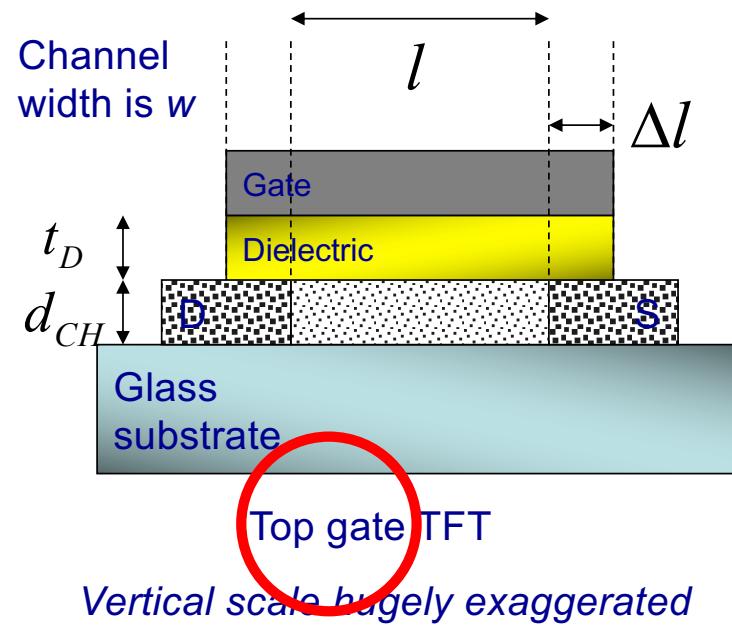


a-Si:H Thin Film Transistor



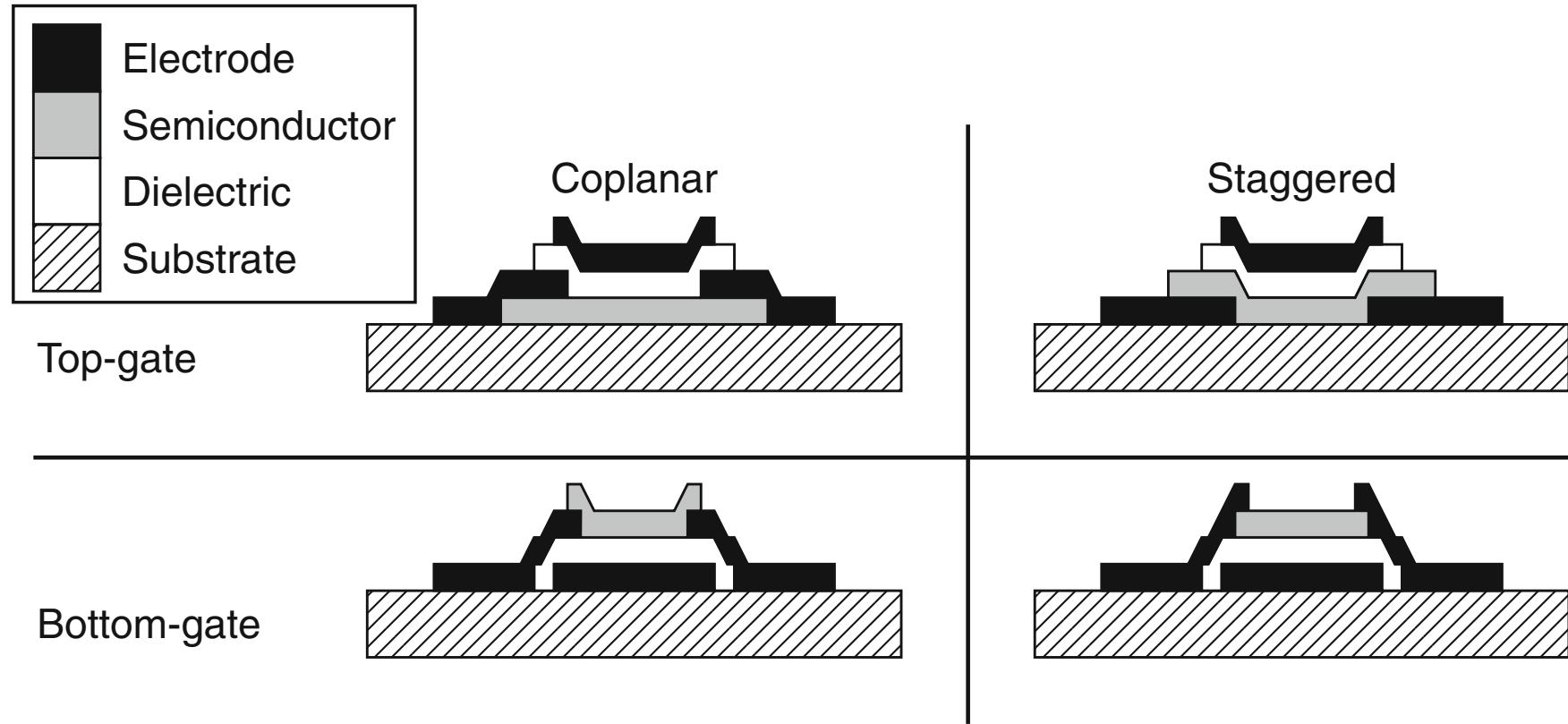
Some similarity in principle to
the operation of
a 3-terminal MOSFET
but

- Much larger dimensions
- Very different materials



MMXXII

Configurations for TFT on glass



Ideal TFT

$$V_{GS} < V_T \ . \ I_{DS} = 0$$

$$V_{GS} - V_T \geq V_{DS}, V_{GS} > V_T \ . \ I_{DS} = \mu C_0 (W/L) \left[(V_{GS} - V_T) V_{DS} - V_{DS}^2 / 2 \right]$$

$$V_{GS} - V_T < V_{DS}, V_{GS} > V_T \ . \ I_{DS} = \frac{\mu C_0 (W/L)}{2} (V_{GS} - V_T)^2$$

$$\ . \ C_0 = \epsilon_0 \epsilon_R / t_D$$

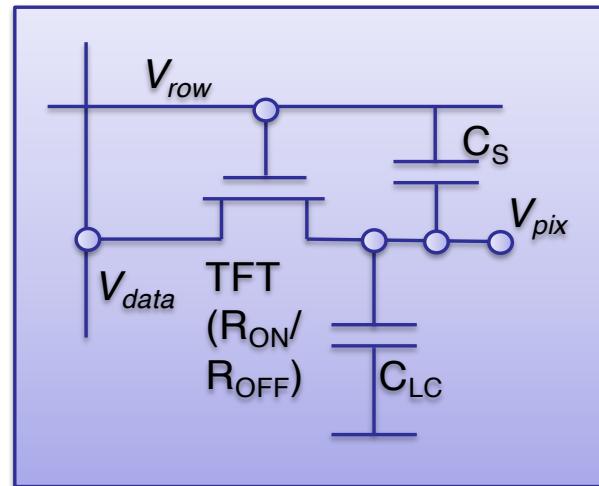
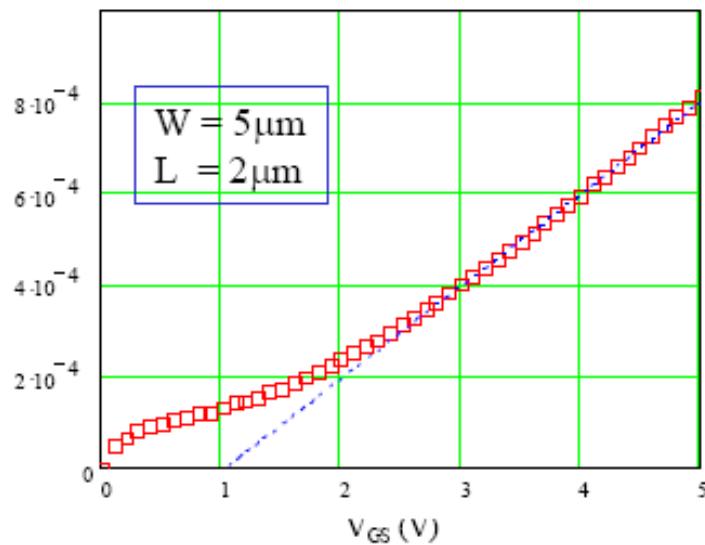
$$\ . \ V_T = -en_0 d / C_G$$

Look very similar to I_{DS} equations for a MOSFET

Practical TFT

$\sqrt{I_{DS}}$ (A $^{1/2}$)

a-Si:H TFT



In practice

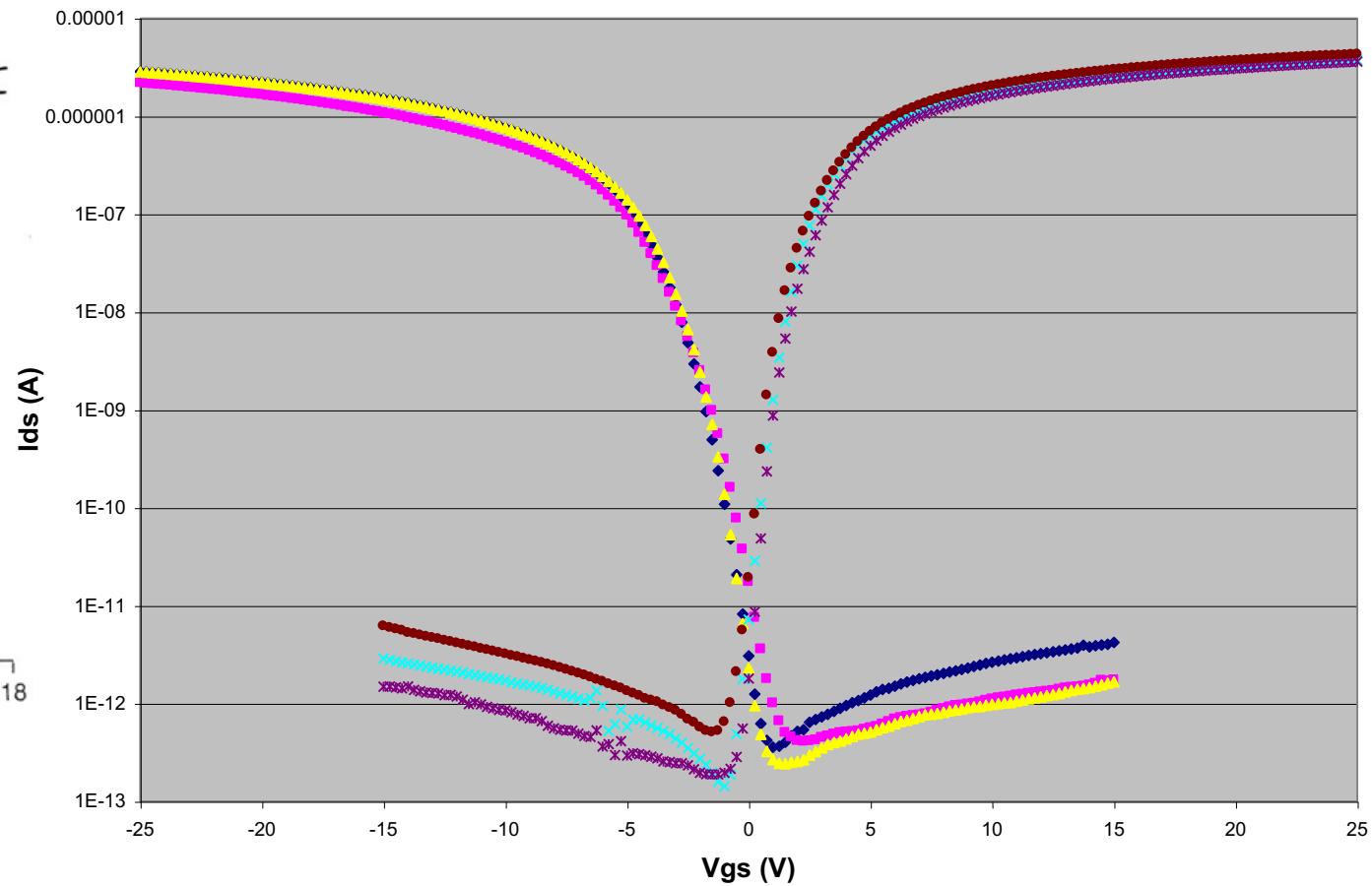
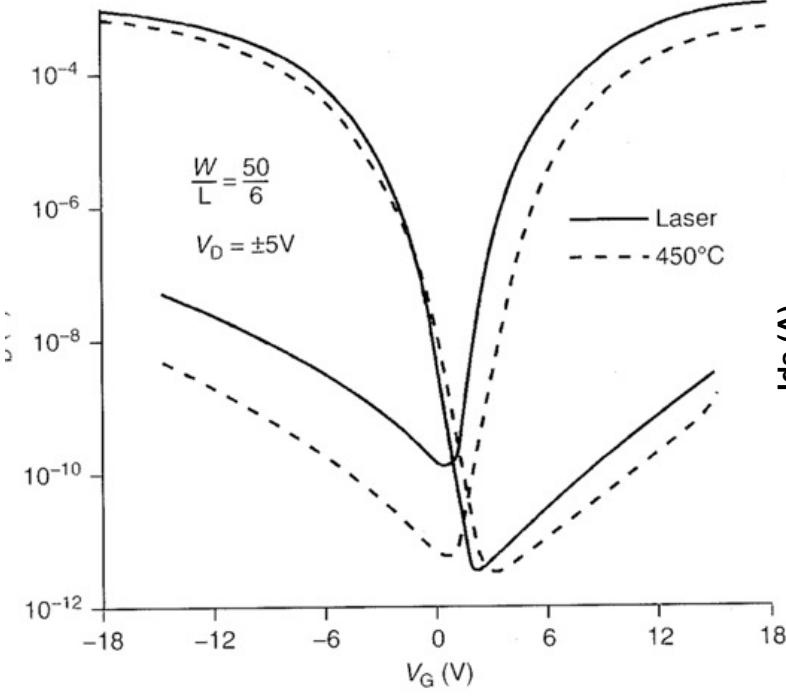
$$I_{OFF} = \frac{W}{L} \frac{V_{DS}}{R_{CH,OFF}}$$

and from

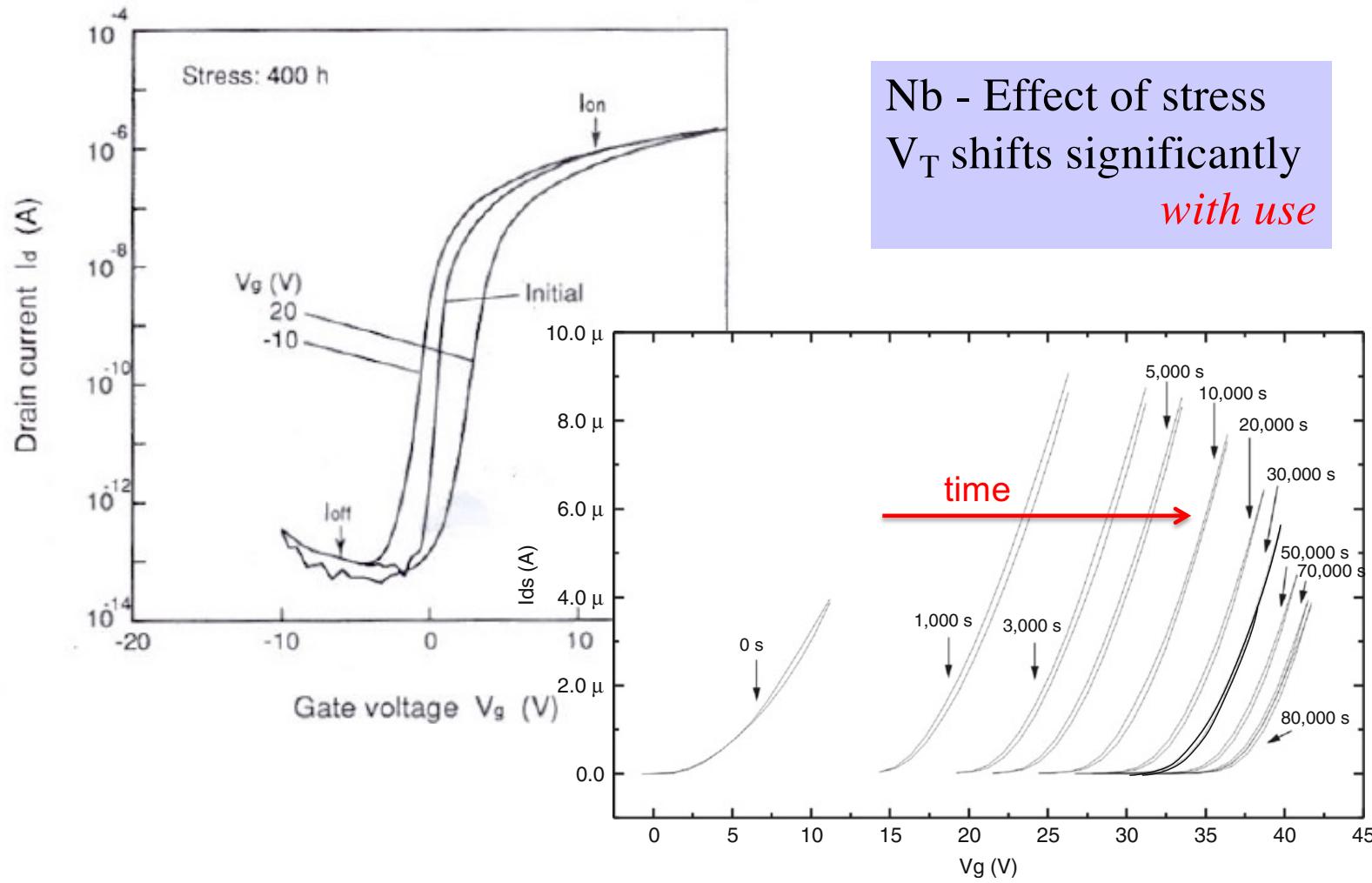
$$\sqrt{I_{DS}} = M(V_{GS} - V_T)$$

$$\mu = M^2 2 l d_{CH} / \epsilon_0 \epsilon_r w$$

Example poly-Si TFT Characteristics



Example α -Si TFT Characteristics



Nb - Effect of stress
 V_T shifts significantly
with use

Pixel constraints on TFT

$$T_{ROW_ADDRESS} = 5T_{RC}$$

$$T_{FRAME} / N = 5R_{ON}(C_{LC} + C_s)$$

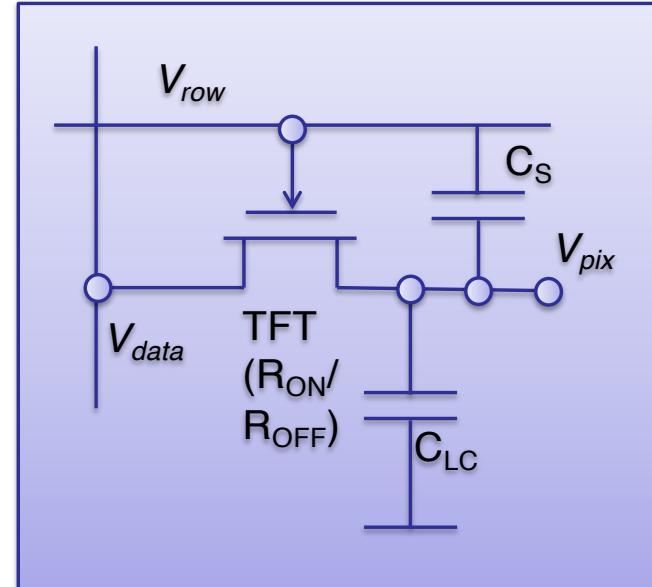
$$R_{ON} = \frac{T_{FRAME}}{5N(C_{LC} + C_s)}$$

ensures that C charges to within 1%

$$\begin{aligned} T_{OFF} &= R_{OFF}(C_{LC} + C_s) \\ &= T_{FRAME} / 0.01 \end{aligned}$$

$$R_{OFF} = \frac{100T_{frame}}{(C_{LC} + C_s)}$$

ensures that C leaks less than 1%



$$\frac{R_{OFF}}{R_{ON}} \geq 500N$$

ensures that the pixel voltage is within
2% of the intended value

Backplane Technology Comparison

Table 2 Comparison among representative TFTs. This table is modified from that taken from J. K. Jeong (Jeong 2007)

	a-Si:H TFT	Poly-Si TFT	TAOS TFT
Generation	>10G	6.5G(LTPS)/8G (HTPS)?	8.5G
Channel	a-Si:H	ELA LTPS/SPC HTPS	a-InGaZnO ₄
TFT mask steps (LCD/OLED)	4–6/6–7	5–9	4–6
Mobility (cm²/Vs)	<1	30–100 (or larger)	1–30 (100?)
TFT uniformity	Good	Poor/better	Good
Pixel TFT	NMOS	PMOS, CMOS	NMOS
Pixel circuit (OLED)	Complex (e.g., 4 T + 2C)	Complex (e.g., 5T + 2C)	Simple (2 T + 1C) in prototypes Several T in products
Cost/yield	Low/high	High/low	Low/high
TFT reliability	Poor	Good	Good
V_{th} shift	>30 V	<0.5 V	<1 V
Stability	Poor	Good	Better than a-Si Large negative ΔV_{th} by light illumination
Circuit integration	No	Yes	Yes
Process T	150–350 °C	250–550 °C	RT – 450 (600) °C
Display mode	LCD, e-paper	LCD, OLED	LCD, OLED, e-paper
Substrate	Glass, metal, plastic	Glass, metal, plastic	Glass, metal, plastic

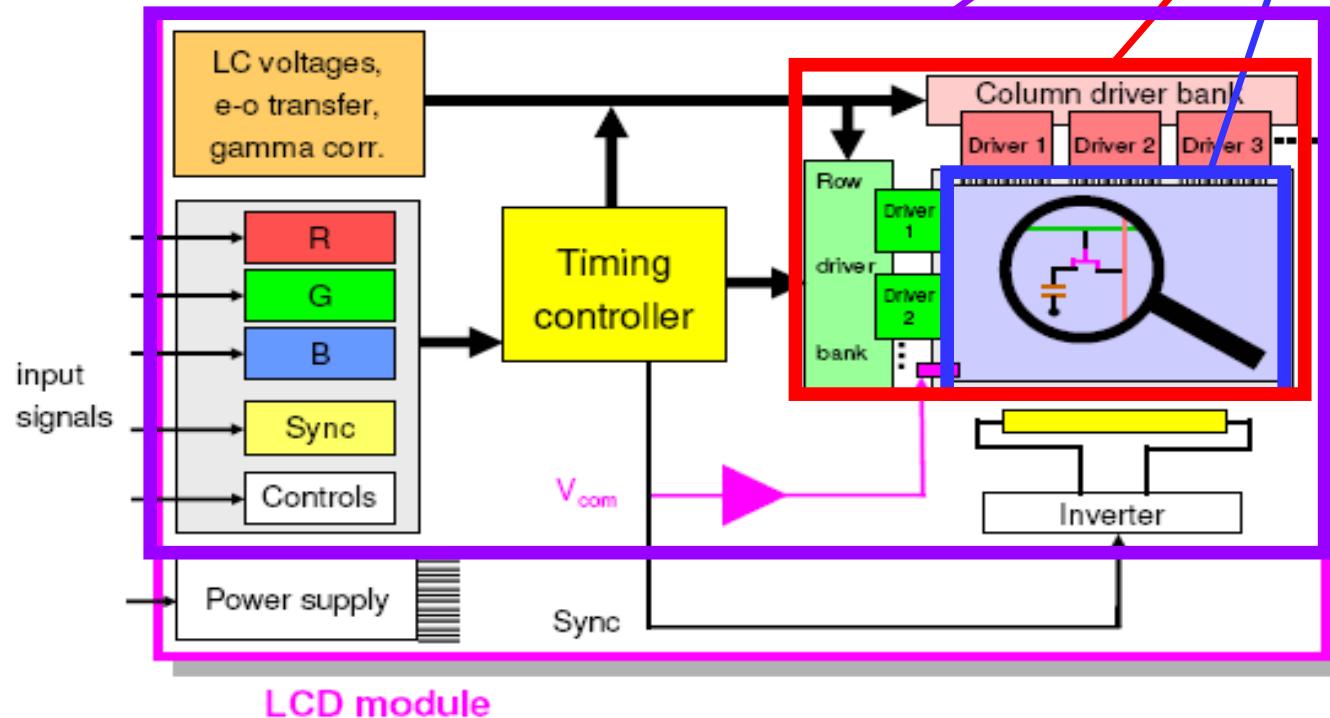
Intended for qualitative comparison

AM LCD Module (including backlight)

Integration on chip capability of CMOS for microdisplay

Integration on glass capability of LTPO

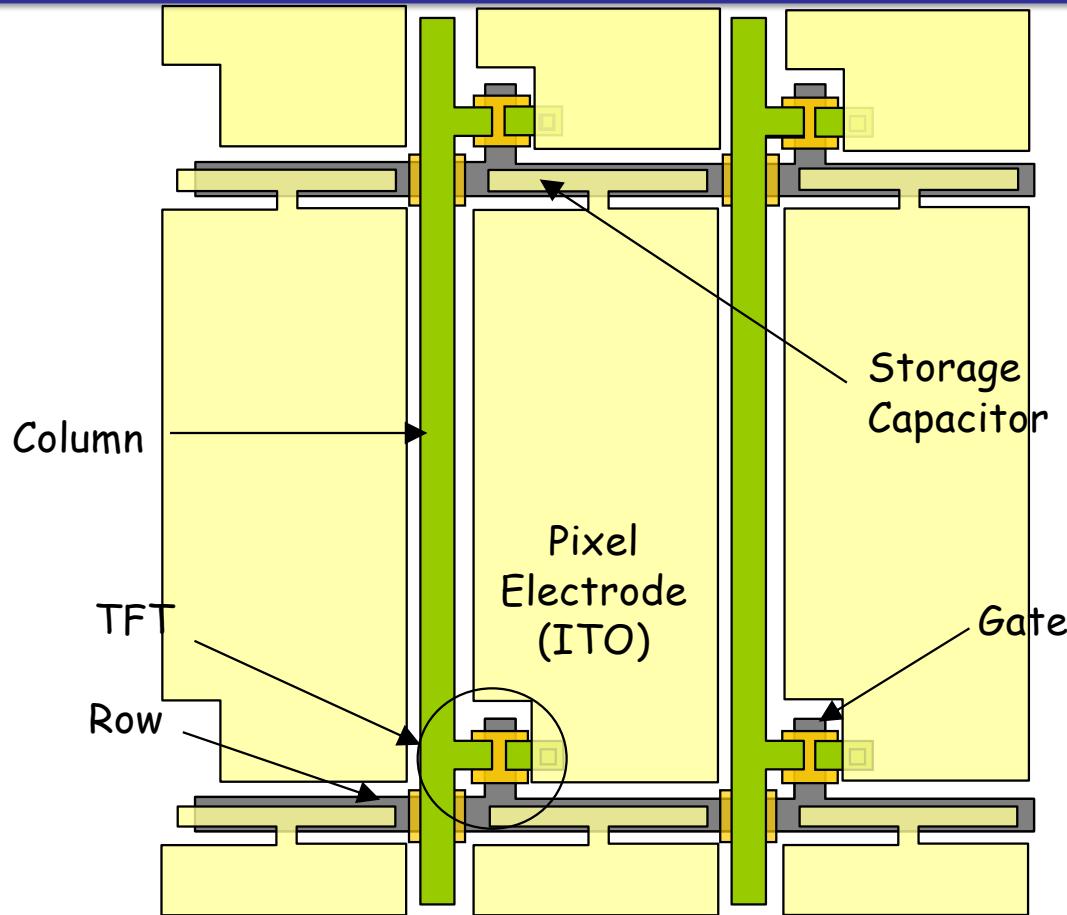
Integration on glass capability of amorphous silicon



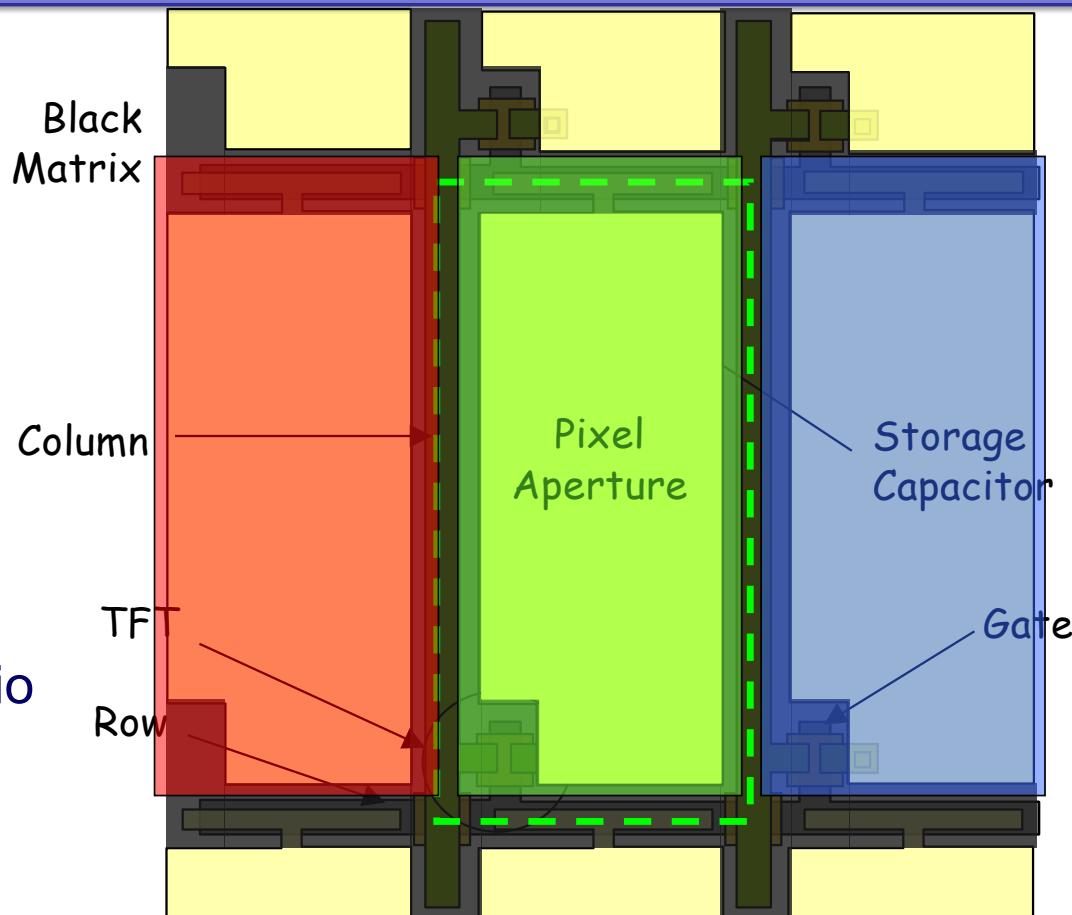
TFT AMLCD pixel layout

With all that area available in the pixel

-why only 1 TFT stuck in the corner of the pixel?



TFT AMLCD pixel layout



Maximize Aperture ratio
= aperture / footprint

Means

Maximize aperture

Means

Minimize circuitry & interconnect

a-Si:H TFT Active Plate Process

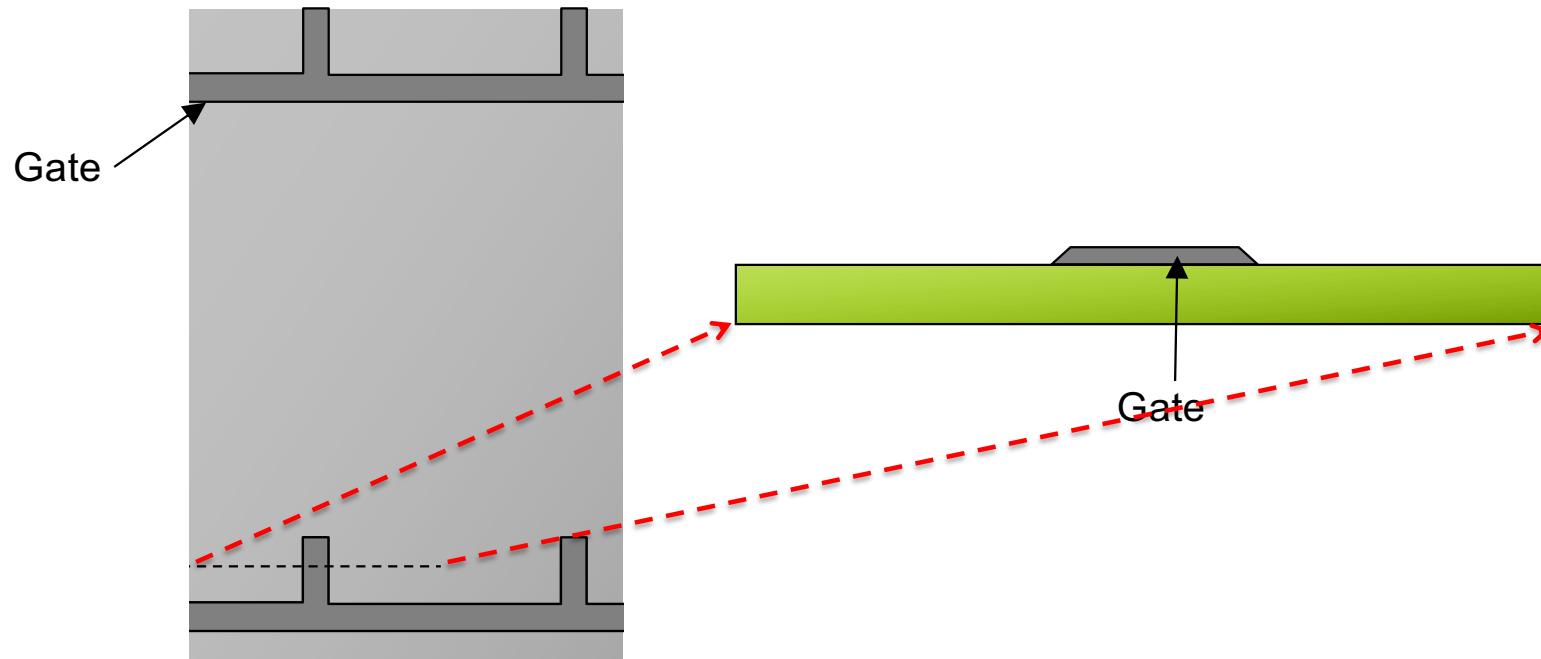
5 mask Back Channel Etched (BCE) TFT Process

- Classic standard in AMLCD industry
- Transmissive display
- Some manufacturers using 4 mask process
- Process split up into photo-lithography mask stages.

Mask 1: Gate

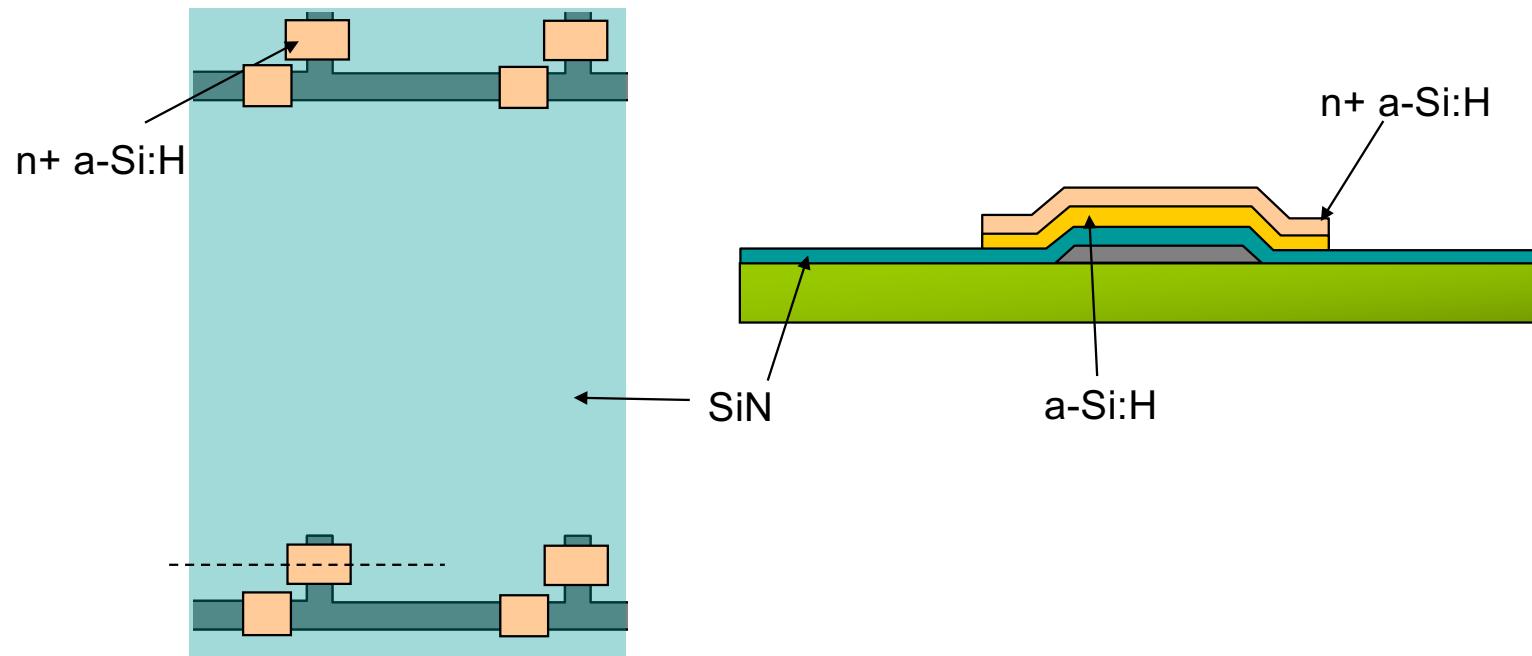
Deposit: Gate metal

Pattern & Etch: Gate metal



Mask 2: Amorphous Si

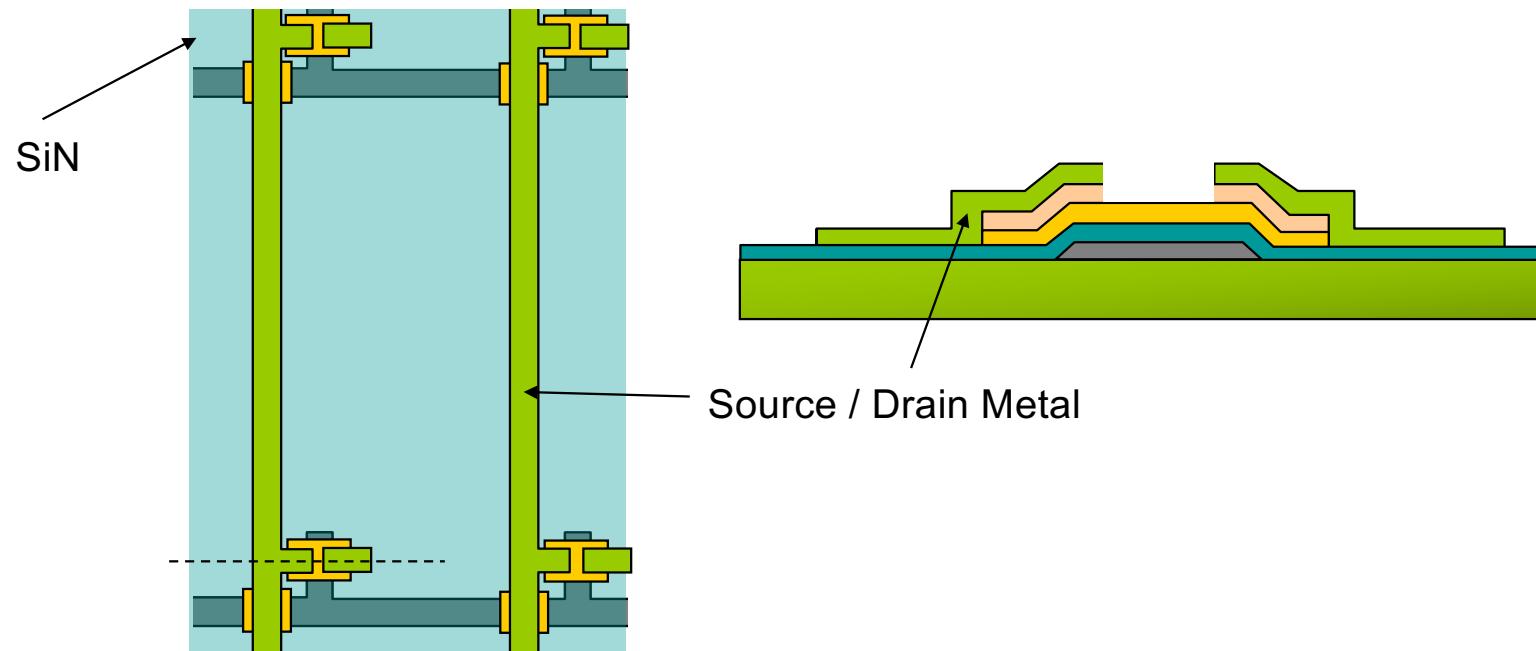
Deposit: SiN, a-Si:H & n+ a-Si:H
Pattern & Etch: n+ a-Si:H & a-Si:H



Mask 3: Source & Drain

Deposit: Source / Drain metal

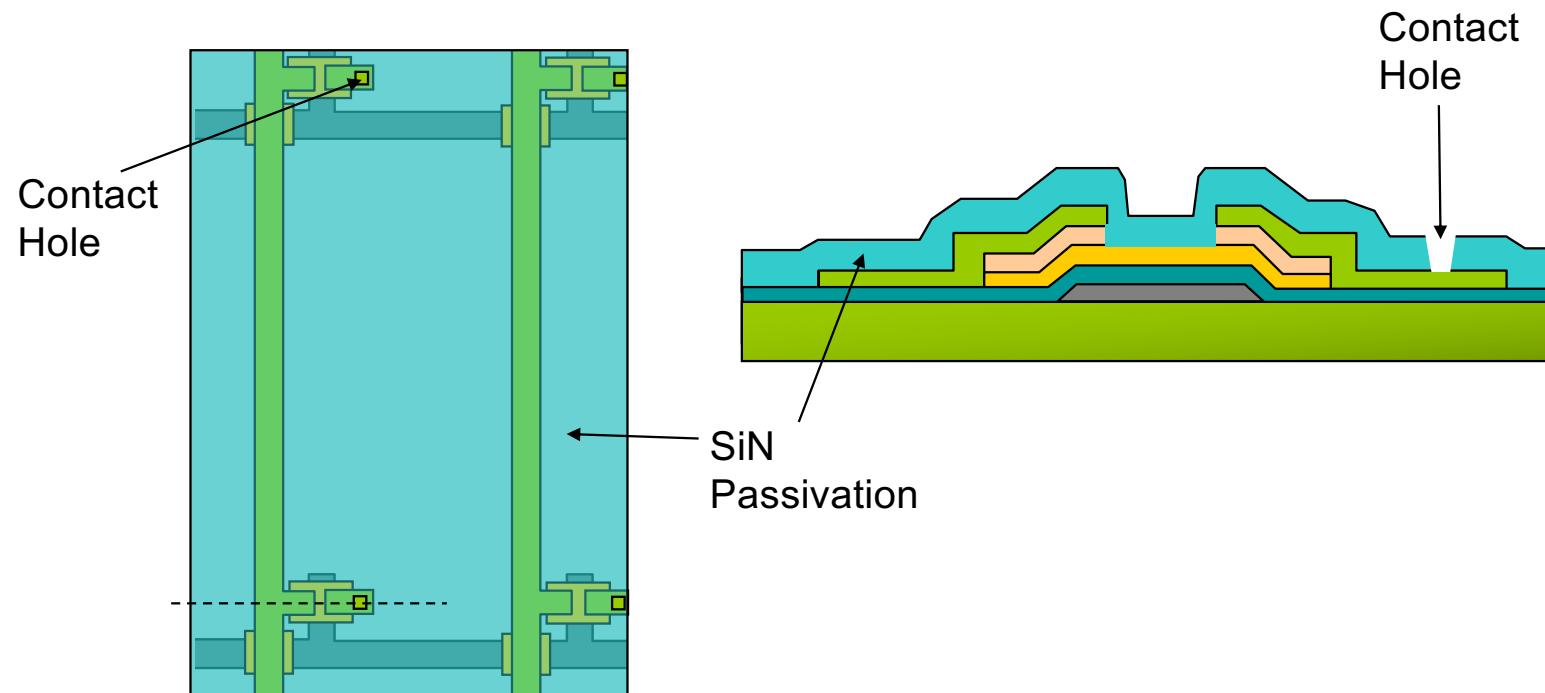
Pattern & Etch: Source / Drain metal & n+a-Si



Mask 4: Contact Hole

Deposit: SiN (Passivation)

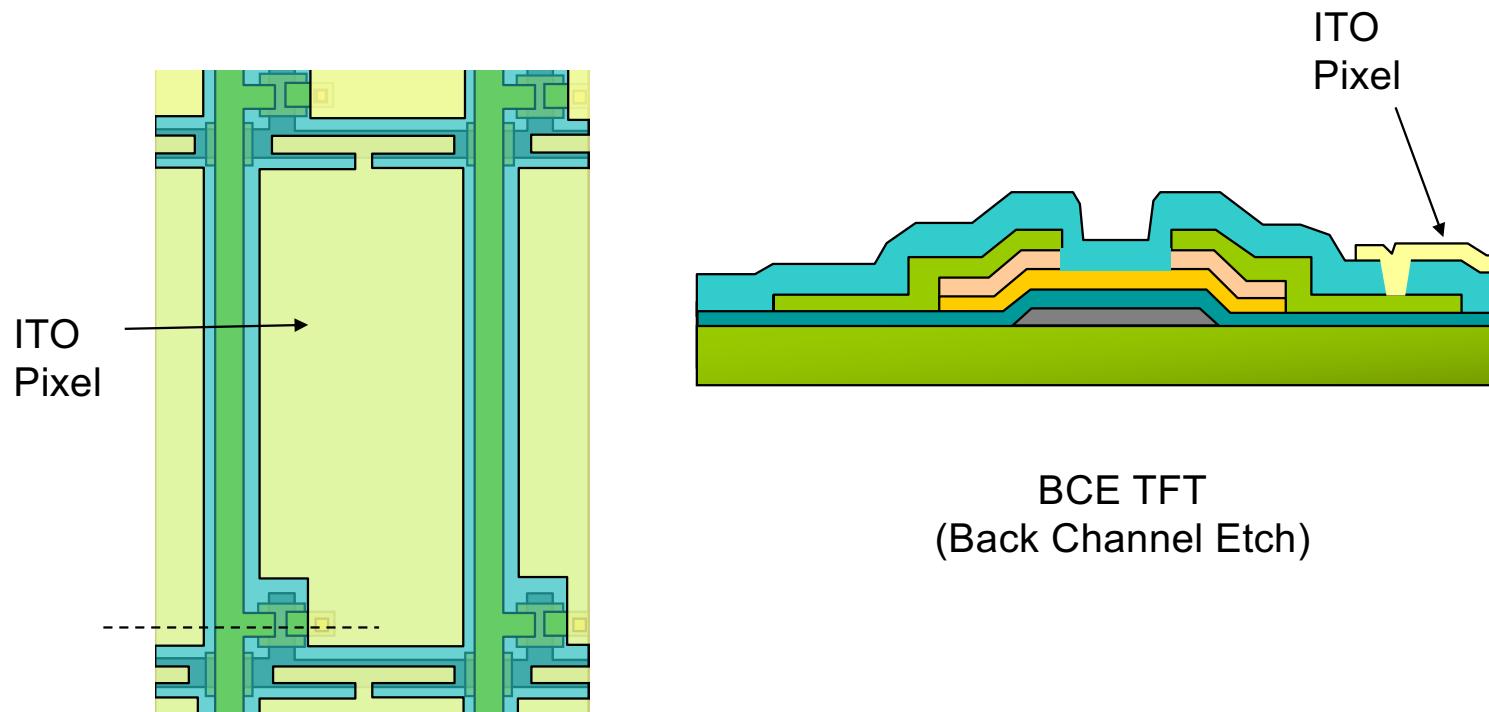
Pattern & Etch: SiN (Passivation) & Gate SiN



Mask 5: Pixel Electrode

Deposit: ITO (Transmissive)

Pattern & Etch: ITO



Polysilicon TFT

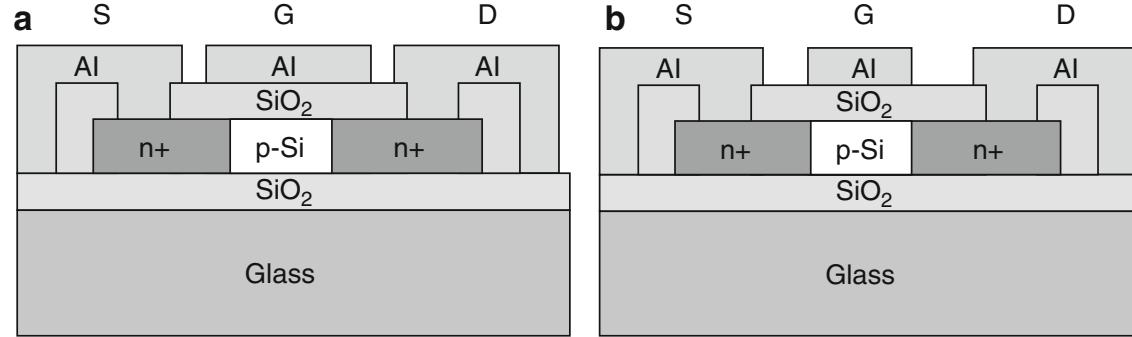


Fig. 6 Cross-sectional diagrams of poly-Si TFT architectures (a) non-self-aligned, (b) self-aligned

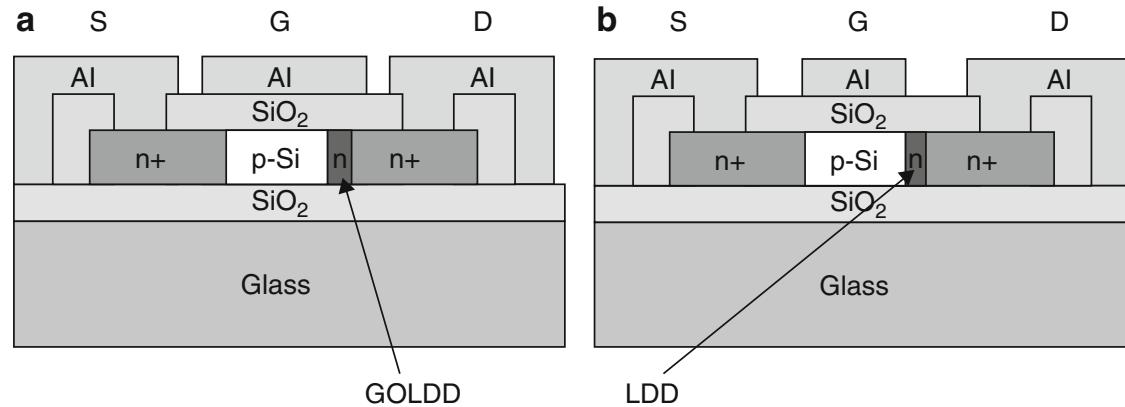


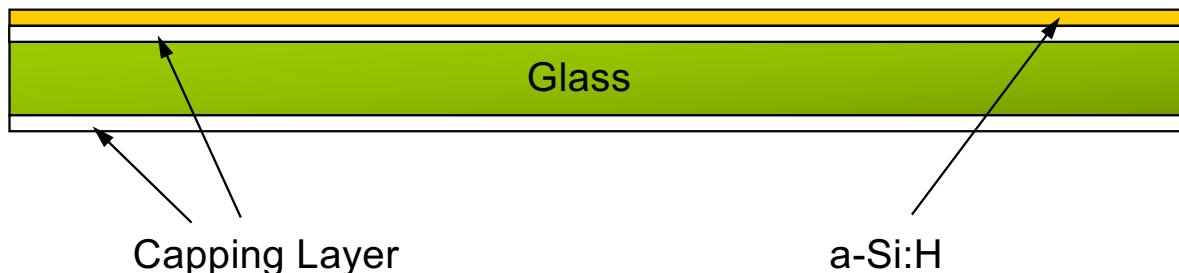
Fig. 10 Cross-sectional diagrams of field relief structures in self-aligned poly-Si TFTs: (a) gate overlapped LDD (GOLDD), (b) LDD

LTPS

- More complex process than for α -Si:H TFTs
 - Form p-Si from α -Si:H e.g. Excimer Laser Annealing
 - Forming both n-type & p-type devices (CMOS)

Deposit dielectric layers on front & back surface of glass & α -Si:H

- SiO_Y capping layers - prevents contamination from glass
 - acts as a heat buffer during laser crystallisation of α -Si:H



LTPS

Dehydrogenate – remove hydrogen from a-Si:H

- Otherwise explosive evolution of H₂ occurs during laser crystallisation
- Could badly damage a-Si/pSi surface
- ~8% H as deposited, < 3% after dehydrogenation

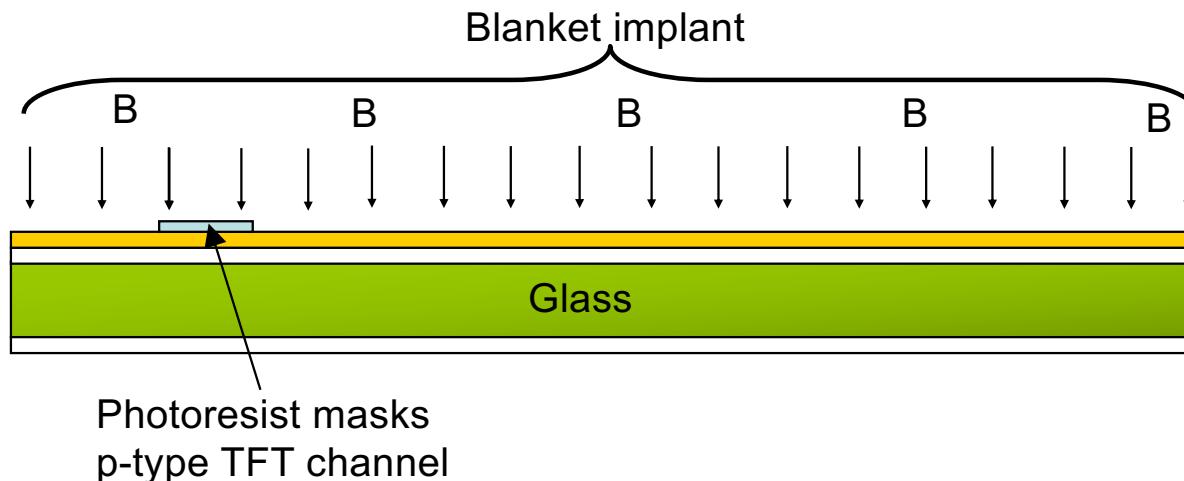


- Thermal anneal: 400°C – 450°C for ~1-2 hours, in pure N₂

Mask 1: Low Ion Implantation Dose

Adjustment of TFT threshold voltage V_t

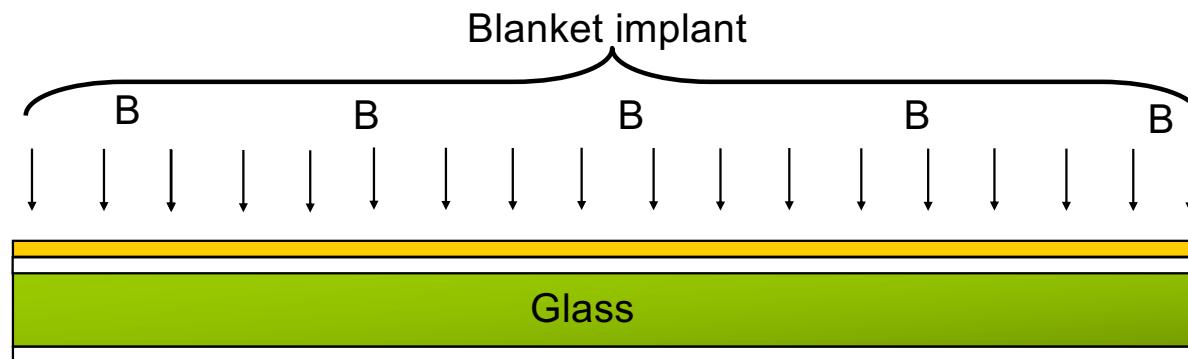
- Boron (B)
- Different adjustment required for n-type & p-type TFTs
- e.g. mask p-channel TFTs (in peripheral circuits) by photoresist



Blanket Implant

Blanket Ion Implantation

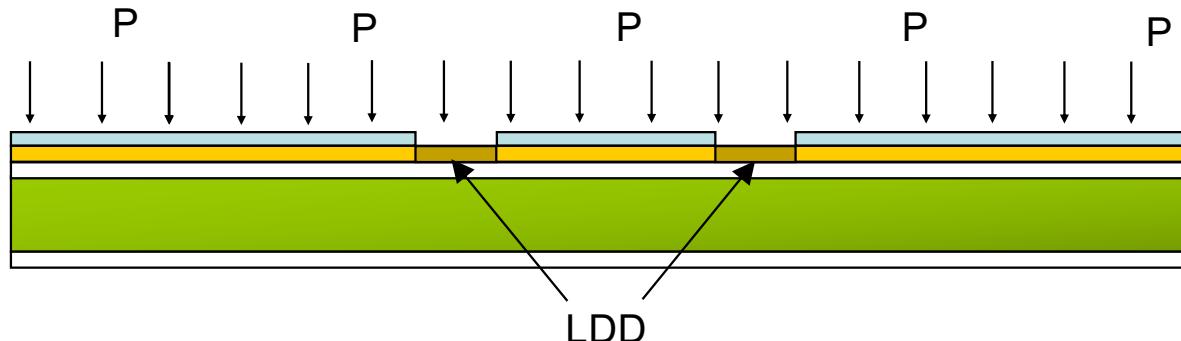
- Allows adjustment of both n-type & p-type TFT threshold voltages V_t
- B implant



Mask 2: Lightly Doped Drain (LDD)

n-type p-Si TFTs need LDD to reduce E-field

- Hot carrier injection – high electric field
- Causes high leakage current
- Not required for p-type



- LDD acts as a field relief region

Laser Crystallisation then Mask 3: PolySi Island

- Substrate cleaned – a-Si surface
- Excimer Laser Anneal
 - Crystallisation



Dry etch to form p-Si islands



Mask 4: Gate

Gate oxide deposition

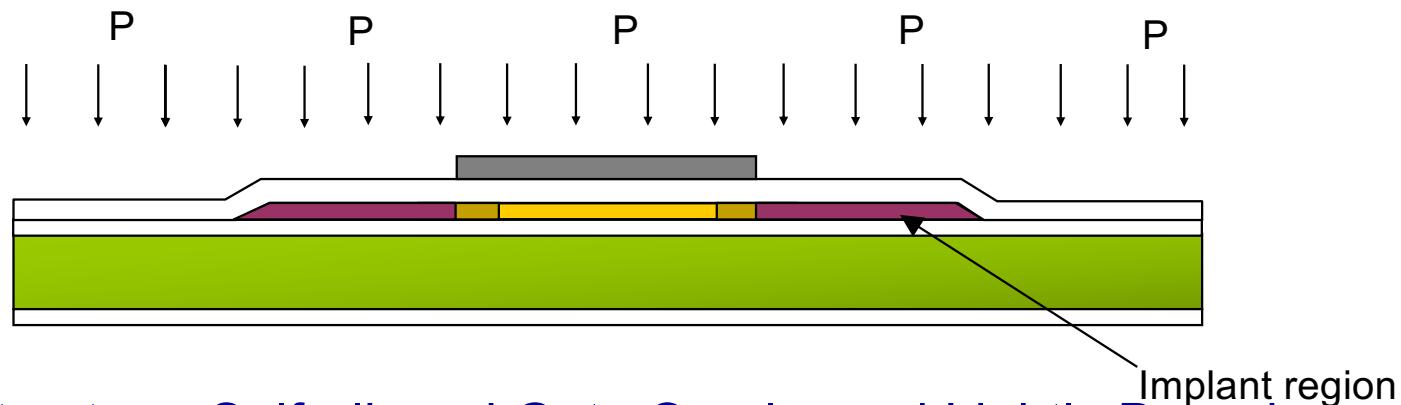
- Gate metal deposition
- Pattern (wet etch)



Mask 5: High Dose S/D Contacts (n-type)

High P implant for n-type TFTs

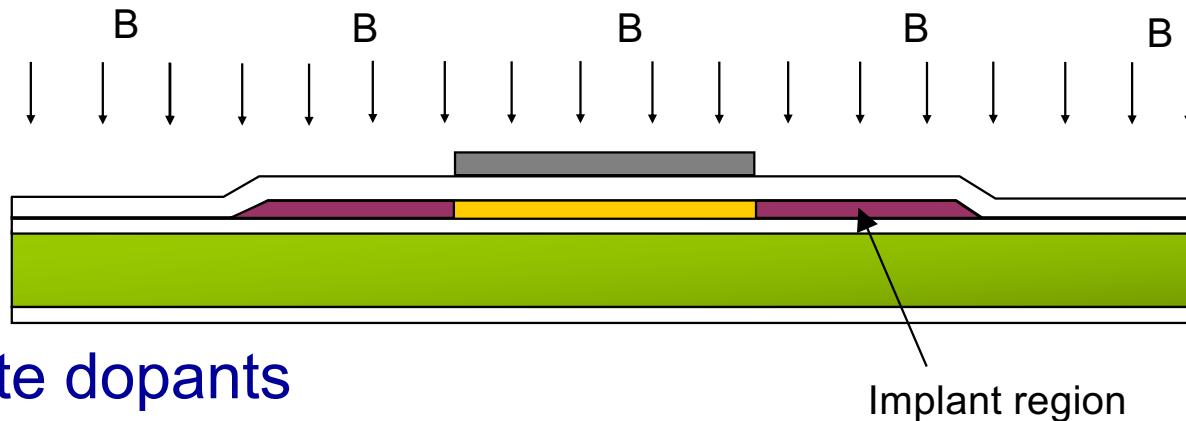
- Uses photoresist mask (not shown) – protects p-type TFTs
- Through gate oxide
- Forming self-aligned Source & Drain contacts



- Structure: Self-aligned Gate Overlapped Lightly Doped Drain (SA-GOLDD)

Mask 6: High Dose S/D Contacts (p-type) then Dopant Activation

- High B implant for p-type TFTs
 - Uses photoresist mask (not shown) – protects n-TFTs



Activate dopants

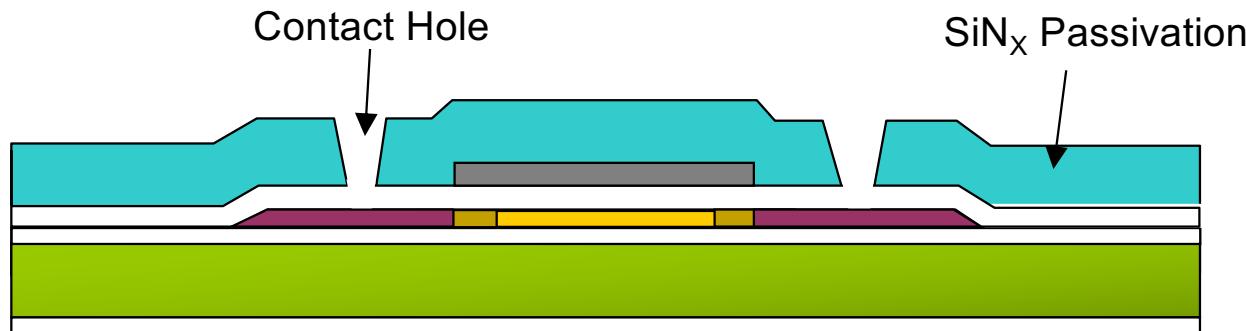
- Furnace: $\sim 450^{\circ}\text{C}$, 1- 2 hours in N_2/H_2
- Excimer Laser Anneal (ELA): Lower E than for crystall'n
 - Through gate oxide layer, do not want re-melting



Mask 7: Contact Holes to Source, Drain & Gate

Deposit SiN_X passivation layer

- Pattern & Etch down to implanted Source & drain regions
 - Wet or dry etch through SiN_X & gate oxide – sloped side walls preferred

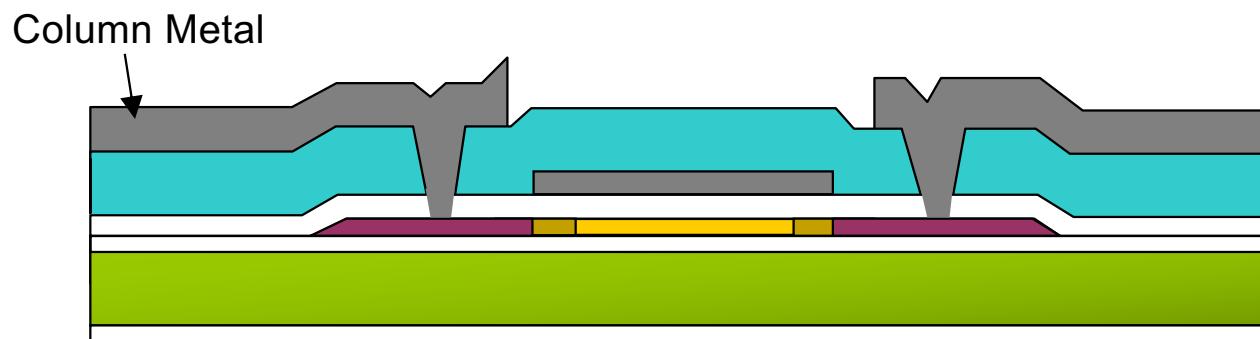


- Etch to gate metal at edge of display (not shown). Etching through SiN_X only required

Mask 8: Column Metal

Deposit Column Metal

- Pattern & Etch: wet etch

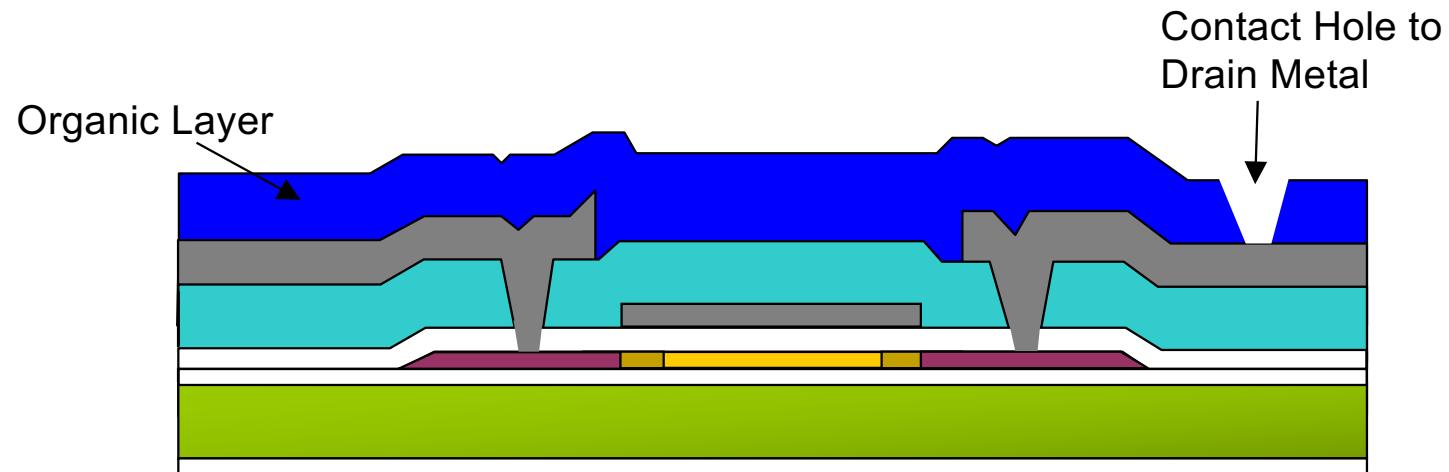


- Hydrogenation in N_2/H_2 , 1-2 hours, $\sim 300^\circ C$

Mask 9: Contact Hole

Thick organic layer

Pattern & Etch: possibly photosensitive

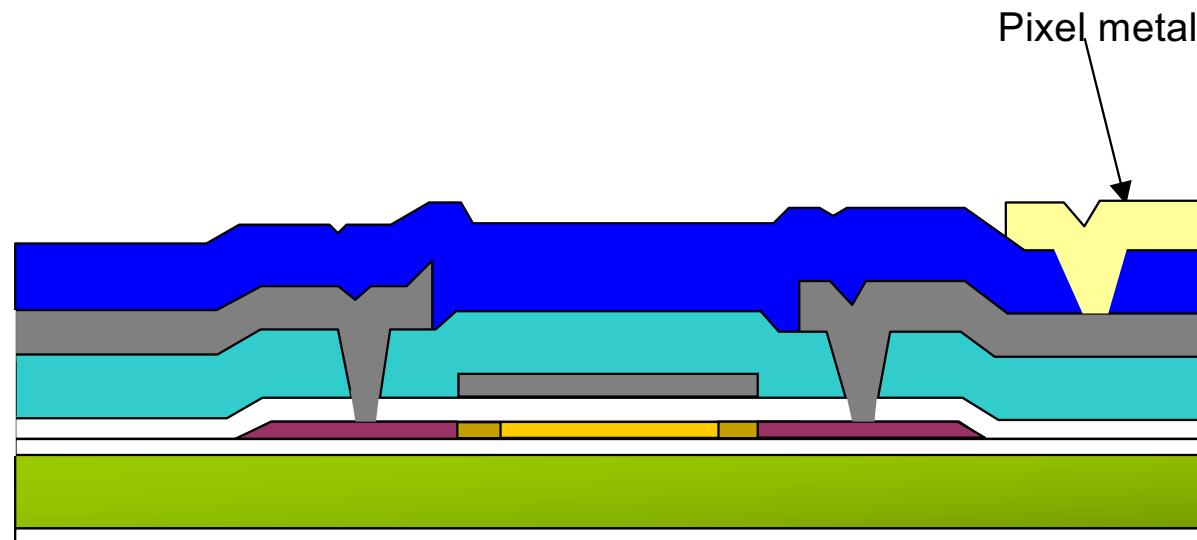


- Organic layer is cleared at edge of display over lead-ins

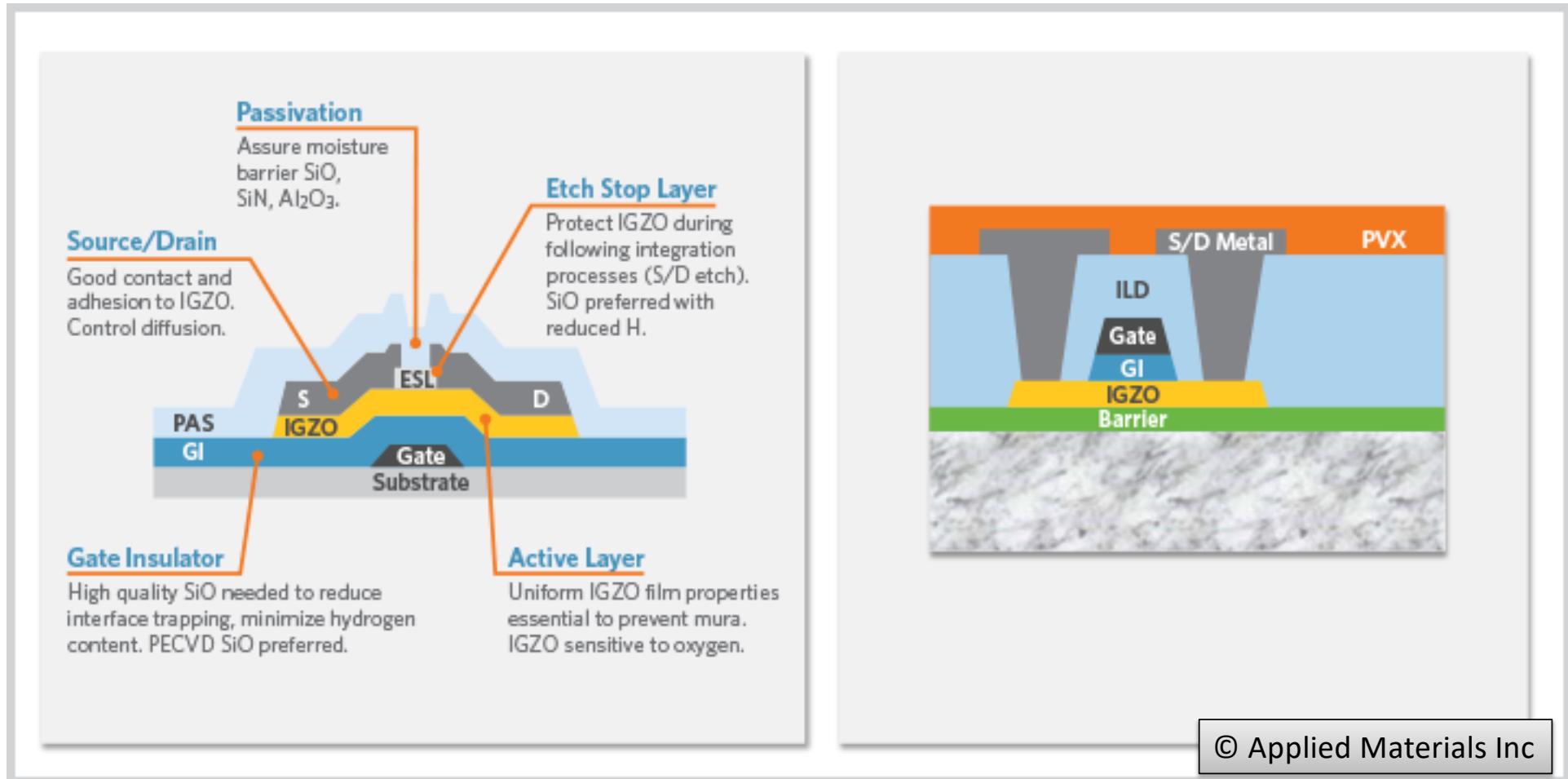
Mask 10: “Pixel”

Deposit ITO (transmissive)

– Pattern & Etch



IGZO – Top Gate vs Bottom Gate





SECTION 8

OLED TECHNOLOGY

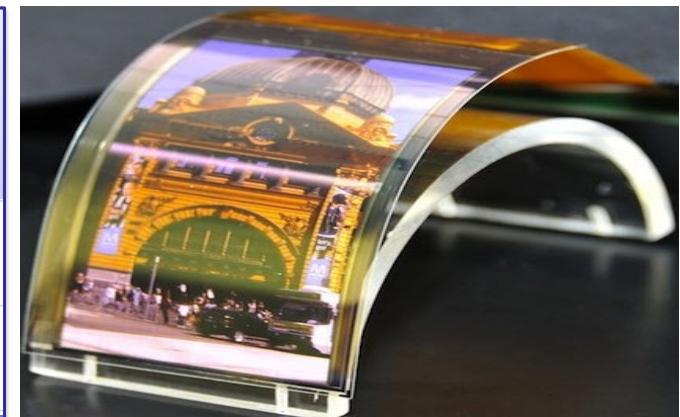
HANDBOOK OF VISUAL DISPLAY
TECHNOLOGY 2ND EDITION (2016)

AMOLED Manufacture

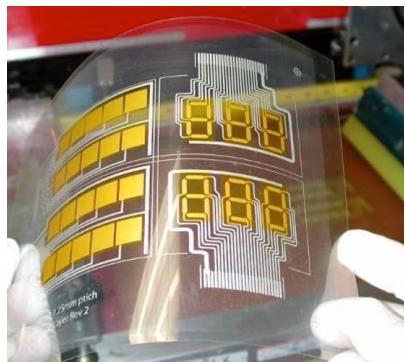
Glory K. J. Chen, Janglin Chen
Pages 1779-1797

Organic Light-Emitting Diodes (OLEDs)

Ruiqing Ma
Pages 1799-1820



Applications of OLEDs - Historical



SM - AMOLED Displays



SONY 24" tiled top emitting



Sony Clie PEG-VZ90
LTPS (480 x 320)
(Multi-media handheld)

OLED International 2005



SONY 13" top emitting



IDT/CMO/IBM 20 " a Si
top emitting



eMagin 0.72 " microdisplay on Si
White with CFA – top emitting



AUO / UDC 4" a Si bottom emission

Organic LED Device Classification

MATERIAL FAMILY

Small molecule Polymer long chain

LIGHT EMISSION

Fluorescent Phosphorescent

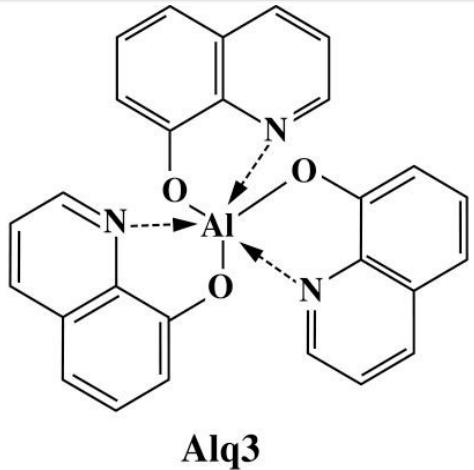
MANUFACTURING

Vacuum process Solution process

“I think you’ll find it’s a little bit more complicated than that”

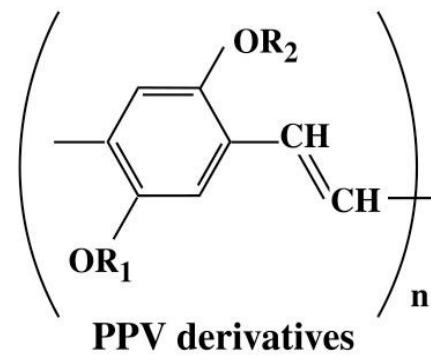
Two Main families of materials

Tris(8-hydroxyquinolino)aluminium

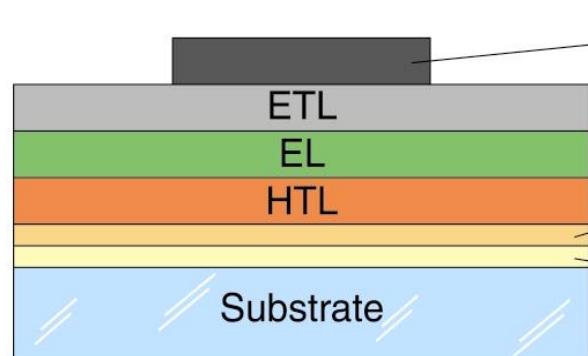


Alq3

Polyparaphhenylenevinylene (PPV)



PPV derivatives



Evaporated molecule based OLED



Polymer based OLED

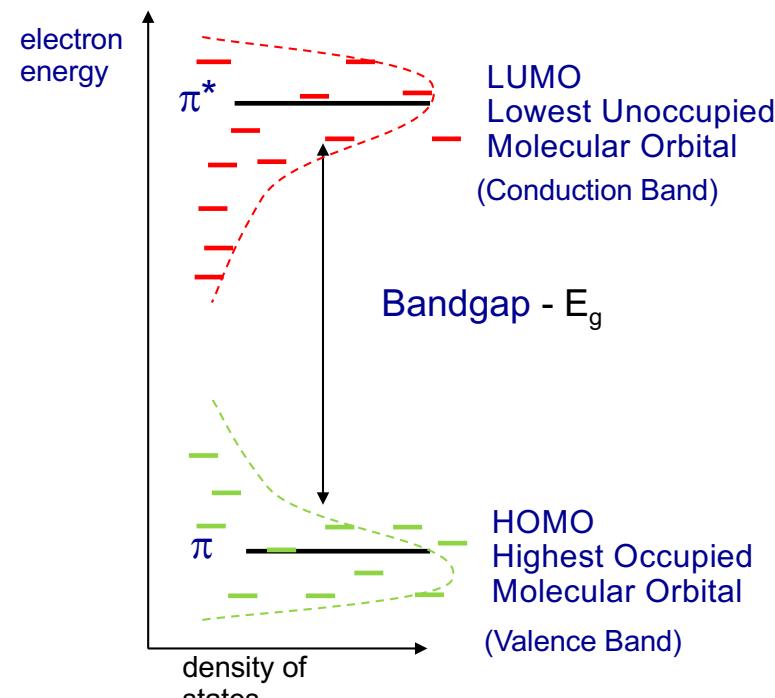
Electronic structure

The bonding state (π) forms the HOMO level, while the anti-bonding state (π^*) forms the LUMO level.

These are roughly analogous to the valence and conduction band in inorganic semiconductors

Due to disorder, charges are localised within the conjugation length

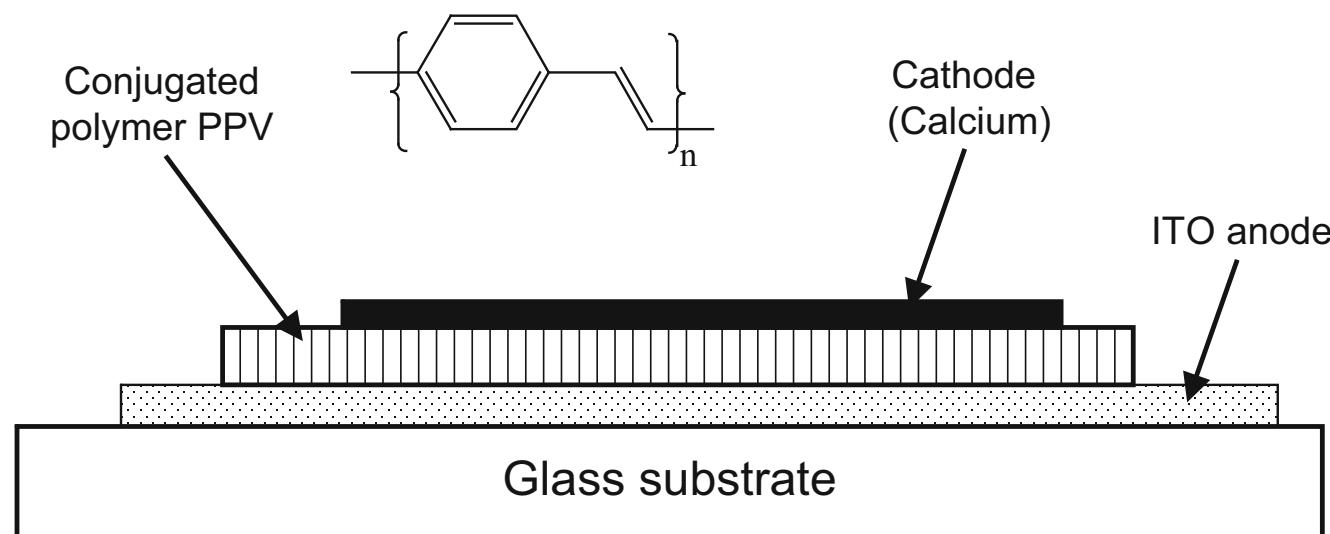
- several repeat units long



Broad distribution of energy levels



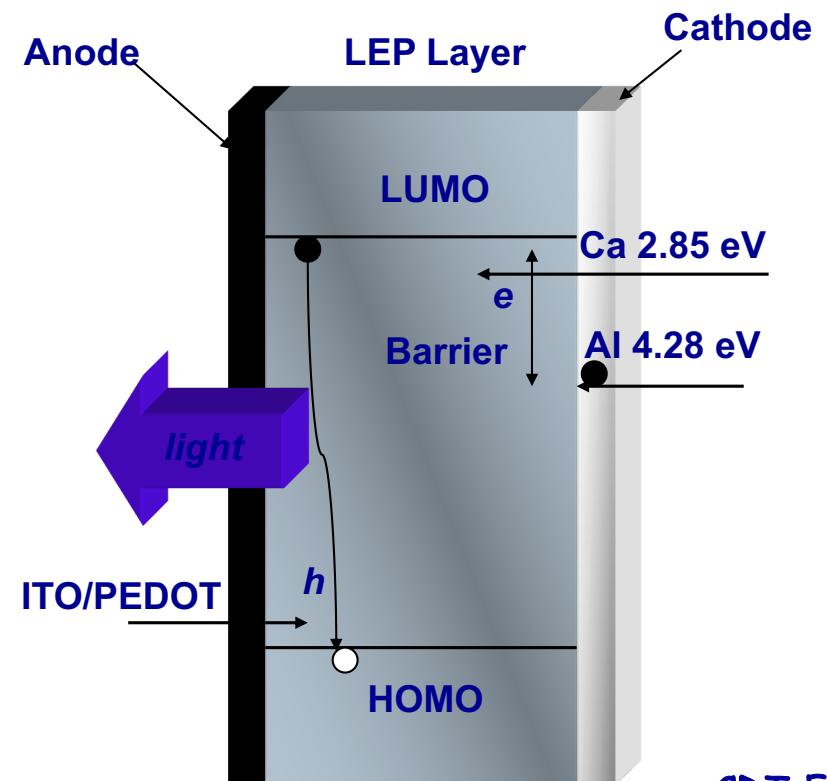
Simple Polymer OLED



Burroughes JH, Bradley DDC, Brown AR, Marks RN, Mackay K, Friend RH, Burn PL, Holmes AB (1990) Light-emitting diodes based on conjugated polymers. *Nature* 347:539–541

OLED – principle of operation

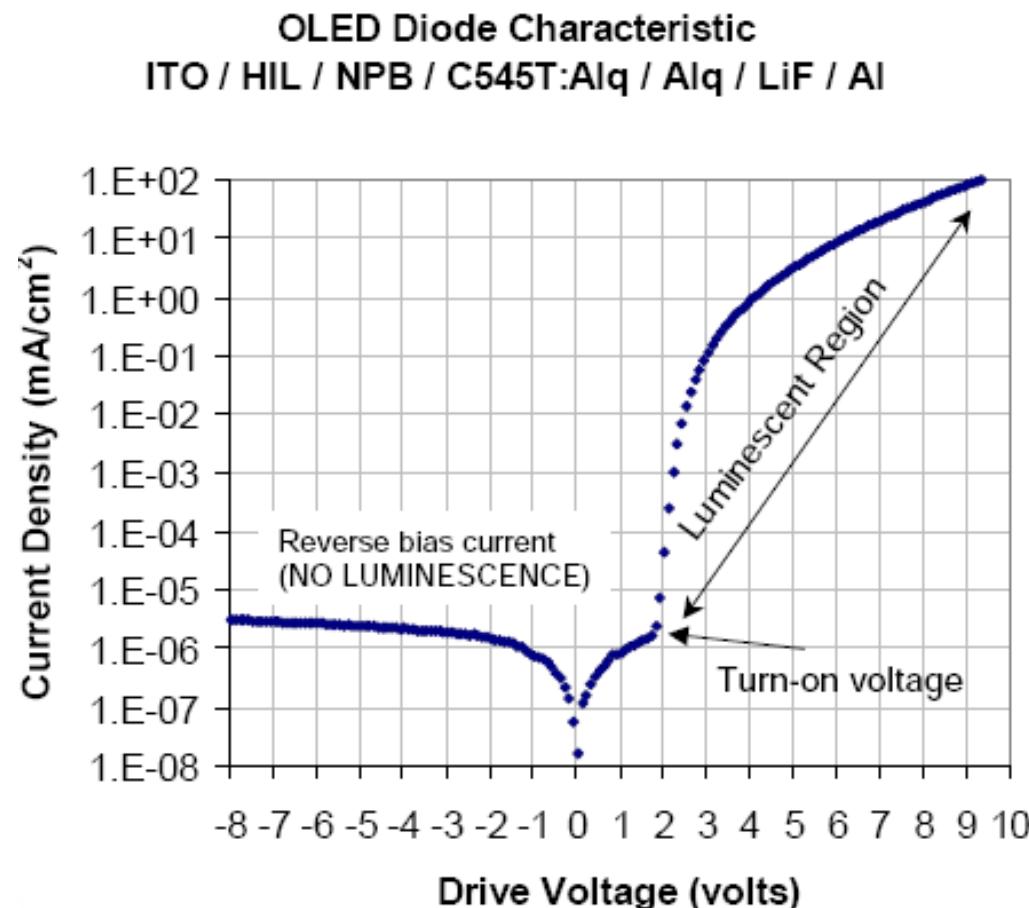
- Low work function cathode to assist electron injection
- High work function anode to assist hole injection
- High mobility to reduce voltage and increase recombination probability
- Colour of emission is determined by HOMO-LUMO energy gap



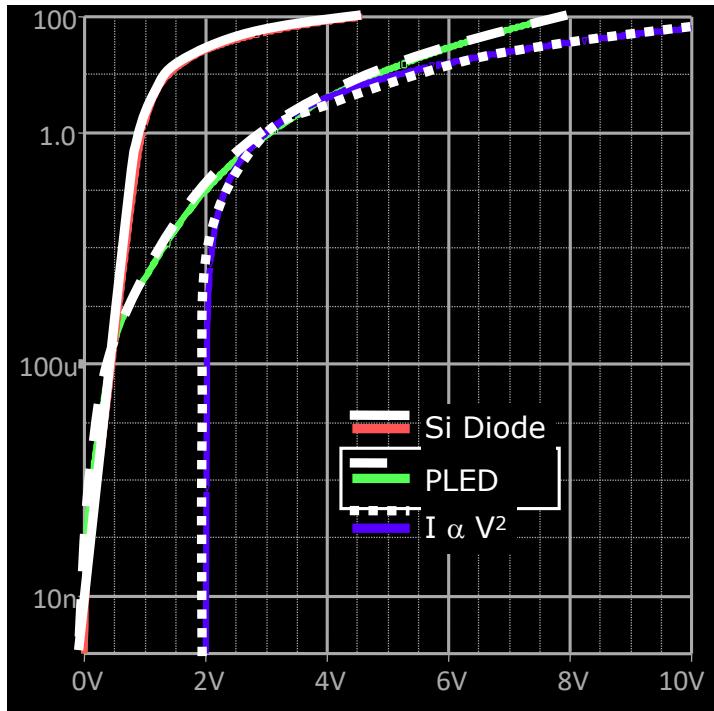
CDT-ES

Viewgraph courtesy CDT

Typical IV Characteristic



Device Operation – IV characteristic



Log-linear plot of IV characteristics

The chart left shows the I-V characteristics of a silicon diode and a PLED

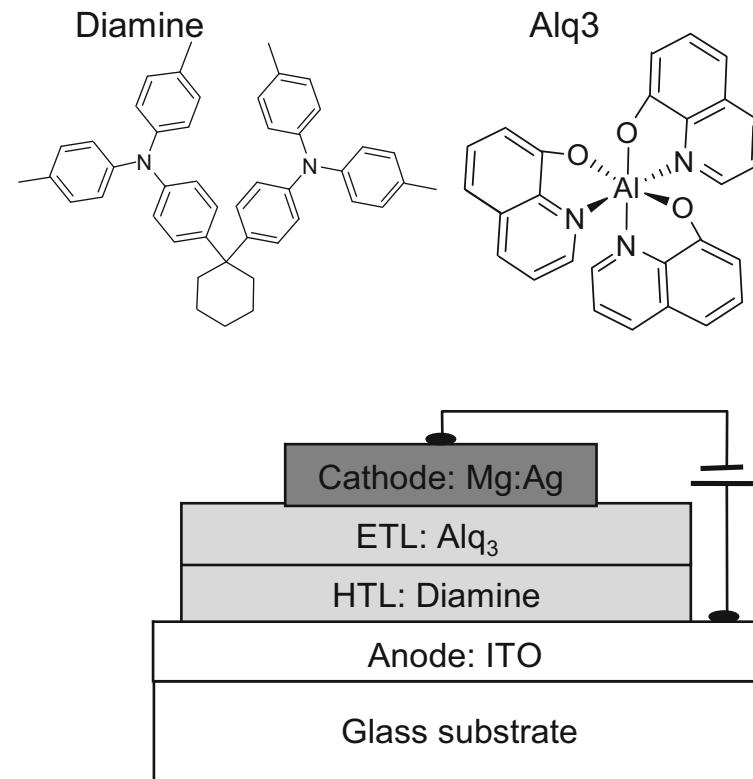
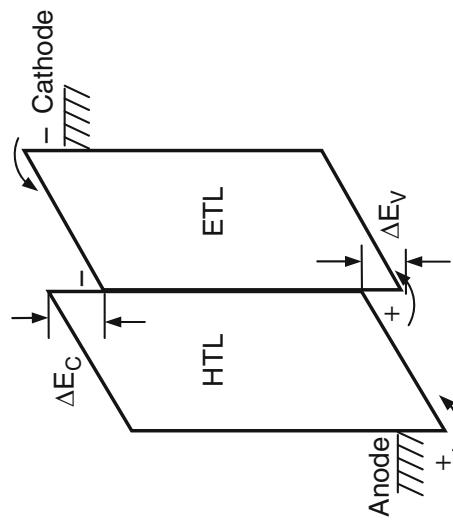
The silicon diode shows an exponential I-V curve, and is therefore injection limited

The PLED lies between the exponential and quadratic

The PLED is space-charge limited, however a field dependent carrier mobility increases the power relationship with field

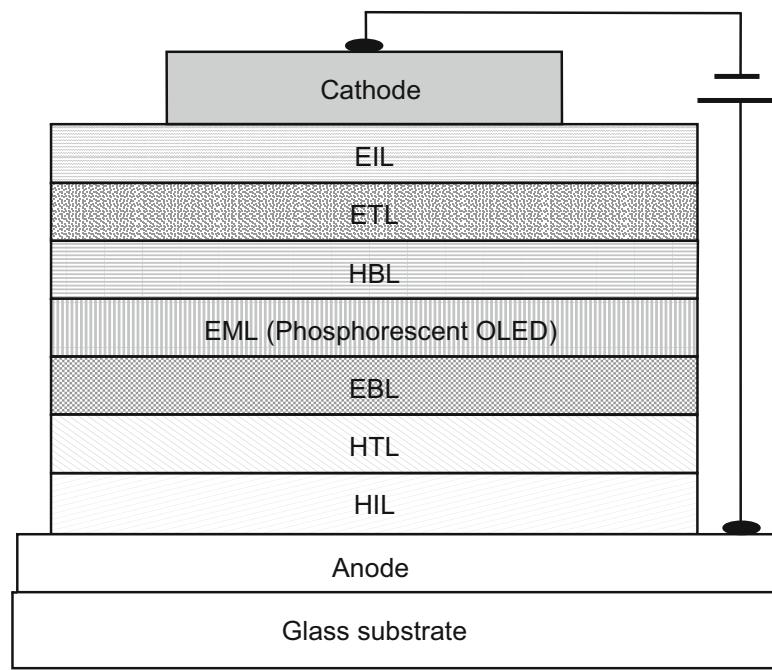
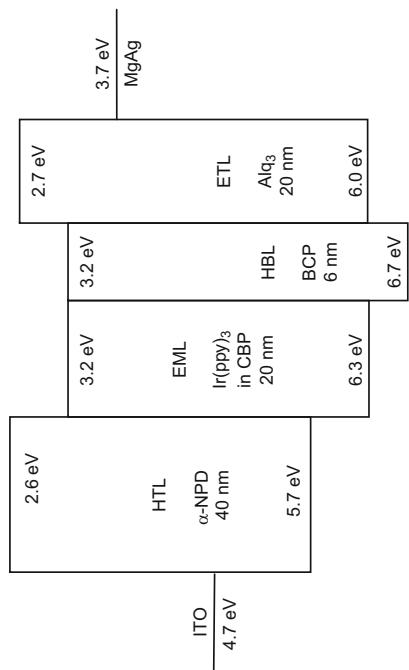
Simple Bilayer OLED Device

Cross Section and
Energy Band diagram
*Reproduced from Tang
and VanSlyke (1987)*

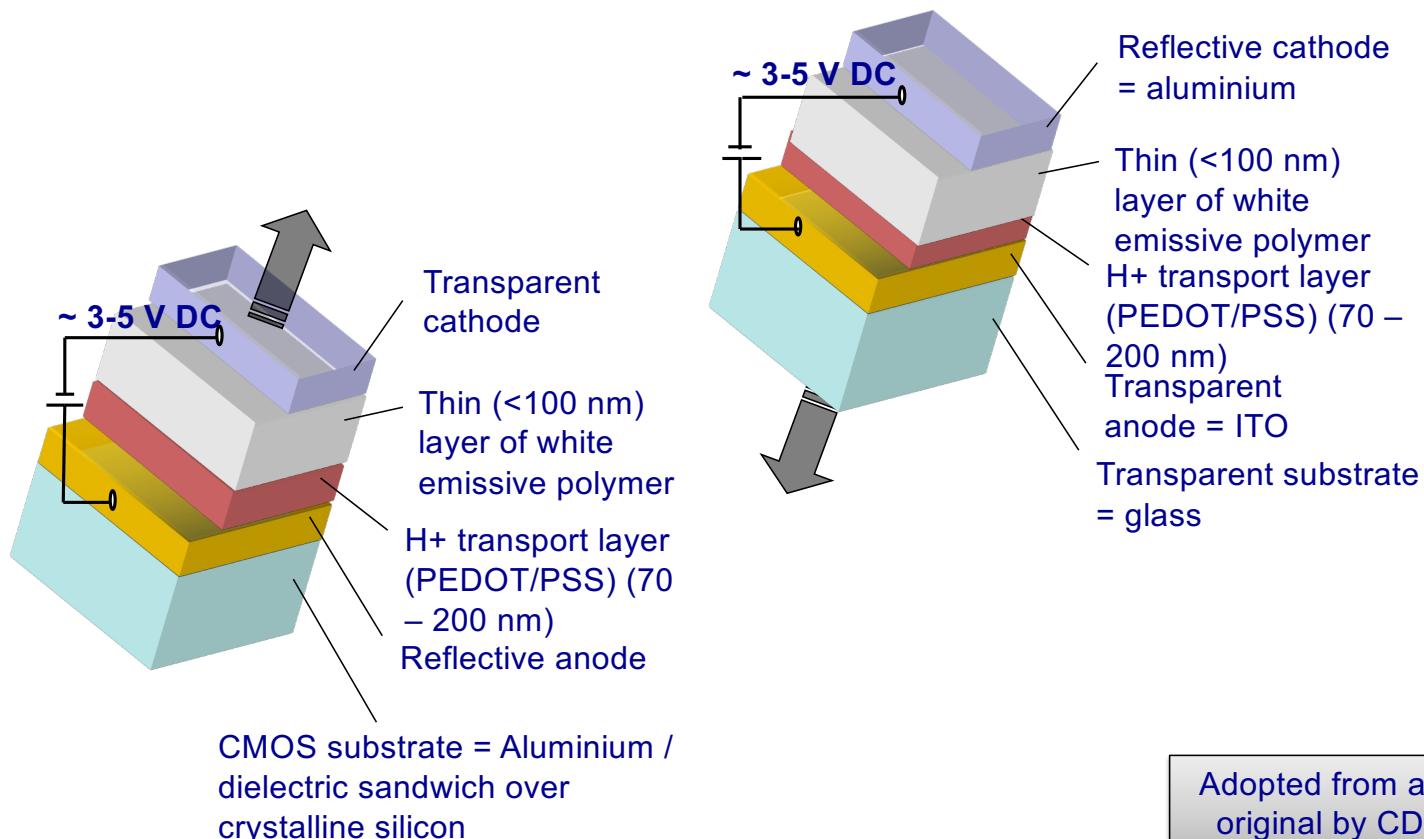


Advanced high-efficiency OLED Device

Energy level diagram of a phosphorescent OLED device with ITO anode; Mg:Ag cathode; HTL, EML, HBL, and ETL organic layers



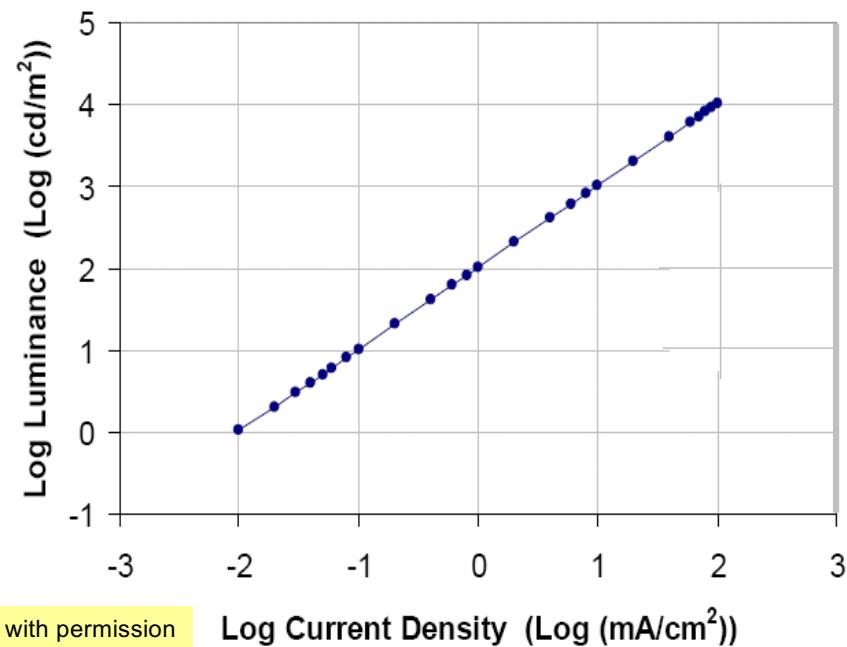
OLED – bottom and top emitting



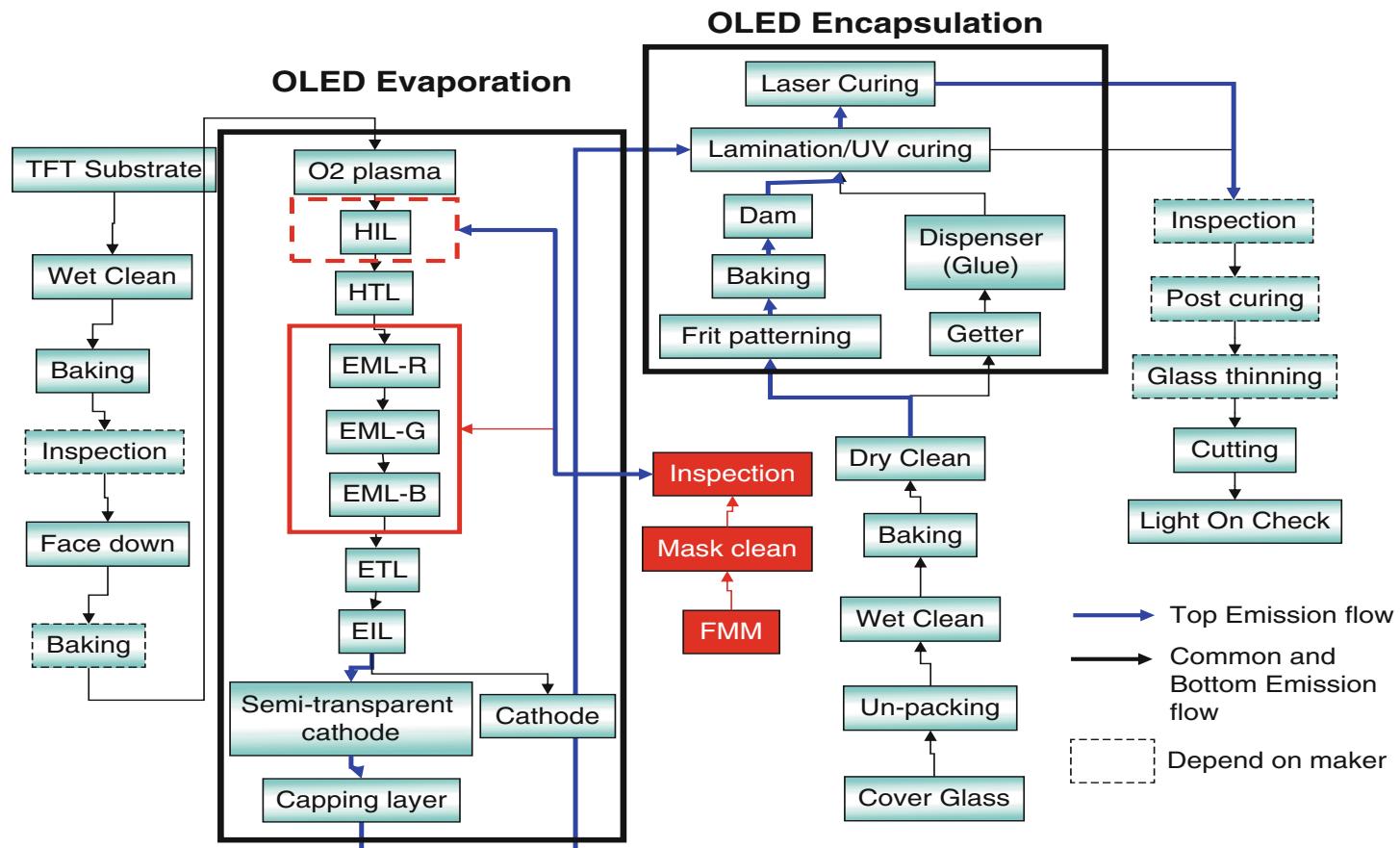
OLED Optical response

OLED response is highly linear

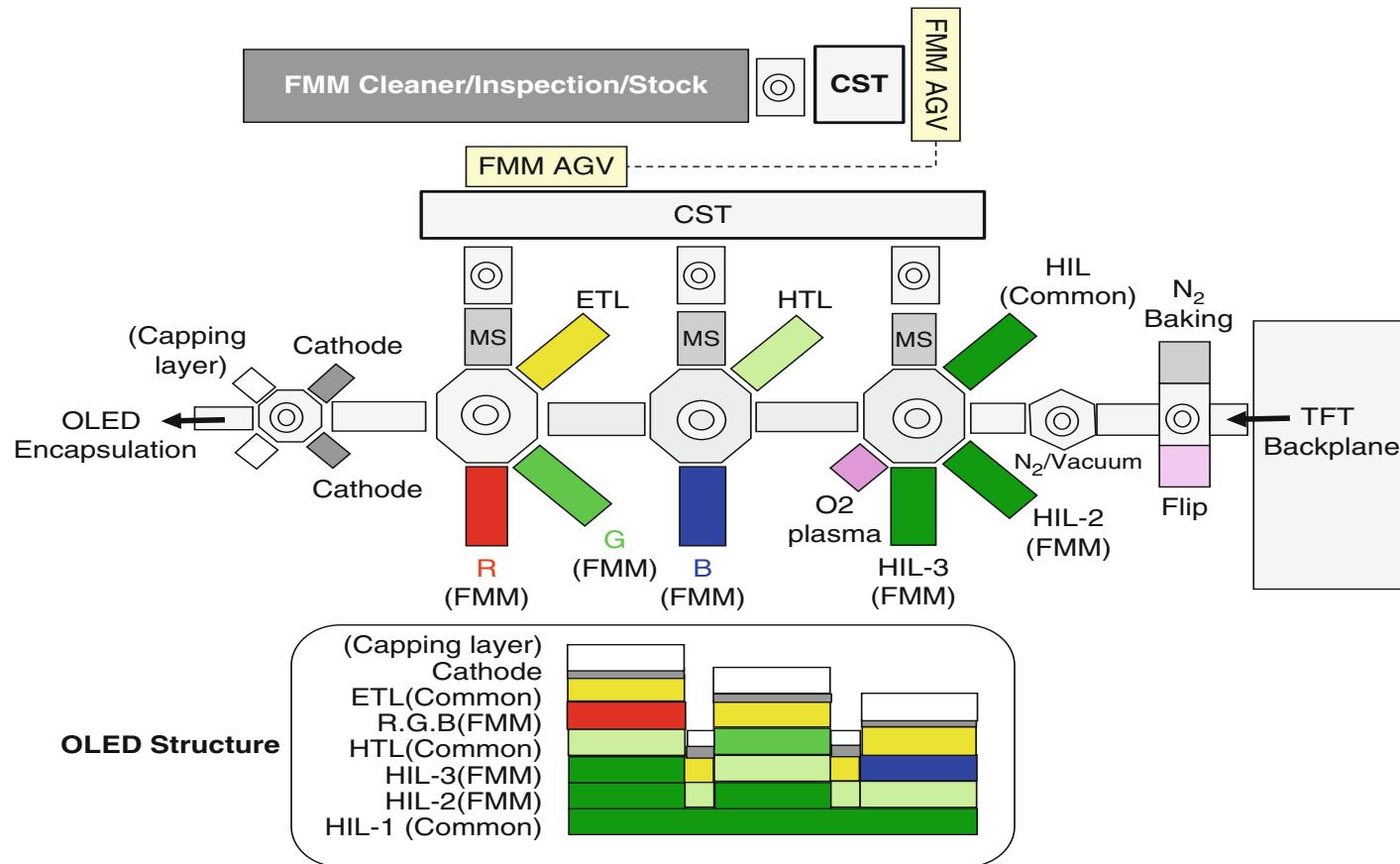
Luminance proportional to current density over many decades of dynamic range



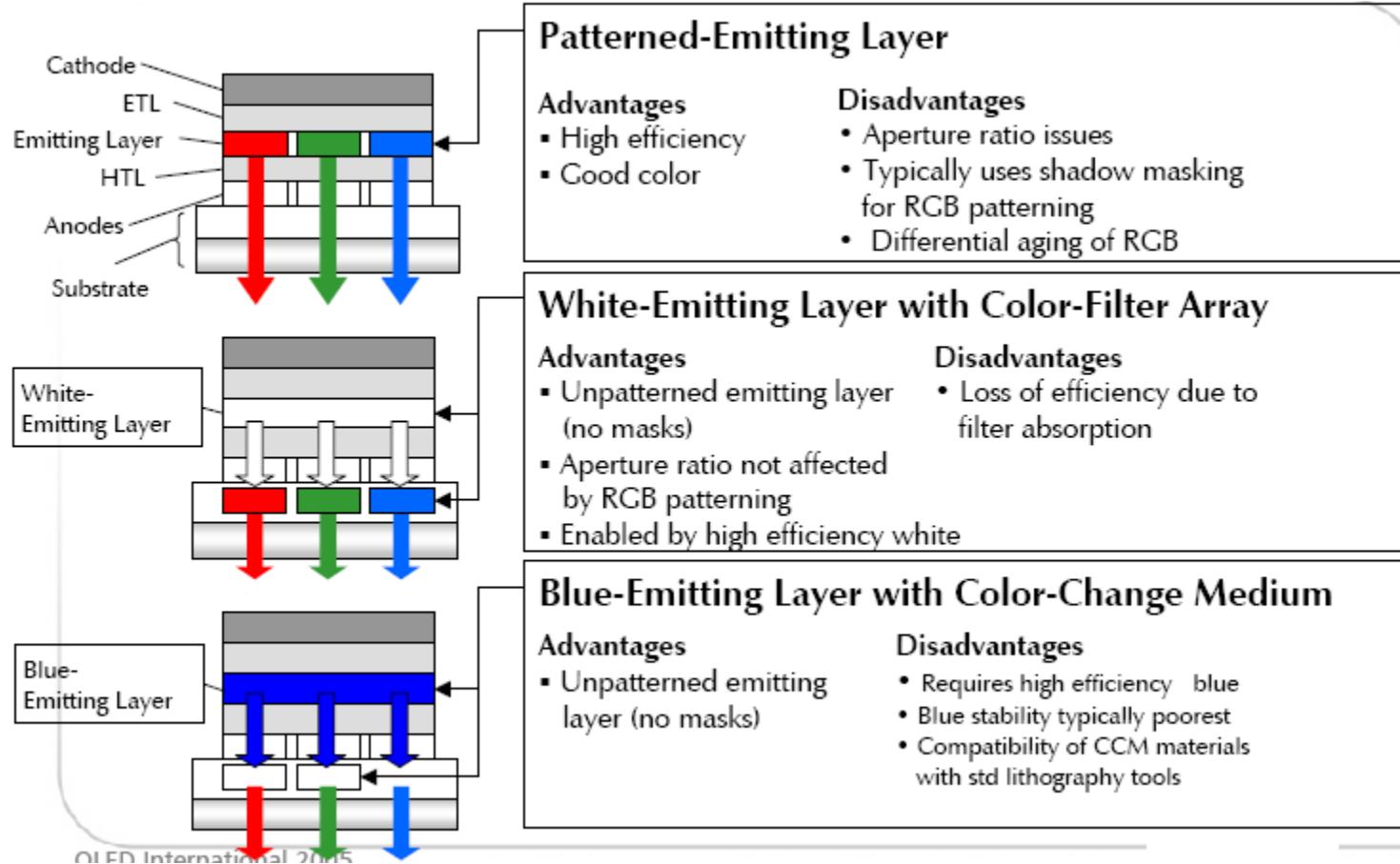
OLED Manufacturing Process Flow



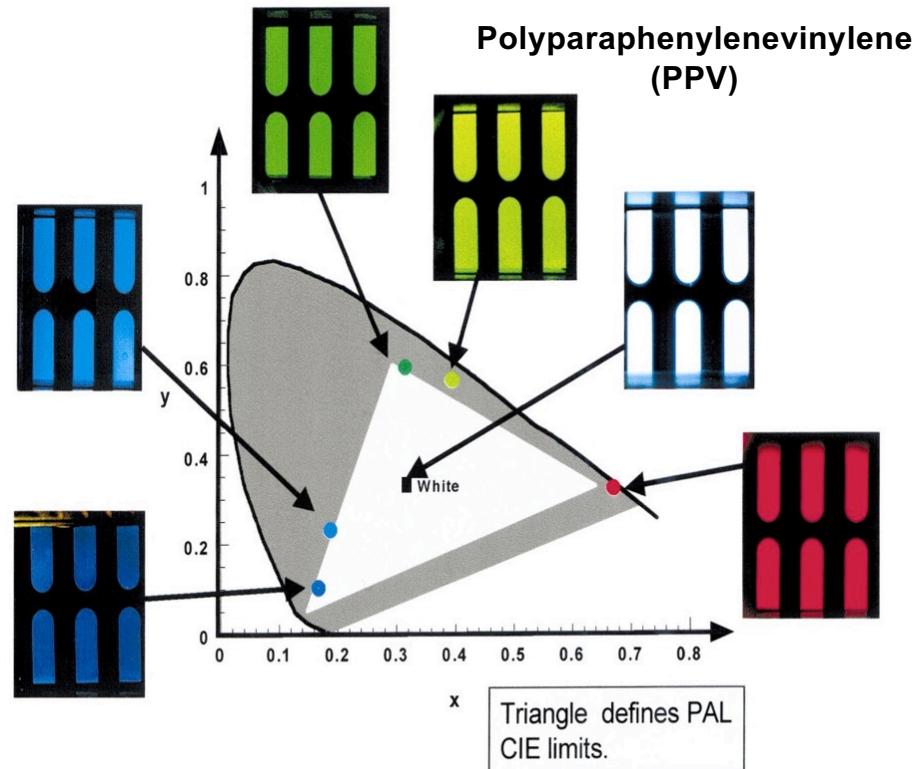
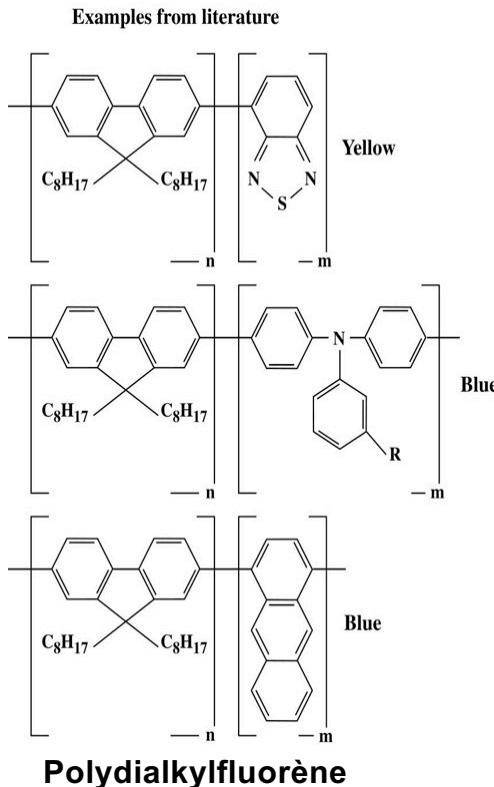
OLED Manufacturing Equipment Schematic



Creating RGB Colour in OLEDs



Colour tuning by chemical modification

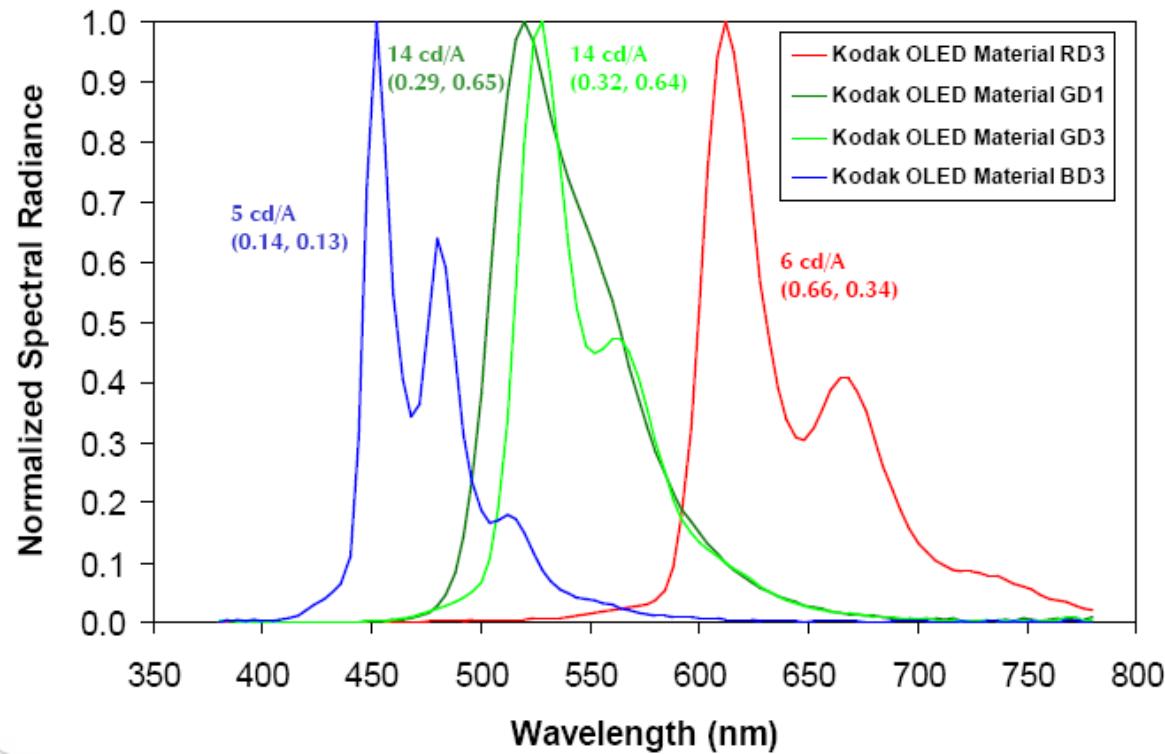


Colour from OLEDs



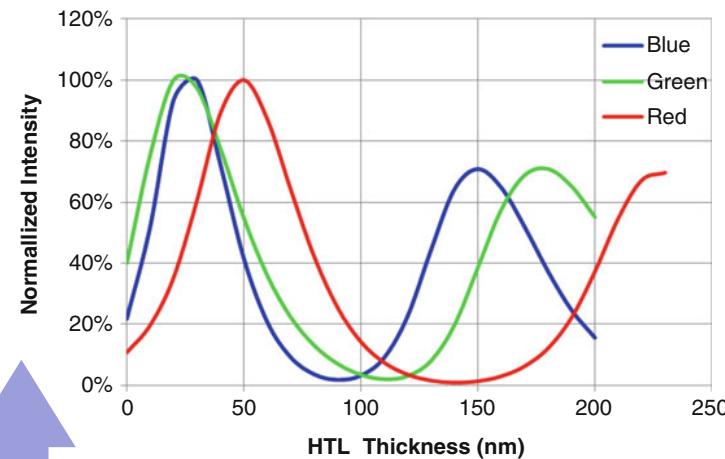
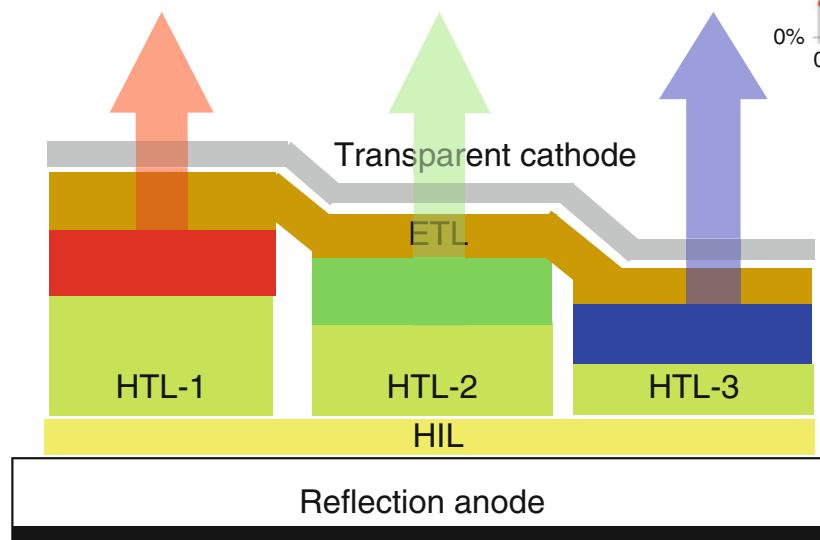
Typical Electroluminescent Spectra

C|D|T



Colour tuning

The “cavity” in which the OLED is located affects the colour efficiency



Properties for Different Colors

Colour	Efficiency @100cd/m ² (lm/W)	Voltage @100cd/m ² (V)	Luminous intensity @5.5V (cd/m ²)	Time to half luminous intensity at room temp.
Red	2.3	2.4	2,000	>40,000
Green	11	2.7	20,000	>25,000
Blue	2.5	3.5	2,000	>6,500
Yellow	7 18	3 2.1	2,000 100,000	60,000 ~14,000
White	1.5	4.3	400	>10,000

NB. Beware that this data improves rapidly
Check independently for up-to-date figures

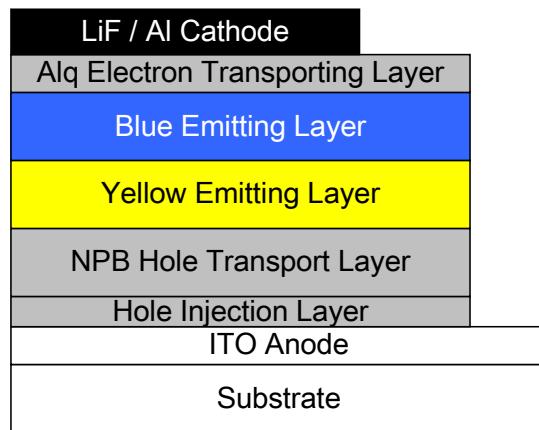
CDT-ES

STATE OF THE ART

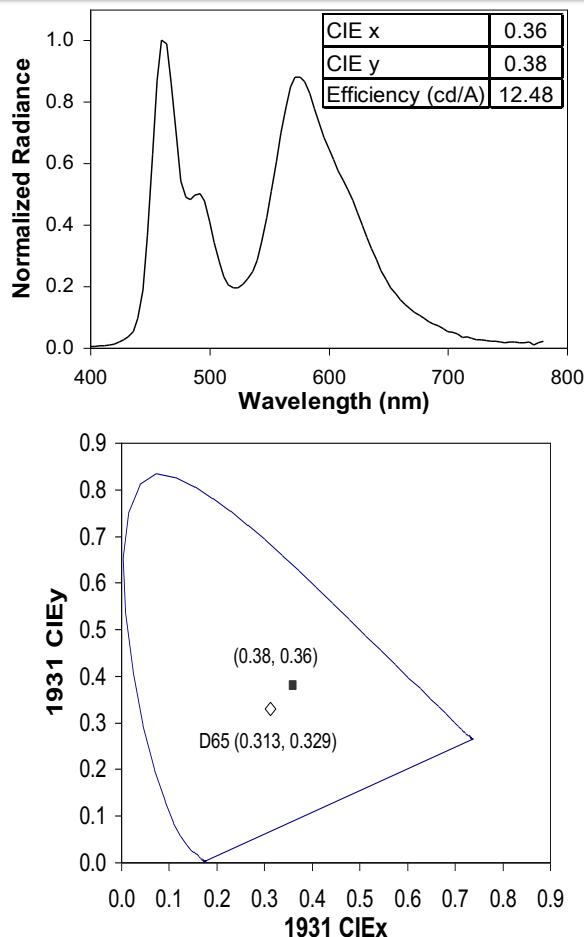


2019
LG's 88in Signature OLED
TV is only 2.5mm thick

White emitting OLED (1) for lighting



Note: Better power efficiency results if white point of emitter = D65



OLED Lighting

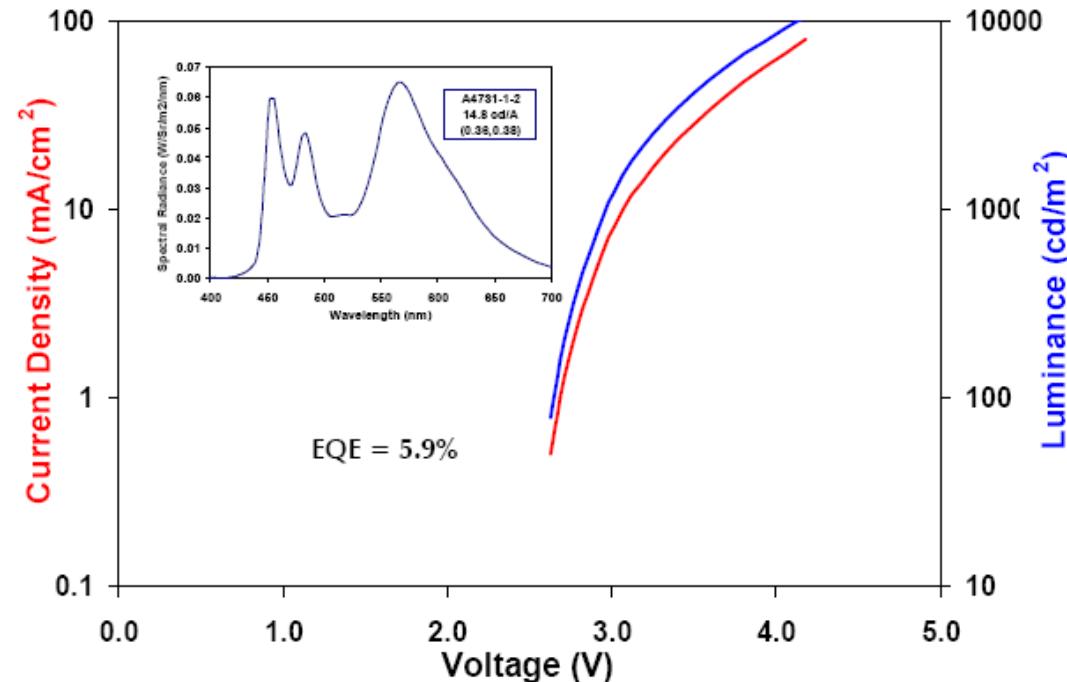


White emitting OLED (2) for display

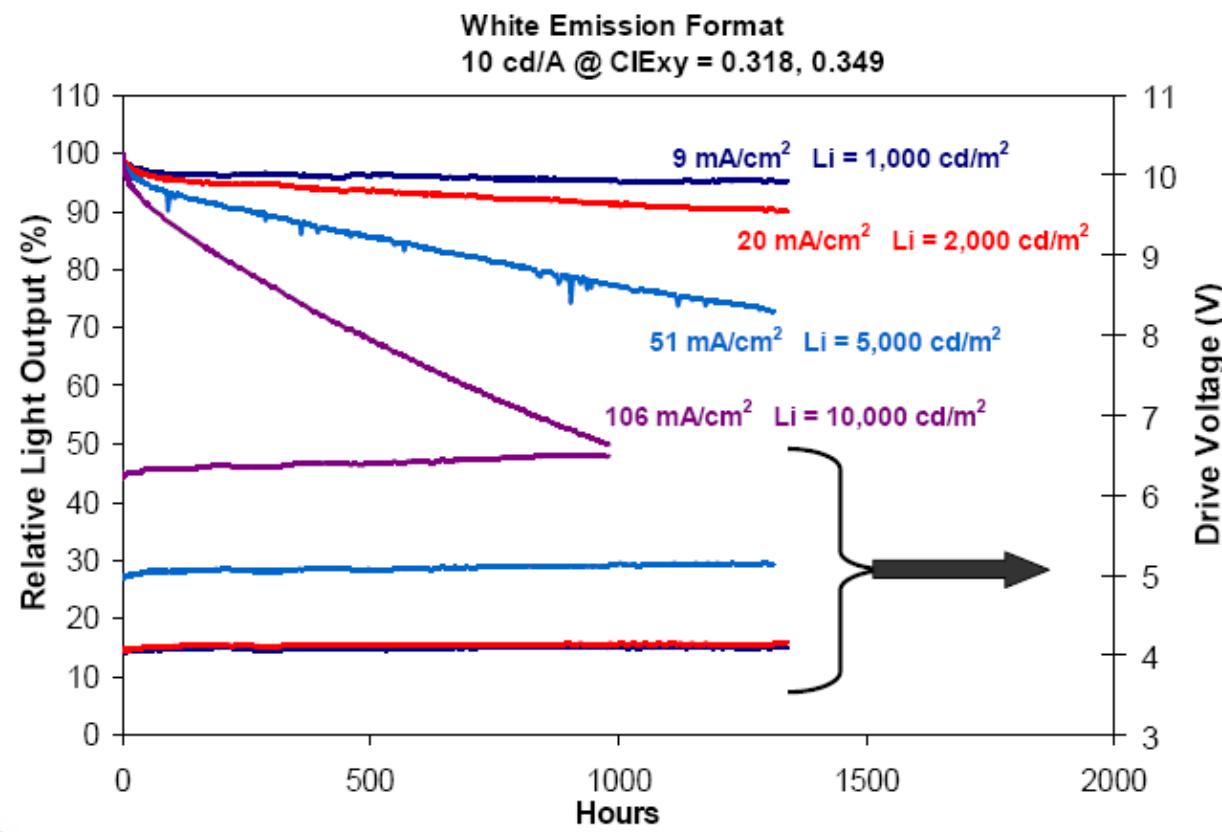


Low Voltage OLED (white)

C|D|T



Reduction in output with use

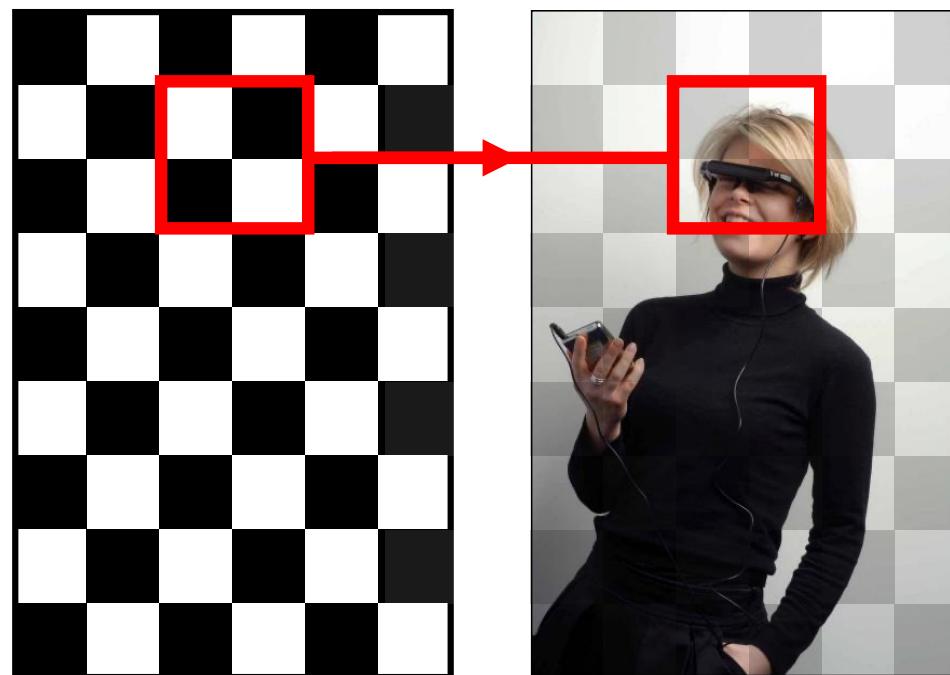


Consequences of OLED Lifetime

Image sticking

Caused by
Differential pixel
ageing

Pixels used
more become
dimmer sooner



Effect of OLED Luminance Characteristics

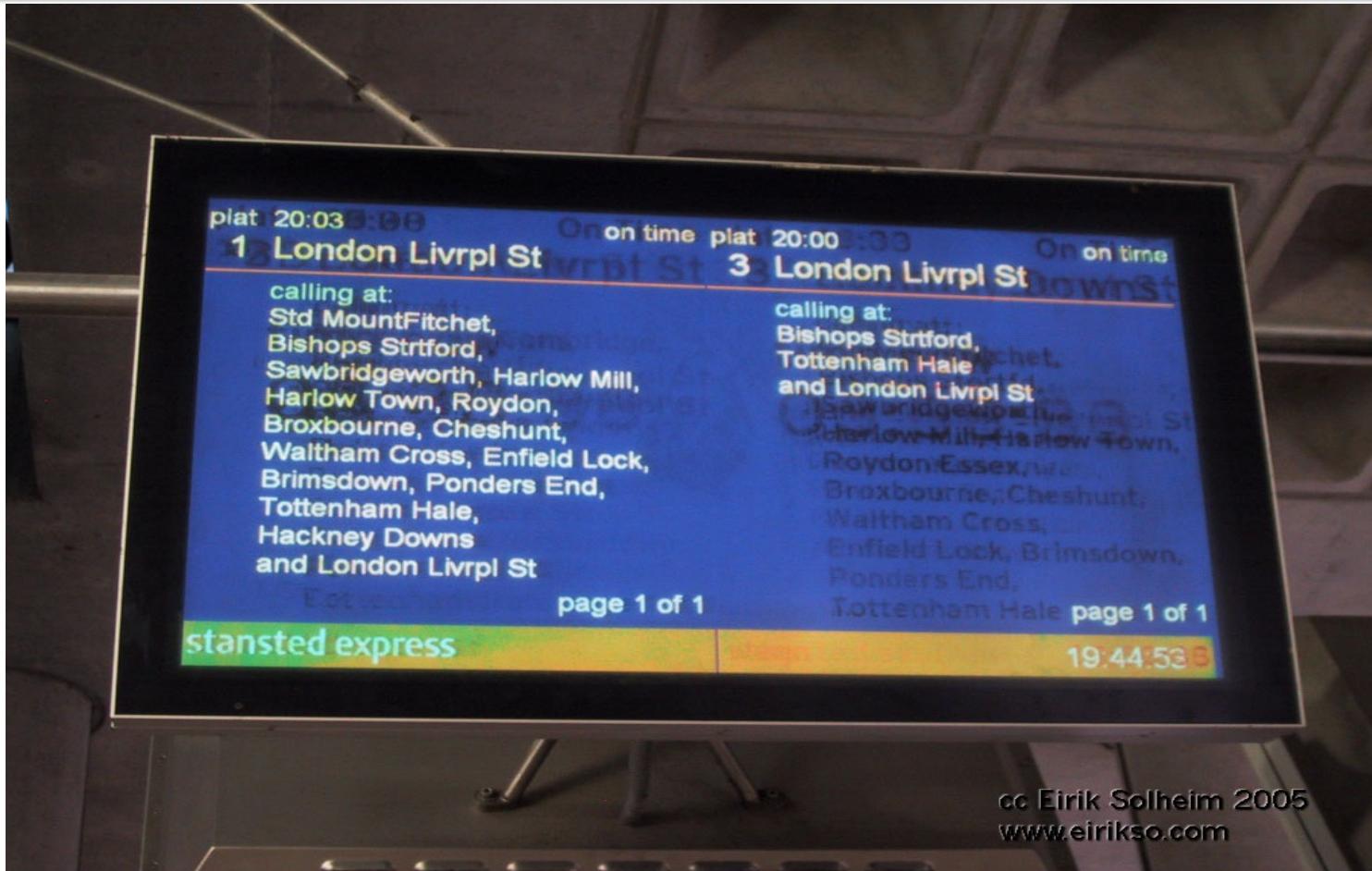
Display “lifetime” is related to material / device lifetime

Display dims with use



Differential color decay rates means
Display acquires color cast with use

Example of image sticking (burn-in) on PLASMA



cc Eirik Solheim 2005
www.eirikso.com

Additional Slides

OLEDs - List of Abbreviations

AMOLED	Active-matrix OLED
AR	Antireflection
BE	Bottom emission
ELA	Excimer laser annealing
EML	Emission layer
ETL	Electron transport layer
FPD	Flat panel display
FMM	Fine metal mask
HIL	Hole injection layer
HTL	Hole transport layer
LTPS	Low temperature polysilicon
NTSC	National Television System Committee
RPL	Redundant pixel line
SBS	Side-by-side
TE	Top emission
VAS	Vacuum assembly system
WOLED	White organic light-emitting diode

Charge injection

Work-function does not line up with HOMO, LUMO

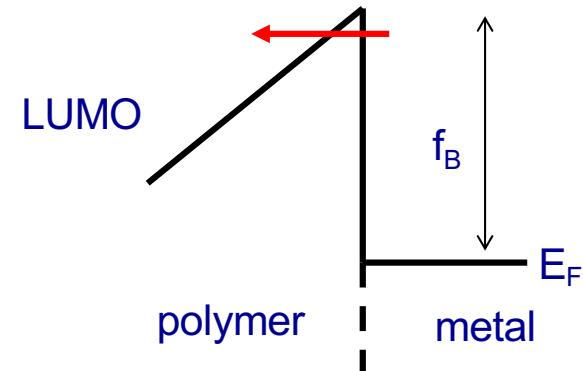
- potential barriers at the interfaces between electrodes and semiconductors

Thermionic emission

$$J = AT^2 \exp(V_{app} - q\varphi_B)/kT$$

Tunnelling

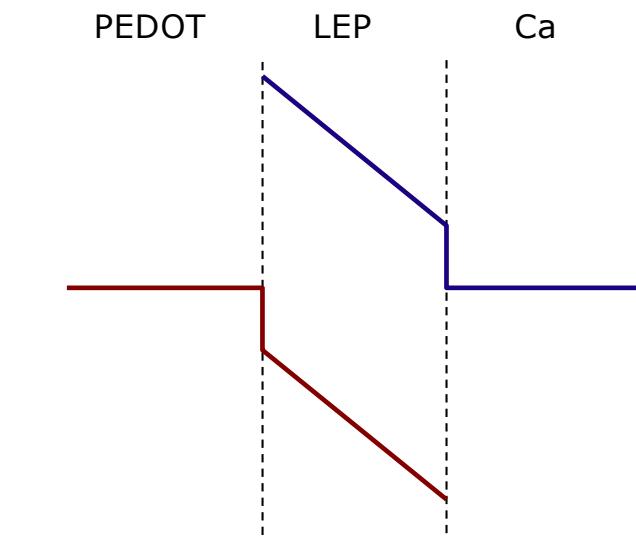
$$J = CE^2 \exp(-E_0/E)$$



At low bias and high barriers current limited by injection

better engineering of the barrier heights (interfacial chemistry) leads to improvement in performance (low threshold voltages)

Device Operation – zero bias



Polymer OLED zero bias condition

Left is an OLED device under zero bias

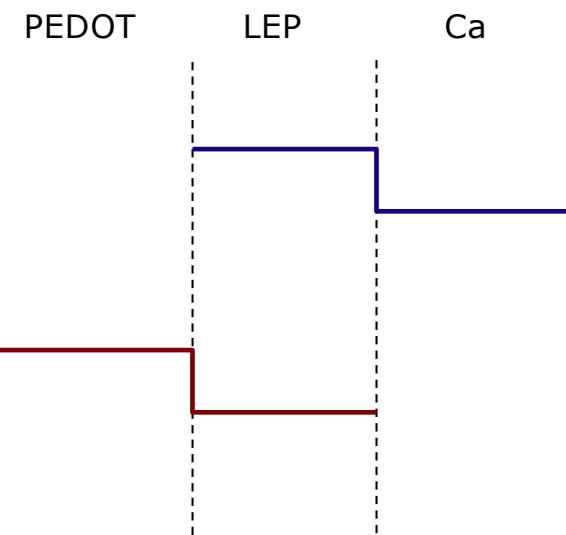
The carrier mobility in both the anode and cathode is much greater than in the LEP

- All the built-in field falls across the LEP

A (very) small current can flow due to dissociation of photo-excited excitons.

Under reverse bias small leakage currents will dominate

Device Operation – threshold

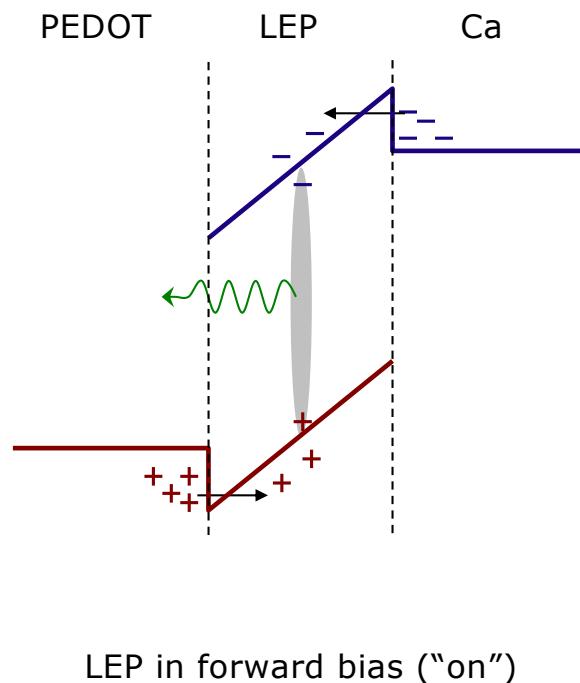


Left is an OLED device
at turn-on threshold
("flat-band" condition)

Thermionic emission
allows carriers over the
barriers to injection
– Temperature
dependent

Polymer OLED in flat-band condition

Device Operation – carrier injection



Left is an OLED under forward bias
bias

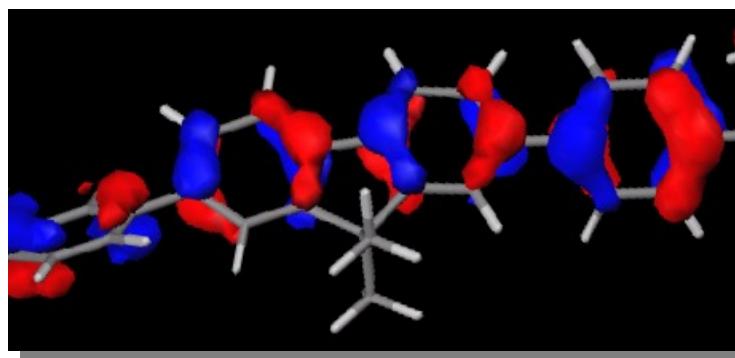
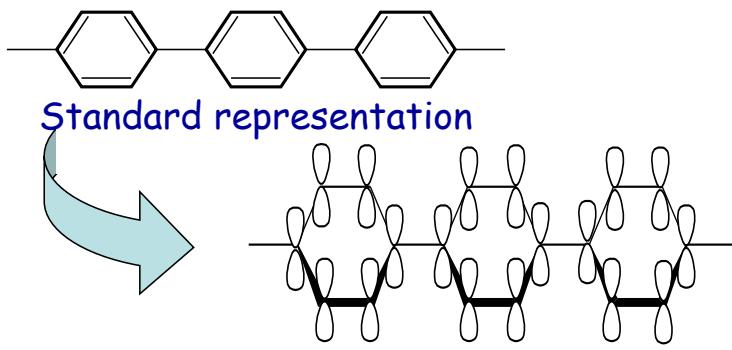
The current passing through any diode will be limited by either

- Carrier injection
- Space-charge

An injection limited device will be characterised by an exponential current-voltage relationship

A space-charge limited device will have a quadratic current-voltage relationship

Conjugated polymers



HOMO level of a polyfluorene

The outer valence electrons can form two types covalent bonds - p and s bonds.

An s bond is the overlap of orbitals of two atoms, and is localised around the axis joining the two atoms.

A p orbital is formed between the un-hybridised p orbitals perpendicular to the axis of the s bond.

Continuous sections of molecules with p bonds are *conjugated*, in this case the p electrons are delocalised along the length of the conjugation.

Electrical conduction in conjugated polymers

Conduction is very different from metals or typical inorganic semiconductors:

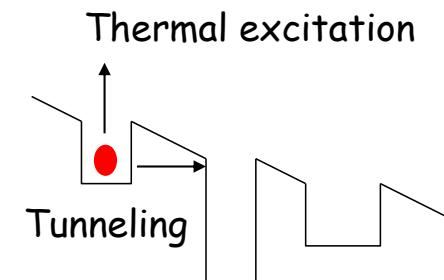
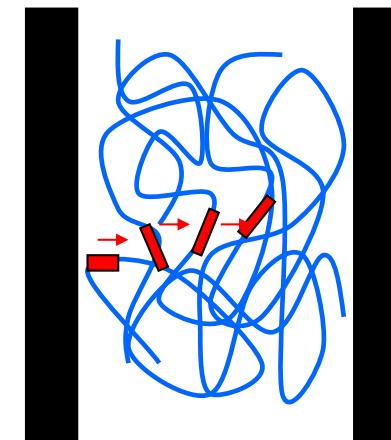
Conjugation breaks present energy barriers to free charge flow. In this type of situation conduction proceeds via *hopping*.

Charge Mobility μ is used to characterise conduction: $v = \mu E$

Mobility is very low compared to inorganic semiconductors

($<10^{-3}$ cm²/Vs)

Mobility depends on the electric field



State of the Art

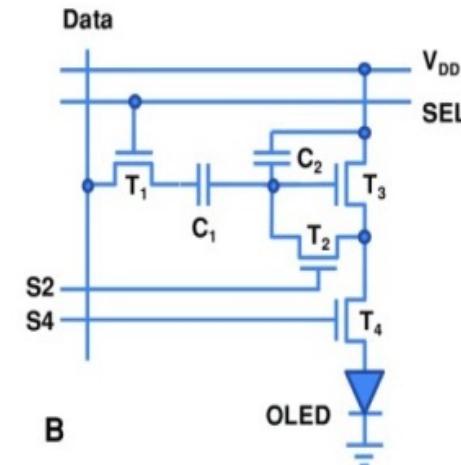
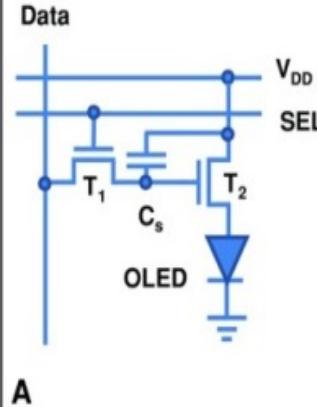


Top: LG Display (Luflex)
Bottom left?
Right: DesignLED (not OLED)



Applications of OLEDs - Lighting





SECTION 9

OLED DISPLAY ELECTRONICS

HANDBOOK OF VISUAL DISPLAY TECHNOLOGY 2ND EDITION (2016)

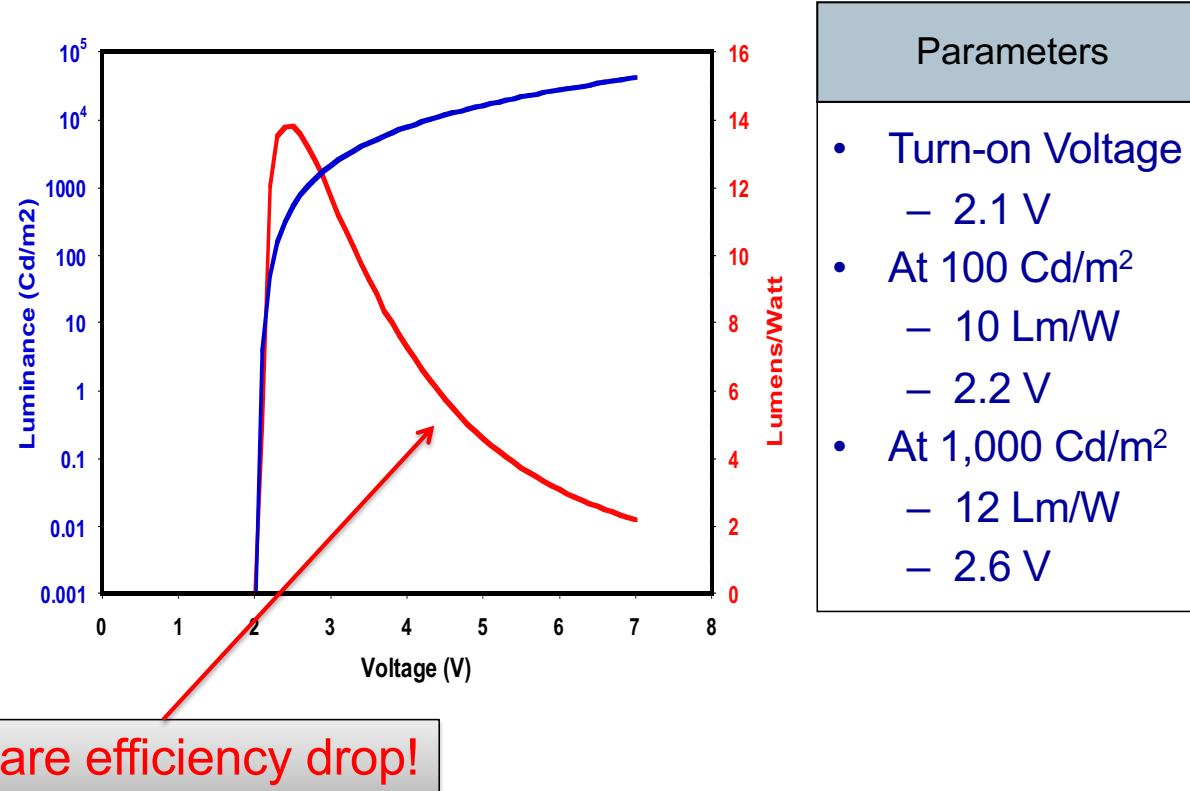
Active Matrix for OLED Displays

Ruiqing Ma

Pages 1821-1841

Example device performance

CDT Yellow, Ink Jet Printed – Luminance and Efficiency

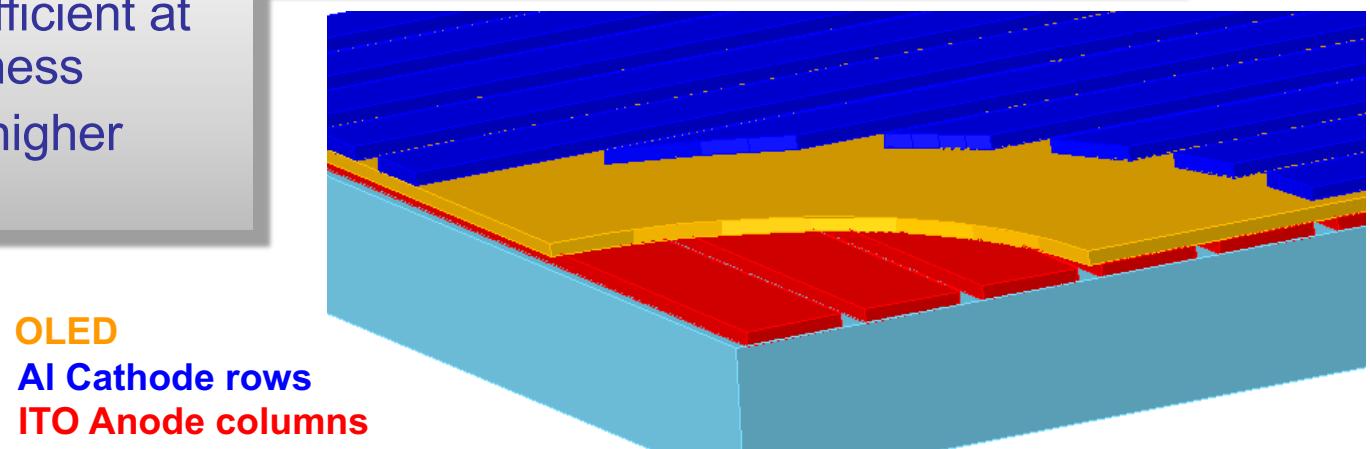


OLED / LCD Addressing - Compare

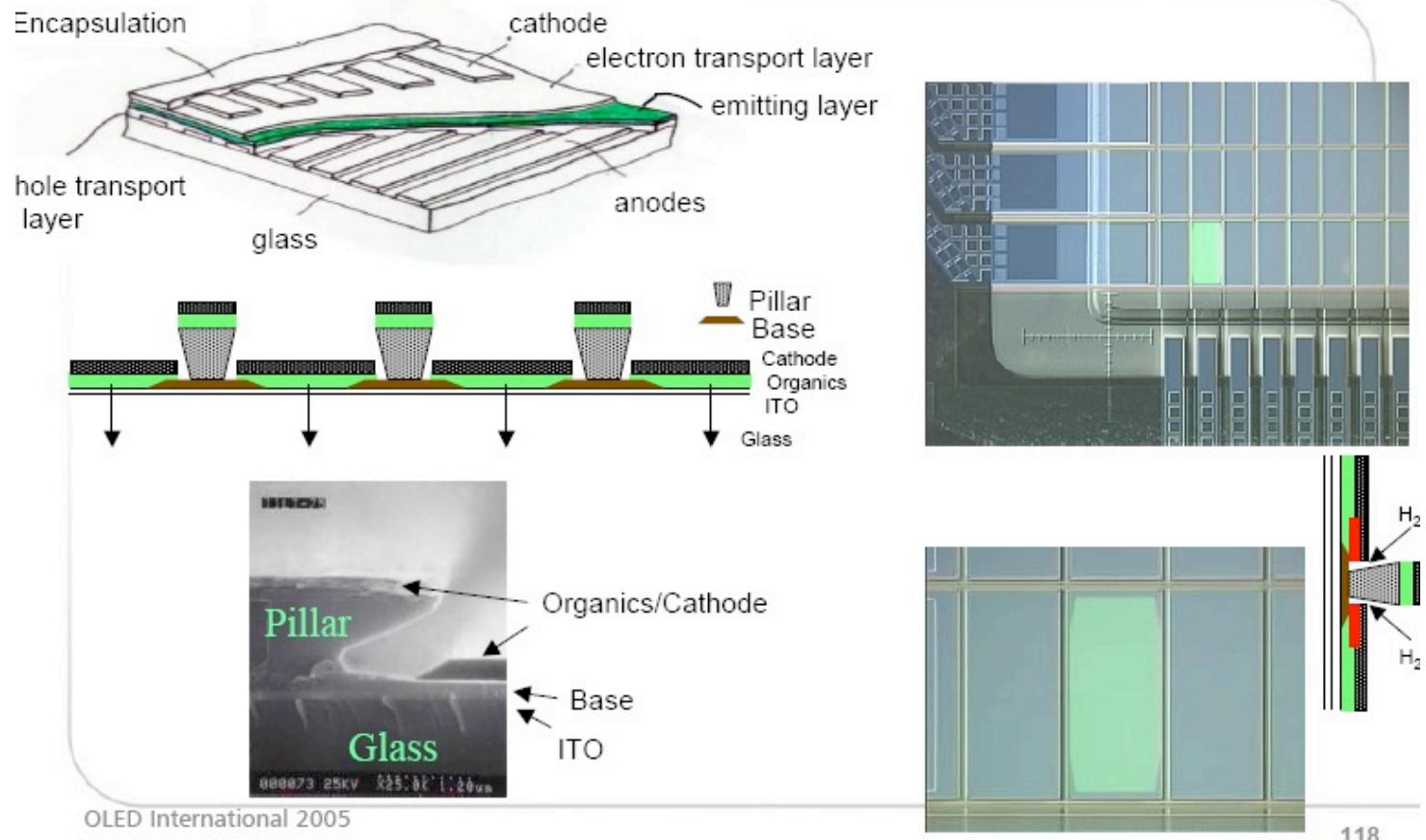
Parameter	LCD	OLED
Optical	Modulating (backlit)	Emissive
Electronic	Capacitive	Diodic
Drive	Voltage	Current
Polarity	a.c. (rms)	d.c.
Switching	>ms	< μ s

Passive Matrix OLED Displays

- Simplest structure for a matrix display
 - Usually ITO anodes are ‘columns’ and Al cathodes are ‘rows’ due to the large peak currents the rows must cope with
 - Only one row active at any time, rows are activated in sequence within one ‘frame’
 - Columns are driven, illuminating the pixels on the currently active row
- Devices are less efficient at high pulsed brightness
 - Inevitable due to higher drive voltage



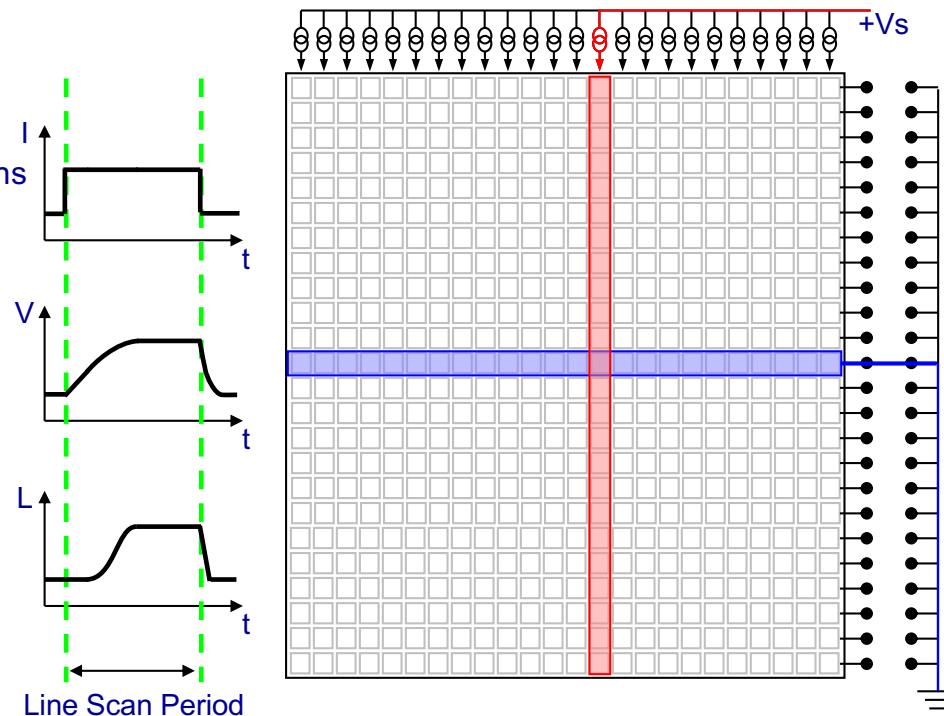
Passive Matrix OLED construction



Passive Matrix Driving

Line-scan Sequence

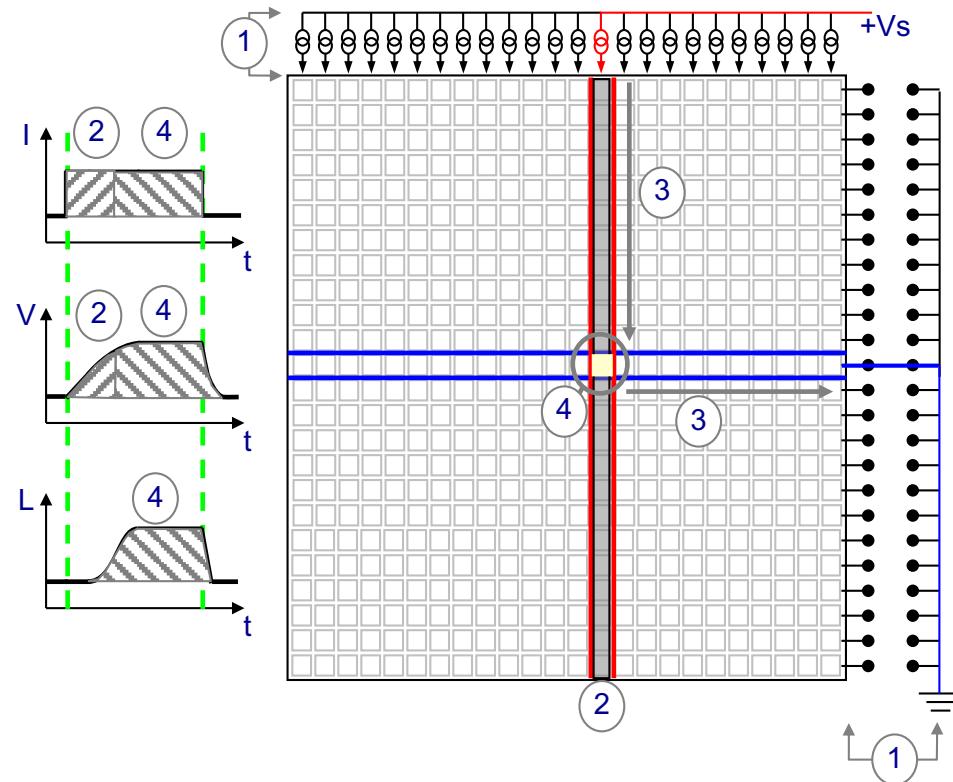
1. Row is selected
2. Current driven onto all columns (only 1 is shown)
3. Capacitance of column charges up
4. Pixel starts to emit light
5. Pixel on full brightness
6. Row is deselected



Passive Matrix Driving – Power Consumption

Four Factors Dominate

1. Driver compliance
2. Column capacitive charging
3. Resistive losses
4. Diode Power



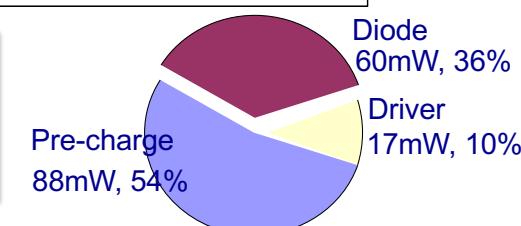
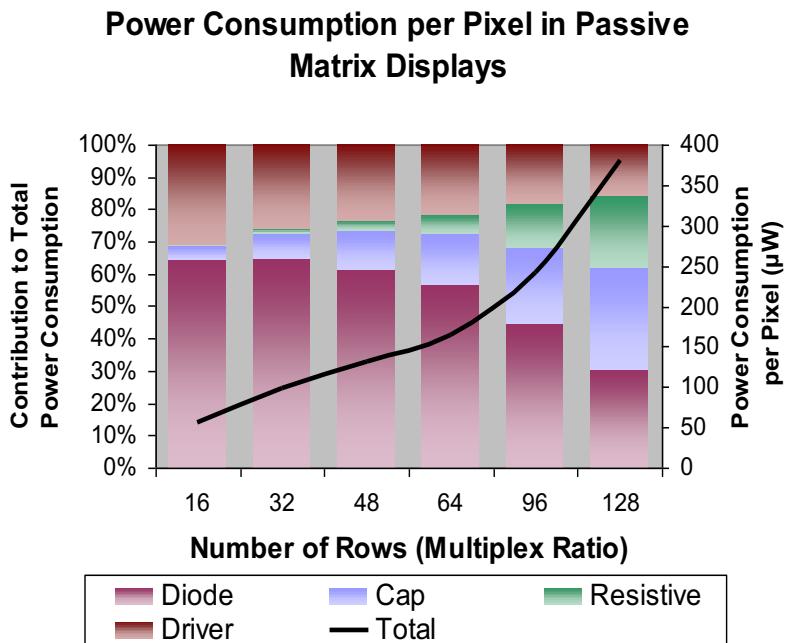
Passive Matrix Driving – Power Consumption

Four Factors Dominate

1. Driver compliance
2. Column capacitive charging
3. Resistive losses
4. Diode Power

Example

Clare Micronix presented, at OLED 2001 in San Diego, power consumption data for a 100 x 80 display panel driven with their MXED series of OLED/PLED passive matrix drivers.



Passive Matrix Drive Scheme

The simplest scheme to examine is the commonly used current driven Pulse Width Modulation (PWM)

- As the OLED is always driven with the same current density, linearity is good.
- The use of pre-charge can remove the charge-up time resulting in superb linearity.
- many discernable grey-scale levels can be achieved.
- Uniformity is also good as the use of current drive is insensitive to variations in threshold voltage.
- At the end of each line period, the charge is removed from the display, thus leading and trailing edges are not susceptible to the cross-talk that can occur.
- **HOWEVER**, the continual charge-up and discharge can result in a high power consumption.

Passive-Matrix enhancements

Skiping blank lines

- There are often blank rows on a screen, for example between lines of text.
- Skipping blank rows effectively reduces the multiplex ratio and therefore the power consumption per pixel.

A built-in reduced multiplex ‘screensaver’ or ‘standby’ mode

- Displaying, say, only the centre 16 rows, or a logo only 16 rows high scrolling over the screen.

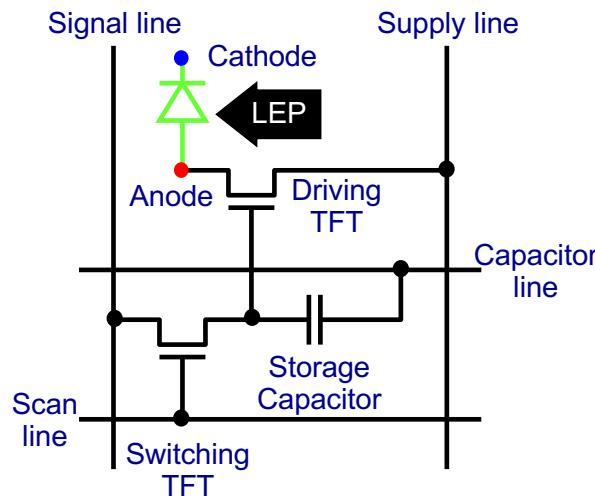
	Standard	Line skip
All on 96x64 monochrome		118mW
Screen of text	41mW	36mW
Screen-saver mode	12mW	5mW

Active Matrix Displays

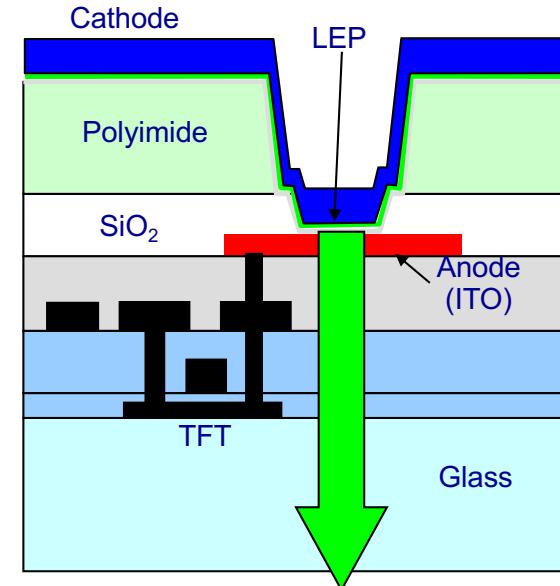
TFT (Thin Film Transistor) active matrix displays

- DC driven pixellated displays scalable up to large area
- Monochrome and full colour already demonstrated

PLED TFT Pixel Circuit



PLED TFT Cross-section



Active Matrix OLED

Active matrix driving of OLED displays allows

- Longer, less intense current pulse in the pixel

Leading to

- Ease of design of driver circuits
- Reduction in I^2R power dissipation
- Reduction in IR voltage drop
- Improvement in OLED efficiency / reduction in OLED power

Pixel circuits for LCD are designed to supply a voltage (analog or digital)

Pixel circuits for OLED are usually designed to supply a current

This involves either

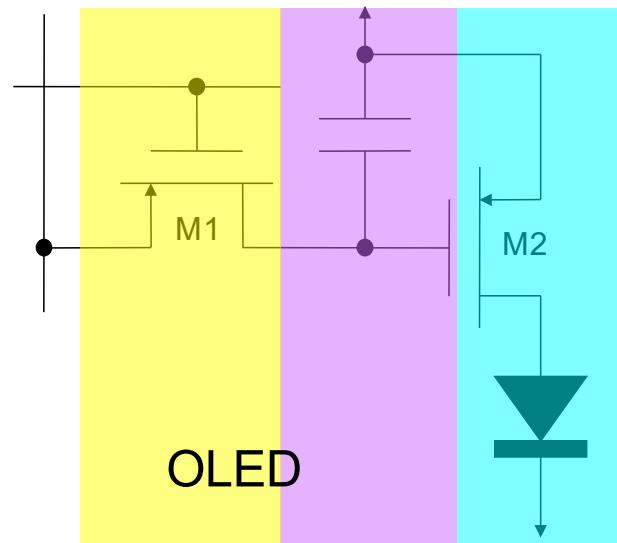
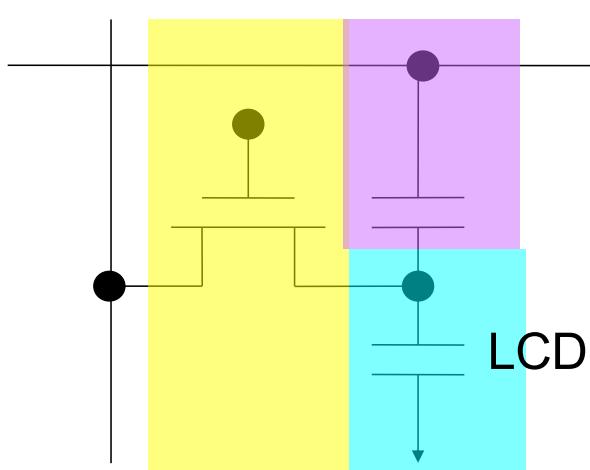
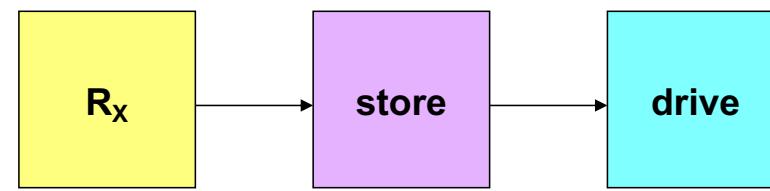
- Sending a voltage and converting it to a current
- Sending a current

These circuits are more complex and more prone to manufacturing variation

AM-OLED Backplane Technologies

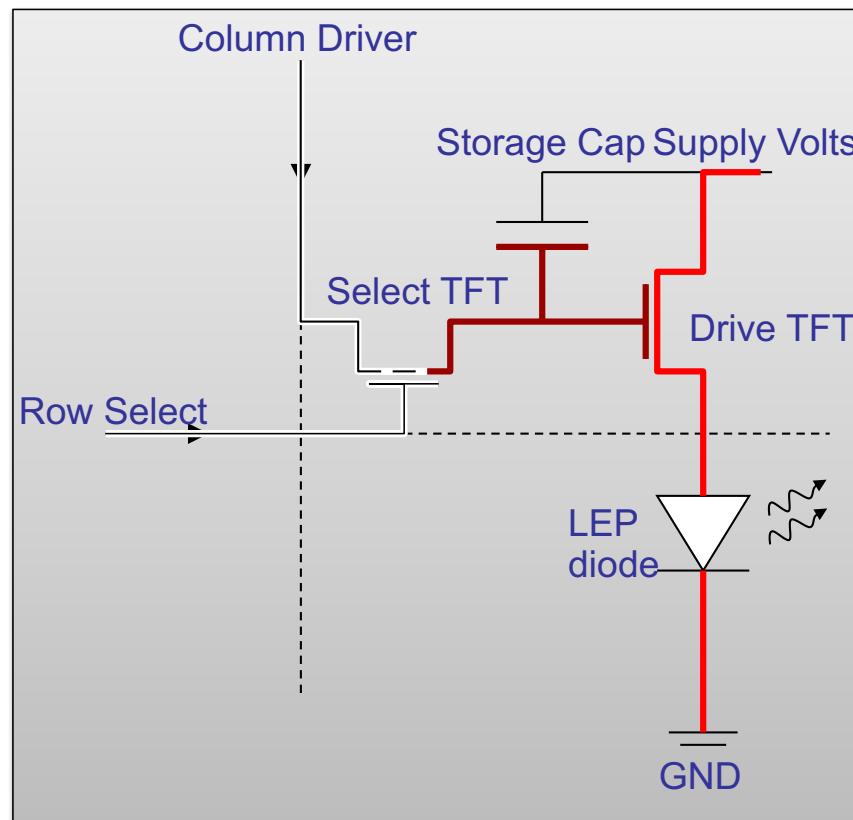
	LTPS	Oxide (IGZO)
Type	CMOS	NMOS
TFT structure	Coplanar	Inverted staggered w ES
Mobility (cm²/Vs)	50~100	10~30
Process	Laser	Sputtering
Uniformity	Issue	OK
Stability	Excellent	Issue
Environment sensitivity	Low	High
Off current	Low	Extremely low
Pixel circuit	>5 T, 1~2C	2T1C, 5T2C
Compensation	In-pixel	External
Manufacturability	Matured	Maturing
Run-to-run reproducibility	Excellent	Issue
Mask steps	8~11	4~5
Scaling up	Difficult	Good
Cost	High	Low

Simple Pixel Circuit



Voltage Control (Source Follower)

- Row is selected
- Driver TFT gate voltage set by column driver
- Row select is off, gate voltage held by capacitor until next frame
- Very simple (low TFT count)
- I_{DS} varies with V_G^2 (gamma 2 control by default)
- Sensitive to TFT variations (can be compensated) and LEP variations
- V_{DS} can be high (4-7V)



AMOLED limitations

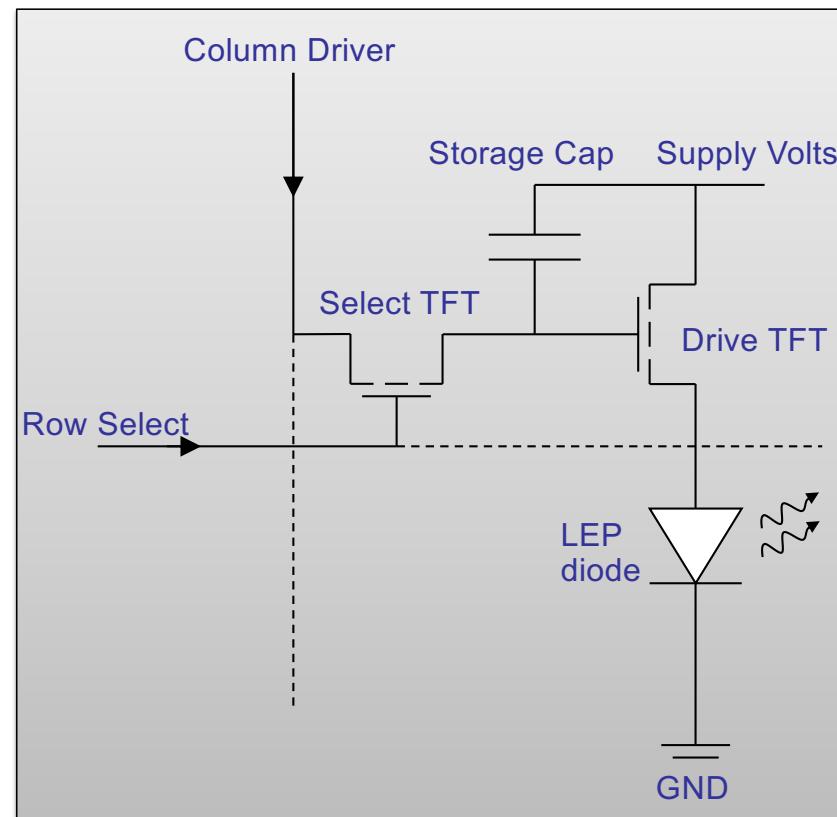
The limitations of simple AMOLED

No allowance for

- OLED process variation
 - Batch variability
- TFT process variation
 - Fixed pattern noise
- TFT aging & OLED luminance decay
 - Lifetime reduction
 - Image sticking
 - Differential decay of RGB

Pulse Coded Modulation (PCM) Voltage Drive

- Address period split into sub-frames
- Drive TFT acts as a switch
- OLED effectively voltage controlled
- Not sensitive to TFT properties
- V_{DS} low ($\sim 0.5V$) efficient operation
- Accelerated pixel aging – LEP V_t increases with time reduce operating current
- Very susceptible to burn-in and differential aging
- Image artifacts possibly introduced
- Higher data rates



Threshold Voltage Correction

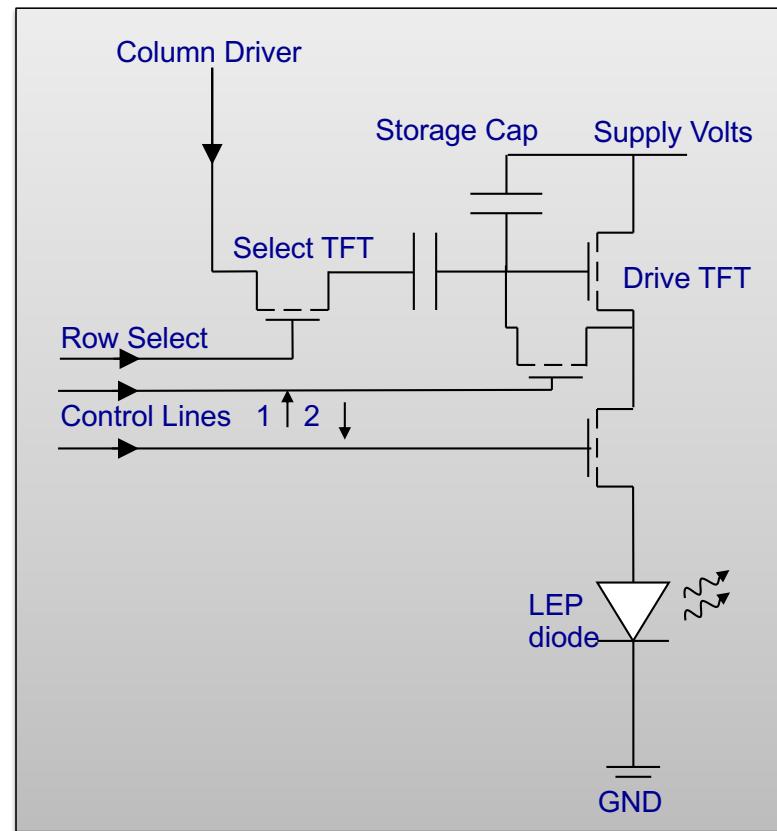
Selected with 0V data, C1 off, C2 on

C1 turned on, Discharging the gate voltage to threshold

C2 turned off then C1, holding the threshold at the gate

Any voltage applied by the column driver is now offset by the threshold voltage

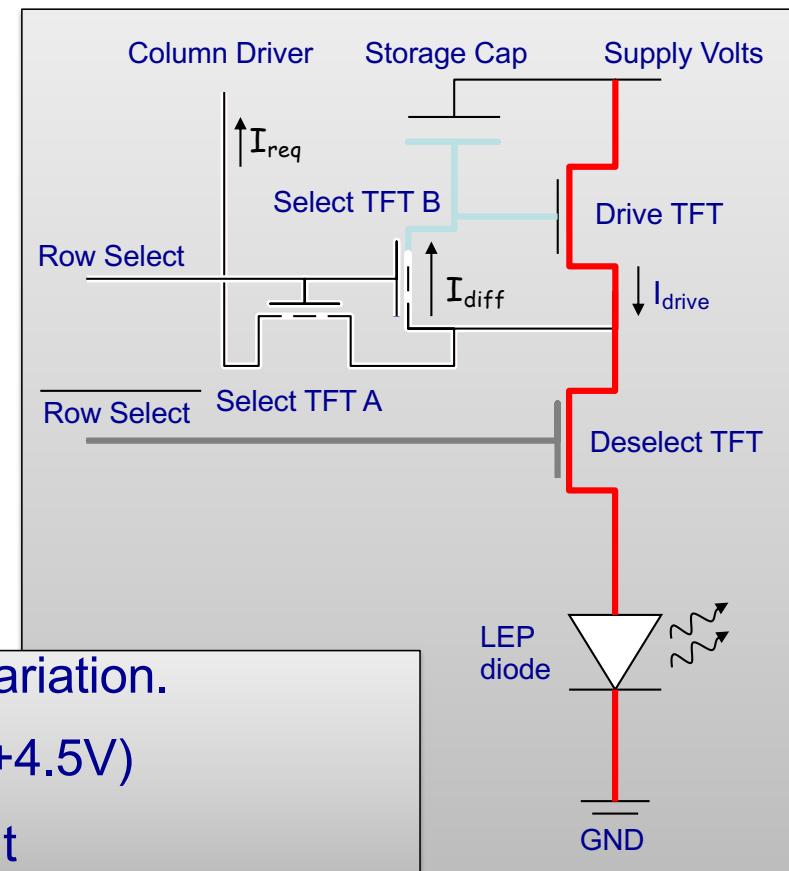
- 2 large TFTs
- V_{DS} high ($4V+0.5V$)



Current Control (Sarnoff method)

- Row is selected, diverting the drive current into the column driver
- Required drive current is sunk by the column driver.
- Any difference in the currents flows into the capacitor, modifying the drive voltage until the current is correct
- Row is deselected, redirecting the drive current through the LEP diode

- Linear current drive, insensitive to TFT variation.
- Complex, high TFT count, large V_{DS} (4V+4.5V)
- 3 of the TFTs must cope with max current



Amplifying Current Mirror

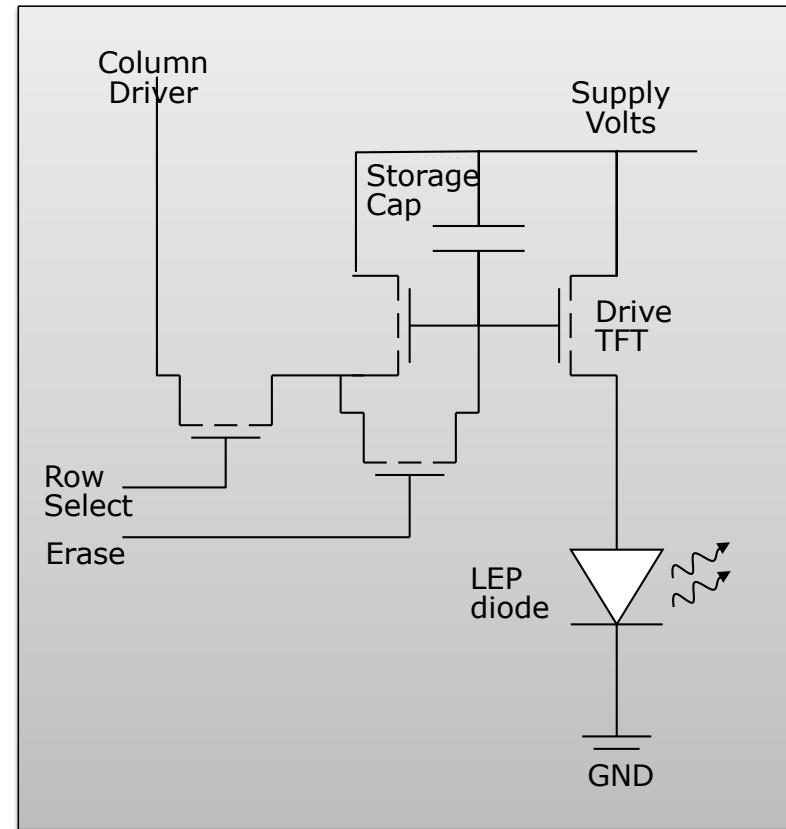
In use primarily by Sony

A similar feedback mechanism (to the Sarnoff circuit) sets the current on a 'mirror' TFT

The mirror TFT is geometrically scaled by a known factor (k) to the drive TFT

The drive TFT will exactly pass k times the mirror TFT current for a given gate voltage

- Three small TFTs and low currents on the column line
- Very linear and demonstrated on 13" diagonal display
- V_{DS} still $\sim 4V$



Charge programmed optical feedback

Very simple circuit

A charge is put on the capacitor

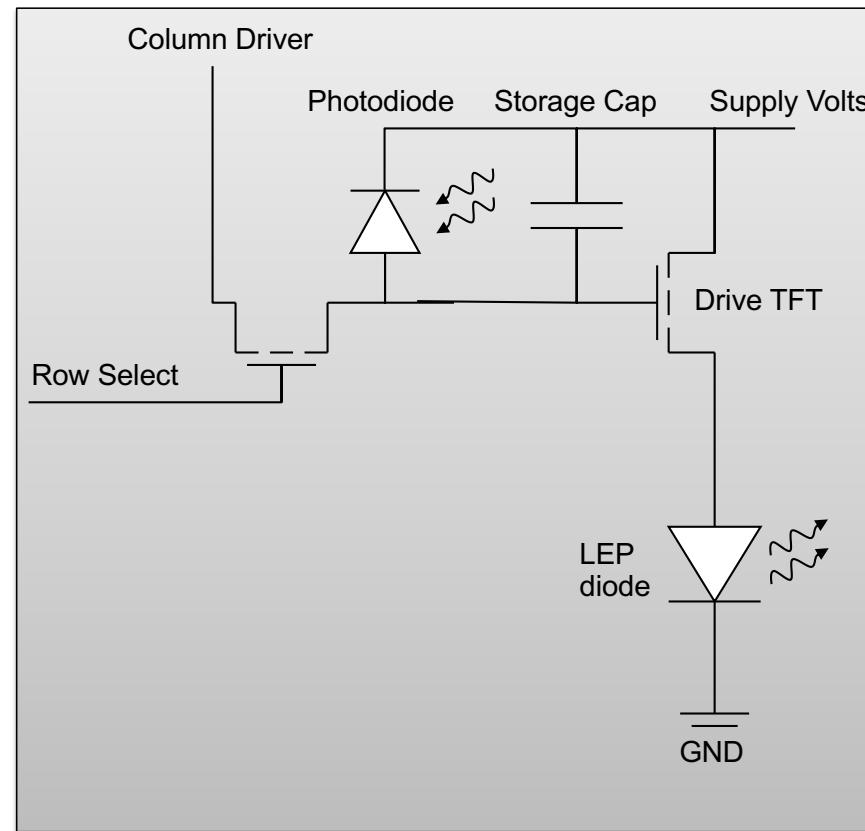
The photodiode will discharge the capacitor until the gate voltage drops sufficiently to turn off the OLED

The light output should be proportional to the charge

Sensitive to ambient light.

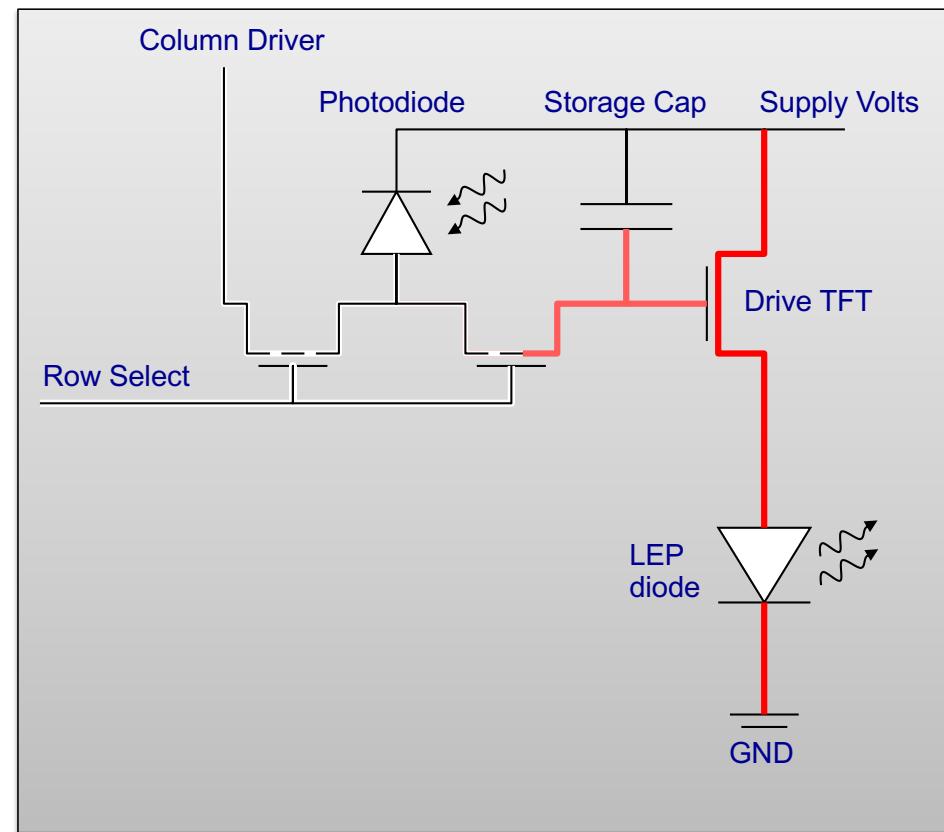
OLED is pulsed – less efficient

Long tail of pulse can cause nonlinearities

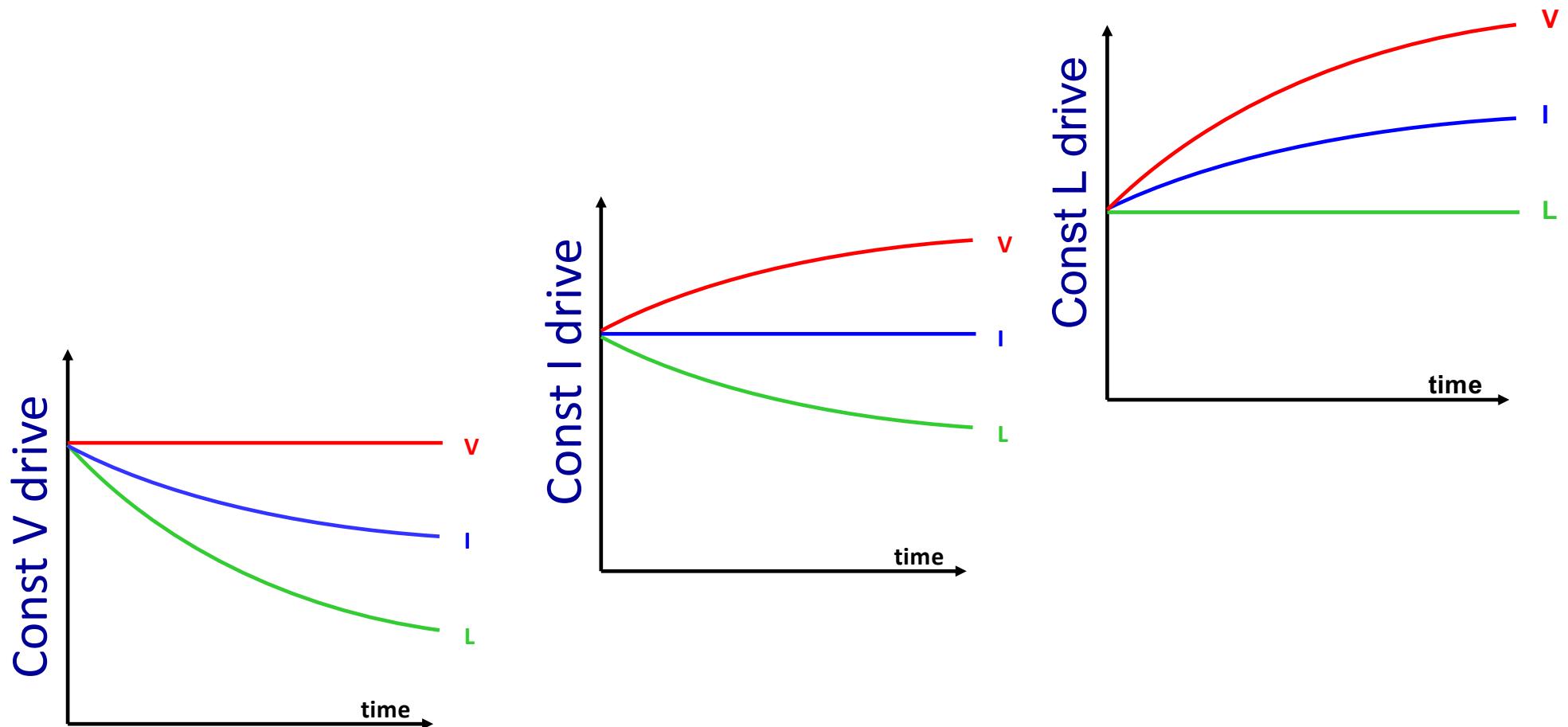


Current programmed optical feedback

- Row is selected
- Column driver requests photocurrent
- Current difference flows into the capacitor
- Row is deselected, holding the drive level on the storage cap
- Developed by CDT
- Medium TFT count, only one TFT needs to handle max current
- Insensitive to TFT and LEP variation, depends only on photodiode sensitivity – highly linear
- Automatically compensates for non-uniformities and aging



Summary of OLED Drive schemes



OLED Drive Circuit and Process Variability

CAUSE AND EFFECT	Effect of TFT Process variation	Effect of OLED process variation	Reduced lifetime due to resistive effects	Reduced lifetime due to reduced conversion efficiency
Voltage program Voltage drive	V small	Medium	Medium	Medium
Voltage program Current drive	Medium	Small	Very Small	Medium
Voltage program VT compensated current drive	Small	Small	Very Small	Medium
Current programmed current drive	Small	Small	Very Small	Medium
Optical feedback	Medium	Small	Very small	Very small