Designing with the IP Integrator Demo Script

Introduction

This demonstration introduces the IP integrator (IPI) feature available in the Vivado® Design Suite.

Preparation:

- Required files: `$TRAINING_PATH/IP_Integrator/demo/KCU105/verilog`
- Required hardware: None

Designing with the IP Integrator

Action with Description	Point of Emphasis and Key Takeaway
• Launch Vivado Design Suite 2021.2.	
• Click the **Create Project** link in the Quick Start section of the Getting Started page.	• The New Project link in the Getting Started page allows you to create a new Vivado Design Suite project.

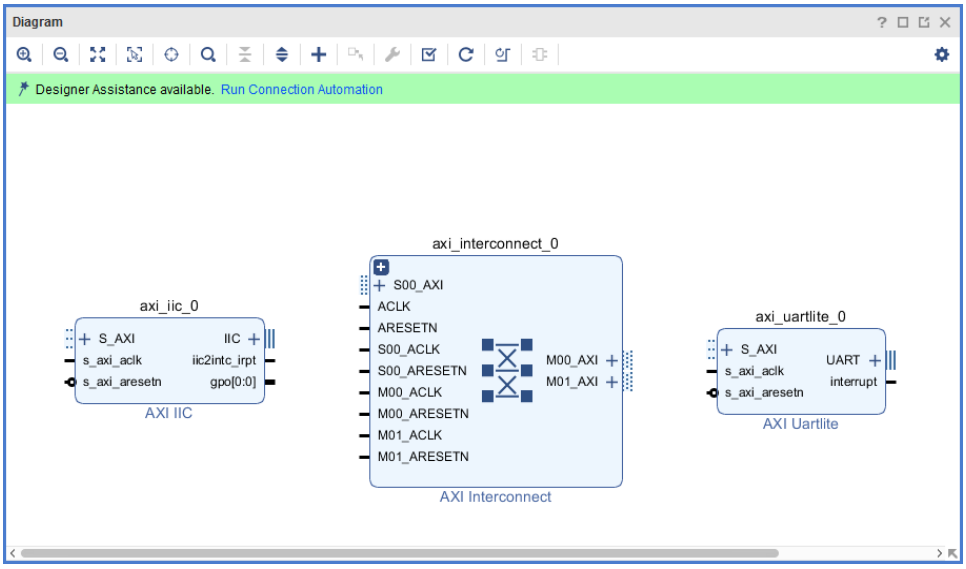
• Create a new project using the New Project Wizard with the following details:
  • Project name: *project_IPI*
  • Project location: `$TRAINING_PATH/IP_Integrator/demo/KCU105/verilog`
  • Select **Do not specify the sources at this time**.
  • Select the **KCU105** Board.
	• By default, the Vivado IDE creates the project name as *project_1*.

• Click **Create Block Design** under IP Integrator in the Flow Navigator.	• The IP integrator allows you to:
	  • Create a new block design
	  • Open an existing block design
	  • Generate the block design

Action with Description	Point of Emphasis and Key Takeaway

• Enter **subsystem_1** as the design name in the Create Block Design dialog box.	• The canvas provides options to:
	  • Add IPs (**Add IP**) into the subsystem
	  • Validate the subsystem (**Validate Design**)

• Click the **Add IP** link in the canvas. • Alternatively, you can click the **Add IP** icon (+) from the horizontal toolbar.	• This opens the IP repository of Xilinx and third-party IPs. • IPs can be searched by name via the Search field.
• Enter **AXI Interconnect** in the Search field. • Select the **AXI Interconnect** IP from the results. Double-click the IP.	• This adds the AXI Interconnect IP into the subsystem.
• Similarly, add the **AXI Uartlite** IP to the block design in the same way.	• Adding the AXI uartlite IP into the subsystem.
• Add the **AXI IIC** IP to the block design.	• Adding the AXI IIC IP into the subsystem. • IP have been added to IP integrator canvas. Now, it is time to connect IP together to create a subsystem.

Action with Description	Point of Emphasis and Key Takeaway
	
• Select the **S00_AXI** interface in the AXI Interconnect IP. • Right-click and select **Create Interface Port**. • Click **OK** in the dialog box to make the S00_AXI interface as an interface port.	• This is used to create ports on the interfaces, which are groupings of signals that share a common function. • For example, S_AXI is an interface port on several Xilinx IP. The command gives more control in terms of specifying the interface type and the mode (master/slave). • You specify the interface name, the vendor, library, name, and version (VLNV), as well as the mode (MASTER or SLAVE or MONITOR) in this dialog box.

Action with Description	Point of Emphasis and Key Takeaway
• Select the **ACLK** port in the AXI Interconnect IP. • Right-click and select **Create Port**. • Enter **100** in the Frequency (MHz) field of the dialog box. • Click **OK** in the dialog box to make ACLK as a top-level port.	• Create Port gives you more control in terms of specifying the input/output and the bit width and the type (clk, reset, data). • In the case of a clock, you can even specify the input frequency.
• Select the **ARESETN** port in the AXI Interconnect IP. • Right-click and select **Create Port**. • Click **OK** in the dialog box to make ARESETN as a top-level port.	• You can change the polarity of the reset in the Customize Port dialog box.
• Double-click the **ARESETN** port to open the Customize Port dialog box. • Select the **ACTIVE LOW** option and click **OK**.	

• Place the cursor on the S00_ACLK port of the AXI Interconnect block.	• Making connections in IP integrator is simple.
	  • As you move the cursor near an interface or pin connector on an IP block, the cursor changes into a pencil.
	  • You can then click an interface or pin connector on an IP block, hold down the left mouse button, and then draw the connection to the destination block.

Action with Description	Point of Emphasis and Key Takeaway

• Click-and-drag the cursor from S00_ACLK to ACLK.
• Make the following connections in the same way:
  • M00_ACLK → ACLK
  • M01_ACLK → ACLK
	• As you drag the connection wire, a green check appears on the ACLK port, indicating that a valid connection can be made between these ports.
	• The Vivado IP integrator highlights all possible connection point in the subsystem.

• Click-and-drag the cursor from S00_ARESETN to ARESETN.
• Make the following connections in the same way:
  • M00_ARESETN → ARESETN
  • M01_ARESETN → ARESETN
	• The pencil symbol makes it easy for making connections.

• Make the following connections between the AXI uartlite IP and AXI Interconnect IP:
  • S_AXI → M00_AXI
  • s_axi_aclk → ACLK
  • s_axi_aresetn → ARESETN	

• Make the following connections between the AXI IIC IP and AXI Interconnect IP:
  • S_AXI → M01_AXI
  • s_axi_aclk → ACLK
  • s_axi_aresetn → ARESETN	

Action with Description	Point of Emphasis and Key Takeaway
• Click the **Run Connection Automation** link in the banner at the top of the design canvas. • Select **/axi_iic_0/IIC** and click **OK**.	• Run Connection Automation provides assistance in hooking interfaces and/or ports to external I/O ports. • This makes the iic port of the AXI IIC IP as an external port.
• Click the **Run Connection Automation** link again. • Select **axi_uartlite_0/UART** and click **OK**.	• This makes the UART port of the AXI uartlite IP as an external port.
• Click the **Validate Design** icon (☑) in the Diagram tab to validate the block design. • Clock **OK** after validation is successful.	• The Vivado IP integrator runs basic design rule checks in real time as the design is being put together. • Validate Design runs a comprehensive design check on the design.
• Select the **subsystem_1** block design in the Hierarchy tab of the Sources window. • Right-click and select **Generate Output Products**. • Click **Generate** in the dialog box to generate the output products for the subsystem. • Click **OK** after the successful generation of the output products.	• Once the block diagram is complete and the design is validated, there are two more steps required to complete the design. • First, the output products must be generated. • This is when the source files and the appropriate constraints for all the IP will be generated and made available in the Vivado IDE Sources pane. Depending upon the target language selected during project creation, appropriate files will be generated.

Action with Description	Point of Emphasis and Key Takeaway
• Select **Verilog** as the Target language from the Settings. • Right-click **subsystem_1** in the Hierarchy tab of the Sources window and select **Create HDL Wrapper**. • Click **OK** in the Create HDL Wrapper dialog box.	• An IP integrator block diagram can be integrated into a higher-level design or it can be the highest level in the design hierarchy. • To integrate the IP integrator design into a higher-level design, simply instantiate the design in the top-level HDL file.
• Select **File** > **Save Block Design** to save the block design.	
• Enter `write_bd_tcl $::env(TRAINING_PATH)/IP_Integrator/demo/KCU105/verilog/IPI.tcl` in the Tcl Console to generate the Tcl script.	• The Tcl script enables designers to re-create entire block design just by running this Tcl script.
• Run implementation to implement the IPI subsystem.	
• Click **Cancel** in the Open Implemented Design dialog box.	
• Select **File** > **Exit**.	• This option closes the Vivado Design Suite.

Summary

In this demonstration, you walked through creating a simple Vivado IP integrator subsystem design by integrating some common peripherals and cores and connecting them via an AXI Interconnect block. You then created the top-level HDL wrapper for the completed subsystem design, which is later implemented in the Vivado Design Suite.

References:

- Supporting materials
  - *Vivado Design Suite User Guide: Designing IP Subsystems Using IP Integrator* (UG994)