6th International Conference on
I-SMAC (IoT in Social, Mobile, Analytics and Cloud)
I-SMAC 2022

A REVIEW ON STATISTICAL POWER MODELLING FOR A GRAPHICS PROCESSING UNIT (GPU)

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Table of Contents

- INTROCUCTION
- GPU BASICS
- SILICON POWER
- RESULTS
- REFERENCES

INTRODUCTION

Scaling Architectures

- GPU computing is defining a new Supercharged Law, specifically due to the huge parallelism in its computing architecture.

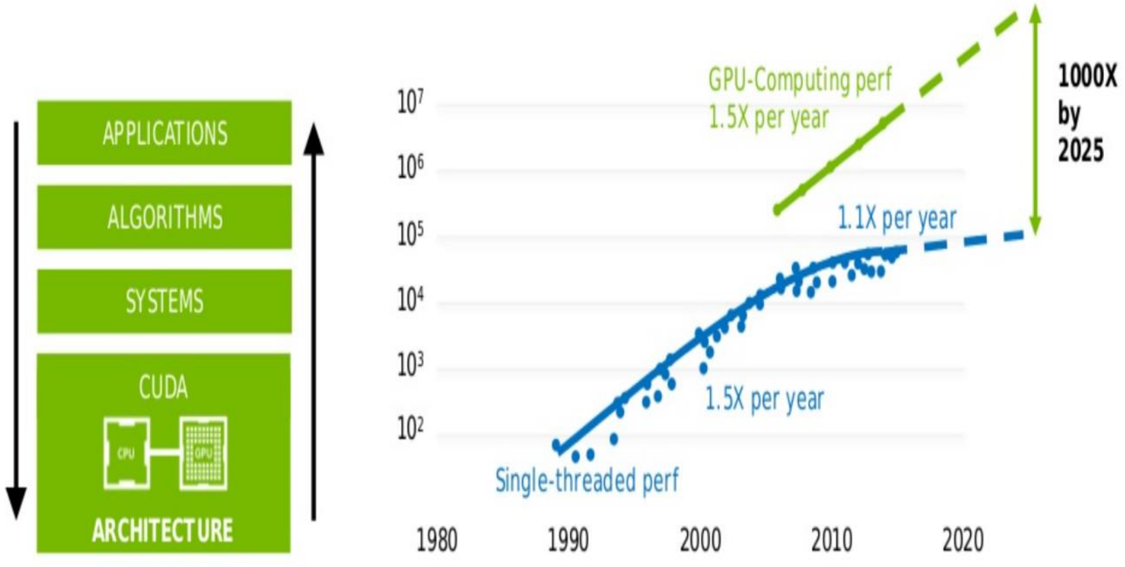


Figure 1.1: GPU Parallelism Compute Perf [7]

Shifting Trends towards GPU

- The Graphics Processing Unit (GPU) or the Virtual Processing Unit (VPU) as shown in Figure 1.2 is a specialized electronic circuit designed to rapidly manipulate or alter memory to accelerate heavy workloads in shorter intervals of time as compared to a CPU.

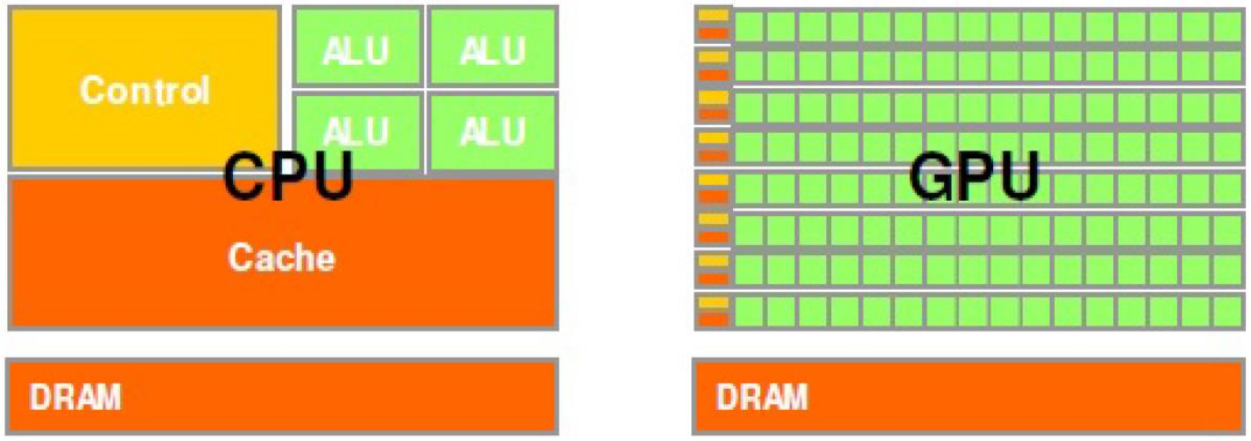
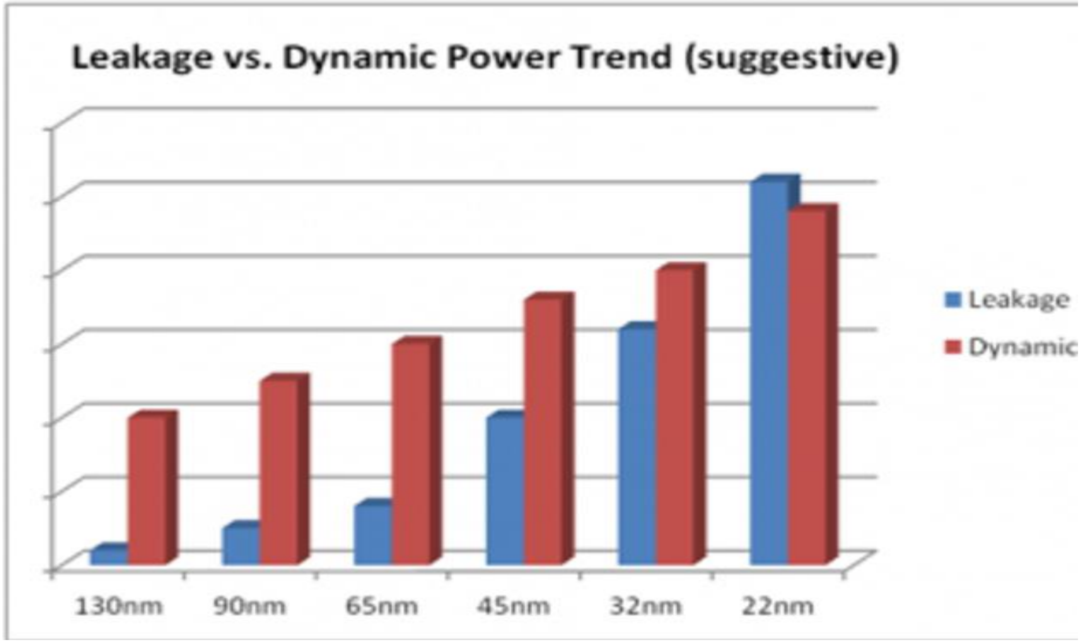


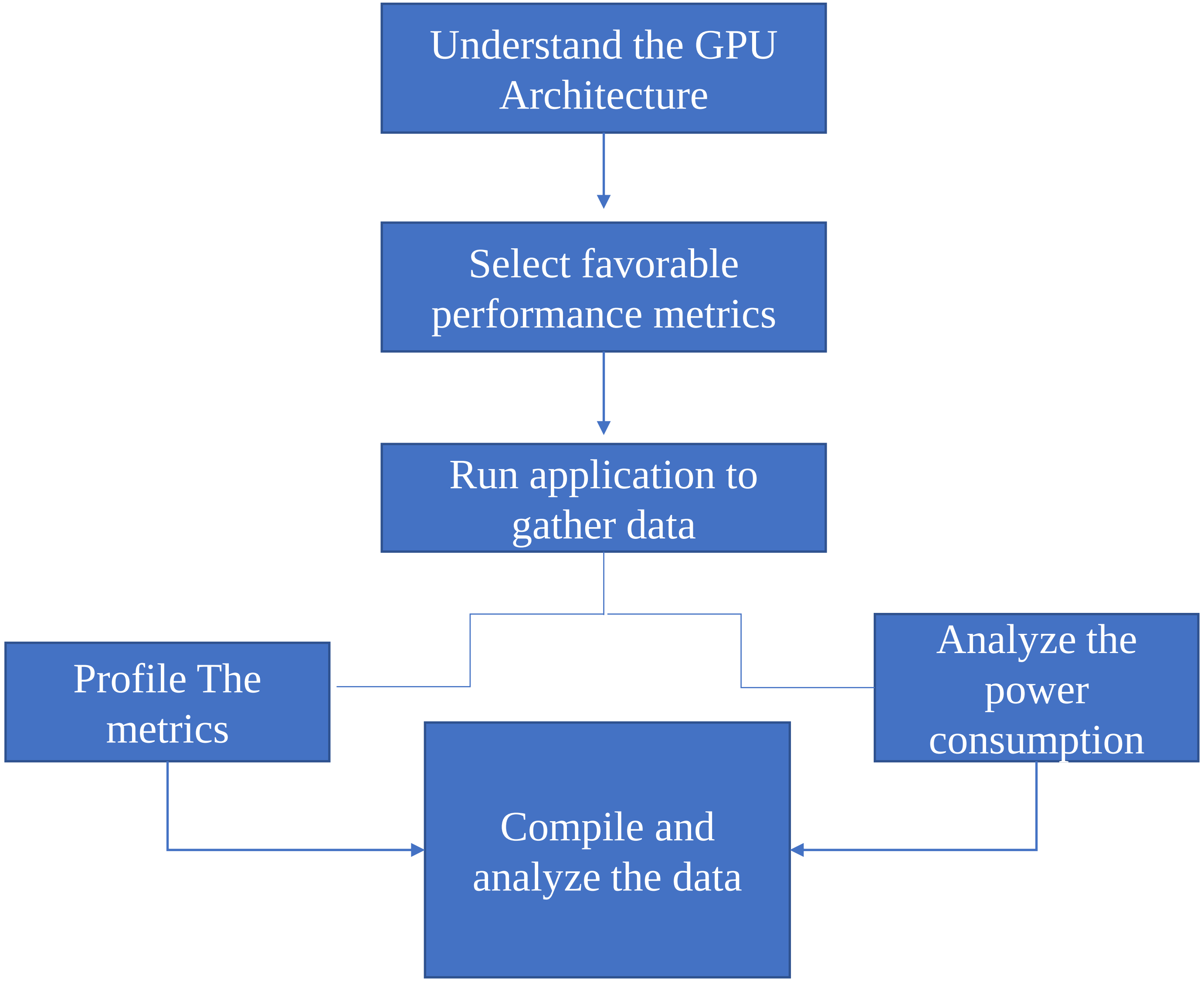
Figure 1.2: Parallelism between CPU and GPU architectures. [2]

Motivation

- Designing for low power as architectures scaled down in technology became essential as number of transistors on a dye kept on increasing to accommodate more cores.
- It is hence becoming increasingly difficult for speed to keep par with increasing number of transistors.



Working Methodology



Understand the GPU Architecture

Select favorable performance metrics

Run application to gather data

Profile The metrics

Analyze the power consumption

Compile and analyze the data

GPU BASICS

Parallelism in CPU’s

- The five essential steps required for an instruction to execute in a CPU RISC Architecture are:
  - Instruction Fetch (IF)
  - Instruction Decode (ID)
  - Instruction Execute (Ex)
  - Memory Access (Mem)
  - Register Write-Back (WB)

Pipelining

- Pipelining is a technique of executing multiple instructions in parallel per clock. Instruction Level Parallelism can fix the inefficiencies brought about by sequential execution like latency, resource utilization.

Instruction No	**Pipeline Stage**						
1	IF	ID	Ex	Mem	WB		
2		IF	ID	Ex	Mem	WB	
3			IF	ID	Ex	Mem	WB
4				IF	ID	Ex	Mem
5					IF	ID	Ex
Clock Cycle	**1**	**2**	**3**	**4**	**5**	**6**	**7**

GPU Design

- A GPU comprises of a large number of cores (significantly greater than a CPU) each of which run at a clock speed significantly slower than a core of a CPU.

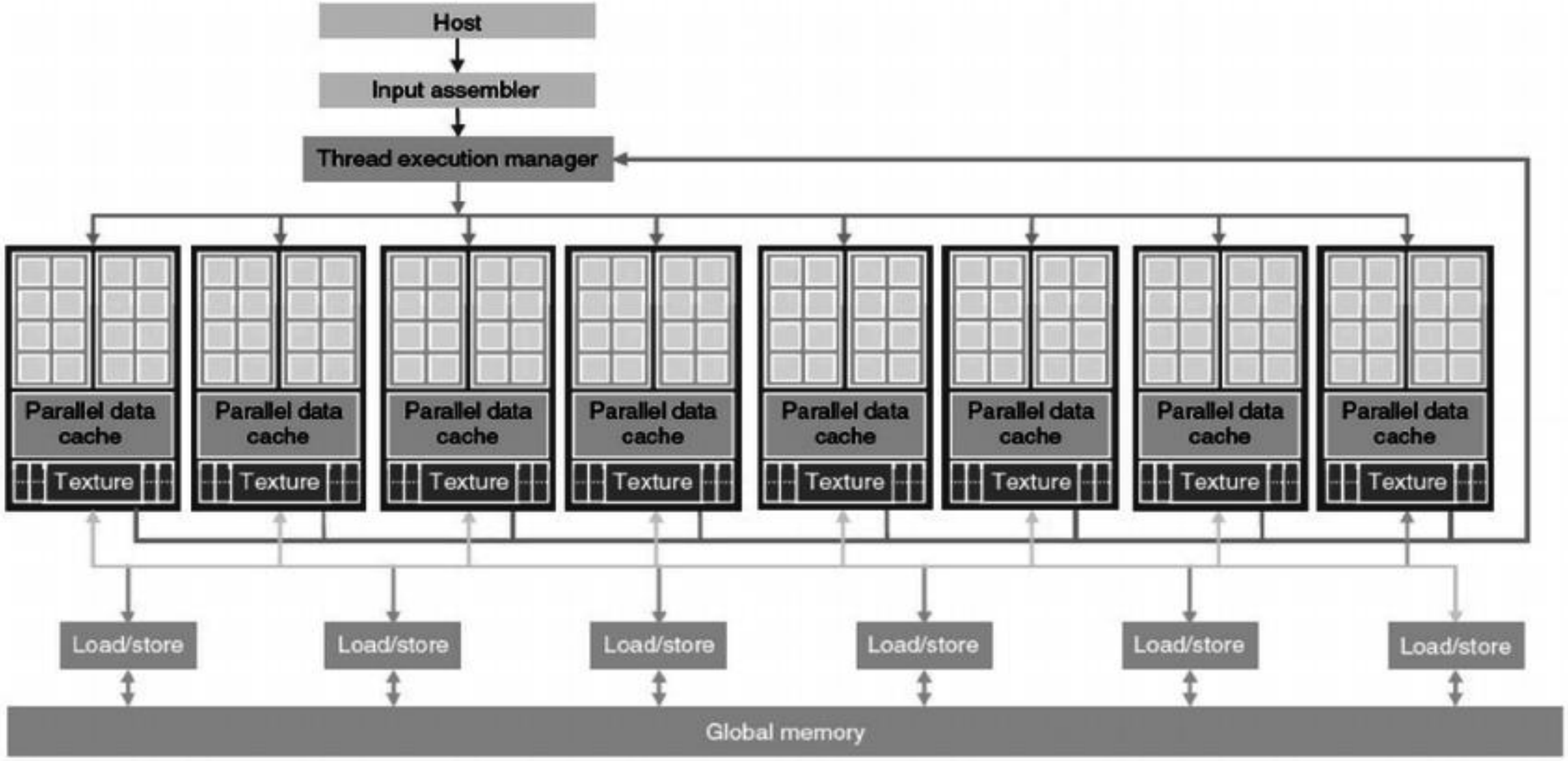
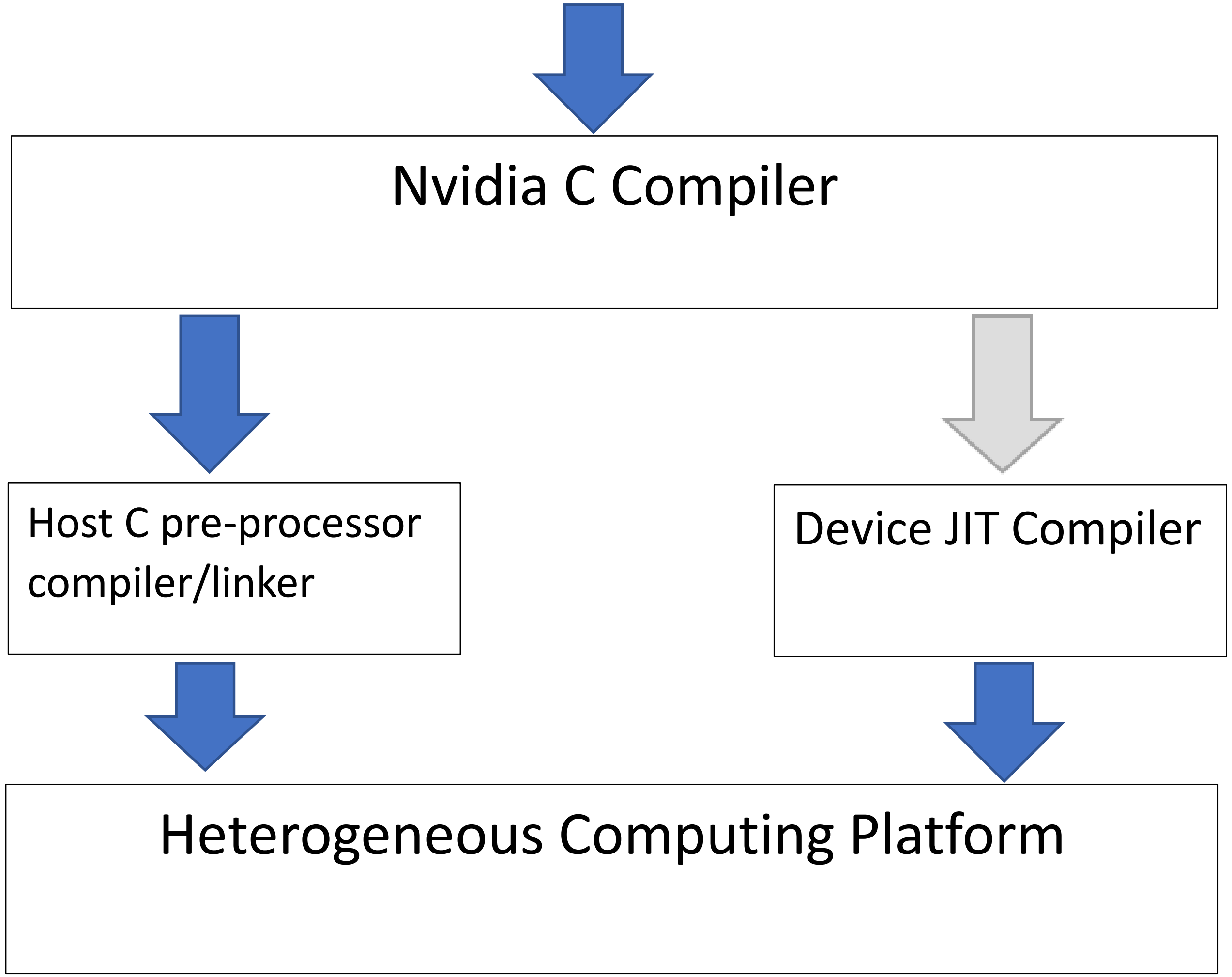


Figure 1.3 : GPU Architecture

GPU Execution

- A typical CUDA program has code intended for both the CPU and the GPU
- The NVCC or Nvidia C Compiler splits the Data intensive code from the program.
- The Host machine processes the less intensive code.
- The Device processes the more intensive code.
- Together it forms a heterogeneous computing platform.


Nvidia C Compiler

Host C pre-processor compiler/linker

Device JIT Compiler

Heterogeneous Computing Platform

CUDA Memories

- Following are the supported memory types on a CUDA supported GPU
  - R/W per-thread registers
  - R/W per-thread local memory
  - R/W per-block shared memory
  - R/W per-grid global memory
  - Read only per-grid constant memory.

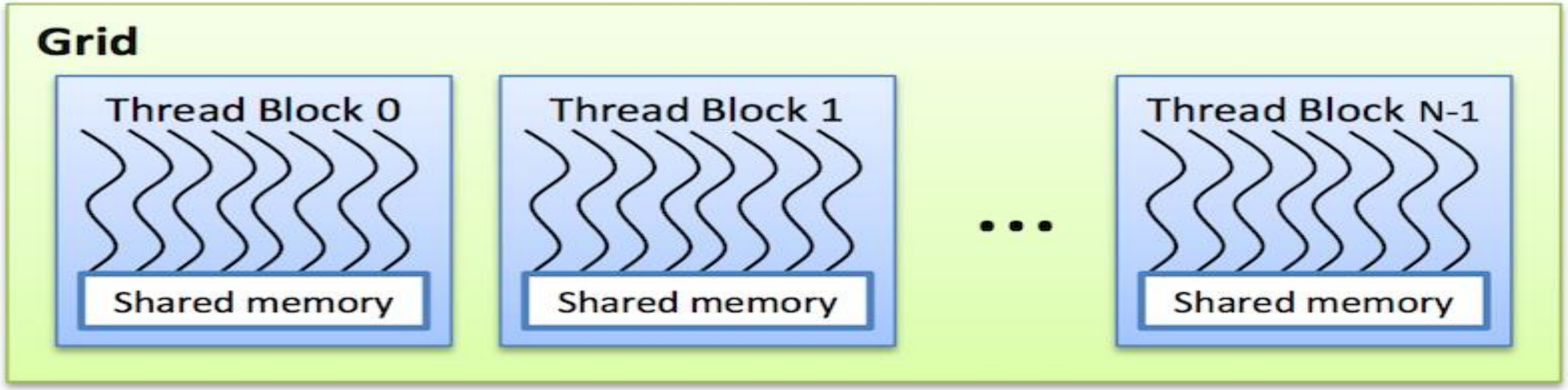


Figure 1.4: Thread Level Hierarchy

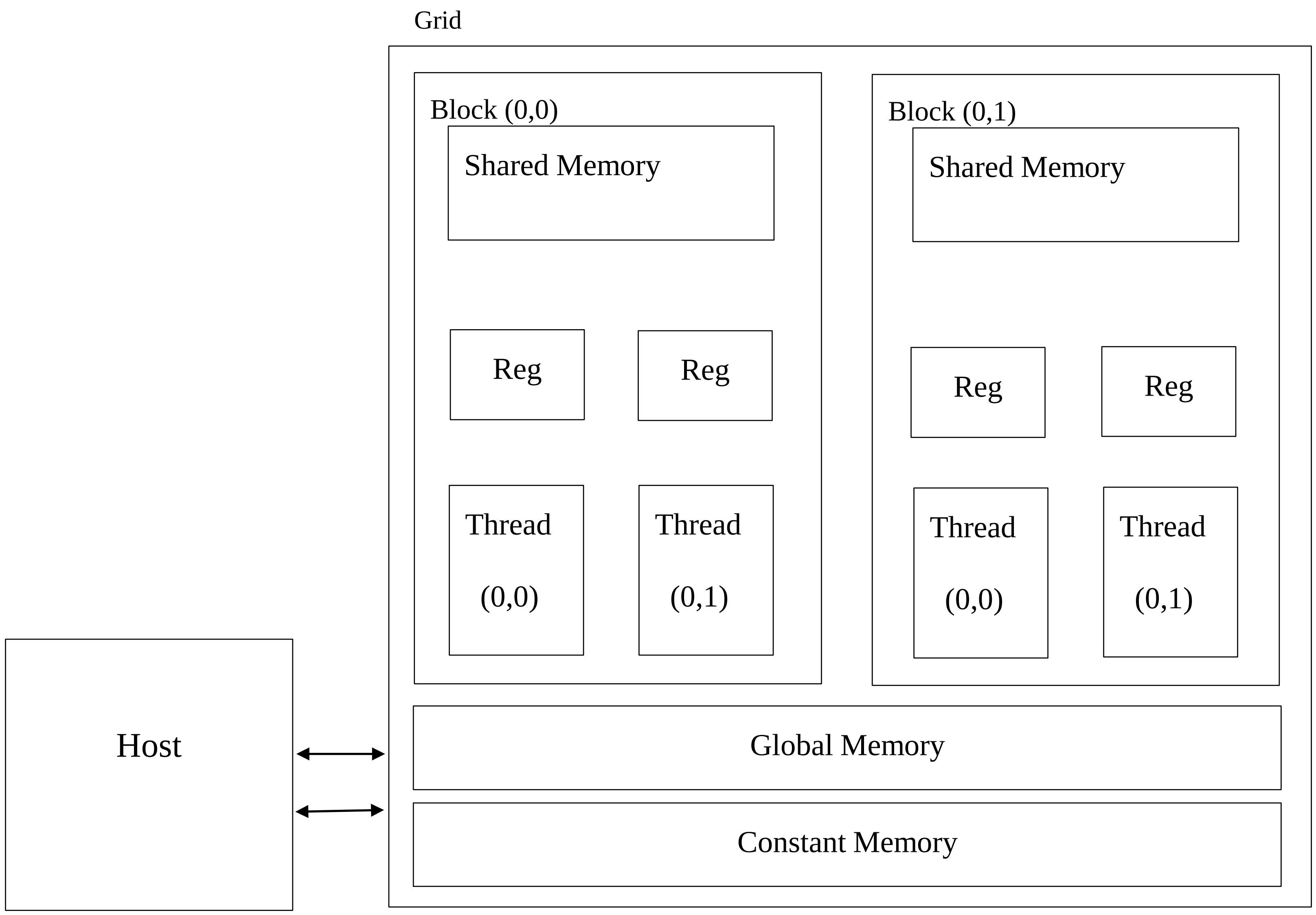


Figure 1.5: Memory Assignment

SILICON POWER

Dynamic Power

- Consists of the power consumed during logic transitions and can be sub-divided into two types, Switching and Internal Power.
  - Switching Power: As the name suggests, this power manifests itself when there are transitions between logics.

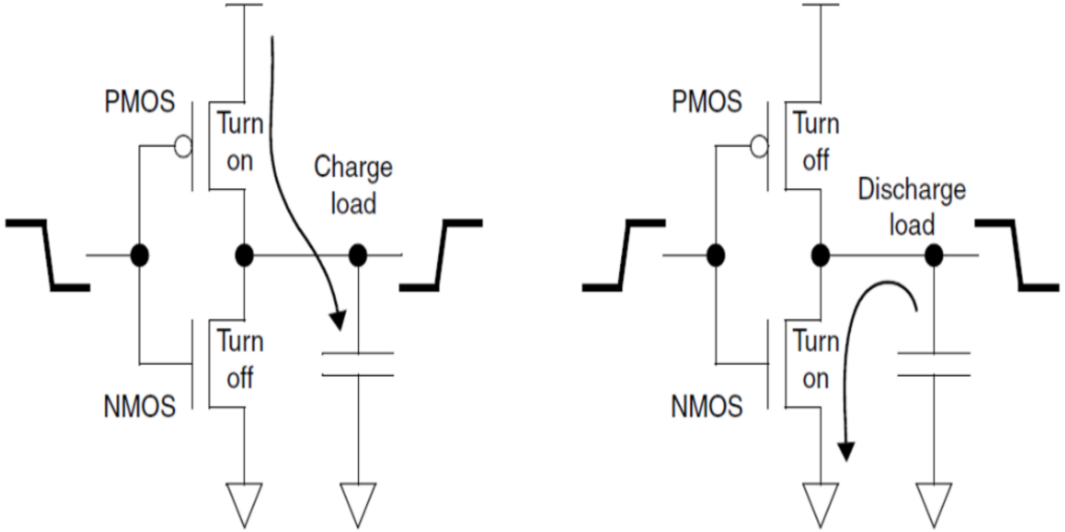


Figure 1.6: Logic transitions in an inverter

- Internal Power: When the input signal is at an intermediate voltage level, a relatively large amount of current flows through the transistors for a brief period of time as shown in Figure 1.7 contributing to internal power.

$$P_{dyn} = \left(C_{eff}.V_{dd}{}^{2}.f_{clk}\right) + (t_{sc}.V_{dd}.I_{peak}.f_{clk}) \qquad (1.1)$$

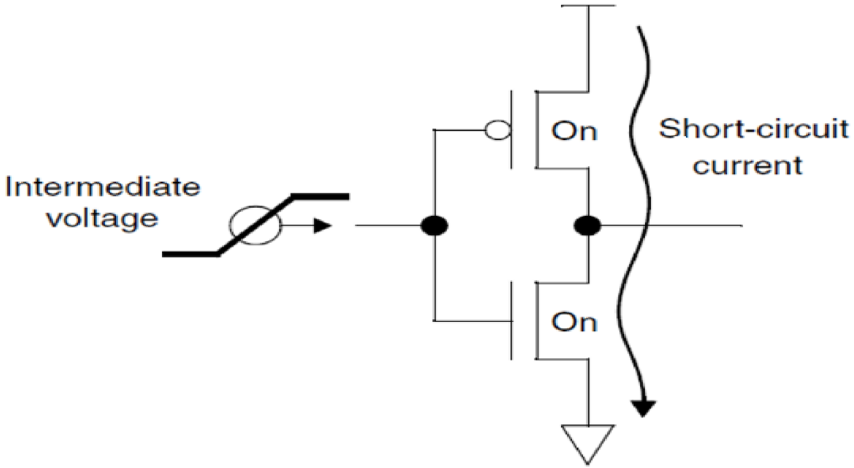


Figure 1.7: Short Circuit Current

Static (Leakage) Power

- Static power is the transistor leakage current whenever power is applied to the device. The main causes of leakage power as displayed in Figure 1.8 are
  - Reverse bias p-n junction diode leakage: Caused by minority carrier drift
  - Sub threshold leakage: Current which flows from drain to source when transistor operates in weak inversion region. Sub threshold leakage is the biggest contributor of leakage power.
  - Gate leakage: Current which flows directly from the gate to the substrate either through hot carrier injection or oxide tunneling.

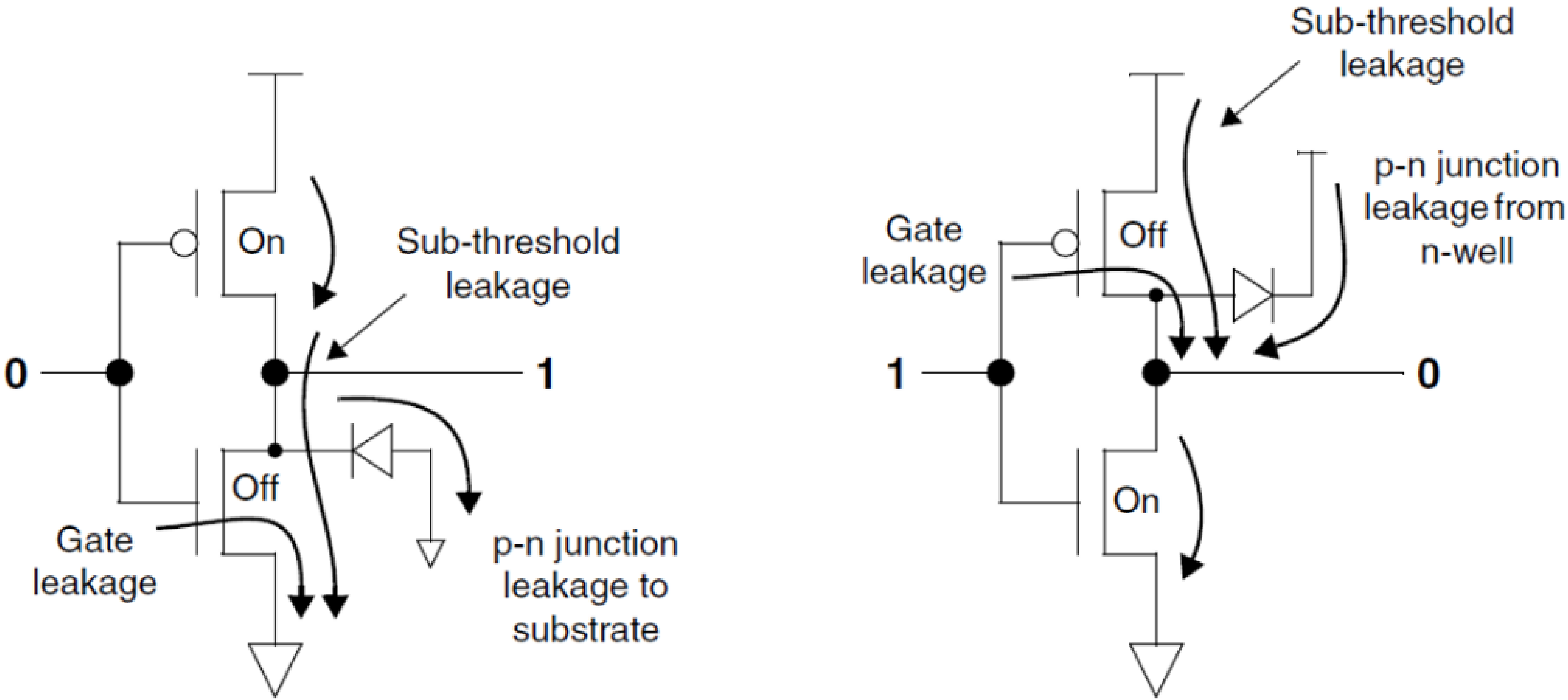


Figure 1.8: Static (Leakage) Power causes

RESULTS

Captured Data

- **Compute Metrics:** Metrics represent the counters that can be involved in a computation.
  - Number of additions.
  - Number of bytes transferred from the memory.
  - Number of instructions executed.
- **Power:** Core Voltage, Core Current, Memory Voltage, Memory Current.

Feature Selection

- Features represent the various groups of obtained data under the captured metrics.
- Reducing the feature count to minimize the complexity of the data, helps in efficient modelling.
- This can be achieved using largely available Machine Learning algorithms like PCA (or Principal Component Analysis) which helps eliminate the features from a set which do not contribute to large changes in the Target Variable (here, power) , i.e., feature prioritization.

Correlations in Data

- Multiple data points can be scaled versions of a data point.
- Such data points make data model complex and their removal will not affect the model in any way.

- Techniques to remove correlations:
  - Clustering.
  - Cosine Similarity.

Power Modelling

- Implemented Steps
  - Minimum number of features obtained.
  - Redundant data, representing similar data points removed.

1. **Total Power from running workload:** This is the power obtained from the GPU with operating workload.
2. **Computed Power from Statistical Models:** This is the computed power after Feature Selection and removing Correlations in data.
3. **Accuracy of Prediction**

- Implement Statistical Power model for energy consumed and obtain the convergence error.
  - $Error = Total\ Energy - Computed\ Energy$

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