

Yojan Chitkara

📍 Rajeshwari Homes Apartment , RR Nagar | Bangalore , Karnataka | India

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Education

- 2015-2019 **BACHELOR OF ENGINEERING** *R.V College Of Engineering (IND)*
Bachelors in Electronics and Telecommunication Engineering
GPA : 9.26 (out of 10.0)
- 2014-2015 **12TH GRADE** *National Hill View Public School (IND)*
Physics , Chemistry , Mathematics , Computer Science
Overall Percentage : 94.2
- 2013-2014 **11TH GRADE** *National Hill View Public School (IND)*
Physics, Chemistry, Mathematics , Computer Science
Overall Percentage : 90
- 2012-2013 **10TH GRADE** *National Hill View Public School (IND)*
Physics , Chemistry , Biology , Mathematics , History , Geography , Political Science
Overall GPA : 10.0 (Out of 10.0)

Courses taken apart from Majors

- 2016 **CERTIFIED PREDICTIVE ANALYTICS COURSE** *R.V College of Engineering (Autonomous) Bangalore*
Overall Grade : O (Outstanding)
- 2018 **CERTIFIED CRYPTOGRAPHY AND NETWORK SECURITY** *(Coursera an Online Platform) Stanford University* . Overall Grade : O (Outstanding)

Industry Experience

- December 2019 - Current **INTEL CORPORATION**
FPGA Hardware Engineer
1.) Coherent Architecture Validation on Intel Servers and CPUs. (Compute Express Link and Ultra-Path Interconnect)
2.) Bus Functional Modelling (Transaction Layer Verification Model) of Coherency Protocol in a Heterogeneous Computing Environment and triage performance issues in RTL.
3.) Performance Validation of CXL.cache and CXL.mem protocol on Intel Servers, using internally developed tools to characterise Bandwidth and Latency.
- January-July 2019 **NVIDIA GRAPHICS PVT LTD**
ASIC System Design Intern
1.) Performance Analysis for compute workloads on a GPU.
2.) GPU Architecture (Power aware design) and Statistical Power Modelling using Machine Learning.
3.) Post Silicon Power Estimation and Power Analysis for compute workloads on a GPU.
4.) GPU Validation set up, reading PCB specifications and profiling GPU's to estimate for power and performance using Digital Aquisition Units (DAQ) and Digital Multimeters (DMM).
- May-July 2017 **CENTER FOR DEVELOPMENT OF TELEMATICS**
Mobile Application Developer for the Public Data Office App using Android Studio Software.
1.) Working with handling Front end and Back end development of PDO using a Mobile Application created on Android Studio which provides Wi-Fi portability to small scale industries and the rural population.
2.) Controlling requests using a back end of PHP and MYSQL linked to Android Studio using the JSON frame/packet structure, monitored using wireshark.

Publications and Patents

- 2018-19 **INSPECTION, IDENTIFICATION AND REPAIR MONITORING OF CRACKED CONCRETE STRUCTURES –AN APPLICATION OF IMAGE PROCESSING 1.)***Detection and Segmentation of Cracks using CANNY and SOBEL filters implemented using MATLAB with a camera attached to a UAV.*
Published at International Conference on Communication and Electronics Systems - 2018
Link : <https://ieeexplore.ieee.org/document/8723898>
- 2018-19 **BACKGROUND MODELLING TECHNIQUES FOR FOREGROUND DETECTION AND TRACKING USING GAUSSIAN MIXTURE MODEL 1.)***To present the improvements in Object detection and tracking using Background Models (Implemented using Gaussian Mixture Modelling, by creating a model of the background in video frames.) when compared to Foreground Detection (Supervised Learning Algorithms) techniques.*
2.) *Able to limit the amount of False Positive detections to 10% with a 100-fold drop in training data.*
Published at International Conference on Computing Methodologies and Communication - 2019.
Link : <https://ieeexplore.ieee.org/document/8819825>
- 2020-21 **A HOST-LESS APPROACH TO VALIDATE CXL TEST CARD IN EMULATION** *Bus Functional Modelling of a CXL Host Processor using C++ to aid in CXL Test Card Emulation.*
Published at Design and Test Technology Conference - 2021
Intel Corporation Internal
- 2021-22 **STATISTICAL POWER MODELLING FOR A GRAPHICS PROCESSING UNIT** *The need for power estimation and performance modelling in GPUs and the statistical modelling algorithms implemented to achieve an accurate power prediction model running compute applications like cuBLAS, cuDNN and cuFFT.*
Published at International Conference on IoT in Social, Mobile, Analytics and Cloud - 2022.
IEEE-Xplore ISBN: 978-1-6654-6941-8
Link : Not available yet (Paper and Certificate attached)
- 2021-22 **A SYNTHETIC CXL TRAFFIC GENERATOR FOR SOC PERFORMANCE VALIDATION** *Developing a NUMA Aware Synthetic CXL Workload in C++ to compute Performance (Latency and Bandwidth) and implement False Sharing between CXL Subsystems.*
Published at Design and Test Technology Conference - 2022 (Intel Corporation Internal)
Presented at SuperCompute'22 (Intel) - <https://www.computeexpresslink.org/sc-22>
Github : <https://github.com/ychitkar>
- 2022-23 **PATENT : A METHOD TO SHARE MEMORY COHERENTLY ACROSS SYSTEM NODES USING CXL PROTOCOL** *Presenting a mechanism to share memories across systems without the use of huge back-store memories on CXL by earmarking a region of conventional memory from one of the connected system nodes. CXL protocol helps maintain coherency across the nodes thus eliminating the need for double-copying*
Submitted to Intel Patent Group committee, Under Review

Achievements

- 2011-2012 Top 10 percent in School *International Association Of Physics Teachers (IAPT)*
- 2014-2015 Topper in School *AISSCE Rank Holder for English*
- 2019 Top 5 percent in ETE *Rank Holder - 3rd Rank for Electronics and Telecommunications Engineering*

Software Skills

PROGRAMMING LANGUAGES : CUDA, Python, C++/DPC++, C, Scala, System Verilog , Java , Perl , PHP , MySQL
PLATFORMS USED : MATLAB , LabVIEW , PSpice , oneAPI , Simulink , Quartus Prime.