IC設計實驗期中考練習1　2024

班級:_____ 學號:_____ 姓名:_____ 成績:_____

1. The input signal rising/falling time is 0.5ns. The output loading is 1pf. Please design the 3-input dynamic XOR with the same delay time as 1ns for various input patterns. (0.95ns < T_{000}, T_{001}, T_{010}, T_{011}, T_{100}, T_{101}, T_{110}, T_{111} < 1.05ns) **(Function Validation: 30%, 0.8ns < Delay < 1.2ns: 30%, 0.9ns < Delay < 1.1ns: 10%, 0.95ns < Delay < 1.05ns: 10%)**

2. Please write down your consideration during constructing function and sizing procedure. **(20%)**

IC設計實驗期中考練習2　2024

班級:_____ 學號:_____ 姓名:_____ 成績:_____

1. The input signal rising/falling time is 0.5ns. The output loading is 1pf. Please design the 3-input pseudo nMOS XOR with the same delay time as 1ns for various input patterns. (0.95ns < T_{000}, T_{001}, T_{010}, T_{011}, T_{100}, T_{101}, T_{110}, T_{111} < 1.05ns) **(Function Validation: 30%, 0.8ns < Delay < 1.2ns: 30%, 0.9ns < Delay < 1.1ns: 10%, 0.95ns < Delay < 1.05ns: 10%)**

2. Please write down your consideration during constructing function and sizing procedure. **(20%)**

IC設計實驗期中考練習3　2024

班級:_____ 學號:_____ 姓名:_____ 成績:_____

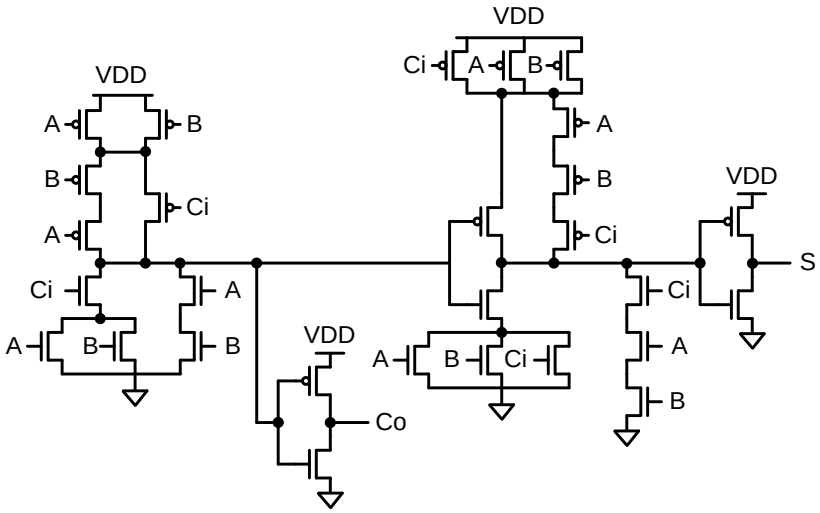
1. The input signal rising/falling time is 0.5ns. The output loading is 1pf. Please design the 3-input pass-transistor XOR with the same delay time as 1ns for various input patterns. (0.95ns < T_{000}, T_{001}, T_{010}, T_{011}, T_{100}, T_{101}, T_{110}, T_{111} < 1.05ns) **(Function Validation: 30%, 0.8ns < Delay < 1.2ns: 30%, 0.9ns < Delay < 1.1ns: 10%, 0.95ns < Delay < 1.05ns: 10%)**

2. Please write down your consideration during constructing function and sizing procedure. **(20%)**

IC設計實驗期中考練習4　2024

班級:_____ 學號:_____ 姓名:_____ 成績:_____

1. The input signal rising/falling time is 0.5ns. The output loading of Co and S is 1pf. Please design the single bit pseudo-nMOS Full-adder with the same rising time and falling time as 1ns in both S and Co. (0.95ns < T_{000}, T_{001}, T_{010}, T_{011}, T_{100}, T_{101}, T_{110}, T_{111} < 1.05ns) (You can only tune the size of transistor. Altering the circuit architecture is not allowed.)
   (Function Validation: 30%, 0.8ns < Delay < 1.2ns: 30%, 0.9ns < Delay < 1.1ns: 10%, 0.95ns < Delay < 1.05ns: 10%)



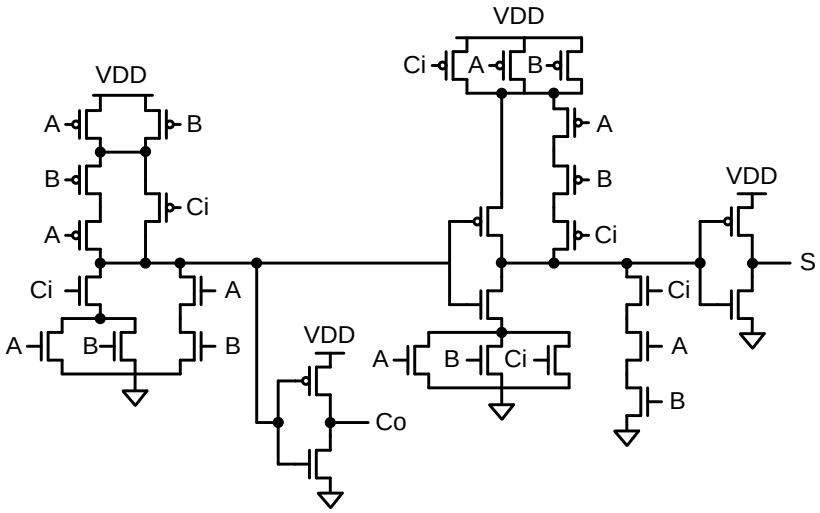
(Reference Full-Adder Circuit)

2. Please write down your consideration during constructing function and sizing procedure. **(20%)**

IC設計實驗期中考練習5　2024

班級:_____ 學號:_____ 姓名:_____ 成績:_____

1. The input signal rising/falling time is 0.5ns. The output loading of Co and S is 1pf. Please design the single bit dynamic CMOS Full-adder with the same rising time and falling time as 1ns in both S and Co. (0.95ns < T_{000}, T_{001}, T_{010}, T_{011}, T_{100}, T_{101}, T_{110}, T_{111} < 1.05ns) (You can only tune the size of transistor. Altering the circuit architecture is not allowed.)
   (Function Validation: 30%, 0.8ns < Delay < 1.2ns: 30%, 0.9ns < Delay < 1.1ns: 10%, 0.95ns < Delay < 1.05ns: 10%)



(Reference Full-Adder Circuit)

2. Please write down your consideration during constructing function and sizing procedure. **(20%)**

IC設計實驗期中考練習6　2024

班級:_____ 學號:_____ 姓名:_____ 成績:_____

1. The input signal rising/falling time is 0.5ns. The output loading is 0.5pf. Please design the 3-input pass-transistor A*B+C*(B*D+A*E) with the same delay time as 1ns for various input patterns. (0.95ns < T_{000}, T_{001}, T_{010}, T_{011}, T_{100}, T_{101}, T_{110}, T_{111} < 1.05ns) **(Function Validation: 30%, 0.8ns < Delay < 1.2ns: 30%, 0.9ns < Delay < 1.1ns: 10%, 0.95ns < Delay < 1.05ns: 10%)**

2. Please write down your consideration during constructing function and sizing procedure. **(20%)**

IC設計實驗期中考練習7　2024

班級:_____ 學號:_____ 姓名:_____ 成績:_____

1. The input signal rising/falling time is 0.5ns. The output loading of A=B, A>B, and A<B are all 0.5pf. Please design the comparator by using pseudo-nMOS with the same rising time and falling time as 1ns. (0.95ns < T_{00}, T_{01}, T_{10}, T_{11} < 1.05ns) (You can only tune the size of transistor. Altering the circuit architecture is not allowed.)
   (Function Validation: 30%, 0.8ns < Delay < 1.2ns: 30%, 0.9ns < Delay < 1.1ns: 10%, 0.95ns < Delay < 1.05ns: 10%)

表 1 一位元數位比較器真值表

輸入		輸出		
a	b	a < b	a = b	a > b
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

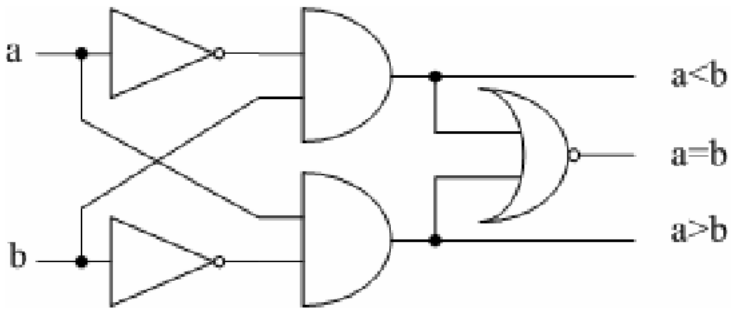


圖 1 一位元數位比較器電路圖

2. Please write down your consideration during constructing function and sizing procedure. **(20%)**

IC設計實驗期中考練習8　2024

班級:_____ 學號:_____ 姓名:_____ 成績:_____

1. The input signal rising/falling time is 0.5ns. The output loading of A=B, A>B, and A<B are all 0.5pf. Please design the comparator by using dynamic CMOS logic with the same rising time and falling time as 1ns. (0.95ns < T_{00}, T_{01}, T_{10}, T_{11} < 1.05ns) (You can only tune the size of transistor. Altering the circuit architecture is not allowed.)
   (Function Validation: 30%, 0.8ns < Delay < 1.2ns: 30%, 0.9ns < Delay < 1.1ns: 10%, 0.95ns < Delay < 1.05ns: 10%)

表 1 一位元數位比較器真值表

輸入		輸出		
a	b	a < b	a = b	a > b
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

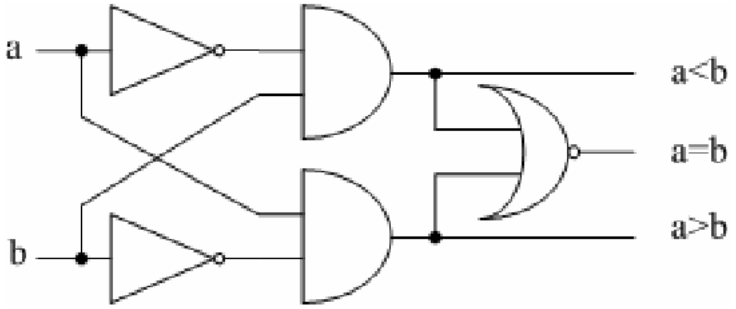


圖 1 一位元數位比較器電路圖

2. Please write down your consideration during constructing function and sizing procedure. **(20%)**

IC設計實驗期中考練習9　2024

班級:_____ 學號:_____ 姓名:_____ 成績:_____

1. The input signal rising/falling time is 0.5ns. The output loading of A=B, A>B, and A<B are all 2pf. Please design the comparator by using pass-transistor with the same rising time and falling time as 1ns. (0.95ns < T_{00}, T_{01}, T_{10}, T_{11} < 1.05ns) (You can only tune the size of transistor. Altering the circuit architecture is not allowed.)
   (Function Validation: 30%, 0.8ns < Delay < 1.2ns: 30%, 0.9ns < Delay < 1.1ns: 10%, 0.95ns < Delay < 1.05ns: 10%)

表 1 一位元數位比較器真值表

輸入		輸出		
a	b	a < b	a = b	a > b
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

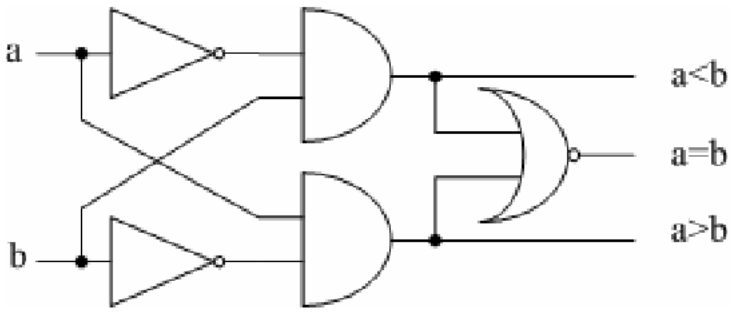


圖 1 一位元數位比較器電路圖

2. Please write down your consideration during constructing function and sizing procedure. **(20%)**

IC設計實驗期中考練習10　2024

班級:_____ 學號:_____ 姓名:_____ 成績:_____

3. The input signal rising/falling time is 0.5ns. The output loading is 2pf. Please design the circuit by using pass-transistor with the same rising time and falling time as 1ns. (0.95ns < T_{00}, T_{01}, T_{10}, T_{11} < 1.05ns)
   (Function Validation: 30%, 0.8ns < Delay < 1.2ns: 30%, 0.9ns < Delay < 1.1ns: 10%, 0.95ns < Delay < 1.05ns: 10%)

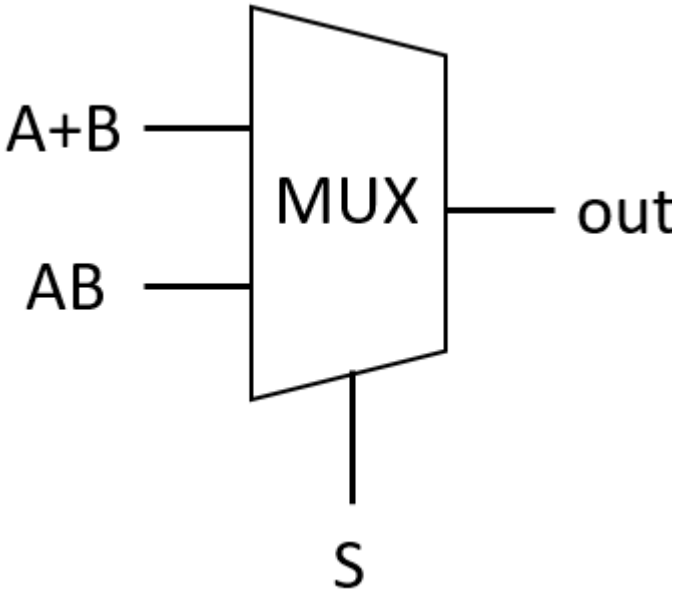


圖1 要求相關電路

4. Please write down your consideration during constructing function and sizing procedure. **(20%)**