IC設計實驗期中考

班級:_____ 學號:_____ 姓名:_____ 成績:

The input signal rising/falling time is 0.5ns. The output loading is 0.5pf. Please design the **3-input dynamic XOR** with **the same delay time as 0.5ns** for various input patterns. (0.4ns < T_{000}, T_{001}, T_{010}, T_{011}, T_{100}, T_{101}, T_{110}, T_{111} < 0.6ns) **(Function Validation: 50%, 0.3ns < Delay < 0.7ns: 30%, 0.4ns < Delay < 0.6ns: 20%)**

IC設計實驗期中考

班級:_____ 學號:_____ 姓名:_____ 成績:

The input signal rising/falling time is 0.2ns. The output loading is 0.5pf. Please design the **3-input pseudo nMOS XOR** with the same delay time as 1ns for various input patterns. (0.4ns < T_{000}, T_{001}, T_{010}, T_{011}, T_{100}, T_{101}, T_{110}, T_{111} < 0.6ns) **(Function Validation: 50%, 0.3ns < Delay < 0.7ns: 30%, 0.4ns < Delay < 0.6ns: 20%)**

IC設計實驗期中考

班級:_____ 學號:_____ 姓名:_____ 成績:

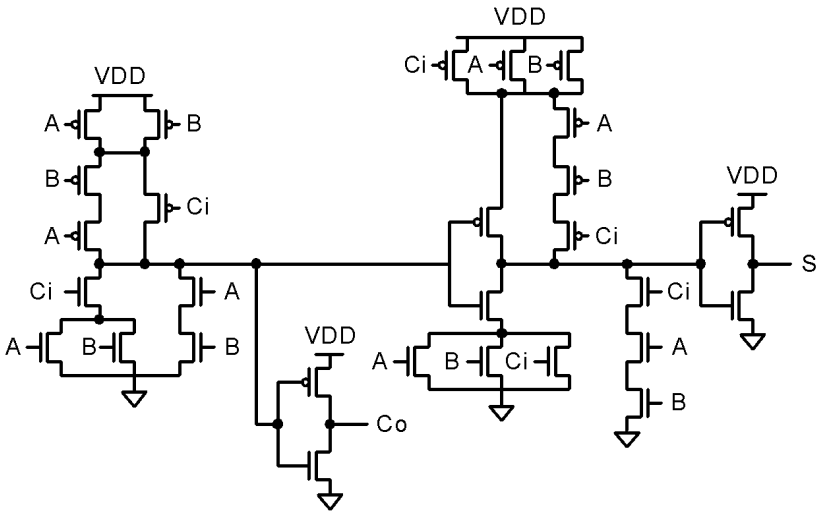
The input signal rising/falling time is 0.2ns. The output loading is 0.5pf. Please design the **3-input pass-transistor XOR** with the same delay time as 0.5ns for various input patterns. (0.4ns < T_{000}, T_{001}, T_{010}, T_{011}, T_{100}, T_{101}, T_{110}, T_{111} < 0.6ns) **(Function Validation: 50%, 0.3ns < Delay < 0.7ns: 30%, 0.4ns < Delay < 0.6ns: 20%)**

IC設計實驗期中考

班級:_____ 學號:_____ 姓名:_____ 成績:

The input signal rising/falling time is 0.5ns. The output loading of Co and S is 0.5pf. Please design the **single bit pseudo-nMOS Full-adder** with the same rising time and falling time as 0.6ns in both S and Co. (0.5ns < T_{000}, T_{001}, T_{010}, T_{011}, T_{100}, T_{101}, T_{110}, T_{111} < 0.7ns) (You can only tune the size of transistor. Altering the circuit architecture is not allowed.)

(Function Validation: 50%, 0.4ns < Delay < 0.8ns: 30%, 0.5ns < Delay < 0.7ns: 20%)



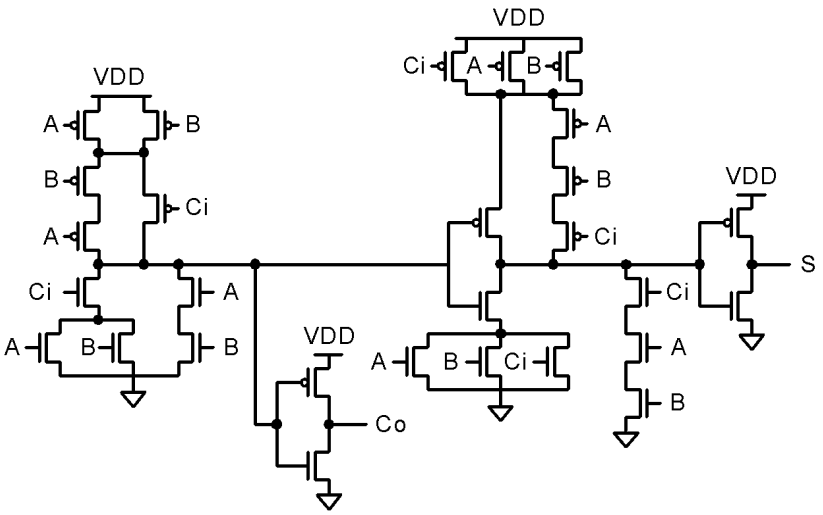
(Reference Full-Adder Circuit)

IC設計實驗期中考

班級:_____ 學號:_____ 姓名:_____ 成績:

The input signal rising/falling time is 0.5ns. The output loading of Co and S is 1pf. Please design the **single bit dynamic CMOS Full-adder** with the same rising time and falling time as 1ns in both S and Co. (0.9ns < T_{000}, T_{001}, T_{010}, T_{011}, T_{100}, T_{101}, T_{110}, T_{111} < 1.1ns) (You can only tune the size of transistor. Altering the circuit architecture is not allowed.)

(Function Validation: 50%, 0.8ns < Delay < 1.2ns: 30%, 0.9ns < Delay < 1.1ns: 20%)



(Reference Full-Adder Circuit)

IC設計實驗期中考

班級:_____ 學號:_____ 姓名:_____ 成績:

The input signal rising/falling time is 0.5ns. The output loading of A=B, A>B, and A<B are all 0.5pf. Please design the comparator by using **pseudo-nMOS** with the same rising time and falling time as 0.5ns. (0.4ns < T_{00}, T_{01}, T_{10}, T_{11} < 0.6ns) (You can only tune the size of transistor. Altering the circuit architecture is not allowed.)

(Function Validation: 50%, 0.3ns < Delay < 0.7ns: 30%, 0.4ns < Delay < 0.6ns: 20%)

表 1 一位元數位比較器真值表

輸入		輸出		
a	b	a < b	a = b	a > b
0	0	0	1	0
0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

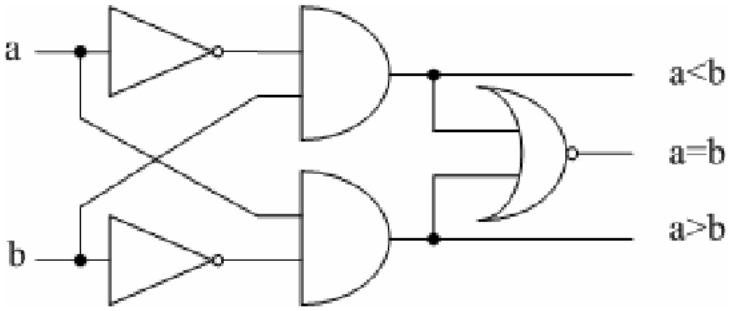


圖 1 一位元數位比較器電路圖

IC設計實驗期中考

班級:_____ 學號:_____ 姓名:_____ 成績:

The input signal rising/falling time is 0.5ns. The output loading of A=B, A>B, and A<B are all 0.5pf. Please design **the comparator by using dynamic CMOS logic** with the same rising time and falling time as 0.5ns. (0.4ns < T_{00}, T_{01}, T_{10}, T_{11} < 0.6ns) (You can only tune the size of transistor. Altering the circuit architecture is not allowed.)

(Function Validation: 50%, 0.3ns < Delay < 0.7ns: 30%, 0.4ns < Delay < 0.6ns: 20%)

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1	1	0	1	0

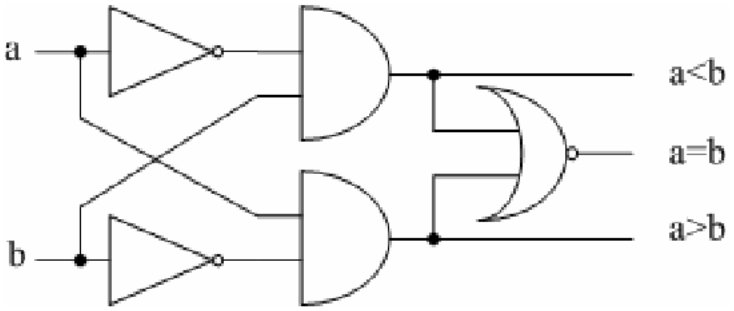

圖 1 一位元數位比較器電路圖

IC設計實驗期中考

班級:_____ 學號:_____ 姓名:_____ 成績:

The input signal rising/falling time is 0.5ns. The output loading of A=B, A>B, and A<B are all 0.5pf. Please design the comparator by using **pass-transistor** with the same rising time and falling time as 0.6ns. (0.5ns < T_{00}, T_{01}, T_{10}, T_{11} < 0.7ns) (You can only tune the size of transistor. Altering the circuit architecture is not allowed.)

(Function Validation: 50%, 0.4ns < Delay < 0.8ns: 30%, 0.5ns < Delay < 0.7ns: 20%)

表 1 一位元數位比較器真值表

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0	1	1	0	0
1	0	0	0	1
1	1	0	1	0

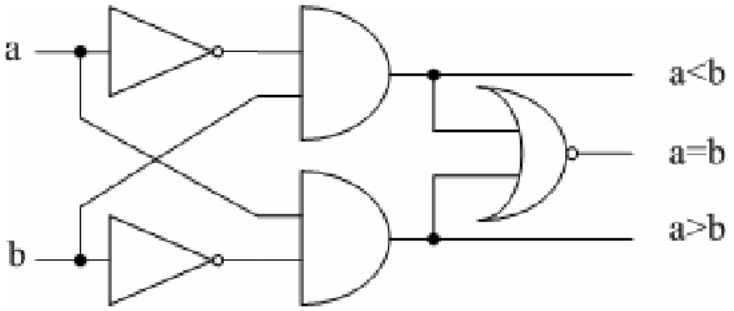

圖 1 一位元數位比較器電路圖