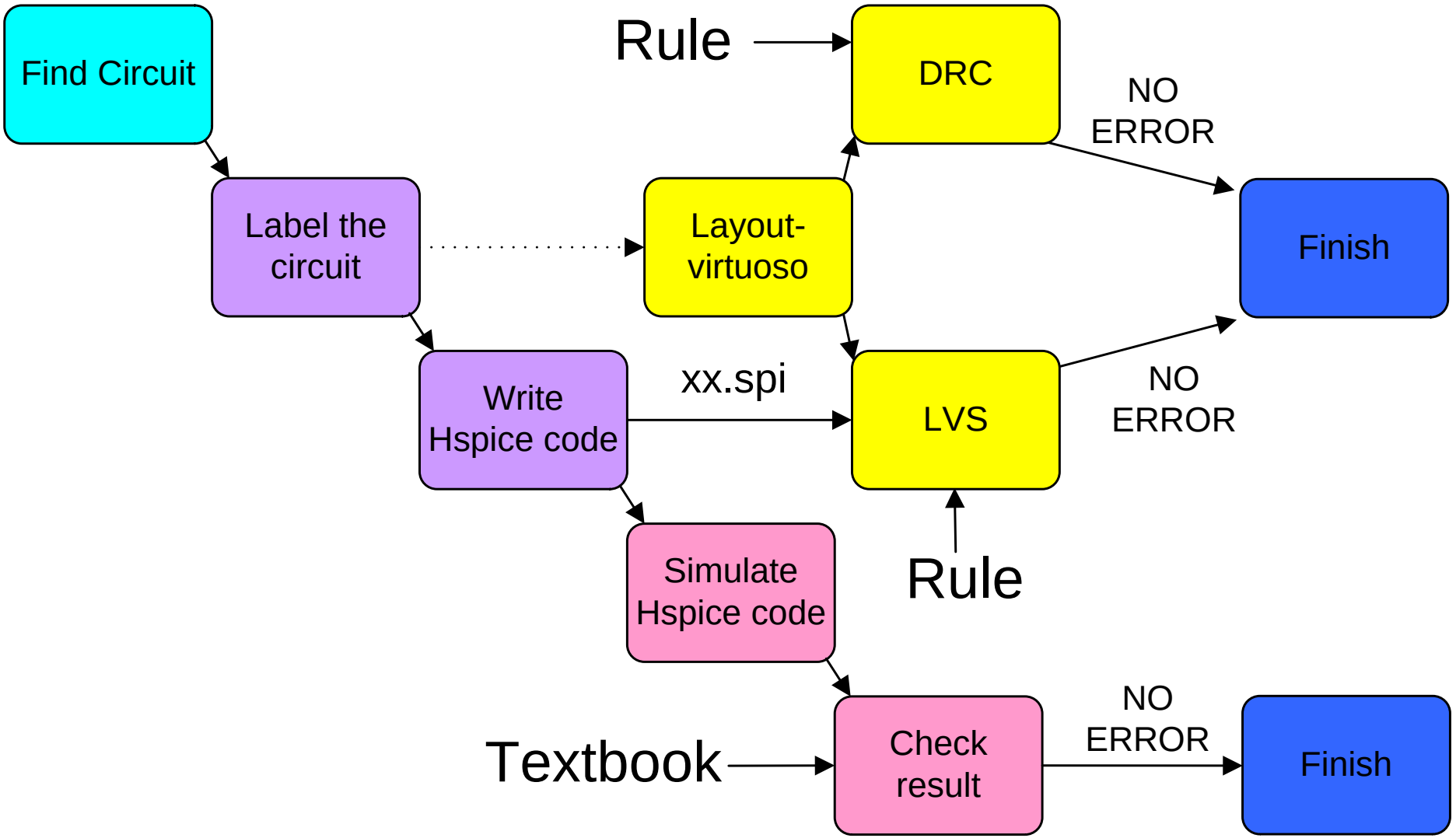
Layout Tool

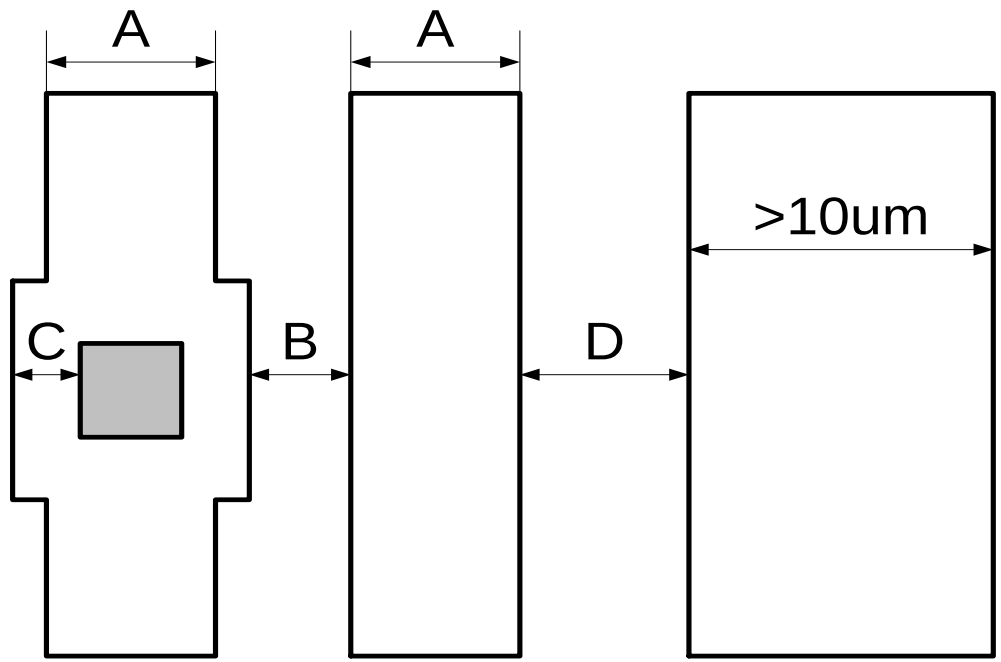
Design Flow Chart



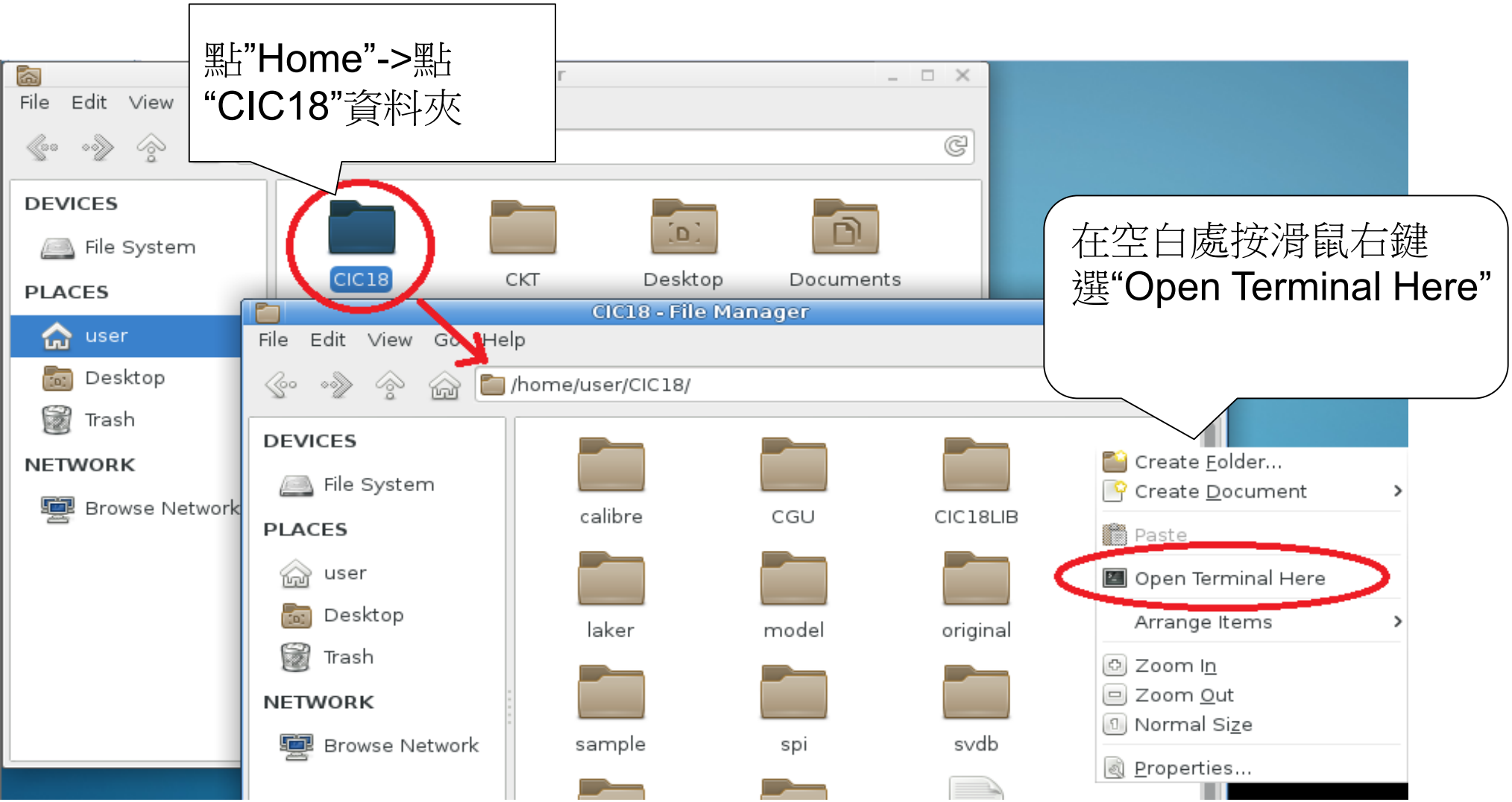
Begin of Cadence Virtuoso

- How to implement physical devices?
  - Transistors, Resistors, Capacitors, Inductors.
  - The layout structure for different technologies are usually different.
- Get the files
  - Layer name for Metal, Poly, Diffusion, Contact, Via.
  - Technology file – cic18.tf (defined by foundry)
  - Display layers – display.drf (can be modified)

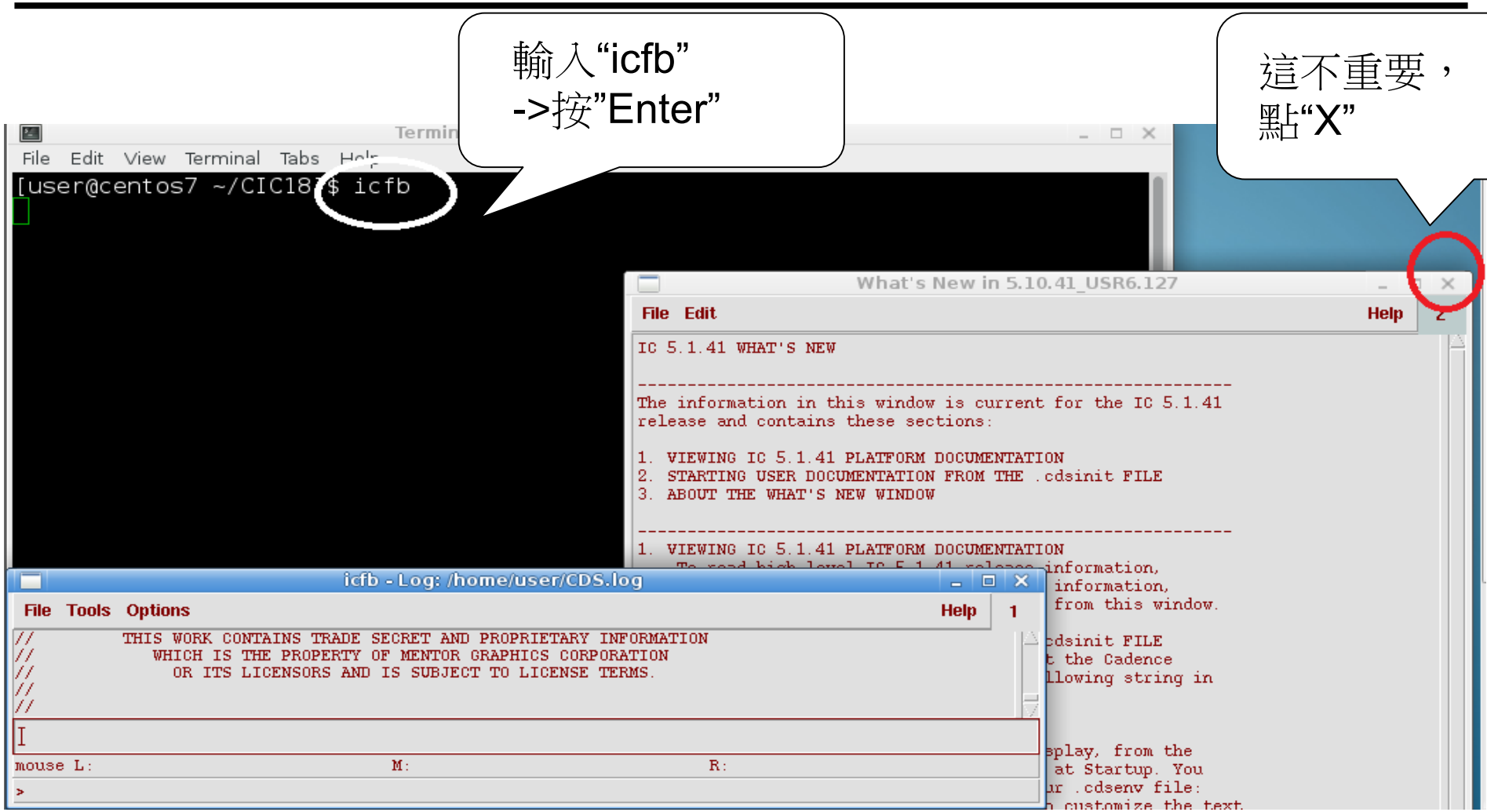
- Preparing required information
  - Design Rules
    - Spacing, Pitch, Width, Area
    - Design rule document



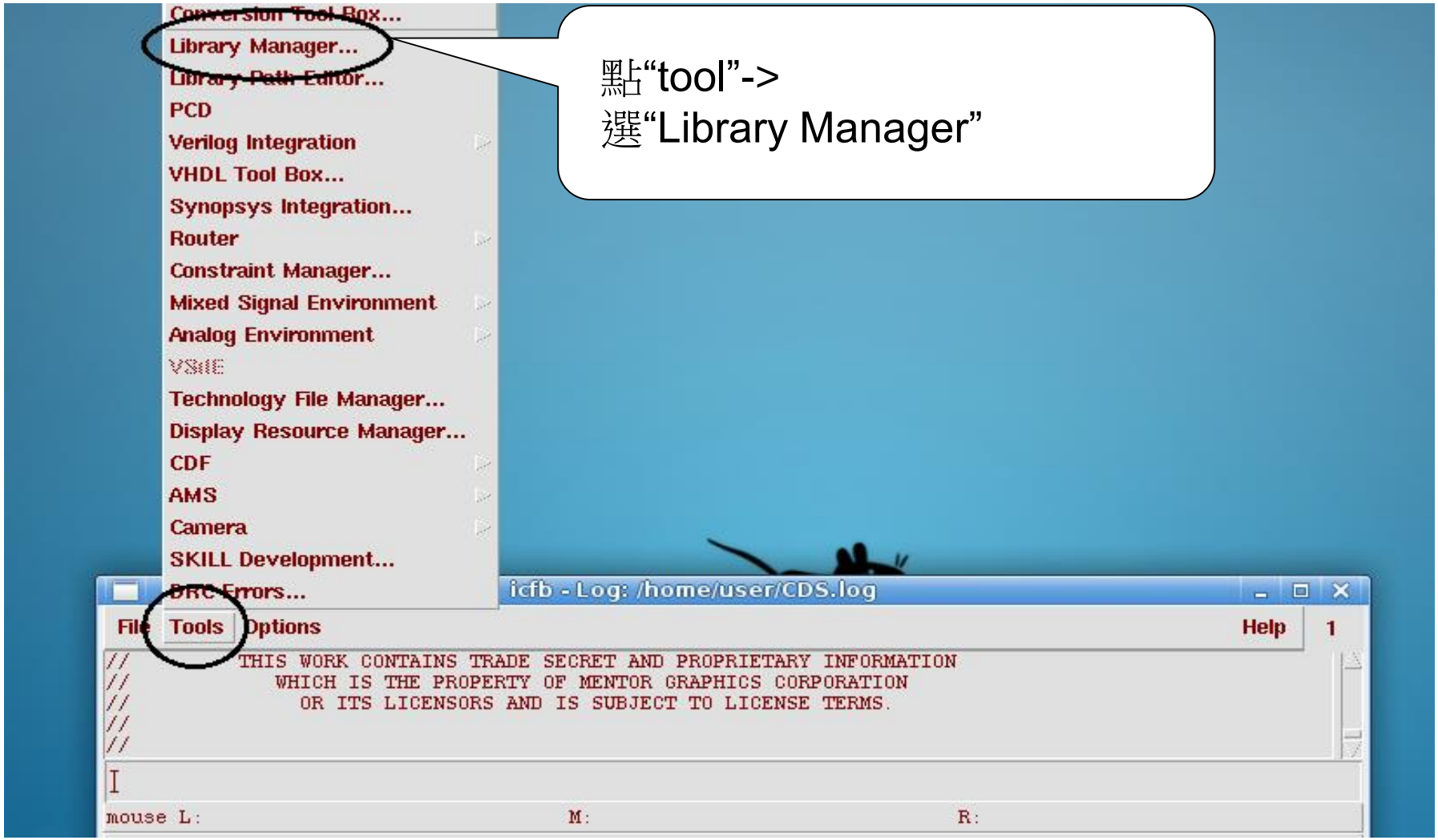
Start Virtuoso



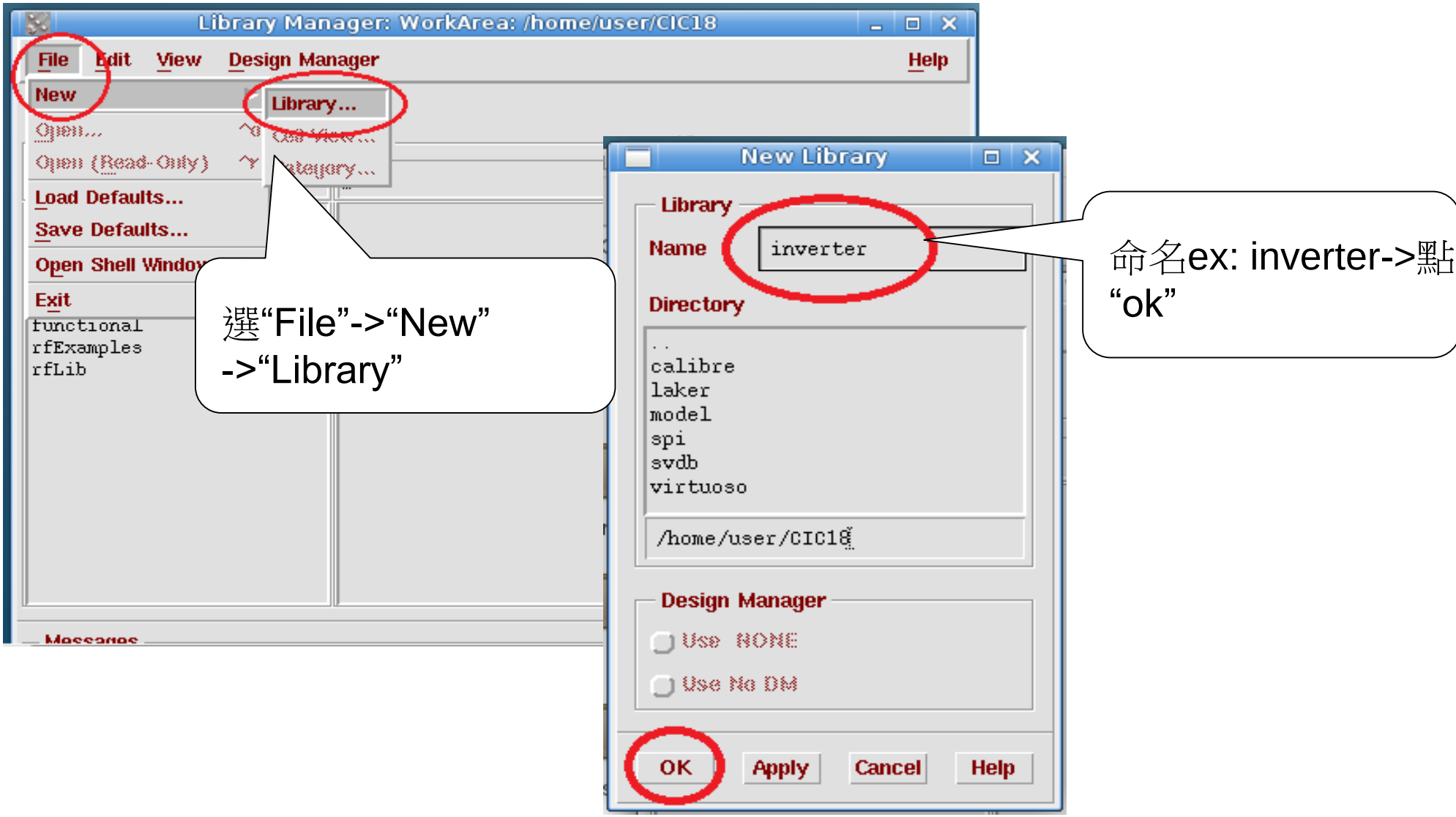
Start Virtuoso



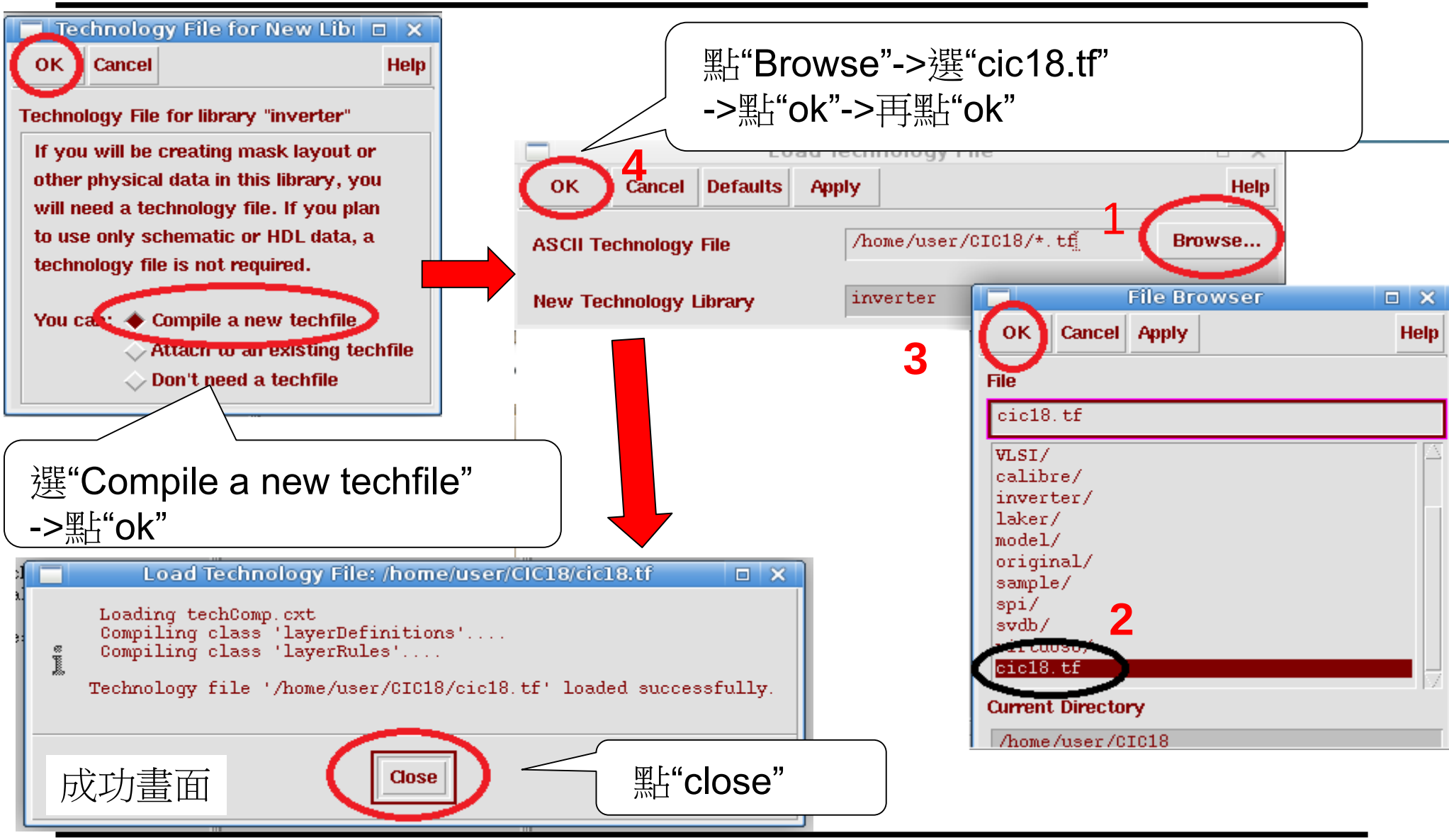
Create a New Library



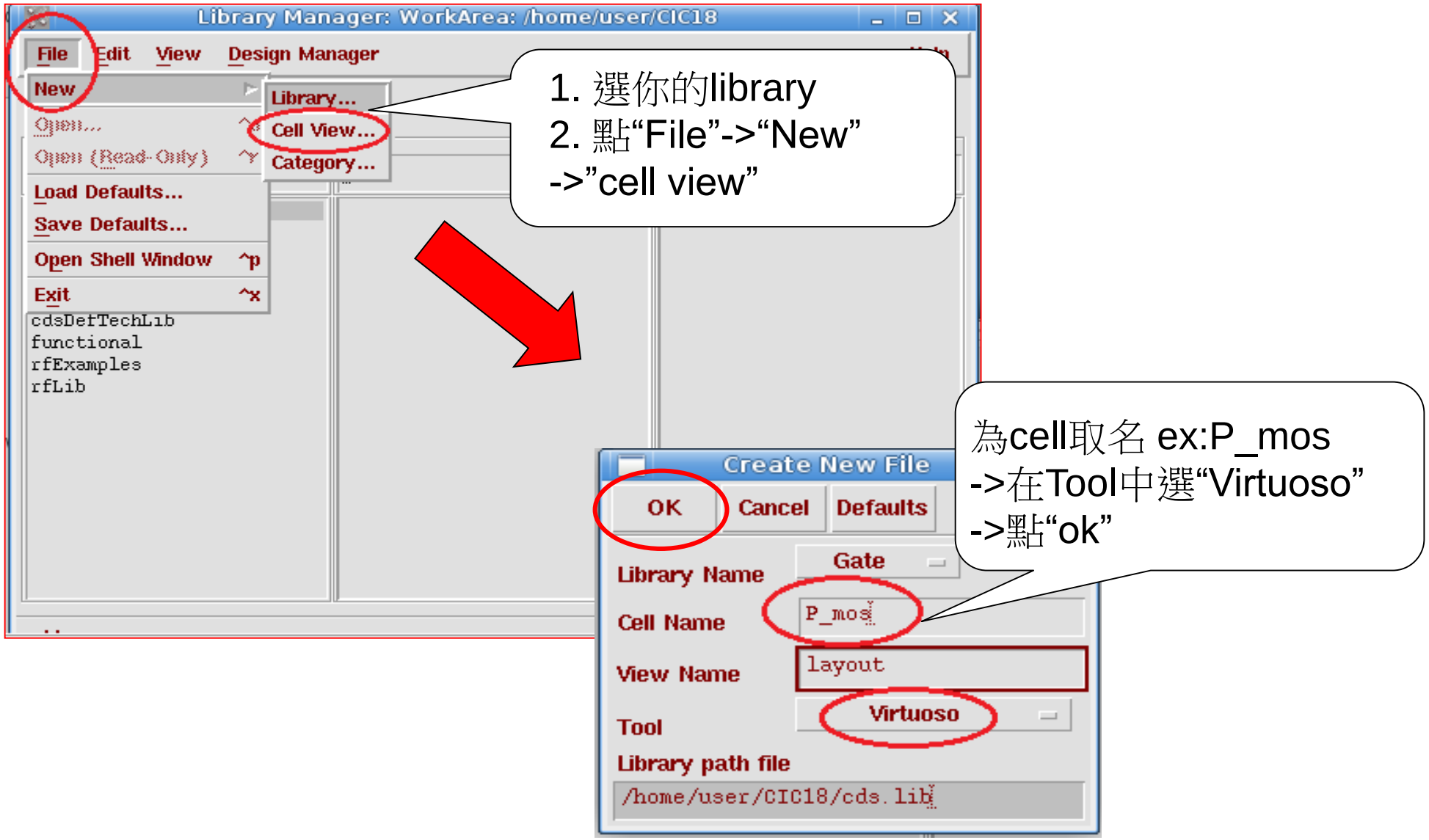
Create a New Library



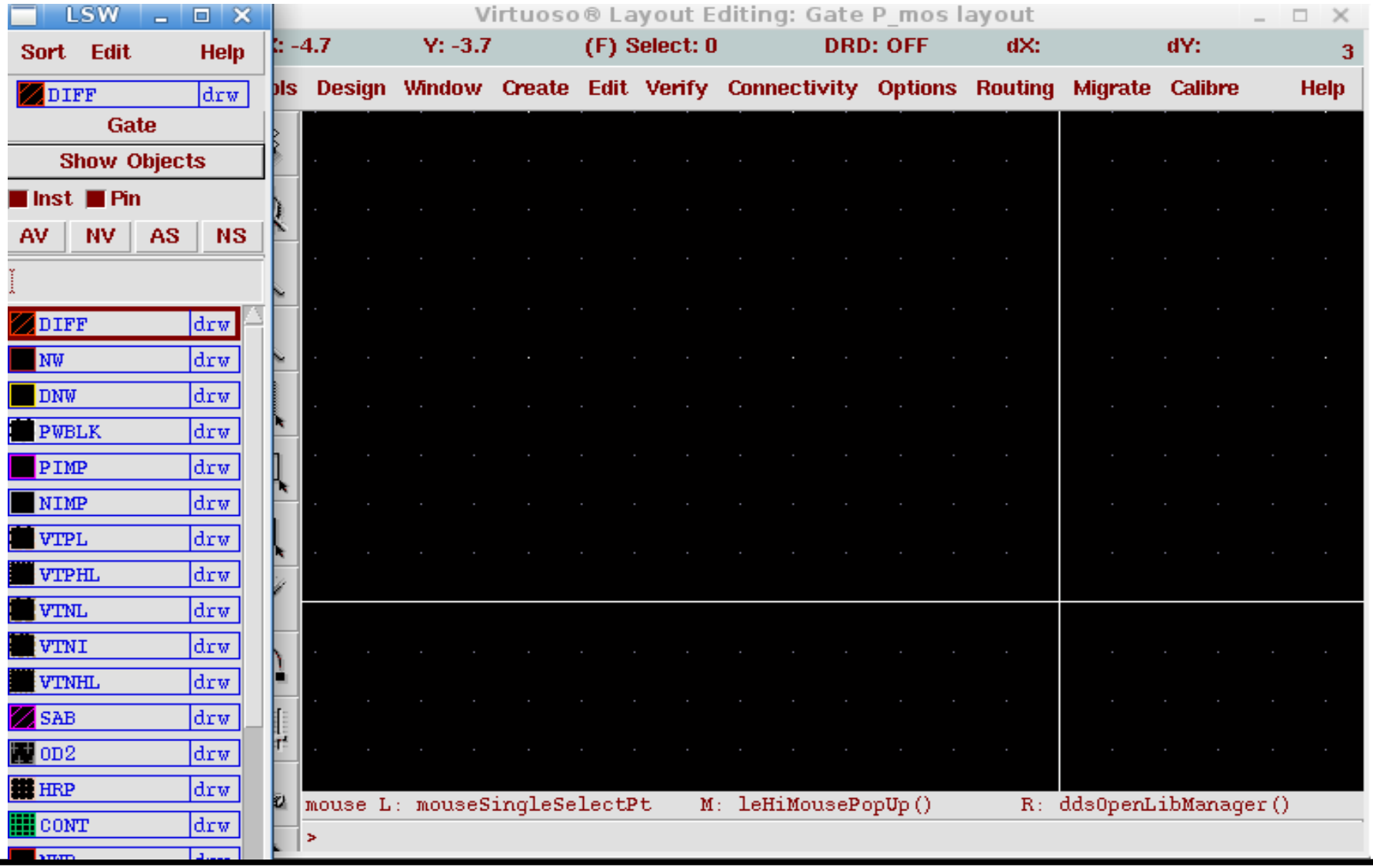
Create a New Library



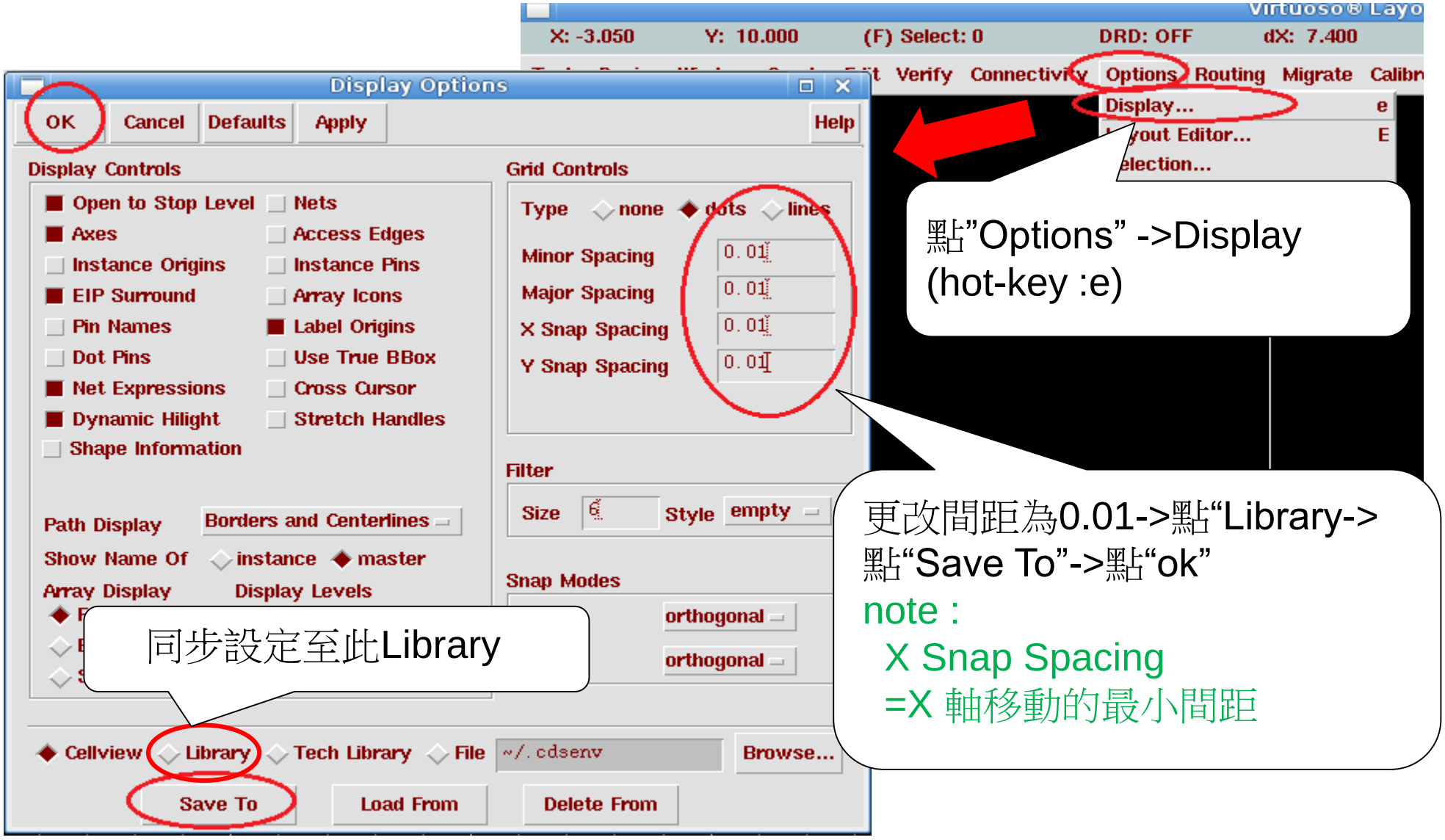
產生cell


Library Manager: WorkArea: /home/user/CIC18
File
Edit
View
Design Manager
New
Open...
Open (Read-Only)
Load Defaults...
Save Defaults...
Open Shell Window ^p
Exit ^x
Library...
Cell View...
Category...
cdsDefTechLib
functional
rfExamples
rfLib
1. 選你的library
2. 點“File”->“New”
->”cell view”
Create New File
OK
Cancel
Defaults
Library Name
Gate
Cell Name
P_mos
View Name
layout
Tool
Virtuoso
Library path file
/home/user/CIC18/cds.lib
為cell取名 ex:P_mos
->在Tool中選“Virtuoso”
->點“ok”

產生Layout視窗


LSW
Sort Edit Help
DIFF drw
Gate
Show Objects
Inst Pin
AV NV AS NS
DIFF drw
NW drw
DNW drw
PWBLK drw
PIMP drw
NIMP drw
VTPL drw
VTPHL drw
VTNL drw
VTNI drw
VTNHL drw
SAB drw
OD2 drw
HRP drw
CONT drw
Virtuoso® Layout Editing: Gate P_mos layout
Y: -3.7
(F) Select: 0
DRD: OFF
dX:
dY:
Design Window Create Edit Verify Connectivity Options Routing Migrate Calibre Help
mouse L: mouseSingleSelectPt M: leHiMousePopUp() R: ddsOpenLibManager()
>

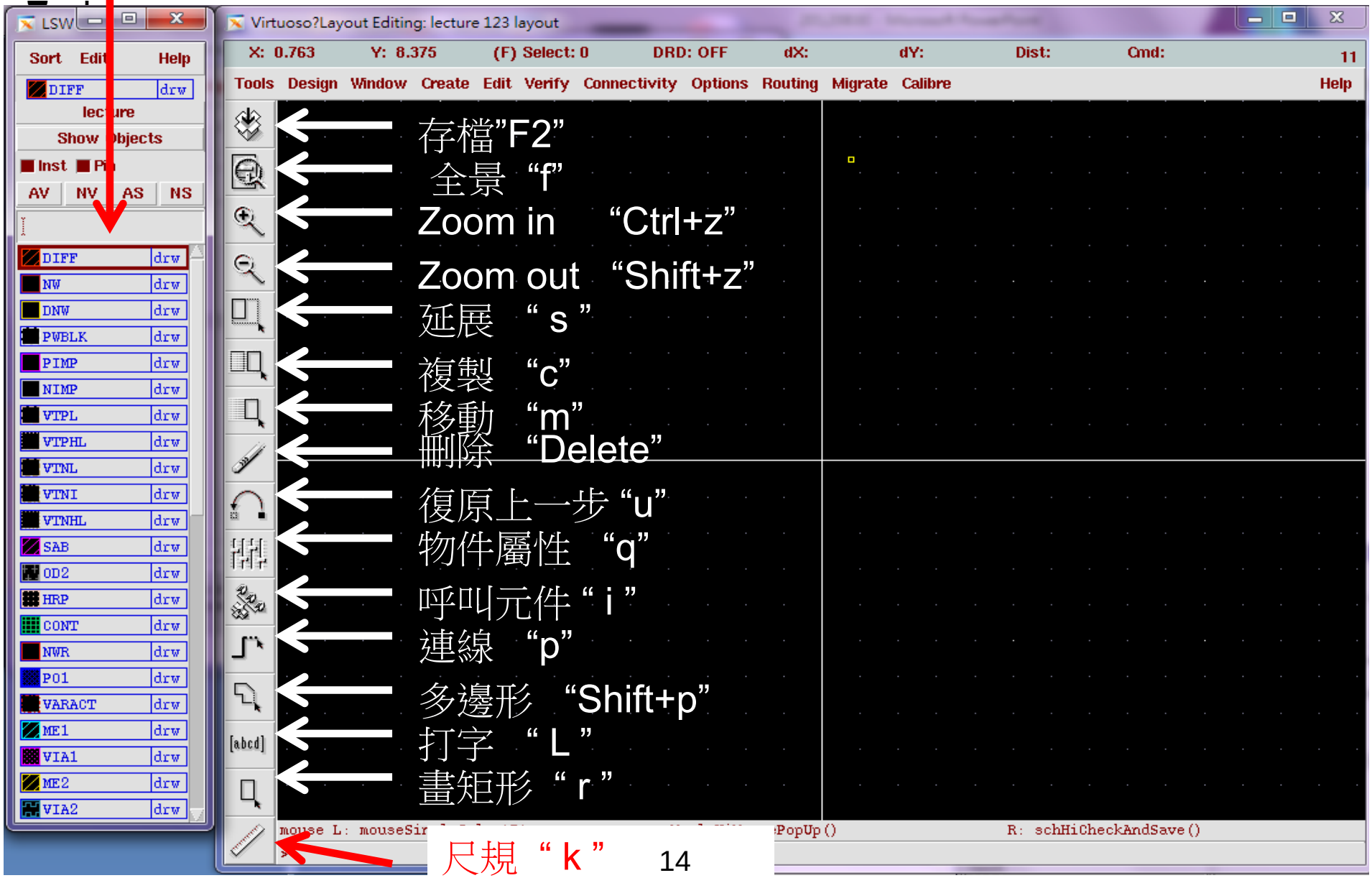
Grid設定


X: -3.050
Y: 10.000
(F) Select: 0
DRD: OFF
dX: 7.400
Verify
Connectivity
Options
Routing
Migrate
Display...
Display Options
OK
Cancel
Defaults
Apply
Help
Display Controls
Open to Stop Level
Axes
Instance Origins
EIP Surround
Pin Names
Dot Pins
Net Expressions
Dynamic Hilight
Shape Information
Nets
Access Edges
Instance Pins
Array Icons
Label Origins
Use True BBox
Cross Cursor
Stretch Handles
Grid Controls
Type
none
dots
lines
Minor Spacing
0.01
Major Spacing
0.01
X Snap Spacing
0.01
Y Snap Spacing
0.01
Filter
Size
Style
empty
Path Display
Borders and Centerlines
Show Name Of
instance
master
Array Display
Display Levels
Snap Modes
orthogonal
orthogonal
Cellview
Library
Tech Library
File
~/.cdsenv
Browse...
Save To
Load From
Delete From
點”Options” ->Display
(hot-key :e)
同步設定至此Library
更改間距為0.01->點“Library->
點“Save To”->點“ok”
note :
X Snap Spacing
=X 軸移動的最小間距

Virtuoso 快捷鍵

快捷鍵	功能	快捷鍵	功能
c	複製	f	顯示全圖
m	移動	i	呼叫元件
k	尺規	p	劃線長短(path)
u	還原上一步	r	劃長方形
e	改變色彩與解析度設定	q	元件內部屬性
s	圖形延伸或縮小	l	標籤工具，標籤要加在特定的text層，打I/O與vdd，gnd腳位名
左鍵拖曳	選擇下一功能方塊	右鍵拖曳	所選方塊全部放大
Shift+k	消除所有尺規	Ctrl+z	放大
Shift+z	縮小	Shift+c	裁切(Chop)
Esc	清除剛键入的命令	Delete	刪除元件
shift+m	合并工具(Merge)	F2	儲存

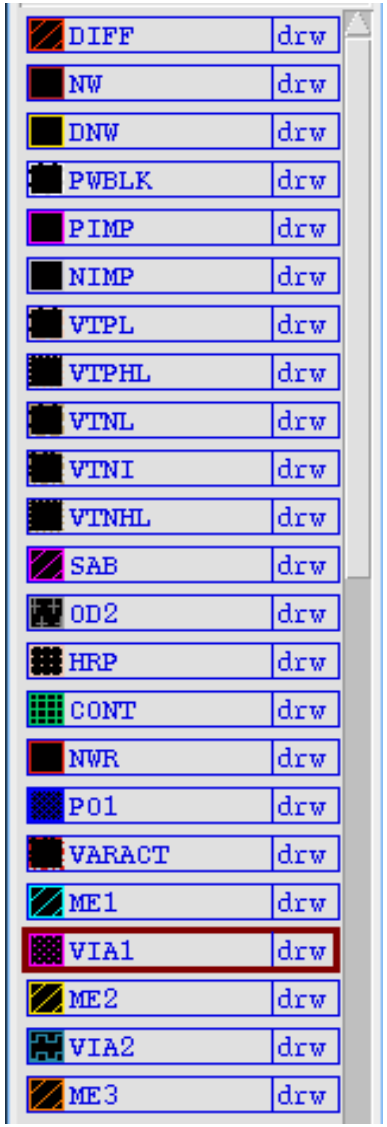
Virtuoso 快捷鍵



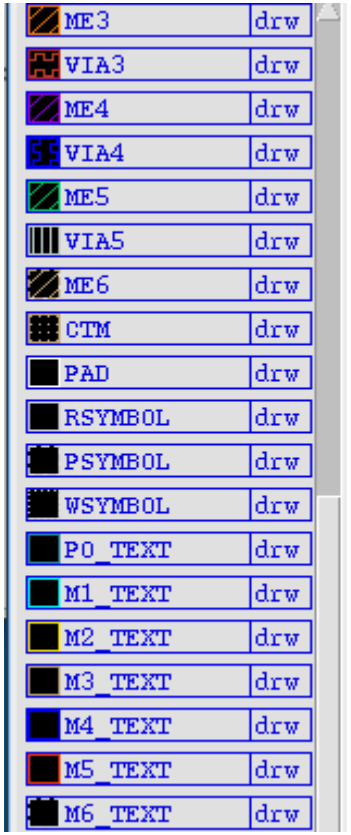
材質


LSW
Sort Edit Help
DIFF drw
lecture
Show Objects
Inst Pin
AV NV AS NS
DIFF drw
NW drw
DNW drw
PWBLK drw
PIMP drw
NIMP drw
VTPL drw
VTPHL drw
VTNL drw
VTNI drw
VTNHL drw
SAB drw
OD2 drw
HRP drw
CONT drw
NWR drw
PO1 drw
VARACT drw
ME1 drw
VIA1 drw
ME2 drw
VIA2 drw
Virtuoso?Layout Editing: lecture 123 layout
X: 0.763 Y: 8.375 (F) Select: 0 DRD: OFF dX: dY: Dist: Cmd: 11
Tools Design Window Create Edit Verify Connectivity Options Routing Migrate Calibre Help
黑底=P Substrate
mouse L: mouseSingleSelectPt M: leHiMousePopUp() R: schHiCheckAndSave()
>

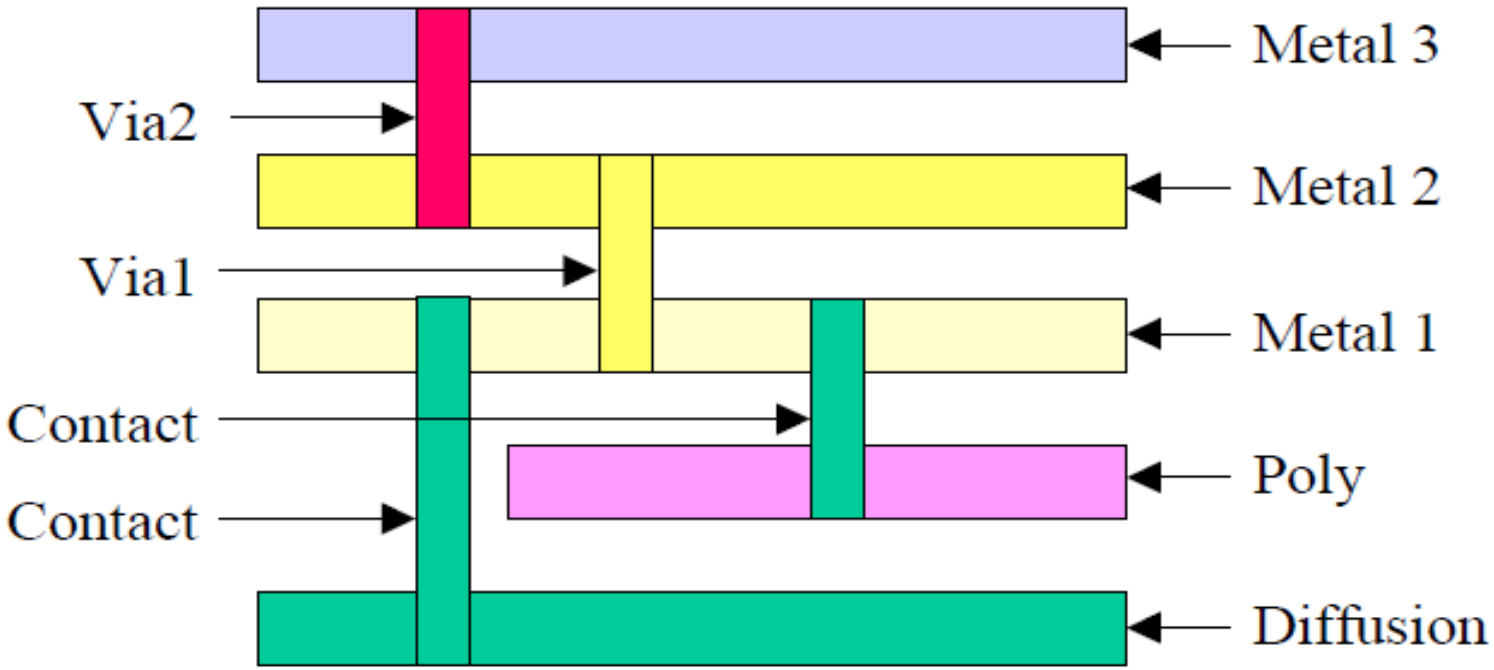
材質



材質名	LSW名
Nwell	NW
N+	NIMP
P+	PIMP
Poly	PO1
Active	DIFF
Contact	CONT
Metal1	ME1
Via1	VIA1
Text	M1_TEXT

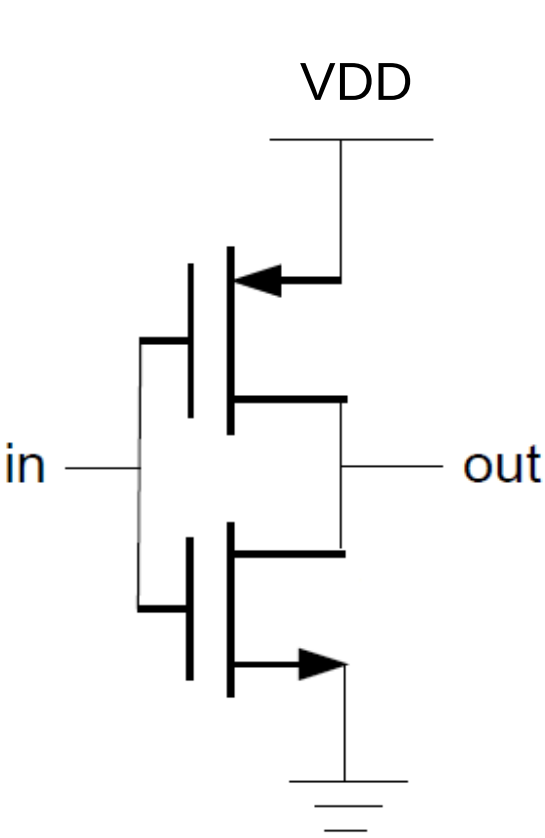


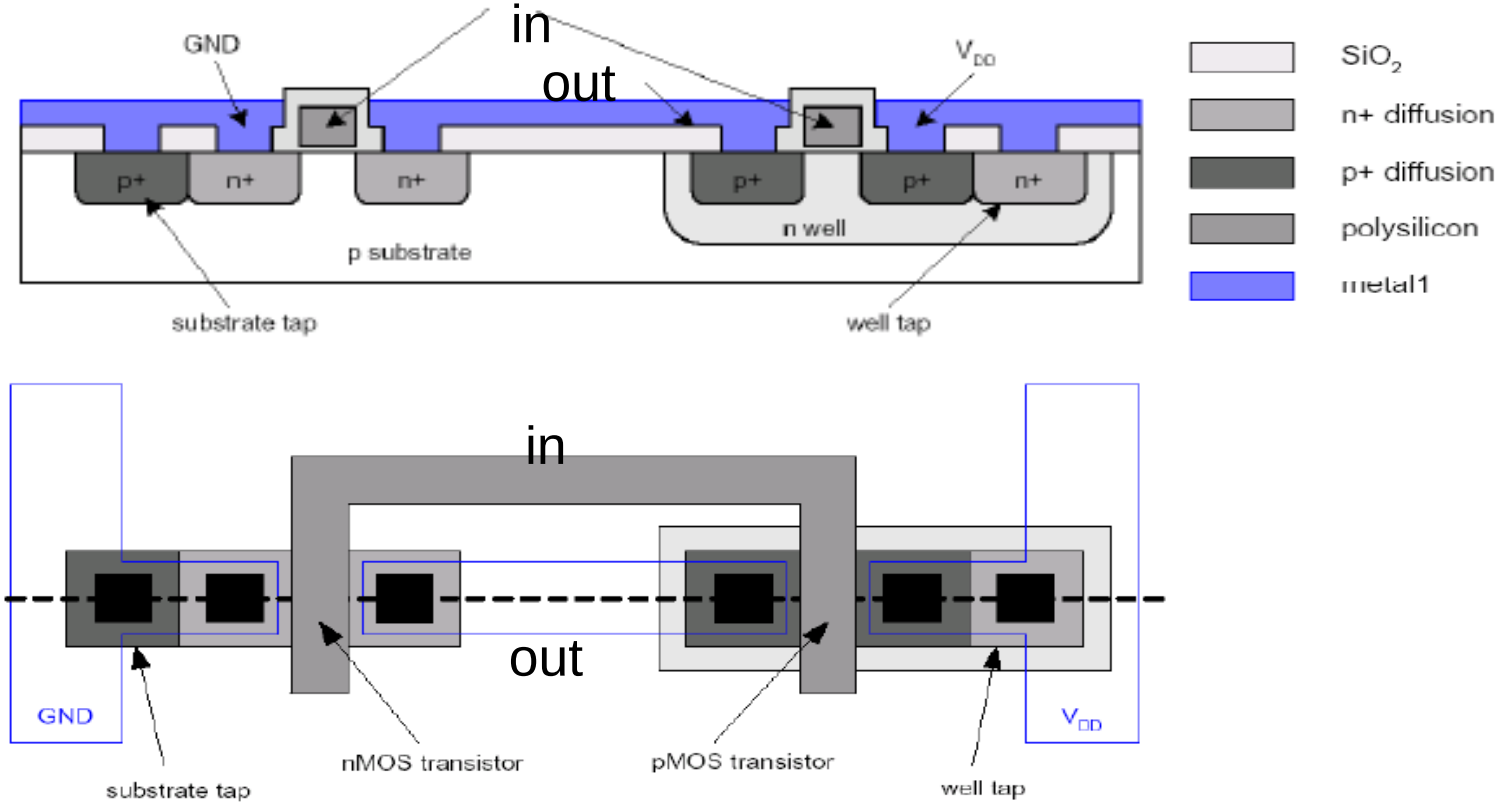
各層中連接貫孔的用法


Metal 3
Via2
Metal 2
Via1
Metal 1
Contact
Poly
Contact
Diffusion

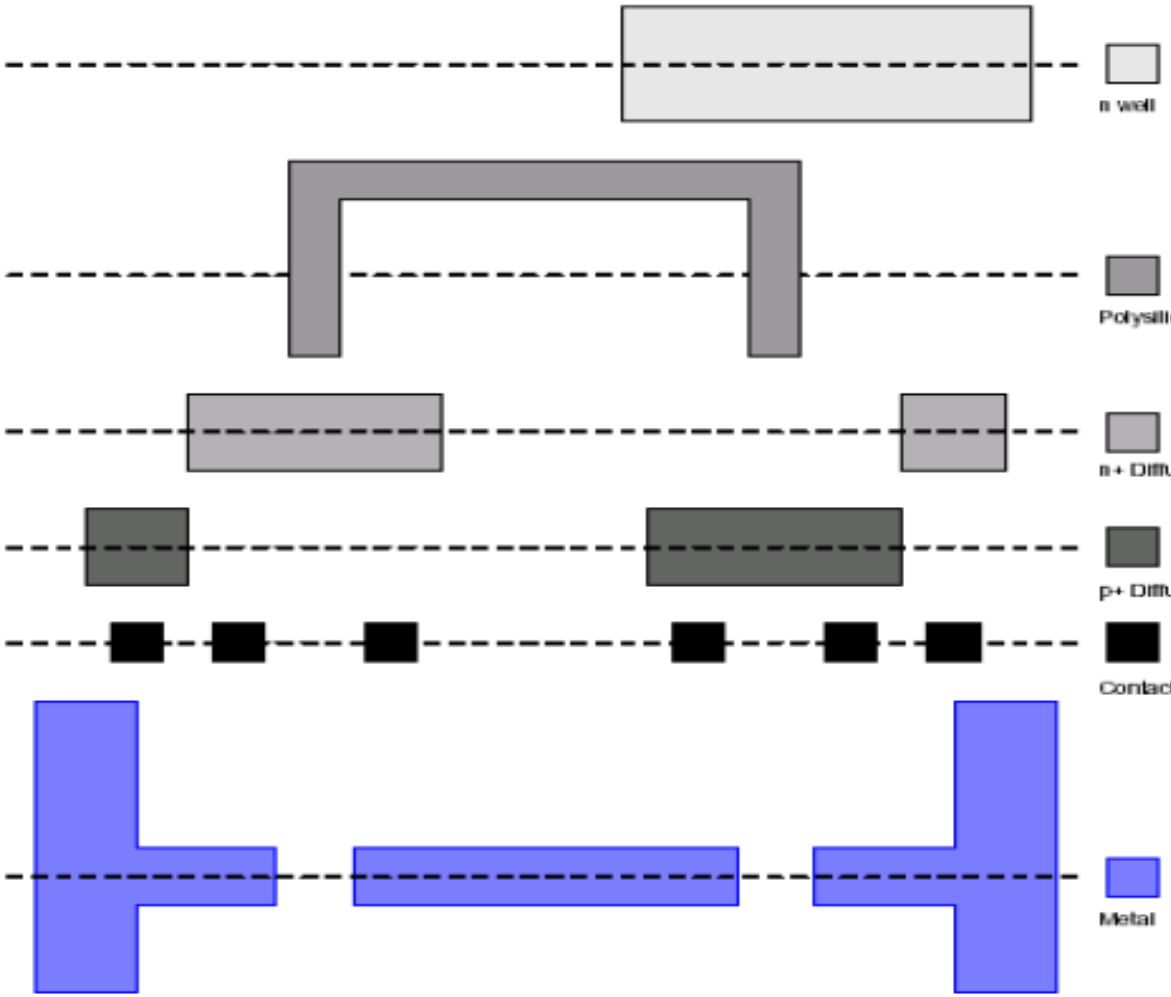
Example of inverter

inverter


VDD
in
out


GND
in
out
V_{DD}
p+
n+
n+
p+
p+
n+
n well
p substrate
substrate tap
well tap
SiO_2
n+ diffusion
p+ diffusion
polysilicon
metal1
in
out
GND
V_{DD}
substrate tap
nMOS transistor
pMOS transistor
well tap

inverter



NWELL (NW)

Polysilicon (PO1)

N^+ Diffusion=Nimp + Diff

P^+ Diffusion=Pimp +Diff

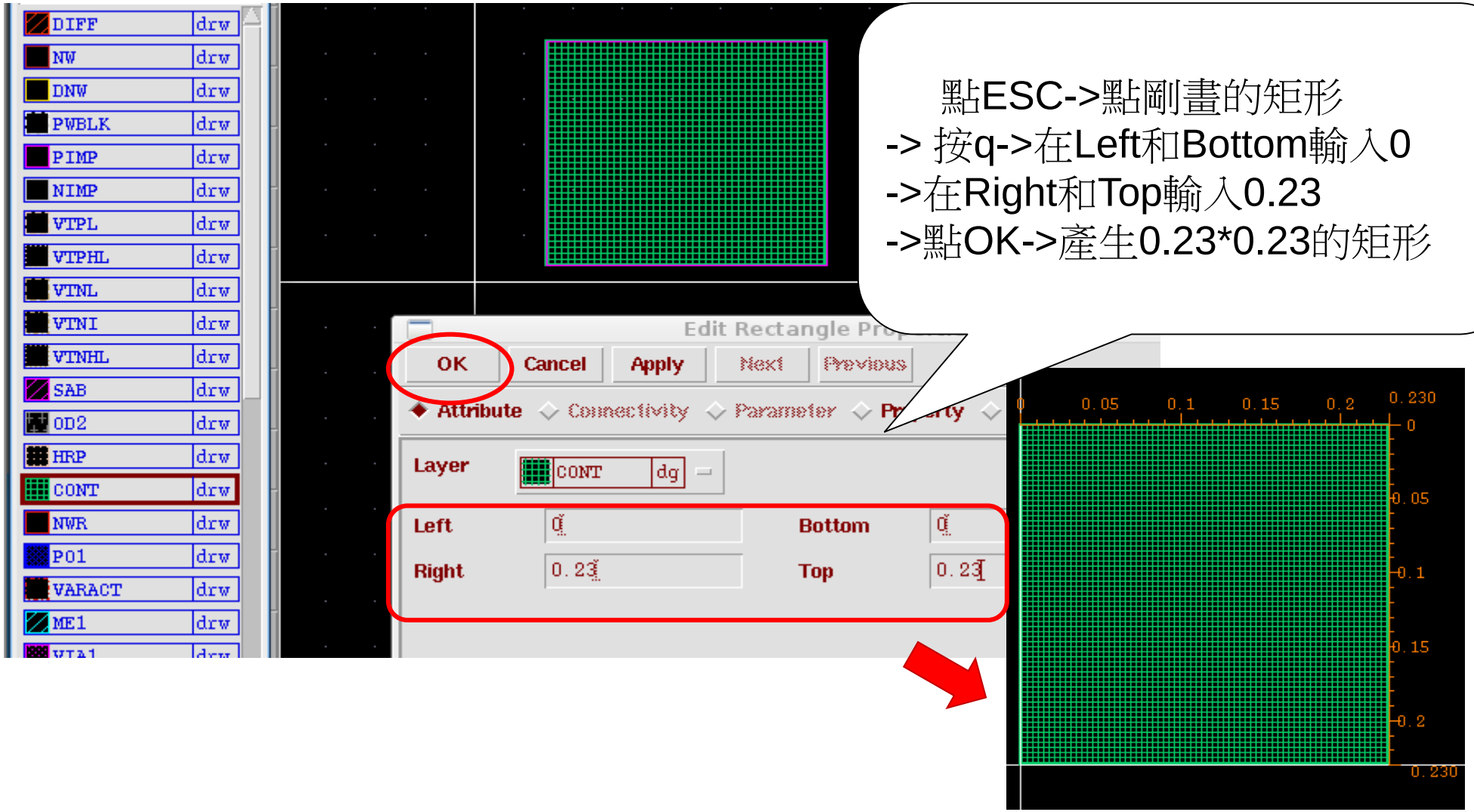
Contact(CON T)

Metal (ME)

畫Contact


LSW
Sort Edit Help
CONT drw
Summer1
Show Objects
Inst Pin
AV NV AS NS
VTPL drw
VTPHL drw
VTNL drw
VTNI drw
VTNHL drw
SAB drw
OD2 drw
HRP drw
CONT drw
NWR drw
PO1 drw
VARACT drw
ME1 drw
VIA1 drw
ME2 drw
VIA2 drw
Virtuoso® Layout E
2.47 Y: 0.70 (F) Select: 0 DRD: OFF dX: 2.53 dY
Design Window Create Edit Verify Connectivity Options Routing Migrate Calib
在LSW中選材質(CONT)
->按r(畫矩形)->點一下左鍵
->拉出想要的大小的矩形
->點一下左鍵

畫Contact

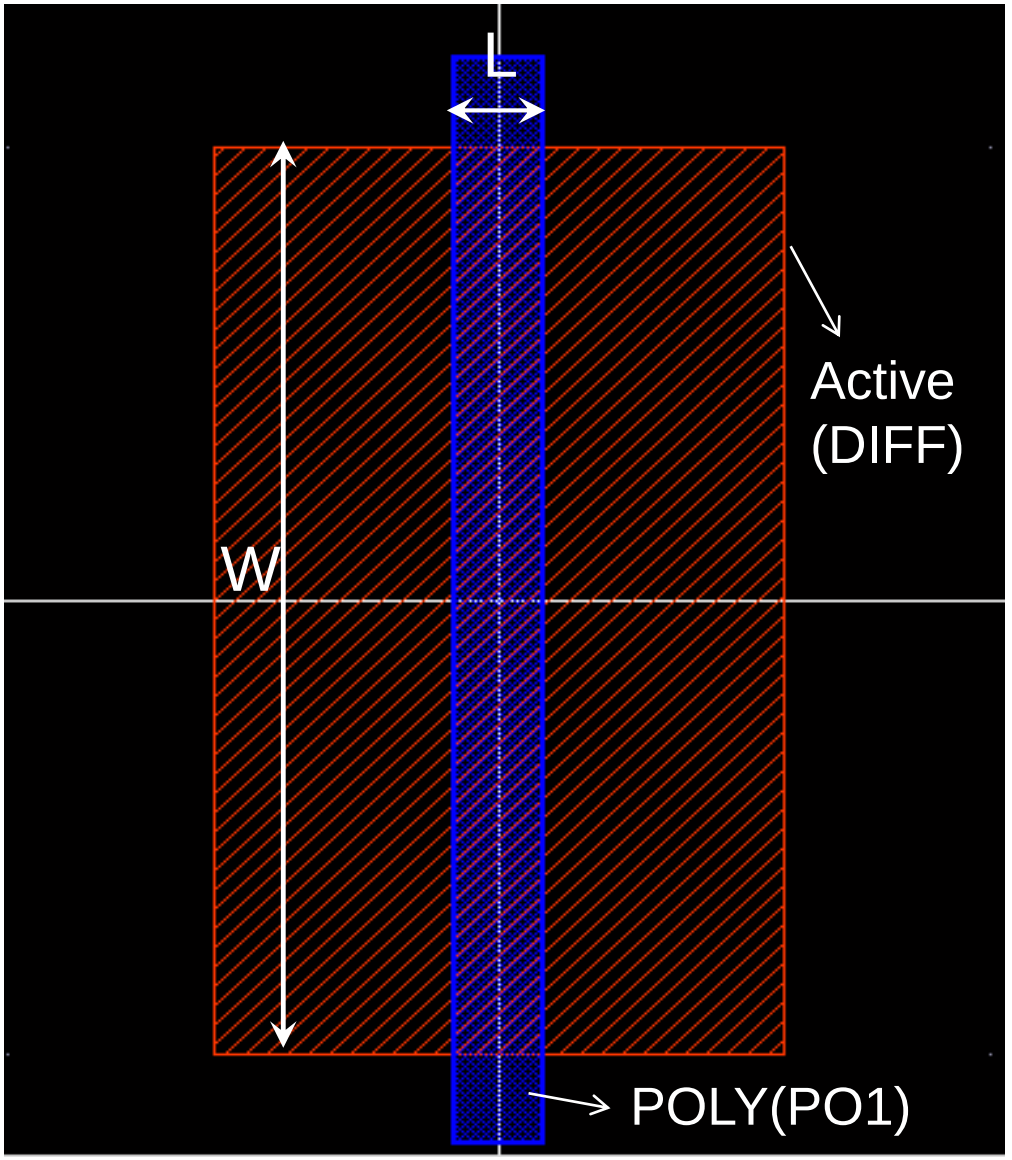


點ESC->點剛畫的矩形
-> 按q->在Left和Bottom輸入0
->在Right和Top輸入0.23
->點OK->產生0.23*0.23的矩形

繪製NMOS

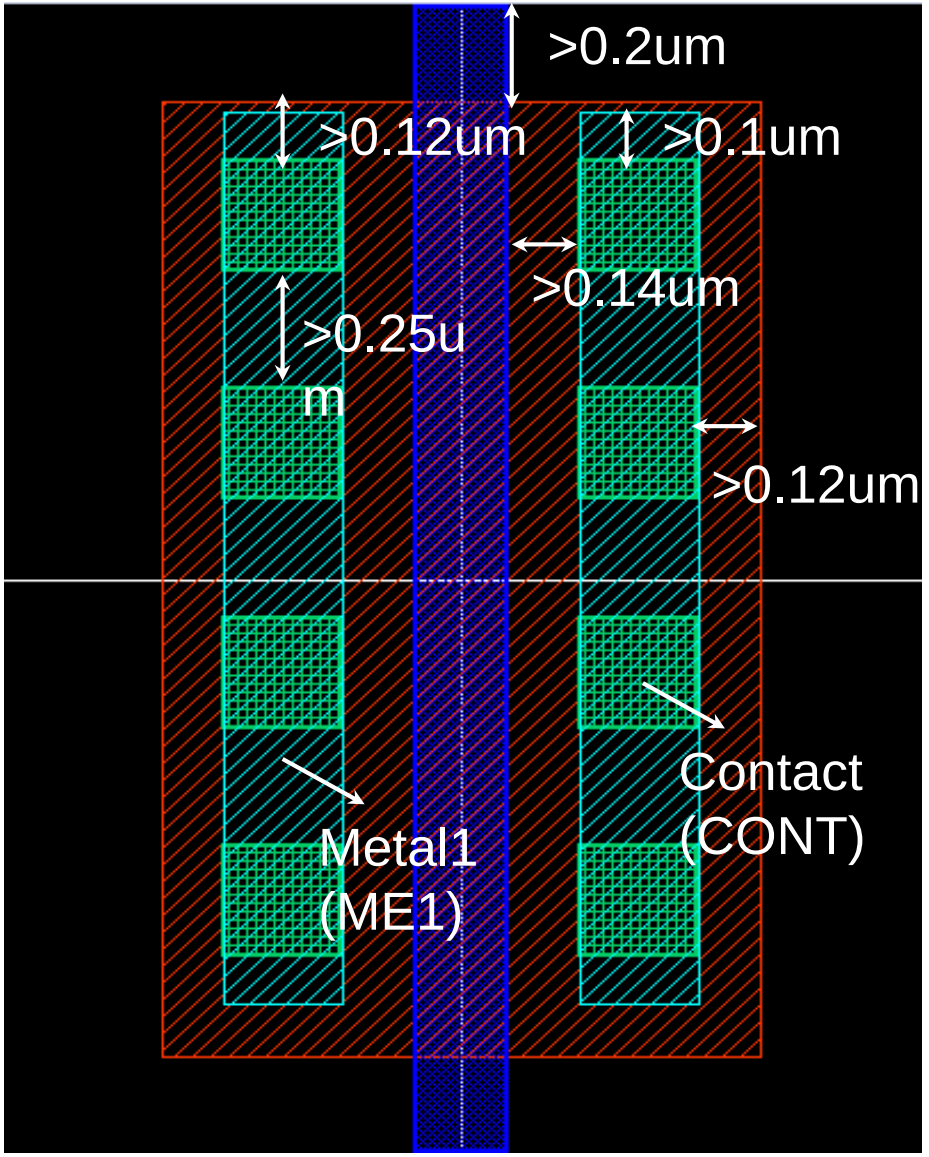
1. 用尺規來量測距離，將會加速布局的速度，按「快速鍵k」後，再拉至所需範圍。

2. 如要把尺規量測距離給刪除，按快速鍵Shift+k。



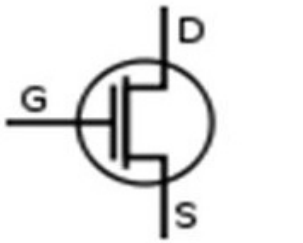
繪製NMOS

1. POLY and Active >0.2um
2. POLY and Contact >0.14um
3. Metal1 and Contact >0.1um
4. Contact and Contact >0.25um
5. Active and Contact >0.12um

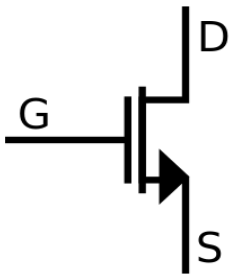


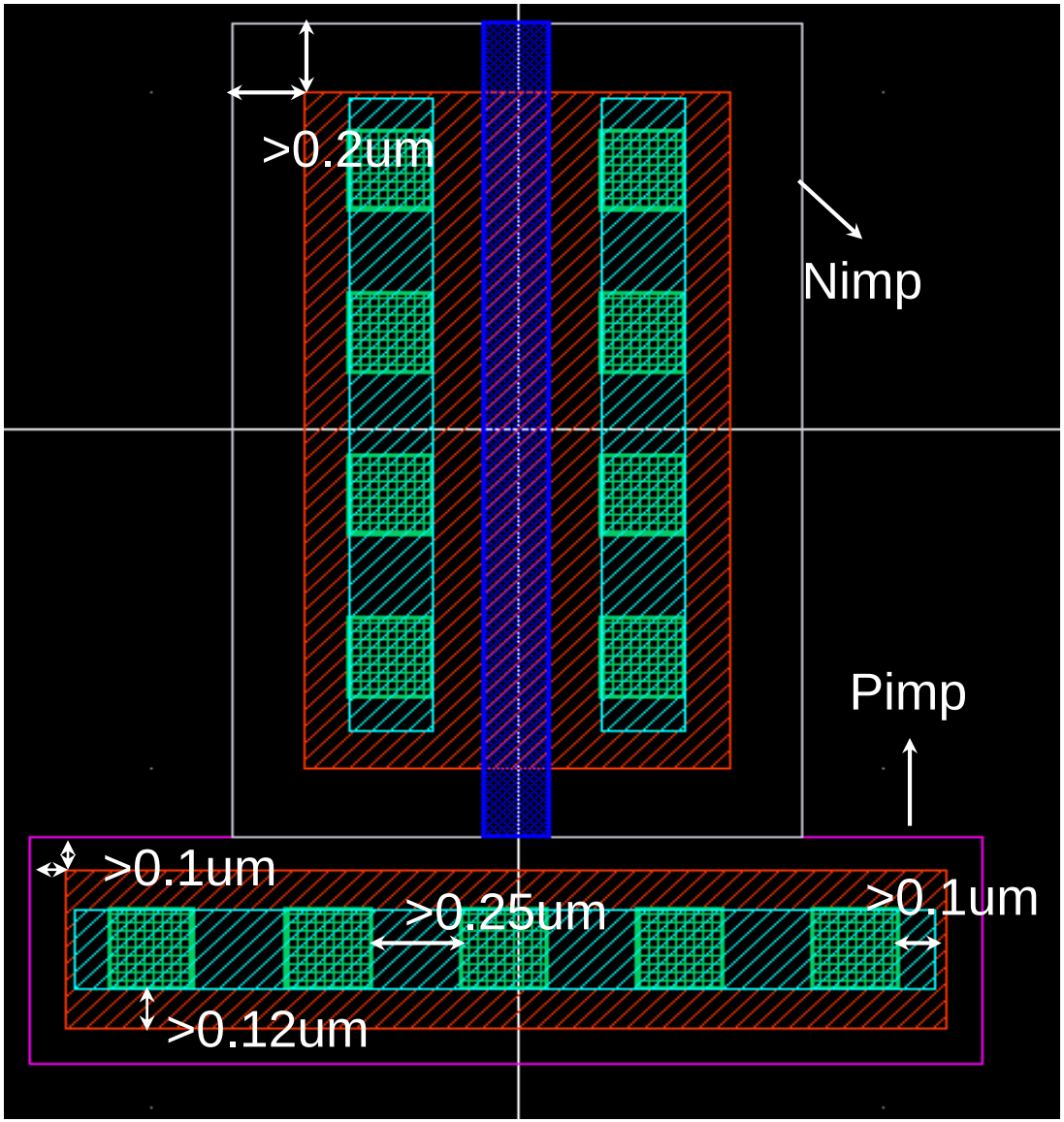
繪製NMOS

1. Metal1 and Contact >0.1um
2. Contact and Contact >0.25um
3. Active and Contact >0.12um
4. Nimp and Active >0.2um
5. Pimp and Active >0.1um



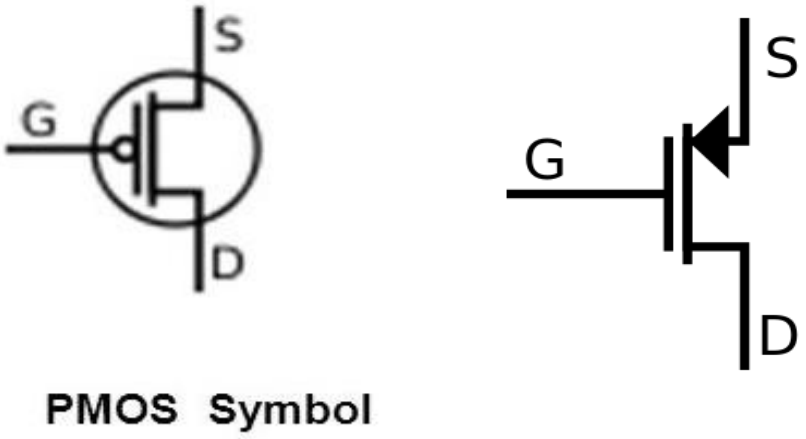
NMOS Symbol



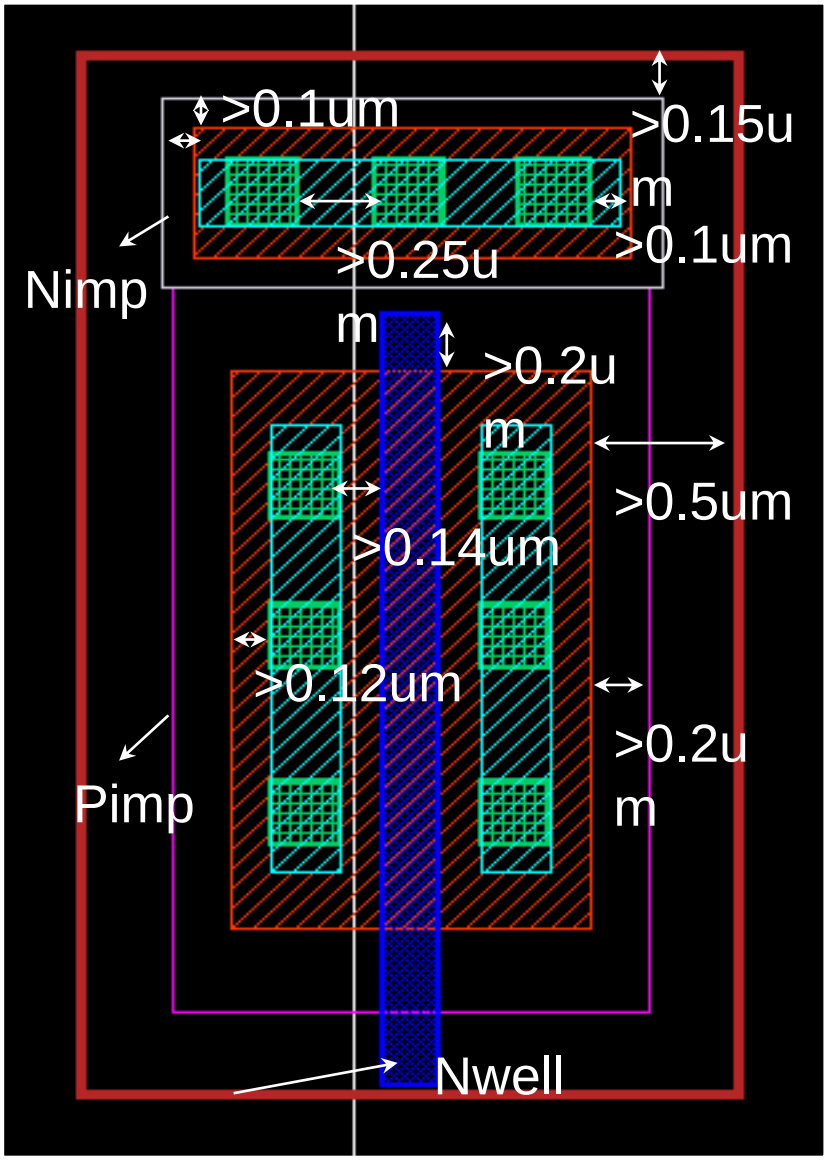


PMOS

1. Pimp and Active >0.2um
2. Nimp and Active >0.1um
3. Nwell and Nimp >0.15um
4. Nwell and Active >0.5um



PMOS Symbol

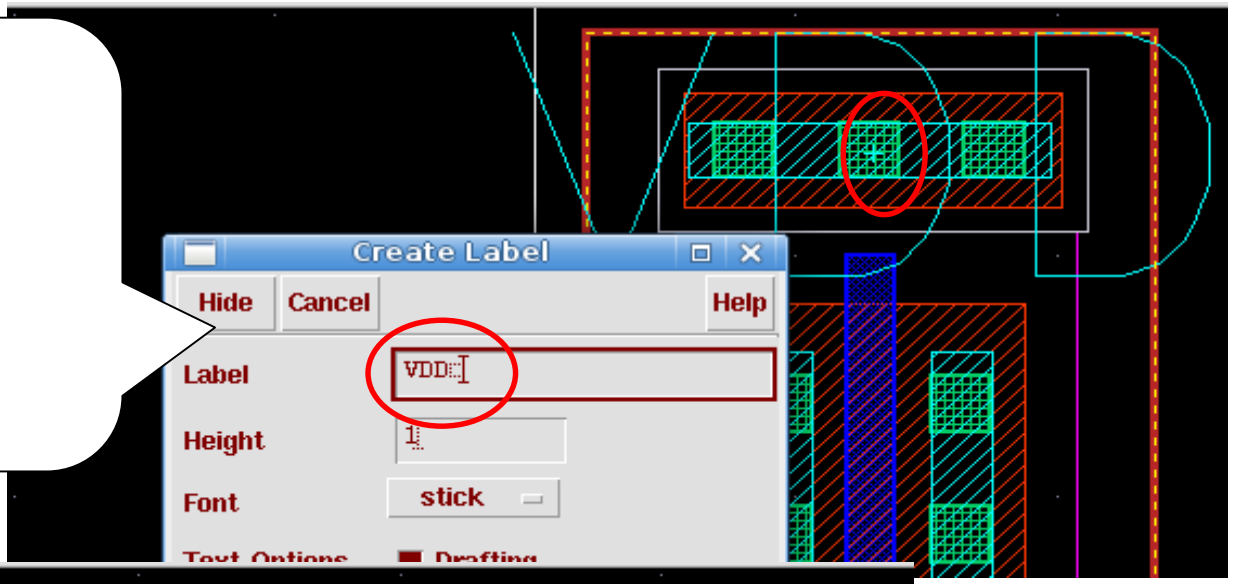


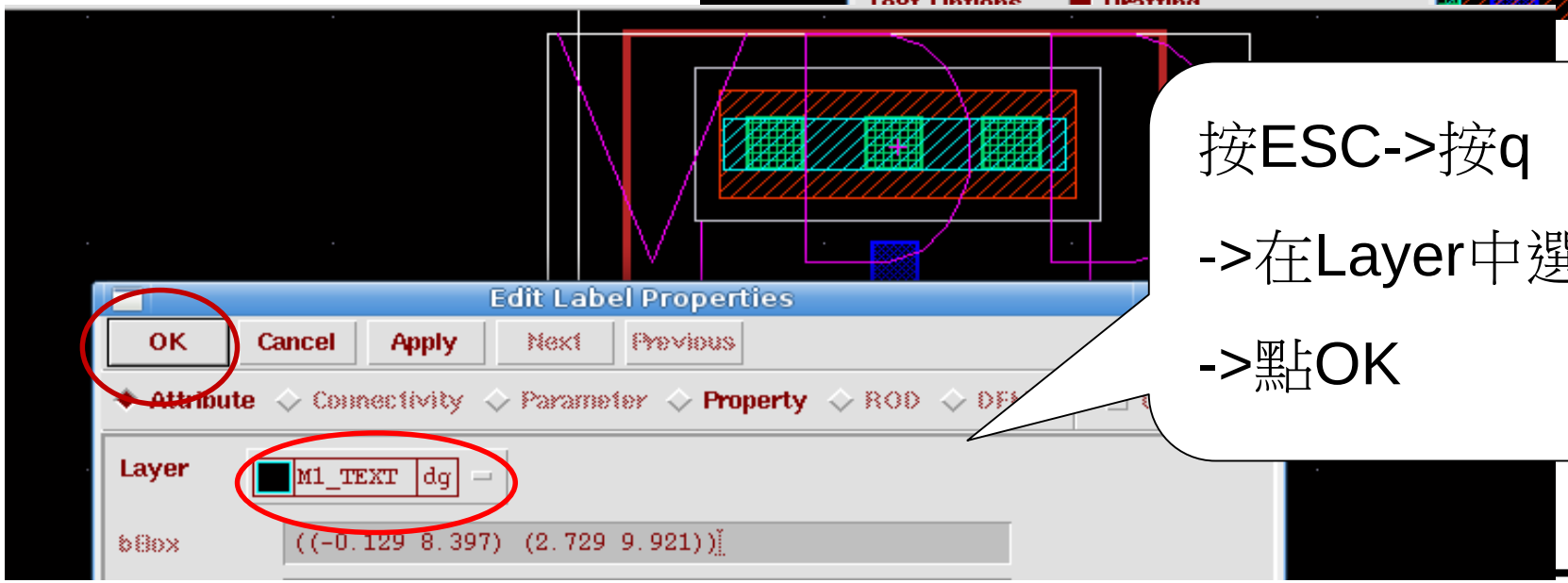
Label

按快速鍵L

->在Label中填上欲標之名

->將“+”放在所需之材質上



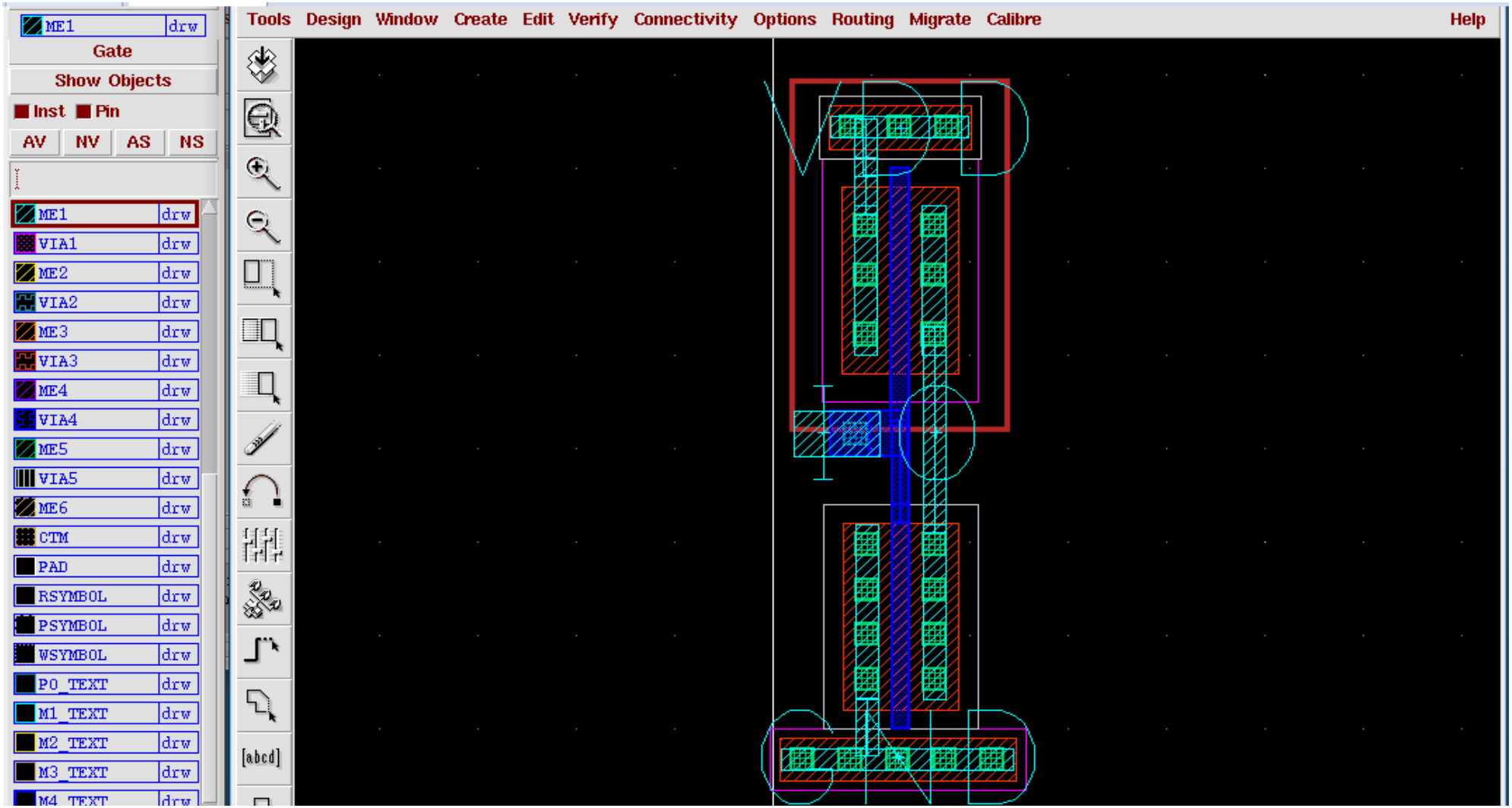


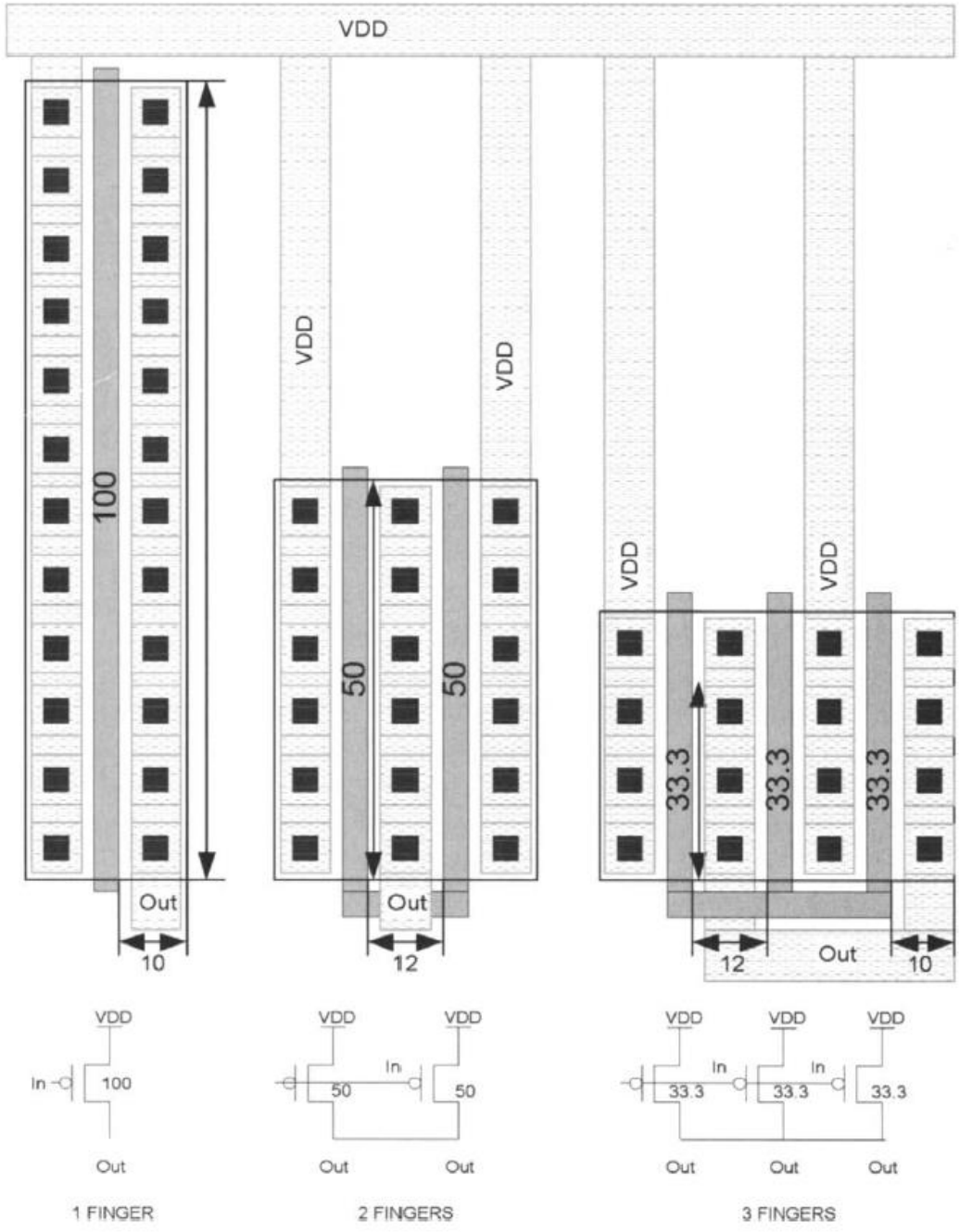
按ESC->按q

->在Layer中選M1_text

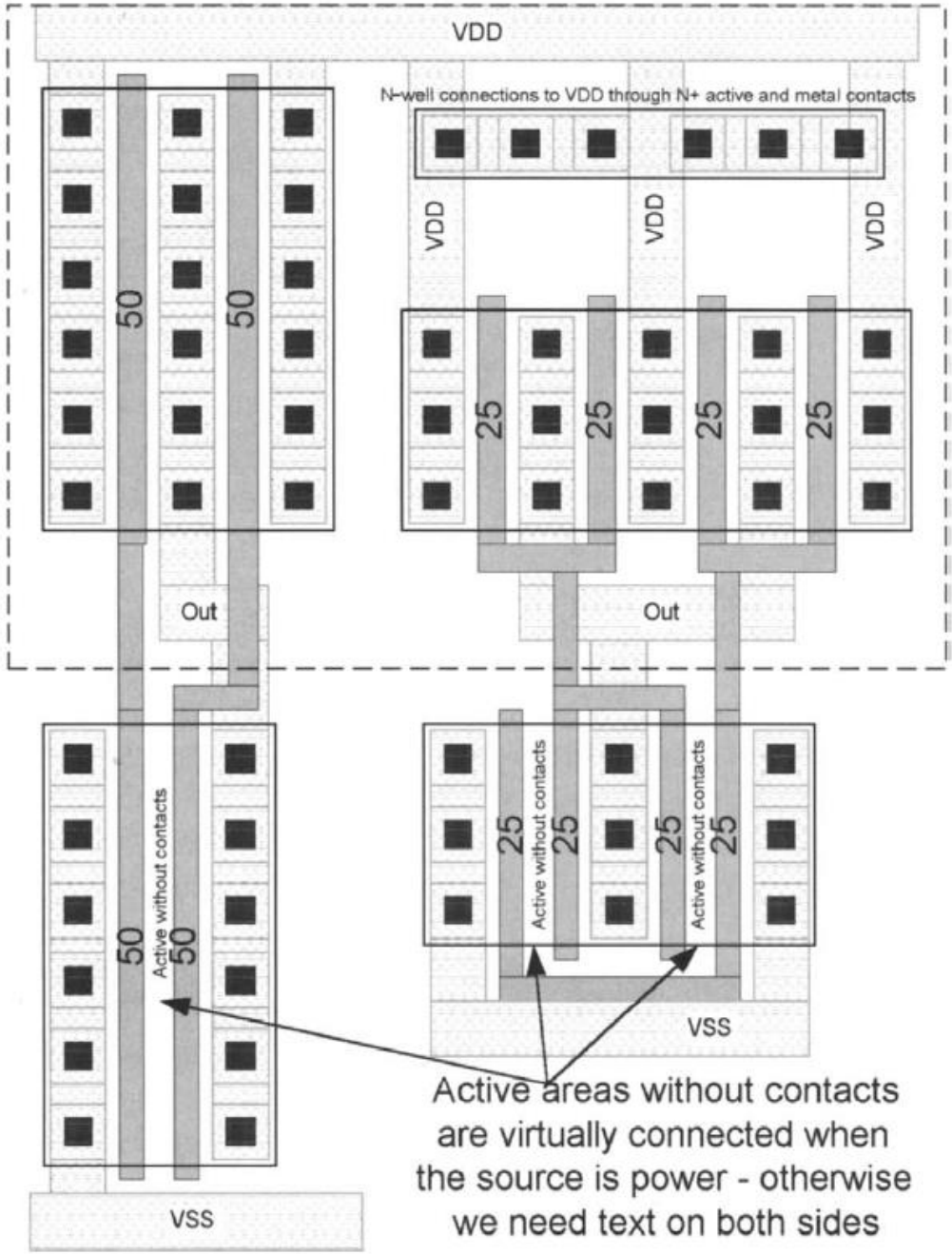
->點OK

Layout of inverter

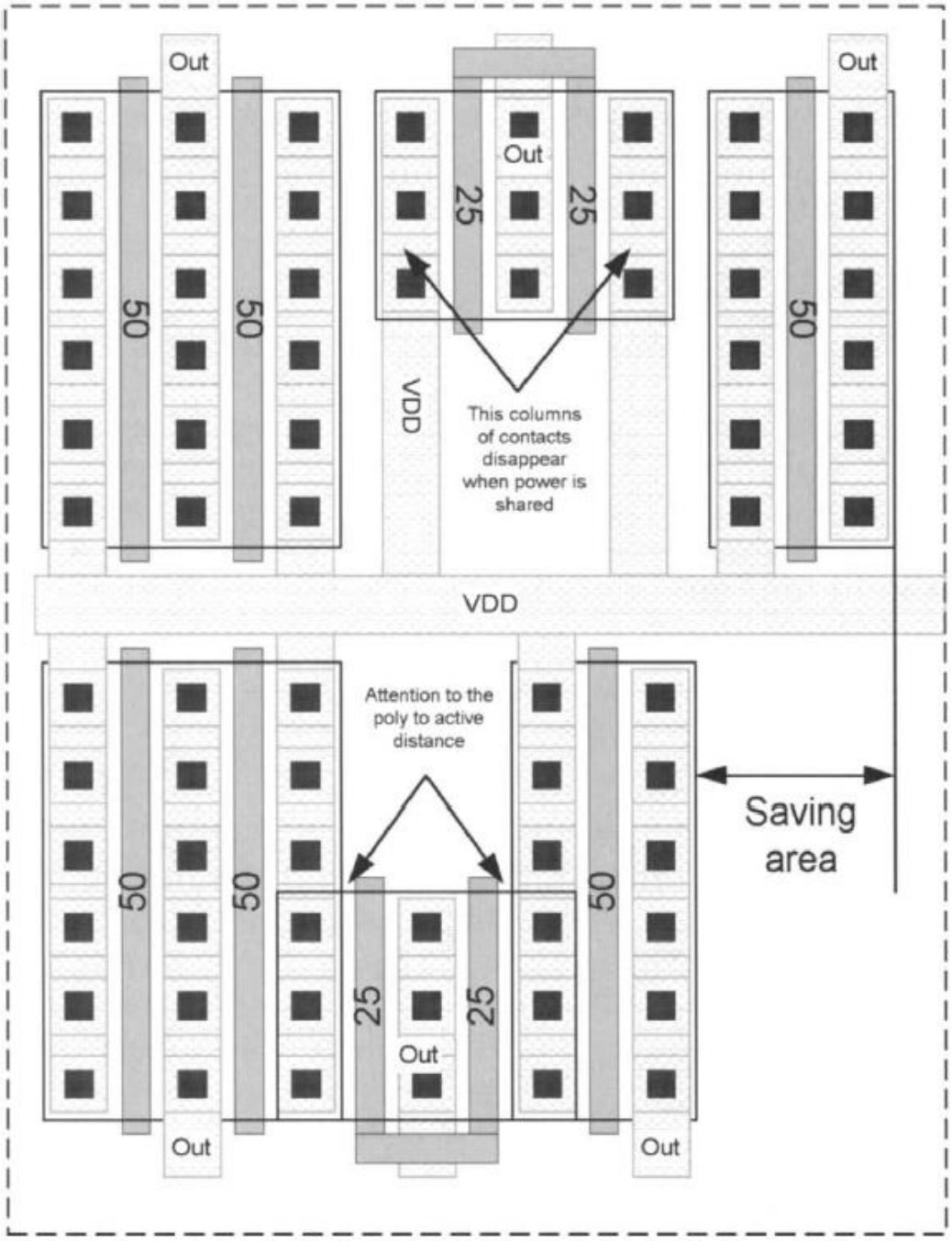




Transistor layout example

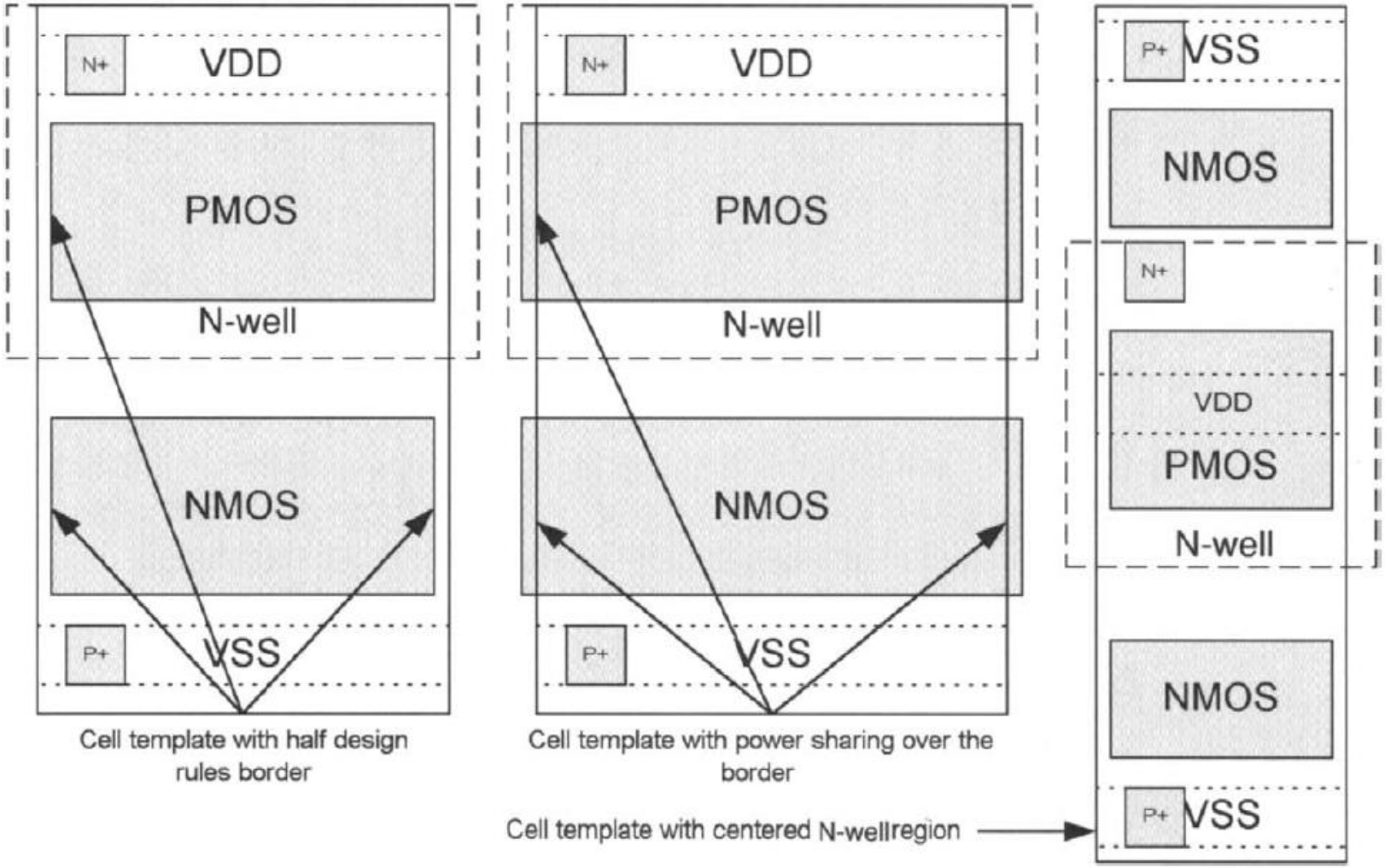


Sharing Source and Drain

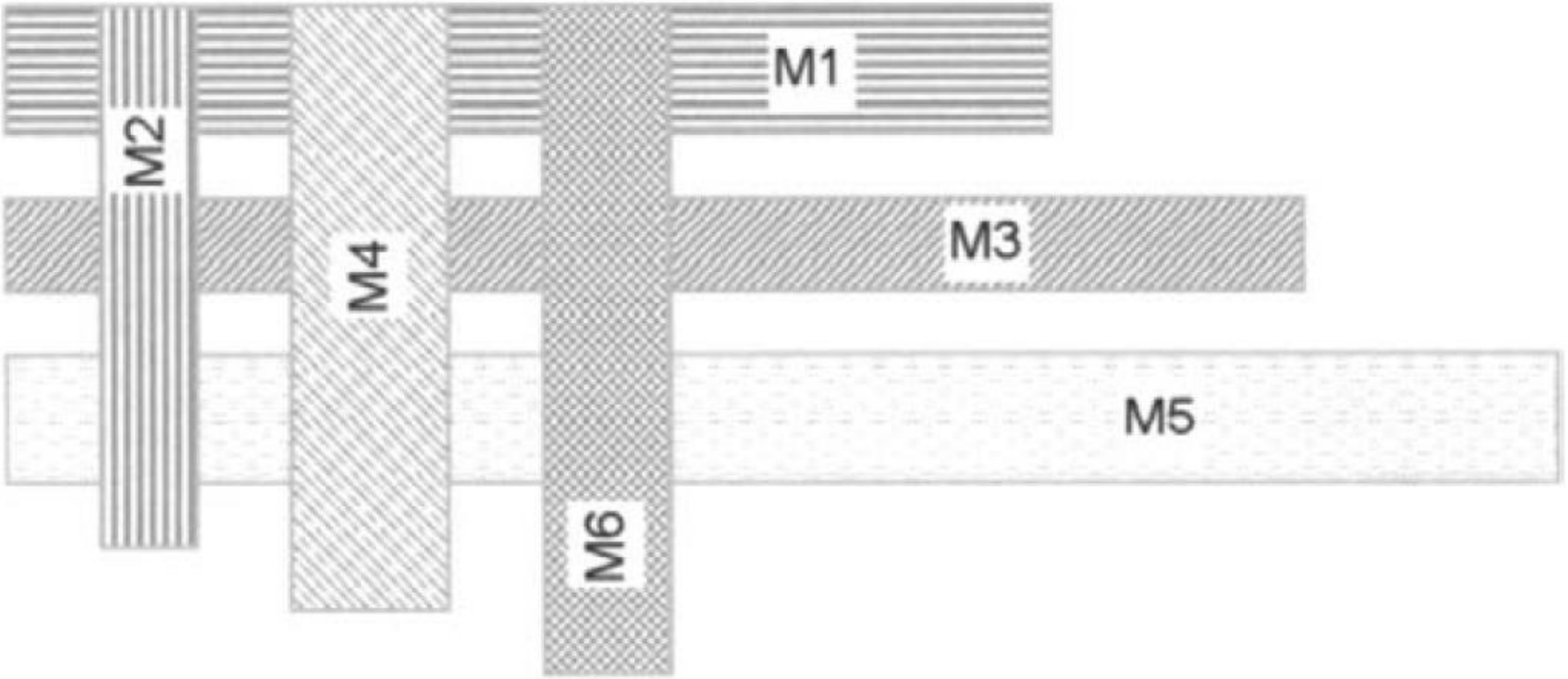


Power Sharing

Power and GND



Routing direction



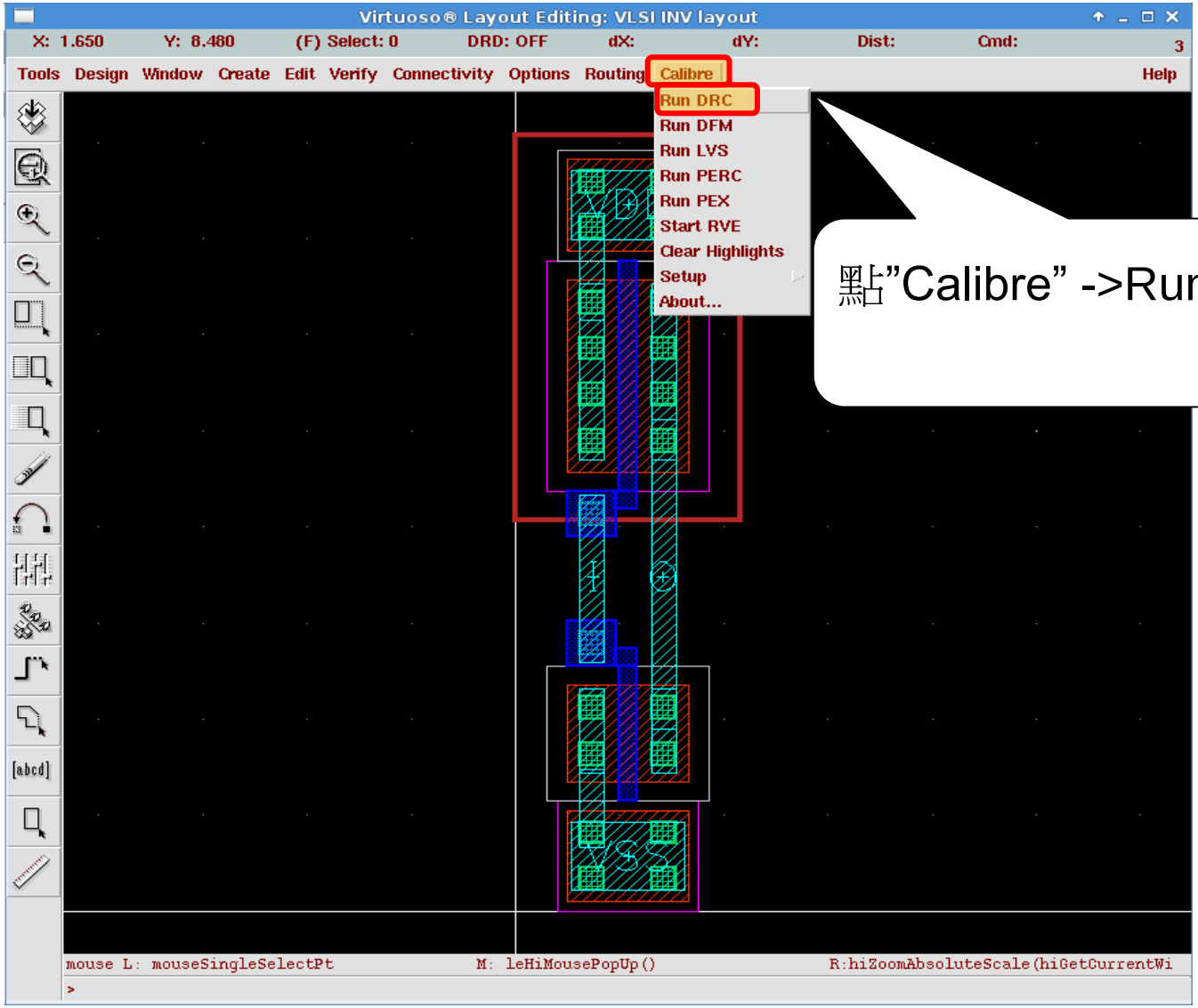
DRC、 LVS 、 PEX

- 畫完IC layout 需要檢查是否符合製程規格和電路匹配
  - 製成規格檢查: **執行Design Rule Check (DRC)**
  - 電路匹配: **執行Layout Versus Schematic (LVS)**

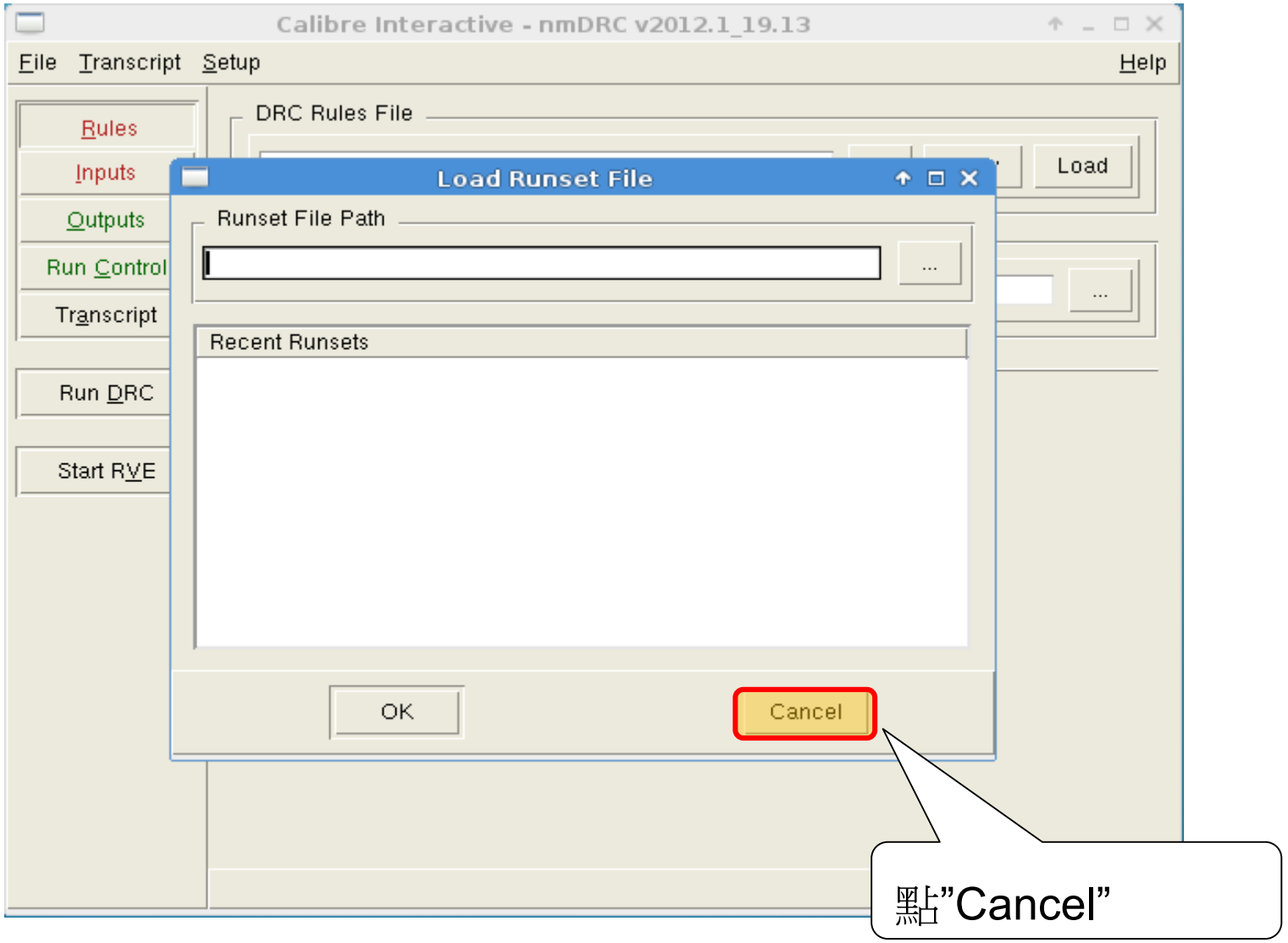
- 如果都符合DRC 和 LVS，可以把電容效應加入電路
  - 電路中有寄生電容效應稱為Post-simulation (沒有稱為pre-simulation)
  - 產生寄生電容: **執行Parasitic Extraction (PEX)**

執行DRC

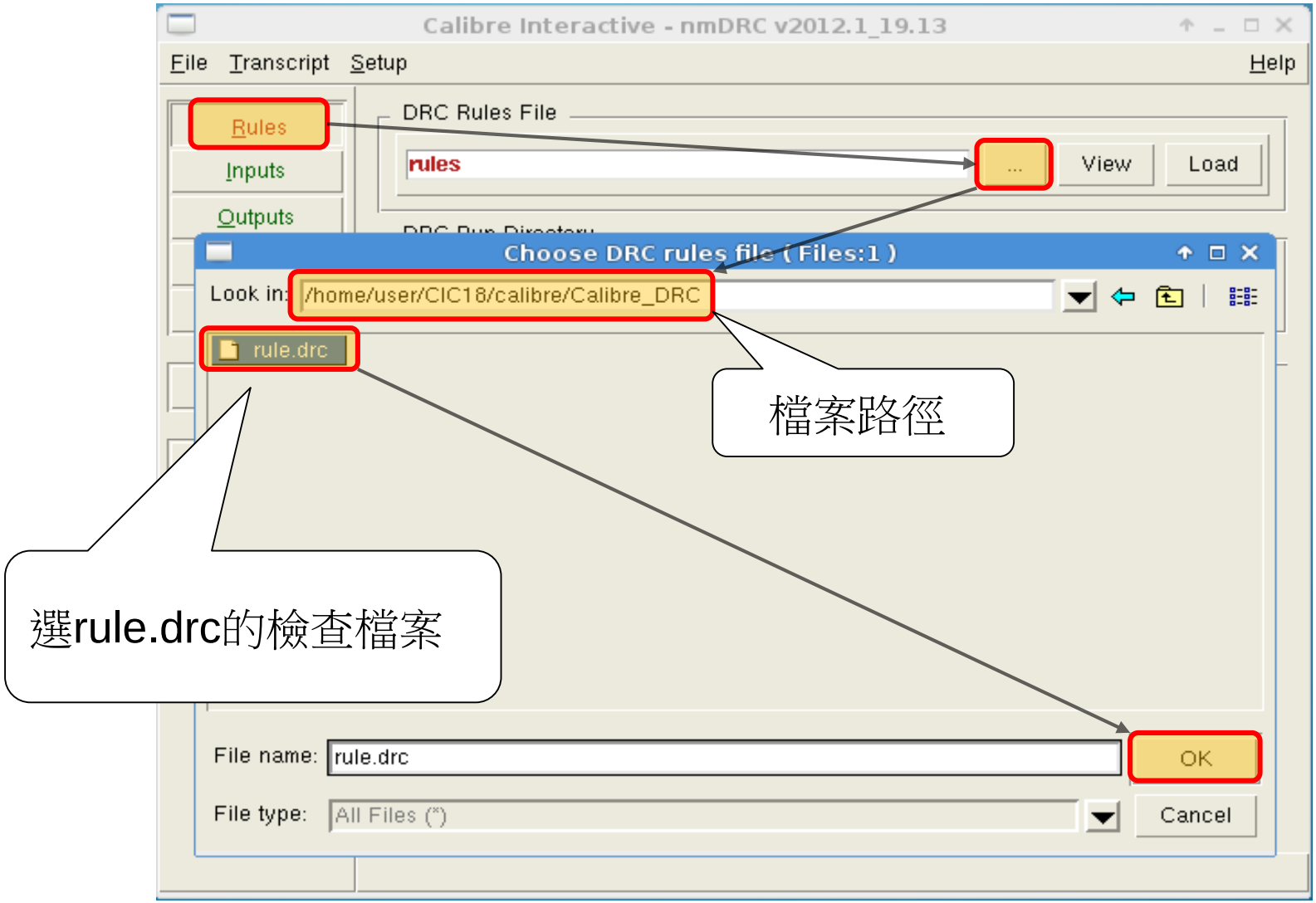
呼叫DRC


Virtuoso® Layout Editing: VLSI INV layout
X: 1.650
Y: 8.480
(F) Select: 0
DRD: OFF
dX:
dY:
Dist:
Cmd:
Tools
Design
Window
Create
Edit
Verify
Connectivity
Options
Routing
Calibre
Help
Run DRC
Run DFM
Run LVS
Run PERC
Run PEX
Start RVE
Clear Highlights
Setup
About...
點”Calibre” ->Run DRC
mouse L: mouseSingleSelectPt
M: leHiMousePopUp()
R:hiZoomAbsoluteScale(hiGetCurrentWi

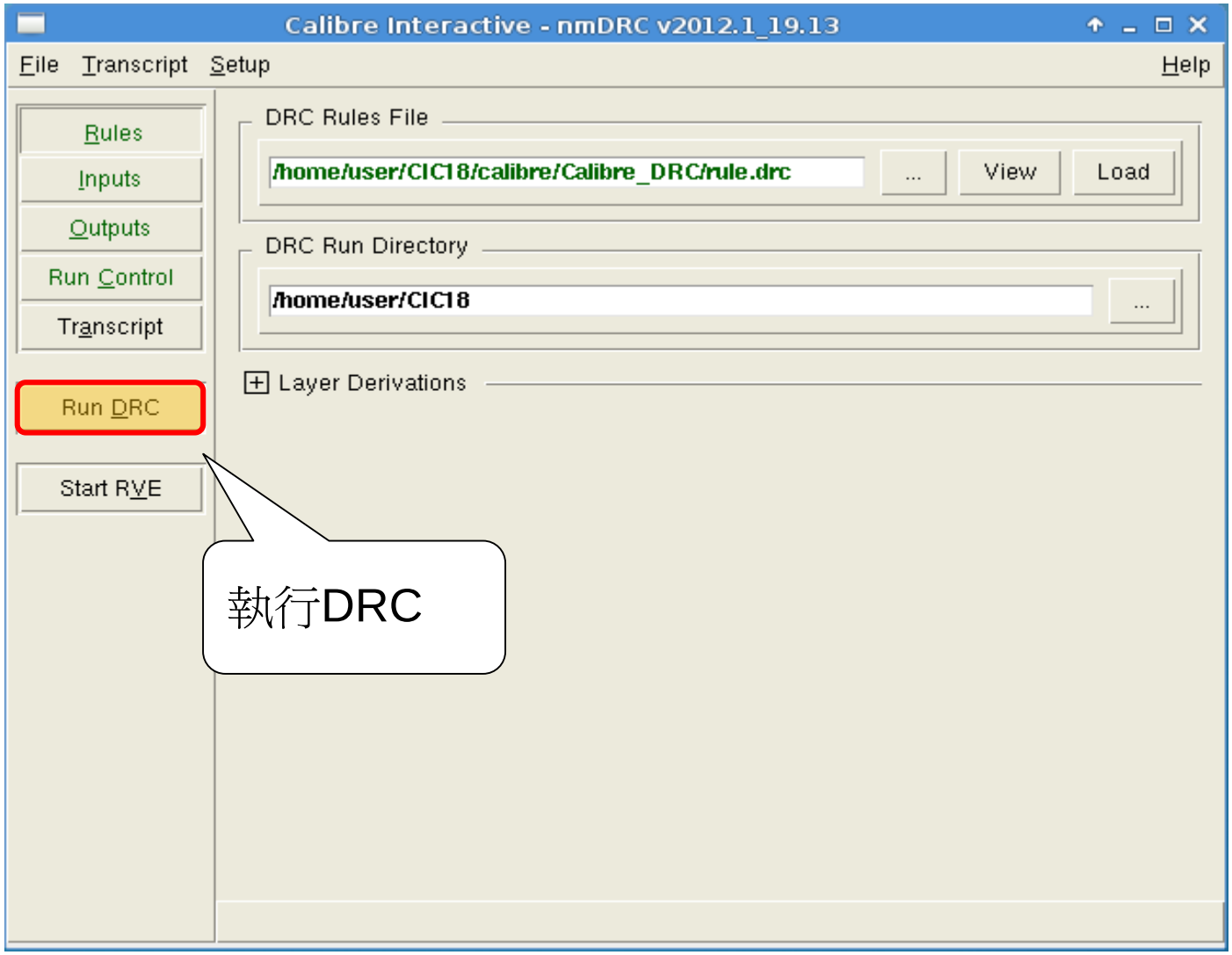
Design Rule Check (DRC)



Design Rule Check (DRC)

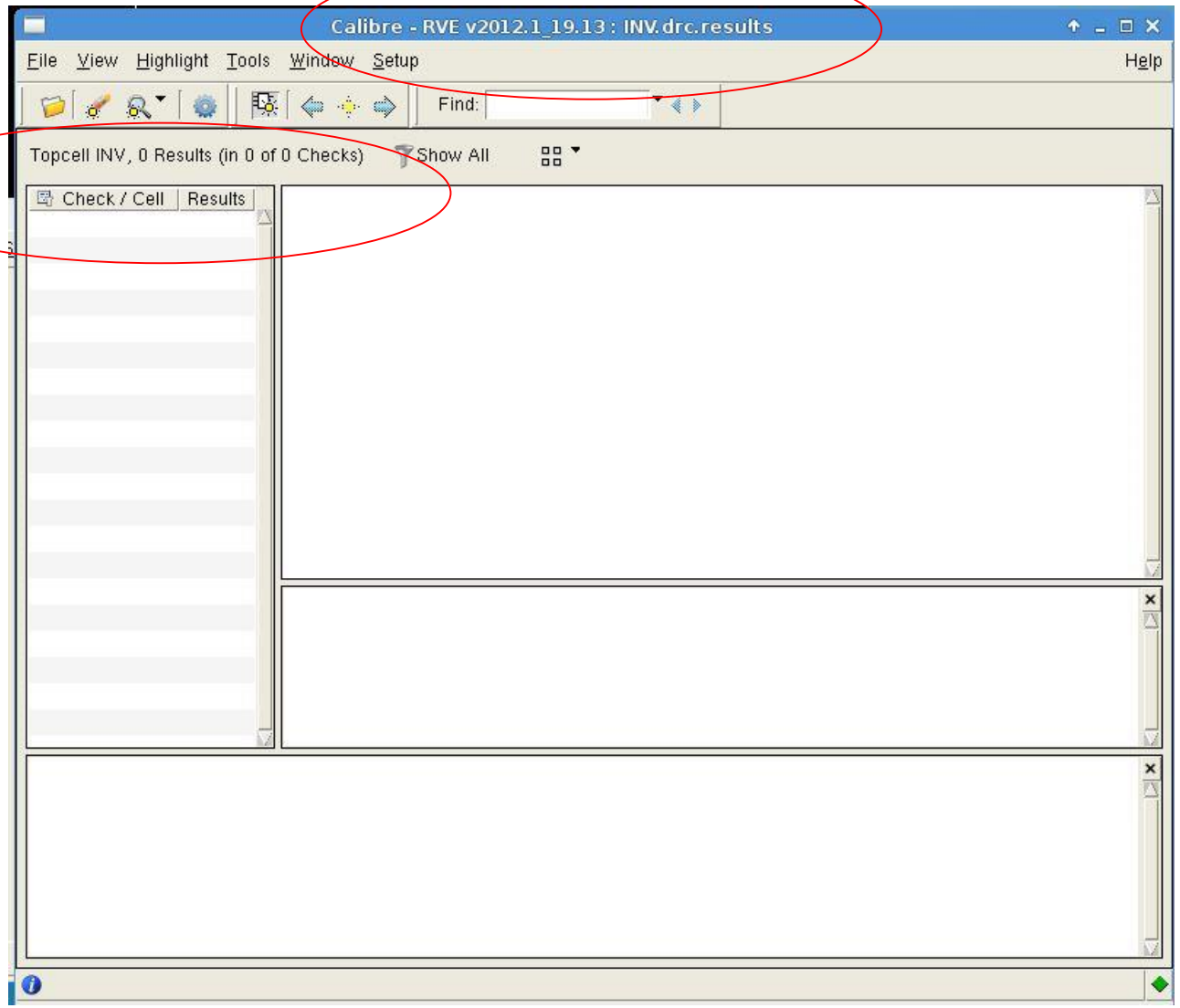


Design Rule Check (DRC)



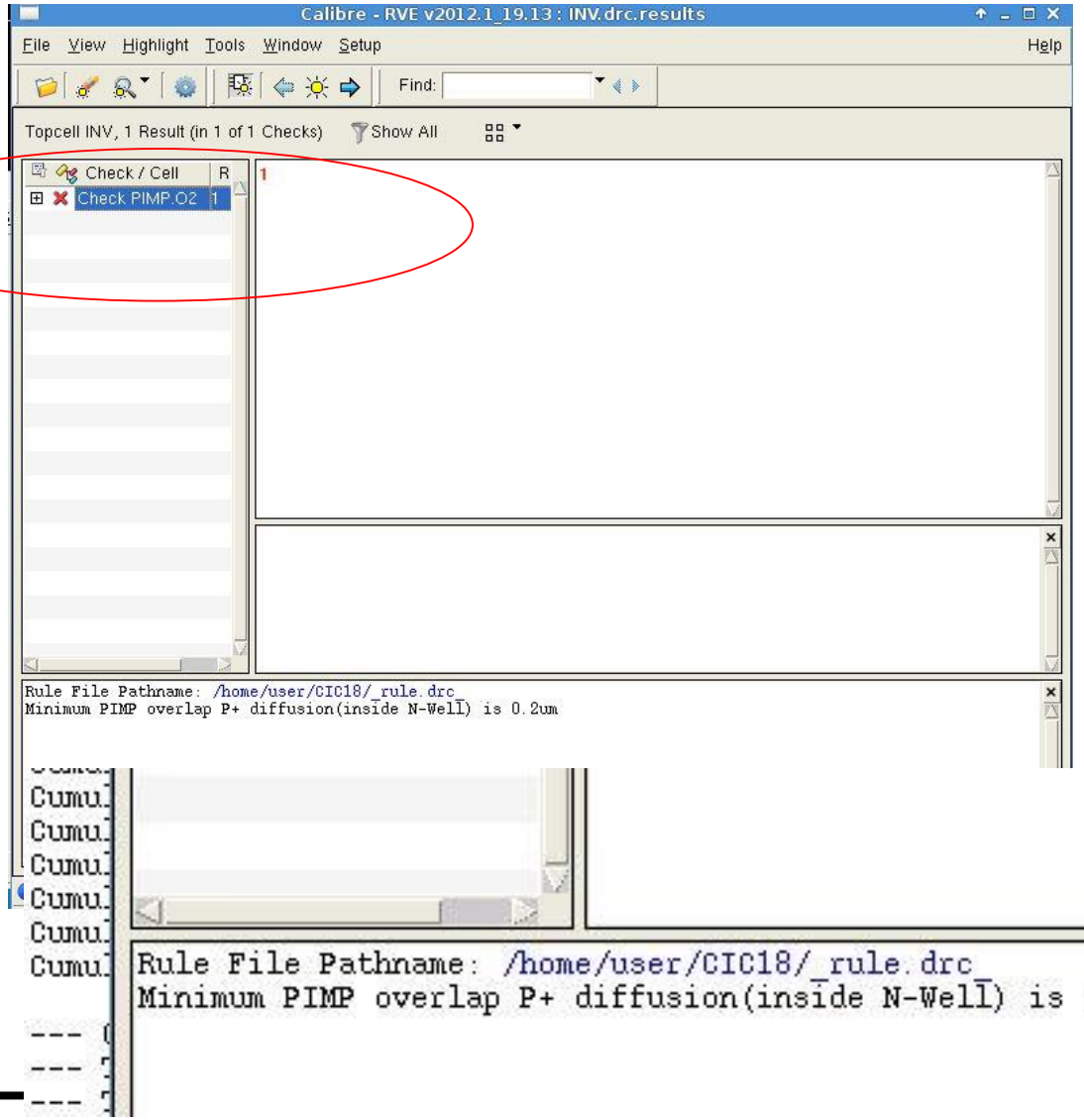
Design Rule Check (DRC) Result - I

檢查是否有錯誤?
無任何錯誤顯示(空的)

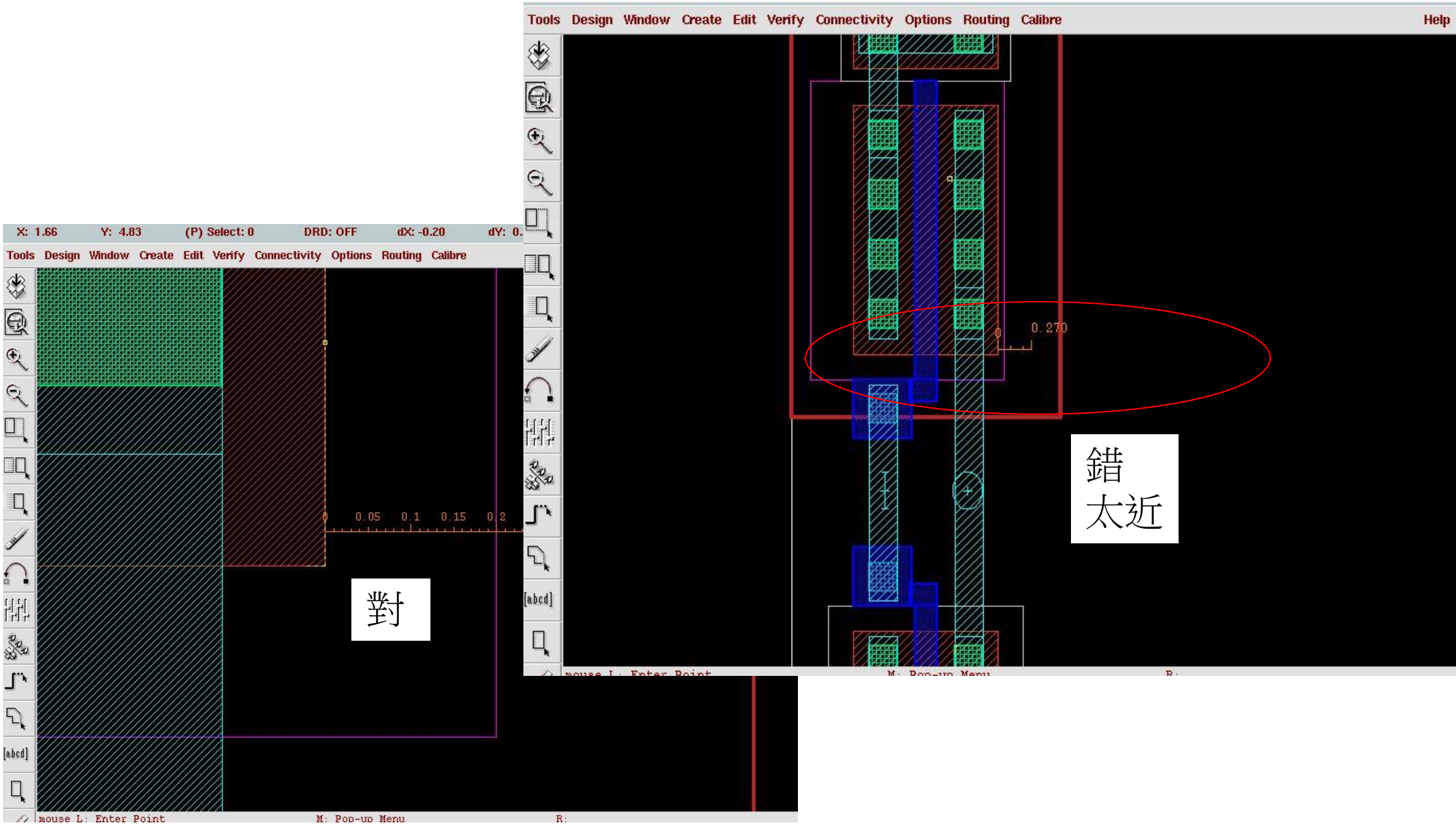


Design Rule Check (DRC) Result - II

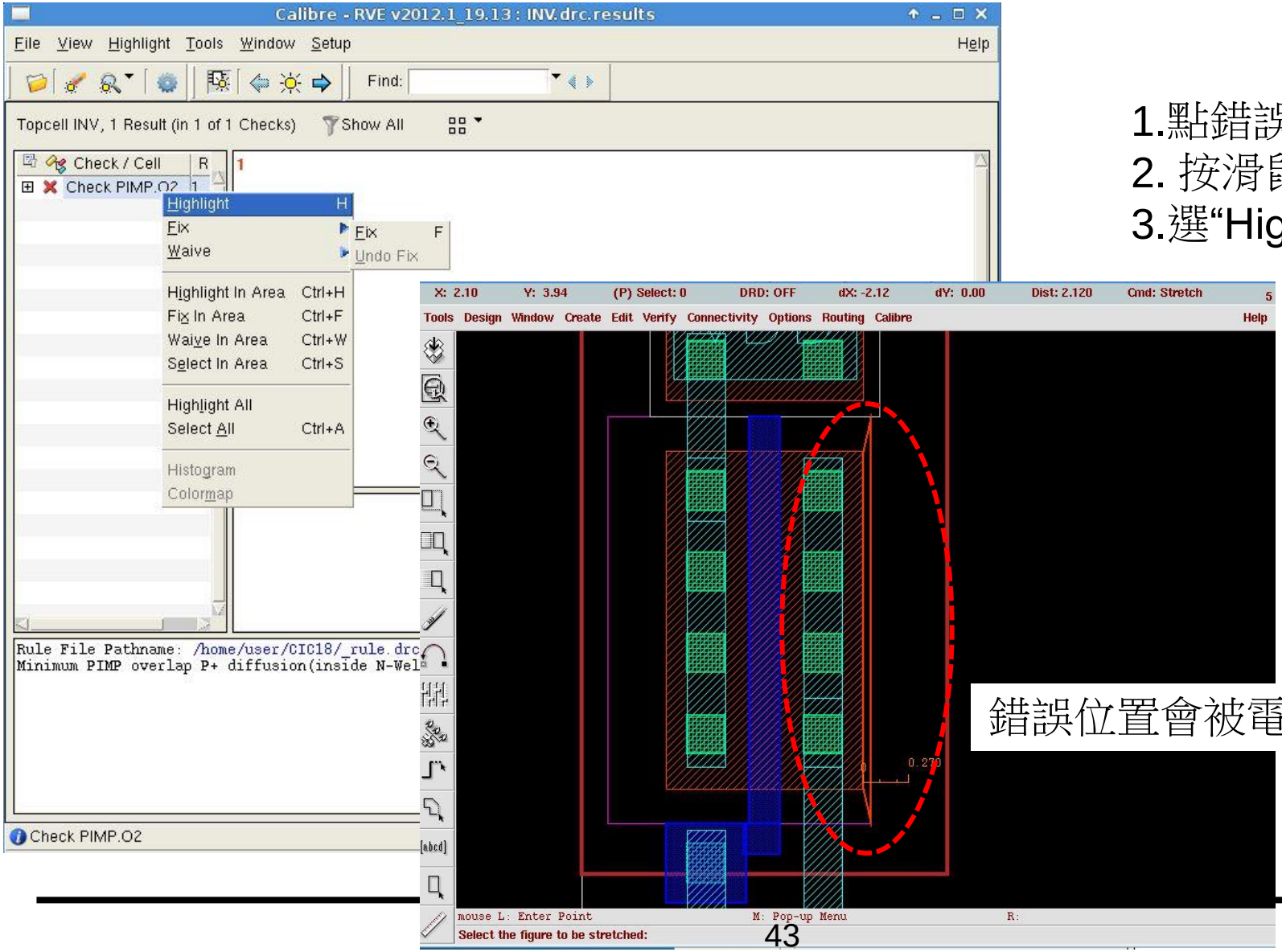
有錯誤產生
P+ imp 和 DIFF距離太小



Design Rule Check (DRC) Result - III



DRC 除錯方法

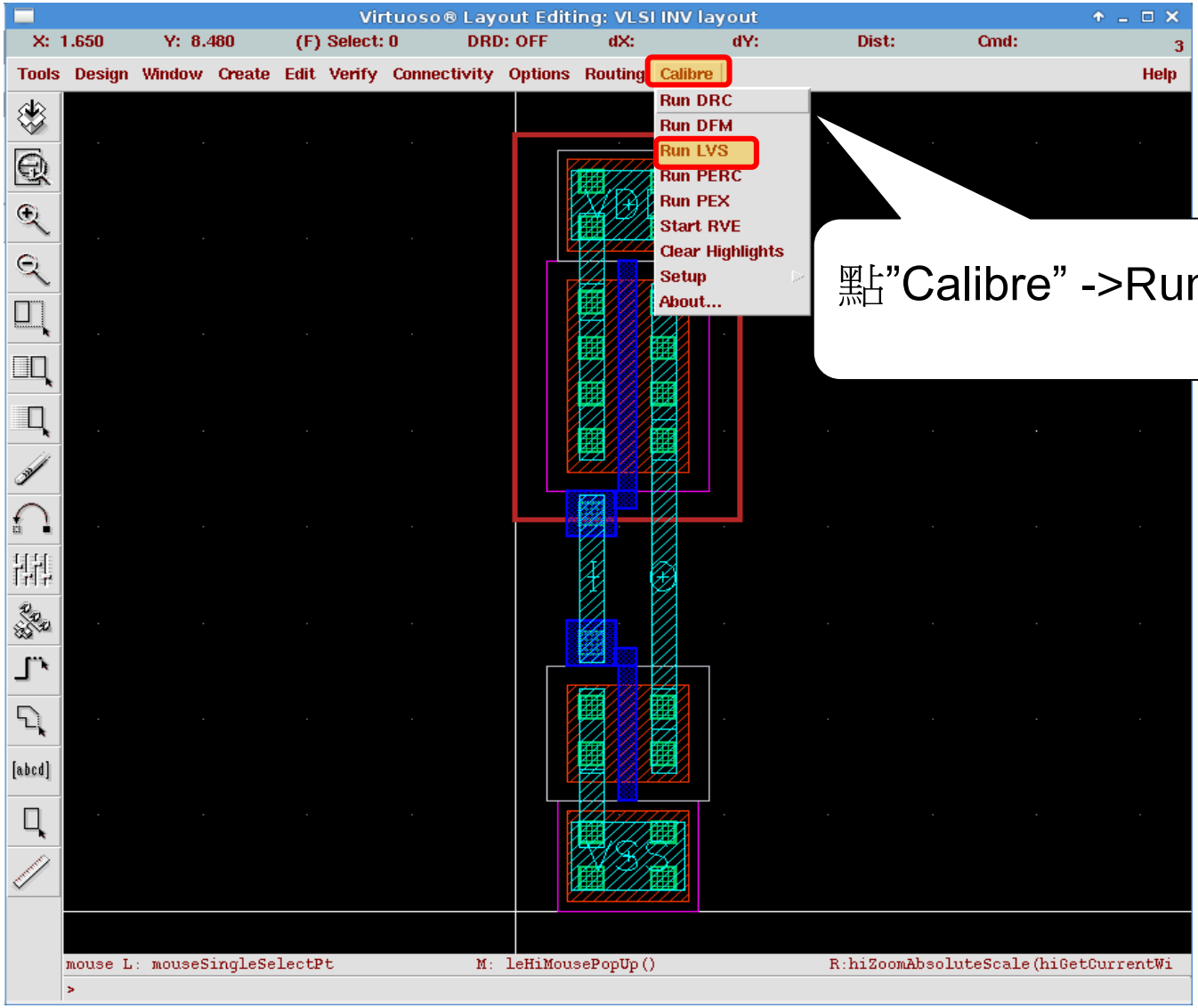


1.點錯誤地方
2. 按滑鼠右鍵
3.選“Hightlight”

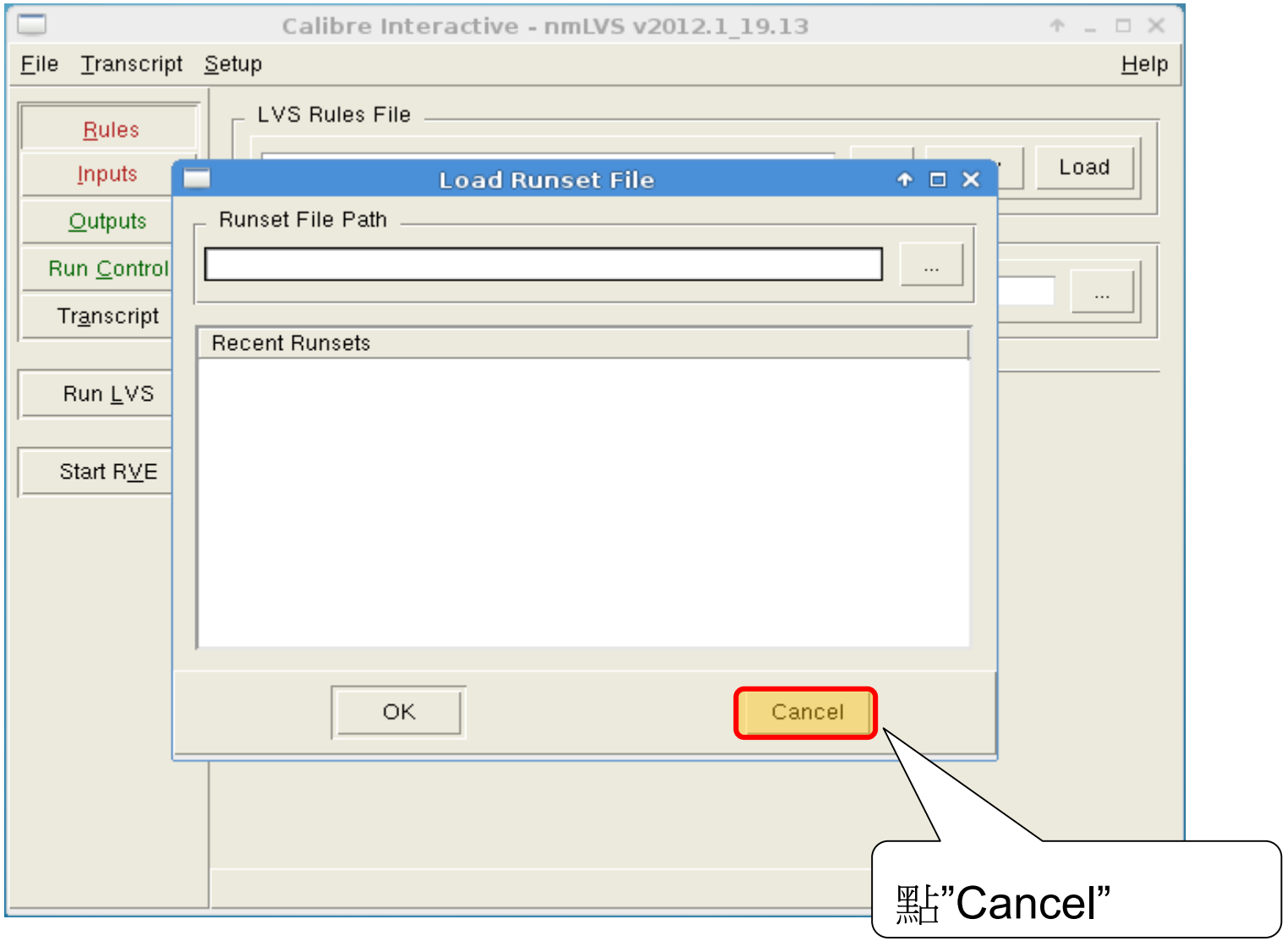
錯誤位置會被電腦指出

執行LVS

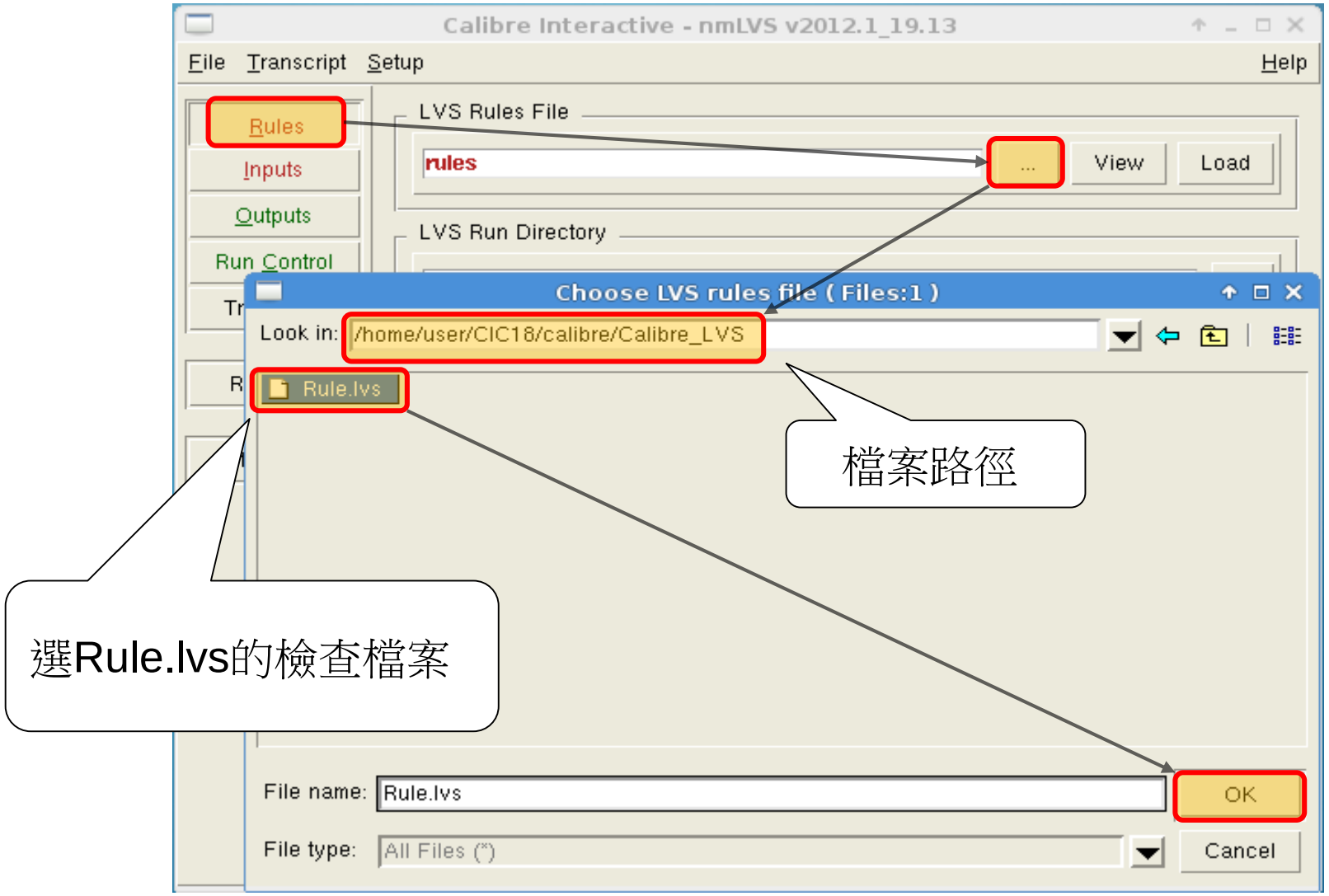
Layout vs. Schematic (LVS)



Layout vs. Schematic (LVS)

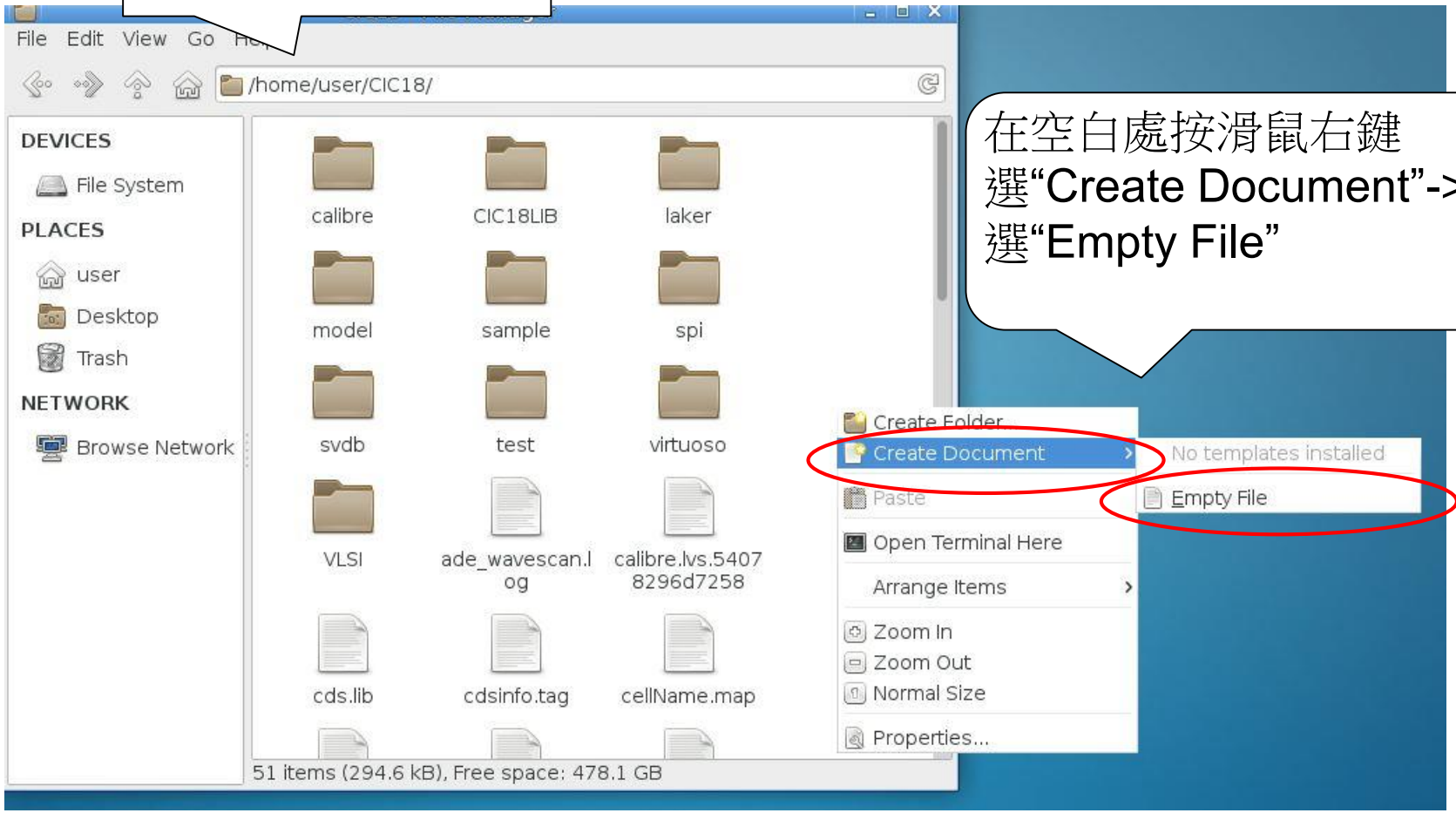


Layout vs. Schematic (LVS)



產生HSPICE電路檔案

點”Home”->點“CIC18”資料夾

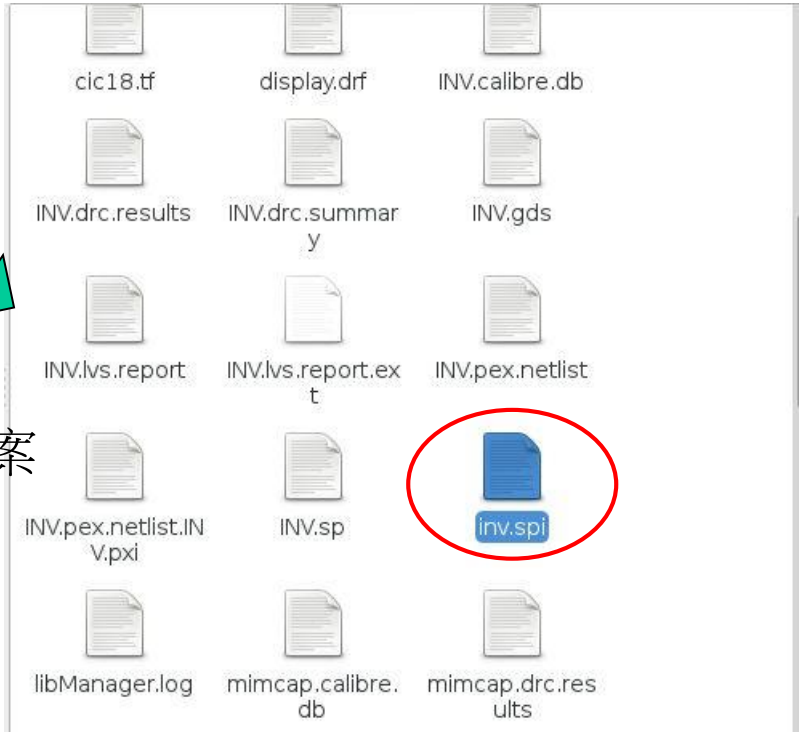


在空白處按滑鼠右鍵
選“Create Document”->
選“Empty File”

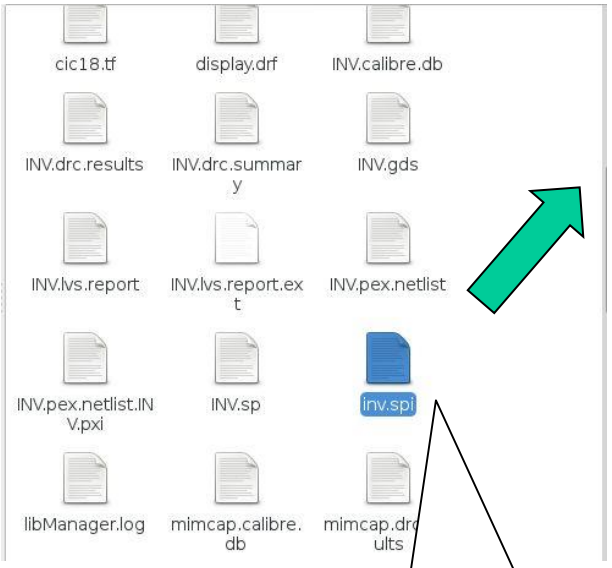
取名文字檔案和產生檔案

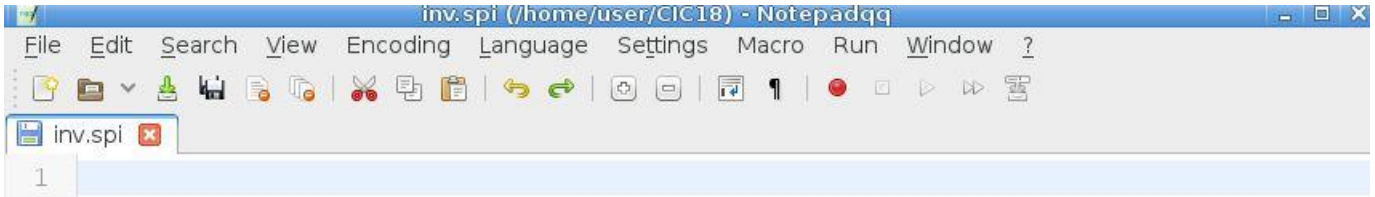
鍵入名

產生檔案



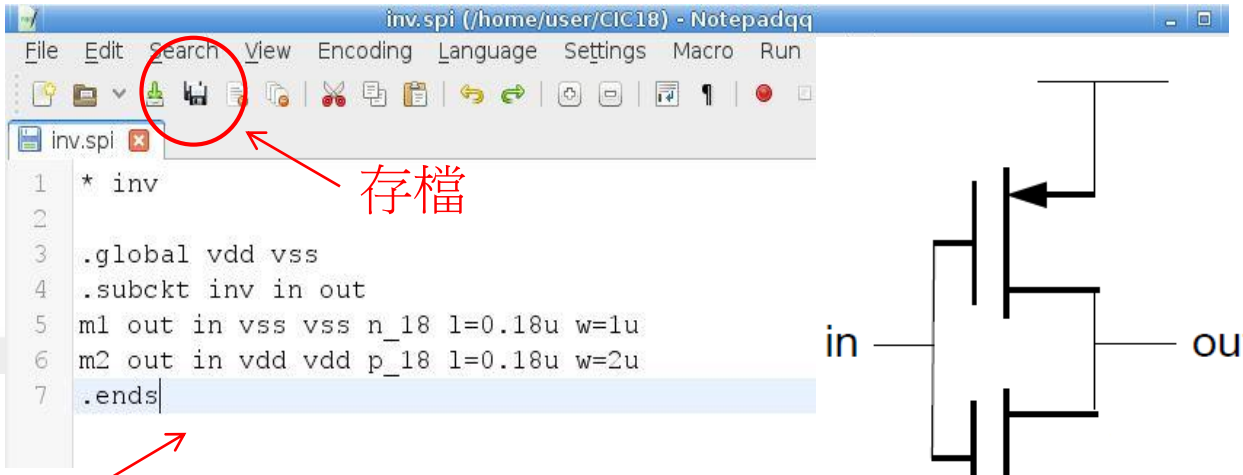
需要HSPICE電路檔案





1.需使用”subckt”指令

2.只需要鍵入電路圖(電晶體、 電阻、電容之間的連線)



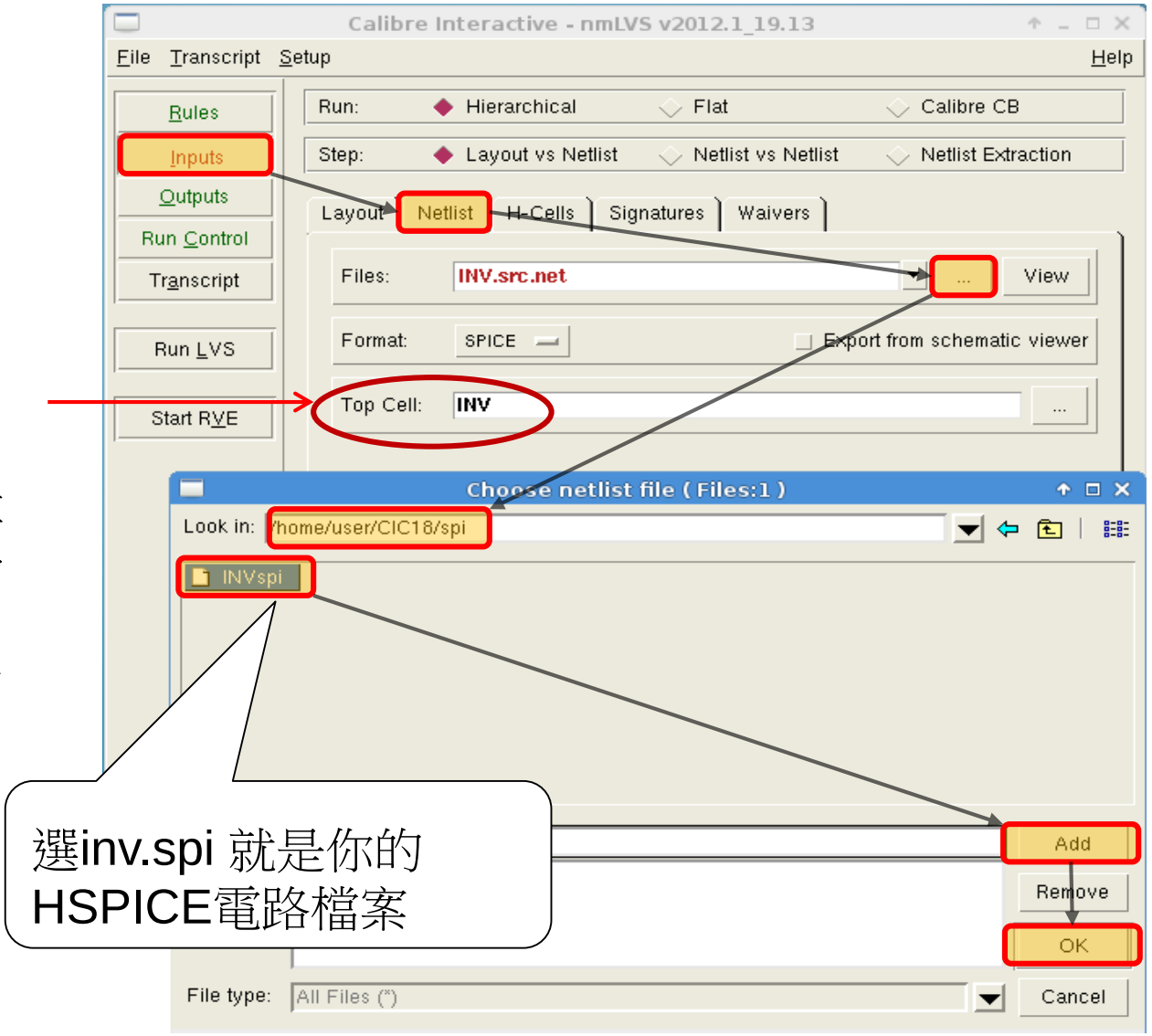
存檔

點選“檔案(inv.spi)

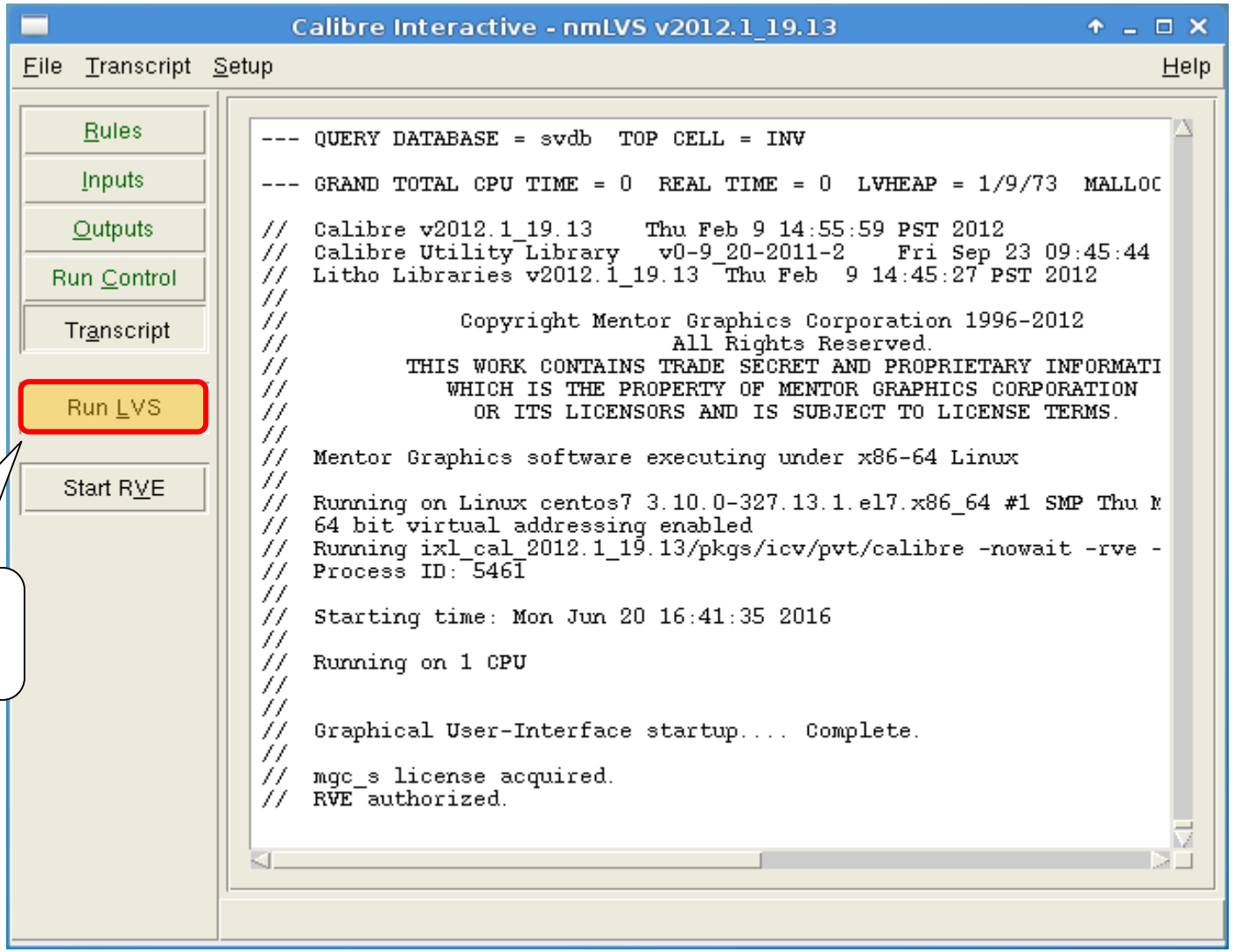

```
* inv
.global vdd vss
.SUBCKT inv in out
M1 out in  VSS VSS N_18 L=0.18u W=1u
M1 out in  VDD VDD P_18 L=0.18u W=2u
.ENDS
```

Layout vs. Schematic (LVS)

注意:
Top Cell
的名字要
和你寫的
subckt的
名字相同

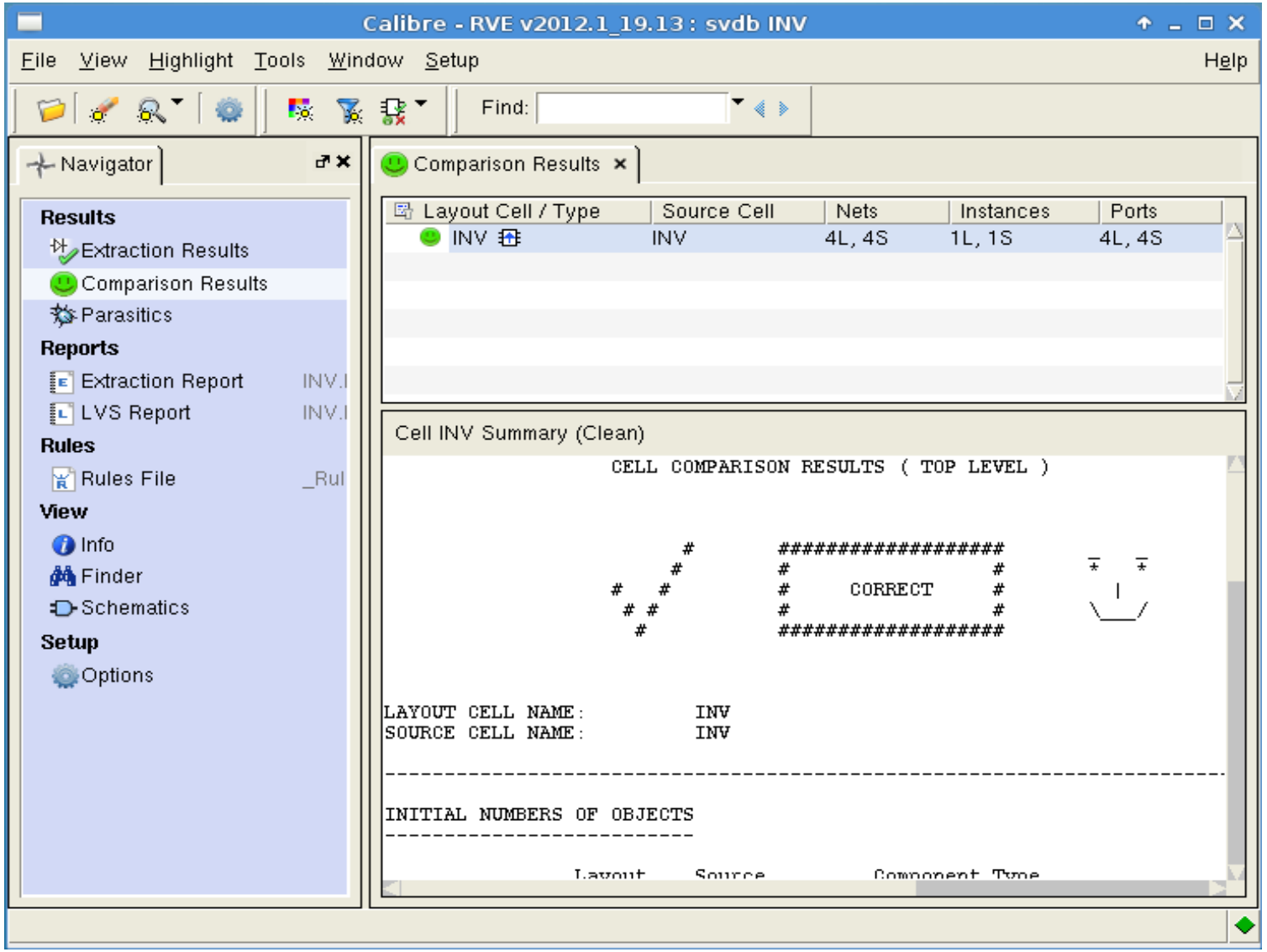


Layout vs. Schematic (LVS)

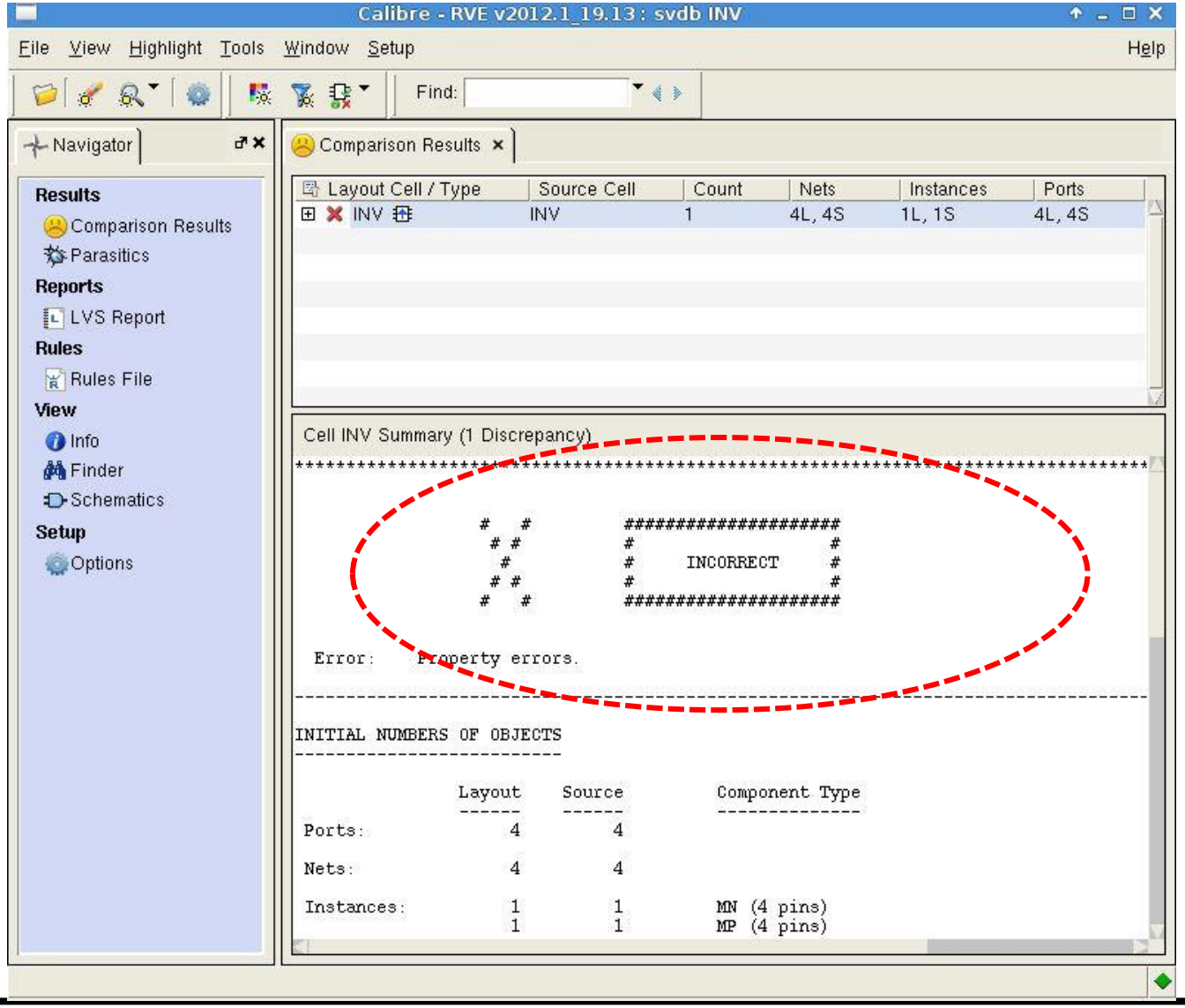


執行LVS

Layout vs. Schematic (LVS)-無錯誤

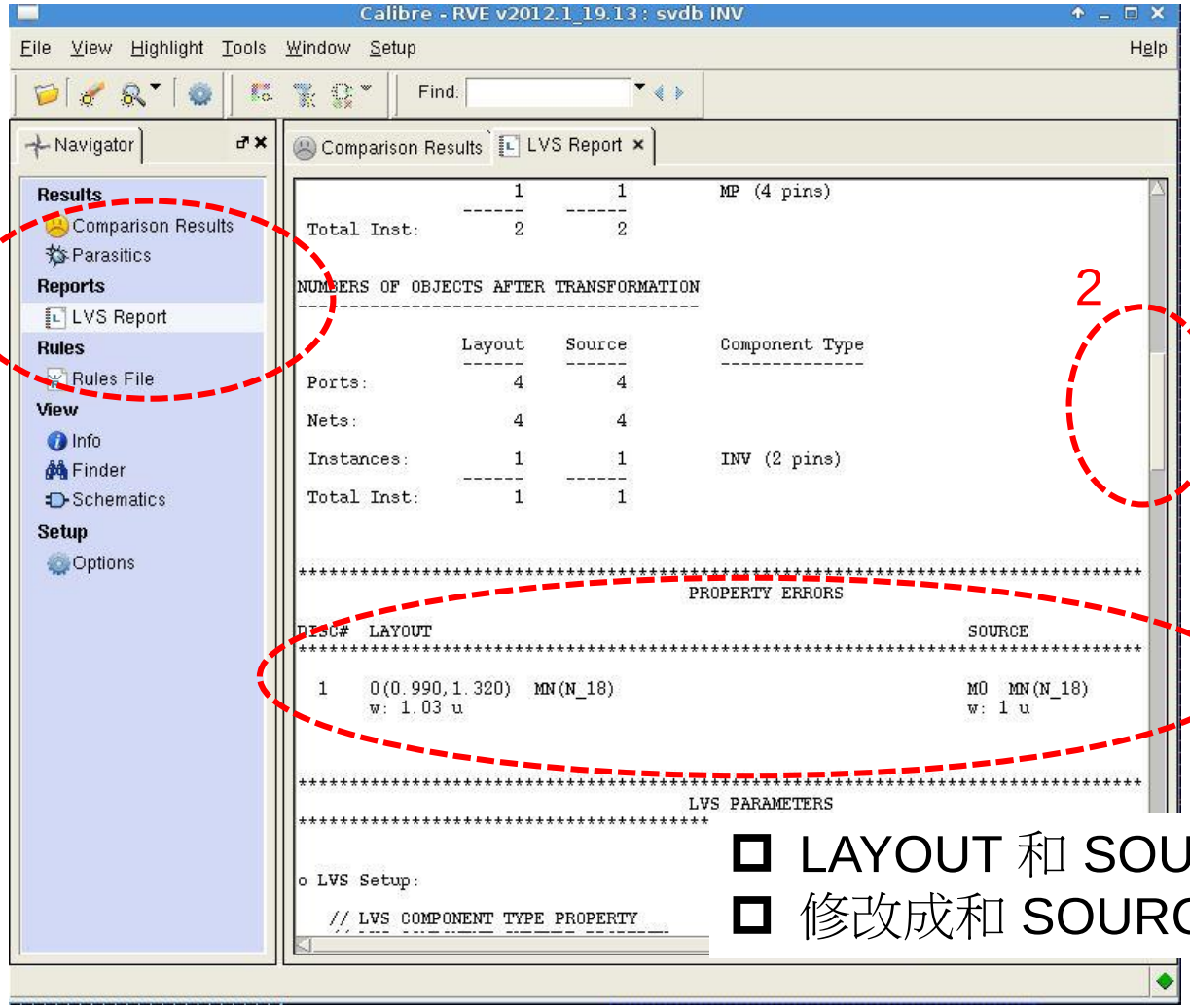


LVS-錯誤發生 -I



No good

哪裡錯??



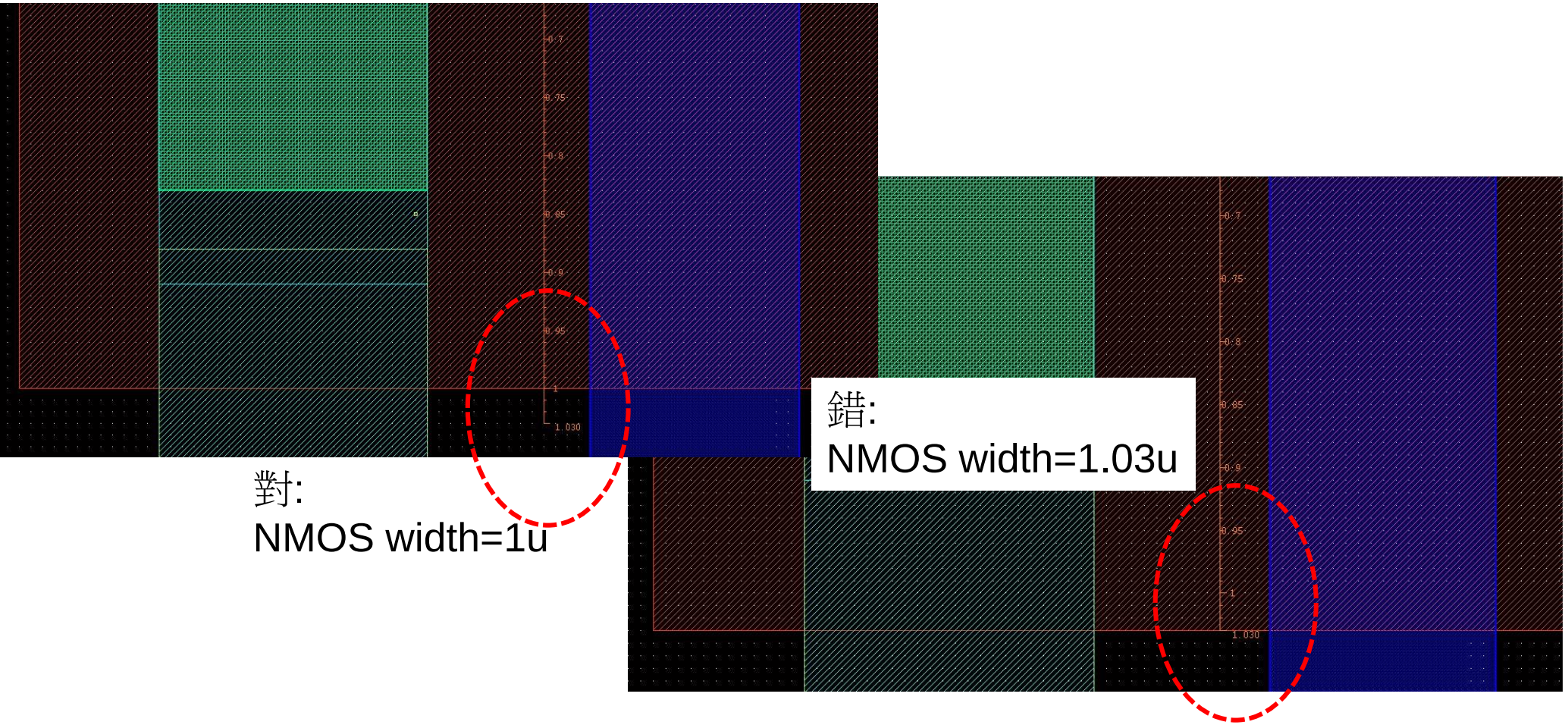
1.選 LVS Report
2. 移動旁邊柱狀體
3.到 PROPERTY ERRORS

- LAYOUT 和 SOURCE(HSPICE code)不同
- 修改成和 SOURCE(HSPICE code)相同

修改Layout

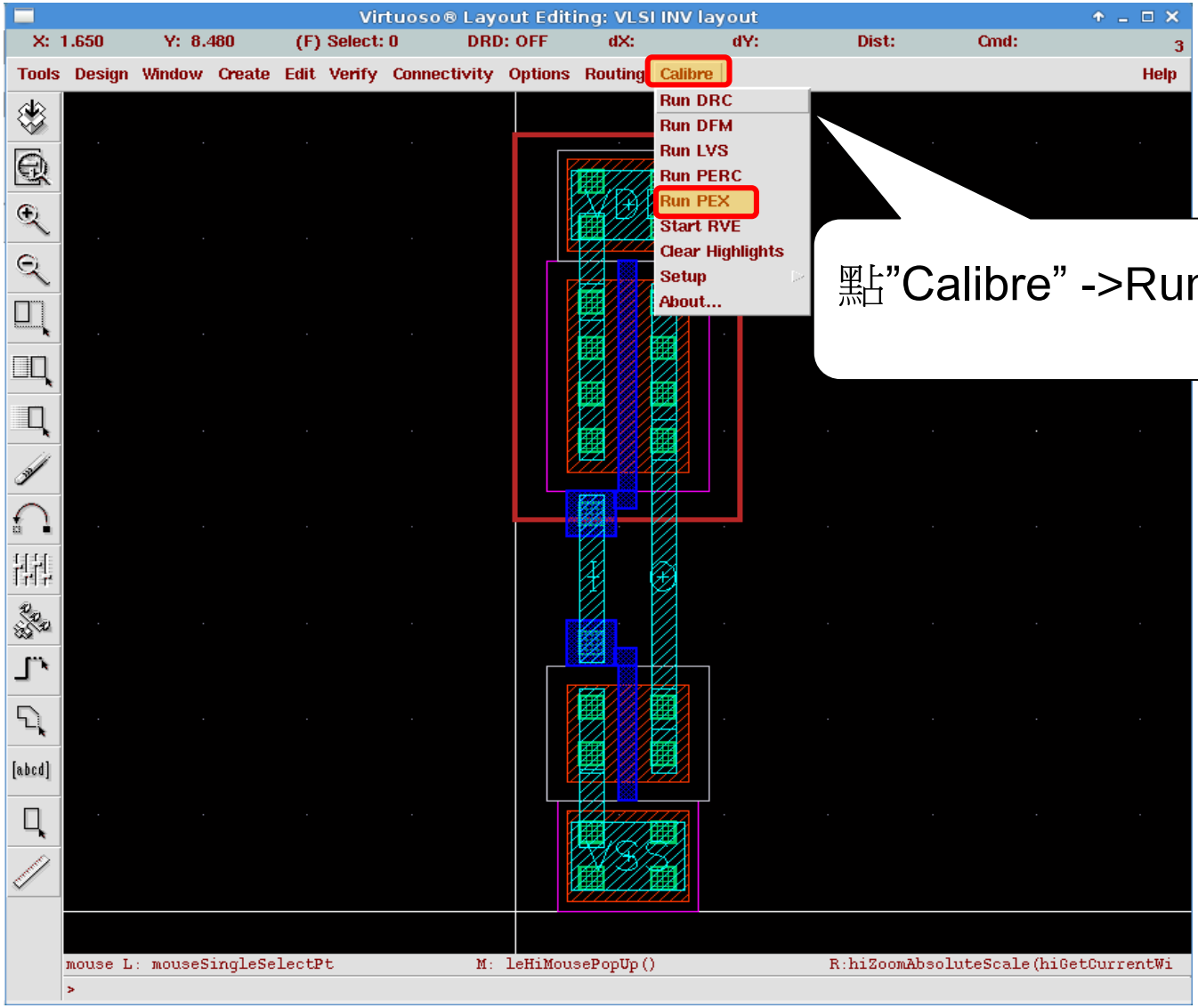
注意:

HSPICE code永遠是對的 ，當發生 LVS error，只能修改layout

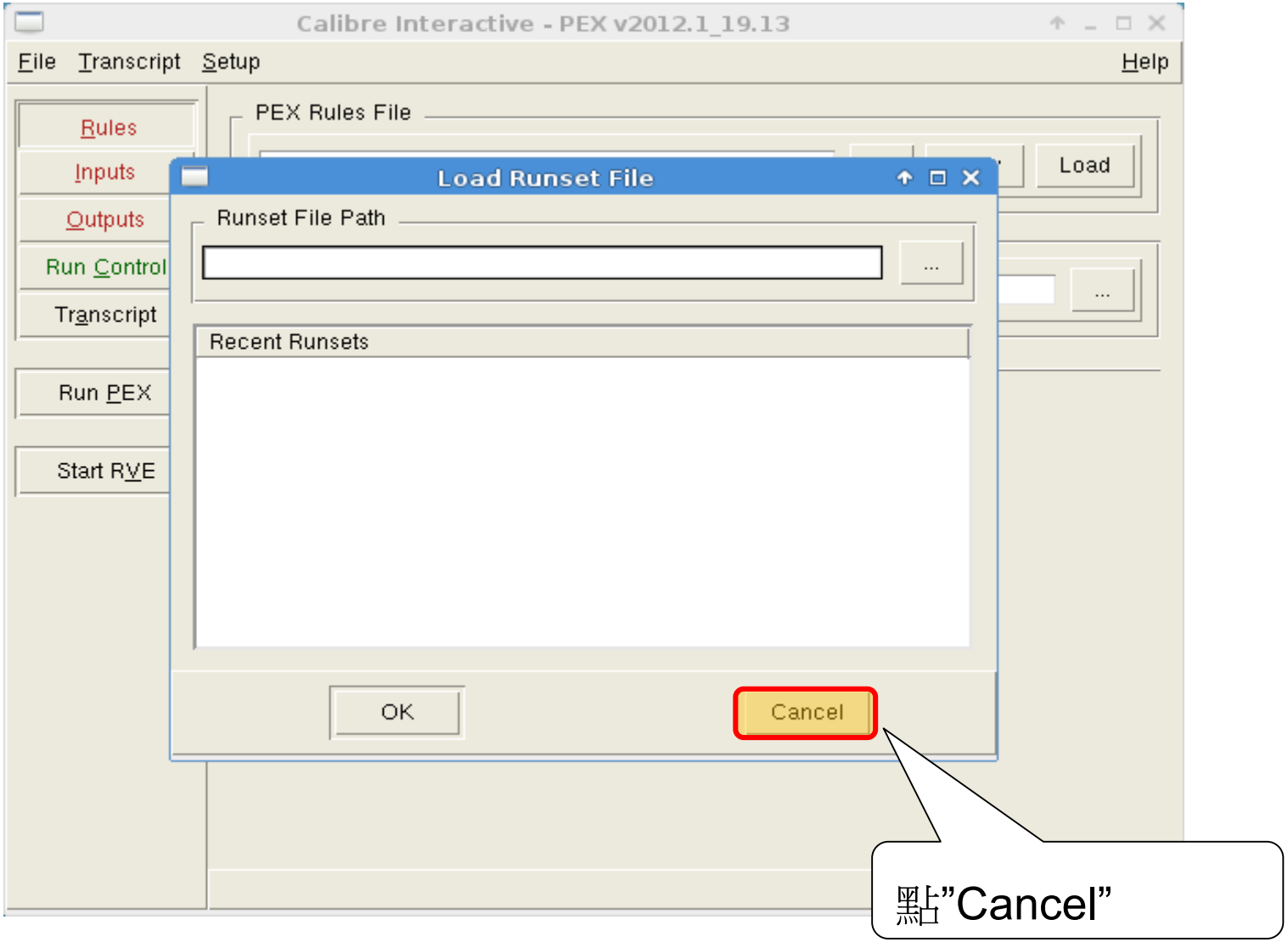


執行PEX

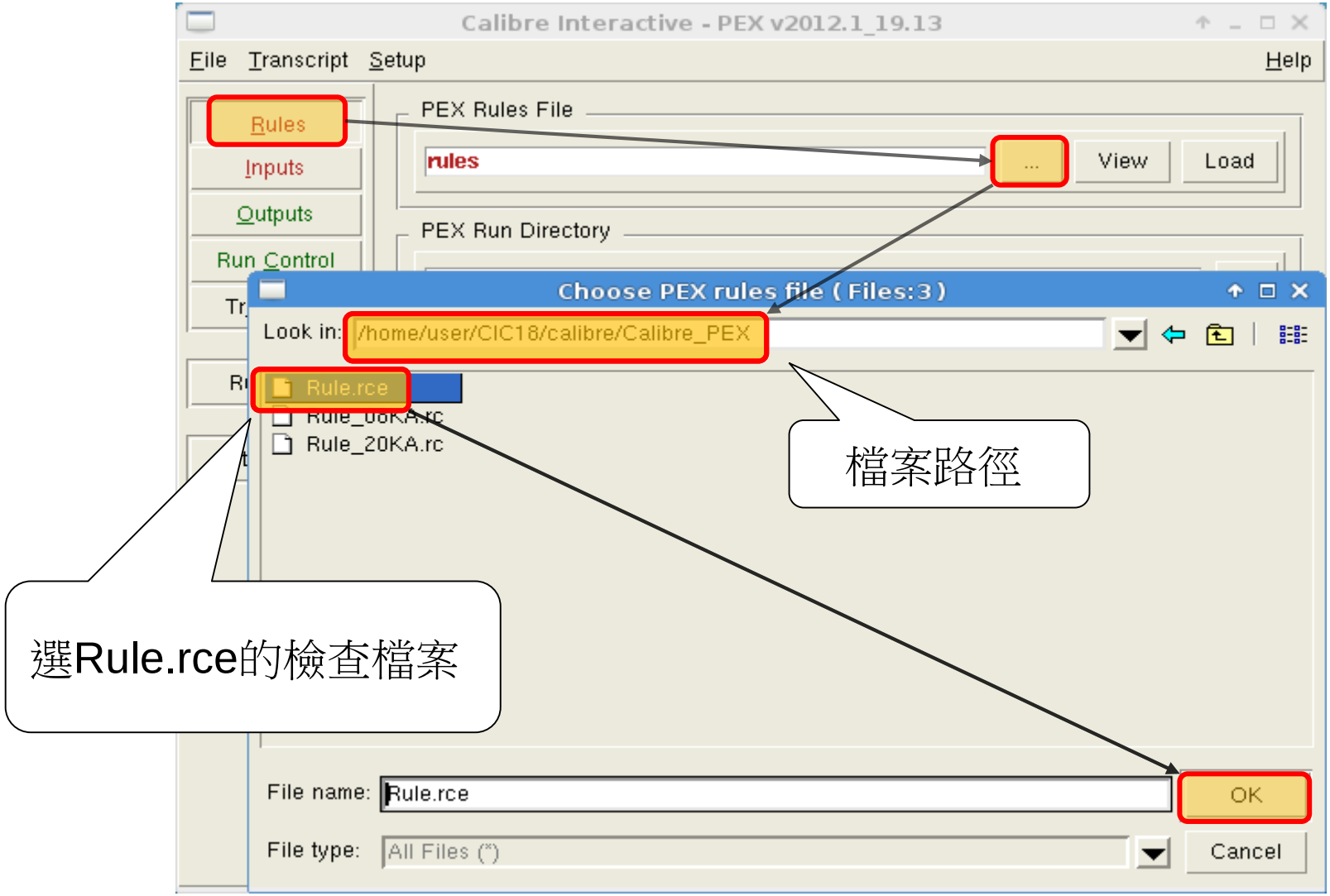
Practices Extraction (PEX)



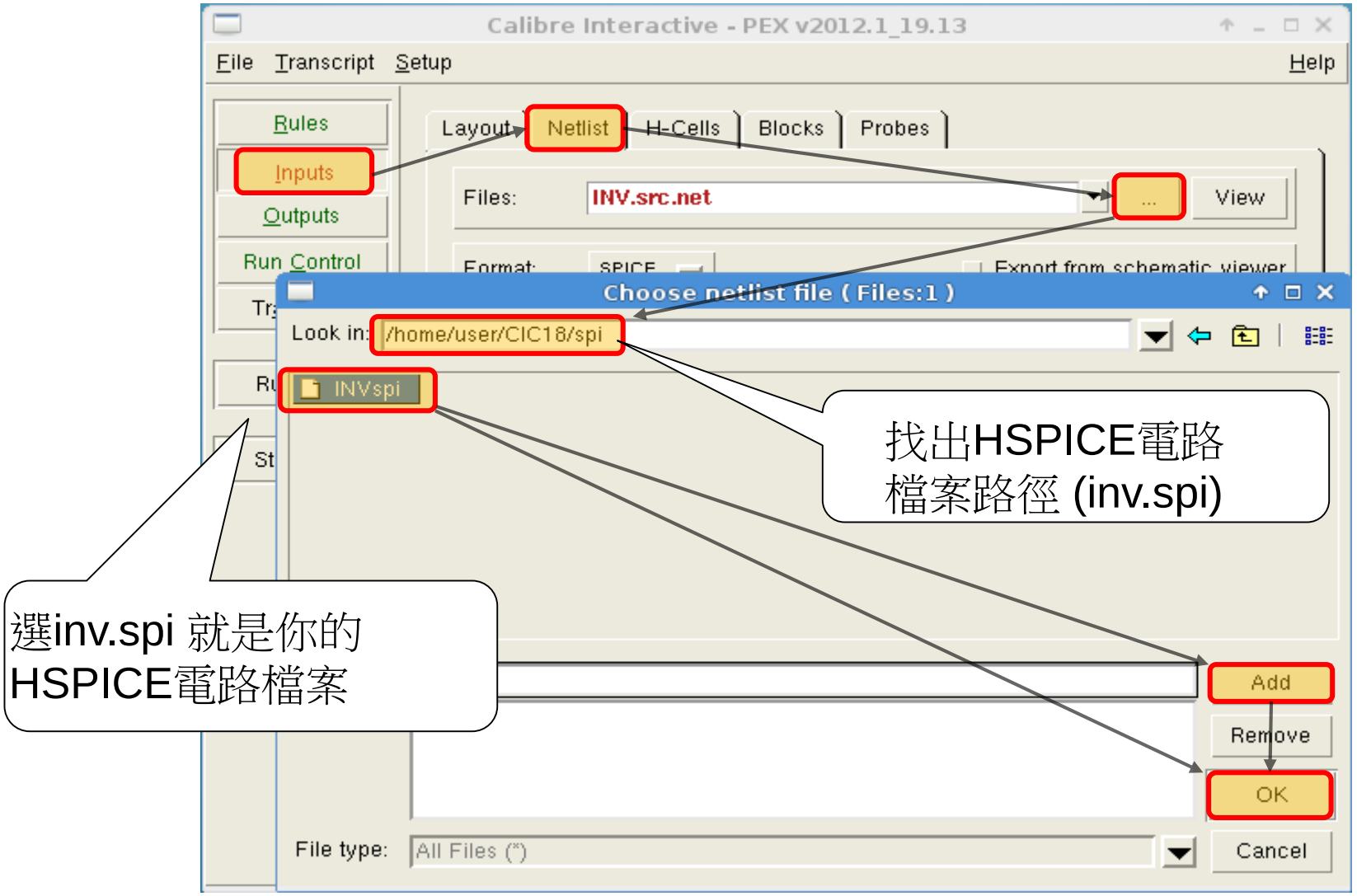
Practices Extraction (PEX)



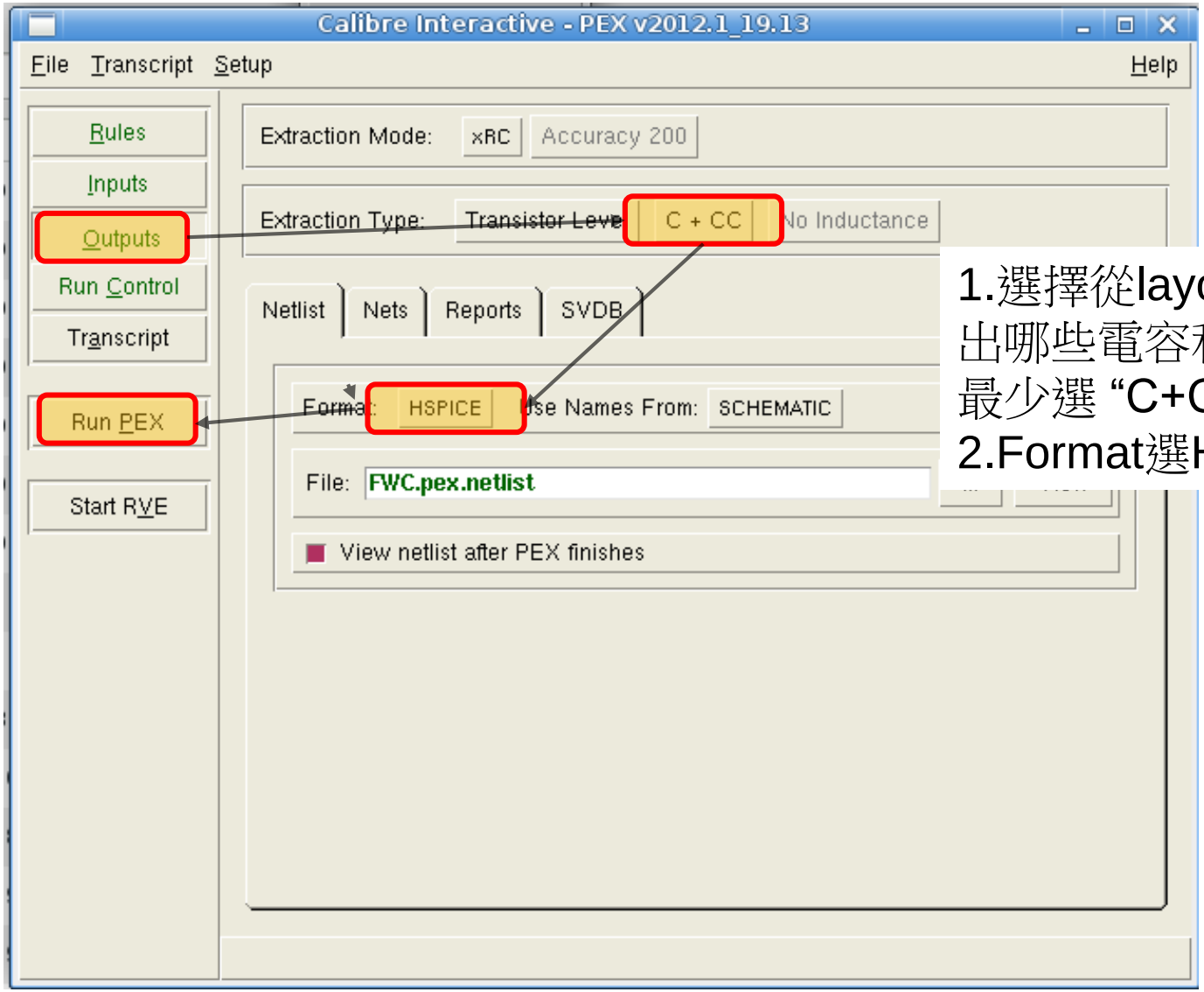
Practices Extraction (PEX)



Practices Extraction (PEX)



Practices Extraction (PEX)

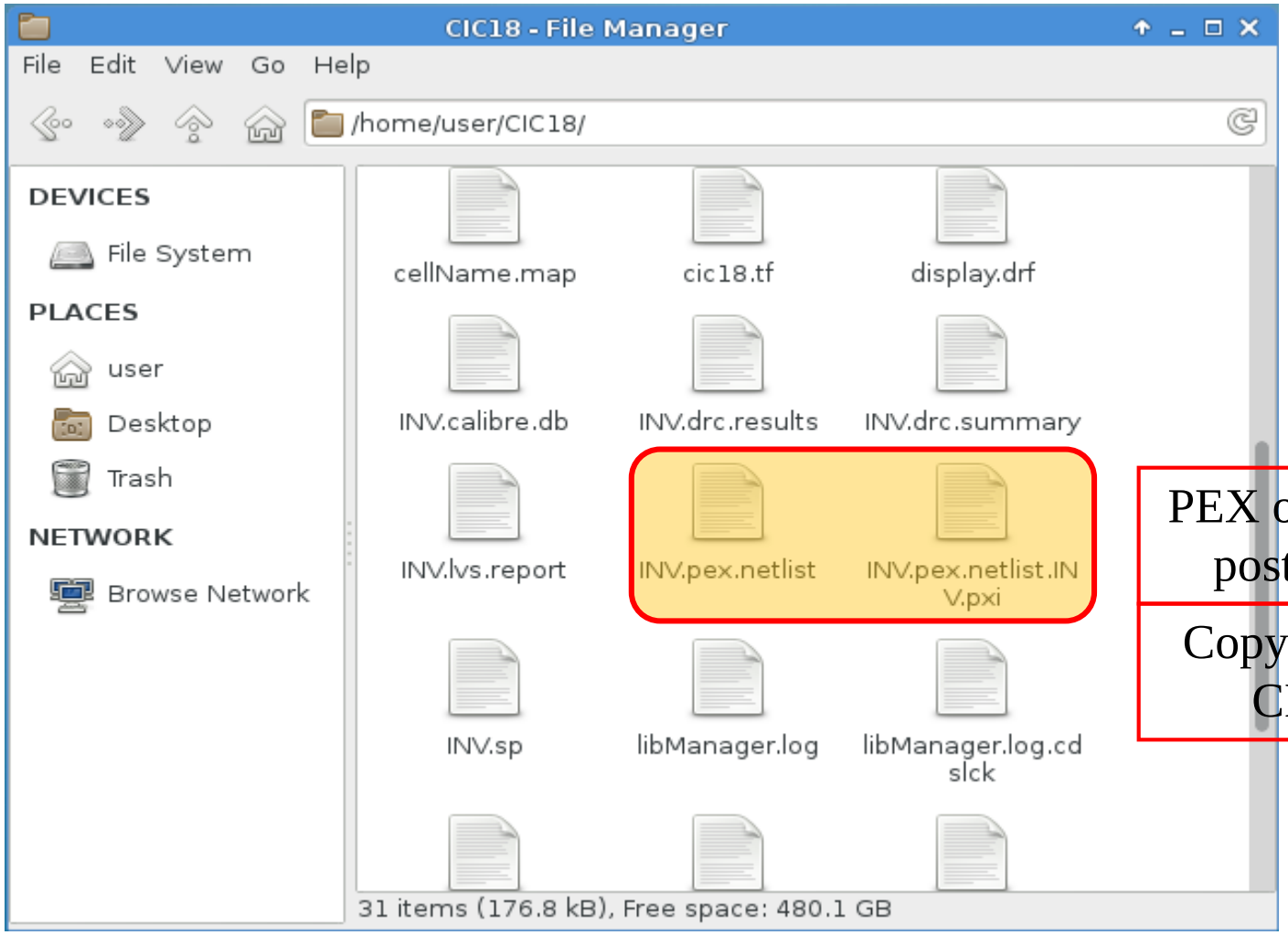


1.選擇從layout中抓出哪些電容和電阻 最少選 “C+CC”
2.Format選HSPICE

Parasitic Extraction / Extract RC

- Extraction Methods:
  - C+CC – Lumped C model
    - Parasitic capacitors between ground and couple
  - R+C – Distributed RC model
    - Net is broken into a resistor network, associated with capacitance between ground.
  - R+C+CC – Distributed RC + Couple C
    - Distributed RC network with the coupling capacitance.
  - R – Distributed R
    - Only resistor in extraction

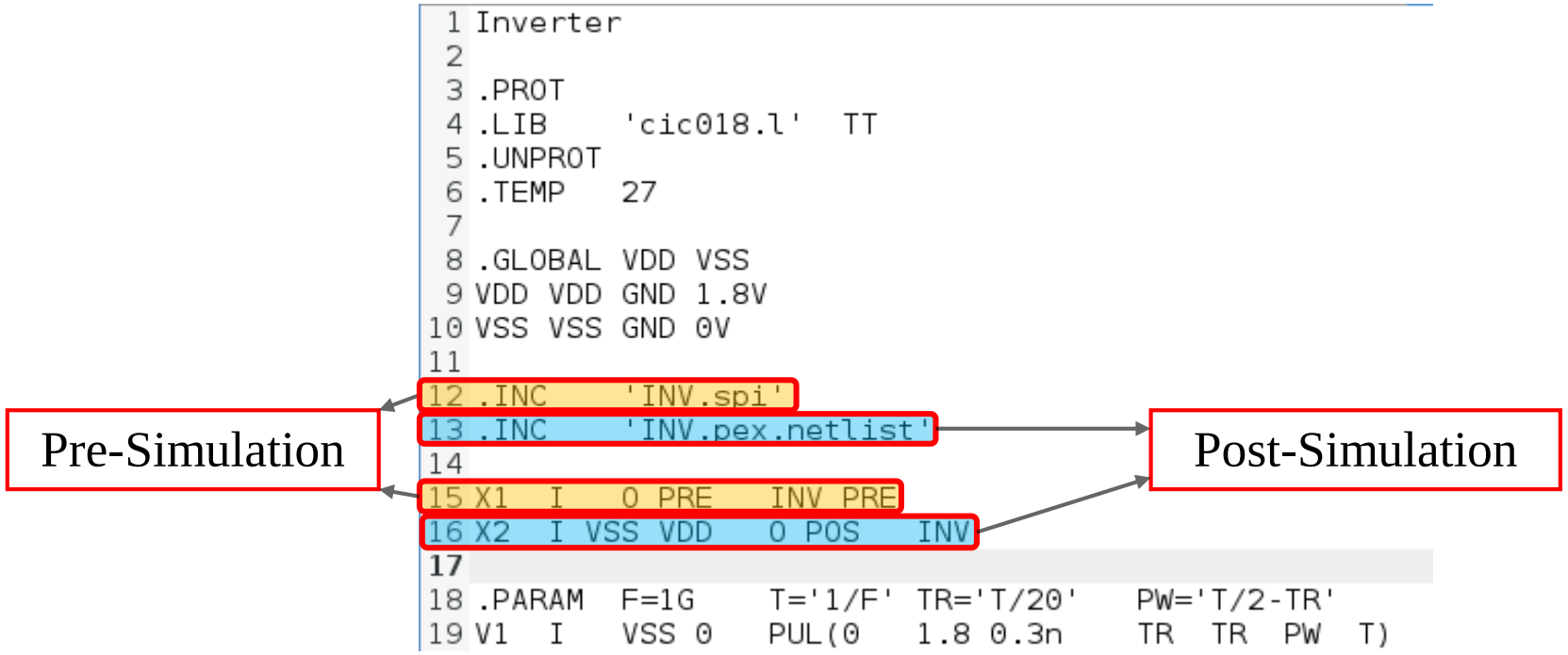
Post-Simulation



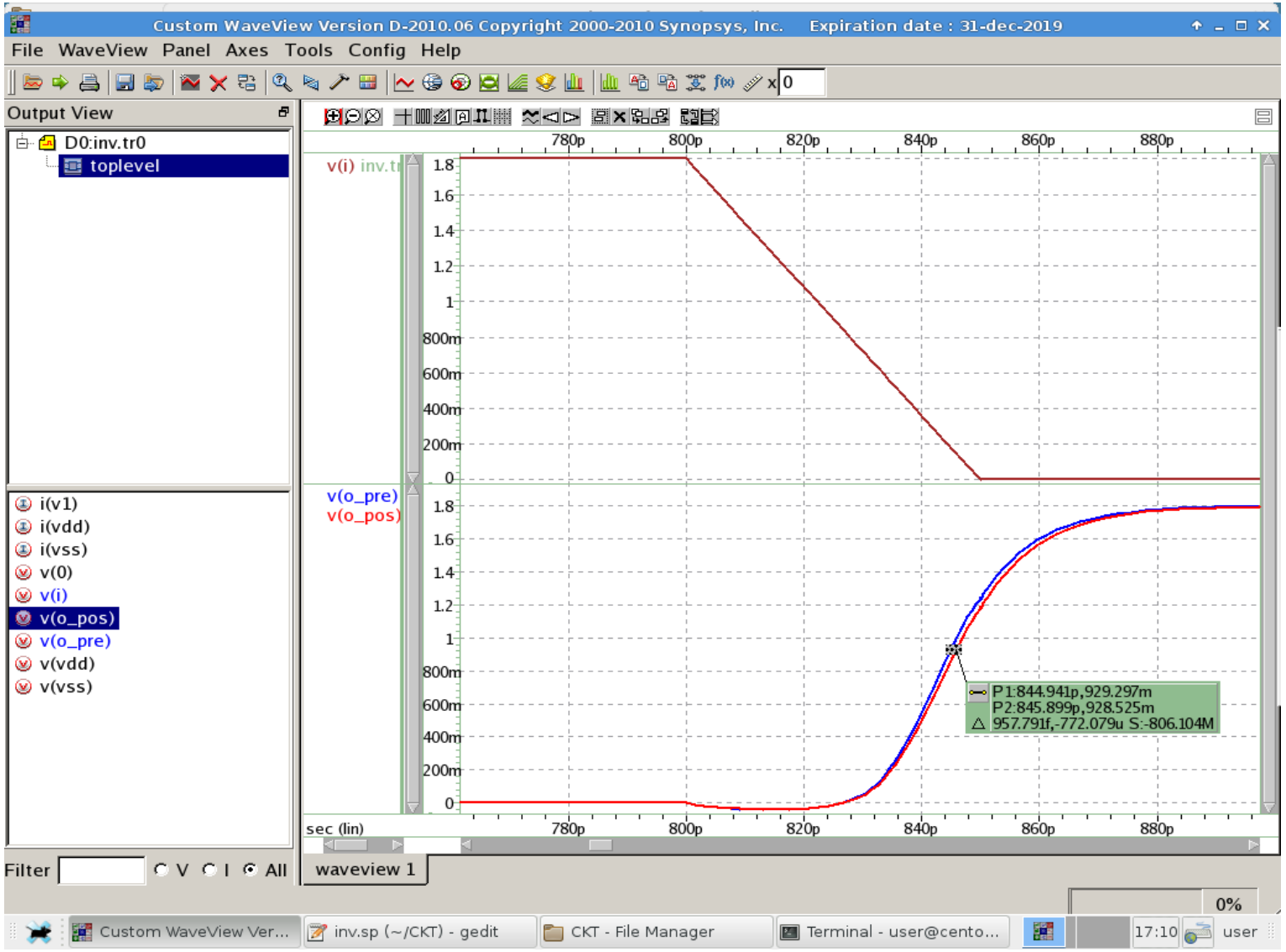
PEX output files for post-simulation

Copy these files to CKT folder

Post-Simulation



Post-Simulation

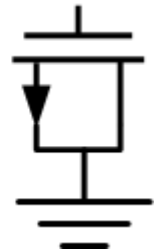


CAP layout

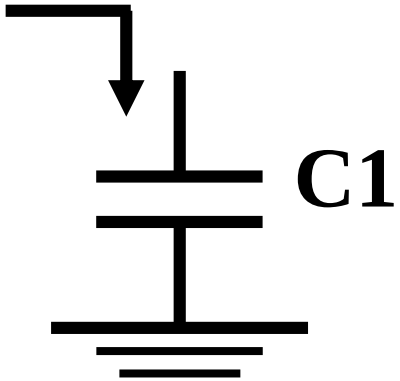
Gate Capacitor

$$C = \frac{\varepsilon_{ox}}{t_{ox}} W \cdot L = C_{ox} \cdot W \cdot L$$

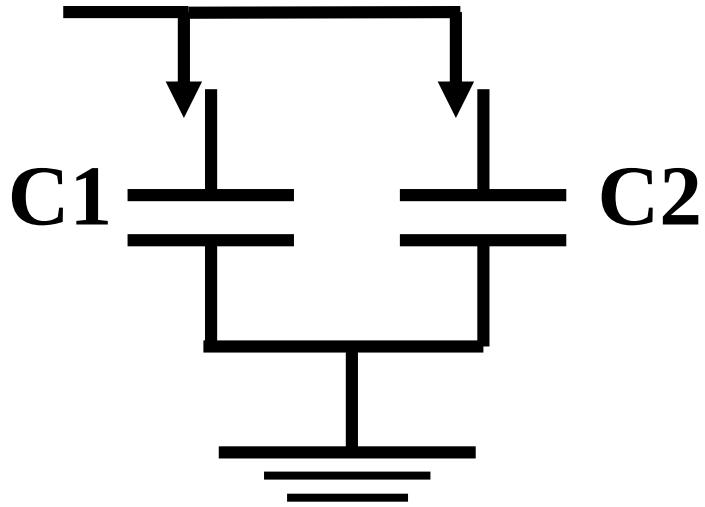
W/L=20u/20u



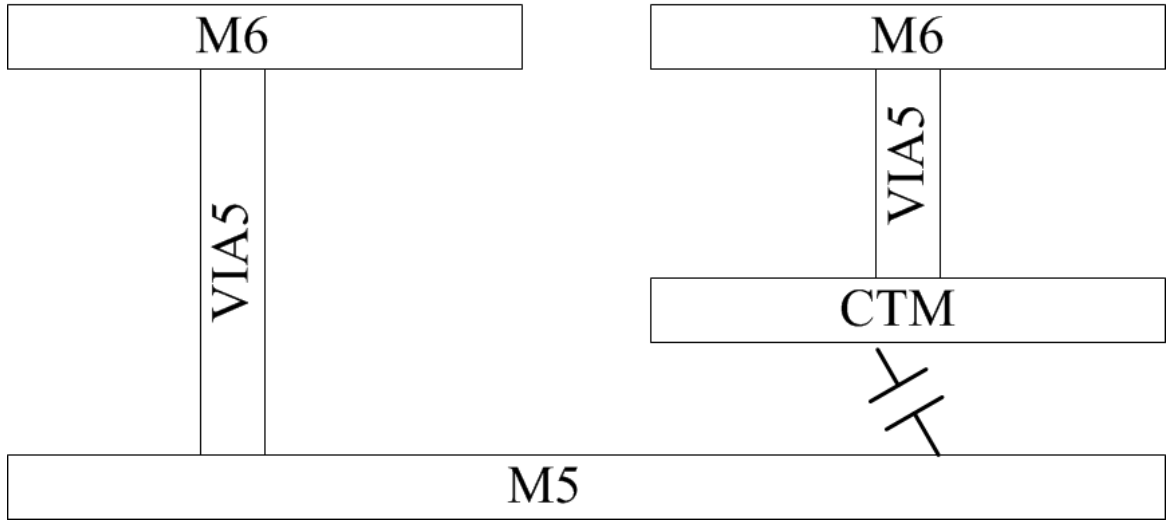
$C_{in} = C_1$

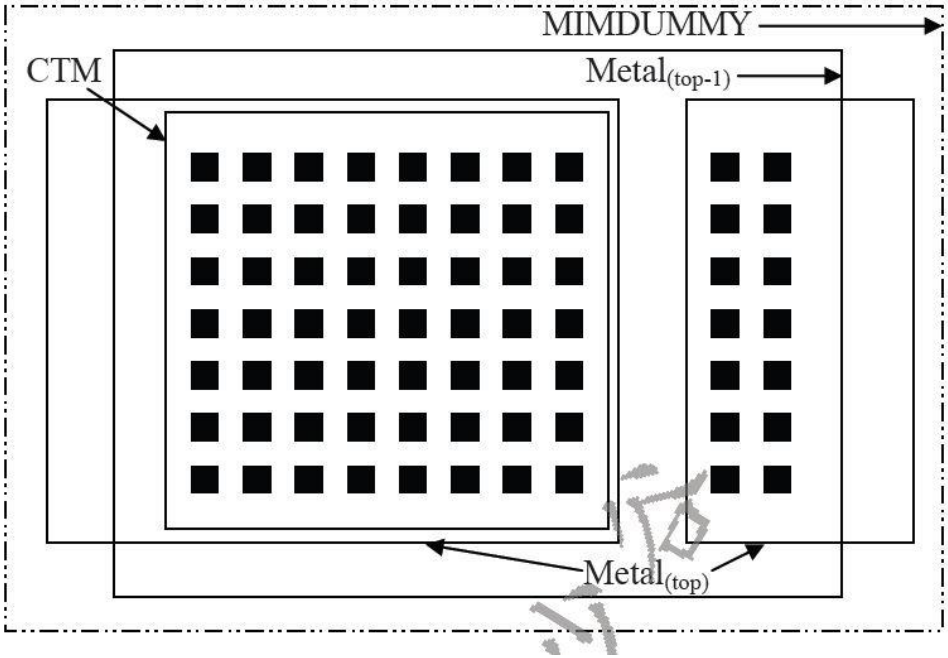


$C_{in} = C_1 + C_2$

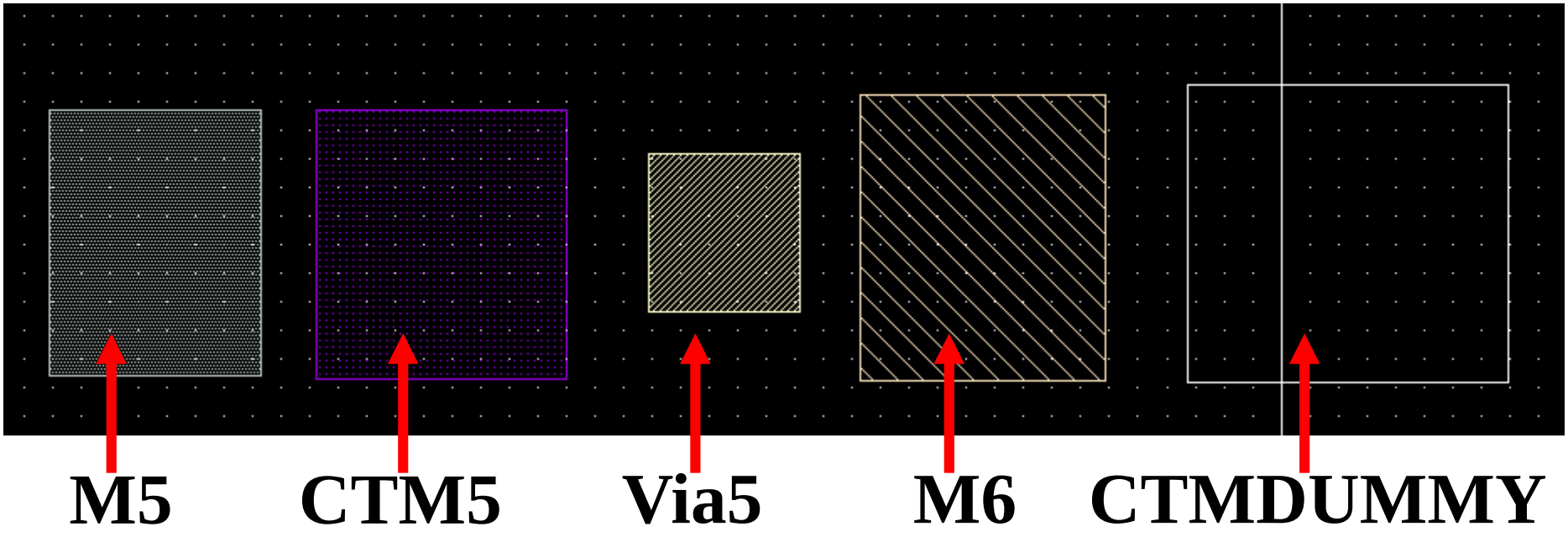


MIM Capacitor





Example of MIM Capacitor



感謝

鄭翔及
李欣芸