



# KC705 PCIe Design Creation

October 2014

XTP197

# Revision History

Date	Version	Description
10/08/14	10.0	Recompiled for 2014.3.
06/09/14	9.0	Recompiled for 2014.2. AR44635 and AR54939 fixed.
04/16/14	8.0	Recompiled for 2014.1.
12/18/13	7.0	Recompiled for 2013.4.
10/23/13	6.0	Recompiled for 2013.3. Added AR54939.
06/19/13	5.0	Recompiled for 2013.2. AR55494 fixed.
04/03/13	4.0	Recompiled for 2013.1. Added AR55494.
12/18/12	3.0	Recompiled for 2012.4. Added AR53392.
10/23/12	2.0	Recompiled for 2012.3. Added AR52368.
08/20/12	1.0	Initial version. Added AR50886.

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# Overview

➤ **Kintex-7 PCIe x8 Gen 2 Capability**

➤ **Xilinx KC705 Board**

➤ **Software Requirements**

➤ **KC705 Setup**

➤ **Generate x8 Gen 2 PCIe Core**

- Modify PCIe Core
- Compile Example Design
- Generate PCIe MCS File
- Program BPI Flash with PCIe Design

➤ **Running the PCIe x8 Gen 2 Design**

➤ **References**

# Kintex-7 PCIe x8 Gen 2 Capability

## ► KC705 Supports PCIe Gen 1 and Gen 2 Capability

- x8, x4, x2, or x1 Gen 1 and Gen 2 lane width
- x8 Gen 2 not supported in -1 parts
- See [PG054](#) for details

## ► LogiCORE PIO Example Design

- KC705 PCIe Design Files (2014.3 C) ZIP file
- Available through <http://www.xilinx.com/kc705>

## ► 7 Series Integrated Block for PCI Express

- See [PG054](#) for details

# Kintex-7 PCIe x8 Gen 2 Capability

## ➤ Integrated Block for PCI Express

- PCI Express Base 2.0 Specification

## ➤ Configurable for Endpoint or Root Port Applications

- KC705 configured for Endpoint Applications

## ➤ GTX Transceivers implement a fully compliant PHY

## ➤ Large range of maximum payload size

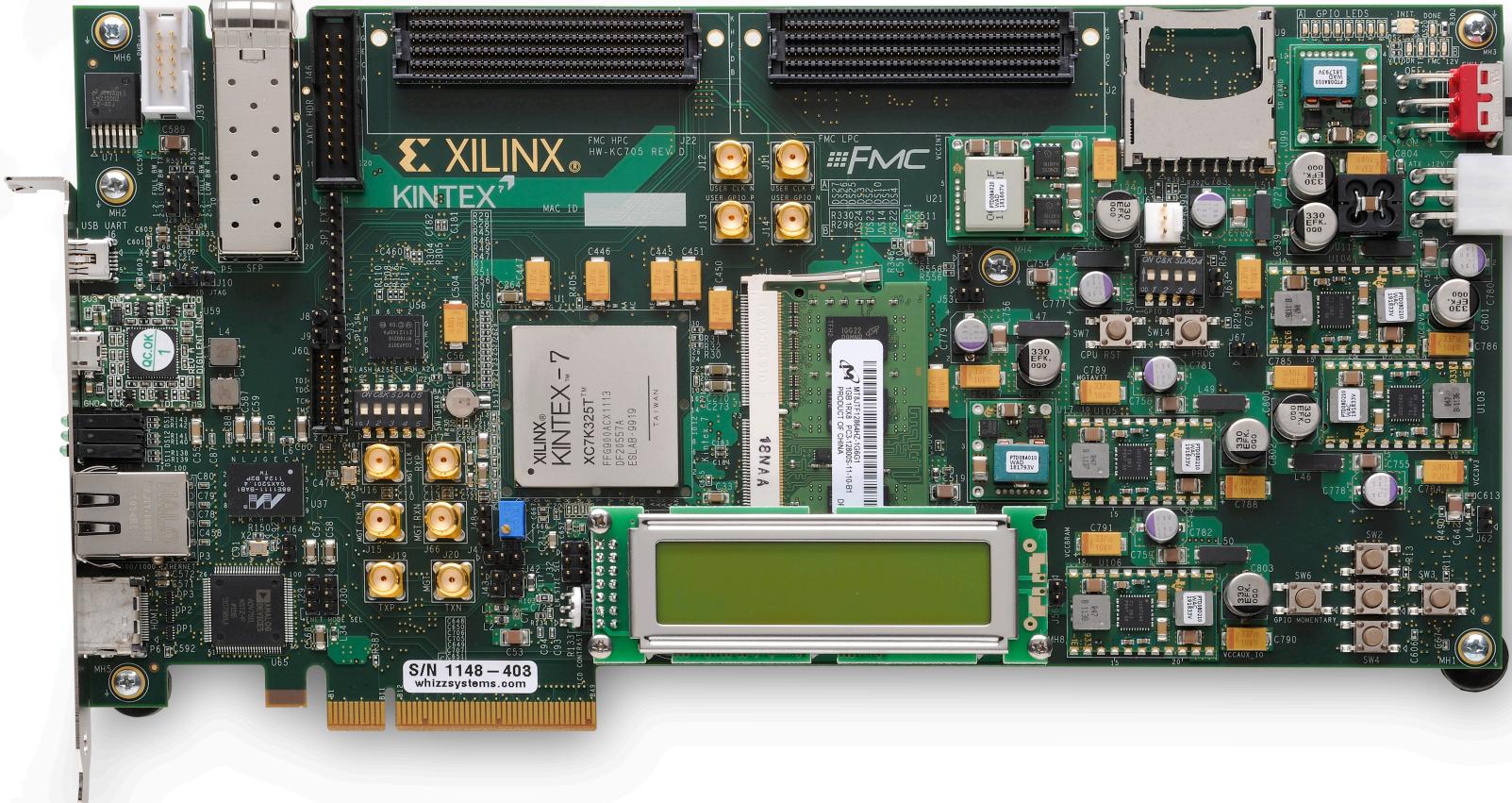
- 128 / 256 / 512 / 1024 bytes

## ➤ Configurable BAR spaces

- Up to 6 x 32 bit, 3 x 64 bit, or a combination
- Memory or IO
- BAR and ID filtering

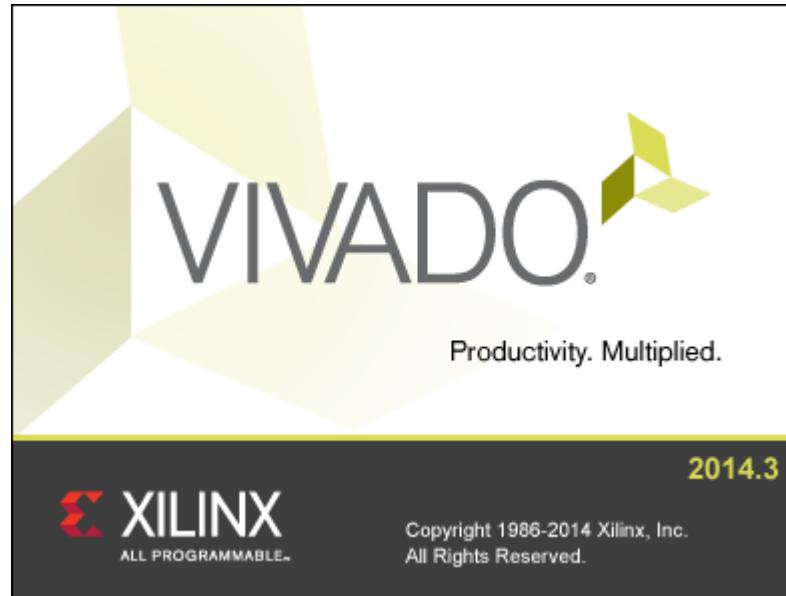
## ➤ Management and Statistics Interface

# Xilinx KC705 Board



# Vivado Software Requirements

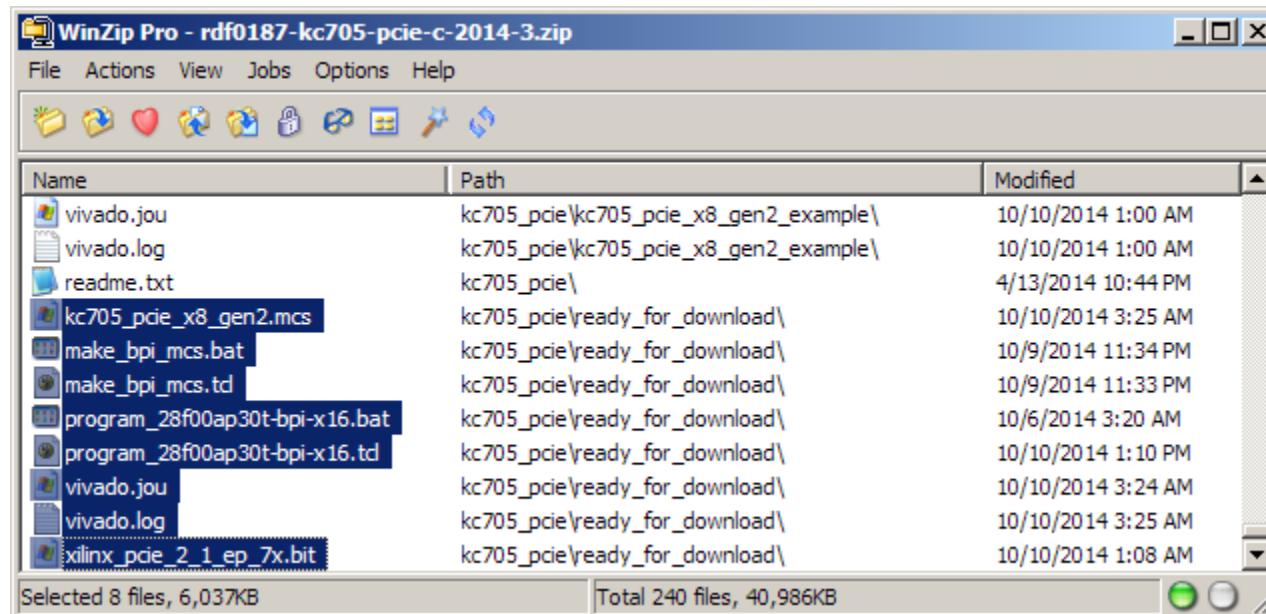
- Xilinx Vivado Design Suite 2014.3, Design Edition



# Setup for the KC705 PCIe Design

► Open the KC705 PCIe Design Files (2014.3 C) ZIP file, and extract these files to your C:\ drive:

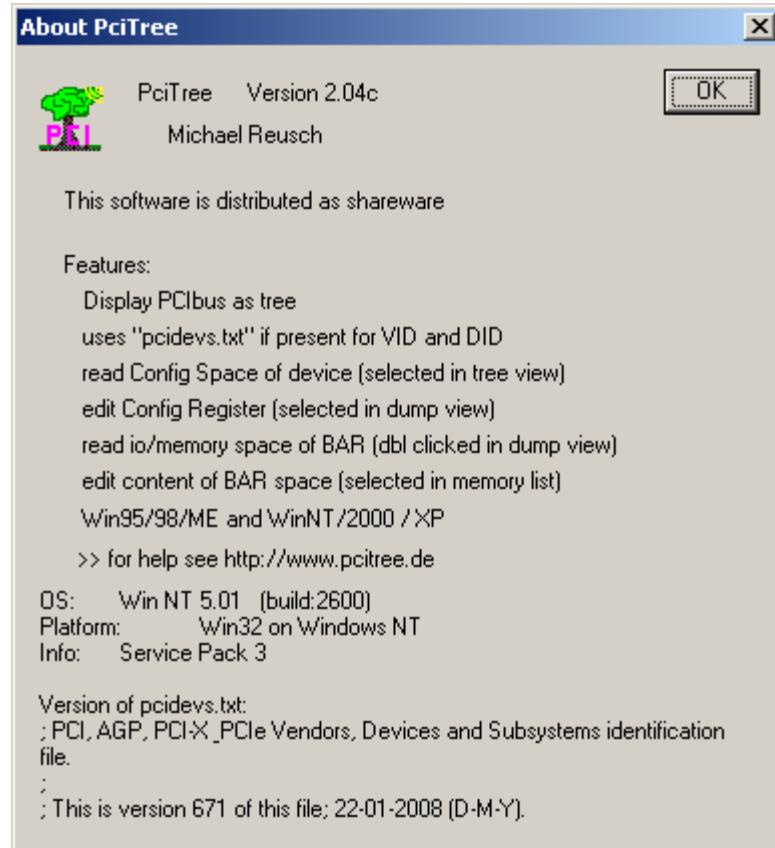
- kc705\_PCIE\ready\_for\_download\\*
- Available through <http://www.xilinx.com/kc705>



# PciTree Software Requirement

## ► PciTree Bus Viewer

- Free [download](#)
- HLP.SYS must be copied to  
C:\WINDOWS\system32\drivers  
directory



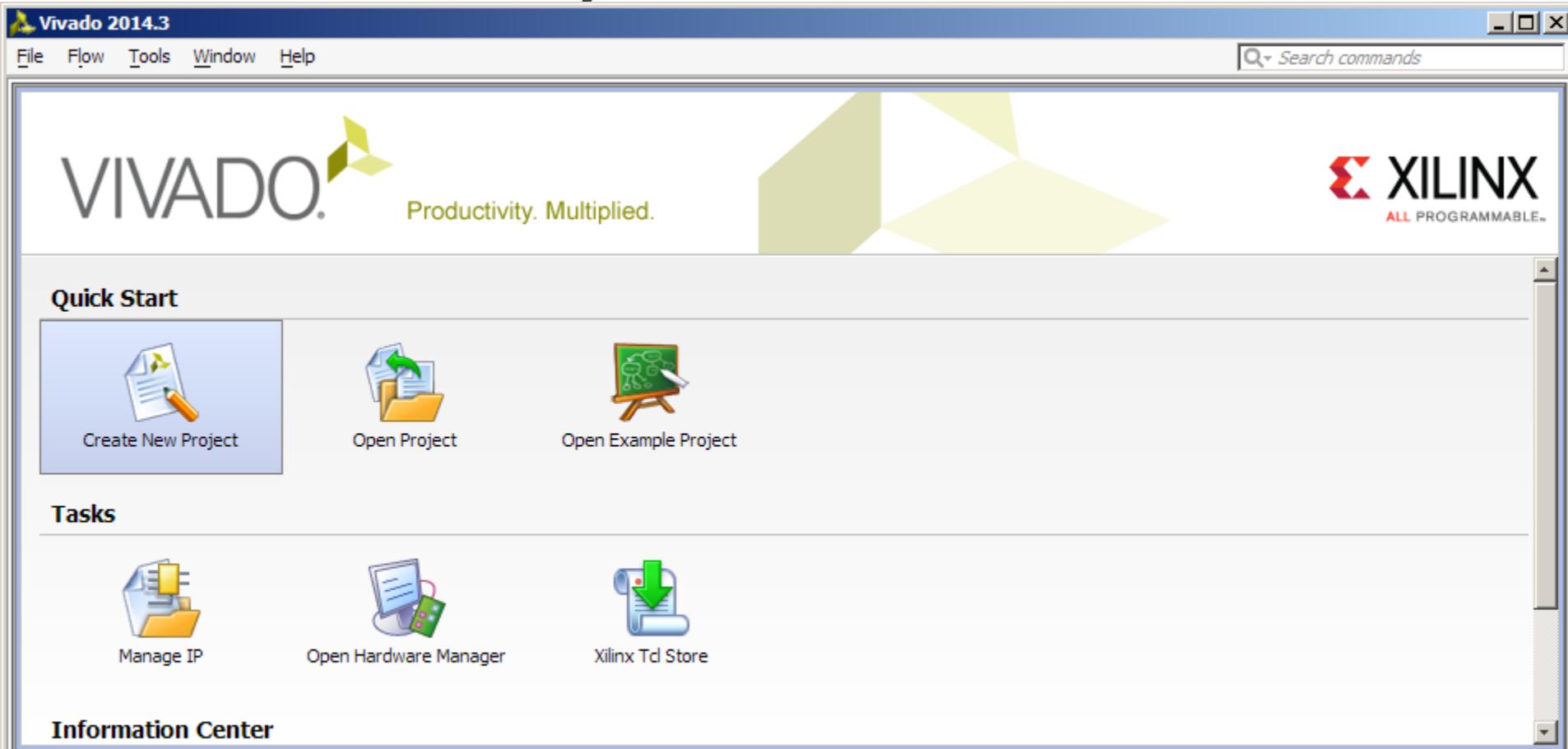
# Generate x8 Gen 2 PCIe Core

# Generate x8 Gen 2 PCIe Core

## ► Open Vivado

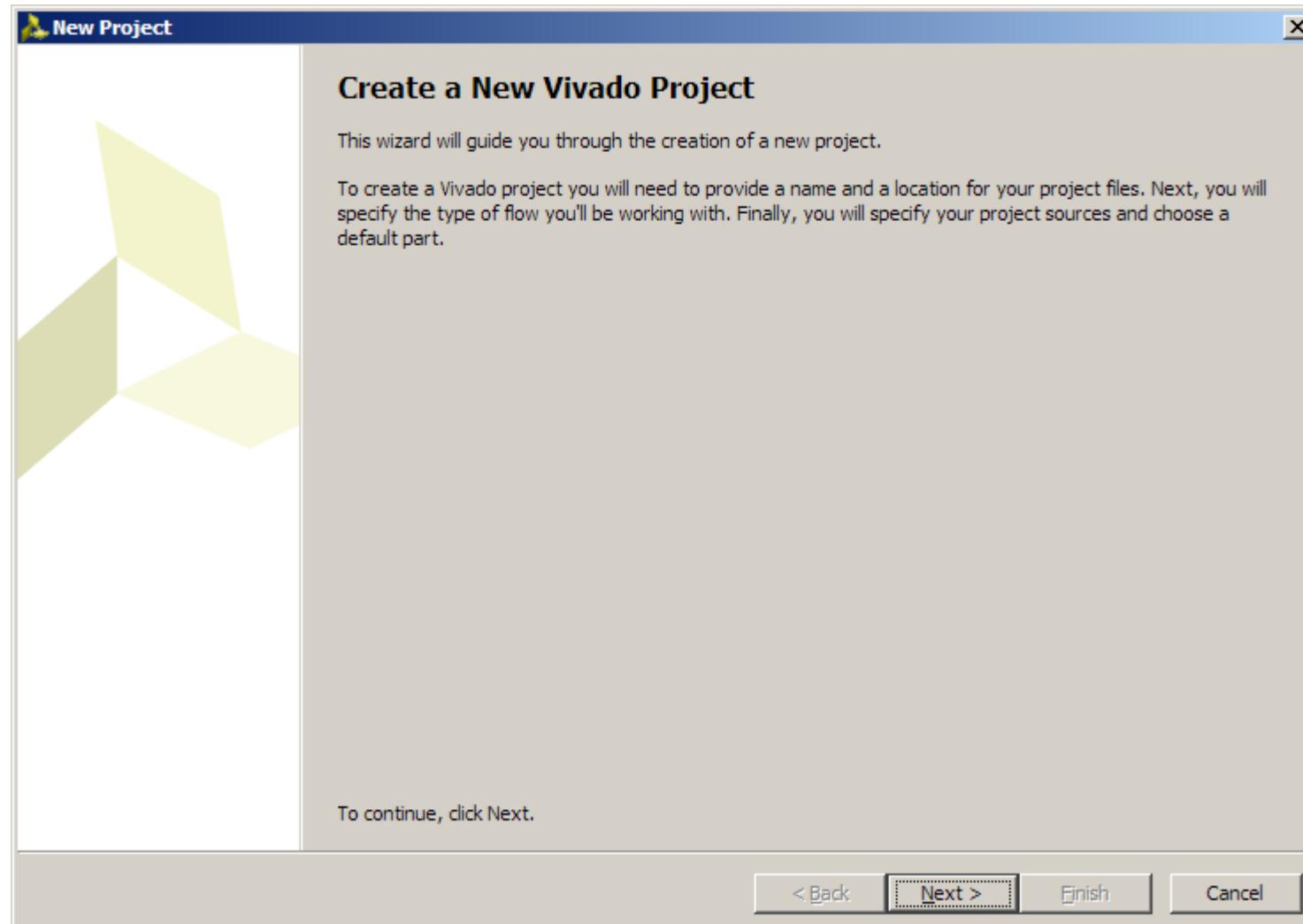
Start → All Programs → Xilinx Design Tools → Vivado 2014.3 → Vivado

## ► Select Create New Project



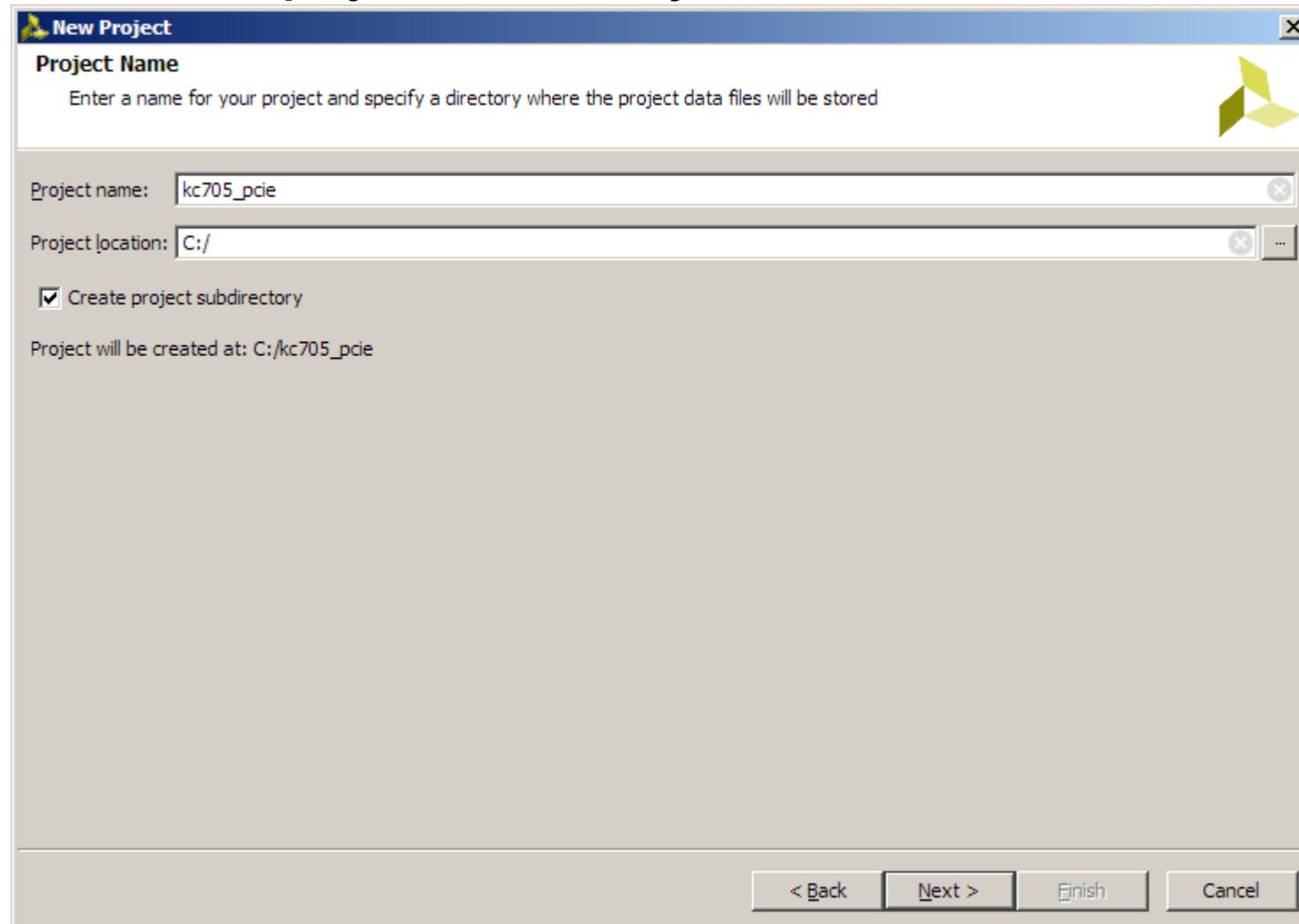
# Generate x8 Gen 2 PCIe Core

► Click Next



# Generate x8 Gen 2 PCIe Core

- Set the Project name and location to **kc705\_pcnie** and **C:\**
  - Check **Create project subdirectory**



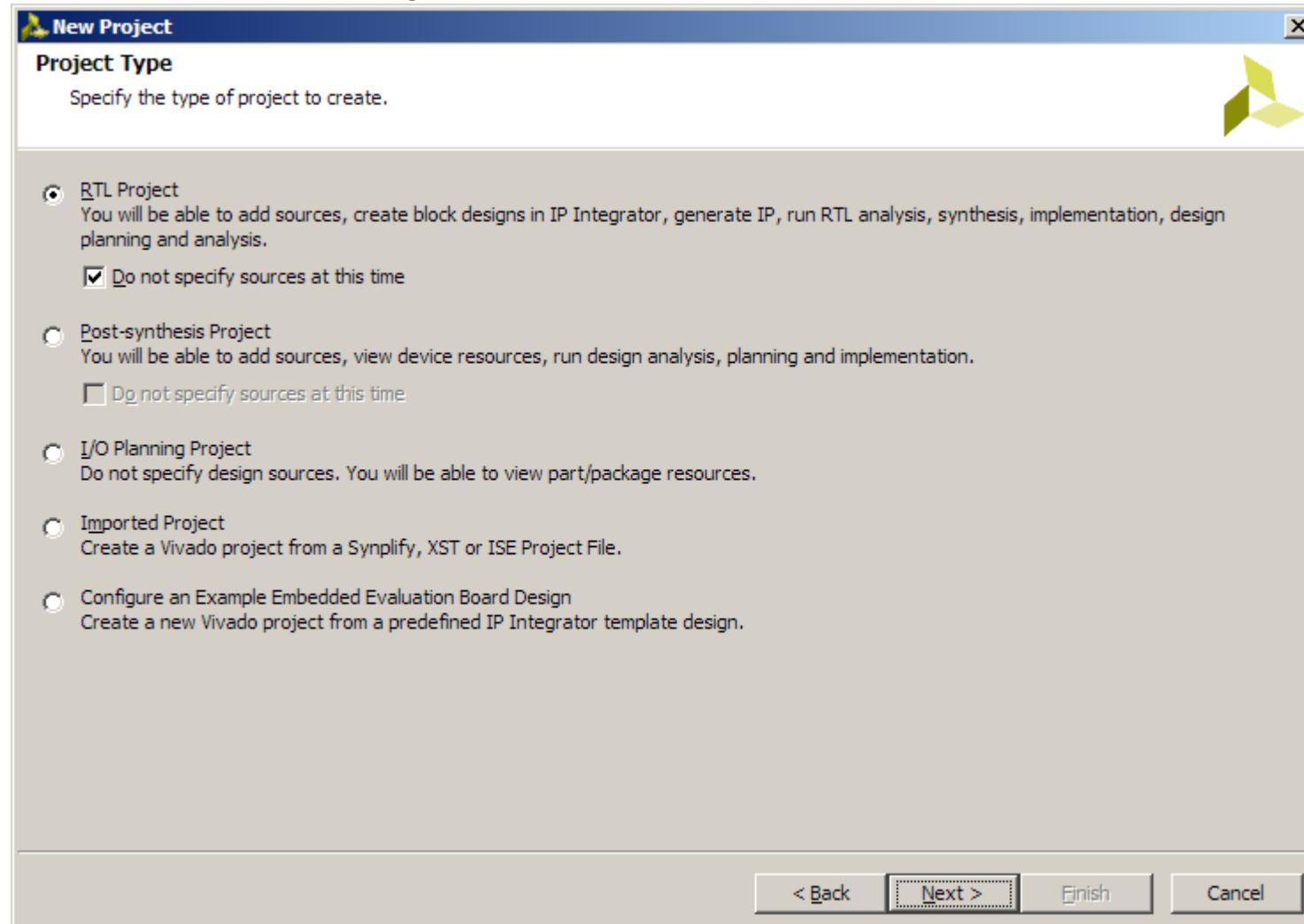
**Note:** Vivado generally requires forward slashes in paths

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# Generate x8 Gen 2 PCIe Core

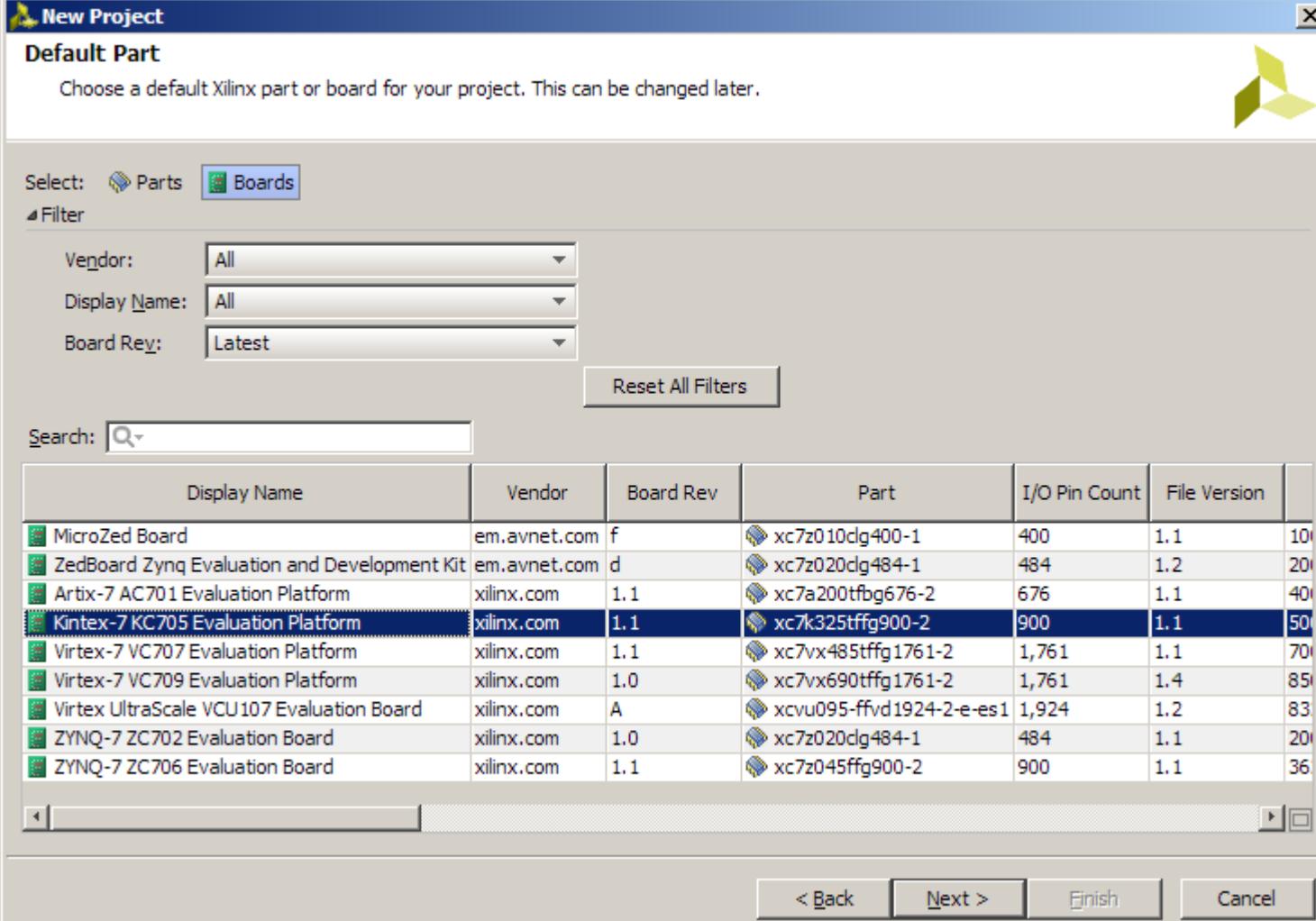
## ► Select RTL Project

- Select **Do not specify sources at this time**



# Generate x8 Gen 2 PCIe Core

## ► Select the KC705 Board



New Project

Default Part

Choose a default Xilinx part or board for your project. This can be changed later.

Select:  Parts  Boards

Filter

Vendor: All

Display Name: All

Board Rev: Latest

Reset All Filters

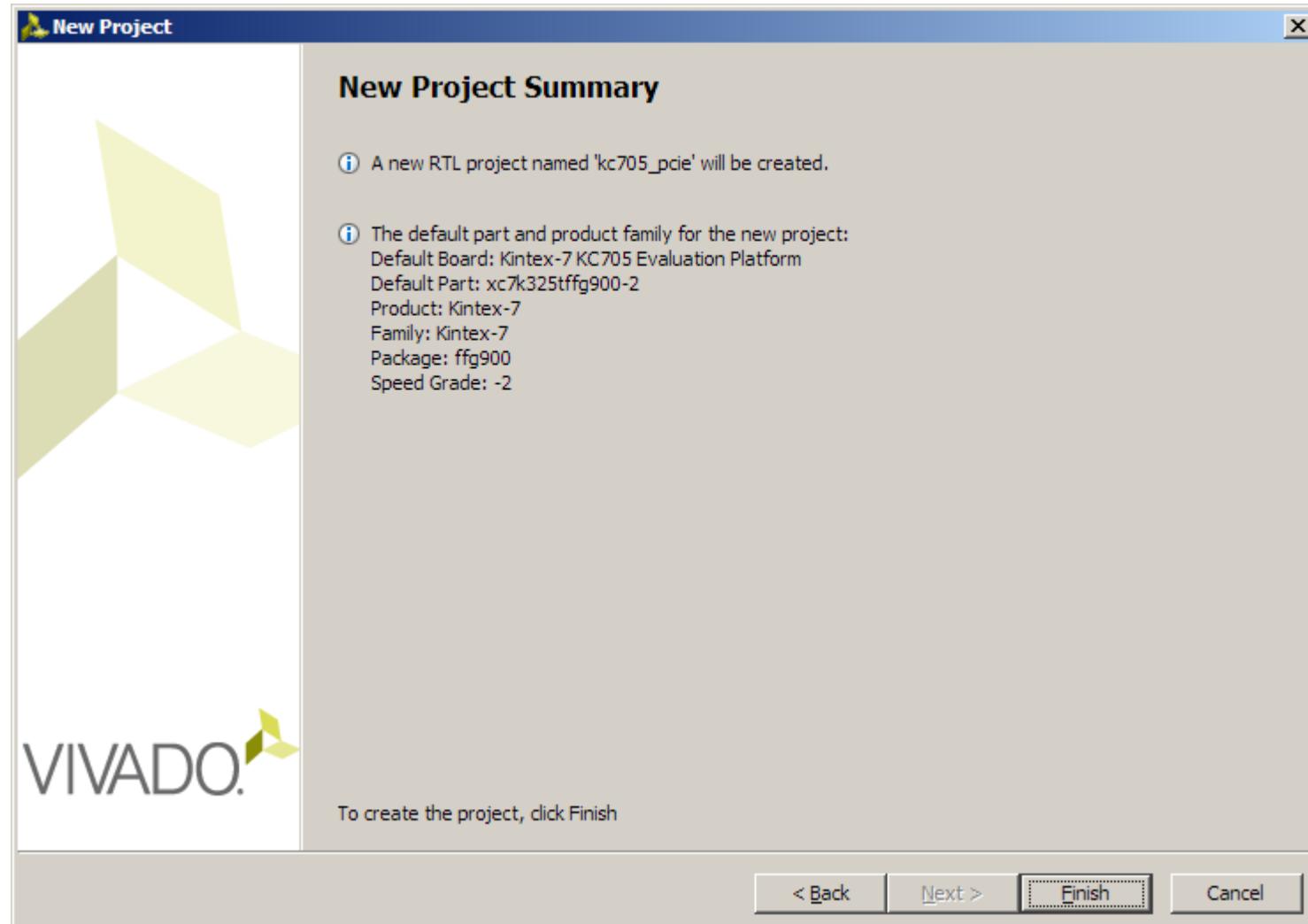
Search:

Display Name	Vendor	Board Rev	Part	I/O Pin Count	File Version	Revision
MicroZed Board	em.avnet.com	f	xc7z010clg400-1	400	1.1	10
ZedBoard Zynq Evaluation and Development Kit	em.avnet.com	d	xc7z020clg484-1	484	1.2	20
Artix-7 AC701 Evaluation Platform	xilinx.com	1.1	xc7a200tfg676-2	676	1.1	40
<b>Kintex-7 KC705 Evaluation Platform</b>	xilinx.com	<b>1.1</b>	<b>xc7k325tffg900-2</b>	<b>900</b>	<b>1.1</b>	<b>50</b>
Vertex-7 VC707 Evaluation Platform	xilinx.com	1.1	xc7vx485tffg1761-2	1,761	1.1	70
Vertex-7 VC709 Evaluation Platform	xilinx.com	1.0	xc7vx690tffg1761-2	1,761	1.4	85
Vertex UltraScale VCU107 Evaluation Board	xilinx.com	A	xcvu095-ffvd1924-2-e-es1	1,924	1.2	83
ZYNQ-7 ZC702 Evaluation Board	xilinx.com	1.0	xc7z020clg484-1	484	1.1	20
ZYNQ-7 ZC706 Evaluation Board	xilinx.com	1.1	xc7z045tffg900-2	900	1.1	36

< Back

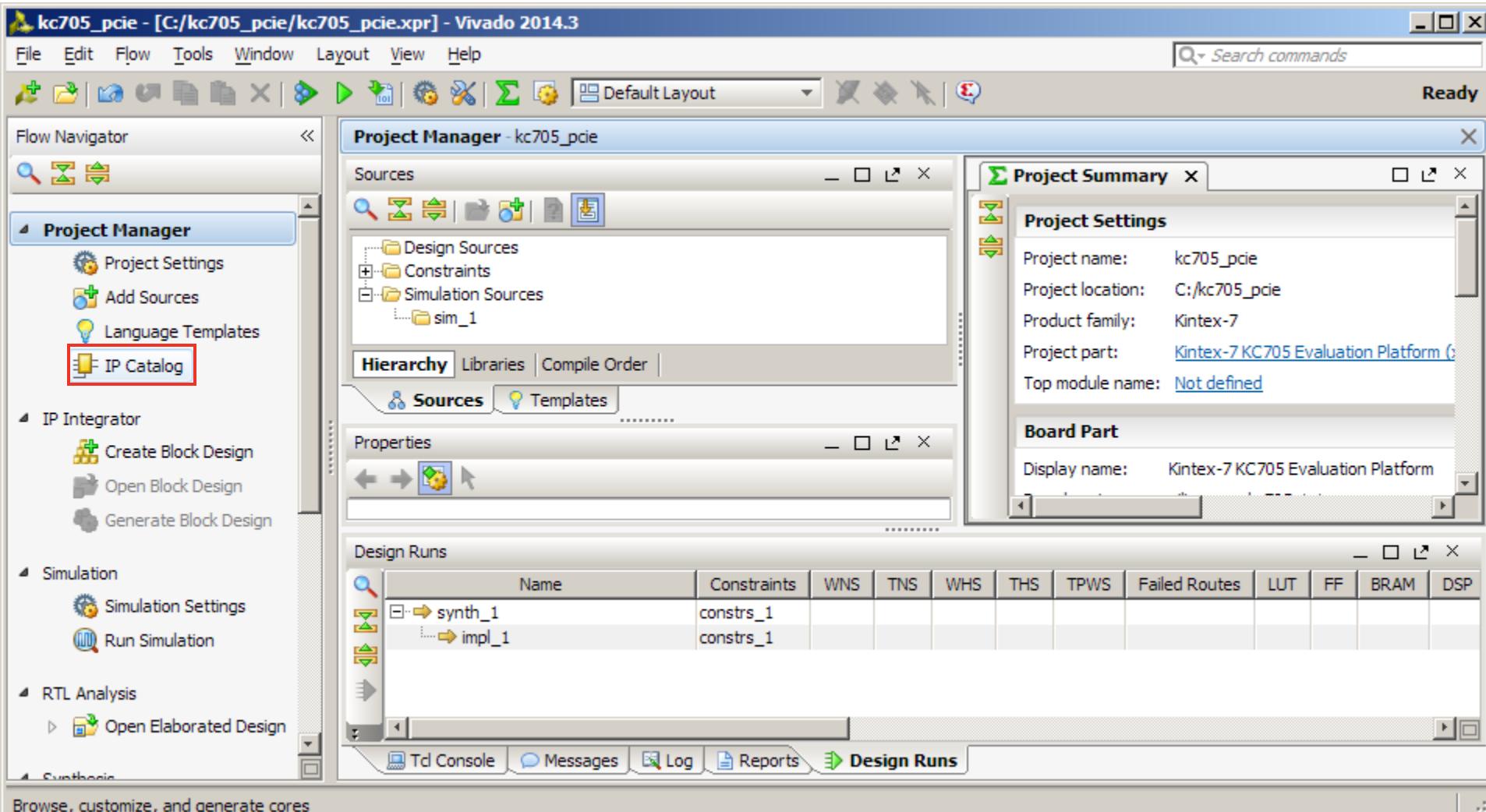
# Generate x8 Gen 2 PCIe Core

► Click Finish



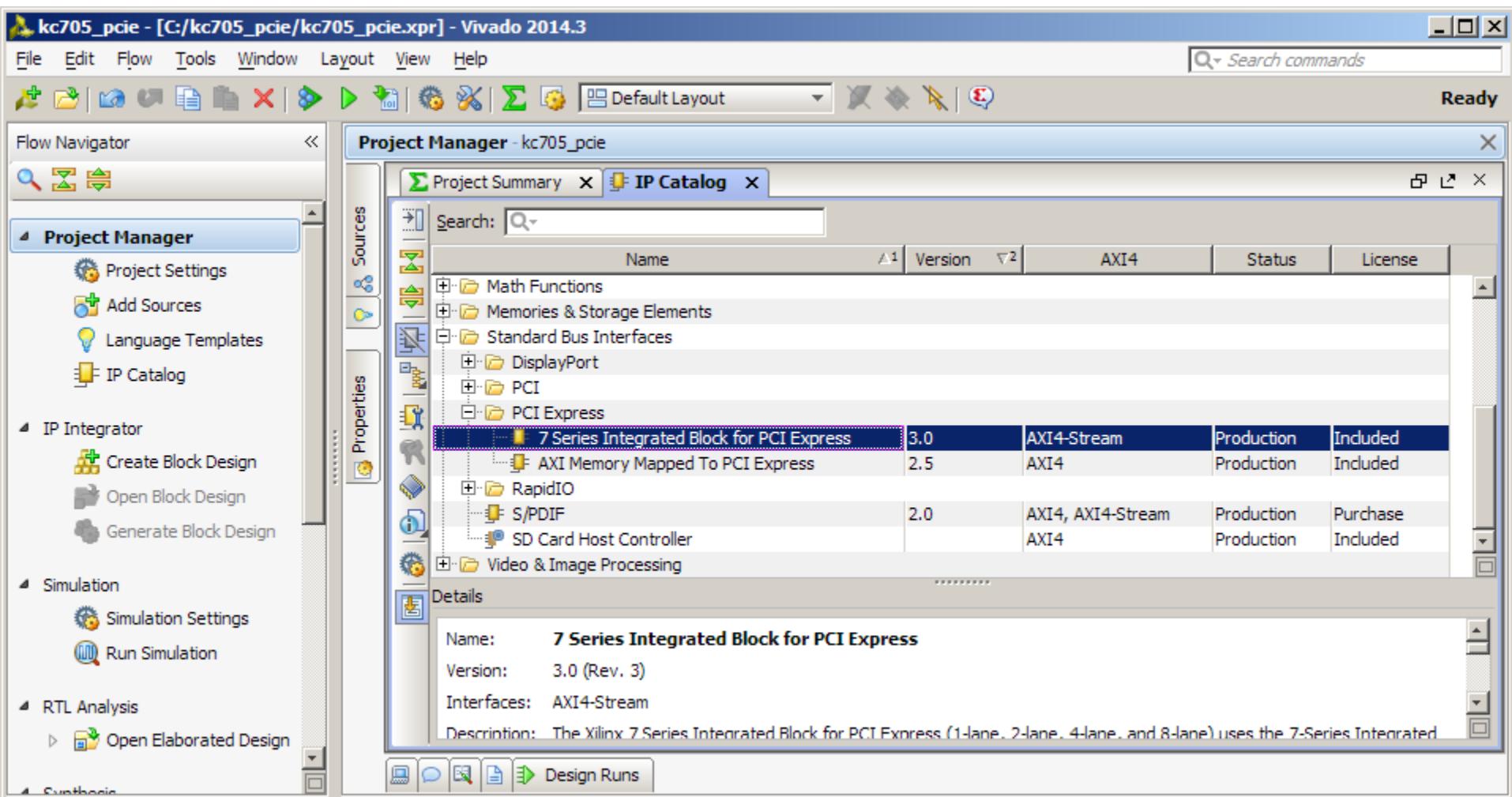
# Generate x8 Gen 2 PCIe Core

► Click on IP Catalog



# Generate x8 Gen 2 PCIe Core

- ▶ Select 7 Series Integrated Block for PCI Express, v3.0 under Standard Bus Interfaces



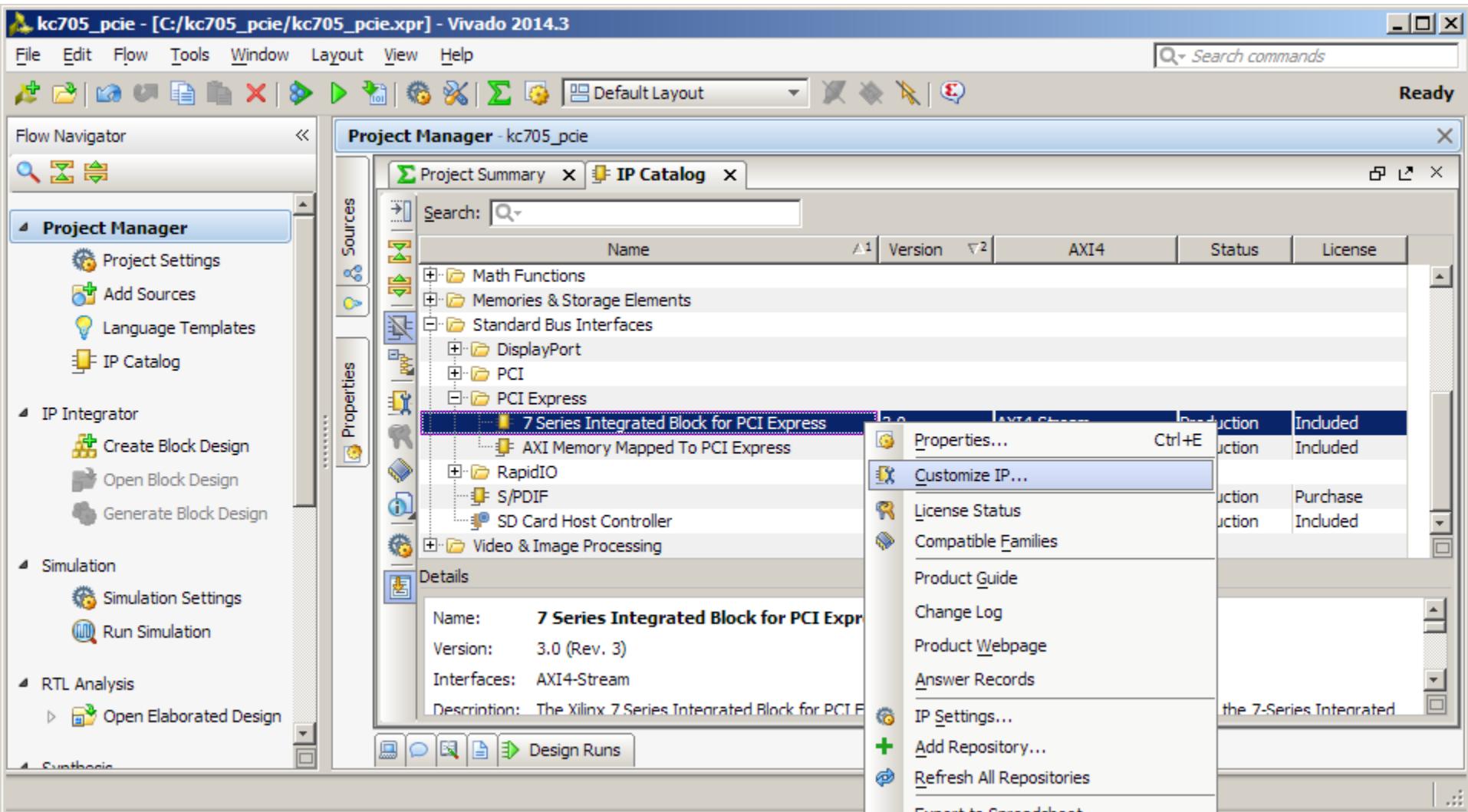
IP: 7 Series Integrated Block for PCI Express

Note: Presentation applies to the KC705

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# Generate x8 Gen 2 PCIe Core

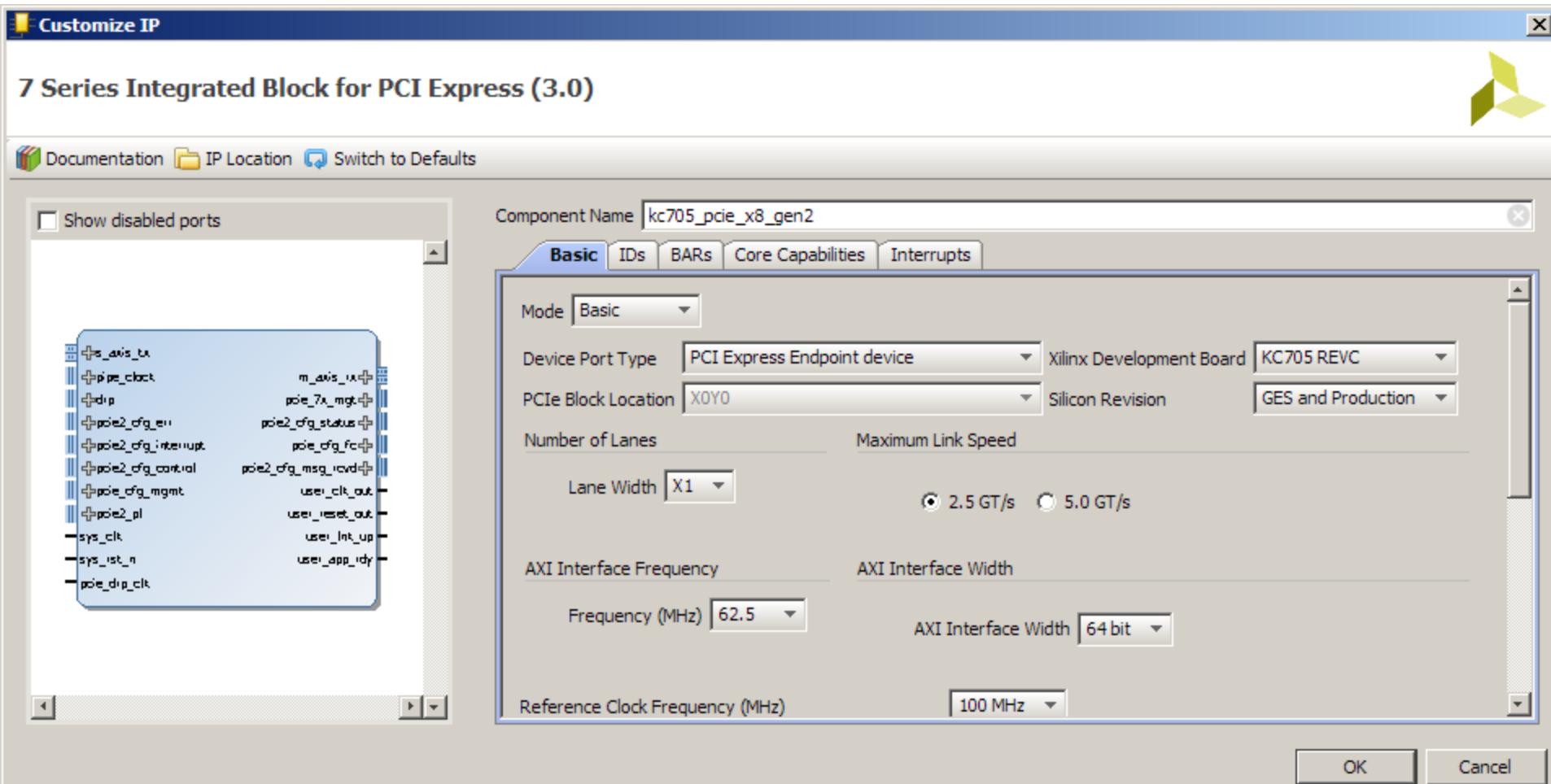
- Right click on 7 Series Integrated Block for PCI Express
  - Select **Customize IP...**



# Generate x8 Gen 2 PCIe Core

## ► Under the Basic tab,

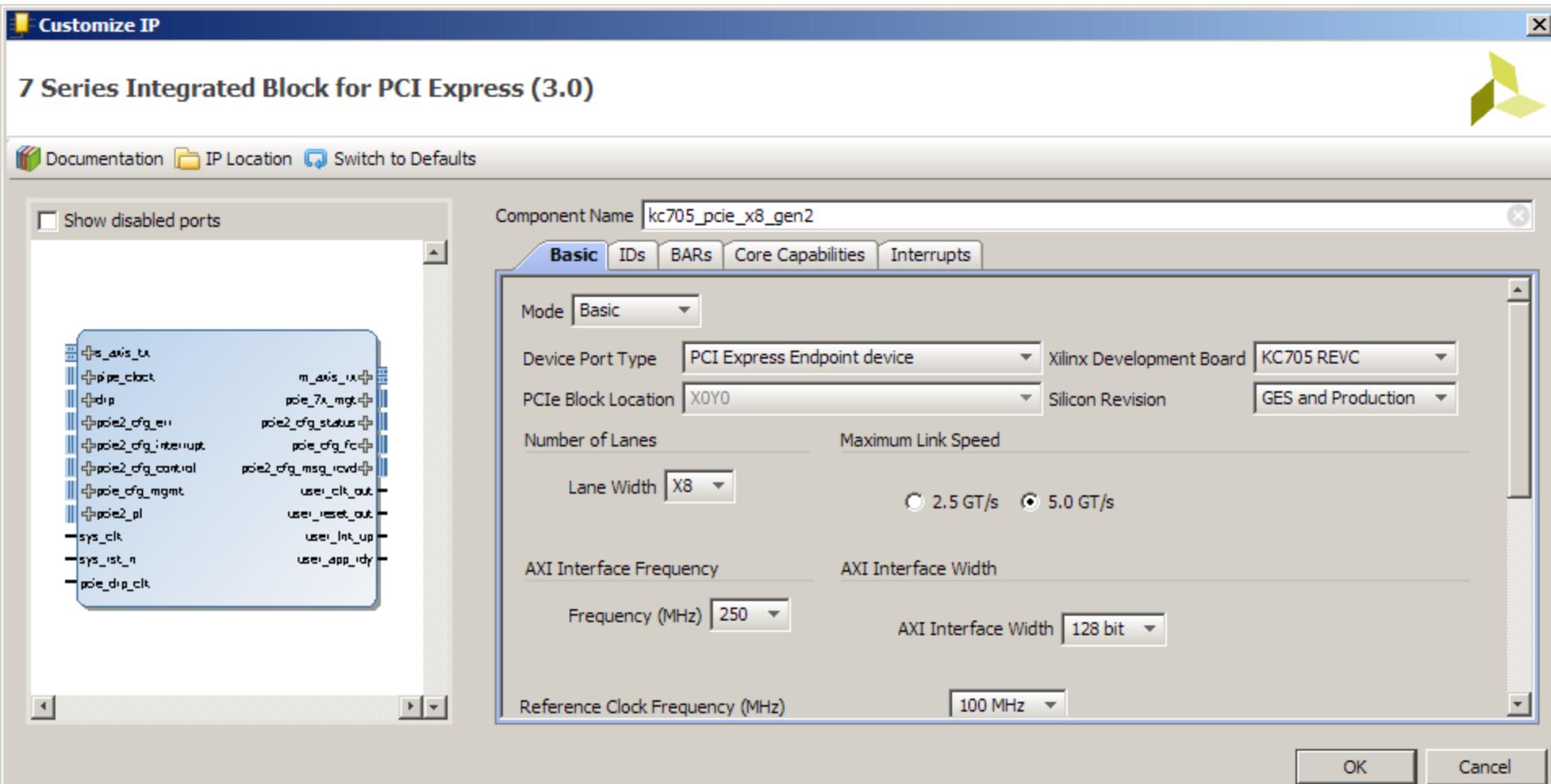
- Set Component name to **kc705\_pcie\_x8\_gen2**
- Set Development Board to **KC705 REVC**
- Set Silicon to **GES and Production**



# Generate x8 Gen 2 PCIe Core

## ► Under the Basic tab,

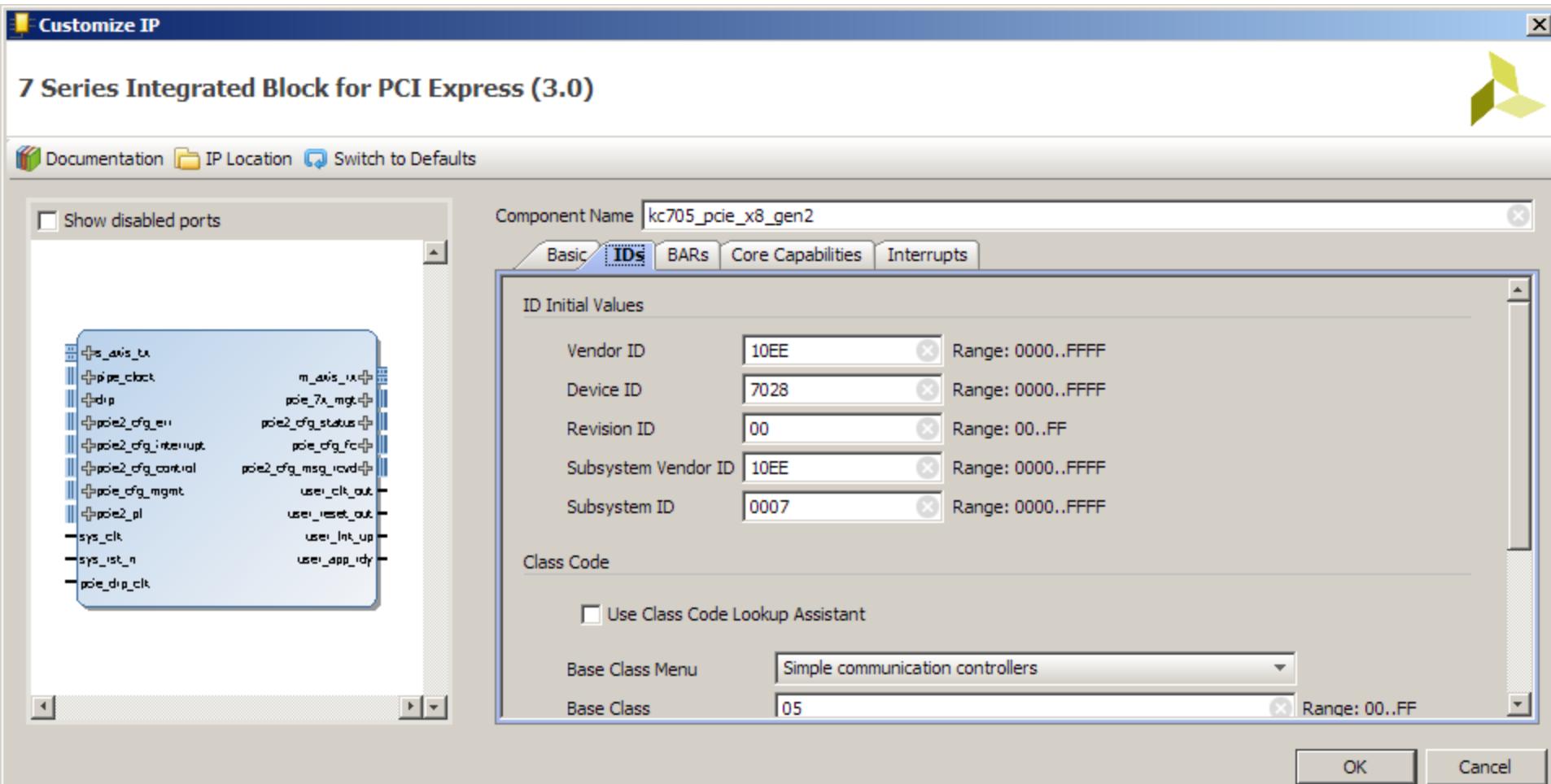
- Set the Lane Width to **X8**
- Set the Max Link Speed to **5 GT/s**
- Set the Ref Clock to **100 MHz**



# Generate x8 Gen 2 PCIe Core

## ► Under the IDs tab, note the ID Initial Values

- Vendor ID = **10EE**; Device ID = **7028**; Revision ID = **00**
- Subsystem Vendor ID = **10EE**; Subsystem ID = **0007**

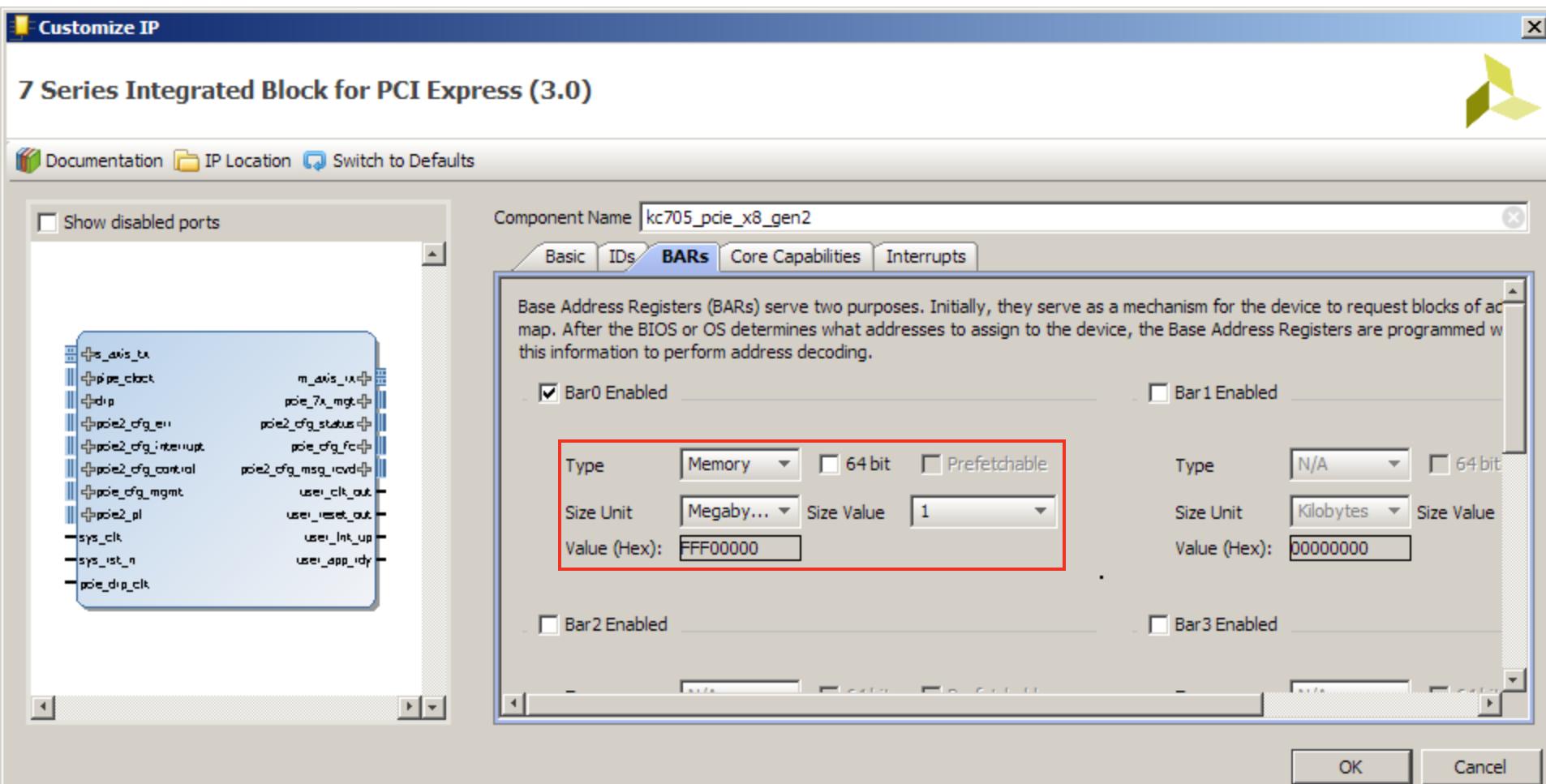


# Generate x8 Gen 2 PCIe Core

► Under the BARs tab, set BAR 0

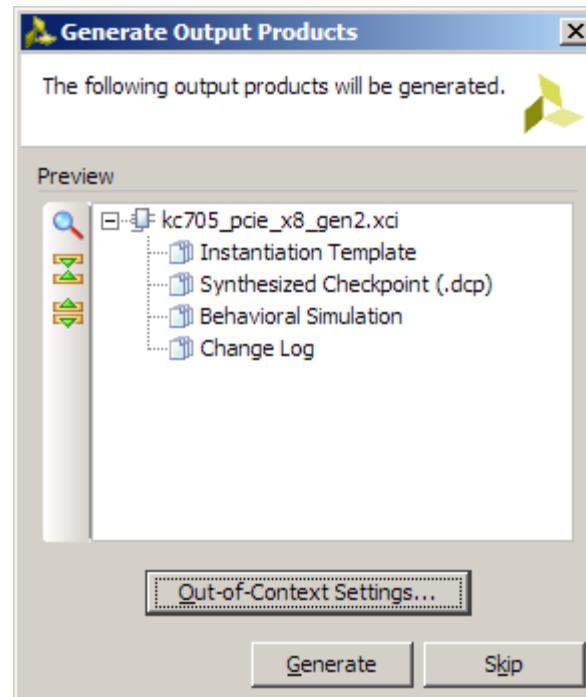
- Set to 1 Megabytes

► Click OK



# Generate x8 Gen 2 PCIe Core

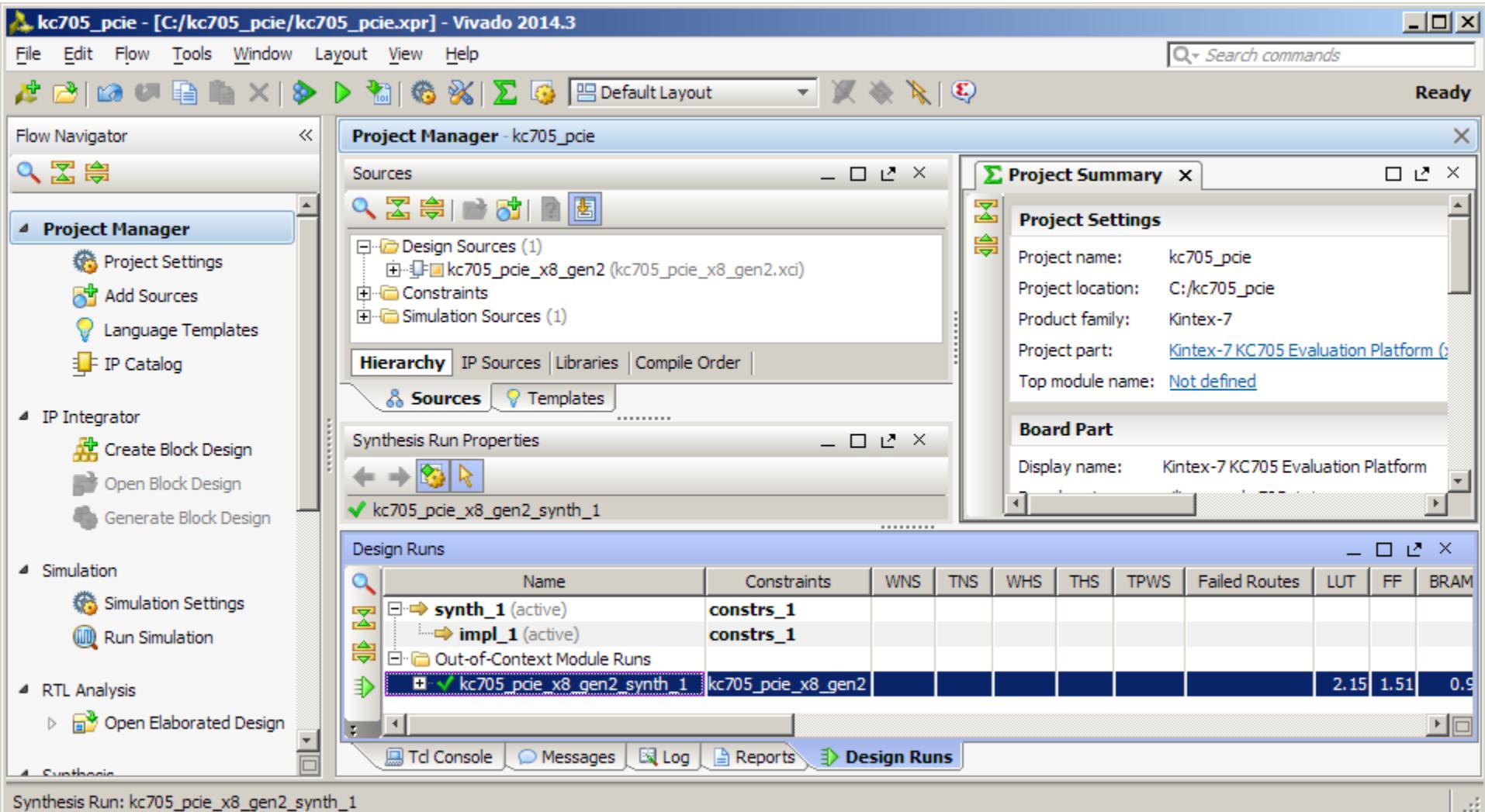
► Click Generate



# Generate x8 Gen 2 PCIe Core

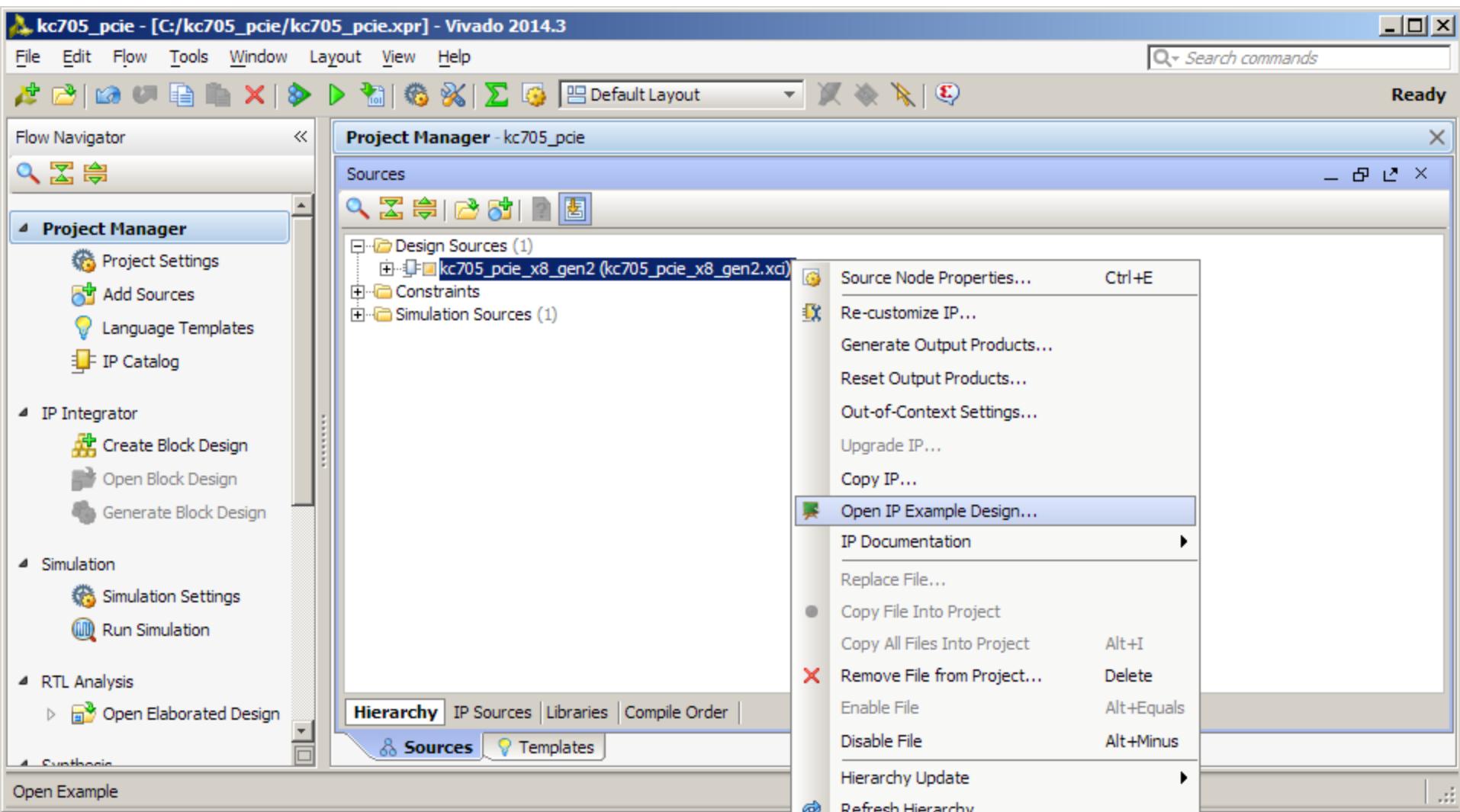
## ► PCIe design appears in Design Sources

- Wait until checkmark appears on kc705\_PCIE\_x8\_gen2\_synth\_1



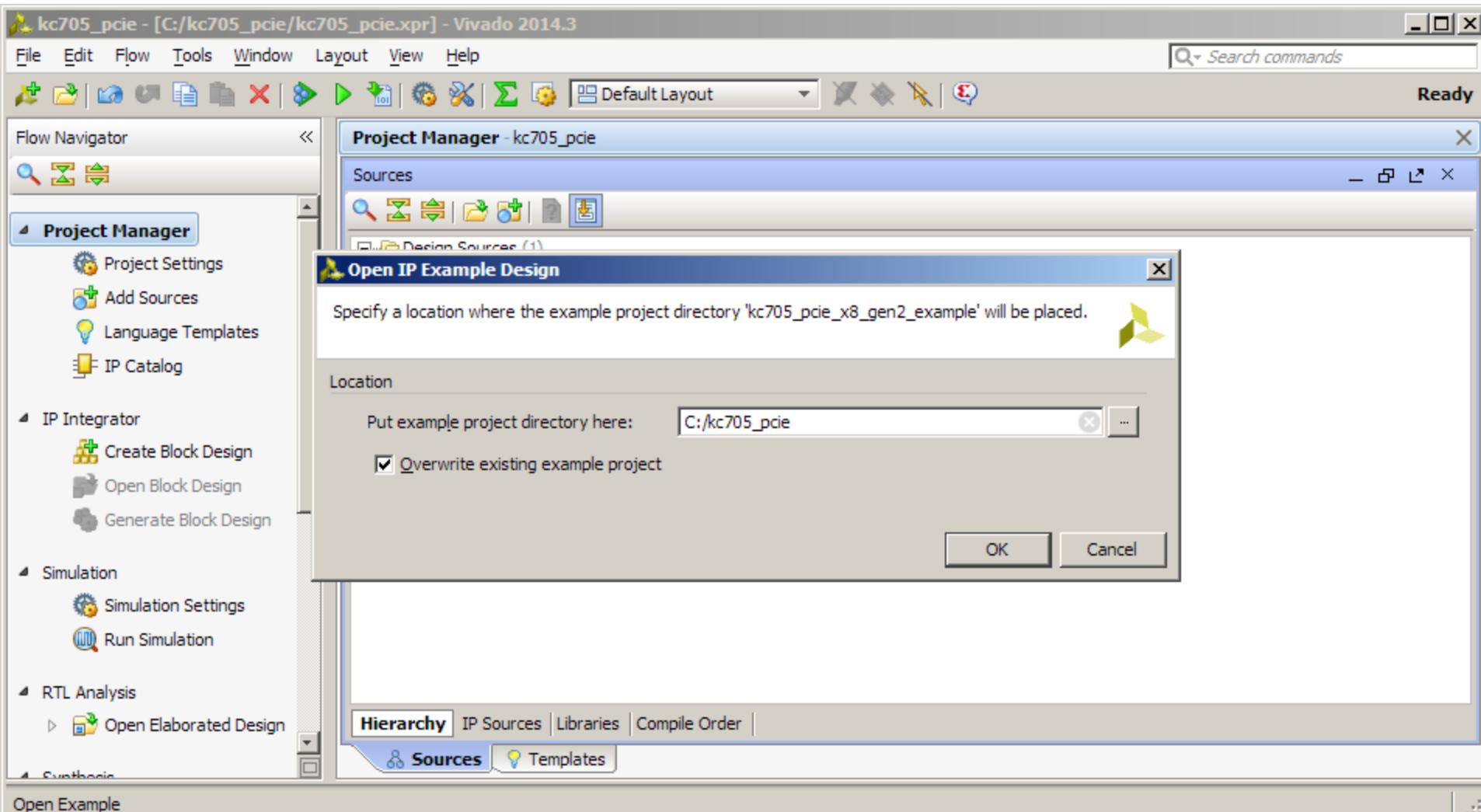
# Generate x8 Gen 2 PCIe Core

- Right-click on `kc705_pcie_x8_gen2` and select Open IP Example Design...



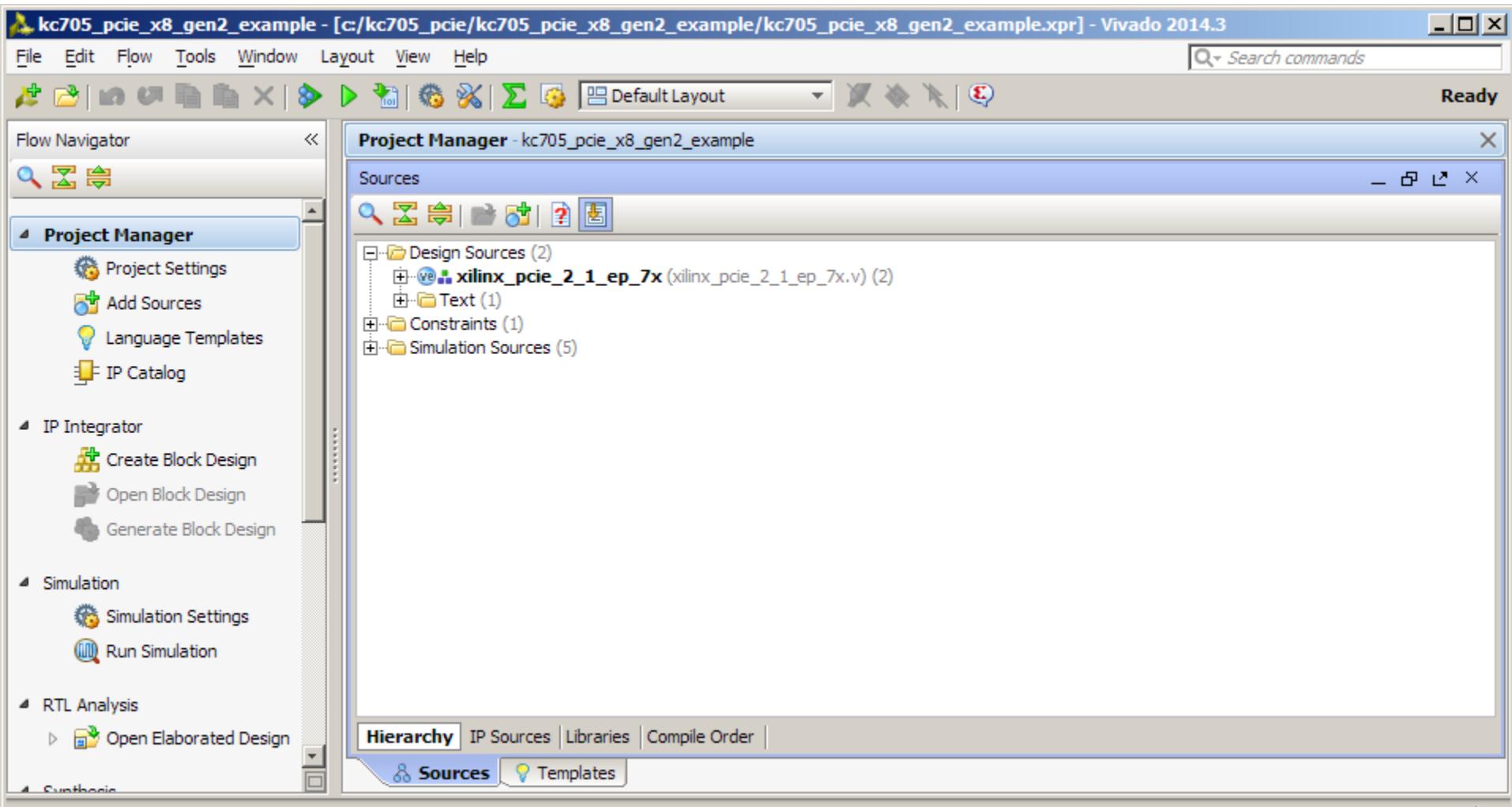
# Generate x8 Gen 2 PCIe Core

► Set the location to C:/kc705\_pcnie and click OK



# Generate x8 Gen 2 PCIe Core

- A new project is created



Note: The original project window can be closed

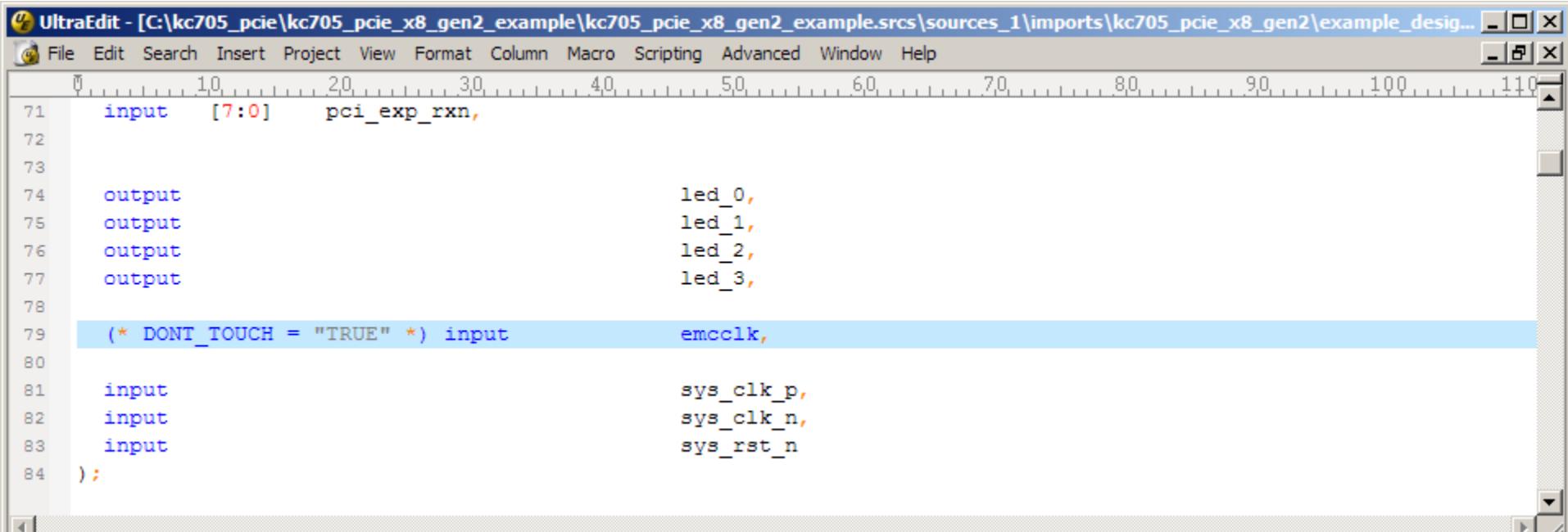
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# Modify PCIe Core

► As per [AR44635](#), the design must be modified

- Open the file: <design path>\kc705\_pcie\_x8\_gen2\_example\kc705\_pcie\_x8\_gen2\_example.srcs\sources\_1\imports\example\_design\xilinx\_pcie\_2\_1\_ep\_7x.v
- Add this line:

(\* DONT\_TOUCH = "TRUE" \*) input emcclk,



The screenshot shows a window of the UltraEdit text editor. The title bar reads "UltraEdit - [C:\kc705\_pcie\kc705\_pcie\_x8\_gen2\_example\kc705\_pcie\_x8\_gen2\_example.srcs\sources\_1\imports\kc705\_pcie\_x8\_gen2\example\_design\xilinx\_pcie\_2\_1\_ep\_7x.v]". The menu bar includes File, Edit, Search, Insert, Project, View, Format, Column, Macro, Scripting, Advanced, Window, and Help. The status bar at the bottom shows line numbers from 71 to 110. The code in the editor is as follows:

```
71  input  [7:0]  pci_exp_rxn,
72
73
74  output          led_0,
75  output          led_1,
76  output          led_2,
77  output          led_3,
78
79  (* DONT_TOUCH = "TRUE" *) input      emcclk,
80
81  input           sys_clk_p,
82  input           sys_clk_n,
83  input           sys_rst_n
84 );
```

Note: Do this after creating the example design

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# Modify PCIe Core

► As per [AR44635](#), the design must be modified

- Open the XDC file: <design path>\kc705\_pcie\_x8\_gen2\_example\kc705\_pcie\_x8\_gen2\_example.srcts\constrs\_1\imports\example\_design\xilinx\_pcie\_7x\_ep\_x8g2\_KC705\_REV.C.xdc
- Add these lines:  
**set\_property IOSTANDARD LVCMOS25 [get\_ports emcclk]**  
**set\_property LOC R24 [get\_ports emcclk]**



The screenshot shows a window of the UltraEdit text editor. The title bar reads "UltraEdit - [C:\kc705\_pcie\kc705\_pcie\_x8\_gen2\_example\kc705\_pcie\_x8\_gen2\_example.srcts\constrs\_1\imports\example\_design\xilinx\_pcie\_7x\_ep\_x8g2\_KC705\_REV.C.xdc]". The menu bar includes File, Edit, Search, Insert, Project, View, Format, Column, Macro, Scripting, Advanced, Window, and Help. The status bar at the bottom shows line numbers from 69 to 110. The main text area contains XDC constraint code. Lines 73 and 74 are highlighted in blue, indicating the new property additions. The code includes sections for User Physical Constraints, Timing Constraints, and a clock creation section.

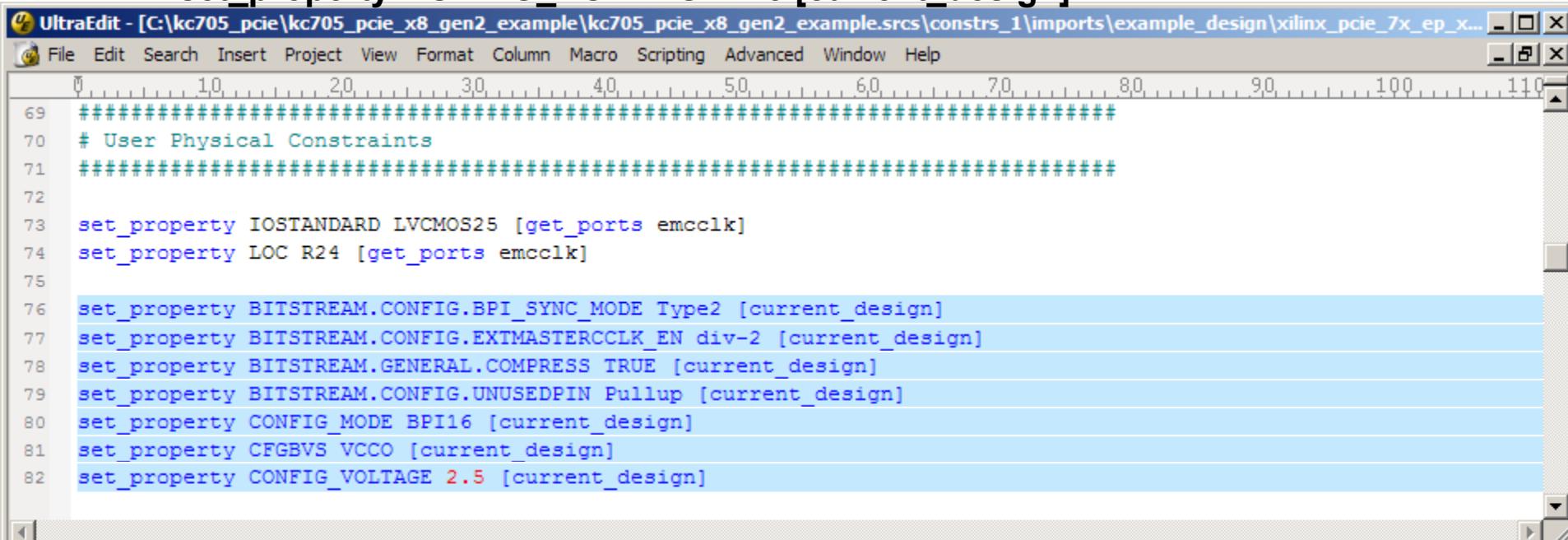
```
69 #####
70 # User Physical Constraints
71 #####
72
73 set_property IOSTANDARD LVCMOS25 [get_ports emcclk]
74 set_property LOC R24 [get_ports emcclk]
75
76 #####
77 # Timing Constraints
78 #####
79 #
80 create_clock -name sys_clk -period 10 [get_ports sys_clk_p]
81 #
82 #
```

# Modify PCIe Core

► As per [UG470](#), [UG899](#), [UG908](#), and [P30 Flash](#) specifications

– In the XDC file, `xilinx_pcie_7x_ep_x8g2_KC705_REV.C.xdc`, add these lines:

```
set_property BITSTREAM.CONFIG.BPI_SYNC_MODE Type2 [current_design]
set_property BITSTREAM.CONFIG.EXTMASTERCCLK_EN div-2 [current_design]
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.UNUSEDPIN Pullup [current_design]
set_property CONFIG_MODE BPI16 [current_design]
set_property CFGBVS VCCO [current_design]
set_property CONFIG_VOLTAGE 2.5 [current_design]
```



The screenshot shows a window of the UltraEdit text editor. The title bar reads "UltraEdit - [C:\kc705\_pcie\kc705\_pcie\_x8\_gen2\_example\kc705\_pcie\_x8\_gen2\_example.srcc\constrs\_1\imports\example\_design\xilinx\_pcie\_7x\_ep\_x...". The menu bar includes File, Edit, Search, Insert, Project, View, Format, Column, Macro, Scripting, Advanced, Window, and Help. The status bar at the bottom shows line numbers from 0 to 110. The main text area contains the following XDC configuration code:

```
#####
# User Physical Constraints
#####

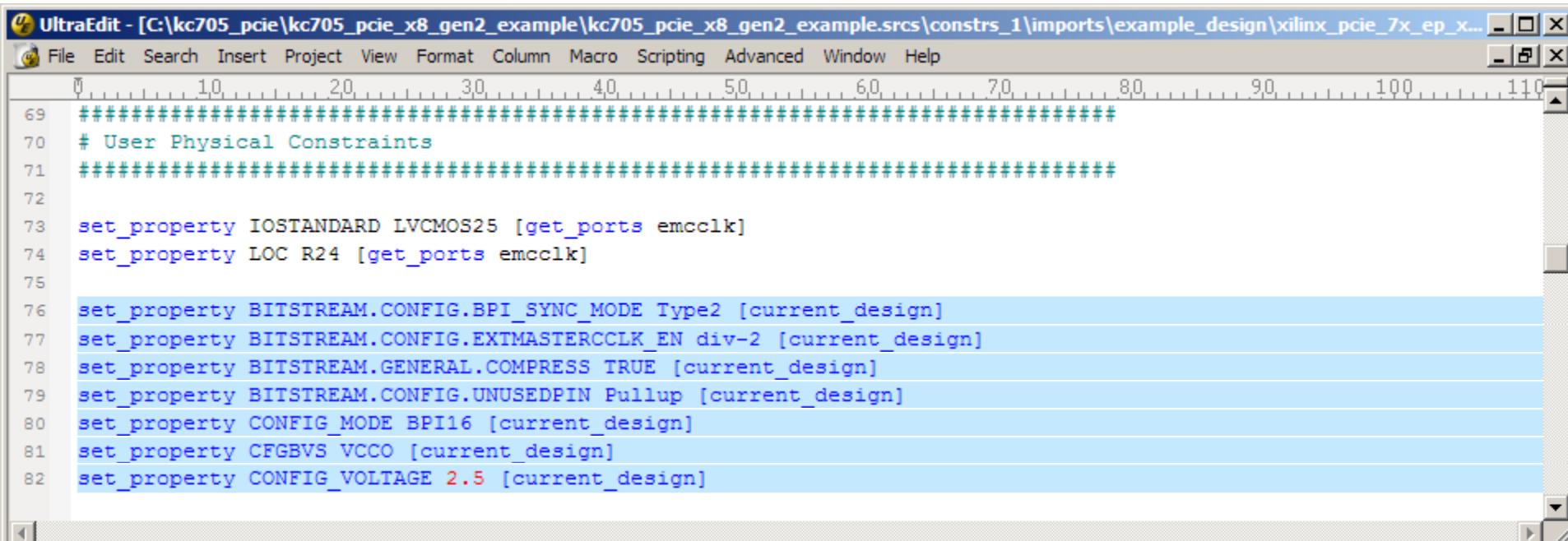
set_property IOSTANDARD LVCMOS25 [get_ports emcclk]
set_property LOC R24 [get_ports emcclk]

set_property BITSTREAM.CONFIG.BPI_SYNC_MODE Type2 [current_design]
set_property BITSTREAM.CONFIG.EXTMASTERCCLK_EN div-2 [current_design]
set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
set_property BITSTREAM.CONFIG.UNUSEDPIN Pullup [current_design]
set_property CONFIG_MODE BPI16 [current_design]
set_property CFGBVS VCCO [current_design]
set_property CONFIG_VOLTAGE 2.5 [current_design]
```

# Modify PCIe Core

## ► Details on the XDC constraints :

- P30T Maximum Frequency: 52 MHz; KC705 EMCCLK Frequency: 66 MHz
- **BITSTREAM.CONFIG.BPI\_SYNC\_MODE Type2**: For Numonyx P30 Family
- **BITSTREAM.CONFIG.EXTMMASTERCCLK\_EN div-2**: Sets the EMCCLK in the FPGA to divide by 2, which meets the P30T Maximum Frequency specification
- **BITSTREAM.GENERAL.COMPRESS TRUE**: Shrinks the bitstream



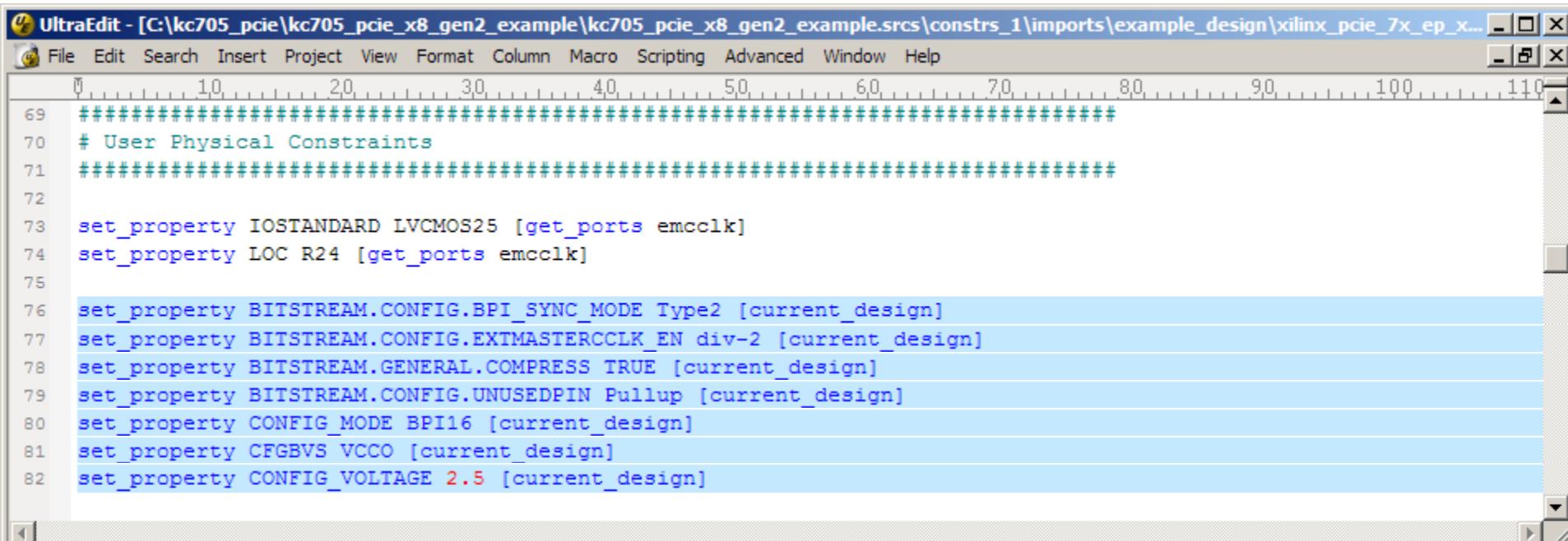
The screenshot shows a code editor window titled "UltraEdit - [C:\kc705\_pcie\kc705\_pcie\_x8\_gen2\_example\kc705\_pcie\_x8\_gen2\_example.srcts\constrs\_1\imports\example\_design\xilinx\_pcie\_7x\_ep\_x...]" with a ruler at the top. The code is written in XDC (Xilinx Design Constraints) and includes the following properties:

```
69 #####  
70 # User Physical Constraints  
71 #####  
72  
73 set_property IOSTANDARD LVCMOS25 [get_ports emcclk]  
74 set_property LOC R24 [get_ports emcclk]  
75  
76 set_property BITSTREAM.CONFIG.BPI_SYNC_MODE Type2 [current_design]  
77 set_property BITSTREAM.CONFIG.EXTMMASTERCCLK_EN div-2 [current_design]  
78 set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]  
79 set_property BITSTREAM.CONFIG.UNUSEDPIN Pullup [current_design]  
80 set_property CONFIG_MODE BPI16 [current_design]  
81 set_property CFGBVS VCCO [current_design]  
82 set_property CONFIG_VOLTAGE 2.5 [current_design]
```

# Modify PCIe Core

## ► Details on the XDC constraints :

- **BITSTREAM.CONFIG.UNUSEDPIN Pullup**: Sets unused pins to be pulled up
- **CONFIG\_MODE BPI16**: The BPI is 16 bits wide
- **CFGVBVS VCCO**: Set to VCCO when CONFIG\_VOLTAGE is either 2.5 or 3.3 V
- **CONFIG\_VOLTAGE 2.5**: The KC705 Configuration Bank (Bank 0) voltage is connected to 2.5 V

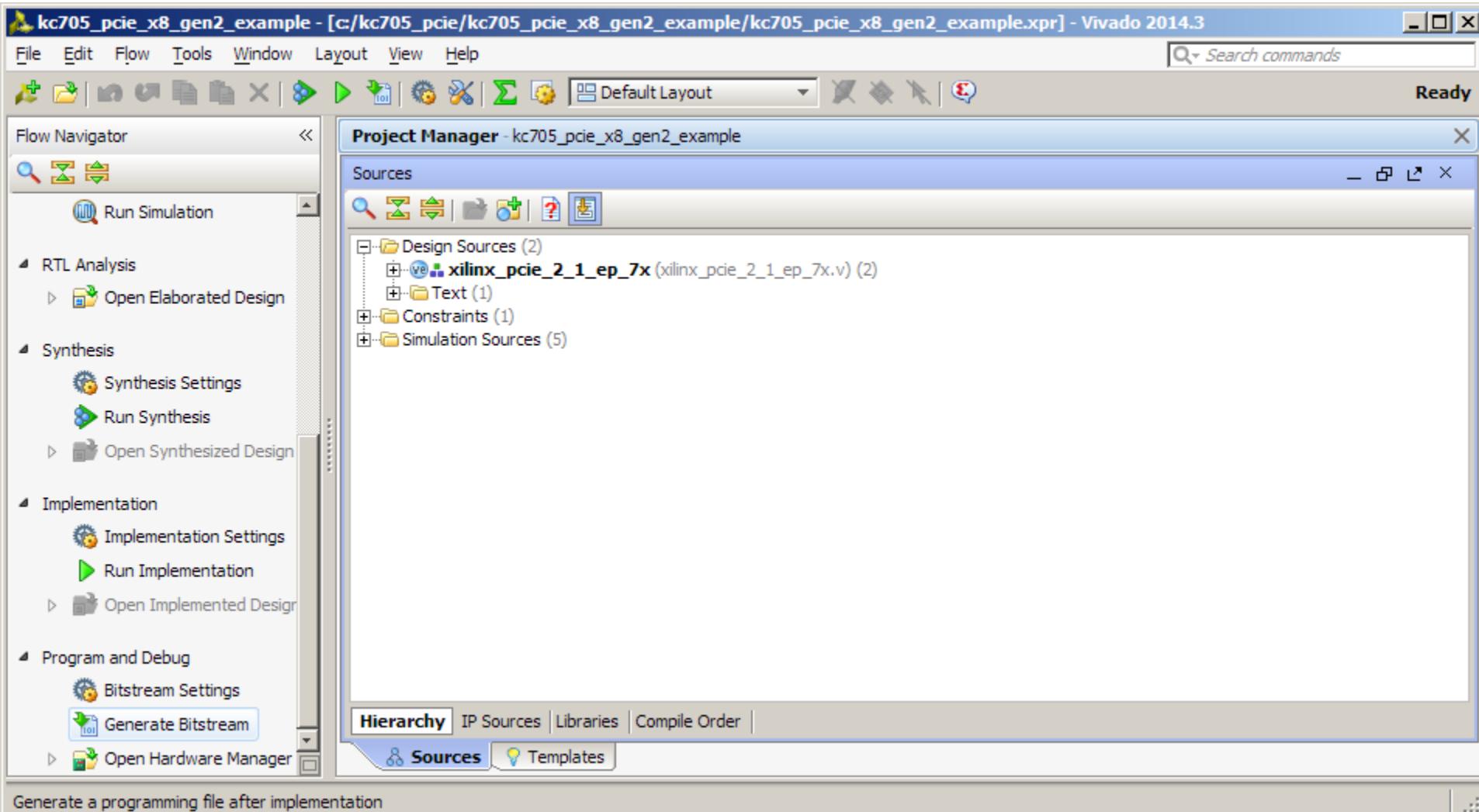


The screenshot shows a code editor window titled "UltraEdit - [C:\kc705\_PCIE\kc705\_PCIE\_x8\_gen2\_example\kc705\_PCIE\_x8\_gen2\_example.srcs\constrs\_1\imports\example\_design\xilinx\_PCIE\_7x\_EP.xdc]". The code is an XDC (Xilinx Design Constraints) file. It starts with a header block, followed by a section for physical constraints, and then a series of set\_property commands defining various configuration parameters. The code is color-coded for syntax highlighting.

```
UltraEdit - [C:\kc705_PCIE\kc705_PCIE_x8_gen2_example\kc705_PCIE_x8_gen2_example.srcs\constrs_1\imports\example_design\xilinx_PCIE_7x_EP.xdc]
File Edit Search Insert Project View Format Column Macro Scripting Advanced Window Help
10 20 30 40 50 60 70 80 90 100 110
69 ##### User Physical Constraints #####
70 # User Physical Constraints
71 #####
72
73 set_property IOSTANDARD LVCMOS25 [get_ports emcclk]
74 set_property LOC R24 [get_ports emcclk]
75
76 set_property BITSTREAM.CONFIG.BPI_SYNC_MODE Type2 [current_design]
77 set_property BITSTREAM.CONFIG.EXTMASTERCCLK_EN div-2 [current_design]
78 set_property BITSTREAM.GENERAL.COMPRESS TRUE [current_design]
79 set_property BITSTREAM.CONFIG.UNUSEDPIN Pullup [current_design]
80 set_property CONFIG_MODE BPI16 [current_design]
81 set_property CFGVBVS VCCO [current_design]
82 set_property CONFIG_VOLTAGE 2.5 [current_design]
```

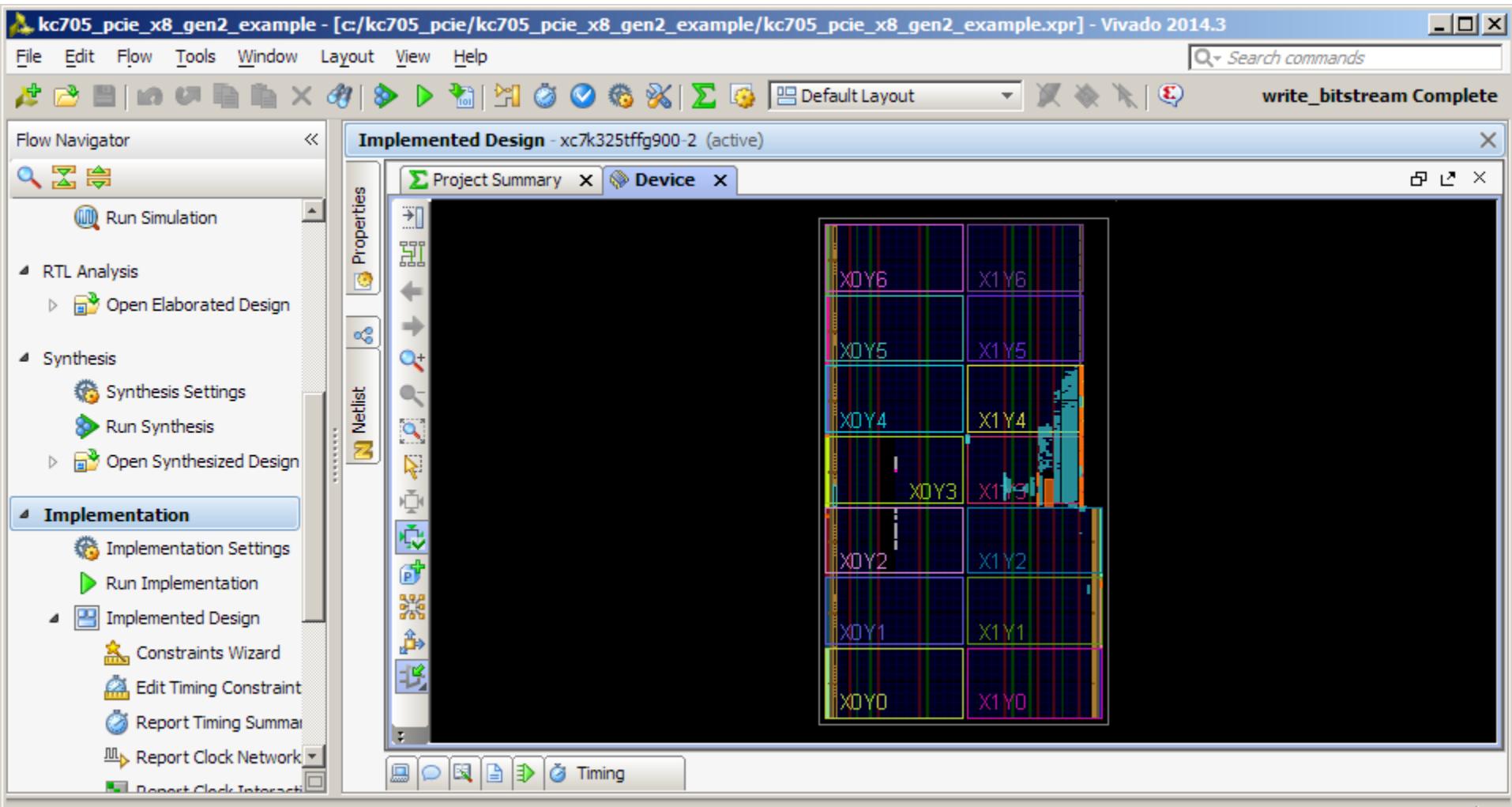
# Compile Example Design

► Click on Generate Bitstream



# Compile Example Design

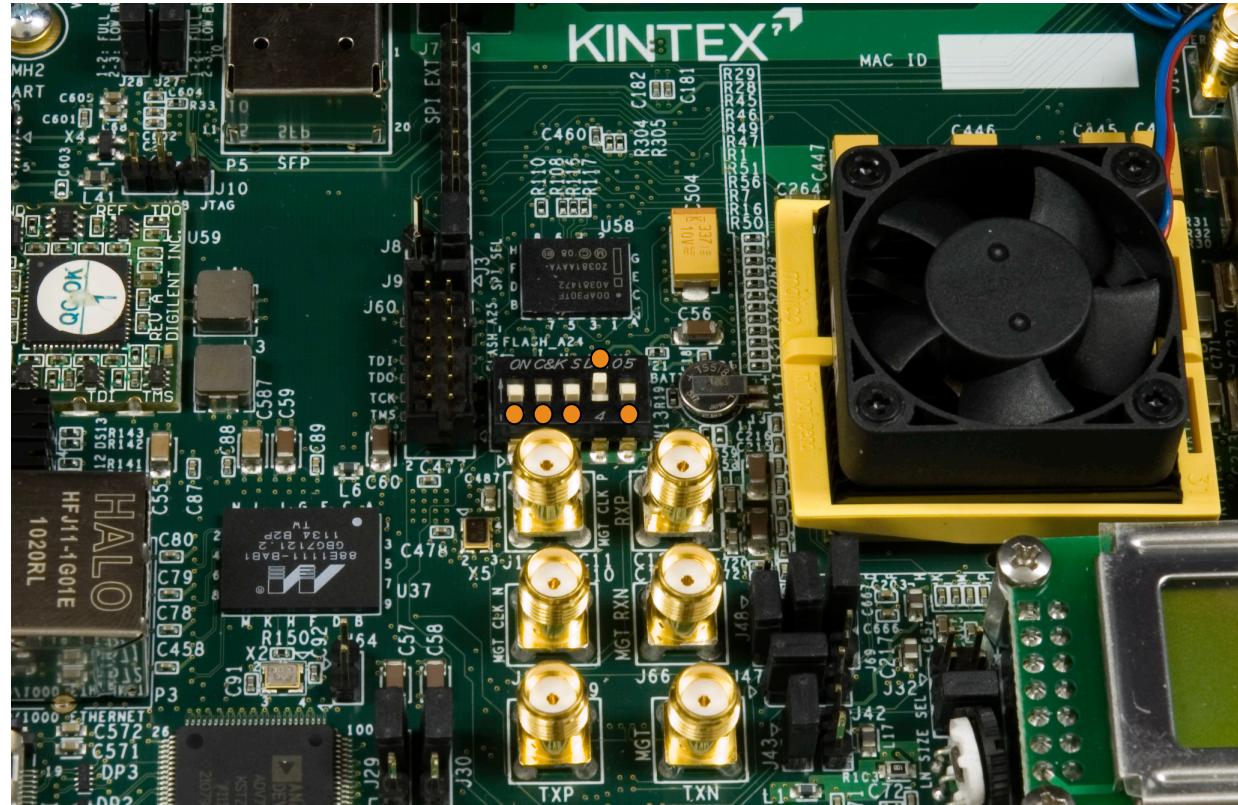
## ► Open and view the Implemented Design



# Hardware Setup

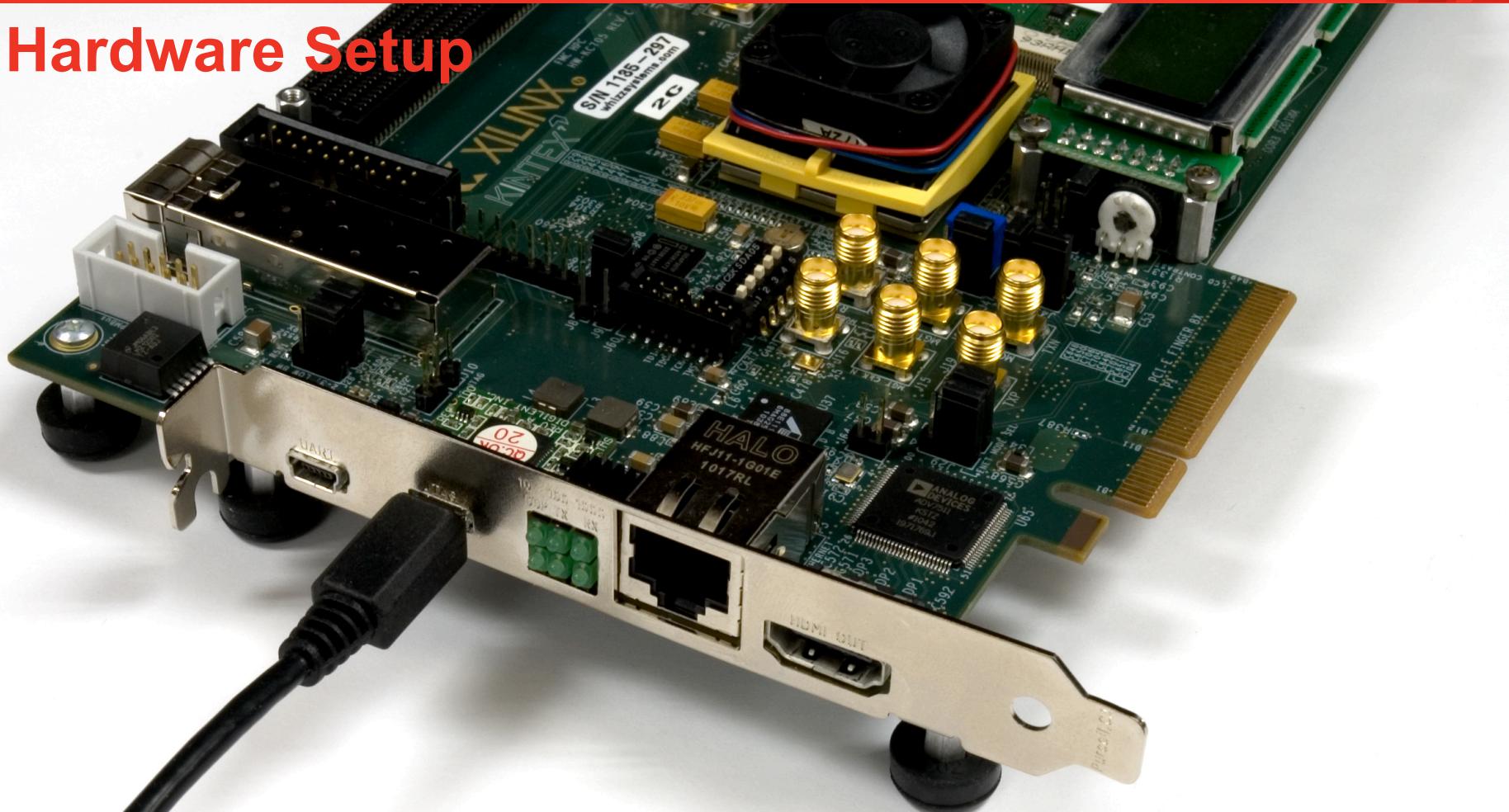
## ► Set SW13 to 00010 (1 = on, Position 1 → Position 5)

- This enables Master BPI configuration from Slot #1
  - Flash A25, A24 = 00
  - FPGA mode pins M[2:0] = 010



**Note:** Presentation applies to the KC705

# Hardware Setup

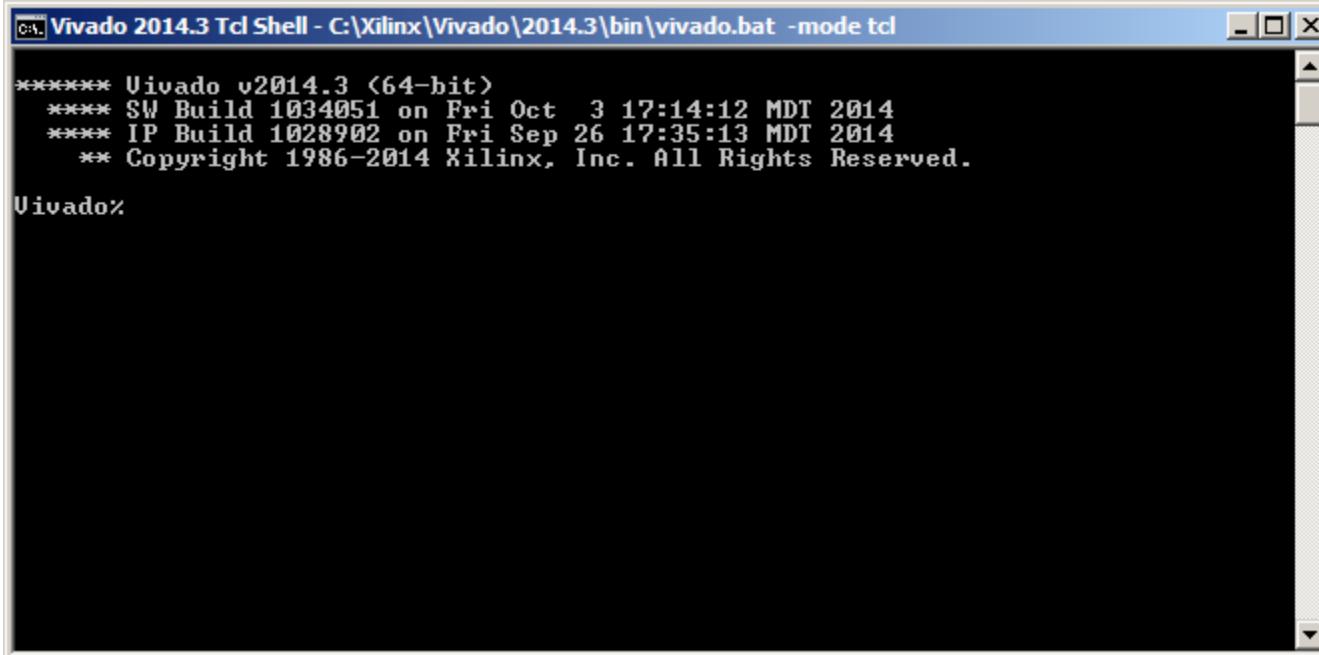


- ▶ **Connect a USB Type-A to Micro-B cable to the USB JTAG (Digilent) connector on the KC705 board**
  - Connect this cable to your PC
  - Power on the KC705 board

# Generate PCIe MCS File

## ► Open a Vivado Tcl Shell:

**Start → All Programs → Xilinx Design Tools → Vivado 2014.3 →  
Vivado 2014.3 Tcl Shell**



Vivado 2014.3 Tcl Shell - C:\Xilinx\Vivado\2014.3\bin\vivado.bat -mode tcl

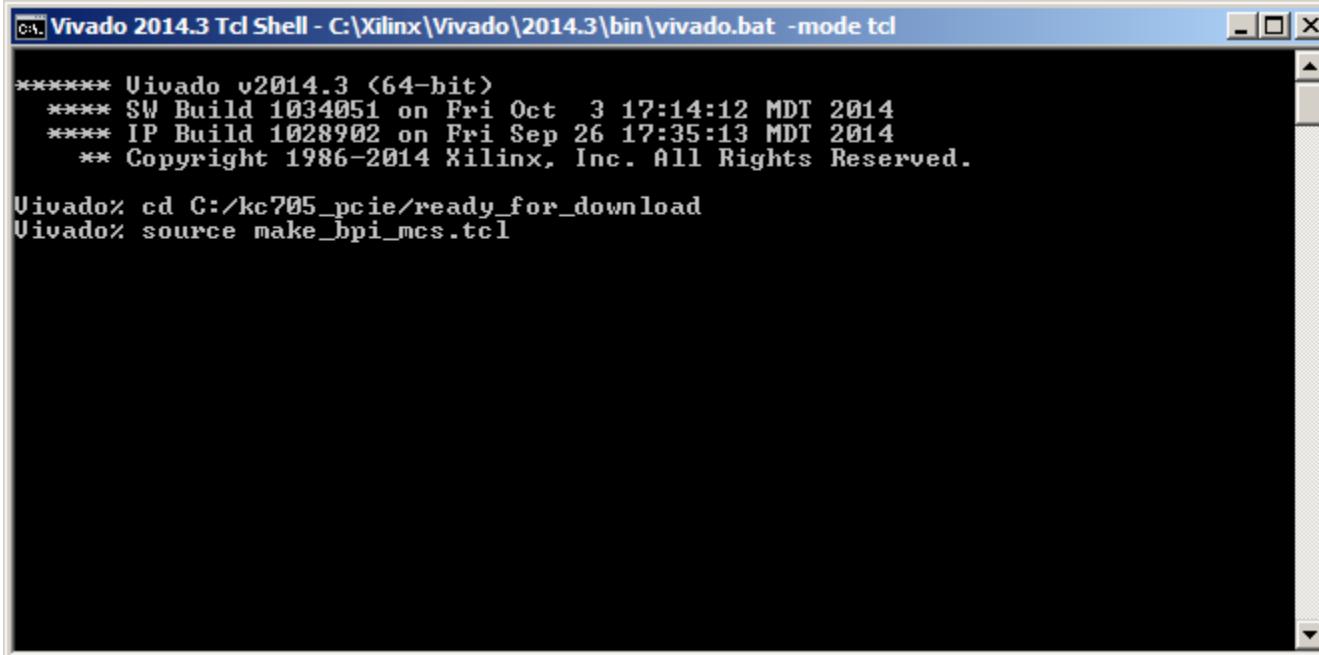
```
***** Vivado v2014.3 (64-bit)
***** SW Build 1034051 on Fri Oct  3 17:14:12 MDT 2014
***** IP Build 1028902 on Fri Sep 26 17:35:13 MDT 2014
** Copyright 1986-2014 Xilinx, Inc. All Rights Reserved.

Vivado%
```

# Generate PCIe MCS File

- In the Vivado Tcl Shell type:

```
cd C:/kc705_pcie/ready_for_download  
source make_bpi_mcs.tcl
```



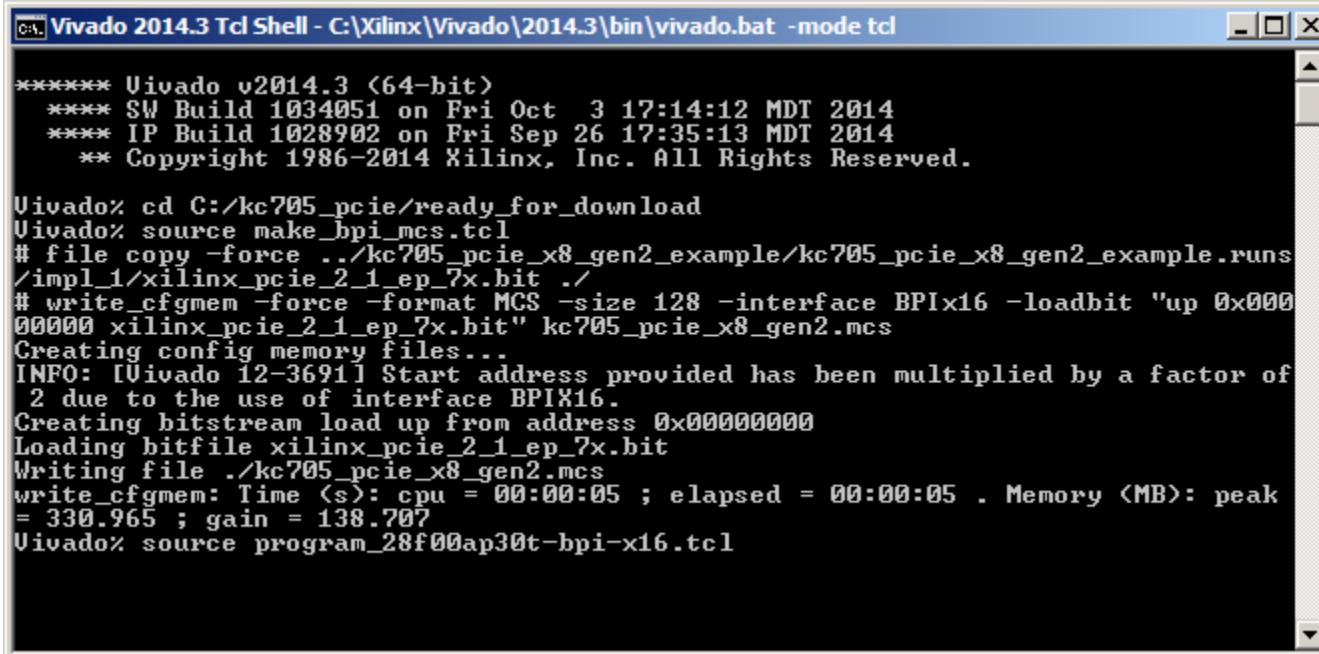
The screenshot shows a Windows command-line interface window titled "Vivado 2014.3 Tcl Shell - C:\Xilinx\Vivado\2014.3\bin\vivado.bat -mode tcl". The window displays the following text:

```
***** Vivado v2014.3 (64-bit)  
***** SW Build 1034051 on Fri Oct  3 17:14:12 MDT 2014  
***** IP Build 1028902 on Fri Sep 26 17:35:13 MDT 2014  
** Copyright 1986-2014 Xilinx, Inc. All Rights Reserved.  
Vivado> cd C:/kc705_pcie/ready_for_download  
Vivado> source make_bpi_mcs.tcl
```

# Program BPI Flash with PCIe Design

- In the Vivado Tcl Shell type:

```
source program_28f00ap30t-bpi-x16.tcl
```



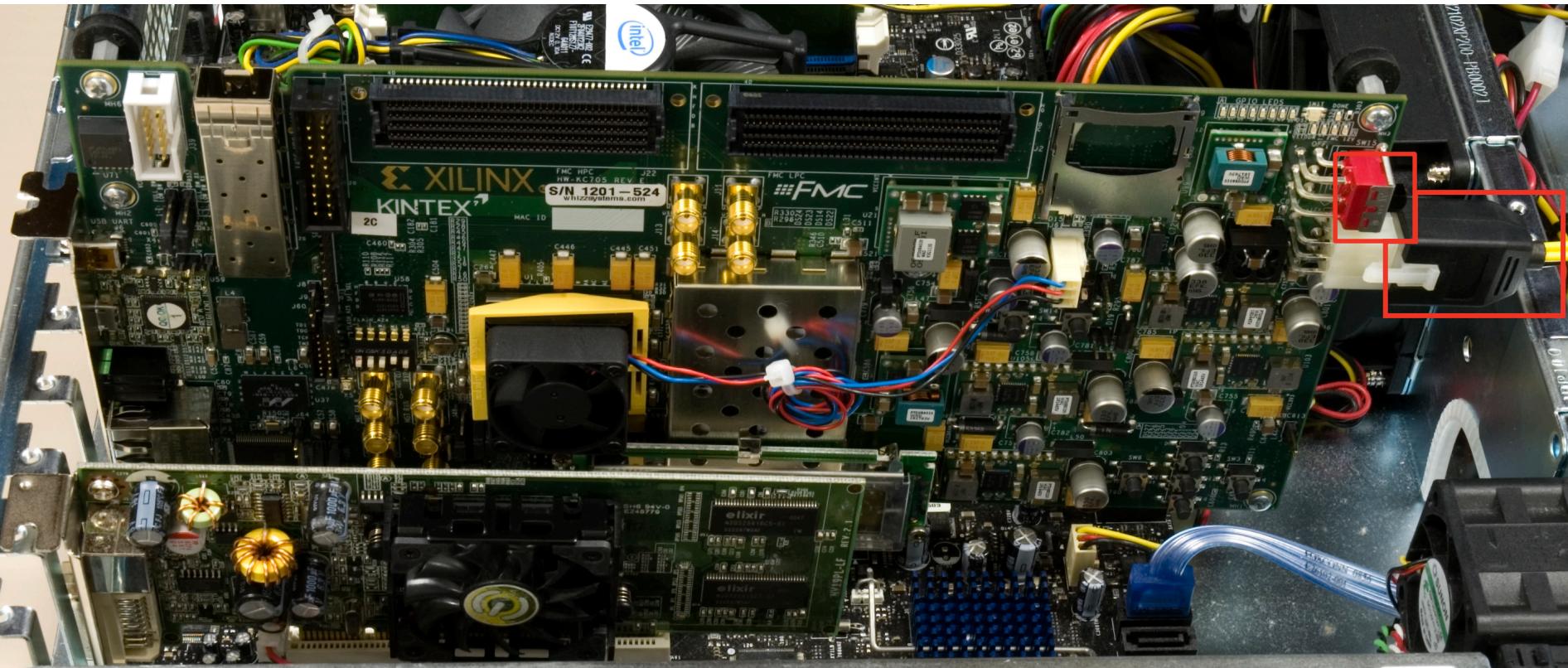
```
***** Vivado v2014.3 (64-bit)
***** SW Build 1034051 on Fri Oct  3 17:14:12 MDT 2014
***** IP Build 1028902 on Fri Sep 26 17:35:13 MDT 2014
** Copyright 1986-2014 Xilinx, Inc. All Rights Reserved.

Vivado> cd C:/kc705_pcie/ready_for_download
Vivado> source make_bpi_mcs.tcl
# file copy -force ../kc705_pcie_x8_gen2_example/kc705_pcie_x8_gen2_example.runs
/impl_1/xilinx_pcie_2_1_ep_7x.bit ./
# write_cfm -force -format MCS -size 128 -interface BPIx16 -loadbit "up 0x000
00000 xilinx_pcie_2_1_ep_7x.bit" kc705_pcie_x8_gen2.mcs
Creating config memory files...
INFO: [Vivado 12-3691] Start address provided has been multiplied by a factor of
2 due to the use of interface BPIX16.
Creating bitstream load up from address 0x00000000
Loading bitfile xilinx_pcie_2_1_ep_7x.bit
Writing file ./kc705_pcie_x8_gen2.mcs
write_cfm: Time <s>: cpu = 00:00:05 ; elapsed = 00:00:05 . Memory <MB>: peak
= 330.965 ; gain = 138.707
Vivado> source program_28f00ap30t-bpi-x16.tcl
```

# Hardware Setup

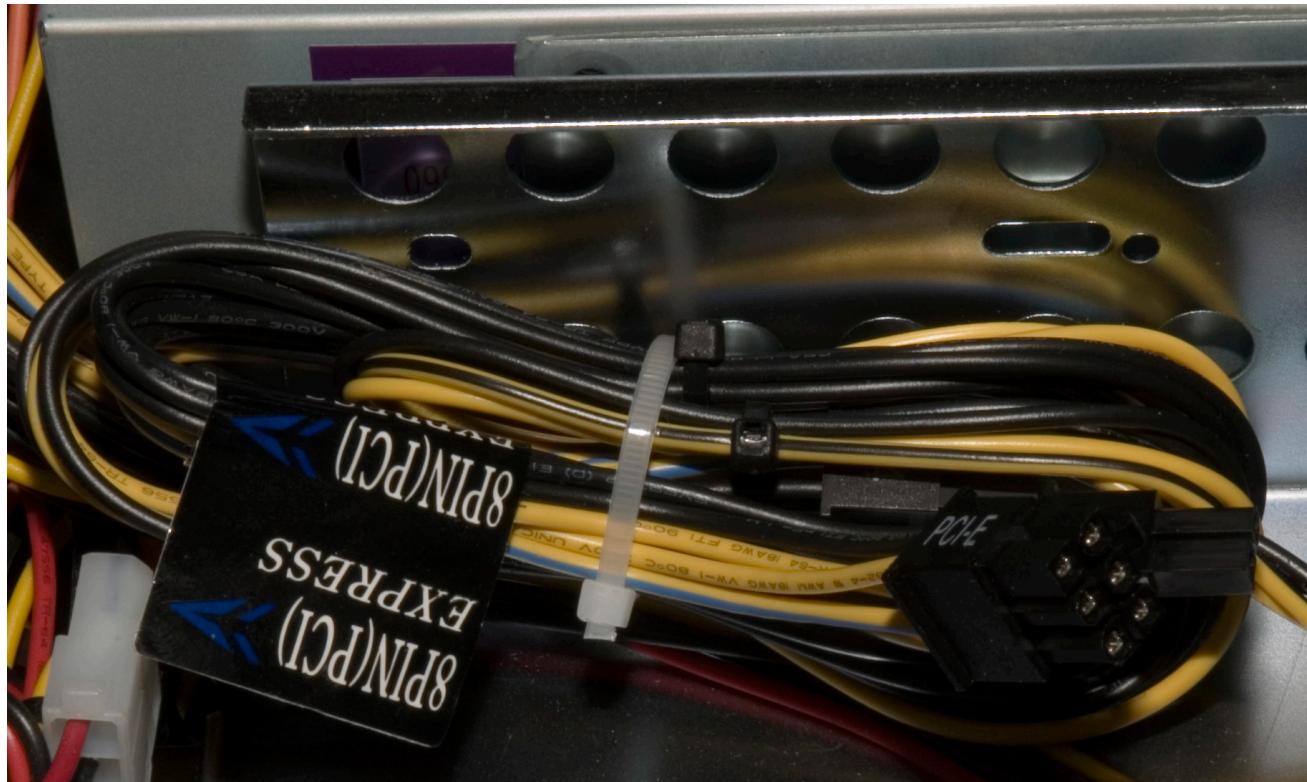
## ► Insert the KC705 Board into a PCIe slot

- Use the included PC Power adapter; turn on Power Switch



# Hardware Setup

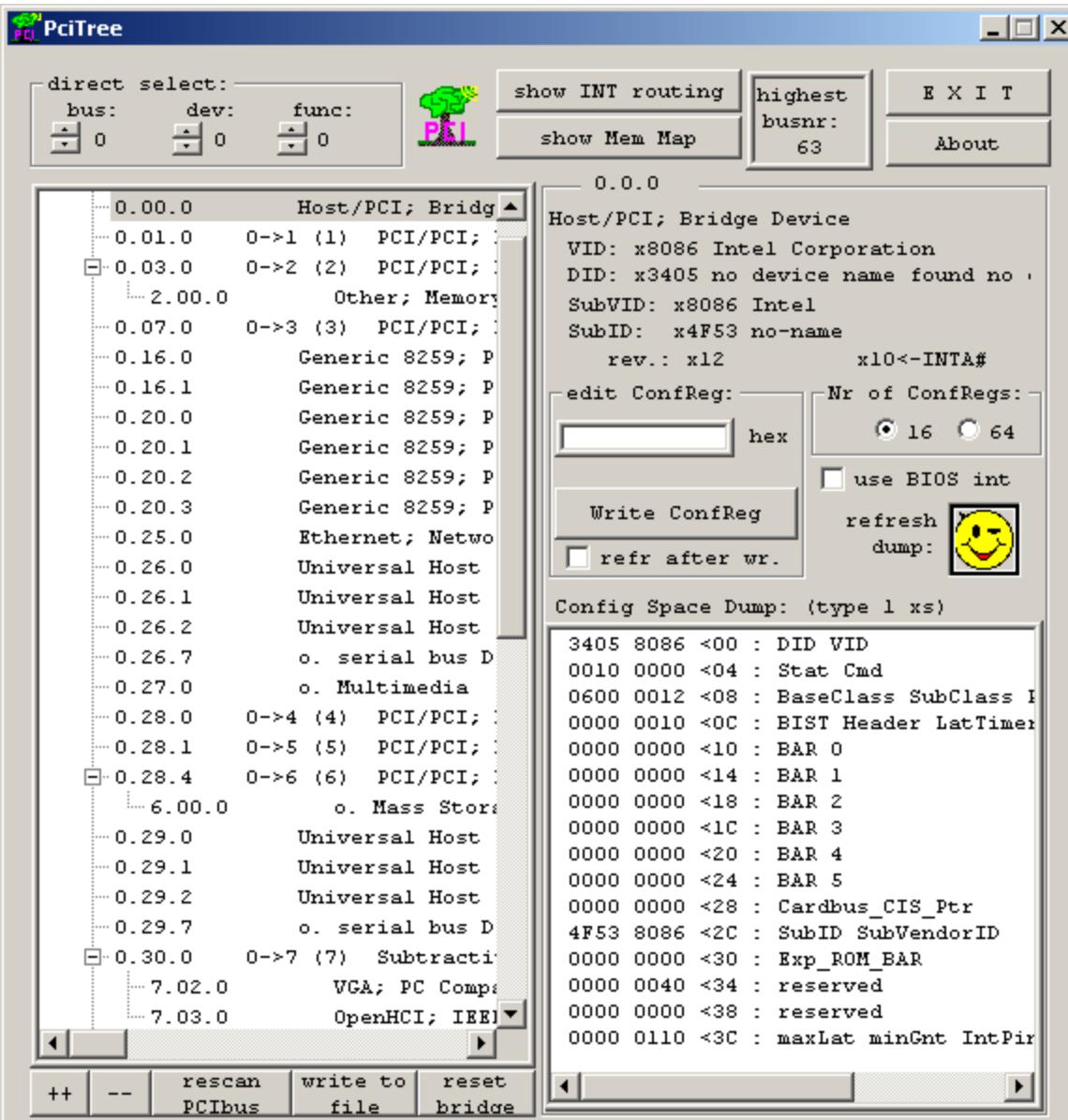
- Do not use the PCIe connector from the PC power supply



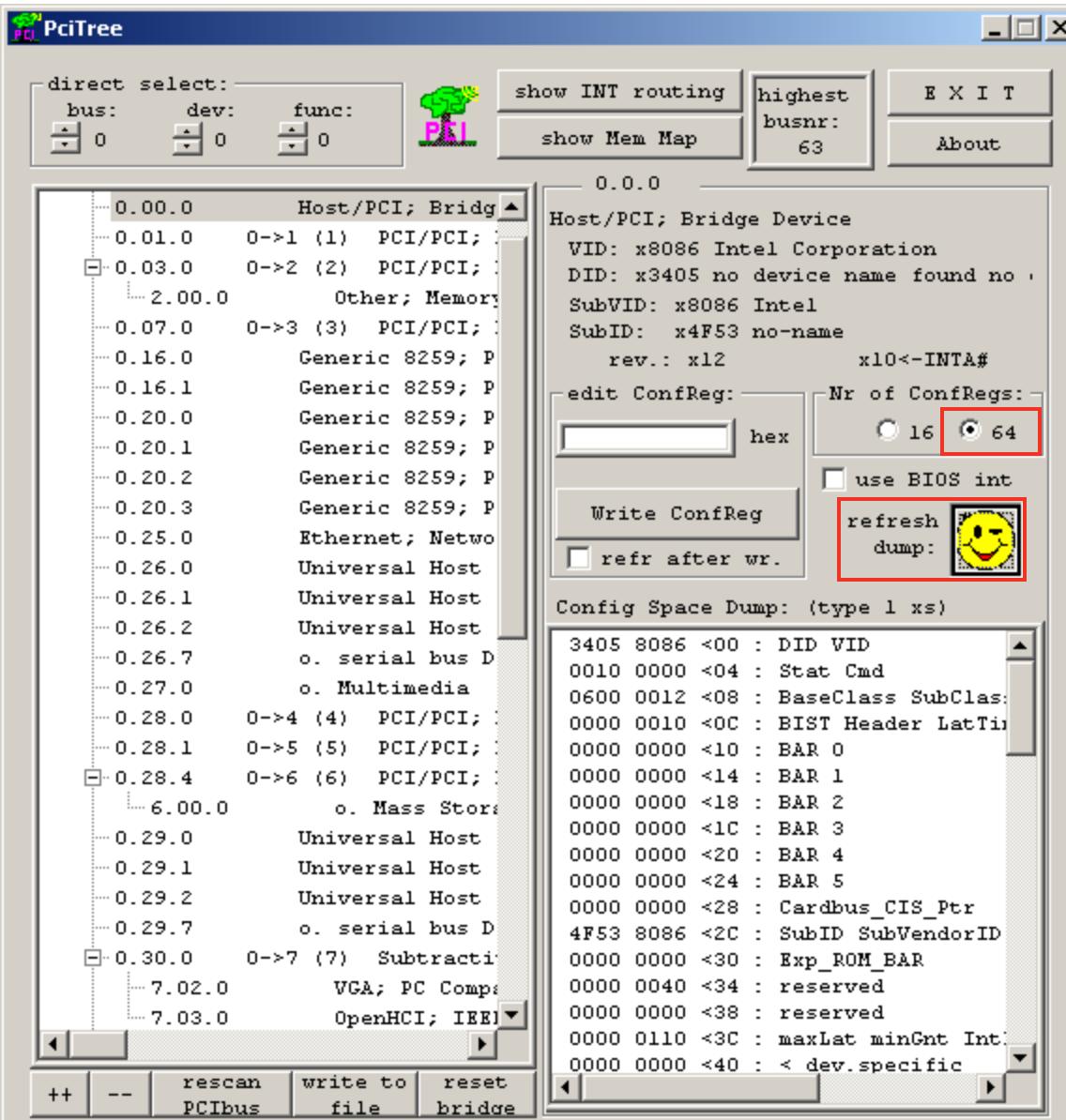
# Running the PCIe x8 Gen 2 Design

► Power on the PC

► Start PciTree



# Running the PCIe x8 Gen 2 Design



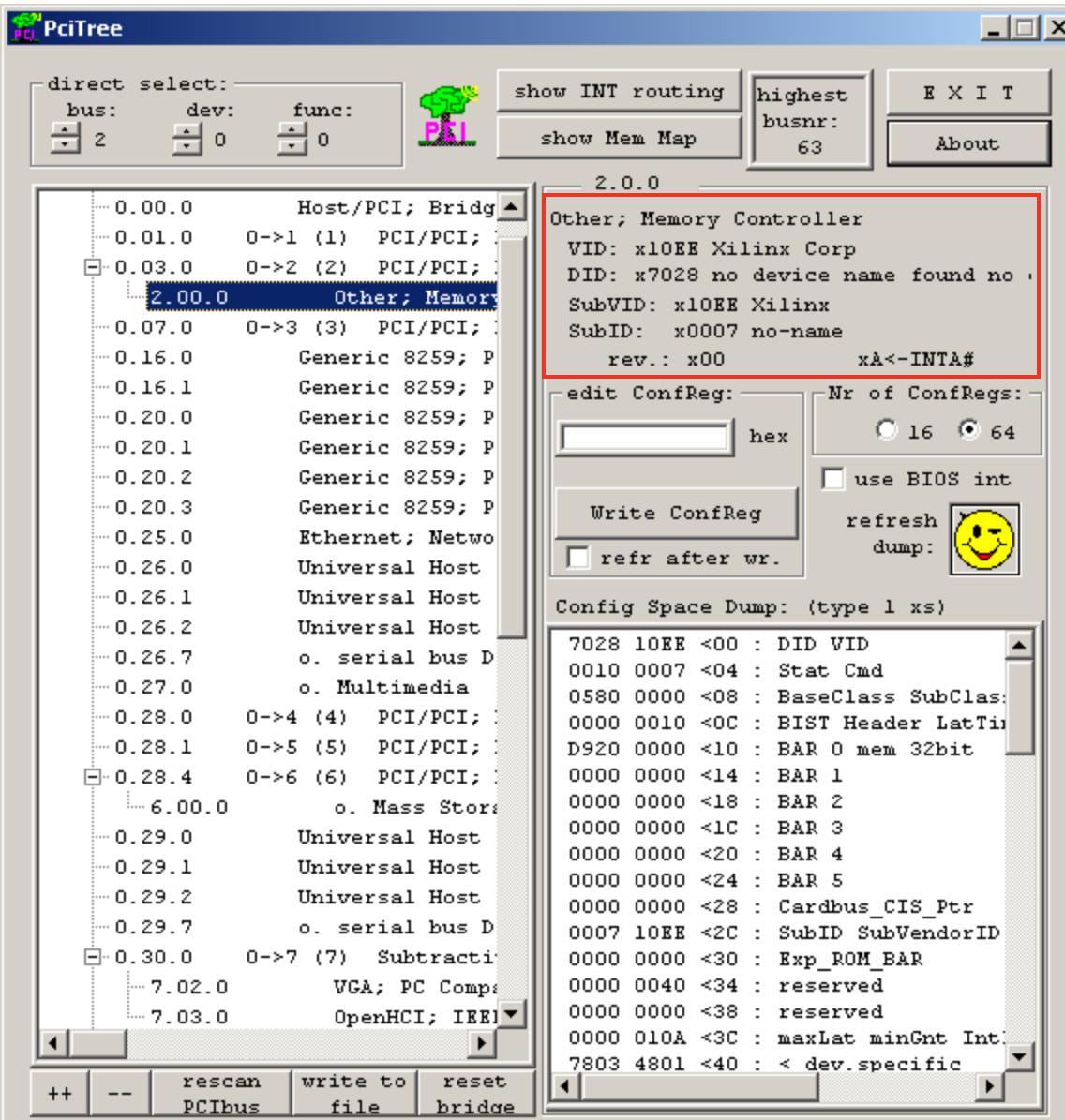
➤ Set Number of Configuration Registers to 64

➤ Click on Refresh dump

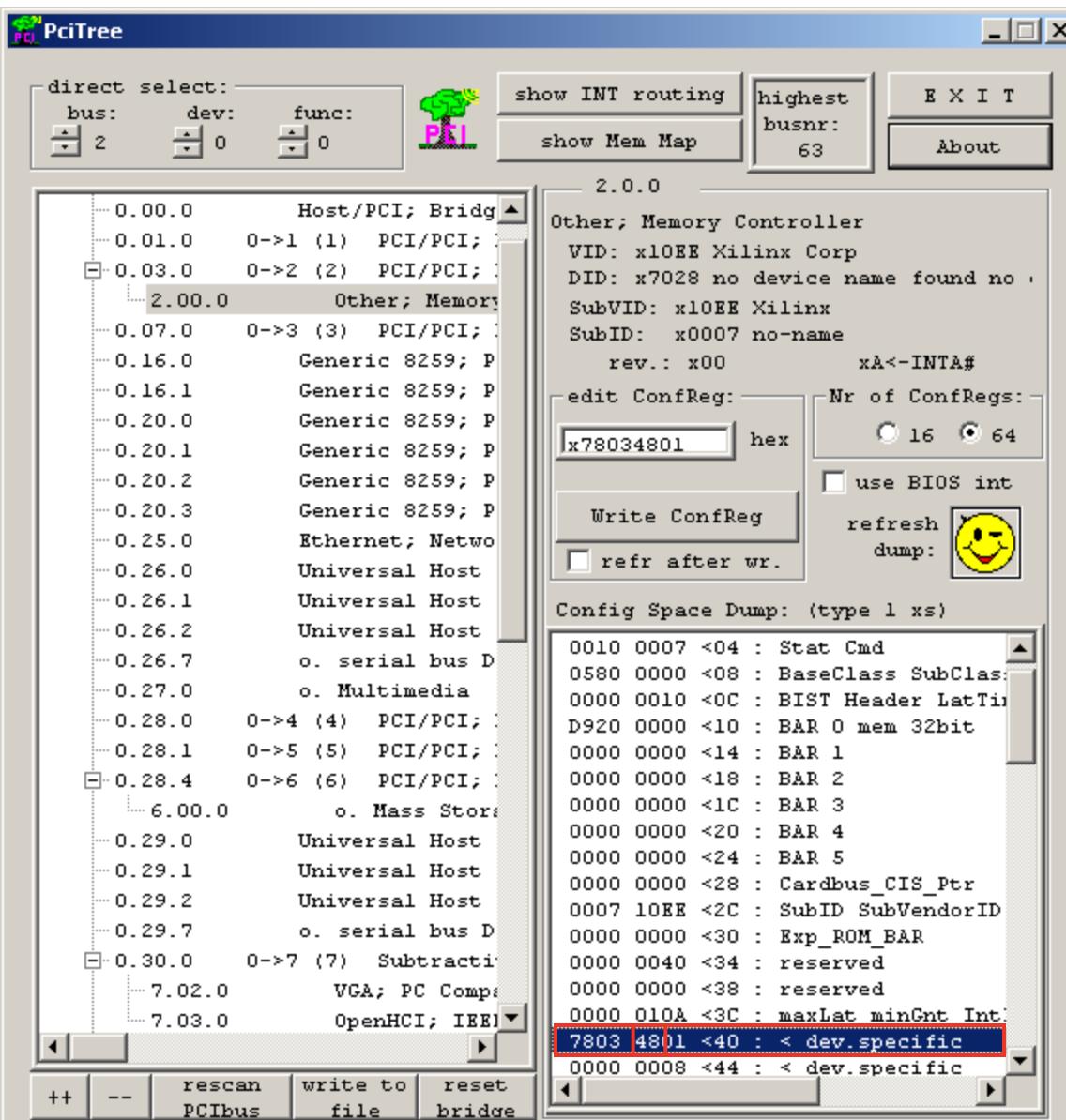
# Running the PCIe x8 Gen 2 Design

## ► Locate the Xilinx Device

- Vendor ID is 0x10EE
- The x8 Gen 2 configuration will have a Device ID of 0x7028



# Running the PCIe x8 Gen 2 Design



➤ Navigate the linked list in configuration space to locate the PCIe Capabilities Structure

- See [PG054](#) for details

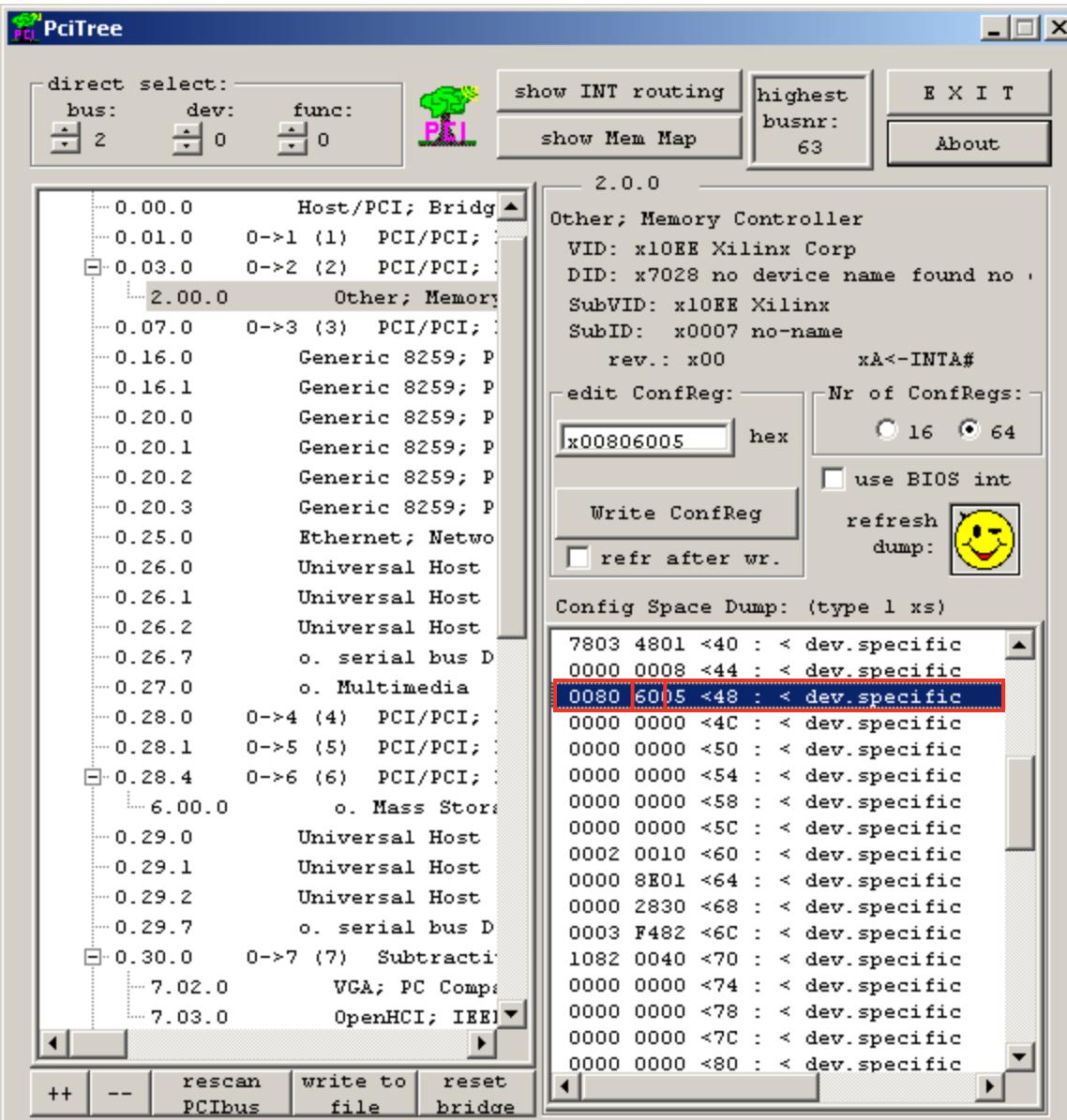
➤ With the Xilinx device selected, select Register 0x40

- Register 0x40 points to the next structure
- 0x48 is the address of the next structure

# Running the PCIe x8 Gen 2 Design

## ► Select Register 0x48

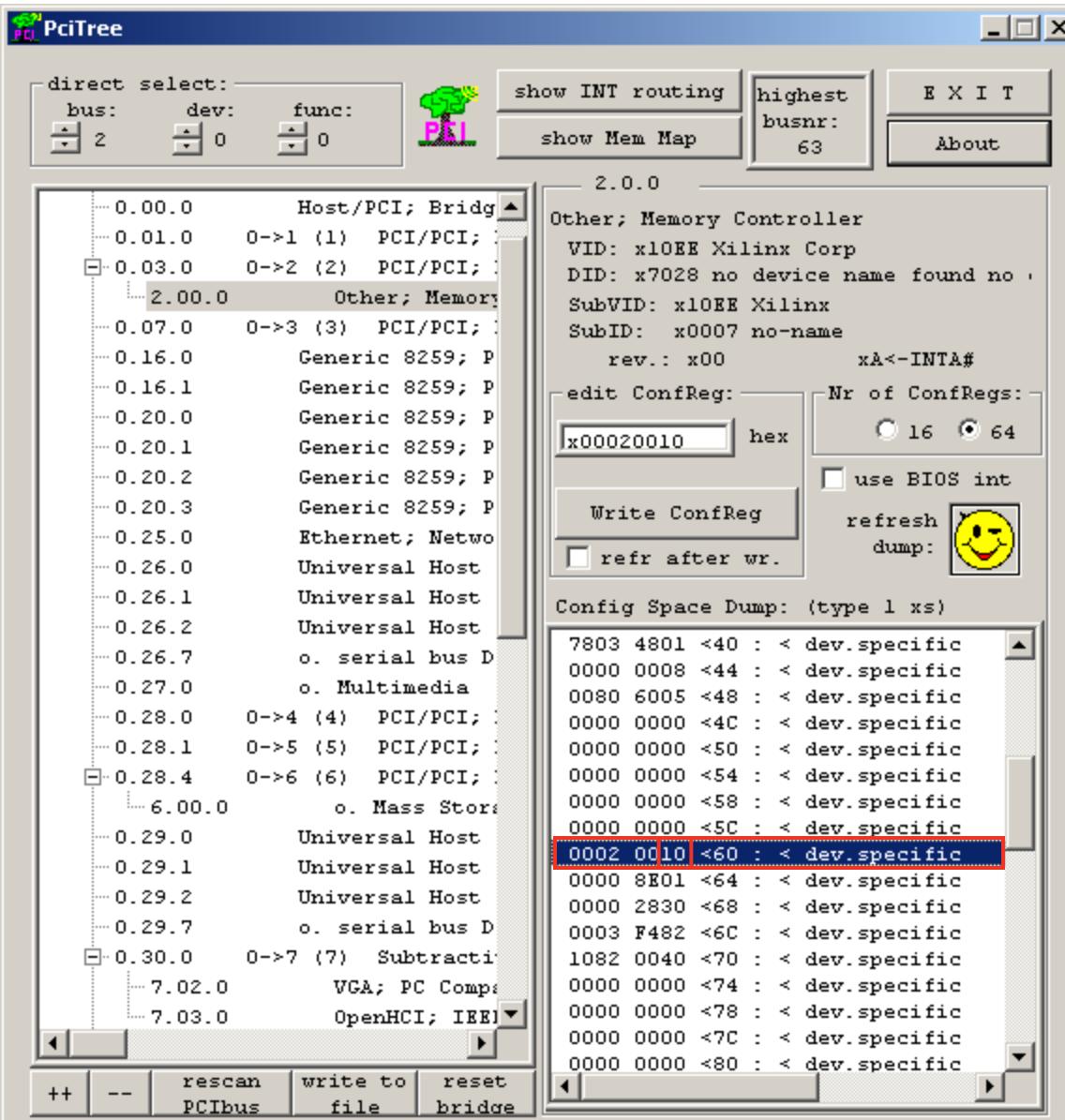
- Register 0x48 points to the next structure
- 0x60 is the address of the next structure



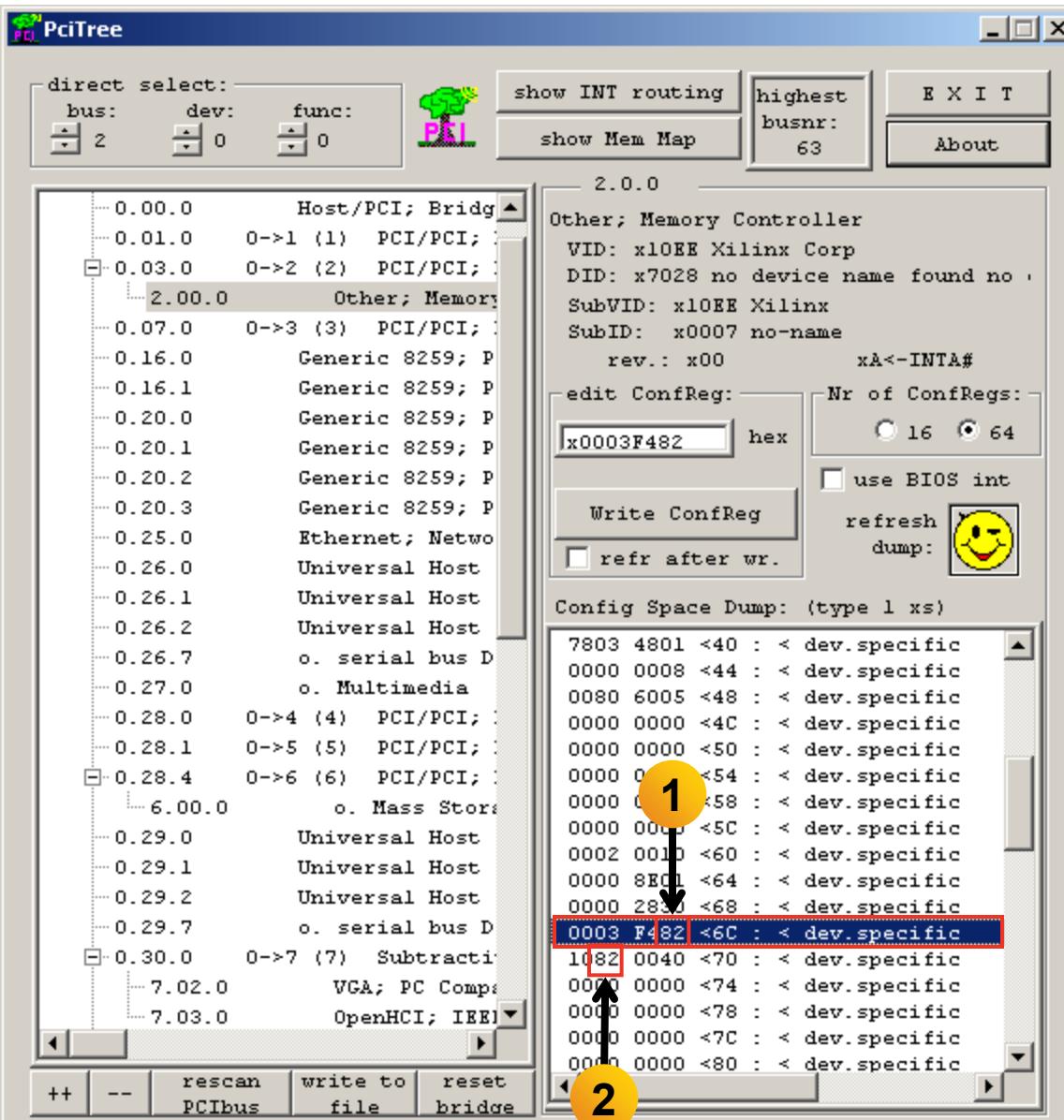
# Running the PCIe x8 Gen 2 Design

## ► Register 0x60

- 0x60 is a type 0x10, indicating PCIe Capabilities Structure
- Last Structure



# Running the PCIe x8 Gen 2 Design



## ► Register 0x6C

- Link Capabilities Register
- Indicates the maximum number of lanes and speed (Gen 1, Gen 2) for device
- The value 0x82 shows this is an x8 Gen 2 device (1)

## ► Link Status Register

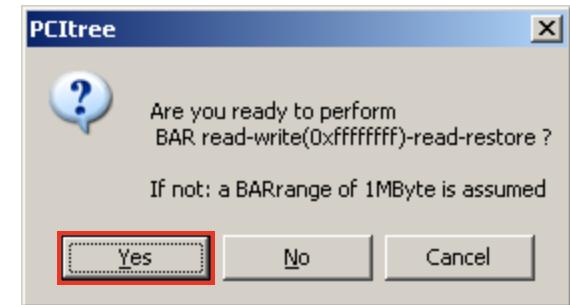
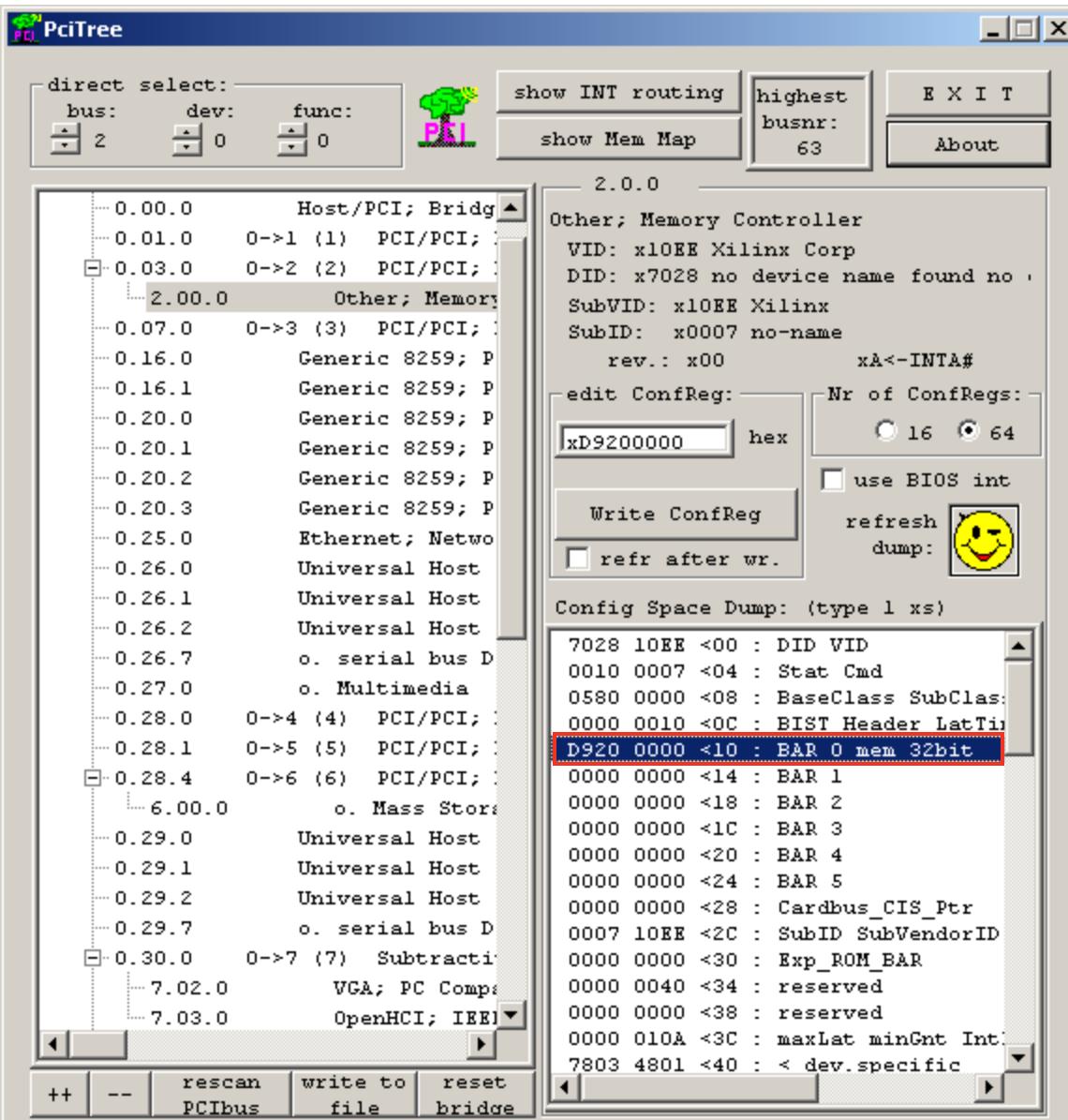
- 0x70
- Shows the current link status
- This design, in a Gen 2 chassis, trained to x8 Gen 2 (2)

# Running the PCIe x8 Gen 2 Design

## ► Double-click on BAR 0

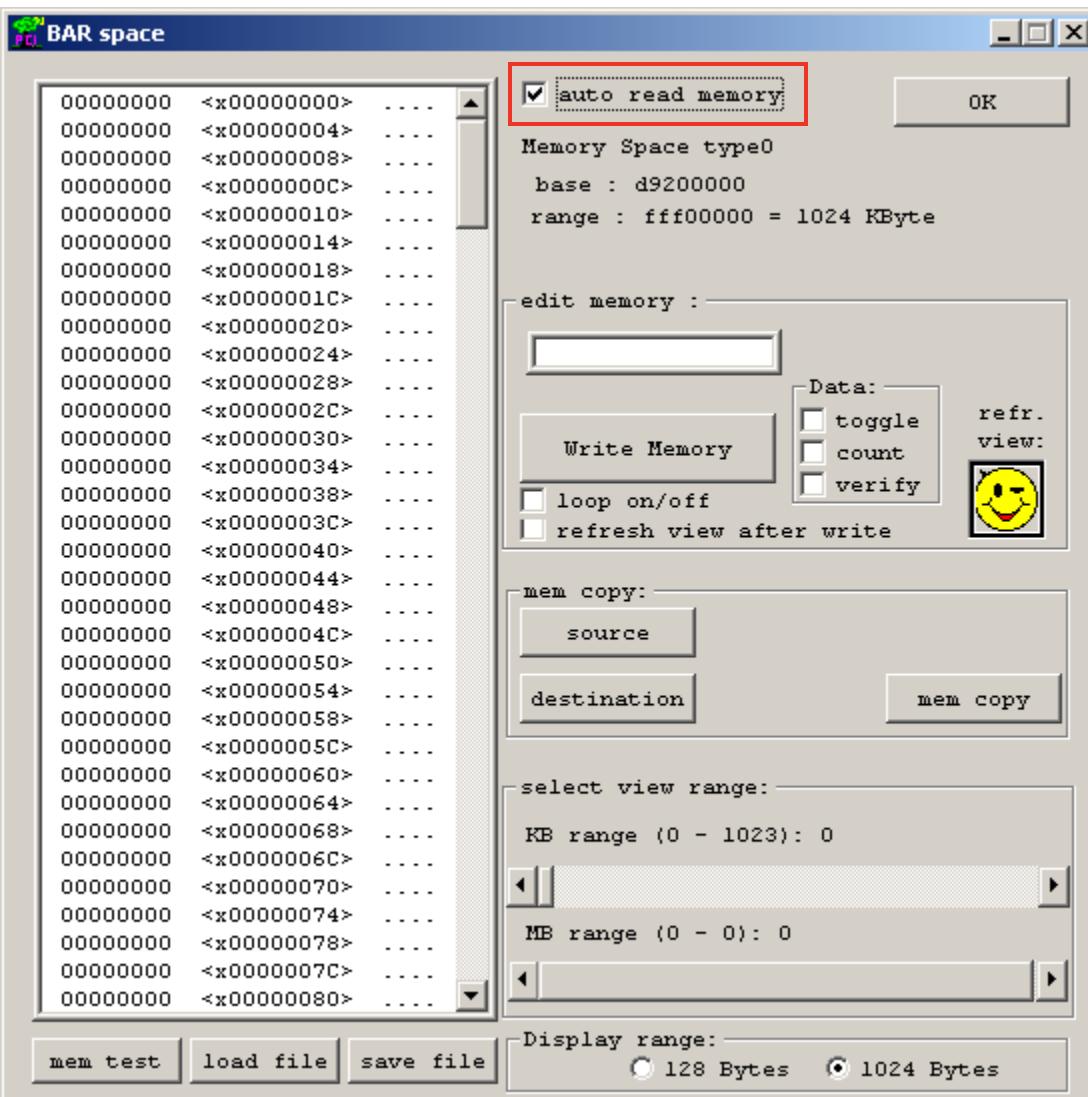
- BAR 0 Address is machine dependent

## ► Click Yes on the Dialog box seen below



# Running the PCIe x8 Gen 2 Design

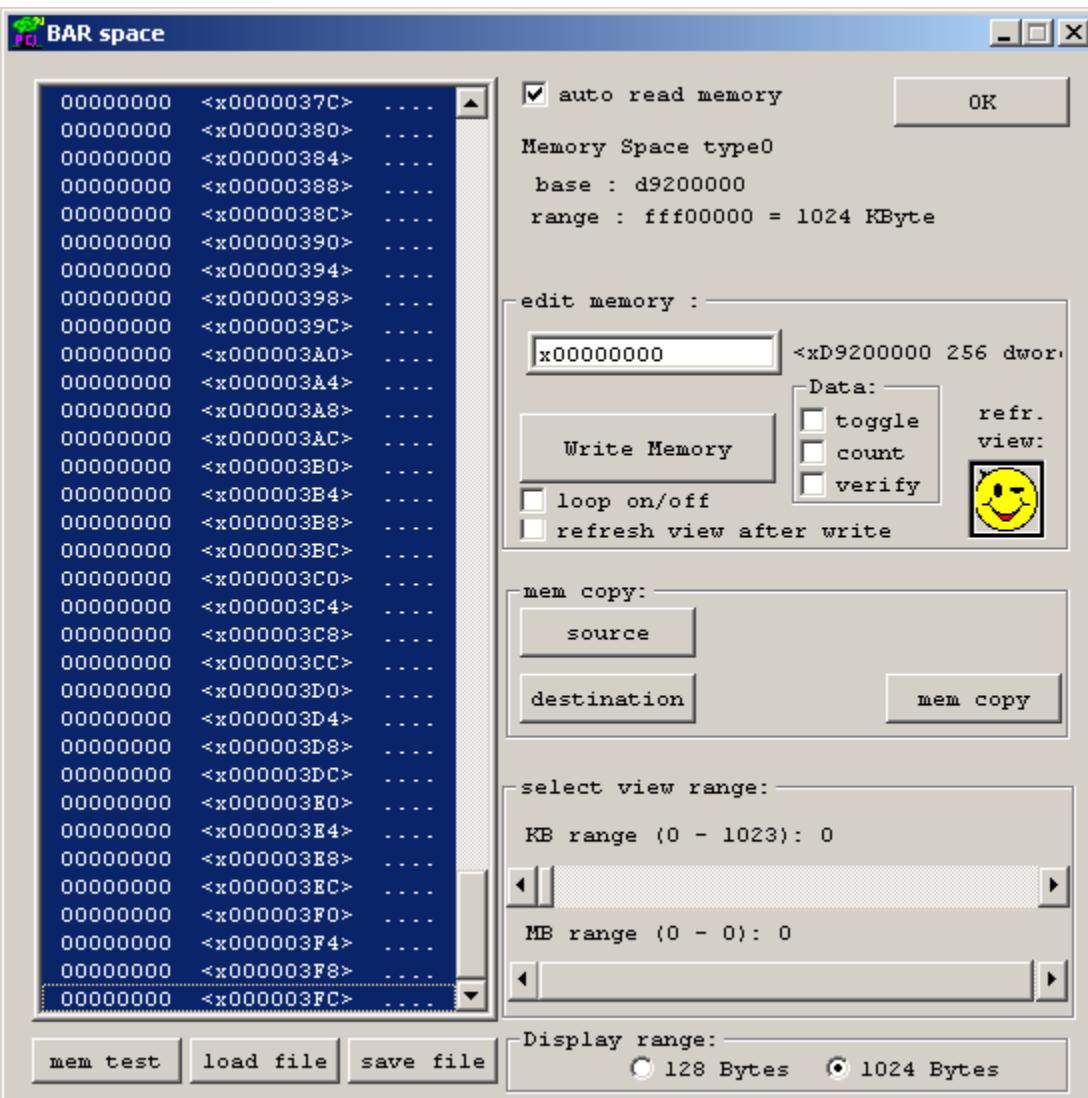
► Select auto read memory



# Running the PCIe x8 Gen 2 Design

► Click on the first memory location

- Type <Shift-End> to select 1024 Bytes

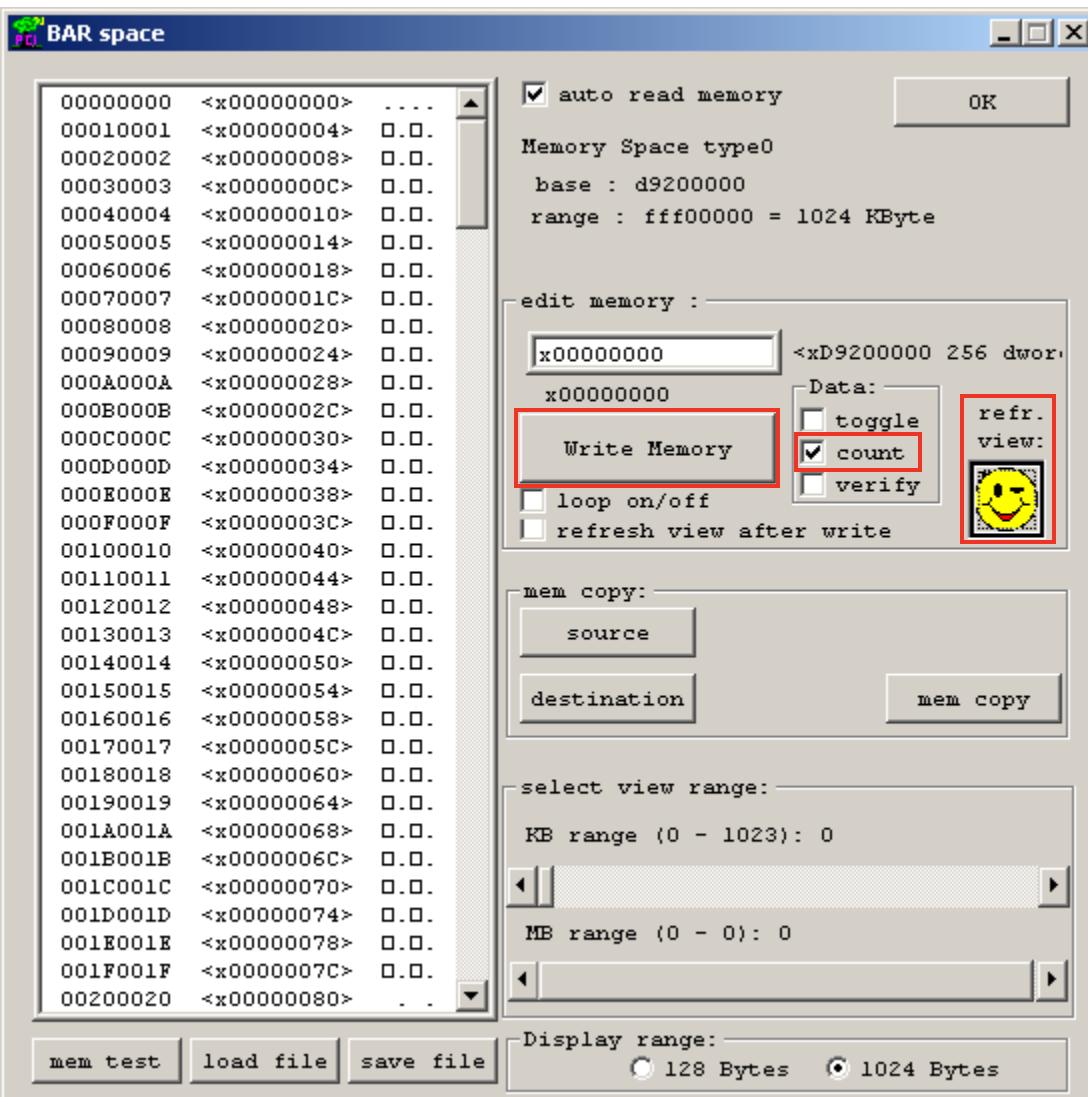


# Running the PCIe x8 Gen 2 Design

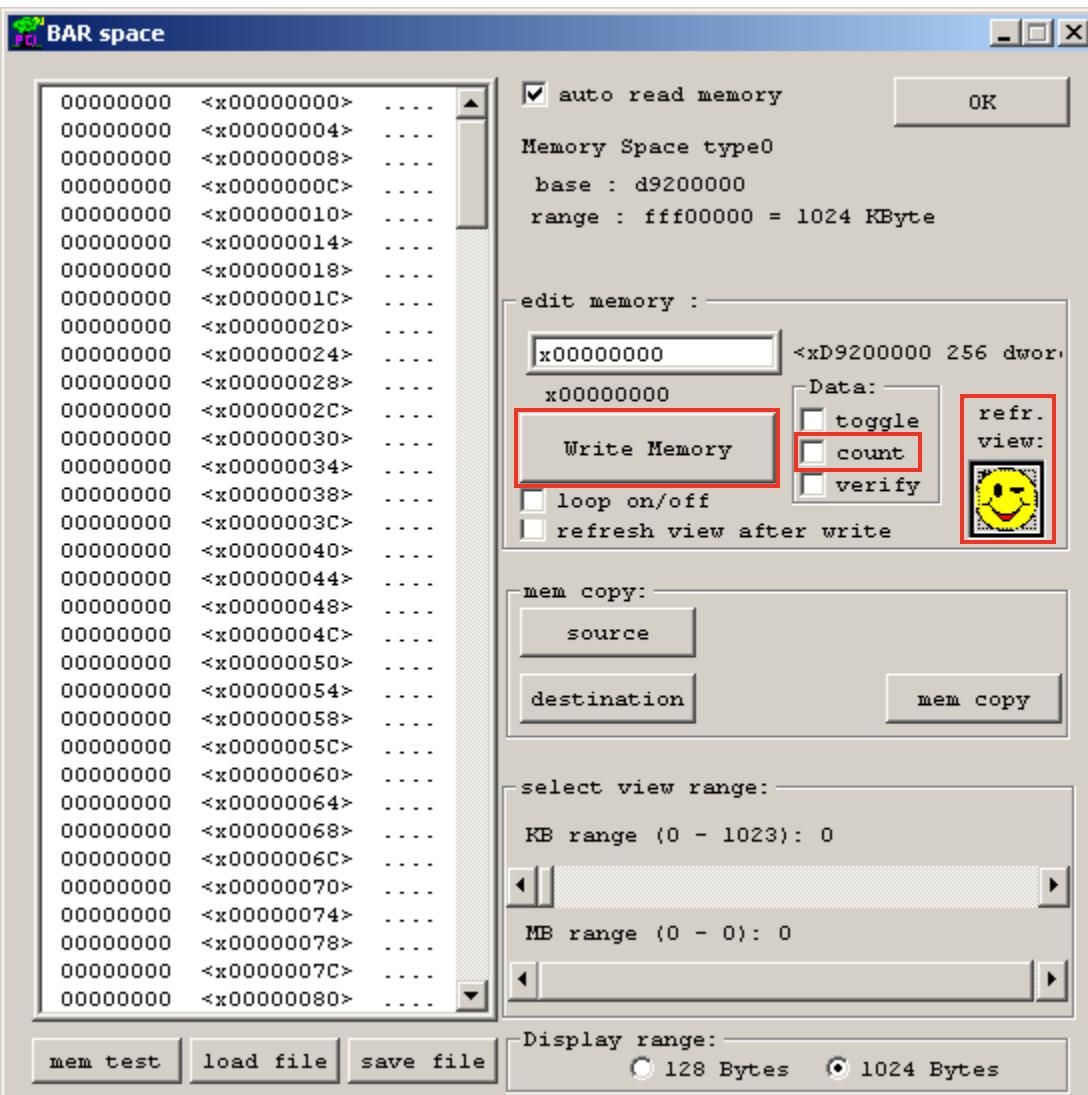
## ➤ Write Memory

- Select count
- Click Write Memory
- Click refr view

## ➤ View results – counting up to FF



# Running the PCIe x8 Gen 2 Design



## ➤ Restore Memory

- Deselect count
- Click Write Memory
- Click refr view

## ➤ Memory is reset to zeros

## ➤ Turn off PCIe chassis and remove KC705 board

## References

# References

## ► PCIe Base Specification

- PCI SIG Web Site
  - <http://www.pcisig.com/home>

## ► Xilinx PCI Express

- Xilinx PCI Express Overview
  - <http://www.xilinx.com/technology/protocols/pciexpress.htm>
- 7 Series Integrated Block for PCI Express Product Page
  - [http://www.xilinx.com/products/intellectual-property/7\\_SERIES\\_PCI\\_Express\\_Block.htm](http://www.xilinx.com/products/intellectual-property/7_SERIES_PCI_Express_Block.htm)
- 7 Series Integrated Block for PCI Express Product Guide – PG054
  - [http://www.xilinx.com/support/documentation/ip\\_documentation/pcie\\_7x/v3\\_0/pg054-7series-pcie.pdf](http://www.xilinx.com/support/documentation/ip_documentation/pcie_7x/v3_0/pg054-7series-pcie.pdf)
- 7 Series Integrated Block for PCI Express – Release Notes
  - <http://www.xilinx.com/support/answers/40469.htm>

# References

## ► Micron NOR Flash

- Micron P30 Flash
  - <http://www.micron.com/partsnor-flash/parallel-nor-flash/pc28f00ap30tfa>
- Datasheet
  - [http://www.micron.com/~media/Documents/Products/Data%20Sheet/NOR%20Flash/Parallel/P30/p30-65nm\\_mlc\\_512mb\\_1gb\\_2gb.pdf](http://www.micron.com/~media/Documents/Products/Data%20Sheet/NOR%20Flash/Parallel/P30/p30-65nm_mlc_512mb_1gb_2gb.pdf)

## ► Xilinx Generation 7 Configuration with BPI Flash

- 7 Series FPGAs Configuration User Guide – UG470
  - [http://www.xilinx.com/support/documentation/user\\_guides/ug470\\_7Series\\_Config.pdf](http://www.xilinx.com/support/documentation/user_guides/ug470_7Series_Config.pdf)
- Vivado Design Suite Programming and Debugging User Guide
  - [http://www.xilinx.com/support/documentation/sw\\_manuals/xilinx2014\\_3/ug908-vivado-programming-debugging.pdf](http://www.xilinx.com/support/documentation/sw_manuals/xilinx2014_3/ug908-vivado-programming-debugging.pdf)
- BPI Fast Configuration with 7 Series FPGAs – XAPP587
  - [http://www.xilinx.com/support/documentation/application\\_notes/xapp587-bpi-fast-configuration.pdf](http://www.xilinx.com/support/documentation/application_notes/xapp587-bpi-fast-configuration.pdf)

# Documentation

# Documentation

## ► Kintex-7

- Kintex-7 FPGA Family
  - <http://www.xilinx.com/products/silicon-devices/fpga/kintex-7/index.htm>
- Design Advisory Master Answer Record for Kintex-7 FPGAs
  - <http://www.xilinx.com/support/answers/42946.htm>

## ► KC705 Documentation

- Kintex-7 FPGA KC705 Evaluation Kit
  - <http://www.xilinx.com/products/boards-and-kits/EK-K7-KC705-G.htm>
- KC705 Getting Started Guide
  - [http://www.xilinx.com/support/documentation/boards\\_and\\_kits/kc705/2014\\_2/ug883\\_K7\\_KC705\\_Eval\\_Kit.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/kc705/2014_2/ug883_K7_KC705_Eval_Kit.pdf)
- KC705 User Guide
  - [http://www.xilinx.com/support/documentation/boards\\_and\\_kits/kc705/ug810\\_KC705\\_Eval\\_Bd.pdf](http://www.xilinx.com/support/documentation/boards_and_kits/kc705/ug810_KC705_Eval_Bd.pdf)