

ECE260: Fundamentals of Computer Engineering

Arithmetic for Computers

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Arithmetic for Computers

- Operations on integers
 - Addition and subtraction
 - Multiplication and division
 - Dealing with overflow
- Floating-point real numbers
 - Representation and operations

Binary Integer Addition

- Benefit of 2's complement integer representation:
 - Same binary addition procedure will work for adding both signed and unsigned numbers
- If result is out of range, **overflow** occurs
 - Adding positive and negative operands
 - No overflow occurs (discard carry-out bit)
 - Adding two positive operands
 - Overflow occurred if sign bit of result is 1
 - Adding two negative operands
 - Overflow occurred if sign bit of result is 0

- Example: $7_{\text{ten}} + 6_{\text{ten}}$

$$\begin{array}{rcccc} (1) & (1) & (0) & (\text{Carries}) \\ 0 & 1 & 1 & 1 \\ 0 & 1 & 1 & 0 \\ \hline 1 & 1 & 0 & 1 \end{array}$$

Grade school style!

- Example expanded to show carries inline

$$\begin{array}{cccccccccccc} & & (0) & & (0) & & (1) & & (1) & & (0) & & (\text{Carries}) \\ & & 0 & & 0 & & 0 & & 1 & & 1 & & 1 \\ \dots & & 0 & & 0 & & 0 & & 1 & & 1 & & 0 \\ \dots & & 0 & & 0 & & 0 & & 1 & & 1 & & 1 \\ \dots & (0) & 0 & (0) & 0 & (0) & 1 & (1) & 1 & (1) & 0 & (0) & 1 \end{array}$$

Binary Integer Subtraction

- Two options:
 - Subtract numbers directly grade school style
 - Negate 2nd operand and perform an addition
- If result is out of range, **overflow** occurs
 - Subtracting two positive or two negative operands
 - No overflow will occur
 - Subtracting positive from negative operand
 - Overflow occurred if sign bit of result is 0
 - Subtracting negative from positive operand
 - Overflow occurred if sign bit of result is 1

- Example: $7_{\text{ten}} - 6_{\text{ten}}$

- Grade school style

	0000	0111	$_{\text{two}}$	=	7_{ten}
-	0000	0110	$_{\text{two}}$	=	6_{ten}
<hr/>					
=	0000	0001	$_{\text{two}}$	=	1_{ten}

- Negate 2nd operand and add

	0000	0111	$_{\text{two}}$	=	7_{ten}
+	1111	1010	$_{\text{two}}$	=	-6_{ten}
<hr/>					
=	0000	0001	$_{\text{two}}$	=	1_{ten}

Dealing with Overflow

- Some languages (e.g., C) ignore overflow
 - Up to the programmer to address potential overflow issues
- Other languages (e.g., Fortran, Ada) will cause an **exception** if overflow occurs
 - Exception notifies programmer so that overflow can be handled
- In MIPS, overflow behavior is as follows:
 - Signed instructions raise exceptions (e.g. add, addi, sub)
 - Unsigned instructions do not raise exceptions (e.g. addu, addiu, subu)

- The following table summarizes the results that indicate overflow occurred

Operation	Operand A	Operand B	Result indicating overflow
$A + B$	≥ 0	≥ 0	< 0
$A + B$	< 0	< 0	≥ 0
$A - B$	≥ 0	< 0	< 0
$A - B$	< 0	≥ 0	≥ 0

- Examples:
 - $\text{Result} = \text{Op}_A + \text{Op}_B$
IF ($\text{Op}_A \geq 0$ and $\text{Op}_B \geq 0$ and $\text{Result} < 0$)
THEN overflow occurred
 - $\text{Result} = \text{Op}_A - \text{Op}_B$
IF ($\text{Op}_A \geq 0$ and $\text{Op}_B < 0$ and $\text{Result} < 0$)
THEN overflow occurred

Integer Multiplication

- Here's the classic grade school "Times Table"
 - At some point you probably memorized this

×	0	1	2	3	4	5	6	7	8	9
0	0	0	0	0	0	0	0	0	0	0
1	0	1	2	3	4	5	6	7	8	9
2	0	2	4	6	8	10	12	14	16	18
3	0	3	6	9	12	15	18	21	24	27
4	0	4	8	12	16	20	24	28	32	36
5	0	5	10	15	20	25	30	35	40	45
6	0	6	12	18	24	30	36	42	48	54
7	0	7	14	21	28	35	42	49	56	63
8	0	8	16	24	32	40	48	56	64	72
9	0	9	18	27	36	45	54	63	72	81

- Multiplying two numbers together looks something like this:

Multiplicand	A_3	A_2	A_1	A_0
Multiplier	$\times B_3$	B_2	B_1	B_0
<hr/>				
	A_3B_0	A_2B_0	A_1B_0	A_0B_0
	A_3B_1	A_2B_1	A_1B_1	A_0B_1
	A_3B_2	A_2B_2	A_1B_2	A_0B_2
+	A_3B_3	A_2B_3	A_1B_3	A_0B_3
<hr/>				
Product	RESULT			

- Note:** multiplying N-digit number by M-digit number gives (N+M)-digit result

Binary Integer Multiplication

- Once again, it's the same as grade school multiplication, only easier
- The "Times Table" is significantly smaller

×	0	1
0	0	0
1	0	1

but the process is exactly the same!

- **Example of multiplying two numbers together:**

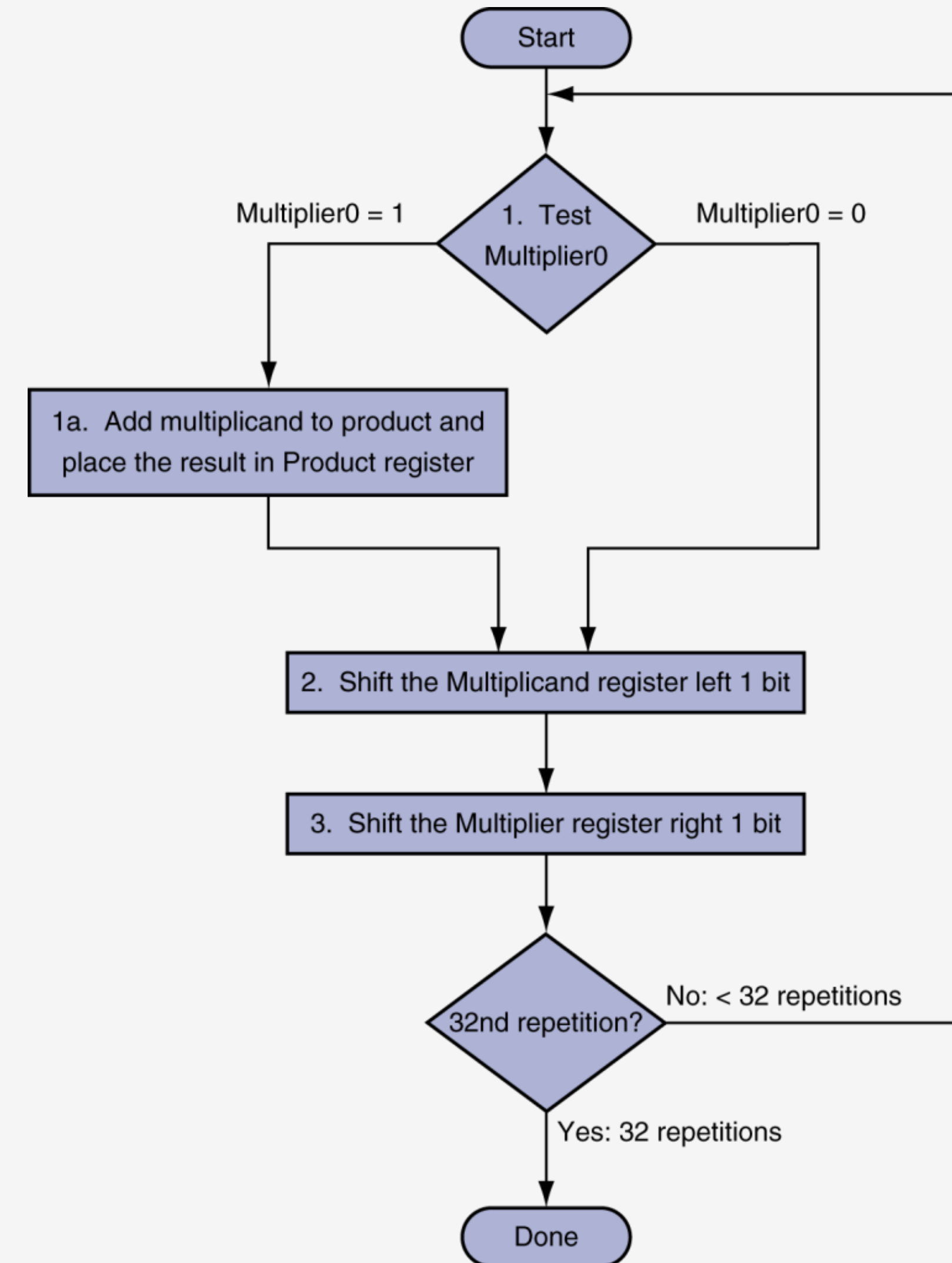
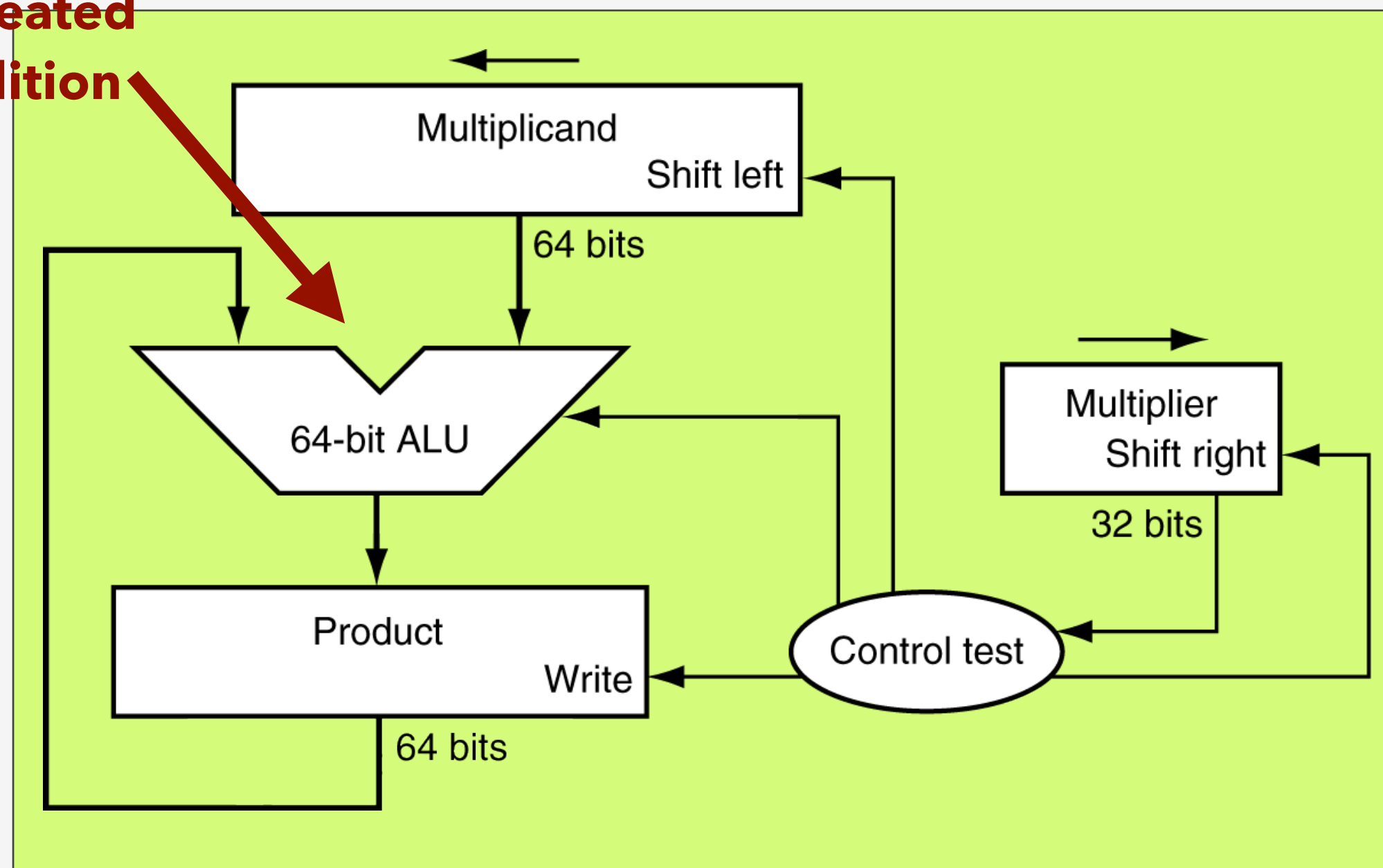
Multiplicand				1	0	0	0 _{two}
Multiplier		×		1	0	0	1 _{two}
				1	0	0	0
			0	0	0	0	0
		0	0	0	0	0	0
	+	1	0	0	0	0	0
Product			1	0	0	1	0

- **Note:** multiplying two 4-bit numbers together produces an 8-bit result

Multiplication Hardware & Algorithm

- Basic hardware for 32-bit architecture
 - 64-bit registers for multiplicand and product
 - 32-bit register for multiplier
 - 64-bit ALU to perform repeated additions

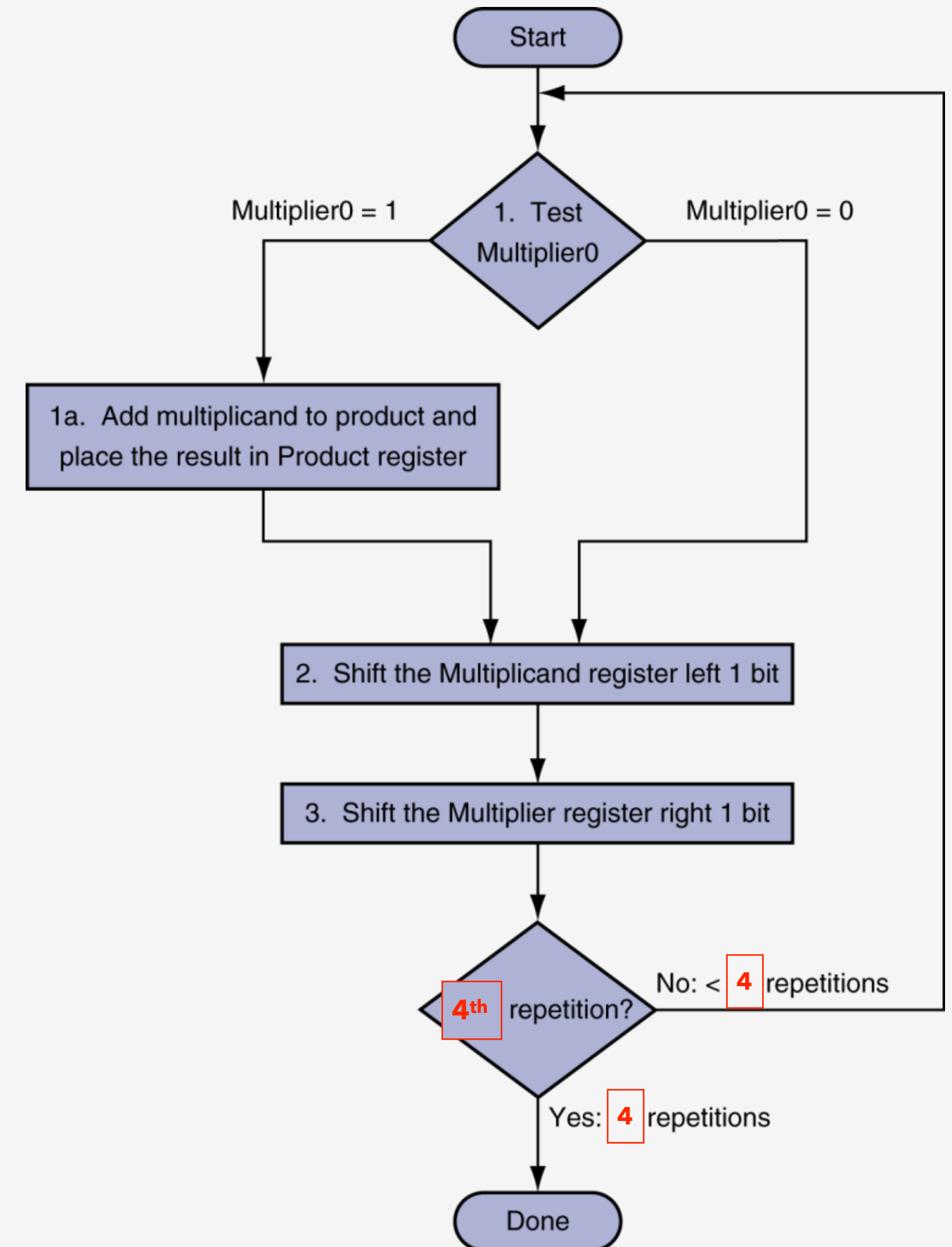
**Repeated
addition**



Multiplication Example

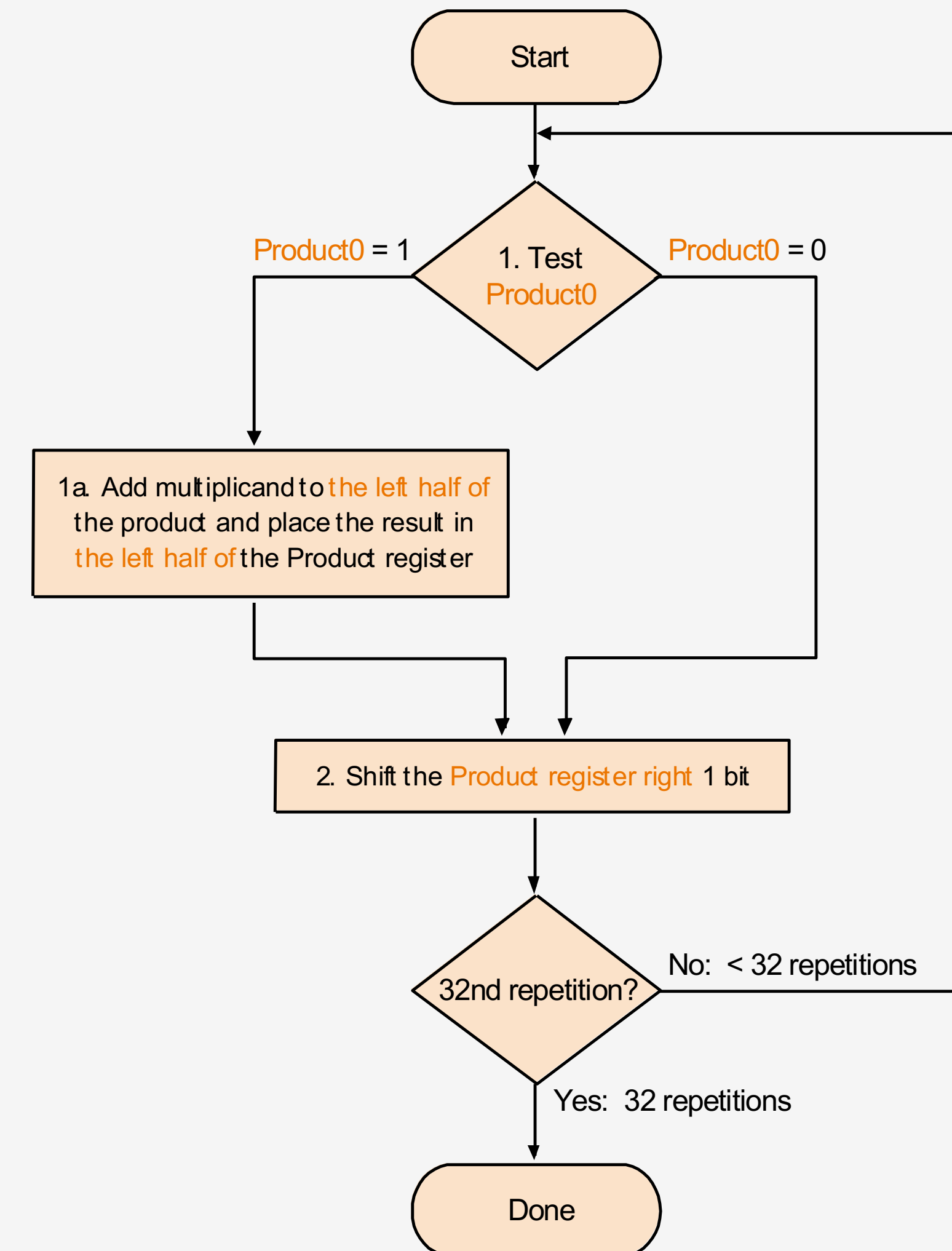
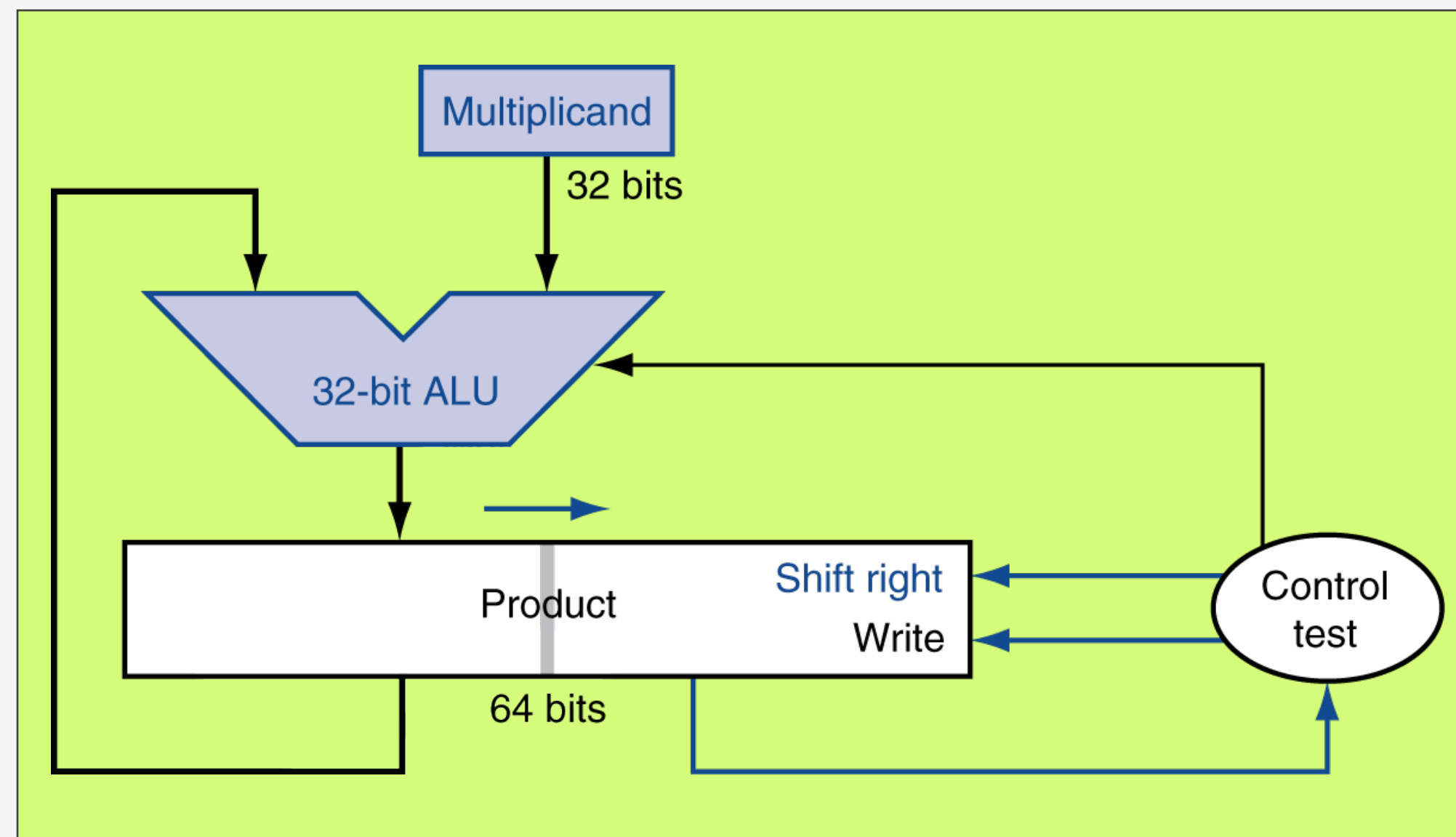
- Multiplication example using basic hardware and 4-bit inputs
 - 4-bit example requires only 4 iterations, not 32
 - Initialize Product register to 0
 - Example: $2_{\text{ten}} \times 3_{\text{ten}}$

Iteration	Step	Multiplier	Multiplicand	Product
0	Initial values	001 <u>1</u>	0000 0010	0000 0000
1	1a: $1 \Rightarrow \text{Prod} = \text{Prod} + \text{Mcand}$	0011	0000 0010	0000 0010
	2: Shift left Multiplicand	0011	0000 0100	0000 0010
	3: Shift right Multiplier	000 <u>1</u>	0000 0100	0000 0010
2	1a: $1 \Rightarrow \text{Prod} = \text{Prod} + \text{Mcand}$	0001	0000 0100	0000 0110
	2: Shift left Multiplicand	0001	0000 1000	0000 0110
	3: Shift right Multiplier	000 <u>0</u>	0000 1000	0000 0110
3	1: $0 \Rightarrow$ No operation	0000	0000 1000	0000 0110
	2: Shift left Multiplicand	0000	0001 0000	0000 0110
	3: Shift right Multiplier	000 <u>0</u>	0001 0000	0000 0110
4	1: $0 \Rightarrow$ No operation	0000	0001 0000	0000 0110
	2: Shift left Multiplicand	0000	0010 0000	0000 0110
	3: Shift right Multiplier	000 <u>0</u>	0010 0000	0000 0110



Optimized (for size) Multiplication Hardware

- Reduced hardware requirements
 - Multiplicand register and ALU now 32-bit
 - Multiplier no longer has dedicated register
 - Right half of Product register is initialized with multiplier, left half initialized to zero

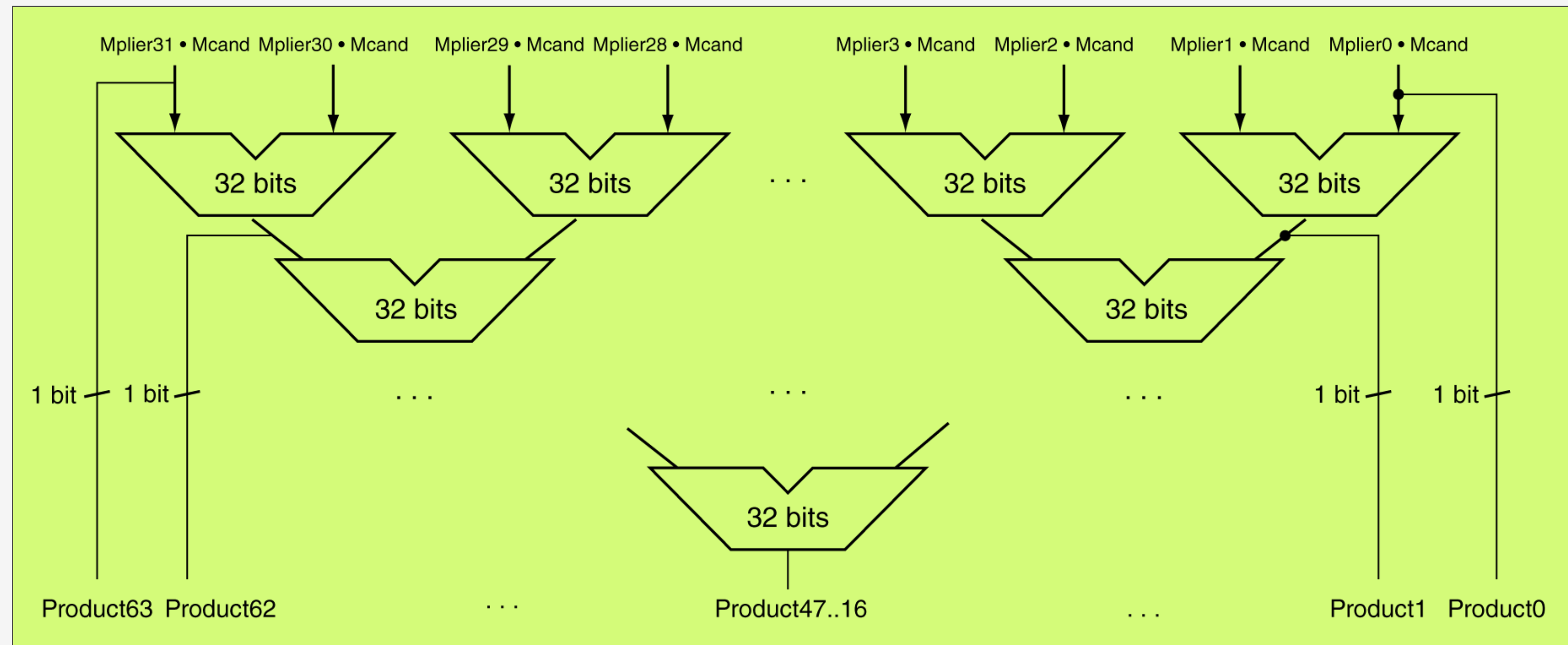


Multiplication Example #2

- Be sure to try out the previous multiplication example using the optimized hardware!
 - Example: $2_{\text{ten}} \times 3_{\text{ten}}$

A Faster Multiplier

- Uses multiple adders in a tree structure
- Requires more silicon but can be pipelined to perform much faster
- Cost/performance tradeoff



Signed Multiplication

- Recall from grade school arithmetic that the Product is negative if the signs of the Multiplicand and the Multiplier differ

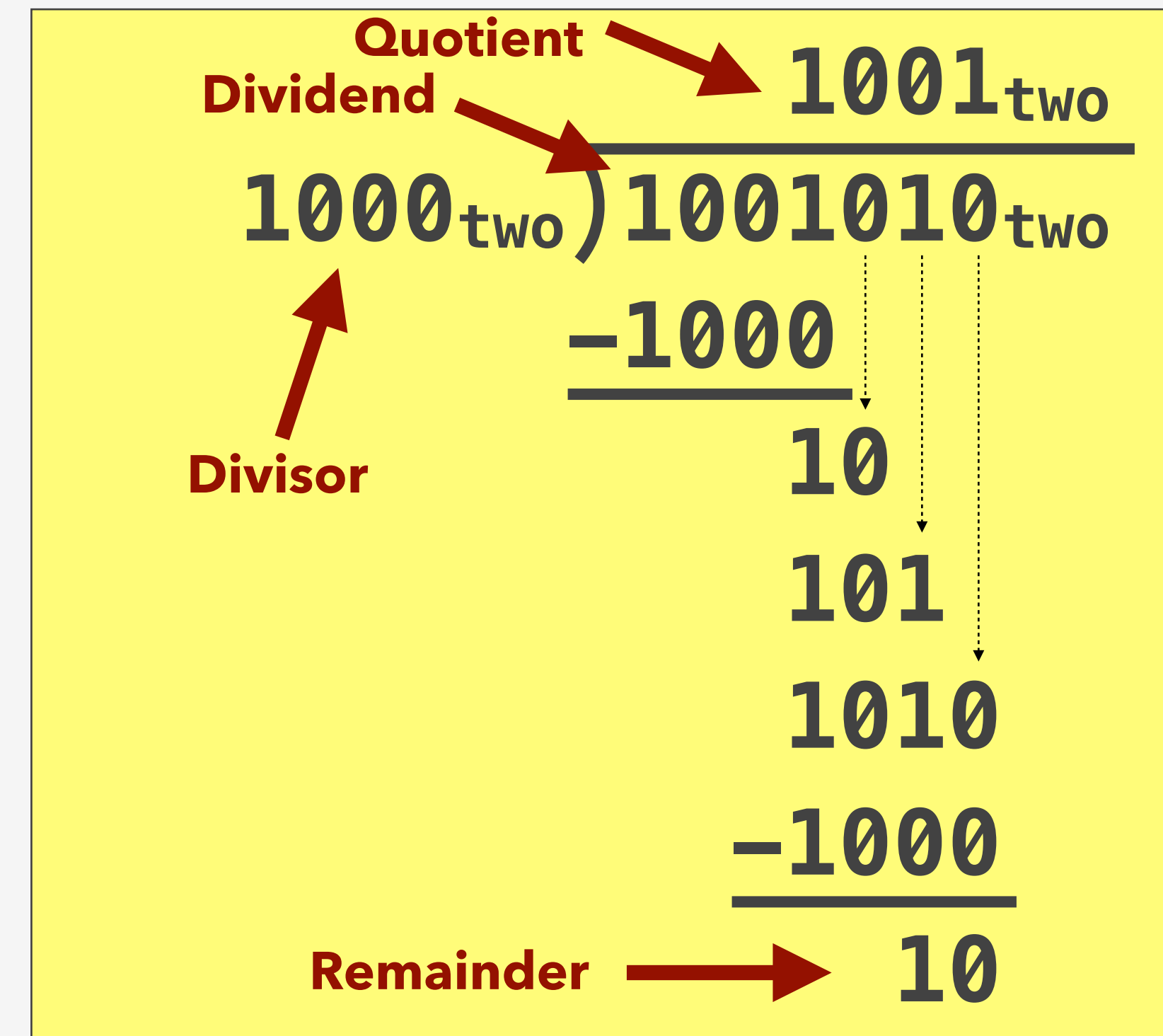
positive × **positive** = **positive**
negative × **negative** = **positive**
positive × **negative** = **negative**

- Thus, in hardware:
 - Perform the multiplication algorithm for 31 iterations (not 32) (this ignores the sign bit)
 - If the original sign bits differed, then negate the result
 - Be sure to do sign extension during computation when shifting multiplier to the right

Binary Integer Division

- The grade school long-division algorithm works for binary integer division
 - First, ensure that the divisor is not 0
 - IF divisor \leq dividend THEN
place a 1 in the quotient and subtract the divisor from the dividend
 - ELSE
place a 0 in the quotient and expand the dividend to include the next bit
- When dividend is exhausted, whatever is left over is the remainder

- Example of long-division on binary numbers:



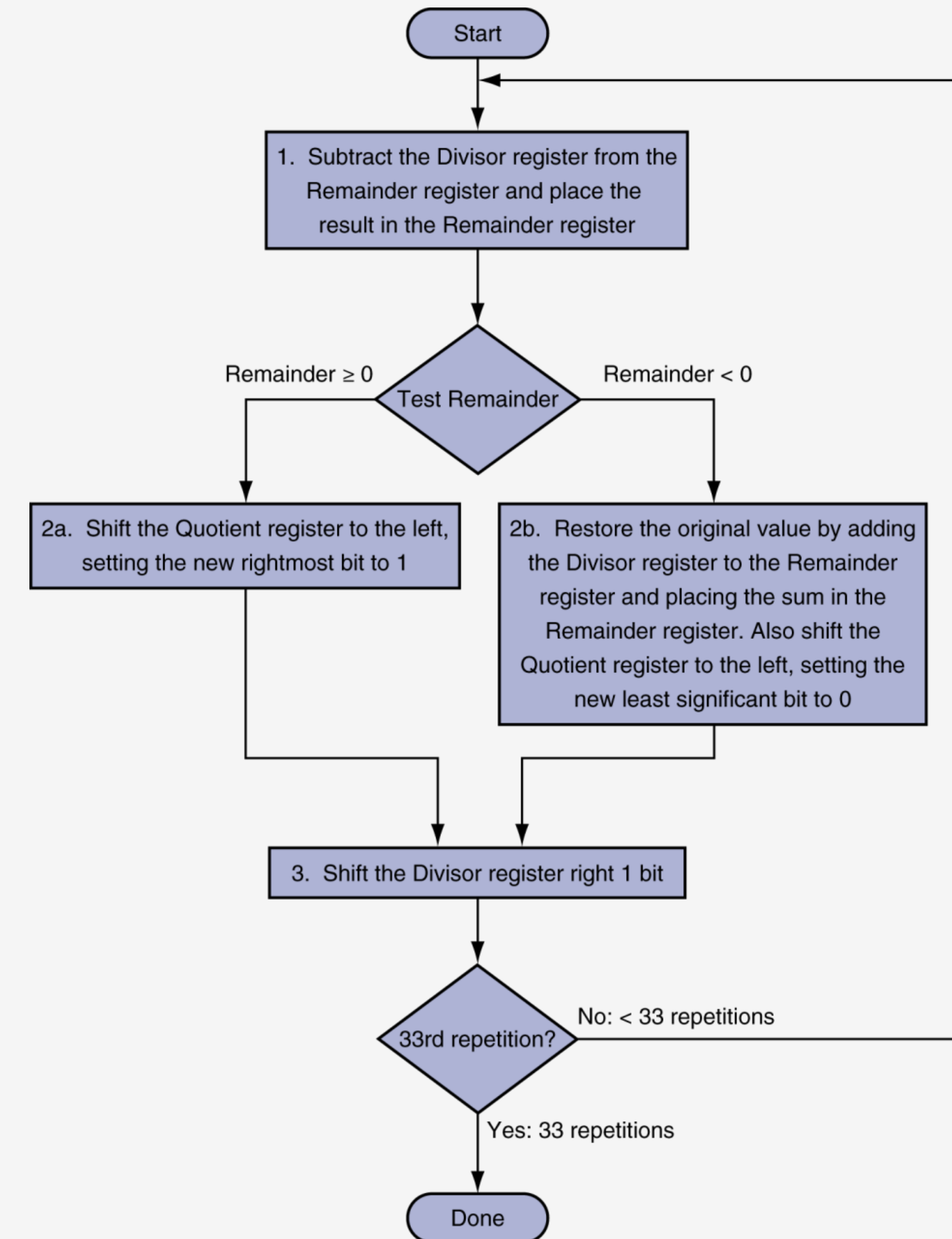
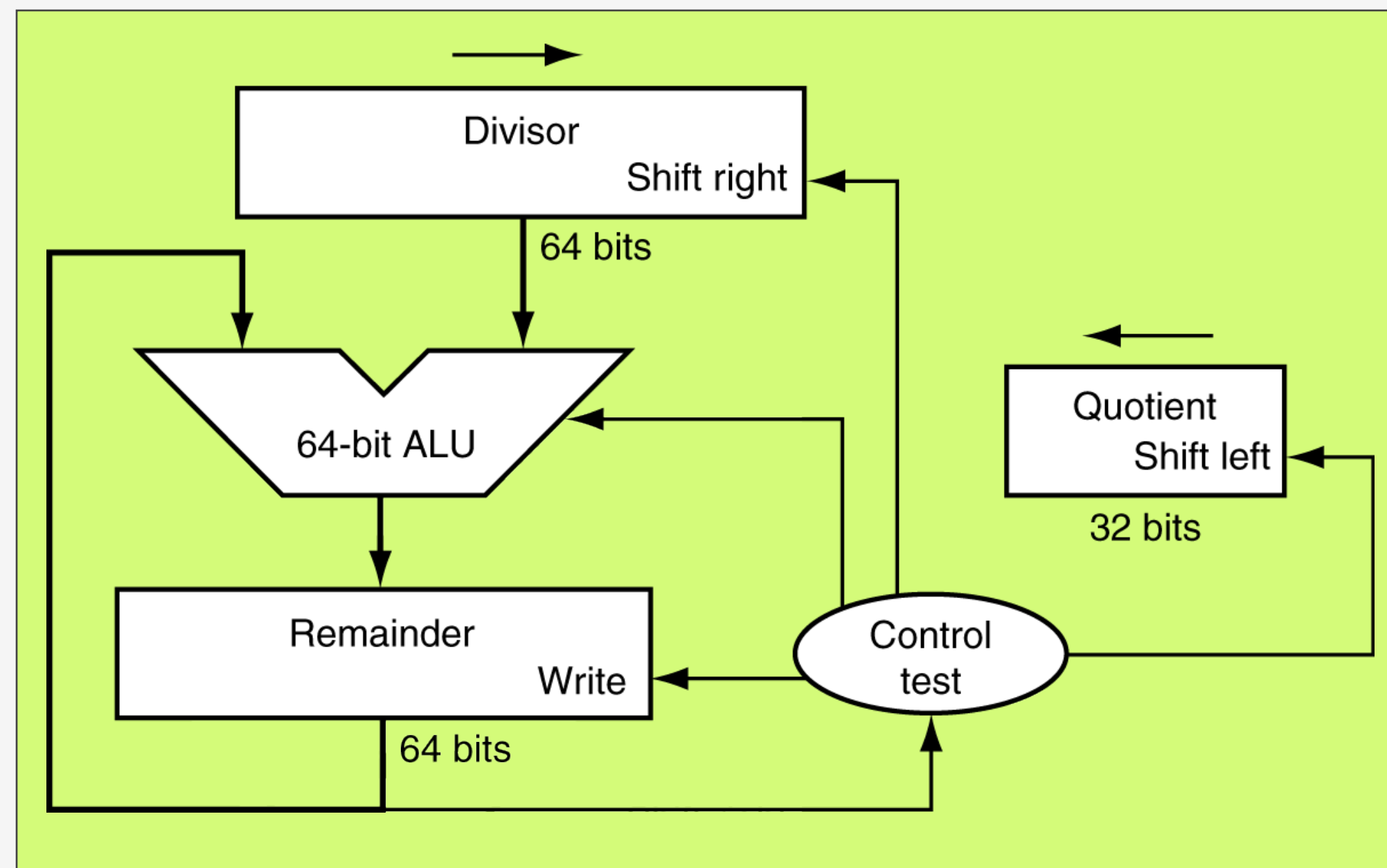
- Note: dividing n-bit operands yields an n-bit quotient and an n-bit remainder

Binary Integer Division

- Several different approaches to perform long-division in hardware
 - **Restoring division** subtracts the divisor from the dividend without comparing them
 - If the result of the subtraction is < 0 , then the dividend was smaller than the divisor
 - Insert a 0 into the quotient
 - Restore the dividend to its previous state by adding the divisor back in
 - If the result of the subtraction is ≥ 0 , then the dividend was larger than or equal to the divisor
 - Insert a 1 into the quotient

Division Hardware & Algorithm

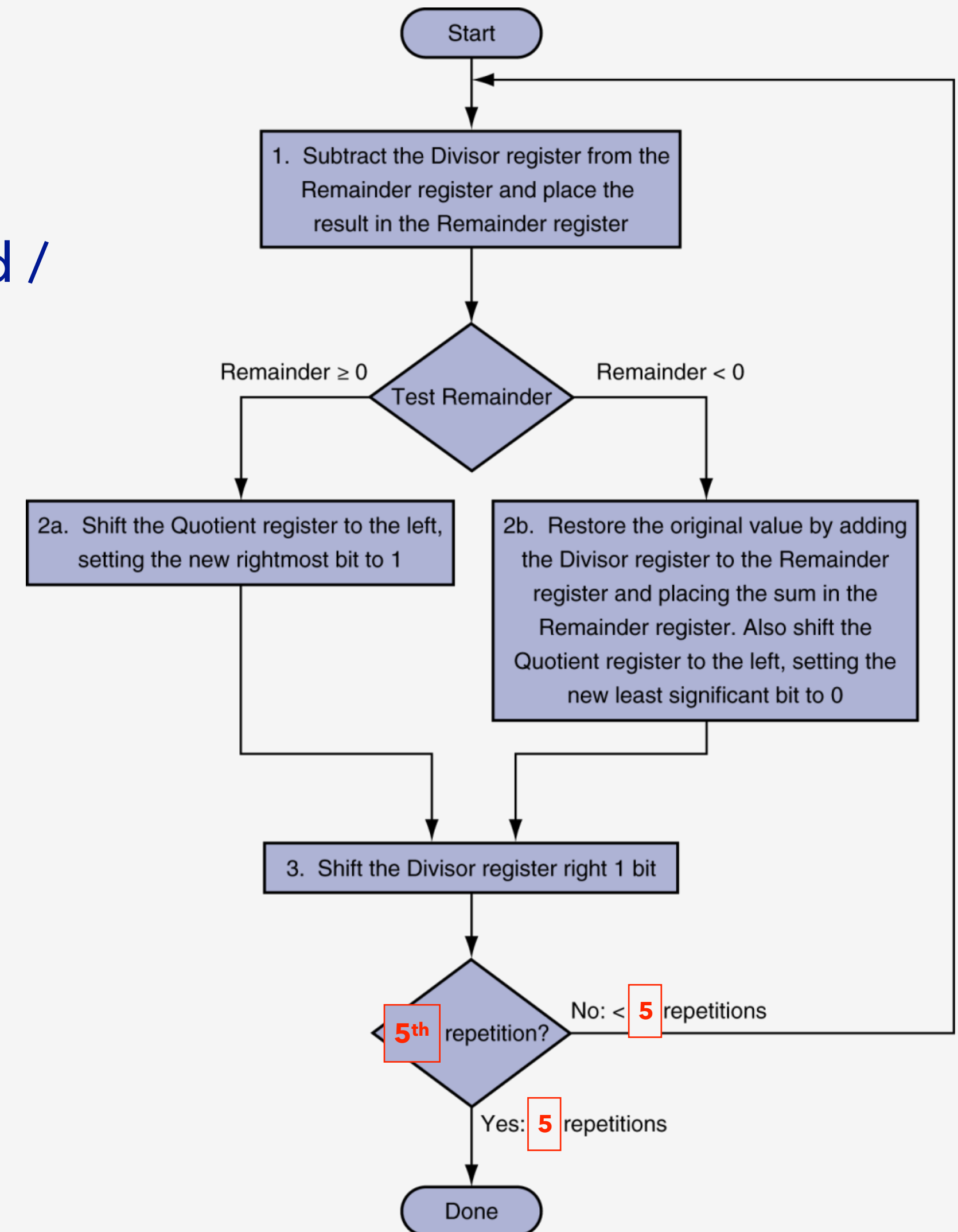
- Basic hardware for 32-bit architecture
 - 64-bit registers for divisor and remainder
 - 32-bit register for quotient
 - 64-bit ALU to perform repeated sub/add ops



Division Example

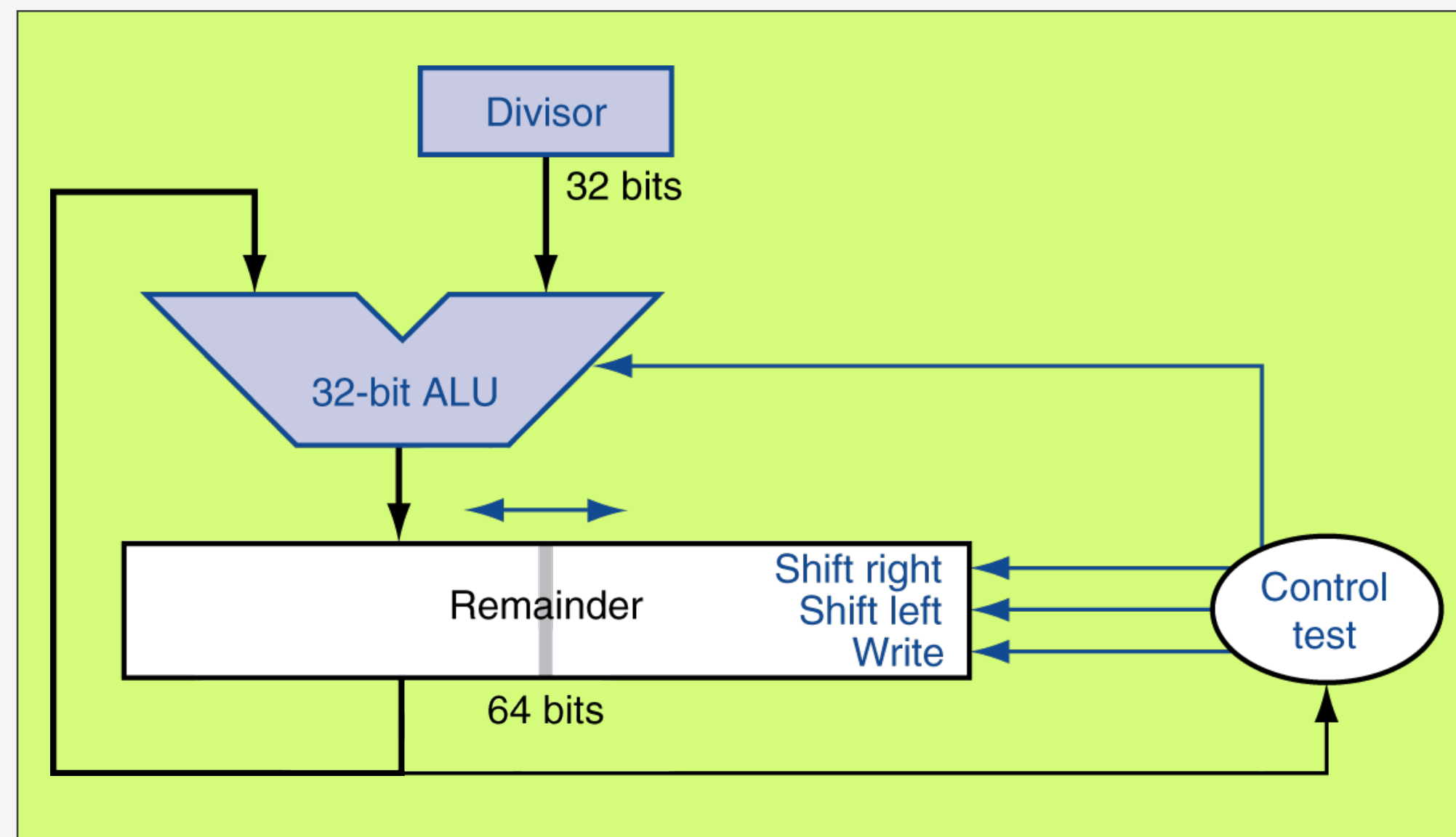
- Division example using basic hardware and 4-bit inputs
 - 4-bit example requires **5 iterations** (one more than word size)
 - Initialize Quotient register to 0 / Remainder register to dividend / and place divisor in top half of Divisor register
 - Example: $7_{\text{ten}} \div 2_{\text{ten}}$

Iteration	Step	Quotient	Divisor	Remainder
0	Initial values	0000	0010 0000	0000 0111
1	1: Rem = Rem - Div	0000	0010 0000	①110 0111
	2b: Rem < 0 \Rightarrow +Div, sll Q, Q0 = 0	0000	0010 0000	0000 0111
	3: Shift Div right	0000	0001 0000	0000 0111
2	1: Rem = Rem - Div	0000	0001 0000	①111 0111
	2b: Rem < 0 \Rightarrow +Div, sll Q, Q0 = 0	0000	0001 0000	0000 0111
	3: Shift Div right	0000	0000 1000	0000 0111
3	1: Rem = Rem - Div	0000	0000 1000	①111 1111
	2b: Rem < 0 \Rightarrow +Div, sll Q, Q0 = 0	0000	0000 1000	0000 0111
	3: Shift Div right	0000	0000 0100	0000 0111
4	1: Rem = Rem - Div	0000	0000 0100	①000 0011
	2a: Rem \geq 0 \Rightarrow sll Q, Q0 = 1	0001	0000 0100	0000 0011
	3: Shift Div right	0001	0000 0010	0000 0011
5	1: Rem = Rem - Div	0001	0000 0010	①000 0001
	2a: Rem \geq 0 \Rightarrow sll Q, Q0 = 1	0011	0000 0010	0000 0001
	3: Shift Div right	0011	0000 0001	0000 0001



Optimized (for size) Division Hardware

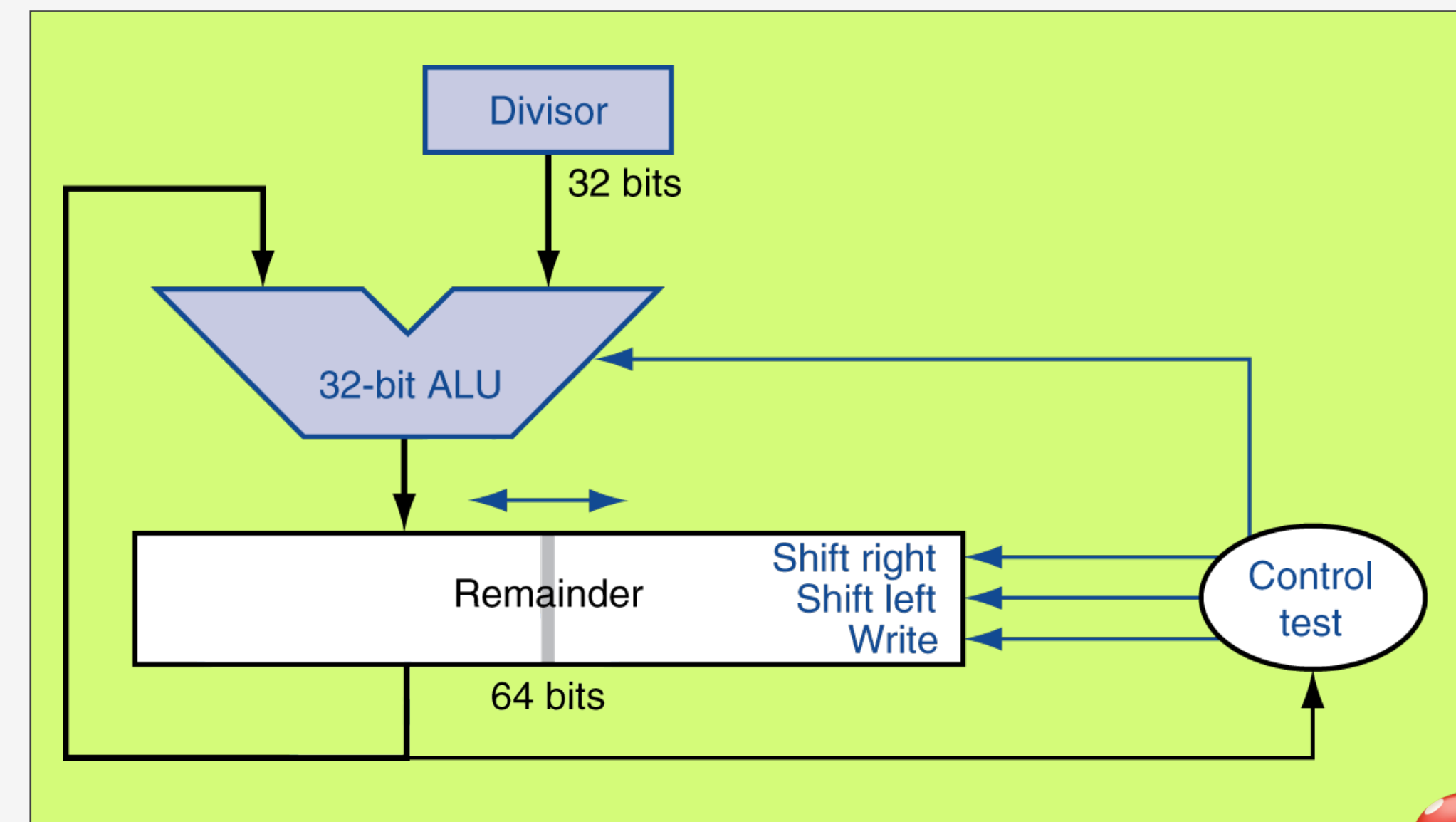
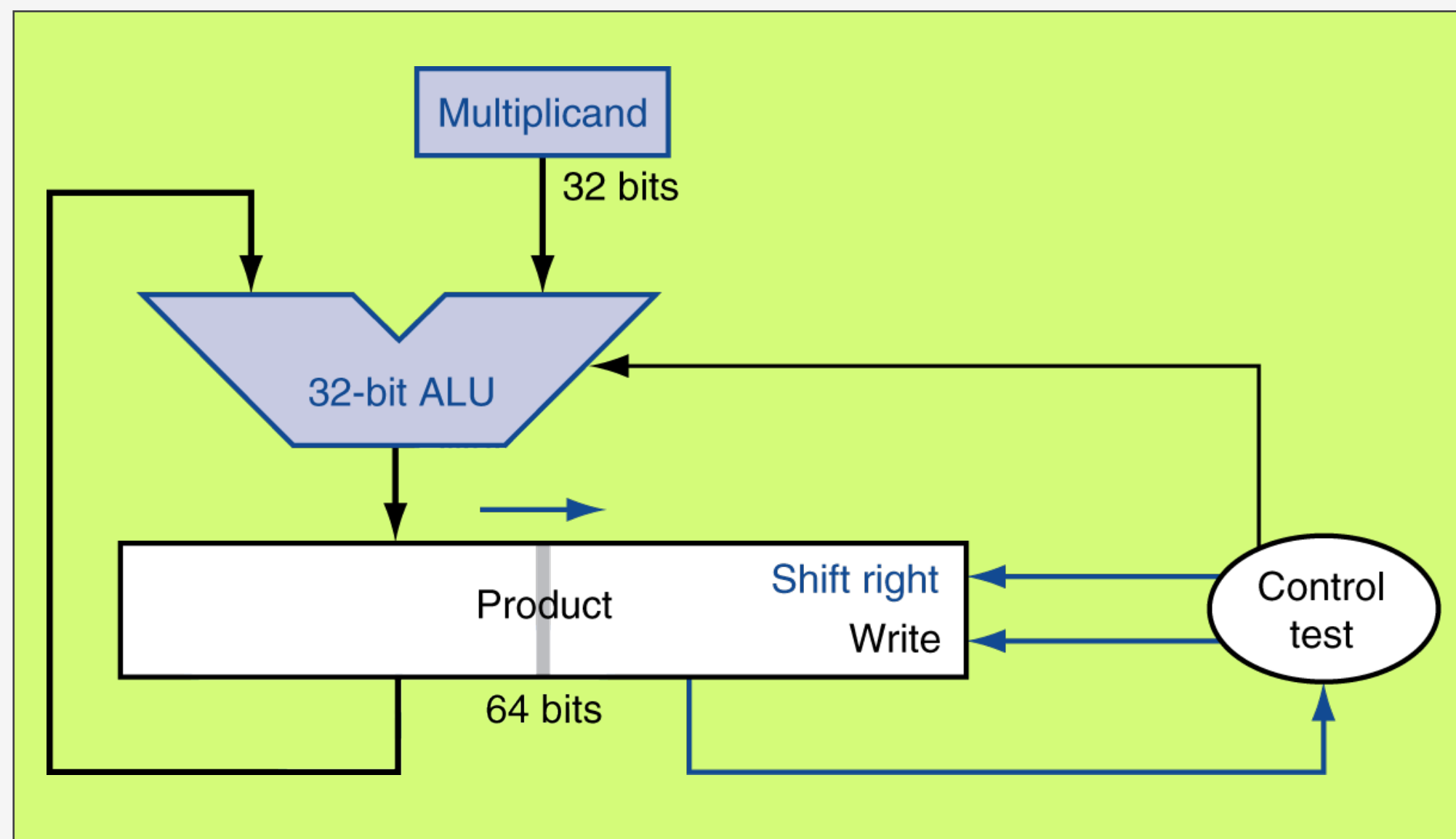
- Reduced hardware requirements
 - Divisor register and ALU now 32-bit
 - Quotient no longer has dedicated register
 - Right half of Remainder register is initialized with dividend, and left half to 0




- When division operation is complete:
 - Left half of Remainder register contains the 32-bit remainder value
 - Right half of the Remainder register contains the 32-bit quotient value
- Only the "shift left" operation is used for the division operation
 - Well, then why is there a "right shift" input?!?!?!?!?

Combined Hardware for Multiplication/Division

- Same hardware can be used for both multiplication and division algorithms
 - Earlier, reduced hardware requirement for each unit when they were optimized for size
 - Now, reusing same hardware for both MUL and DIV further reduces hardware requirements



A Faster Divider

- Multiplication can be parallelized
 - Additional hardware resources can be used to perform multiplication faster
 - Sacrifice size and cost for better performance
- Division cannot be parallelized like multiplication
 - Dividers are slow _ _ _ _ 
 - Only produce a single bit for the quotient on each iteration
 - Other, faster division algorithms do exist, but we won't cover them here

Signed Division

- Recall from grade school arithmetic that the Quotient is negative if the signs of the Dividend and the Divisor differ

positive ÷ positive = positive
negative ÷ negative = positive
positive ÷ negative = negative

- Thus, in hardware:
 - Perform the division algorithm
 - If the sign bits of the dividend and the divisor differ, then negate the quotient
 - Set the sign of the remainder to be the same as the dividend