

# YAN CHENG “YC” POON

+1(734)3538120 | [yanchengpoon@gmail.com](mailto:yanchengpoon@gmail.com) | [ycpoon.github.io](https://ycpoon.github.io) | [linkedin.com/in/yan-cheng-poon/](https://linkedin.com/in/yan-cheng-poon/) |

## EDUCATION

**University of Michigan, Ann Arbor**

Dec. 2025

*Bachelor of Science in Engineering - Computer Engineering, Total Undergraduate CGPA: 3.69*

- Relevant Courses: Computer Architecture, Logic Design (Verilog), Computer Org, Digital Integrated Circuits, Semiconductor Devices
- Focused and Specialized Field: Computer Architecture, VLSI Design
- Dean's List, University Honors, Transferred in as a sophomore from Taylor's University (Best Engineering Student Award)

## WORK EXPERIENCE

**University of Michigan Computer Science and Engineering, Ann Arbor**

Aug. 2024 – Present

*Teaching Assistant, EECS 270: Digital Logic Design*

- Responsible in leading weekly lab sessions, guiding students on RTL design projects in the course, and grading students' designs.
- Supporting the development of the course's Autograder, mainly responsible for structuring test cases using UVM frameworks to verify students' digital designs and working on bash scripts to automate compilation, simulation and synthesis on RTL designs.

**Efinix Inc, Cupertino**

May 2024 – Aug. 2024

*FPGA Post-Silicon Validation & Design for Testability (DFT) Engineering Intern*

- Contributed to the development of the test program for Efinix's Ti375C529 Configurable PLL Duty Cycle Distortion (DCD) IP, involved in the full process including defining test methodologies, implementing RTL designs, running simulations on Cadence Xcelium and QuestaSim, simulation debugging, and VCD conversion to Advantest V39000 tester format.
- Researched and designed a low latency March C variant with 100% coverage in most fault models for Efinix's Memory BIST design.
- Developed Python/Perl scripts automating GPIO assignments and coverage analysis, increasing efficiency of test runs by ~150%
- Gained hands-on experience in JTAG-based debugging, scan insertions, ATPG, & fault simulation using Cadence First Encounter tool
- Collaborated with Design Verification in the testing and verification of Efinix's RISC-V Core and Triple Speed Ethernet MAC Core, assisted in refining UVM testbenches for Efinix's EdgeVision image processing module and speed verification of Ethernet IP.

**University of Michigan Solar Car Team, Ann Arbor**

Aug. 2023 – Present

*Microsystems and Firmware Engineer*

- Led in redesigning the circuit schematics and layout for a PCB that controls the car's lights and turn signals with Altium.
- Analyzed and rewrote the firmware code for the car's light and brake system on STM32Cube to increase response rate by ~120%
- Developed an RTOS-based firmware that handles interrupts and schedules tasks for the MCU based on specific priorities.

**Aerodyne Group, Malaysia**

Jan. 2023 – Mar. 2023

*Tech Research Intern*

- Worked with the project team on the prototype and pseudocode design of a UAS Traffic Management application.
- Contributed to the software integration of infra-red and LiDAR sensors onto drones using Arduino and Embedded C programming.
- Performed research & analysis into emerging drone and chip technologies, tailoring drone solutions to fit clients' needs.

## PROJECTS & EXTRACURRICULAR

### RISC-V In-Order Pipelined Processor

- Developed a pipelined RISC-V processor using SystemVerilog, and synthesized on Synopsys Design Compiler
- Implemented structural, control, data hazard management and forwarding logic, increasing throughput by ~170% for general programs.
- Link to the GitHub repository: [https://github.com/ycpoon/RISCV\\_5\\_Stage\\_Pipelined\\_Processor](https://github.com/ycpoon/RISCV_5_Stage_Pipelined_Processor)

### IP Core Library

- Redesigned various common IP cores in SystemVerilog for additional features or latency/performance improvements.
- Reworked IP cores: Asynchronous High-Speed FIFO, AXI4-Stream Interconnect, Integer Square Root, Arithmetic Calculator etc.
- Link to the Full Library: <https://ycpoon.github.io/iplib/>

### Michigan Hackers - Embedded Systems Team Co-Lead, Ann Arbor

- Led a team of 20 members in building Arduino projects such as an LED roulette machine and a password-protected digital lock.
- Reviewed and improved firmware codes and circuit designs to ensure optimal functionality of the embedded device.
- Spearheaded the software and hardware integration of sensors, cameras, and speakers onto the Arduino project.

### Other Experiences, Personal Projects, and Accomplishments

- Check out <https://ycpoon.github.io/> for the full list of experiences and personal projects.
- *Other Personal Projects:* 1) Worked on a project to build cheap \$80 computers with Raspberry Pi as an initiative to provide underprivileged children with access to computers. 2) Developed an LED roulette game machine with Arduino.

## SKILLS

**Technical Skills:** Verilog/SystemVerilog, VHDL, C/C++, Python, Perl, TCL, Assembly, MATLAB, UNIX/Linux

**Frameworks & Tools:** UVM, VMM, Cadence, Synopsys, Quartus, Vivado, Arduino, Altium, STM32Cube

**Protocols:** AXI4, SPI, UART, I2C, PCIe, Ethernet, TCP/IP, IEEE 802.3

**Language:** English, Chinese, Malay, Cantonese