Y.C. POON

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EDUCATION

University of Michigan, Ann Arbor — Dec. 2025

Bachelor of Science in Engineering - Computer Engineering, Total Undergraduate CGPA: 3.72

- Relevant Courses: Computer Architecture, Logic Design (Verilog), GPU Programming, Integrated Circuits, Semiconductor Devices
- Dean's List, University Honors, Transferred in as a sophomore from Taylor's University (Best Engineering Student Award)

WORK EXPERIENCE

Advanced Micro Devices (AMD) — May 2025 – Aug. 2025

Silicon Design Engineering Intern – Design Verification

- Contributed to the verification flow of a USB xHCI sub-block device reset verification test, including designing test plans based on coverage plan and design specifications, writing UVM test sequences with constrained random sequence items, developing SystemVerilog Assertion (SVA) checkers, debugging testcase failures, performing functional and code coverage analysis, verifying waveform behavior against specification through Verdi, and deploying testcase to regression.
- Assisted in refining UVM monitors by extracting protocol-layer data transaction packets, enabling more detailed debug printing.
- Developed a Python script for parsing post-simulation UVM logs and generating an interactive GUI centralized tracker for USB transactions, comprising of transfers queued in system memory, AXI reads/writes, protocol-level packet exchanges, and more.
- Refactored 1000+ lines of xHCI test sequence library by reorganizing general sequence classes to testcase-specific sequence classes and reconfiguring internal build scripts to support the new structure, improving test clarity and scalability for easier future debugging.

University of Michigan Computer Science and Engineering — Aug. 2024 – Aug. 2025

Teaching Assistant, EECS 270: Digital Logic Design

- Led and guided students on RTL designs, Altera FPGA synthesis using Quartus, and simulation debugging using ModelSim.
- Supported the development of the course's Autograder, mainly responsible for structuring test cases using UVM frameworks to verify students' digital designs and writing Python/Bash scripts to automate compilation, simulation verification and synthesis process.

Efinix Inc. — May 2024 – Aug. 2024

FPGA Post-Silicon Validation & Design for Testability (DFT) Engineering Intern

- Contributed to the development of the test program for Efinix's Ti375C529 Configurable PLL Duty Cycle Distortion (DCD) IP, involved in the full process including defining test methodologies, implementing RTL designs, running simulations on Cadence Xcelium and QuestaSim, simulation debugging, and VCD conversion to Advantest V39000 tester format.
- Researched and designed a low latency March C variant with 100% coverage in most fault models for Efinix's Memory BIST design.
- Developed Python & Perl scripts automating GPIO & PLL, DSP block assignments, increasing efficiency of test runs by ~150%
- Collaborated with the Design Verification team on the verification of Ethernet 10G MAC Core, assisting the team in refining UVM testbenches for improved scoreboard-based protocol adherence check and more comprehensive stress tests sequence generation.

University of Michigan Solar Car Team — Aug. 2023 – May 2024

Microsystems and Firmware Engineer

- Led in redesigning the circuit schematics and layout for a PCB that controls the car's lights and turn signals with Altium.
- Refactored old firmware code and developed an RTOS-based firmware for real-time processing of CAN messages.

PROJECTS & EXTRACURRICULAR

MIPS R10k Style RISC-V Processor

- Designed a 32-bit Out of Order CPU for the RV32I subset with SystemVerilog, synthesizable on Synopsys Design Compiler
- Implemented features including N-way Superscalar Width, Early Tag Broadcasting, Early Branch Resolution, Tournament Branch Predictor, Instruction Prefetcher, Non-Blocking & Banked Caches, full details here: https://ycpoon.github.io/files/470finalreport.pdf
- Developed a comprehensive SystemVerilog Assertion (SVA) suite for verification of internal data structures and cache subsystems.

SystemVerilog IP Core Library

- Redesigned various common IP cores in SystemVerilog for additional features or latency/performance improvements.
- Reworked IP cores: Asynchronous High-Speed FIFO using CDC, AXI4-Stream Interconnect, Efficient Parameterizable Priority Selector, Integer Square Root, Low Latency Memory BIST Design, BRAM Wrapper, Link to Library: https://ycpoon.github.io/iplib/

Other Experiences, Personal Projects, and Accomplishments

- Check out https://ycpoon.github.io/ for the full list of experiences and personal projects.
- *Leadership Experiences:* 1) MHackers Embedded Systems Team Lead. 2) IEEE Corporate Relations Officer
- *Other Personal Projects:* 1) Worked on a project to build cheap $80 computers with Raspberry Pi as an initiative to provide underprivileged children with access to computers. 2) Developed an LED roulette game machine with Arduino.

SKILLS

Technical Skills: Verilog/SystemVerilog, VHDL, C, C++, Python, Perl, Tcl, RISC-V, ARM Assembly, MATLAB, UNIX/Linux
Frameworks: Universal Verification Methodology (UVM), SystemVerilog Assertions (SVA), CUDA, STM32Cube
Tools: Synopsys VCS, Synopsys Design Compiler, Verdi, Quartus (Altera), Vivado (Xilinx), Cadence Virtuoso, Altium, Git
Protocols: AXI4 Stream/Memory-Mapped/Lite, SPI, UART, I2C, USB, SerDes, PCIe, Ethernet, TCP/IP, UDP, RGMII