YAN CHENG "YC" POON

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EDUCATION

University of Michigan, Ann Arbor **Dec. 2025**

Bachelor of Science in Engineering - Computer Engineering, Total Undergraduate CGPA: 3.71

- Relevant Courses: Parallel Computer Architecture, Microarchitecture, Computer Architecture, Logic Design (Verilog), GPU Programming, Operating Systems, Integrated Circuits, Semiconductor Devices, Data Structures & Algorithm
- Dean's List, University Honors, Transferred in as a sophomore from Taylor's University (Best Engineering Student Award)

WORK EXPERIENCE

Advanced Micro Devices (AMD) **May 2025 – Aug. 2025**

Silicon Design Engineering Intern – Design Verification

- Contributed to the verification flow of a USB host controller (xHCI) sub-block device reset verification test, including designing test plans based on coverage plan and design specifications, writing UVM test sequences with constrained random sequence items, developing SystemVerilog Assertion (SVA) checkers, debugging testcase failures, performing functional and code coverage analysis, verifying waveform behavior against specification through Verdi, and deploying testcase to regression.
- Assisted in refining UVM monitors by extracting protocol-layer data transaction packets, enabling more detailed debug printing.
- Developed a Python script for parsing post-simulation UVM logs and generating an interactive GUI centralized tracker for USB transactions, comprising of transfers queued in system memory, AXI reads/writes to DMA, protocol-level packet exchanges, and more.
- Refactored 1000+ lines of xHCI test sequence library by reorganizing general sequence classes to testcase-specific sequence classes and reconfiguring internal build scripts to support the new structure, improving test clarity and scalability for easier future debugging.

University of Michigan Computer Science and Engineering **Aug. 2024 – Present**

Teaching Assistant, EECS 270: Digital Logic Design

- Led and guided students on RTL designs, Altera FPGA synthesis using Quartus, and simulation debugging using ModelSim.
- Supported the development of the course's Autograder, mainly responsible for structuring test cases using UVM frameworks to verify students' digital designs and writing Python/Bash scripts to automate compilation, simulation verification and synthesis process.

Efinix Inc. **May 2024 – Aug. 2024**

FPGA Post-Silicon Validation & Design for Testability (DFT) Engineering Intern

- Contributed to the development of the test program for Efinix's Configurable PLL Duty Cycle Distortion (DCD) IP, involved in the full process including defining test methodologies, implementing RTL designs, running simulations on Cadence Xcelium and QuestaSim, simulation debugging, and VCD conversion to Advantest V39000 tester format.
- Researched and designed a low latency March C variant with 100% coverage in most fault models for Efinix's Memory BIST design.
- Developed Python & Perl scripts automating GPIO & PLL, DSP block assignments, increasing efficiency of test runs by ~150%
- Assisted the DV team briefly in the refinement of UVM scoreboard RGMII/GMII/MII protocol checkers for Ethernet-based IPs.

PROJECTS & EXTRACURRICULAR

32-bit RISC-V Out-of-Order Processor (based on the MIPS R10000 architecture)

- Implemented the CPU design with SystemVerilog, simulated with Synopsys VCS and synthesized with Synopsys Design Compiler, CPU achieved ~3.5x speedup over in-order processor design, GitHub repo: https://github.com/ycpoon/MIPS_R10K_RISCV_Processor
- Implemented features including N-way Superscalar Width, Early Tag Broadcasting, Early Branch Resolution, Tournament Branch Predictor, Instruction Prefetcher, Non-Blocking & Banked Caches, full details here: https://ycpoon.github.io/files/470finalreport.pdf
- Developed a comprehensive SystemVerilog Assertion (SVA) suite for verification of internal data structures and cache subsystems.

SystemVerilog IP Core Library

- Redesigned common IP cores in SV for additional features or latency/performance improvements, such as AXI-Stream Interconnect IP, full-duplex RGMII-interfaced Ethernet MAC Core with CRC checker/generator, and an efficient FSM-based Round-Robin Arbiter.
- Other reworked IP cores: Asynchronous High-Speed FIFO using CDC, RISC-V In-Order Processor, Efficient Parameterizable Priority Selector, Integer Square Root, Efficient Four Function ALU (Add/Sub/Multiply/Divide), Link to Library: https://ycpoon.github.io/iplib/

Other Extracurricular, Leadership Experiences, and Personal Projects

- Check out https://ycpoon.github.io/projects/ for full list of projects and https://ycpoon.github.io/experiences/ for full list of experiences
- ***Extracurricular Experience*:** UMich Solar Car Team Microsystems and Firmware Engineer – Designed circuit schematics and layout for car lighting and braking system PCB and refactored 700+ lines of code of a RTOS-based firmware for CAN messages processing.
- ***Leadership Experiences:*** 1) MHackers Embedded Systems Team Lead. 2) IEEE Corporate Relations Officer
- ***Other Personal Projects:*** 1) Worked on a project to build cheap $80 computers with Raspberry Pi as an initiative to provide underprivileged children with access to computers. 2) Developed an LED roulette game machine with Arduino.

SKILLS

Technical Skills: Verilog/SystemVerilog, C, C++, Python, Perl, Tcl, RISC-V, ARM Assembly, MATLAB, Shell Scripting
Frameworks: Universal Verification Methodology (UVM), SystemVerilog Assertions (SVA), CUDA, STM32Cube, POSIX/Boost Threads
Tools: Synopsys VCS, Synopsys Design Compiler, Verdi, Git, UNIX/Linux, Quartus (Altera), Vivado (Xilinx), Cadence Virtuoso, Altium
Protocols: AXI4 Stream/Memory-Mapped/Lite, SPI, UART, I2C, USB, PCIe, Ethernet, TCP/IP, UDP, RGMII/GMII/MII