Parallel Physical Design Automation System

Partitioning and Floorplanning

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ABSTRACT

Physical Design Automation (PDA) is a crucial step in the Electronic Design Automation (EDA) process, involving the transformation of high-level logical designs into actual hardware layouts. The primary goal of physical design is to ensure that the design has good performance, timing, power consumption, and signal integrity on the chip or circuit board while meeting physical constraints and manufacturing requirements. Modern Very Large Scale Integration (VLSI) circuits have over 10,001 to 100,000 transistors, and as the manufacturing process advances, the number of transistors on a single chip also increases. Using traditional PDA processes would consume a significant amount of verification time. Therefore, we designed a parallelized PDA system that can substantially speed up the chip verification process. The parallelized PDA system can be applied not only to VLSI design but also to system-on-chip (SOC) design and complex scenarios like system-level packaging. It represents a direction of continuous innovation in the EDA field to address the challenges of modern electronic design while shortening the time-to-market and enhancing the competitiveness of chip products.

KEYWORDS

Parallel System, Physical Design Automation, Partitioning, Floorplanning, CUDA, OpenMP

1 Introduction

Modern electronic design continuously pursues higher performance, lower power consumption, and quicker time-to-market, posing significant challenges for handling Very Large Scale Integration (VLSI) designs. In traditional Physical Design Automation process, verifying and optimizing VLSI circuits usually require consuming substantial time and computational resources. To address this challenge, we propose a new design project aimed at implementing a "parallelized Physical Design Automation system." This approach aims to accelerate design verification, enhance design quality, and shorten the time-to-market.

2 Motivation

Increased Complexity of Very Large Scale Integration (VLSI) Circuits: The number of transistors in modern VLSI designs is continuously increasing, leading to a dramatic rise in design complexity. Traditional design methods have become insufficiently efficient in handling this complexity.

- **Market Competitive Pressure:** The market is increasingly urgent in its demand for new products, especially in the consumer electronics, communications, and automotive industries. Shortening the design cycle has become crucial to quickly meet market demands. **Products that complete the design and production stages earlier may gain a competitive advantage of about 15%, signifying that quickly completing the design and launching it in the market is vital, which is a primary benefit of the parallelized chip design process**.
- **Resource Optimization:** Utilizing multi-core processors and distributed computing resources can handle large designs more effectively, thus saving computational time and resource costs.
- **Design Quality and Reliability:** Rapid design verification not only saves time but also offers more opportunities for design optimization to improve performance, power consumption, and reliability.
- **Technological Forefront:** Implementing a parallelized Physical Design Automation system represents continuous innovation in the EDA field to address the ever-changing hardware and software technologies. In this project, we will explore a parallelized Physical Design Automation system to meet the challenges of modern electronic design, accelerate design verification, enhance competitiveness, and enable products to enter the market more quickly.

3 Contribution

Our proposed research project, "Parallelized Physical Design Automation System," has the following contributions:

1. Develop a parallelized Physical Design Automation system that effectively utilizes multi-core processors and distributed computing environments to accelerate the design verification and optimization process.
2. Improving design efficiency by applying parallel processing and optimization algorithms, significantly shortening the time of the design process, and enabling chip design engineers to obtain design results more quickly.

3. Shortening time-to-market, providing a faster Physical Design Automation process, which helps reduce the product's time-to-market, essential for dealing with market competitive pressures and meeting customer demands.
4. Having scalability, applicable to Very Large Scale Integration circuits, including a vast number of components, complexity, and high-performance requirements. It is also portable for future chip designs and verifications with an increasing number of transistors.

In conclusion, the main contribution of this research project is to develop a highly parallelized Physical Design Automation process to handle the design challenges of Very Large Scale Integration circuits, thereby improving design efficiency, enhancing design quality, and reducing time-to-market. This is of significant importance in the modern electronic design field, promoting technological development and improving market competitiveness.

4 Statement of the Problem

The Physical Design Automation process is broadly divided into five steps: Partitioning, Floorplanning, Placement, Routing, and Post-layout Optimization.

1. **Partitioning** - Partitioning is the first step in the physical design process, where a large circuit is divided into smaller circuits or Modules, making subsequent design steps easier. Nowadays, the goal and main use of this phase are to split a large circuit into circuits that an FPGA (Field Programmable Gate Array) can accommodate and use multiple FPGAs to verify circuit behavior.
2. **Floorplanning** - The floorplanning stage involves defining the physical areas of each partition, i.e., the position of the Module pins, the physical area, and the relative positions between Modules. During floorplanning, considerations include the circuit's size, shape, connectivity requirements, and other constraints such as heat dissipation and signal integrity. The goal of this stage is to achieve minimal area consumption, the lowest power consumption, and the best timing performance.
3. **Placement** - Placement involves positioning the components of the circuit within specified areas of the layout. Placement tools usually consider inter-component connectivity requirements, signal integrity, power consumption, and heat dissipation to ensure optimized placement. The goal of this stage is to achieve an optimal layout that meets performance objectives and complies with constraints.
4. **Routing** - The Routing stage involves determining and creating physical connections between components to realize signal paths in the design. Routing tools must resolve path conflicts, timing issues, and signal integrity problems, optimizing connection lengths and delays. The goal of this stage is to achieve reliable connections while meeting performance and power consumption requirements.
5. **Post-layout Optimization** - Post-layout optimization is an additional step used to improve the performance and power consumption of the completed layout. It may include timing optimization, power optimization, electromagnetic compatibility analysis, and other performance improvement techniques. The goal of this stage is to further optimize the circuit to meet stricter design requirements while keeping the layout unchanged.

4.1 Problem

In our current research project, we will target **Partitioning** and **Floorplanning** for parallelization.

A. Partitioning

Modern large-scale integrated circuits are already too large to be implemented and verified in a single FPGA. Therefore, we need to consider how to effectively divide the circuit so that it can be verified and simulated in multiple FPGAs. We must meet the following conditions:

1. Minimize the connections between divided circuits
2. Satisfy the area size constraints of the circuits after partitioning

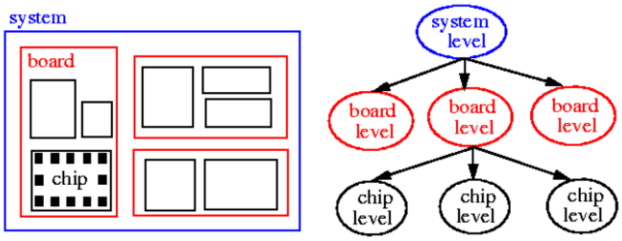

Figure 1: The levels of partitioning: system, board, chip

The decomposition of complex systems into smaller subsystems in integrated circuit design is achieved through the partitioning process. Traditional partitioning processes sequentially and incrementally split the integrated circuit, while parallelized partitioning implies considering the partitioning of multiple sub-circuits simultaneously, rather than handling them one after another. Parallelized partitioning helps improve the efficiency of the entire process, better meet the needs of large-scale circuit design, and ensure the success and efficiency of the entire design process.

B. Floorplanning

The number of modules in modern large-scale integrated circuits is increasing, so we need to consider how to effectively carry out floorplanning, and the following conditions must be met:

1. The circuit area completed by floorplanning should be as small as possible.
2. The overall circuit's physical wires should be as short as possible.

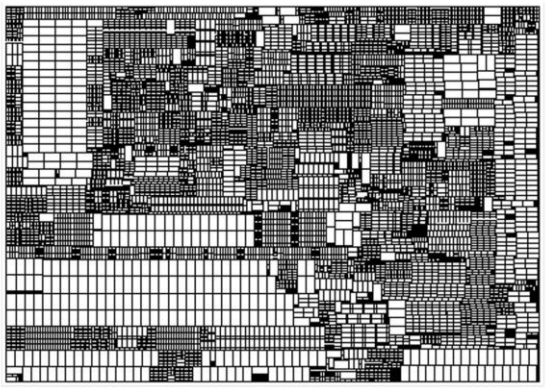

Figure 2: Layout of ami49_200

Parallelized floorplanning allows for the simultaneous handling of the layout of multiple regions, accelerating the speed of layout planning and reducing the time of the entire design process. It considers the layout of multiple areas simultaneously and uses highly complex algorithms to optimize the layout. This helps improve layout quality, ensuring that various design goals such as performance, power consumption, and area are met.

5 Proposed Approaches

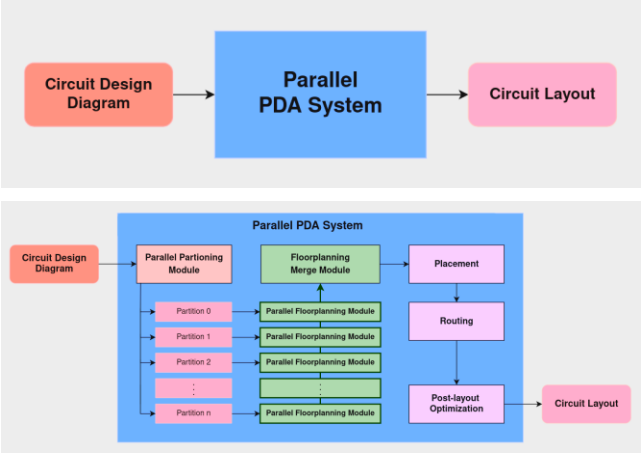

Figure 3: The Architecture Diagram of Parallel PDA System

The input consists of the basic circuit information such as modules of the circuit (length, width, pin positions, etc.) and the connectivity status between pins. First, it goes through the **Parallel Partitioning Module**, which is divided into multiple Partitions. Each Partition is then processed by the **Parallel Floorplanning Module** into several sub-circuits that have completed floorplanning. Finally, the **Floorplanning Merge Module** hierarchically combines them into a complete circuit. After going through Placement, Routing, and Post-layout Optimization steps, the circuit Layout is generated.

6 Language Selection

We will use C++ to program our design. The reason is we implement this research by CUDA and OpenMP. Because modern EDA applications and these parallel tools are most using C++ language. It will be convenient if we use C++ to work.

7 Related Work

Hardware Acceleration of EDA Algorithms, published by Kanupriya Gulati and Sunil P. Khatri in 2010.

(https://link.springer.com/book/10.1007/978-1-4419-0944-2)

Provides guidelines on whether to use GPUs or FPGAs when accelerating a given EDA algorithm, with validation by a concrete example implemented on both platforms.

Demonstrates the acceleration of several popular EDA algorithms on GPUs, with speedups from 30X to 800X presents techniques in a way that the reader can use example algorithms presented to determine how best to accelerate their specific EDA algorithm.

8 Statement of Expected Results

Comparing the traditional sequentially executed partitioning and floorplanning processes with our designed parallelized partitioning and floorplanning processes, the expected result is that the Parallel PDA System can effectively enhance the speed of PDA design. Especially when dealing with larger-scale circuit data, the benefits of parallelization will become more apparent. This is because our parallelization method allows for the simultaneous processing of multiple sub-circuit partitions and floorplanning, thereby utilizing computational resources more effectively and accelerating the entire design process.

Moreover, as modern GPUs (Graphics Processing Units) have a substantial number of computing cores, we anticipate that the parallelization benefits brought by CUDA (Compute Unified Device Architecture) will surpass those of other parallelization tools like OpenMP. CUDA can utilize the multi-core architecture of GPUs more effectively, further increasing computational speed, making it particularly suitable for Physical Design Automation tasks requiring extensive parallel computations.

In conclusion, we expect the Parallel PDA System to bring significant speed improvements to PDA design, especially when handling large-scale circuit data and anticipate that using CUDA parallelization methods will play a crucial role in enhancing efficiency.

9 Timetable

Time	Milestone
11/3-11/9	Reading Related Papers
11/10-11/16	Implement Non-Parallel Partition Algorithm
11/17-11/23	Implement Non-Parallel Floorplanning Algorithm
11/24-11/30	Plan Parallel Partition & Floorplanning Method
12/1-12/7	Implement Parallel Partition & Floorplanning Algorithm (1/2)
12/8-12/14	Implement Parallel Partition & Floorplanning Algorithm (2/2)
12/15-12/21	Evaluate the Performance
12/22-12/28	How to Improve
12/29-1/4	Prepare for Presentation

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