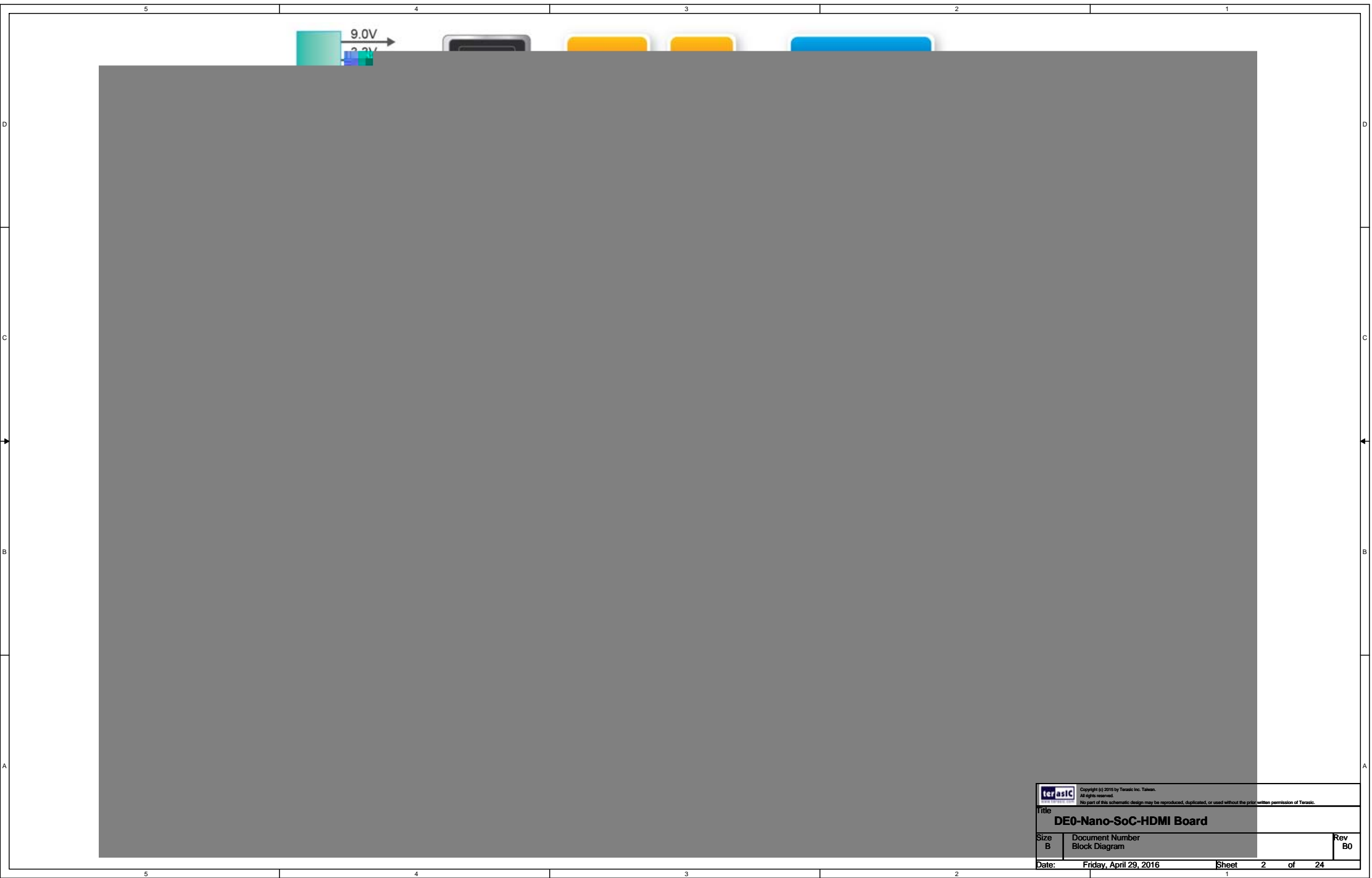
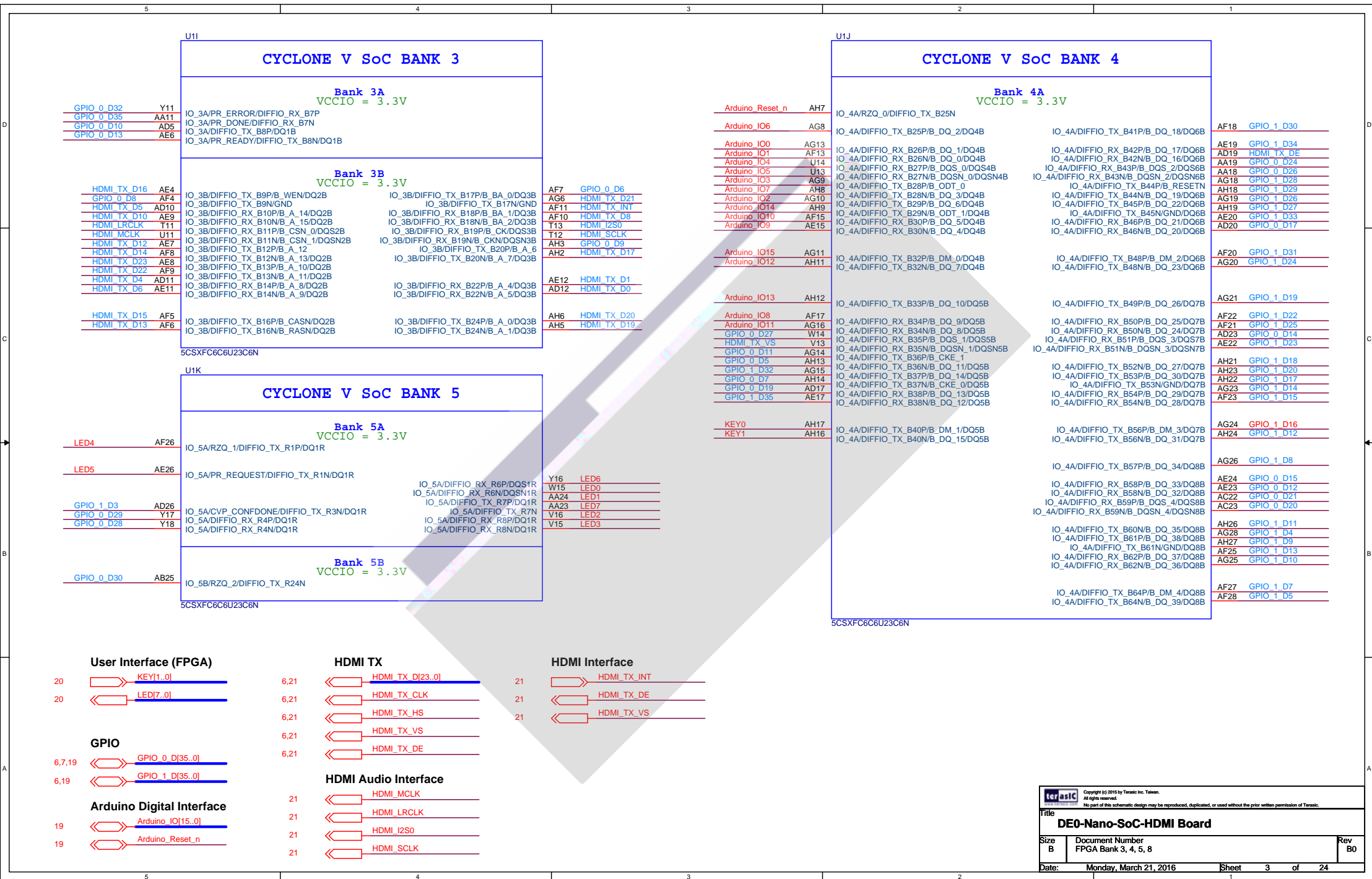
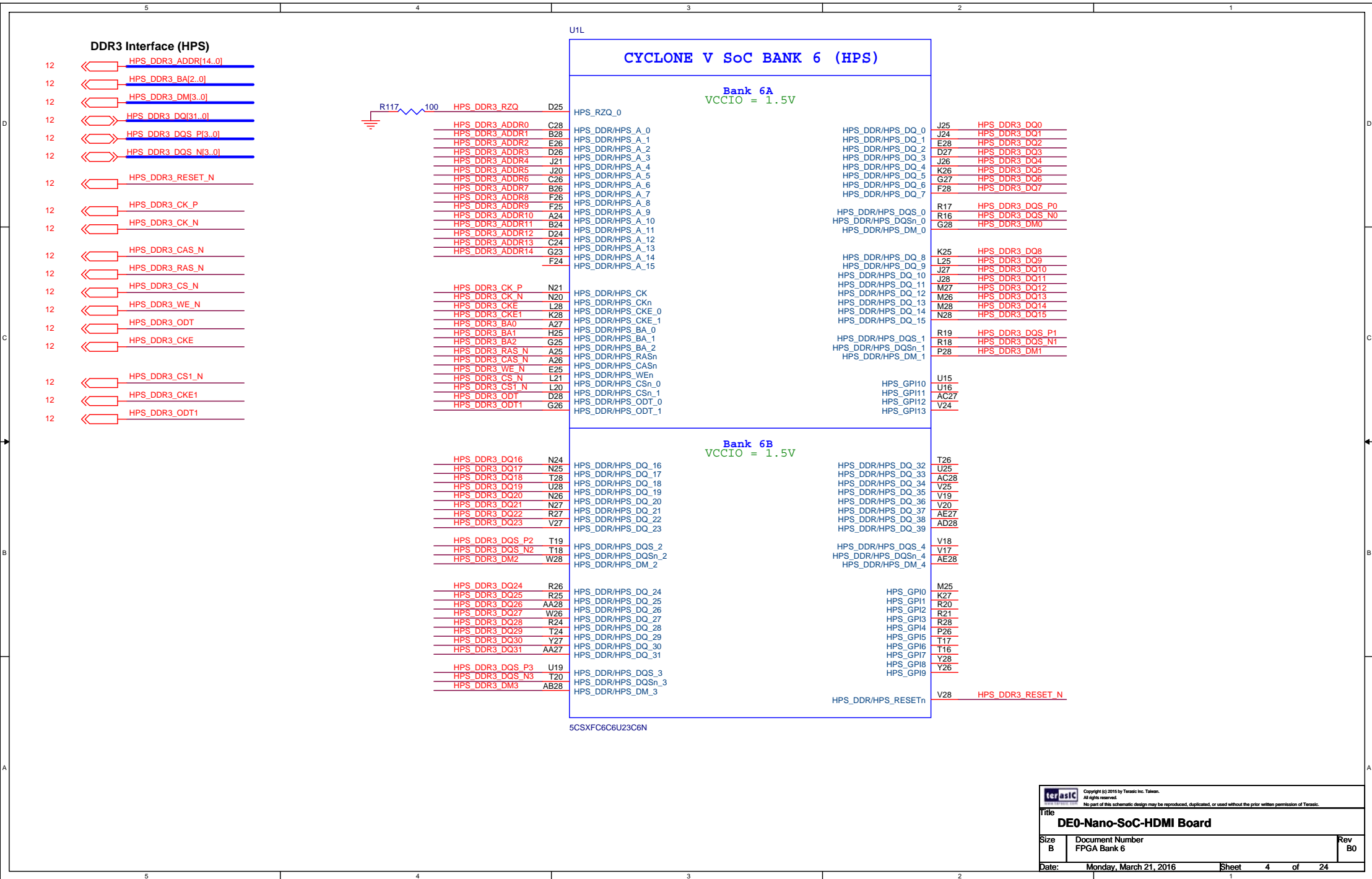


Cyclone V SoC Development & Education Board (DE0-Nano-SoC-HDMI)

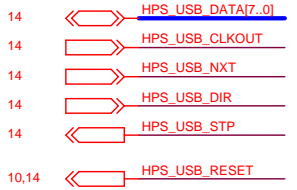
PAGE	CONTENT
01	Cover Page
02	Block Diagram
03	FPGA IO Bank3, 4, 5 and 8
04	FPGA IO Bank 6 (HPS DDR3)
05	FPGA IO Bank 7 (HPS Peripheral Device)
06	FPGA Clock In/Out and Clock Generator
07	FPGA Configuration and EPCS device
08	FPGA Power
09	FPGA Decoupling
10	USB Blaster II
11	JTAG Chain
12	HPS Peripheral : DDR3 SDRAM
13	HPS Peripheral : UART to USB and SD Card Socket
14	HPS Peripheral : USB OTG
15	HPS Peripheral : Gigabit Ethernet
16	HPS Peripheral : Accelerometer & LTC Expansion Header
17	HPS Peripheral : Reset Circuit, Button and LED
18	FPGA : ADC1 (LTC2308) for 8-channel Analog Expansion Header and Arduino Analog input
19	FPGA : GPIO, Analog and Arduino UNO Expansion Header
20	FPGA : Button, Switch and LED
21	FPGA : HDMI TX
22	Power - 1.1V, 5V
23	Power - 2.5V, 3.3V
24	Power - 1.2V, 1.5V, 1.8V, 9V



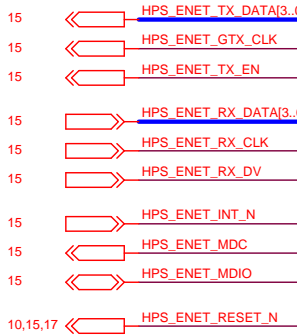




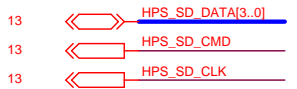
UBS PHY Interface (ULPI)



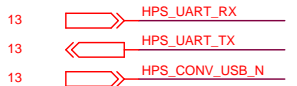
Ethernet PHY Interface (RGMII)



SD Card Interface



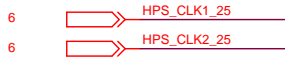
UART Interface



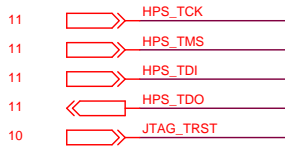
HPS Reset



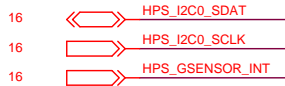
HPS Clock



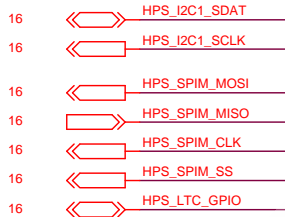
HPS JTAG INTERFACE



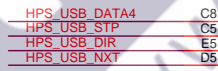
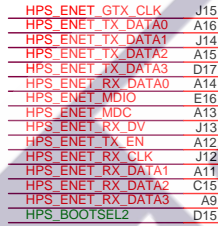
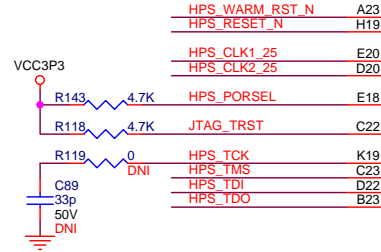
Accelerometer Interface



LTC Interface



HPS Key and LED



U1M

CYCLONE V SoC BANK 7 (HPS)

Bank 7A
VCCIO = 3.3V



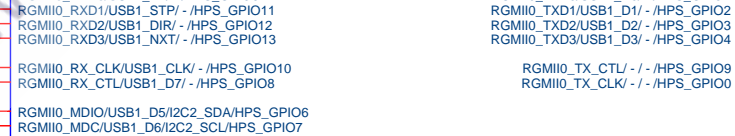
Bank 7B
VCCIO = 3.3V



Bank 7C
VCCIO = 3.3V

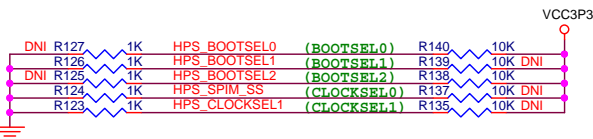


Bank 7D
VCCIO = 3.3V

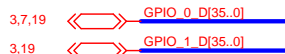


5CSXFC6C6U23C6N

Default Setting: BOOTSEL[2:0]=101 (Boot from SD CARD)
CLKSEL[1:0] =00



GPIO



User Interface (FPGA)



FPGA_CLK1_50 V11
 GPIO_0_D25 W11
 GPIO_0_D0 V12
 GPIO_0_D2 W12

FPGA_CLK2_50 Y13
 GPIO_0_D34 AA13
 GPIO_1_D0 Y15
 GPIO_1_D2 AA15

SW0 Y24
 SW1 W24
 SW2 W21
 SW3 W20

FPGA_CLK1_50 R159 0
 GPIO_0_D3 D11
 GPIO_0_D16 D12
 GPIO_0_D18 C12

FPGA_CLK3_50 E11
 GPIO_0_D3 D11
 GPIO_0_D16 D12
 GPIO_0_D18 C12

CYCLONE V SoC Clock

Bank 3B VCCIO = 3.3V

IO_3B/CLK0P,FPLL_BL_FBP/DIFFIO_RX_B15P
 IO_3B/CLK0N,FPLL_BL_FBN/DIFFIO_RX_B15N
 IO_3B/CLK1P/DIFFIO_RX_B23P
 IO_3B/CLK1N/DIFFIO_RX_B23N

AG5 HDMI_TX_CLK
 AH4 HDMI_TX_D18

Bank 4A VCCIO = 3.3V

IO_4A/CLK2P/DIFFIO_RX_B31P
 IO_4A/CLK2N/DIFFIO_RX_B31N
 IO_4A/CLK3P/DIFFIO_RX_B39P
 IO_4A/CLK3N/DIFFIO_RX_B39N

Bank 5B VCCIO = 3.3V

IO_5B/CLK4P,FPLL_BR_FBP/DIFFIO_RX_R23P
 IO_5B/CLK4N,FPLL_BR_FBN/DIFFIO_RX_R23N
 IO_5B/CLK5P/DIFFIO_RX_R21P
 IO_5B/CLK5N/DIFFIO_RX_R21N

AB26 GPIO_0_D31
 AA26 GPIO_0_D33

Bank 8A VCCIO = 3.3V

IO_8A/CLK6P,FPLL_TL_FBP/DIFFIO_RX_T9P
 IO_8A/CLK6N,FPLL_TL_FBN/DIFFIO_RX_T9N
 IO_8A/CLK7P/DIFFIO_RX_T1P
 IO_8A/CLK7N/DIFFIO_RX_T1N

E8 GPIO_0_D1
 D8 GPIO_0_D4

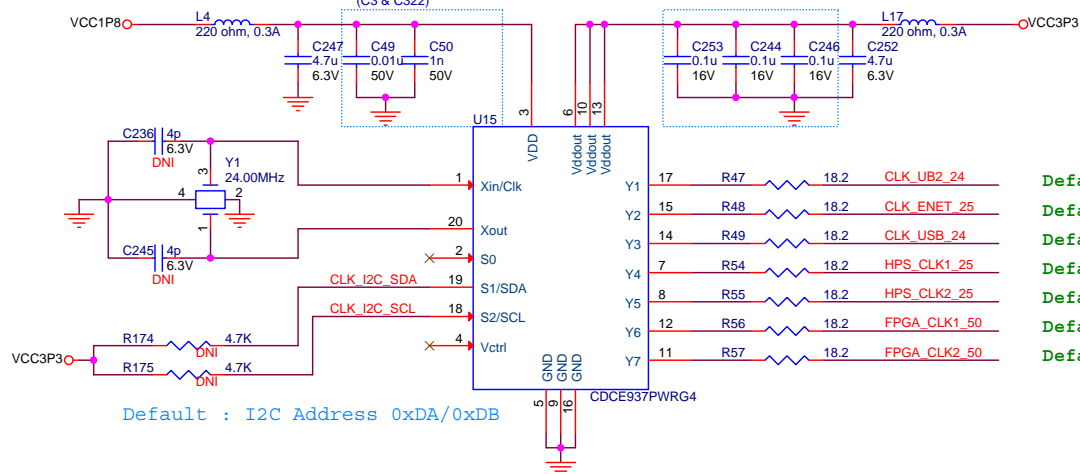
5CSXFC6C6U23C6N

Factory Default Configuration:

50MHz x2
 25MHz x3
 24MHz x2

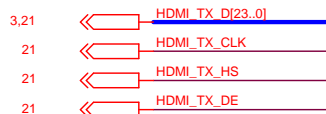
CAD Note:
 Place near pin 3 and 5
 (C3 & C322)

CAD Note:
 Place near IC power pin

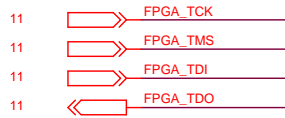


Default : I2C Address 0xDA/0xDB

HDMI TX



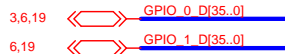
FPGA JTAG INTERFACE



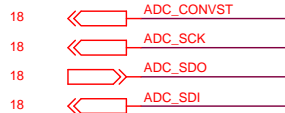
USB Blaster



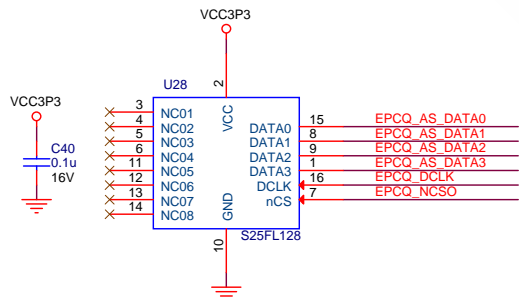
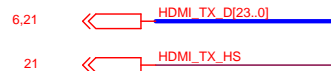
GPIO



ADC



I2C Interface



U1A

CYCLONE V SoC Configuration

Bank 3A
VCCIO = 3.3V

TCK
TMS
TDI
TDO
DCLK

AS_DATA0/ASDO/DATA0
AS_DATA1/DATA1
AS_DATA2/DATA2
AS_DATA3/DATA3

NCSO/DATA4

IO_3A/DATA5/DIFFIO_TX_B2N
IO_3A/DATA6/DIFFIO_RX_B1N/DQ1B
IO_3A/DATA7/DIFFIO_TX_B2P/DQ1B
IO_3A/DATA8/DIFFIO_RX_B1P/DQ1B
IO_3A/DATA9/DIFFIO_TX_B4N/DQ1B
IO_3A/DATA10/DIFFIO_RX_B3N/DQS1B
IO_3A/DATA11/DIFFIO_TX_B4P
IO_3A/DATA12/DIFFIO_RX_B3P/DQS1B
IO_3A/DATA13/DIFFIO_TX_B6N/DQ1B
IO_3A/DATA14/DIFFIO_RX_B5N/DQ1B
IO_3A/DATA15/DIFFIO_TX_B6P/DQ1B
IO_3A/CLKUSR/DIFFIO_RX_B5P/DQ1B

Bank 5A
VCCIO = 3.3V

IO_5A/INIT_DONE/DIFFIO_RX_R2P
IO_5A/DEV_OE/DIFFIO_TX_R5P
IO_5A/DEV_CLRN/DIFFIO_TX_R5N/DQ1R
IO_5A/CRC_ERROR/DIFFIO_RX_R2N
IO_5A/nCEO/DIFFIO_TX_R3P/DQ1R

Bank 9A
VCCIO = 3.3V

CONF_DONE

nSTATUS

nCONFIG

nCE

MSEL0

MSEL1

MSEL2

MSEL3

MSEL4

5CSXFC6C6U23C6N

U1N

CYCLONE V SoC BANK XCVR

Bank GXB_L0

GXB_RX_L0n,GXB_REFCLK_L0n
GXB_RX_L0p,GXB_REFCLK_L0p
GXB_RX_L1n,GXB_REFCLK_L1n
GXB_RX_L1p,GXB_REFCLK_L1p
GXB_RX_L2n,GXB_REFCLK_L2n
GXB_RX_L2p,GXB_REFCLK_L2p

GXB_TX_L0p
GXB_TX_L0n
GXB_TX_L1p
GXB_TX_L1n
GXB_TX_L2p
GXB_TX_L2n

REFCLK0Lp
REFCLK0Ln

Bank GXB_L1

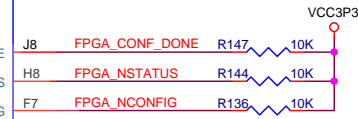
GXB_RX_L3n,GXB_REFCLK_L3n
GXB_RX_L3p,GXB_REFCLK_L3p
GXB_RX_L4n,GXB_REFCLK_L4n
GXB_RX_L4p,GXB_REFCLK_L4p
GXB_RX_L5n,GXB_REFCLK_L5n
GXB_RX_L5p,GXB_REFCLK_L5p

GXB_TX_L3p
GXB_TX_L3n
GXB_TX_L4p
GXB_TX_L4n
GXB_TX_L5p
GXB_TX_L5n

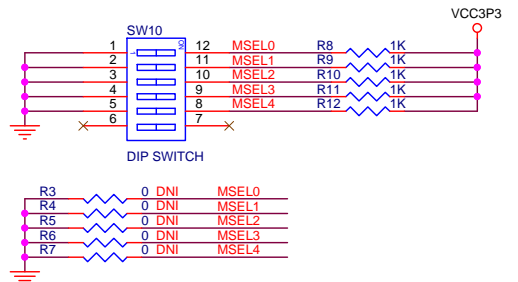
REFCLK1Lp
REFCLK1Ln

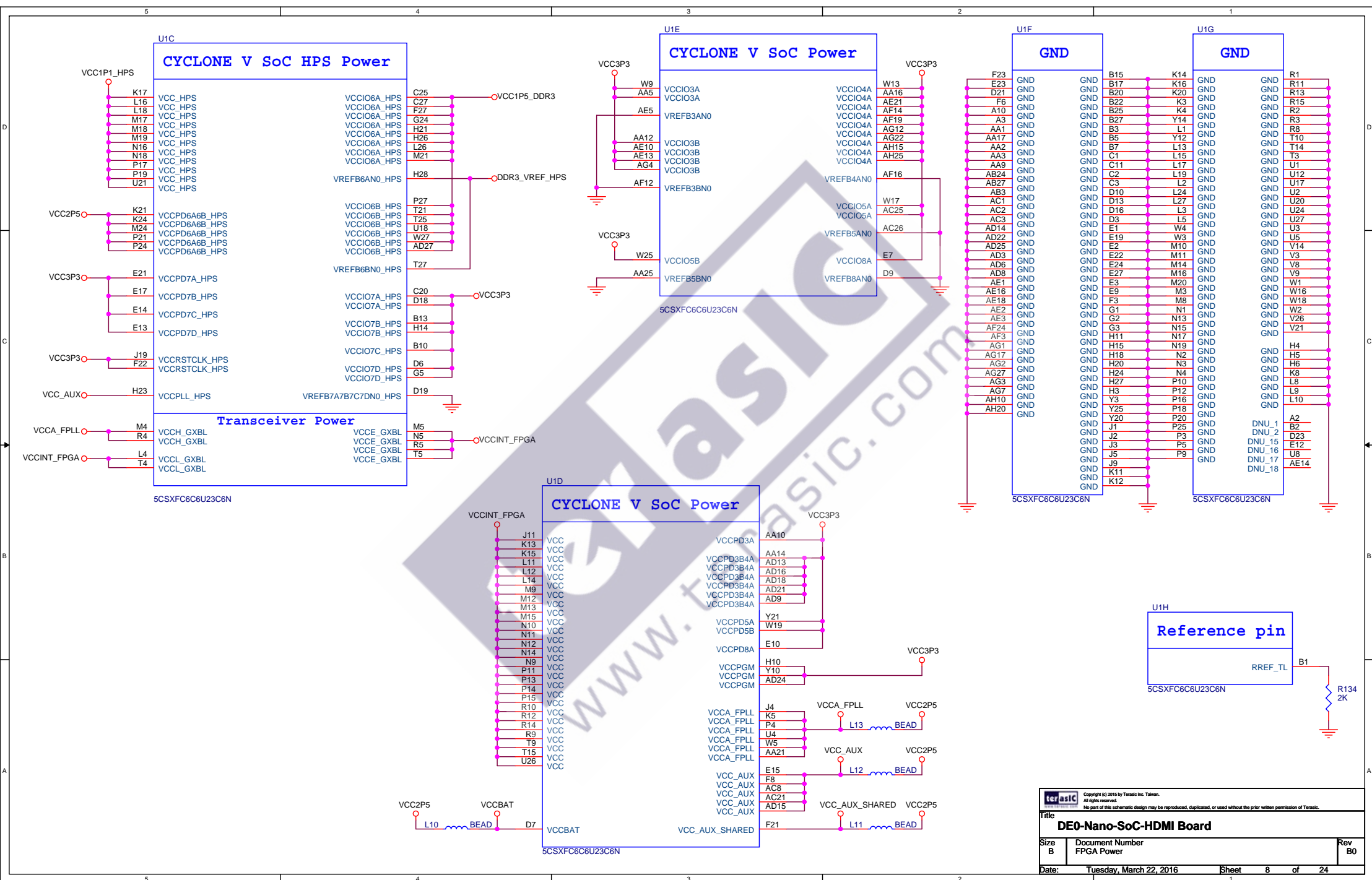
5CSXFC6C6U23C6N

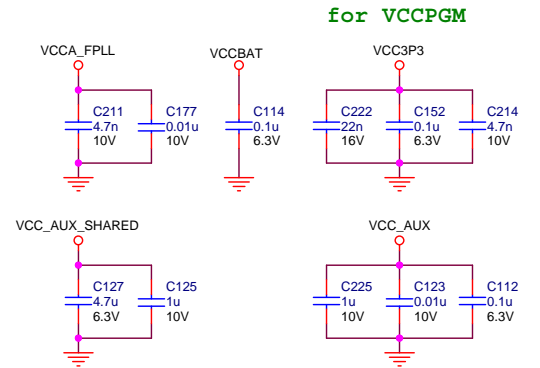
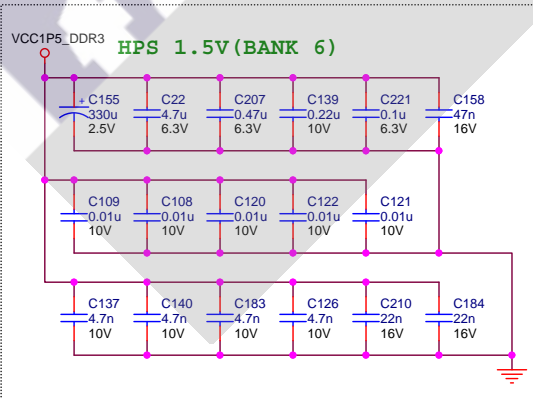
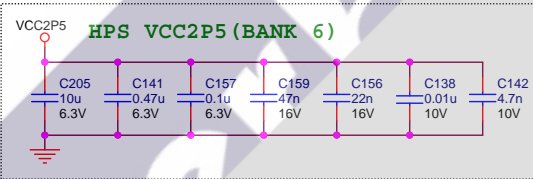
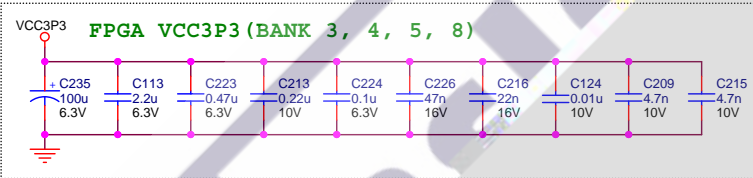
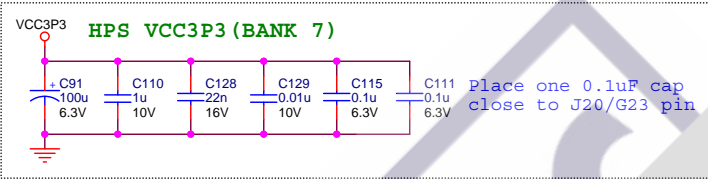
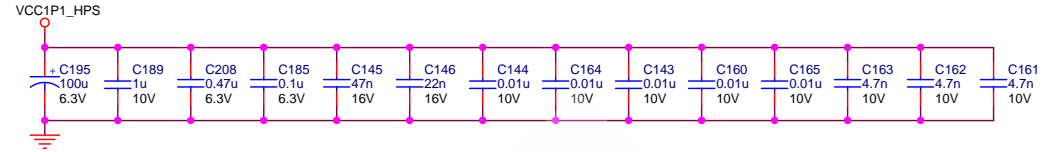
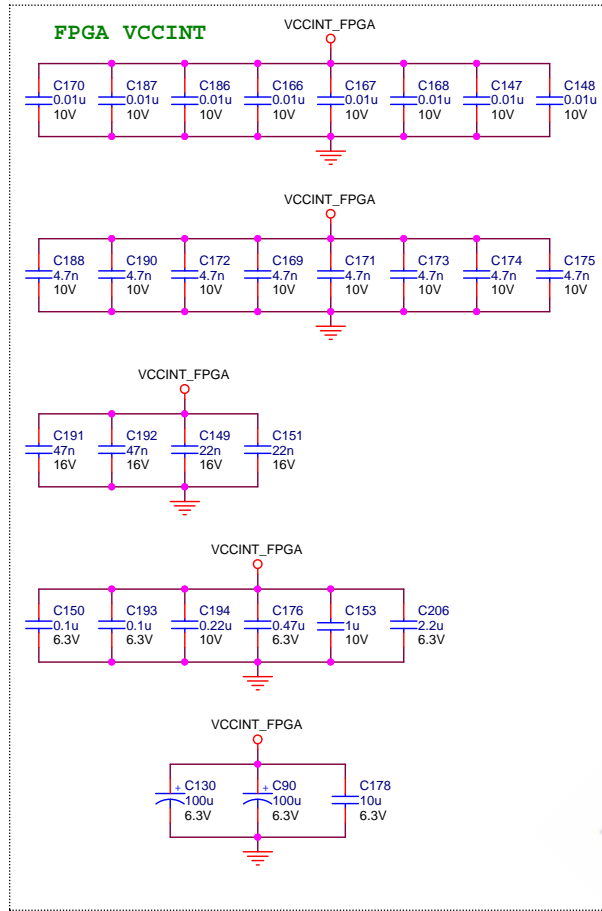
AA20 GPIO_1_D21
AC24 GPIO_1_D1
AB23 GPIO_0_D23
Y19 GPIO_0_D22
AE25 GPIO_1_D6

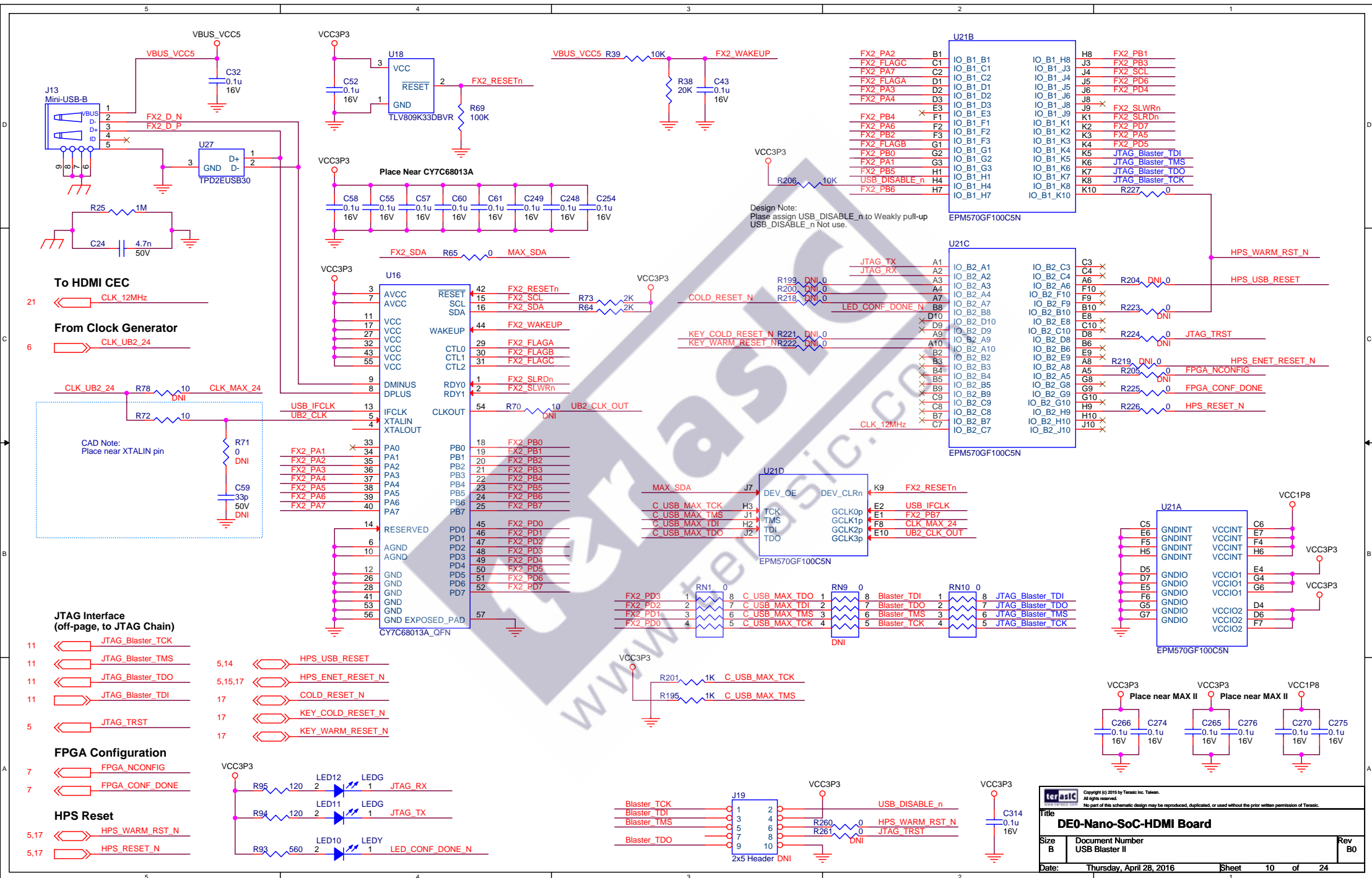


Default Setup MSEL[4:0] = 10010,
AS Fast Mode









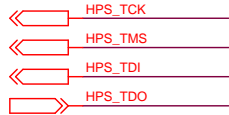
USB Blaster



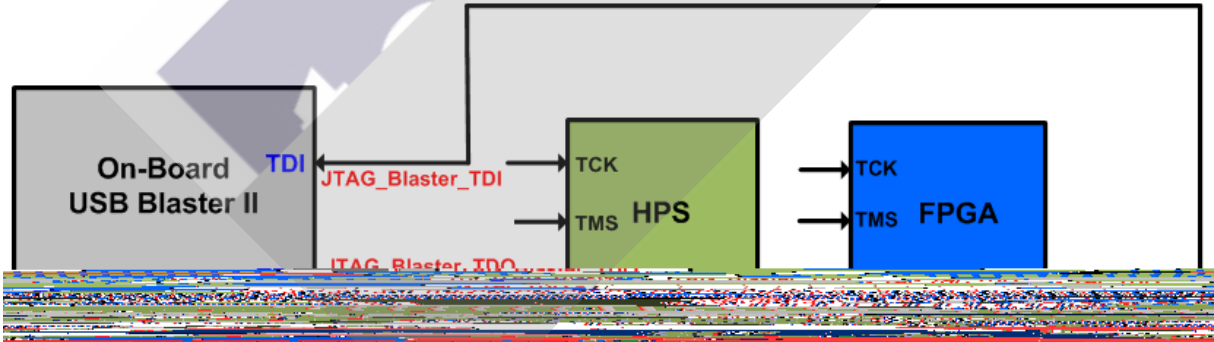
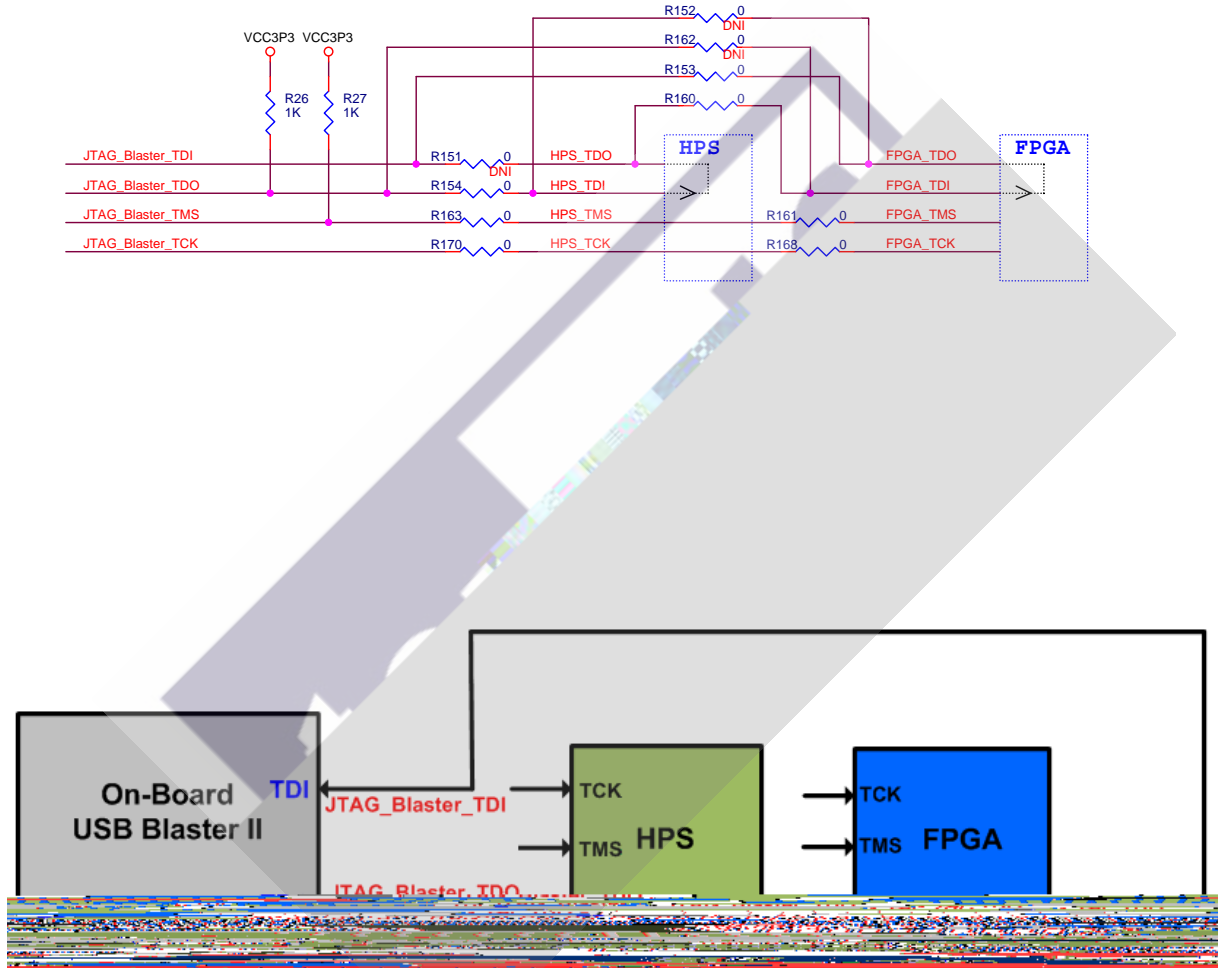
FPGA JTAG INTERFACE



HPS JTAG INTERFACE



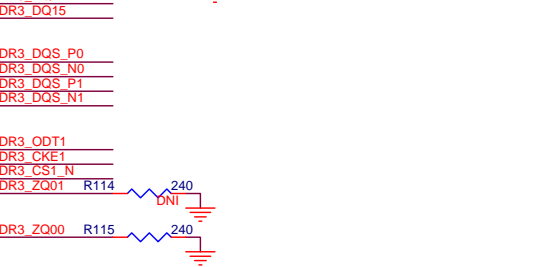
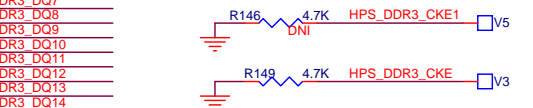
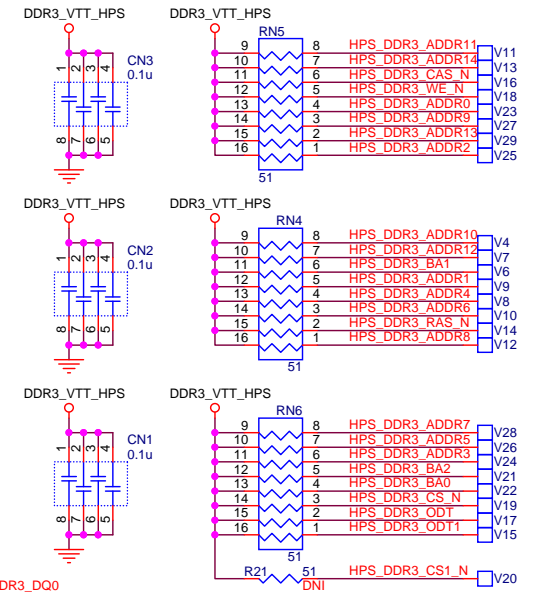
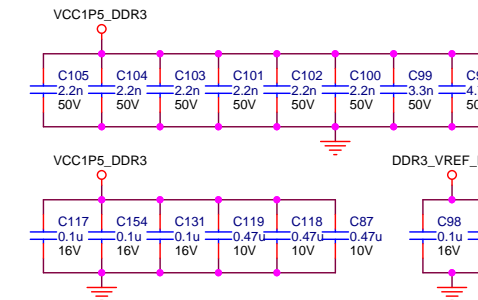
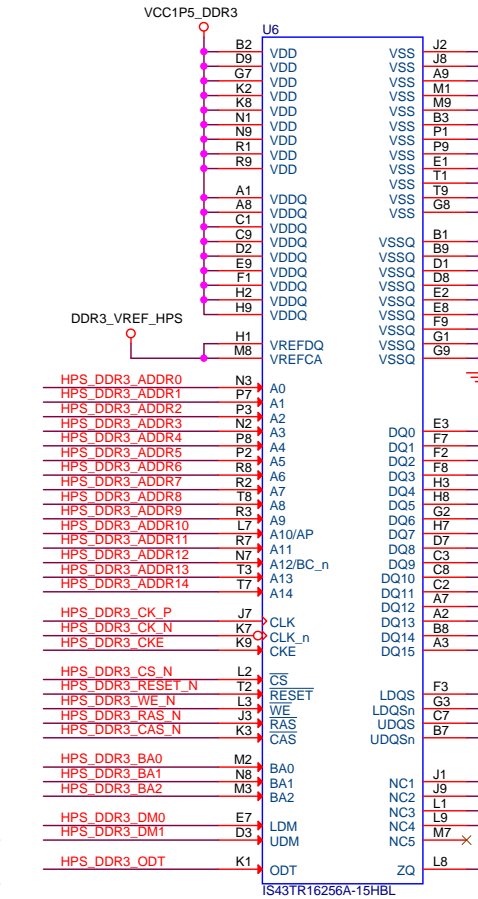
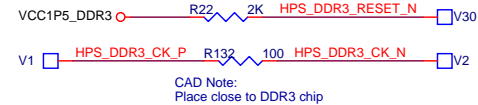
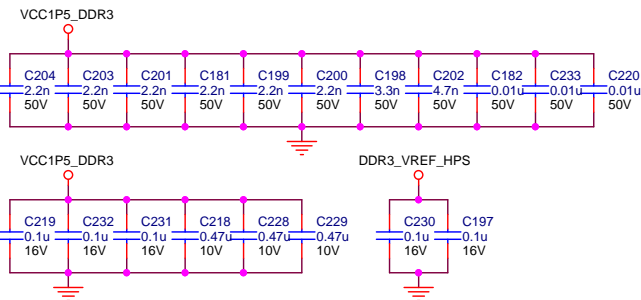
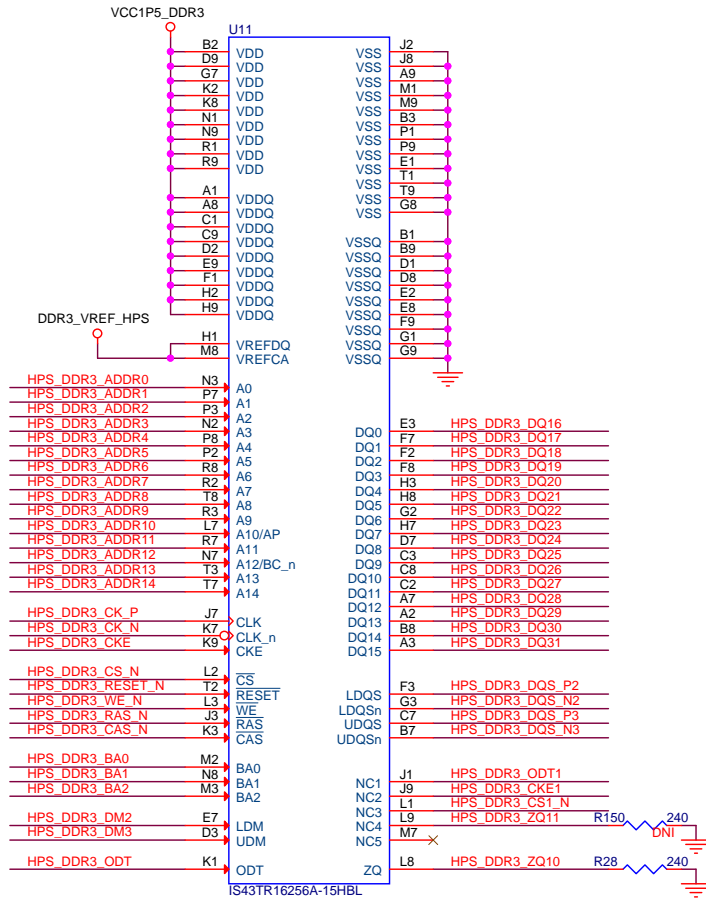
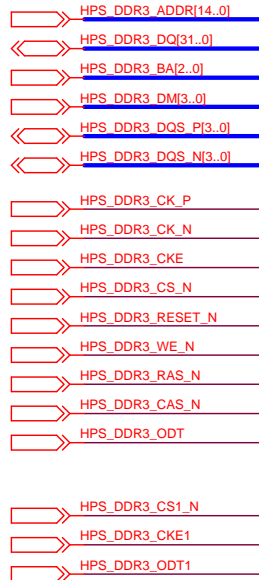
JTAG Chain



DDR3 Interface (HPS)

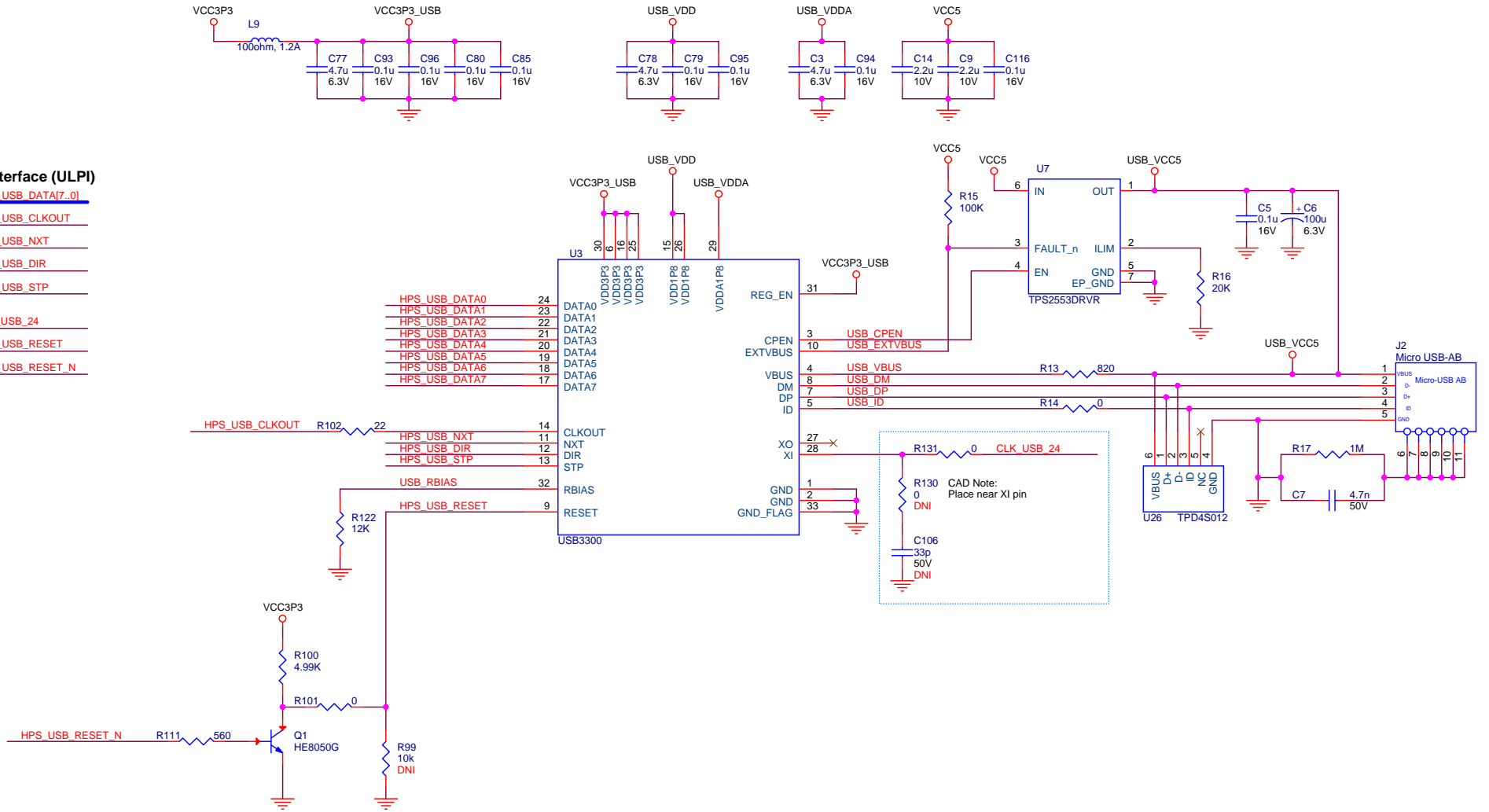
Note :
you can only swap the DQ signals
within x8 group (e.g. 0-7,8-15,16-23,24-31)
on the DDR3 chips

Note : you can swap the signals on the OCT resistor array
(include NC pin)

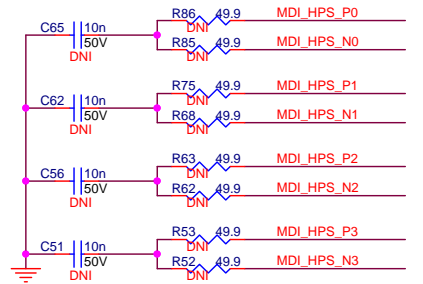
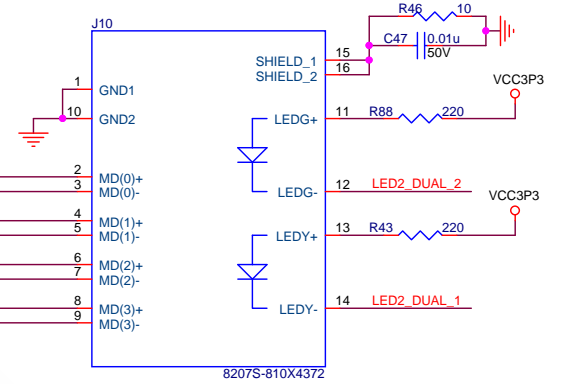
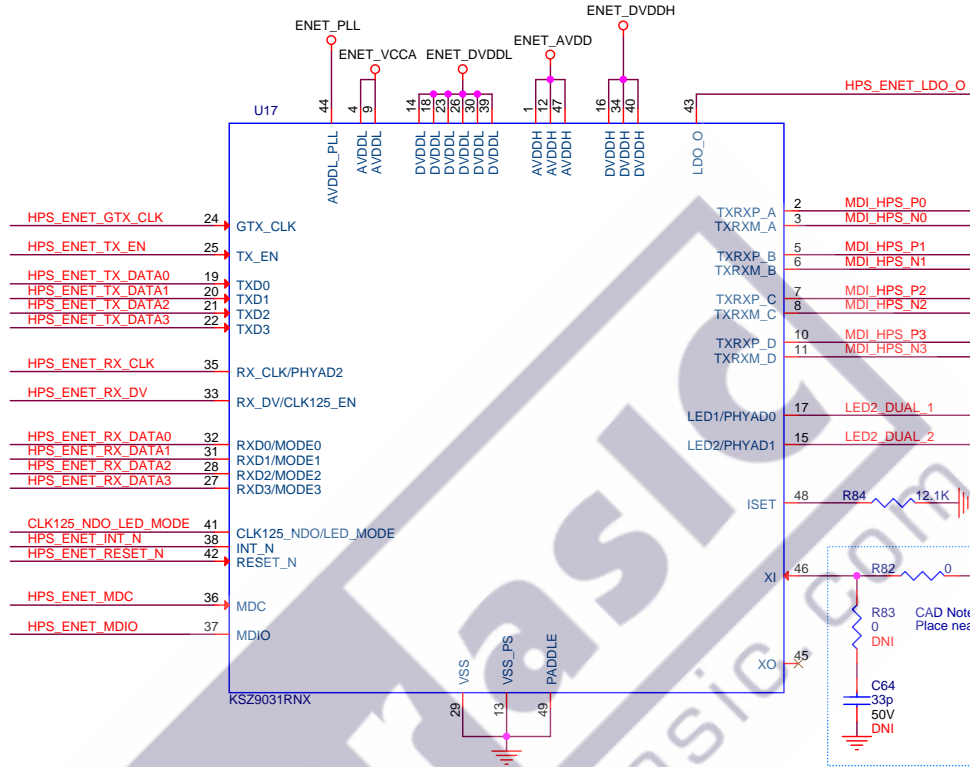
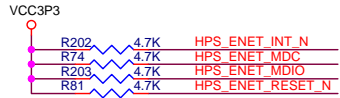
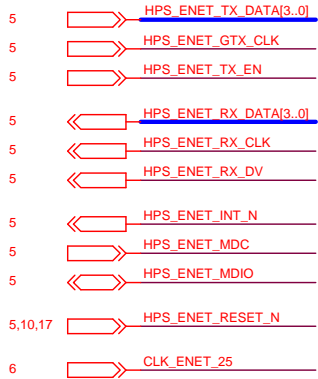


UBS PHY Interface (ULPI)

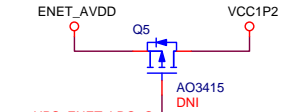
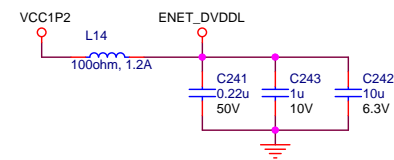
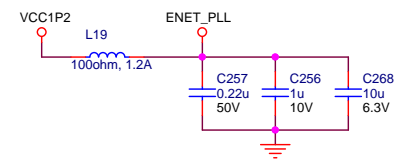
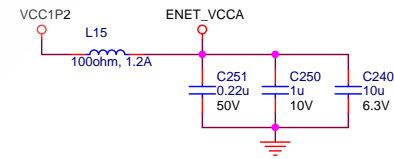
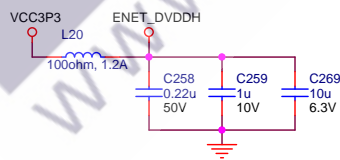
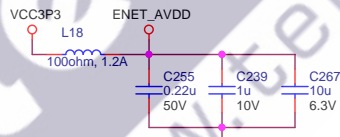
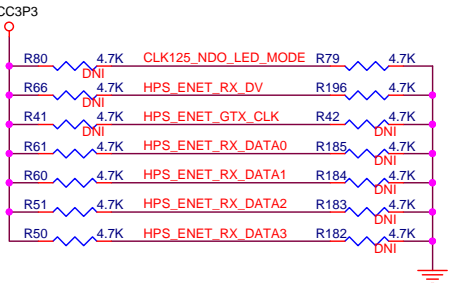
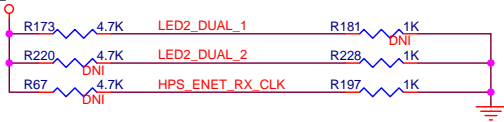
- 5 << HPS_USB_DATA[7..0]
- 5 << HPS_USB_CLKOUT
- 5 << HPS_USB_NXT
- 5 << HPS_USB_DIR
- 5 << HPS_USB_STP
- 6 << CLK_USB_24
- 5,10 << HPS_USB_RESET
- 17 << HPS_USB_RESET_N



Ethernet PHY Interface (RGMII)

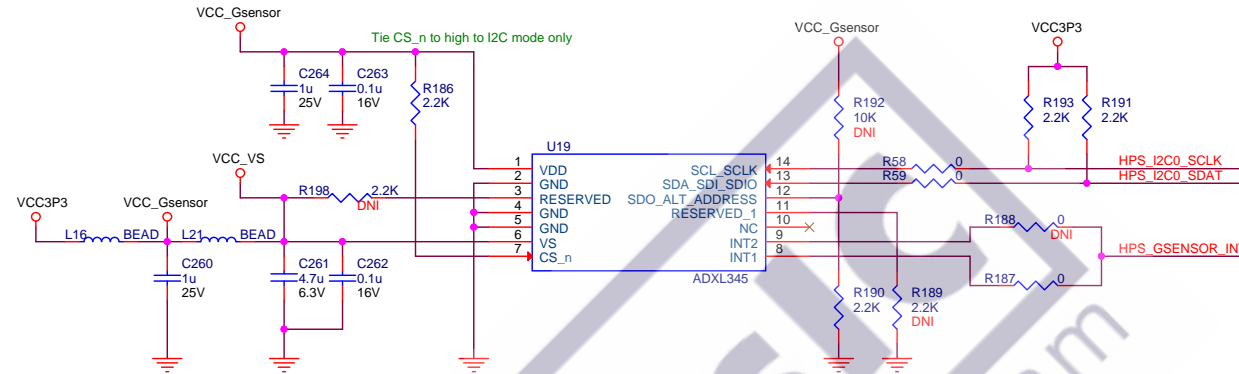


PHY Address is 00001



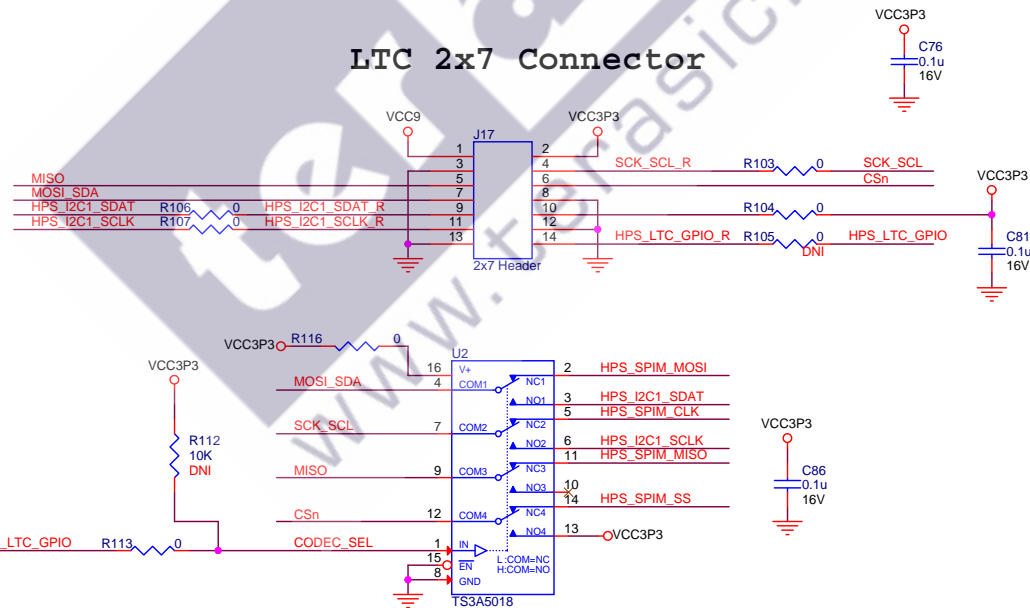
<div> <div>terasic</div> <div>Copyright (c) 2015 by Terasic Inc., Taiwan. All rights reserved. No part of this schematic design may be reproduced, duplicated, or used without the prior written permission of Terasic.</div> </div>			
Title			
DE0-Nano-Soc-HDMI Board			
Size	Document Number	Rev	
B	HPS : GigaBit Ethernet	B0	
Date:	Tuesday, March 22, 2016	Sheet	15 of 24

Accelerometer Interface

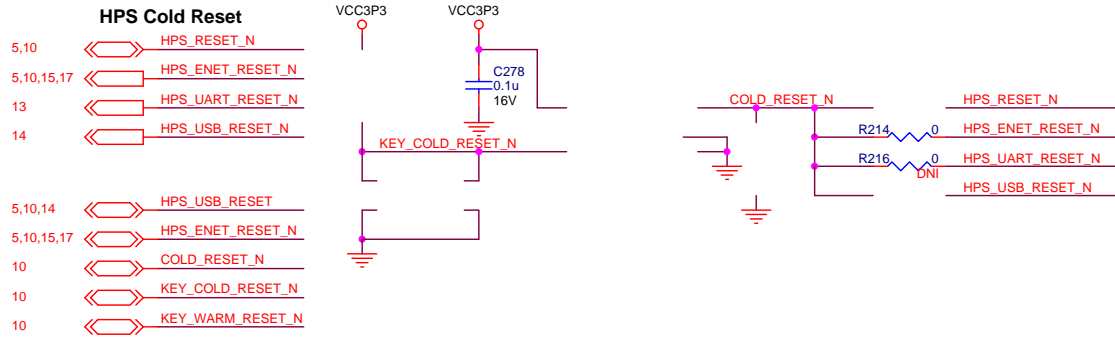


Default : I2C Address 0xA6/0xA7

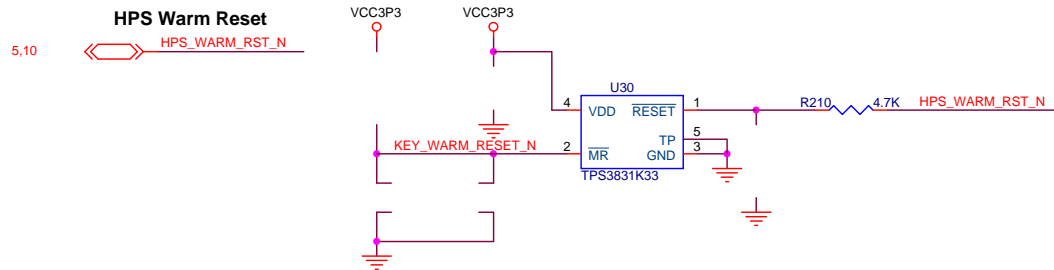
LTC Interface



HPS Cold Reset



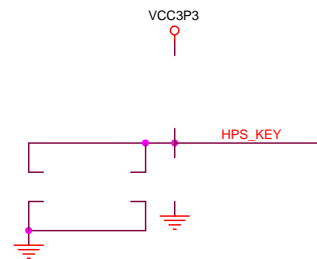
HPS Warm Reset



HPS Key and LED



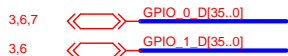
HPS User Button



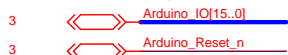
HPS User LED



GPIO



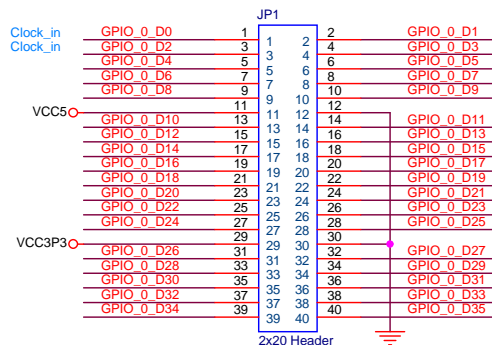
Arduino Digital Interface



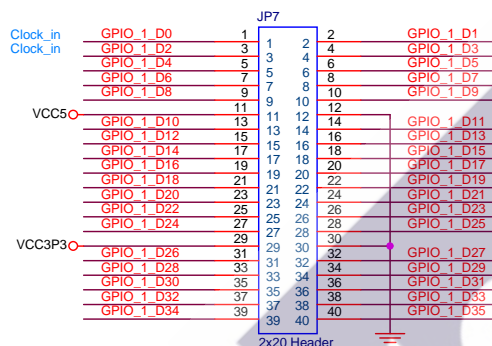
Analog input interface



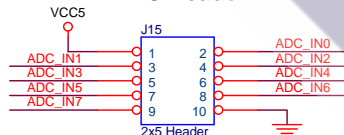
GPIO 0 Header



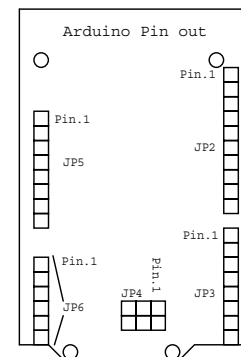
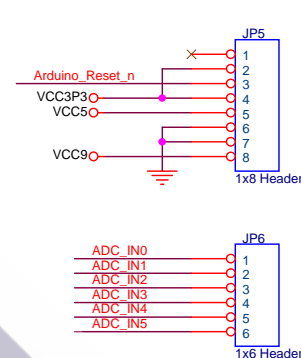
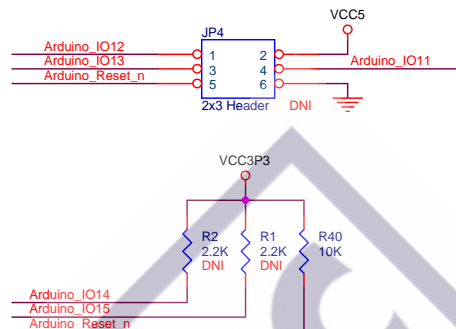
GPIO 1 Header



ADC Header



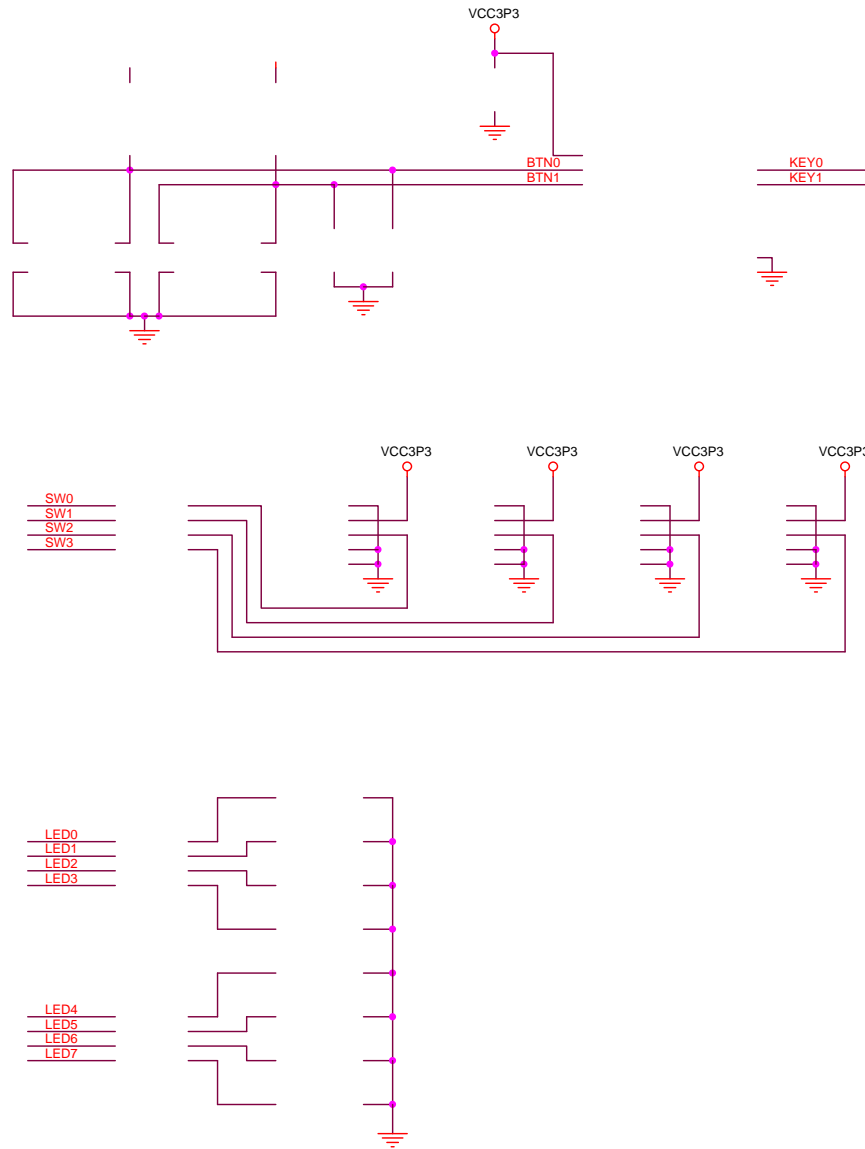
Arduino UNO Rev3

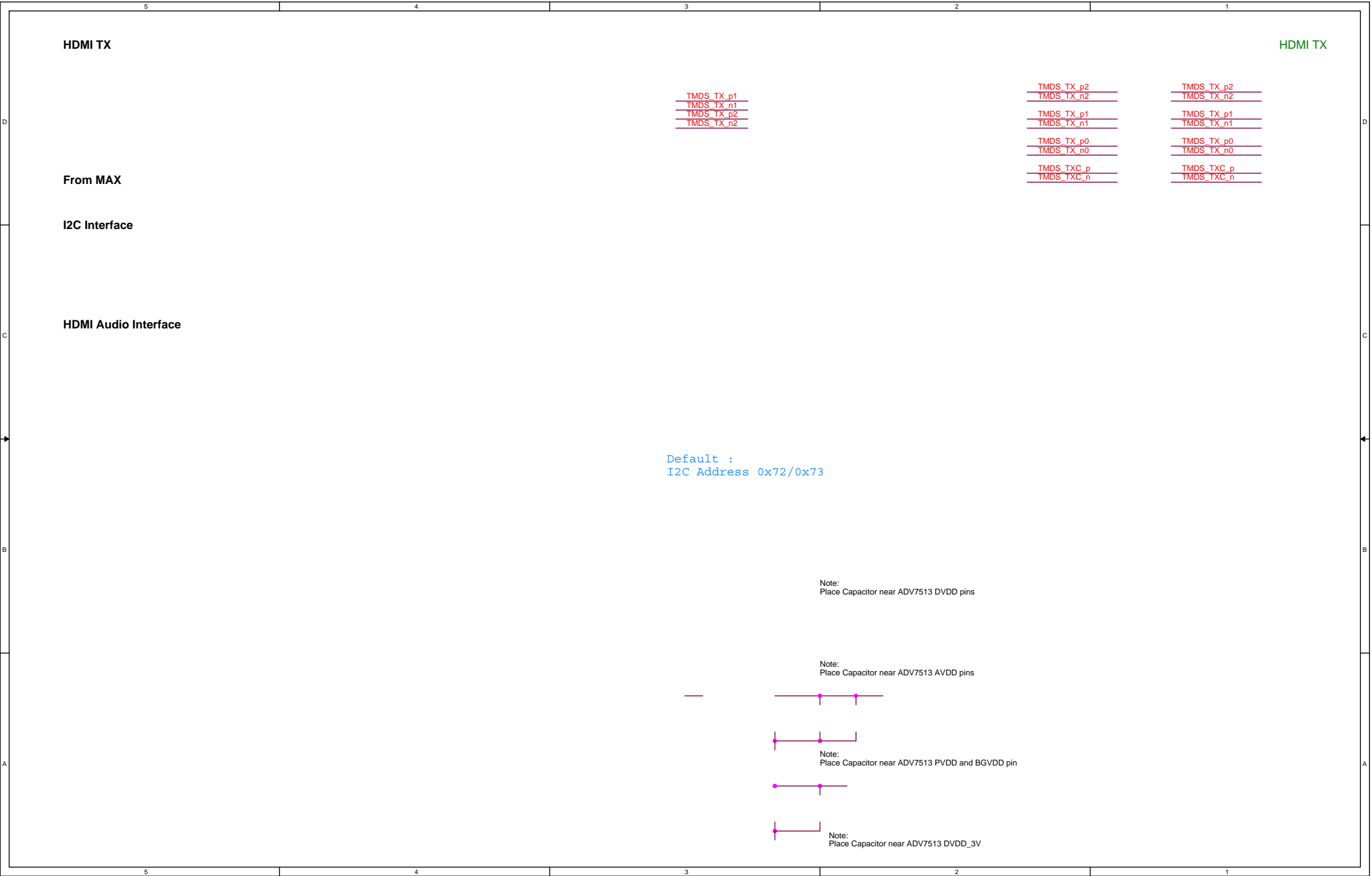


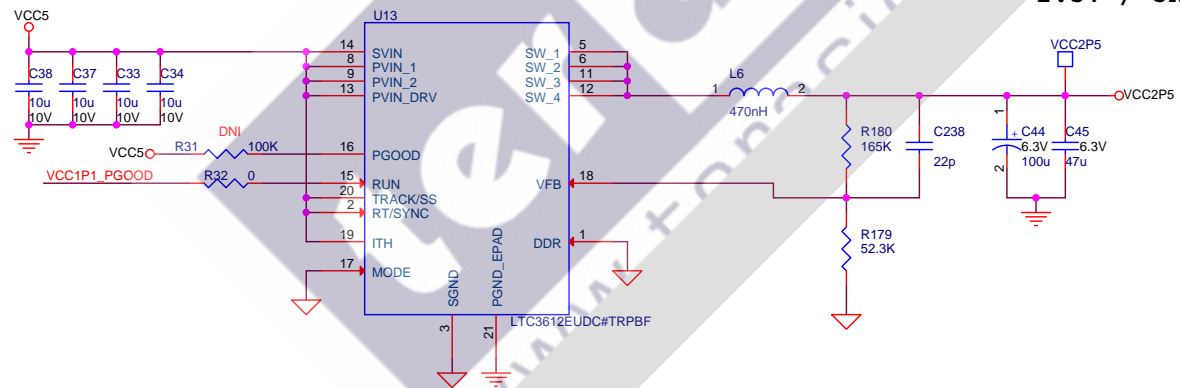
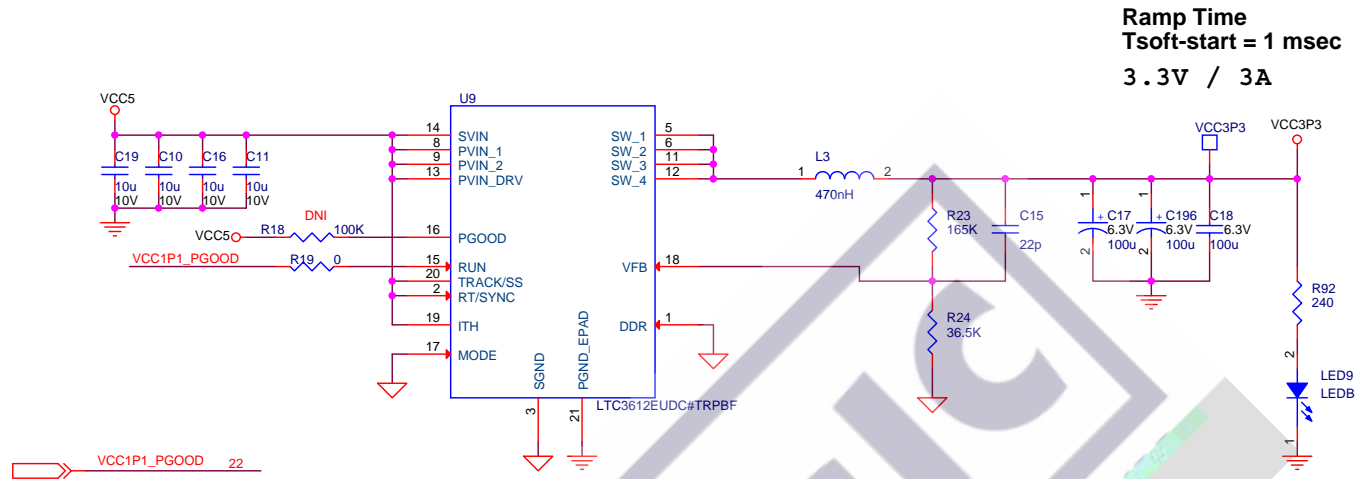
KEY

SWITCH

LED







5 4 3 2 1

