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Jameco Part Number 905643

# OPA277

# OPA4277



OPA277 is a precision, low-noise, rail-to-rail output, single-supply, CMOS operational amplifier. It is designed for use in a wide range of applications, including signal conditioning, instrumentation, and data acquisition. The OPA277 is available in both 8-pin and 14-pin packages, and is designed to operate from a single supply of 1.8V to 5.5V. It features a low input bias current of 10 pA, a low input offset voltage of 1 mV, and a high common-mode rejection ratio (CMRR) of 100 dB. The OPA277 is also designed for high-speed operation, with a slew rate of 10 V/μs and a bandwidth of 1 MHz. It is a true rail-to-rail output device, capable of driving loads of up to 10 kΩ to both the positive and negative supply rails. The OPA277 is a member of the OPAx277 family, which also includes the OPA4277, a quad version of the OPA277.

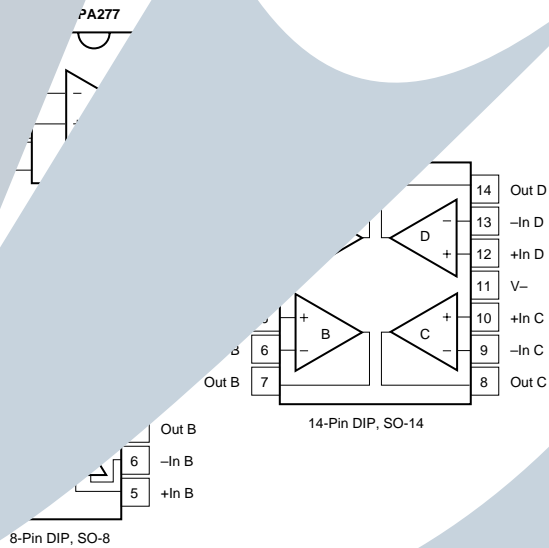
Amplifier

## PARAMETERS

### OPERATIONAL AMPLIFIER

### POWERED INSTRUMENTS

### COMPONENTS



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## ABSOLUTE MAXIMUM RATINGS<sup>(1)</sup>

Supply Voltage .....	36V
Input Voltage .....	(V-) -0.7V to (V+) +0.7V
Output Short-Circuit <sup>(2)</sup> .....	Continuous
Operating Temperature .....	-55°C to +125°C
Storage Temperature .....	-55°C to +125°C
Junction Temperature .....	150°C
Lead Temperature (soldering, 10s) .....	300°C
ESD Rating (Human Body Model) .....	2000V
(Machine Model) .....	100V

NOTE: (1) Stresses above these rating may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Short-circuit to ground, one amplifier per package.



## ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

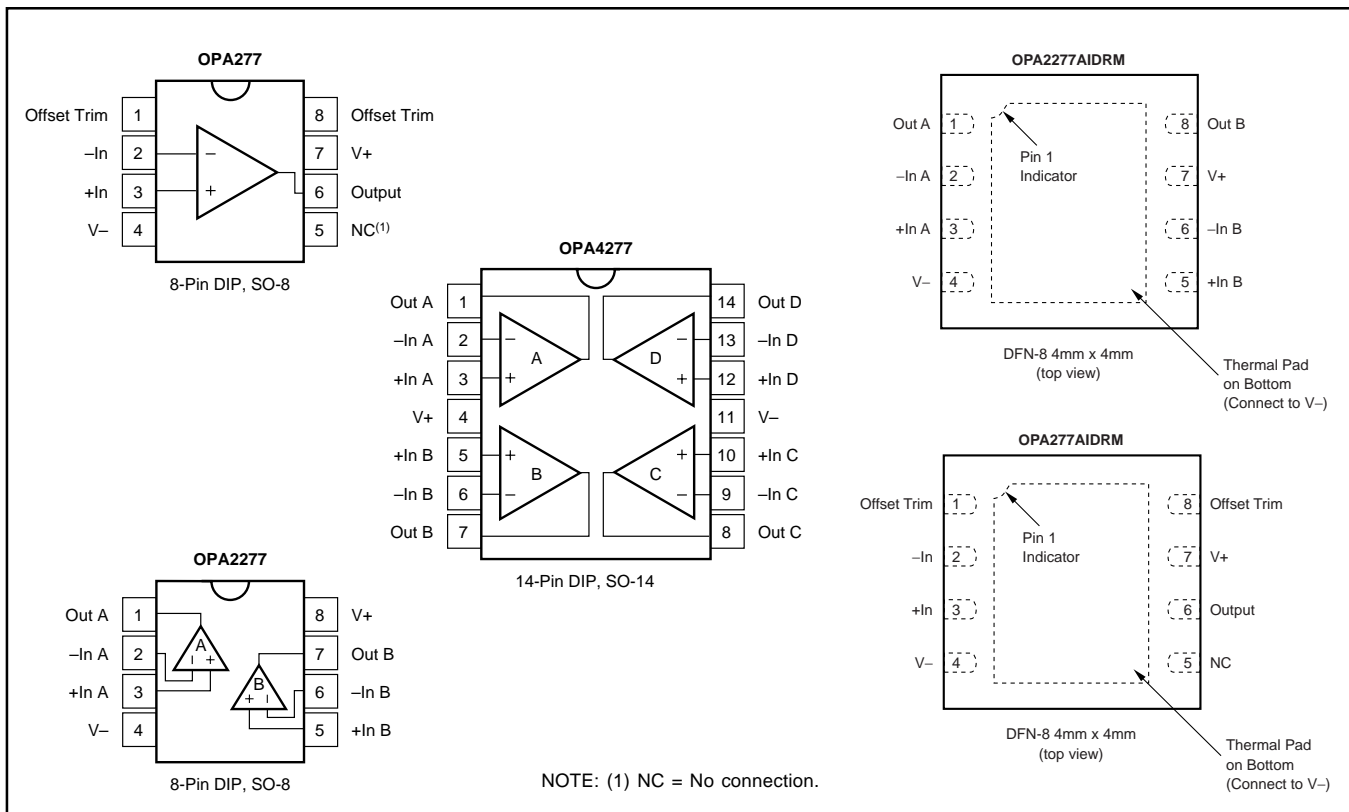
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## PACKAGE/ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	OFFSET VOLTAGE max, $\mu\text{V}$	OFFSET VOLTAGE DRIFT max, $\mu\text{V}/^\circ\text{C}$	PACKAGE-LEAD
<b>Single</b> OPA277PA OPA277P OPA277UA OPA277U OPA277AIDRM	$\pm 50$ $\pm 20$ $\pm 50$ $\pm 20$ $\pm 100$	$\pm 1$ $\pm 0.15$ $\pm 1$ $\pm 0.15$ $\pm 1$	DIP-8 DIP-8 SO-8 Surface Mount SO-8 Surface Mount DFN-8 (4mm x 4mm)
<b>Dual</b> OPA2277PA OPA2277P OPA2277UA OPA2277U OPA2277AIDRM	$\pm 50$ $\pm 25$ $\pm 50$ $\pm 25$ $\pm 100$	$\pm 1$ $\pm 0.25$ $\pm 1$ $\pm 0.25$ $\pm 1$	DIP-8 DIP-8 SO-8 Surface Mount SO-8 Surface Mount DFN-8 (4mm x 4mm)
<b>Quad</b> OPA4277PA OPA4277UA	$\pm 50$ $\pm 50$	$\pm 1$ $\pm 1$	DIP-14 SO-14 Surface Mount

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet or visit the TI web site at [www.ti.com](http://www.ti.com).

## PIN DESCRIPTIONS



## ELECTRICAL CHARACTERISTICS: $V_S =$

# ELECTRICAL CHARACTERISTICS: $V_S = \pm 5V$ to $V_S = \pm 15V$ (CONT)

At  $T_A = +25^\circ\text{C}$ , and  $R_L = 2k\Omega$ , unless otherwise noted.

**Boldface** limits apply over the specified temperature range,  $-40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

PARAMETER	CONDITION	OPA277P, U OPA2277P, U			OPA277PA, UA OPA2277PA, UA OPA4277PA, UA			OPA277AIDRM, OPA2277AIDRM			UNITS
		MIN	TYP <sup>(1)</sup>	MAX	MIN	TYP <sup>(1)</sup>	MAX	MIN	TYP <sup>(1)</sup>	MAX	
<b>OUTPUT</b>											
Voltage Output $V_O$	$R_L = 10k\Omega$	(V-) +0.5		(V+) -1.2	*		*	*		*	V
$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	$R_L = 10k\Omega$	<b>(V-) +0.5</b>		<b>(V+) -1.2</b>	*		*	*		*	V
	$R_L = 2k\Omega$	(V-) +1.5		(V+) -1.5	*		*	*		*	V
$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	$R_L = 2k\Omega$	<b>(V-) +1.5</b>		<b>(V+) -1.5</b>	*		*	*		*	V
Short-Circuit Current $I_{SC}$			$\pm 35$			*			*		mA
Capacitive Load Drive $C_{LOAD}$		See Typical Curve				*			*		
<b>POWER SUPPLY</b>											
Specified Voltage Range $V_S$		$\pm 5$		$\pm 15$	*		*	*		*	V
Operating Voltage Range		$\pm 2$		$\pm 18$	*		*	*		*	V
Quiescent Current (per amplifier) $I_Q$	$I_O = 0$		$\pm 790$	$\pm 825$		*	*		*	*	$\mu\text{A}$
$T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$	$I_O = 0$			<b><math>\pm 900</math></b>			*			*	$\mu\text{A}$
<b>TEMPERATURE RANGE</b>											
Specified Range		-40		+85	*		*	*		*	$^\circ\text{C}$
Operating Range		-55		+125	*		*	*		*	$^\circ\text{C}$
Storage Range		-55		+125	*		*	*		*	$^\circ\text{C}$
Thermal Resistance $\theta_{JA}$											
SO-8 Surface-Mount			150			*					$^\circ\text{C/W}$
DIP-8			100			*					$^\circ\text{C/W}$
DIP-14			80			*					$^\circ\text{C/W}$
SO-14 Surface-Mount			100			*					$^\circ\text{C/W}$
DFN-8 <sup>(2)</sup>								45			$^\circ\text{C/W}$

\* Specifications same as OPA277P, U.

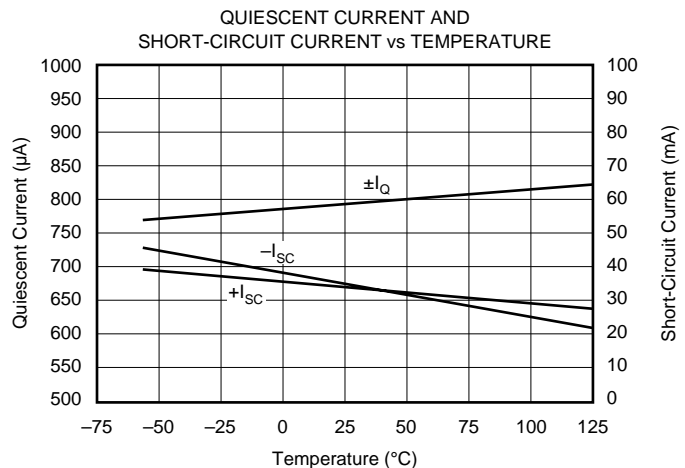
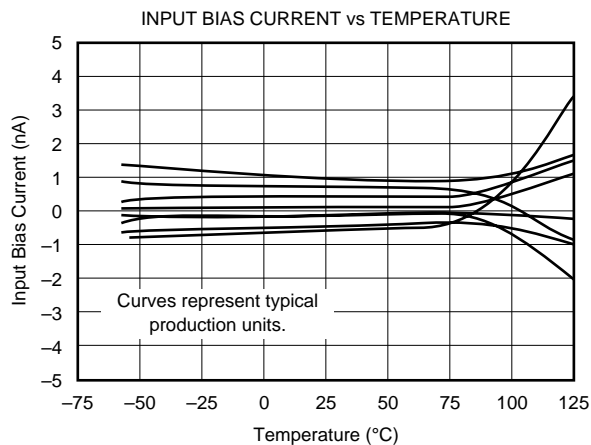
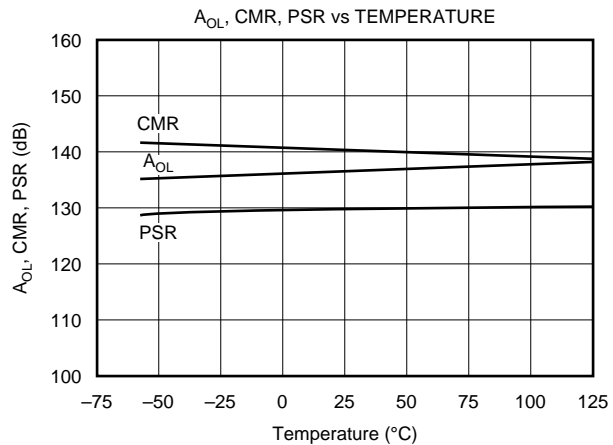
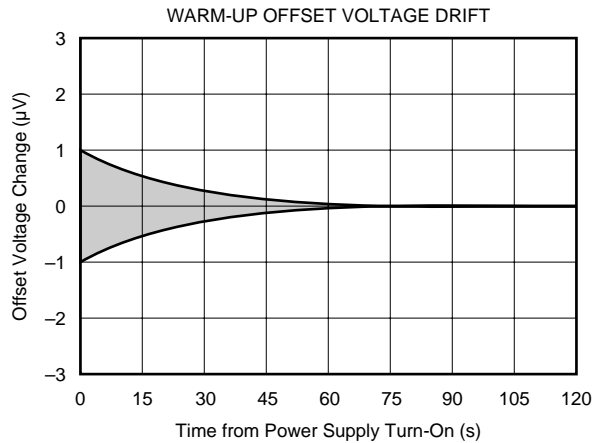
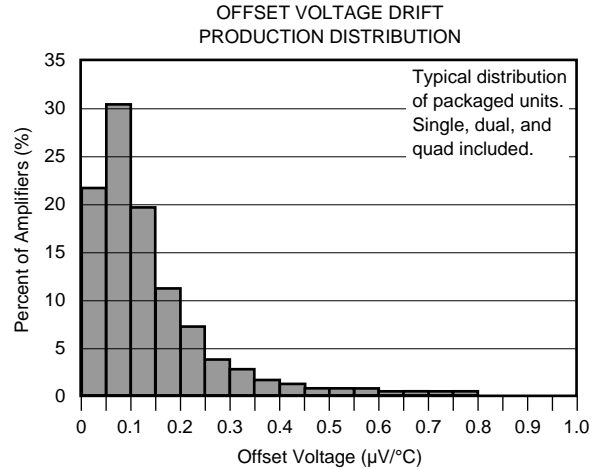
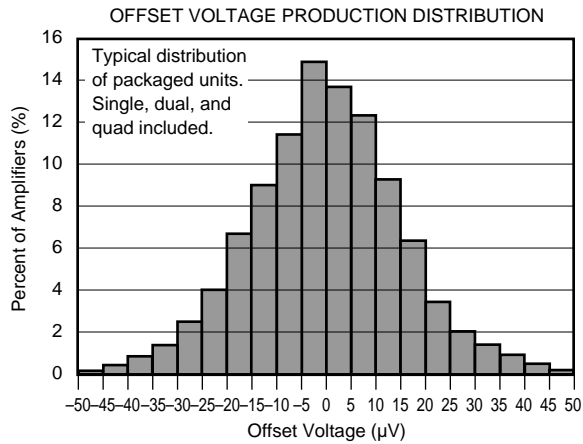
NOTES: (1)  $V_S = \pm 15V$ .

(2) Thermal pad soldered to printed circuit board (PCB).



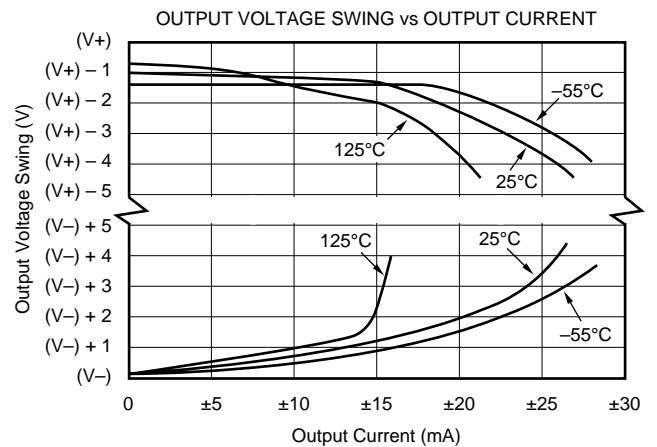
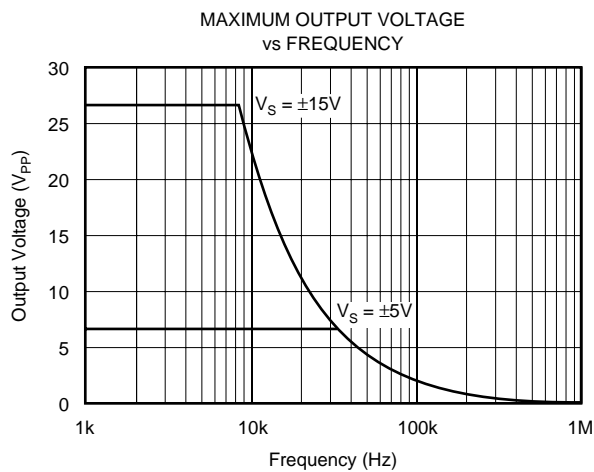
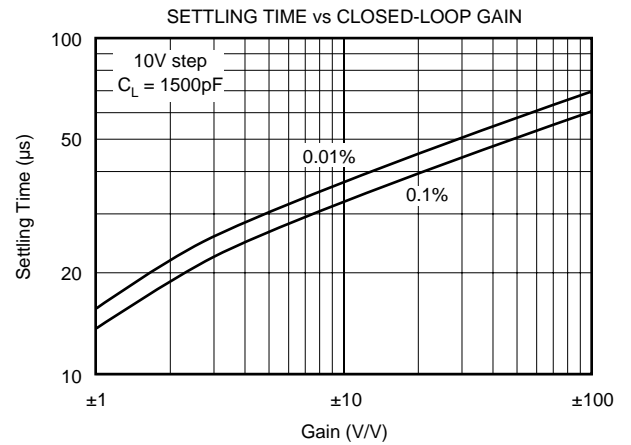
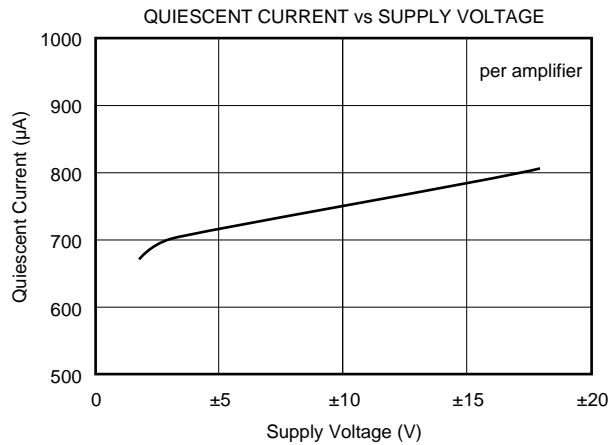
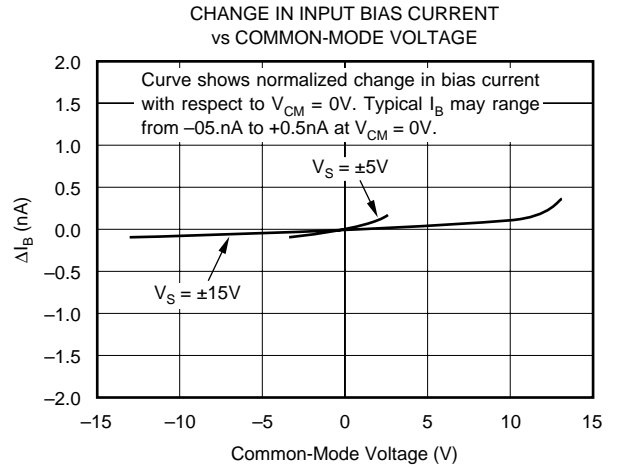
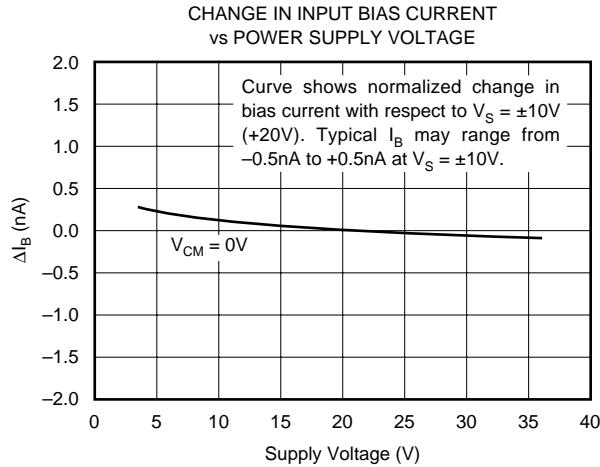
# TYPICAL CHARACTERISTICS (CONT)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , and  $R_L = 2\text{k}\Omega$ , unless otherwise noted.



# TYPICAL CHARACTERISTICS (CONT)

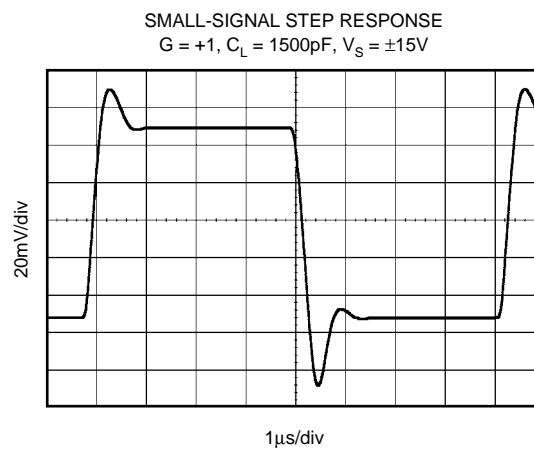
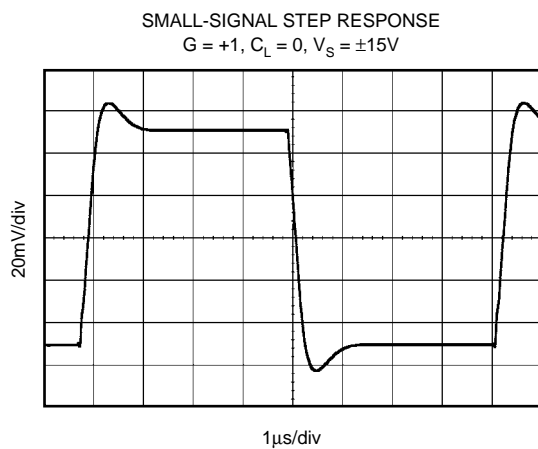
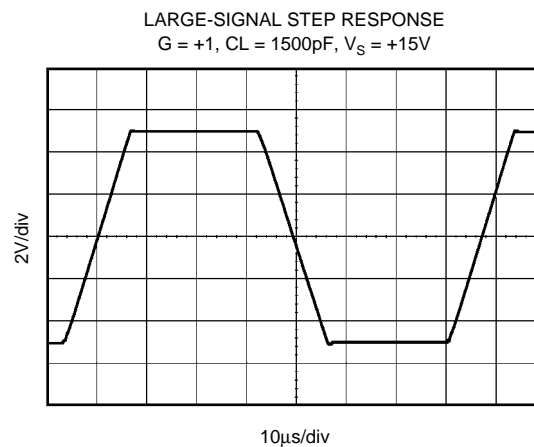
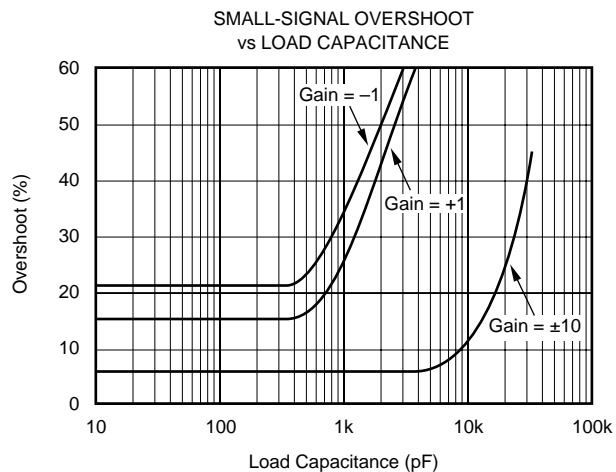
At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , and  $R_L = 2\text{k}\Omega$ , unless otherwise noted.





# TYPICAL CHARACTERISTICS (CONT)

At  $T_A = +25^\circ\text{C}$ ,  $V_S = \pm 15\text{V}$ , and  $R_L = 2\text{k}\Omega$ , unless otherwise noted.



# APPLICATIONS INFORMATION

The OPA277 series is unity-gain stable and free from unexpected output phase reversal, making it easy to use in a wide range of applications. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins. In most cases 0.1µF capacitors are adequate.

The OPA277 series has very low offset voltage and drift. To achieve highest performance, circuit layout and mechanical conditions should be optimized. Offset voltage and drift can be degraded by small thermoelectric potentials at the op amp inputs. Connections of dissimilar metals will generate thermal potential which can degrade the ultimate performance of the OPA277 series. These thermal potentials can be made to cancel by assuring that they are equal in both input terminals.

- Keep thermal mass of the connections made to the two input terminals similar.
- Locate heat sources as far as possible from the critical input circuitry.
- Shield op amp and input circuitry from air currents such as cooling fans.

## OPERATING VOLTAGE

OPA277 series op amp operate from ±2V to ±18V supplies with excellent performance. Unlike most op amps which are specified at only one supply voltage, the OPA277 series is specified for real-world applications; a single limit applies over the ±5V to ±15V supply range. This allows a customer operating at  $V_S = \pm 10V$  to have the same assured performance as a customer using ±15V supplies. In addition, key parameters are assured over the specified temperature range, -40°C to +85°C. Most behavior remains unchanged through the full operating voltage range (±2V to ±18V). Parameters which vary significantly with operating voltage or temperature are shown in typical performance curves.

## OFFSET VOLTAGE ADJUSTMENT

The OPA277 series is laser-trimmed for very low offset voltage and drift so most circuits will not require external adjustment. However, offset voltage trim connections are provided on pins 1 and 8. Offset voltage can be adjusted by

connecting a potentiometer as shown in Figure 1. This adjustment should be used only to null the offset of the op amp. This adjustment should not be used to compensate for offsets created elsewhere in a system since this can introduce additional temperature drift.

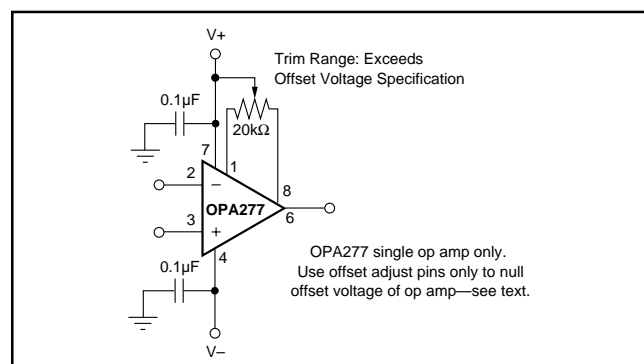


FIGURE 1. OPA277 Offset Voltage Trim Circuit.

## INPUT PROTECTION

The inputs of the OPA277 series are protected with 1kΩ series input resistors and diode clamps. The inputs can withstand ±30V differential inputs without damage. The protection diodes will, of course, conduct current when the inputs are over-driven. This may disturb the slewing behavior of unity-gain follower applications, but will not damage the op amp.

## INPUT BIAS CURRENT CANCELLATION

The input stage base current of the OPA277 series is internally compensated with an equal and opposite cancellation circuit. The resulting input bias current is the difference between the input stage base current and the cancellation current. This residual input bias current can be positive or negative.

When the bias current is canceled in this manner, the input bias current and input offset current are approximately the same magnitude. As a result, it is not necessary to use a bias current cancellation resistor as is often done with other op amps (Figure 2). A resistor added to cancel input bias current errors may actually increase offset voltage and noise.

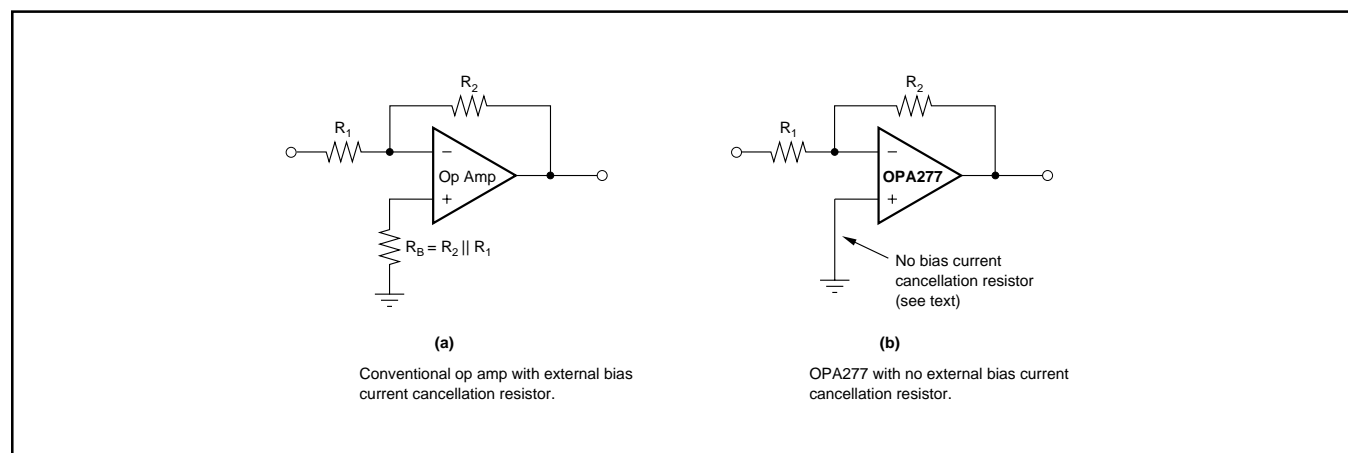


FIGURE 2. Input Bias Current Cancellation.



## DFN PACKAGE

The OPA277 series uses the 8-lead DFN (also known as SON), which is a QFN package with contacts on only two sides of the package bottom. This leadless, near-chip-scale package maximizes board space and enhances thermal and electrical characteristics through an exposed pad.

DFN packages are physically small, have a smaller routing area, improved thermal performance, and improved electrical parasitics, with a pinout scheme that is consistent with other commonly-used packages, such as SO and MSOP. Additionally, the absence of external leads eliminates bent-lead issues.

The DFN package can be easily mounted using standard printed circuit board (PCB) assembly techniques. See Application Note, *QFN/SON PCB Attachment* (SLUA271) and Application Report, *Quad Flatpack No-Lead Logic Packages* (SCBA017), both available for download at [www.ti.com](http://www.ti.com).

**The exposed leadframe die pad on the bottom of the package should be connected to V–.**

## LAYOUT GUIDELINES

The leadframe die pad should be soldered to a thermal pad on the PCB. Mechanical drawings located at the end of this data sheet list the physical dimensions for the package and pad.

Soldering the exposed pad significantly improves board-level reliability during temperature cycling, key push, package shear, and similar board-level tests. Even with applications that have low-power dissipation, the exposed pad **must** be soldered to the PCB to provide structural integrity and long-term reliability.

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
OPA2277AIDRMR	ACTIVE	SON	DRM	8	3000	TBD	Call TI	Call TI
OPA2277AIDRMT	ACTIVE	SON	DRM	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA2277AIDRMTG4	ACTIVE	SON	DRM	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA2277P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA2277PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA2277PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA2277PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA2277U	ACTIVE	SOIC	D	8	100	TBD	CU NIPDAU	Level-3-220C-168 HR
OPA2277U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2277U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2277UA	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2277UA/2K5	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA2277UA/2K5E4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2277UAE4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2277UAG4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA2277UG4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA277AIDRMR	ACTIVE	SON	DRM	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA277AIDRMRG4	ACTIVE	SON	DRM	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA277AIDRMT	ACTIVE	SON	DRM	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA277AIDRMTG4	ACTIVE	SON	DRM	8	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
OPA277P	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA277PA	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA277PAG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA277PG4	ACTIVE	PDIP	P	8	50	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA277U	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA277U/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
no Sb/Br)								
OPA277U/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA277UA	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA277UA/2K5	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA277UA/2K5E4	ACTIVE	SOIC	D	8	2500	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA277UAE4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA277UG4	ACTIVE	SOIC	D	8	100	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA4277PA	ACTIVE	PDIP	N	14	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type
OPA4277UA	ACTIVE	SOIC	D	14	58	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA4277UA/2K5	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA4277UA/2K5E4	ACTIVE	SOIC	D	14	2500	Pb-Free (RoHS)	CU NIPDAU	Level-3-260C-168 HR
OPA4277UAE4	ACTIVE	SOIC	D	14	58	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR
OPA4277UAG4	ACTIVE	SOIC	D	14	58	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

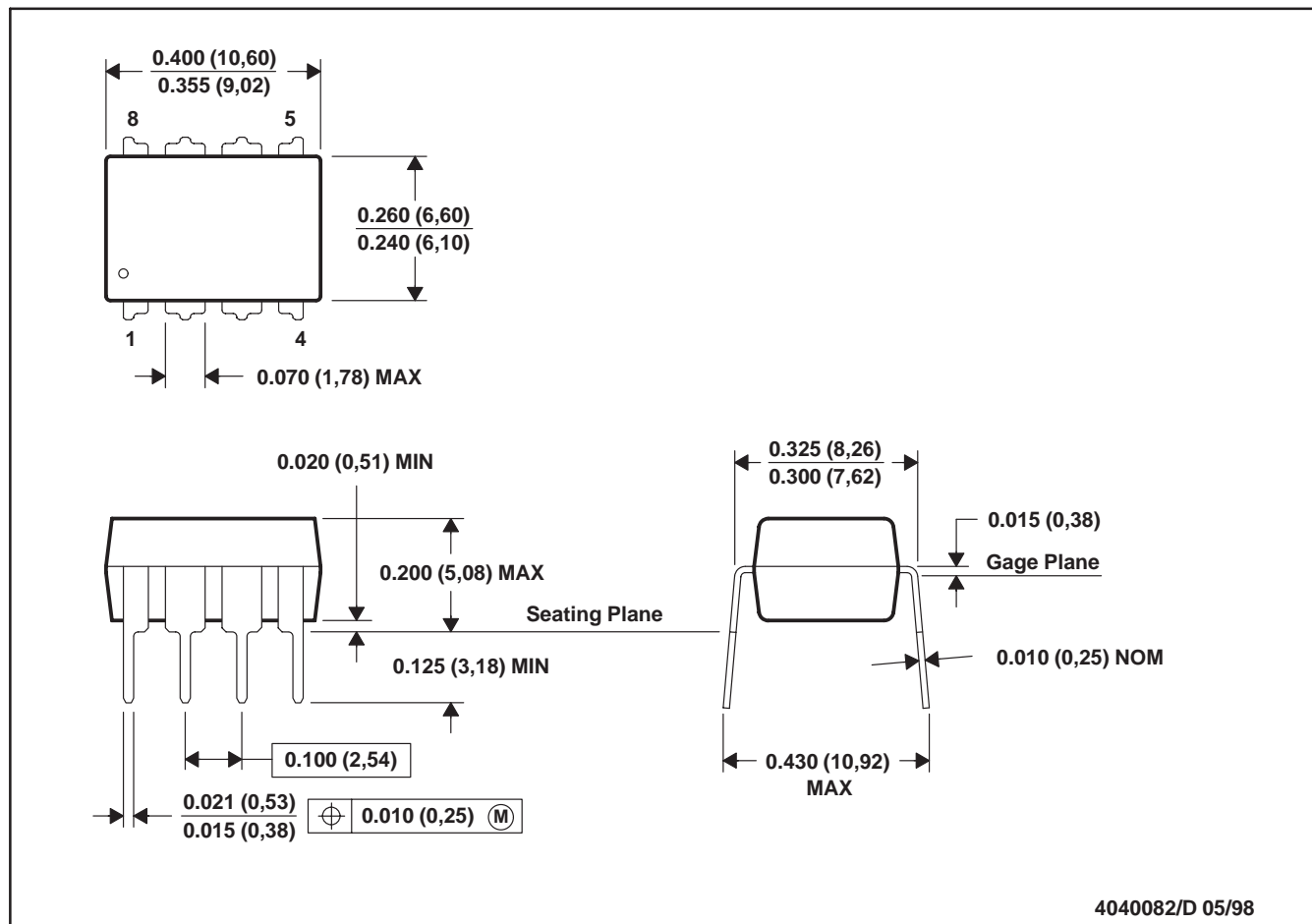
<sup>(3)</sup> MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

## P (R-PDIP-T8)

## PLASTIC DUAL-IN-LINE



NOTES: A. All linear dimensions are in inches (millimeters).  
 B. This drawing is subject to change without notice.  
 C. Falls within JEDEC MS-001

For the latest package information, go to [http://www.ti.com/sc/docs/package/pkg\\_info.htm](http://www.ti.com/sc/docs/package/pkg_info.htm)



## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only  
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - The 20 pin end lead shoulder width is a vendor option, either half or full width.



-G1



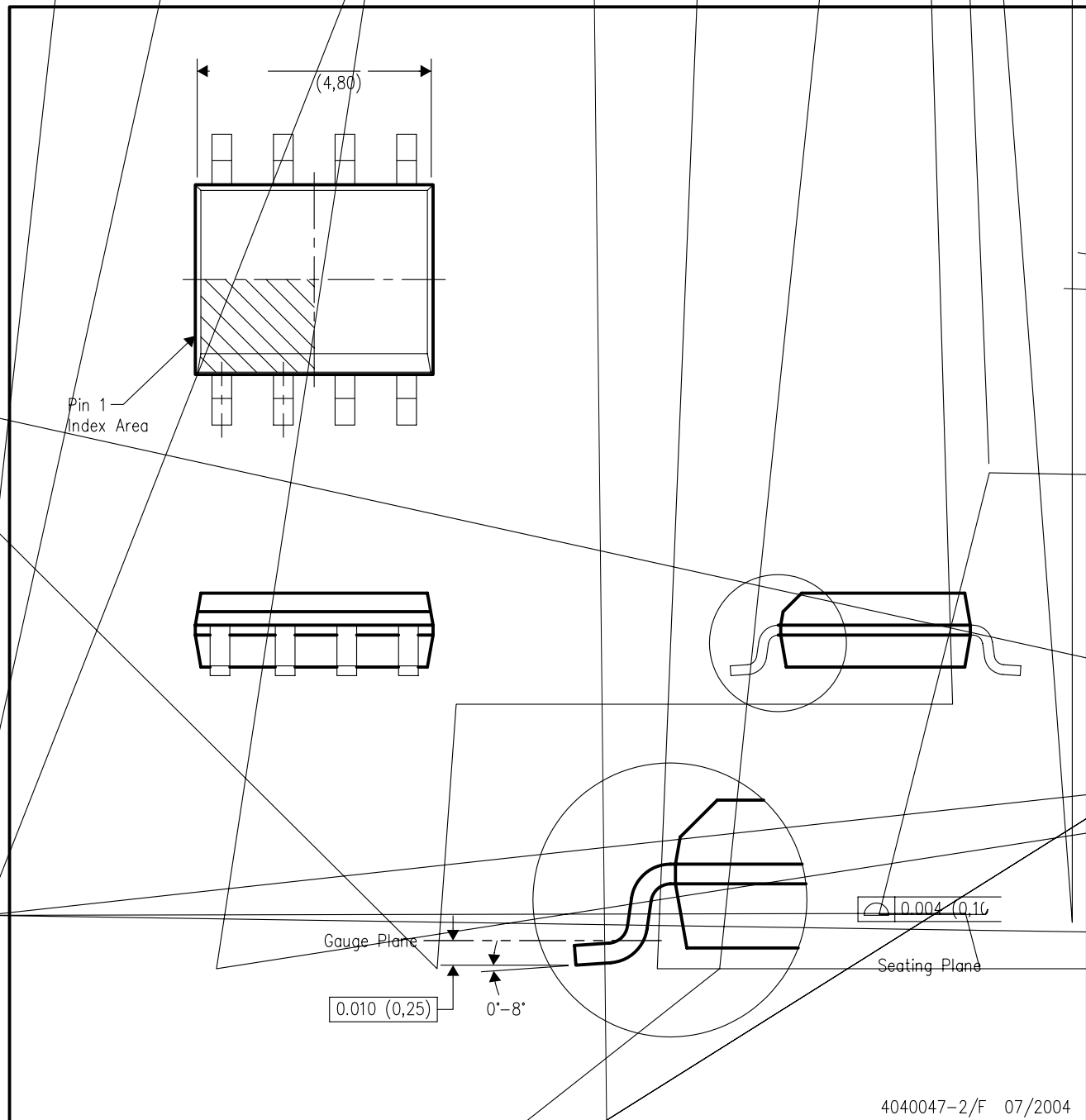
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intrusion not to exceed 0.006 (0,15).

# MECHANICAL DATA

D (R-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-012 variation AA.

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