Computer Organization 104-2

Lab 1: The Arithmetic Logic Unit

Due: 2016/04/04 23:59:59

1. Goal

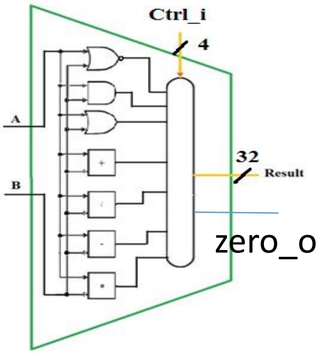
- In this assignment is for you to grasp and comprehend the functionality of the ALU and how to drive it with the control signals.

2. Requirement

- Implement a 32-Bits ALU which computes the arithmetic and the logic operations.
- The ALU Control Input is the signal that tells the ALU what operation needs to be executed.
- The output from the ALU must contain the 32 bits result and one more bit for the Zero flag.
- You will be provided with a testbench file and an empty ALU module. Your work is to create your own ALU and run it with the given testbench. Do not modify the testbench.
- You should use Behavioral Level or RTL Description. DO NOT USE gate level for this assignment.
- The assignment packet contains the input files that the Testbench will use to test your design. To understand better what cases are being test you may refer to the "test case.txt" file.
- This is a No-teams-assignment.
- Upload the assignment to E3 with the format as "**student ID_LAB1.rar**"
- The assignment contains your design (ALU.v) and report (student ID_LAB1_report.pdf).

3. The Arithmetic Logic Unit

- Ctrl_i has 4 bits
- The Result output has 32 bits
- Each input has 32 bits



4. Details

- Use the instruction set taught in the lectures
- to bring about the ALU control signal. The instruction set must include all the instructions on the tables below.

ALU action	Name	ALU control input
AND	And	0000
OR	Or	0001
ADD	Addition	0010
SUB	Subtract	0110
NOR	Nor	1100
NAND	Nand	1101
SLT	Set less than	0111
SGT	Set great than	1000
SLE	Set less equal	1001
SGE	Set great equal	1010
SEQ	Set equal	1011
SNE	Set non equal	1110
MULT	Multiplication	0011
SEQZ	Set equal zero	0100

5. Grading Policy

- Total source: 110pts
  - Design: 100 pts Report: 10 pts.

  ※ **Any Plagiarism will be punished with a null score!**
- **Delay: 10%off/day**