PreLab 3 by Ethan Zhou (yz69)

Question 1.

Localparam is locally scoped, constant declaration, similar to "Constant" declaration with in a function for software.

Parameter is globally scoped, rather than declaring an actual value, the declaration is for a default value which can then be changed when instantiating the module, think of it is similar to a optional input variable to a software function with a locally defined default value.

We use localparam when we need a constant value for internal use, and is not expected change over multiple instantiations.

We use parameter when we need a configuration setting for module use, and is expected to change in different scenarios. This is especially useful when we are trying to package our design into IP/Block diagram, we then can access and change parameter using IP configurator by Vivado or other tools.

Question 2.

Wire is continuous connection, used to connect different elements in the circuit and is usually used with combinational logic.

Register is clocked data storage, it can hold value until assigned by a procedural block, it is usually used with sequential logic.

Syntex rules:

Wire is used for combinational signals, cannot be used in procedural blocks, and is driven by assign or module output, cannot hold value

Register is used for sequential signals, can be assigned inside procedural blocks, can be initialized and can hold value, but cannot be used in continuous assignment.

Question 3.

Register can be used to store current state and used to store data that is used for output for each state, especially for data that needs to persists over multiple clock cycle.

Wire can be user for logic elements with in a signal state/clock cycle and other combinational outputs.

Question 4.

Blocking assignment (=) is executed sequentially (the order in which it is written matters) and is generally used in combinational logic.

Non-blocking assignment (<=) is executed parallely (all of them within the same block with be executed simultaneously), and is generally used in sequential logic.