1. FIFO control signals includes wr_clk, rd_clk, wr_rst, rd_rst, and prog_full. wr_rst and rd_rst are reset signals that we use to reset the FIFO buffer before each frame read to make sure the FIFO is empty before start reading. wr_clk and rd_clk are used to write into and read from the FIFO. In our case, we connect wr_clk to FPGA clock and rd_clk to okClk. Prog_full signal will notify that there are one block of data in FIFO available to be read. We connect prog_full to the ep_ready of the Pipe so the BTPipe know the FIFO is ready and read the next block from it.
2. FIFO overflow can happen when there is a delay between the python code signal the FPGA to read a frame and python start reading from BTPipeOut. In this scenario, the FPGA will read frame data continuously into the FIFO before data start to be read through BTPipeOUT, therefore overflowing the buffer.