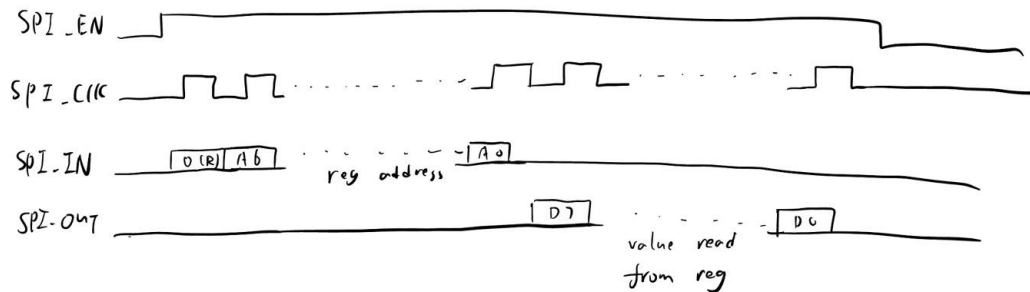


1. The frequency range for the imager's master clock is from 10 MHz to 40 MHz.
2. The SPI clock has a maximum frequency of 40 MHz.
- 3.

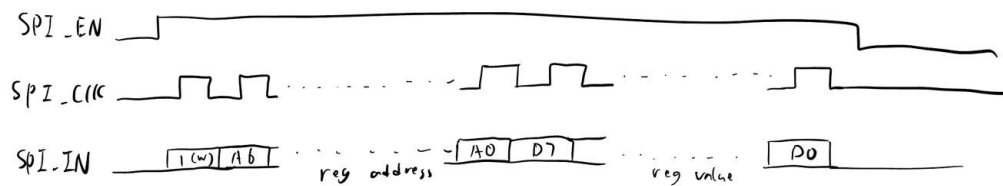
SPI Read



By using the timing diagram, I can develop a FSM to complete SPI read cycle such that I will first send register address in 8 SPI clock cycle and receive one byte of data in 8 SPI clock cycle.

4.

SPI Write



By using the timing diagram, I can develop a FSM to complete SPI write cycle such that I will send register address in 8 SPI clock cycle and send the value to write in 8 SPI clock cycle following the address.