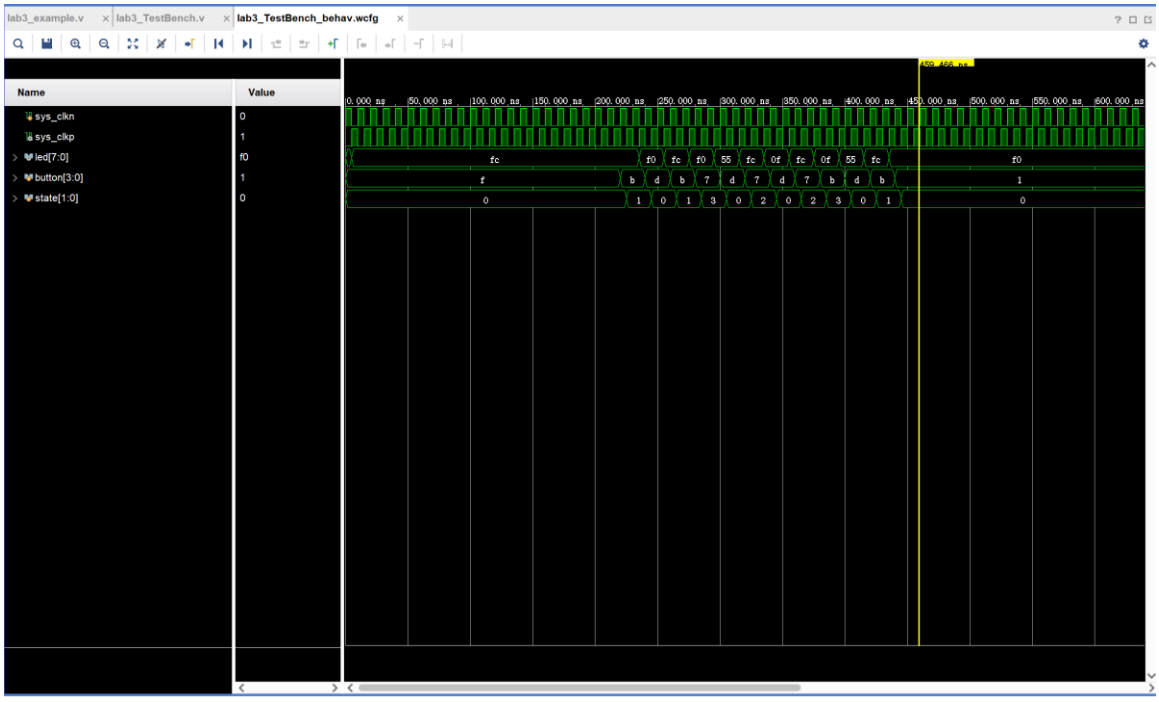
Lab3 Milestone 1 By E. Zhou & Q. Pang

Checkpoint 1.

(A) Screen shot:

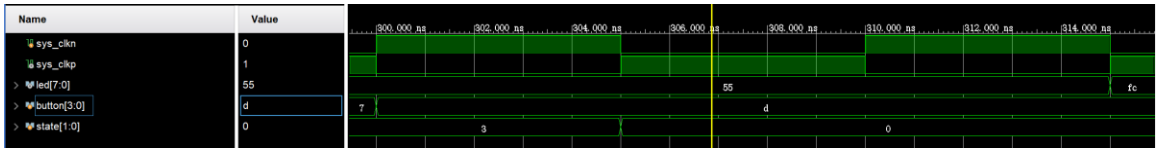


(B) a. The led output (and there for led_register) is floating (undefined) initially and requires the first falling edge to become valid in the post implementation timing simulation while in behavior simulation it is valid immediately, this showcases signal setup time.

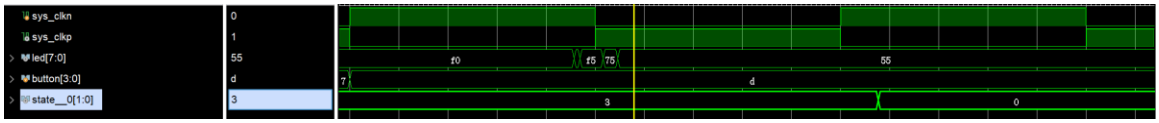
b. All bits in the led output does not update at the same time, they change at different time due to different signal delays.

c. Signals also does not update perfectly aligned with clock edges in post implementation timing sim, while signals edges aligned perfectly with clock edges in behavioral sim

Behavioral simulation:

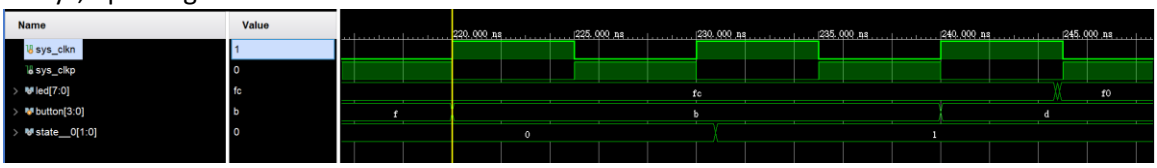


Post implementation timing simulation:



(C) It takes roughly 25ns for LEDs to change its output, there is some erroneous state between state transition, this is due to each bit of the leds output going through different amount of levels of combinational logic to be updated thus having different

delays, updating at different times.



(D) It only takes 15 ns for behavioral sim to update, this is possibally due to that change the button is pressed right at the edge of clock, the FPGA might not be able to capture this change in button resulting the change being captured 1 clock cycle later (10ns) than behavioral sim where rising clock while perfectly capture everything.