Introduction

- Large digital IC designs are made from many smaller blocks
- We can re-use the small blocks across the design
  - If pieces are also designed to a certain standard, then the process of integrating different pieces together is streamlined

Basic Library Cells

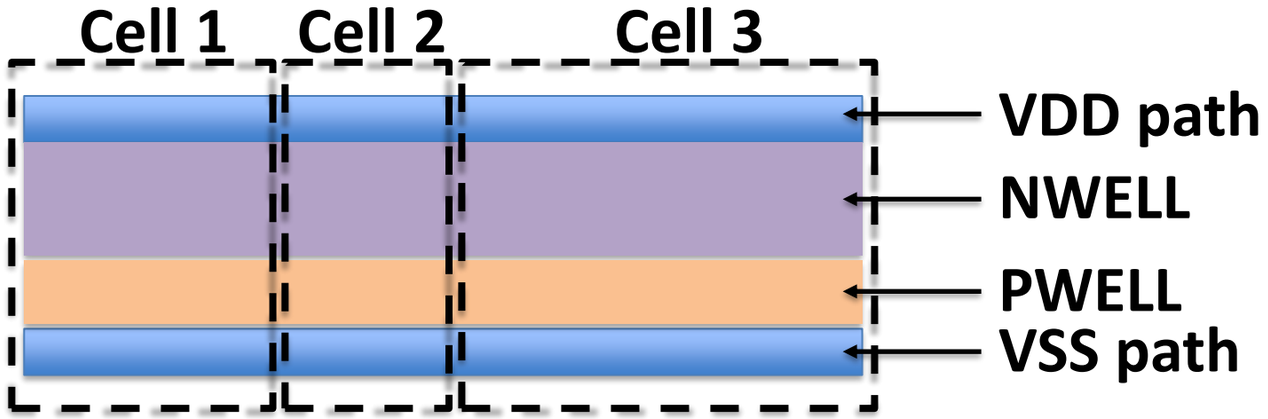
- Combinational Logic Gates
  - NAND, NOR, INV, etc.
- Sequential Logic Gates
  - Register, Latch
- Cells with a variety of sizes are created
  - Integer multiples of the minimum size (2x, 4x, 6x, 8x, etc.)
  - Remember, a 1x NAND2 should have the same current drive capability as a 1x NAND4

Creating a Library: Cell Height

- Within a standard cell library, a uniform cell height is found
  - Width of the active region determines the cell height
    - The cell height not necessarily the PDK minimum width
  - For example, if the cell height is designed to fit a 1-finger size-2 inverter, larger gates will be “wider” while height is held constant
    - Going from 2x to 4x would mean increasing the number of fingers

Creating a Library: Cell Architecture

- Several things must be constant across cells:
  - Well width
  - Cell height
  - Power Rail Path Width
- Power rails and wells should continue uninterrupted across a design

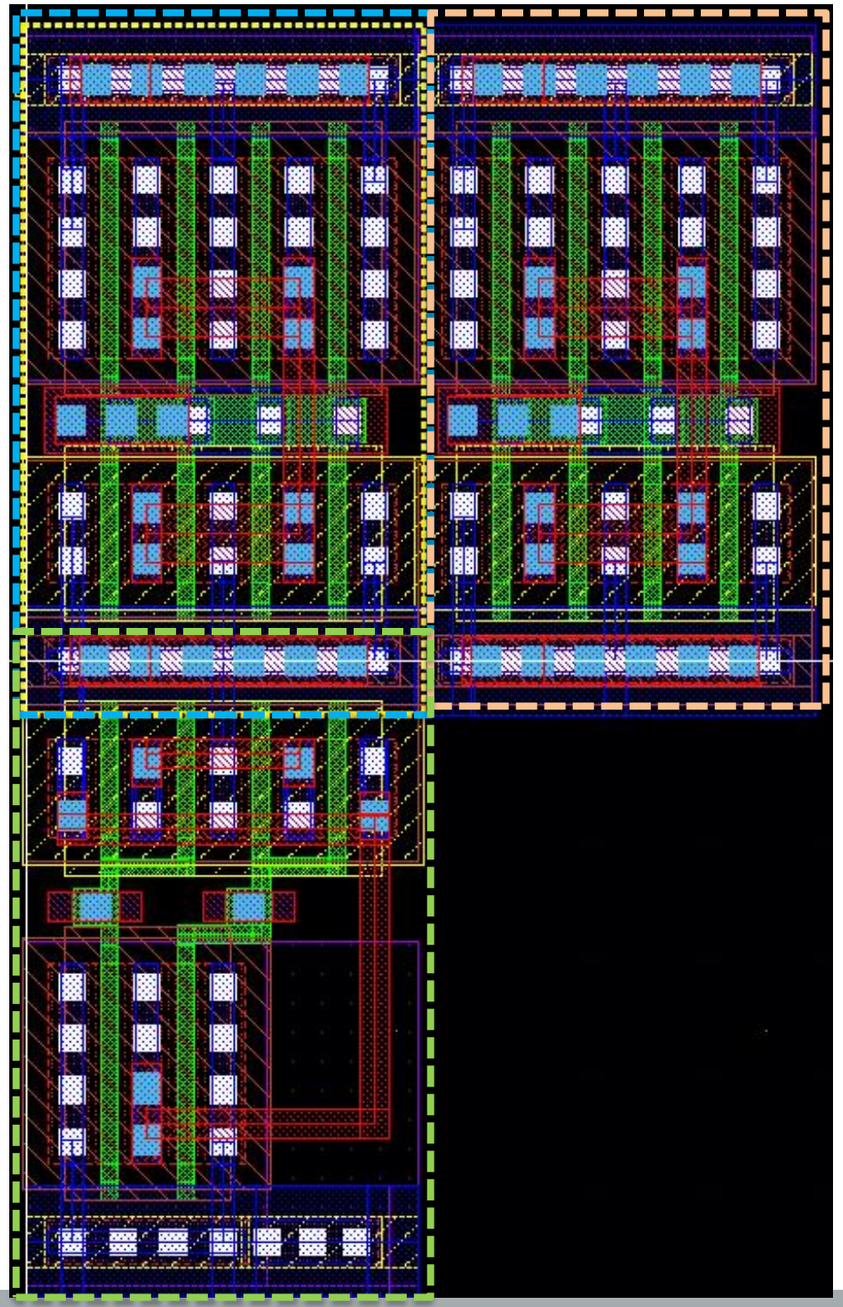


Using a Library: Placement

- Library cells are designed to be placed in a grid
  - Generally, adjacent cells will overlap a certain amount
    - Horizontal cell overlap will combine the wells
    - Vertical alignment allows the VDD/VSS well taps to overlap
  - When stacking vertically, the cells should be mirrored vertically, to merge the wells
    - The DRC spacing requirement between wells is typically large, merging wells when possible increases (improves) packing density

Using a Library: Placement Example

- Here's a screenshot
  - Dashed lines have been added to highlight the different cells
  - Note the overlap of the Psub taps



Using a Library: Routing

- Routing with many digital signals can be difficult; being organized and methodical is key
  - Standard Cells will typically use the first few metals (M1-M2)
  - Local routing between cells will use the next few metals (M3-M5)
  - Longer range routing (inter-functional block or power) will use the thick, top-level metals (M6+)
  - Typically, it helps to only use traces running a single direction on each metal layer
    - Example: traces on M4 are horizontal, traces on M5 are vertical

Using a Library: Well Taps

- Including a well tap in every cell is the easiest way to make sure the wells are properly biased
- In industry designs, there may not be a well tap in every cell
  - Those designs use Filler Cells. Two kinds:
    - Well tap cells
    - Decoupling Capacitance cells
  - This means individual cells will not pass a DRC check
    - More complicated design procedure, but area benefits