A. Target System: Our target system is a pipelined digital circuit implemented with RTL. We approach its timing verification statistically by modeling the system as a directed graph, where each node represents a pipeline register and each edge represents a timing path whose delay is described by a probability distribution. This approach accounts for process variations, environmental factors, and other uncertainties. Xilinx Vivado is used to generate the timing reports that form the basis of our statistical model [1]

   A.1. Model Availability: We Could developed simulation code that extracts a model from RTL descriptions and timing reports produced by Xilinx Vivado. model for analysis.

   A.2. Our model is implemented as simulation code.

B. Target Requirement: The requirement for our project is to verify that the pipelined design meets its timing constraints with a very low probability of failure.

   B.1. Expression as an Invariant/Temporal Property: The timing requirement is formalized as a probabilistic invariant stating that for every clock cycle, the probability of any timing path exceeding its allotted slack must be below a predetermined threshold.

   B.2. Primary Sources of Uncertainty: The main uncertainties in the design arise from process variations during manufacturing, environmental influences such as temperature fluctuations and voltage noise, and the inherent approximations in our statistical delay models.

   B.3. Verification Approach: Instead of using traditional worst-case analysis, our framework employs statistical reasoning. Through techniques like Monte Carlo simulation, we estimate the likelihood of timing violations, which allows us to pursue more aggressive performance margins while still managing risk effectively.

C. Related Work and Innovation: Research in statistical timing analysis and probabilistic verification has paved the way for our project. Notable papers in this field include:

   1. "unified framework for statistical timing analysis with coupling and multiple input switching"[2]
   2. "Low power design flow with static and statistical timing analysis" [3]
   3. "Speeding up Monte-Carlo Simulation for Statistical Timing Analysis of Digital Integrated Circuits"[4]
   4. "Statistical timing analysis of combinational logic circuits" [5]
   5. "On Timing Model Extraction and Hierarchical Statistical Timing Analysis" [6]

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