Project Proposal

1. Introduction

Introduction of the problem or system under study and why it is important. Motivate the reader. Describe your proposed approach at a high level and discuss its novelty and/or importance.

The system under study is pipelined Digital Circuit implemented with Register Transfer Level (RTL). Our proposed approach is timing verification statistically by modeling the system as a directed graph. Each node in the graph represents a pipelined register and each edge represents whose delay is described by probability distribution. This approach can provide us with a simple and easy to understand timing verification of the digital circuits with a graph representation, especially we can estimate the likelihood of timing violations, which allows us to pursue more aggressive performance margins while still managing risk effectively with tools like Monte Carlo simulation.

2. Problem statement

Give a clear mathematical description of your problem.The statement needs to be very specific and accurate. Do not talk about things generally and broadly. Be precise on the exact problem you are going to solve, using rigorous mathematical language to describe the problem when possible.If you want to address a fairly complex problem, you can decompose the problem into smaller and simplified parts. Make sure the problem is feasible.

Our approach accounts for process variations, environmental factors and other uncertainties.

3. Related work

What has been done before? Do a thorough literature review, covering different aspects related to your proposed topics. In general, you want to cite 10+ papers to show that you have done a good background review and understand relevant work.

Research in statistical timing analysis and probabilistic verification has been done previously.Some papers in this field are:

[1] A. Xilinx, "Vivado design analysis: Timing analysis," [Online]. Available: https://docs.amd.com/r/en-US/ug906-vivado-design-analysis/Timing-Analysis. AMD/Xilinx, n.d., accessed: 2025-02-17.

[2] J. K. Liou, K. T. T. Cheng, and S. R. Nassif, "A unified framework for statistical timing analysis with coupling and multiple input switching," in Proceedings of the 2005 IEEE/ACM International Conference on Computer-Aided Design (ICCAD). IEEE, 2005, pp. 134-140. [Online]. Available: https://ieeexplore.ieee.org/document/1560179.

[3] K. C. Kuo and H. T. Ko, "Low power design flow with static and statistical timing analysis," in 2012 International Symposium on Intelligent Signal Processing and Communications Systems (ISPACS). IEEE, 2012, pp. 798-801. [Online]. Available: https://ieeexplore.ieee.org/document/6473600.

[4] S. R. Naidu, "Speeding up monte-carlo simulation for statistical timing analysis of digital integrated circuits," in 20th International Conference on VLSI Design held jointly with 6th International Conference on Embedded Systems (VLSID'07). IEEE, 2007, pp. 265-270. [Online]. Available: https://ieeexplore.ieee.org/document/4076190.

[5] H. F. Jyu, S. Malik, S. Devadas, and K. W. Keutzer, "Statistical timing analysis of combinational logic circuits," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 1, no. 2, pp. 126-137, June 1993.

[6] B. Li, N. Chen, Y. Xu, and U. Schlichtmann, "On timing model extraction and hierarchical statistical timing analysis," IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, vol. 32, no. 3, pp. 367-380, March 2013.

4. Methodology

What is your planned technique to solve this problem? Why do you think it can solve your problem? What is the difference compared to prior work?

Name the tools or algorithms that may be helpful for solving your problem in your project proposal.

Evaluate the technical risks of your project - if the proposed methodology does not work, what are the potential causes? How to mitigate the potential risks?

The requirement for our project is to verify that the pipelined design meets its timing constraints with a very low probability of failure. The timing requirement is formalized as a probabilistic invariant stating that for every clock cycle, the probability of any timing path exceeding its allotted slack must be below a predetermined threshold.

As far as the risk and uncertainties are concerned, the main uncertainties in the design arise from process variations during manufacturing, environmental influences such as temperature fluctuations and voltage noise, and the inherent approximations in our statistical delay models.

We will be using features like Monte Carlo simulation for statistical reasoning instead of traditional worst case analysis. With Monte Carlo simulation, we can estimate the likelihood of timing violations, this allows us to pursue more aggressive performance margins while still managing risk effectively.

We will be using the Xilinx Vivado tool to generate timing reports which will be the basis of our statistical model.

5. Results

Give your timeline and targets (what goals do you aim to achieve? What are the deliverables? What tables/figures do you plan to show?)