SYNOPSYS®

Guide to Documentation for DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI

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DesignWare IP Component Document Set for AMBA/AXI

The DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI includes synthesizable and verification components in a technology-independent bus system that you can configure with a tool interface. DesignWare IP components for AMBA provide:

- AXI, AHB, and APB bus fabrics
- AXI, AHB, and APB components

These components handle memory management, interrupt control, intra-bus and external I/O, timer functions, reset/watch dog functions, and more. The coreAssembler tool enables you to easily connect, test and synthesize your bus system, no matter how complex.

The DesignWare IP components also include verification models for the AXI, AHB, and APB bus environments. You can use these verification models in place of application-specific logic, such as a CPU or custom peripheral device. Verification monitors log simulation activity, bus transactions, and can check for compliant bus behavior. The DesignWare verification models for AMBA are bus-functional models and monitors that you can instantiate in Vera or HDL testbenches. The coreAssembler tool also automatically adds and configures verification models on your bus system testbench.

Installation information for synthesizable components, verification models, and their supporting tools is available in the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide*. For release note information, including global issues, refer to the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Release Notes*.

Table 1-1 lists the documents that describe the DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI environment, components, and tools.

The links below access only top-level documents and are for installed components. If you would like to view documentation that you cannot access from this table, refer to the following web site:

https://www.synopsys.com/designware-ip.html

Table 1-1 Document Descriptions

Document Name	Filename	Description
General IP Component Documents – Describe tools, examples and procedures for all IP components		
DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide	DW_amba_install.pdf	Explains how to download and install the DesignWare components for AMBA and related tools. Lists component and tool versions. Lists environment variables and licenses.
DesignWare Synthesizable Components for AMBA 3 AXI, and AMBA 4 AXI User Guide	DW_iip_axi_user.pdf	Explains how to use the DesignWare components for AXI in a simple subsystem. Describes how to complete tasks using the coreConsultant GUI.
DesignWare Synthesizable Components for AMBA 2 User Guide	DW_iip_amba_user.pdf	Explains how to use the DesignWare components for AMBA in a simple subsystem. Describes how to complete tasks using the coreConsultant GUI.

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Document Name	Filename	Description
DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Release Notes	DW_amba_relnotes.pdf	Contains release note information for all DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI.
Using DesignWare Library IP in coreAssembler	coreassembler_tutorial.pdf	Describes the features provided by using DesignWare Library components in coreAssembler. Contains a number of tutorials that take you through the steps of assembling single-layer and multi-layer DesignWare subsystems for AMBA.
Synthesizable IP Documents – Describe an individual synthesizable component		
DesignWare DW_ahb Databook	DW_ahb_databook.pdf	Describes the DesignWare AHB bus fabric (DW_ahb) for AMBA. The DW_ahb includes an AHB arbiter, address decoder, and multiplexer for the AHB bus. Tutorial gives a step-by-step explanation of how to configure the DesignWare AHB component using coreConsultant.
DesignWare DW_ahb_dmac Databook	DW_ahb_dmac_databook.pdf	Describes the DesignWare AHB Direct Memory Access Controller (DW_ahb_dmac). The DW_ahb_dmac transfers data from a source peripheral to a destination peripheral over one or more AMBA AHB buses.
DesignWare DW_ahb_eh2h Databook	DW_ahb_eh2h_databook.pdf	Describes the DW_ahb_eh2h, which is used to establish an enhanced communication link between two AHB sub-systems, allowing for data exchange between a master on one AHB bus and a slave on another AHB bus.
DesignWare DW_ahb_h2h Databook	DW_ahb_h2h_databook.pdf	Describes the DW_ahb_h2h, which is used to establish a communication link between two sub-systems, allowing for data exchange between a primary master and a secondary slave.
DesignWare DW_ahb_icm Databook	DW_ahb_icm_databook.pdf	Describes the DesignWare AHB MultiLayer Interconnection Matrix synthesizable IP for connecting up to eight AHB buses to a single AHB slave.
DesignWare DW_ahb_ictl Databook	DW_ahb_ictl_databook.pdf	Describes the DW_ahb_ictl, which is a configurable, vectored interrupt controller for AMBA-based systems.

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Document Name	Filename	Description
DesignWare DW_apb Databook	DW_apb_databook.pdf	Describes the DesignWare APB bus fabric (DW_apb) for AMBA. The DW_apb is an AHB-to-APB bridge, appearing as a slave on the AHB bus. It also includes an address decoder and multiplexer for the attached APB peripherals.
DesignWare DW_apb_gpio Databook	DW_apb_gpio_databook.pdf	Describes the general-purpose I/O peripheral synthesizable IP.
DesignWare DW_apb_i2c Databook	DW_apb_i2c_databook.pdf	Describes the DesignWare I^2C bus, which is a two-wire serial interface.
DesignWare DW_apb_i2s Databook	DW_apb_i2s_databook.pdf	Describes the DW_apb_i2s, which provides a serial link designed for digital audio systems.
DesignWare DW_apb_ictl Databook	DW_apb_ictl_databook.pdf	Describes the DW_apb_ictl, a configurable, vectored interrupt controller for AMBA-based systems.
DesignWare DW_apb_rap Databook	DW_apb_rap_databook.pdf	Describes the DW_apb_rap, which is used to implement remap control, pause mode, a reset status register, and an ID code register.
DesignWare DW_apb_rtc Databook	DW_apb_rtc_databook.pdf	Describes the DW_apb_rtc real-time counter and compare peripheral synthesizable IP.
DesignWare DW_apb_ssi Databook	DW_apb_ssi_databook.pdf	Describes the DW_apb_ssi, a full-duplex Synchronous Serial Interface peripheral.
DesignWare DW_apb_timers Databook	DW_apb_timers_databook.pdf	Describes the DW_apb_timers, which are general-purpose timers.ve, or between incompatible AXI interconnect subsystems.
DesignWare DW_apb_uart Databook	DW_apb_uart_databook.pdf	Describes the DW_apb_uart, a Universal Asynchronous Receiver Transmitter.
DesignWare DW_apb_wdt Databook	DW_apb_wdt_databook.pdf	Describes the DW_apb_wdt, which is used to provide watch-dog timing, interrupt, and reset control.
DesignWare DW_axi Databook	DW_axi_databook.pdf	Describes the DW_axi, which is a multi-layer interconnect implementation of the AXI protocol.
DesignWare DW_axi_a2x Databook	DW_axi_a2x_databook.pdf	Describes the DW_axi_a2x, which is a configurable bridge between an AHB or AXI bus and an AXI bus.
DesignWare DW_axi_dmac Databook	DW_axi_dmac_databook.pdf	Describes the DW_axi_dmac, which transfers data from a source peripheral to a destination peripheral over one or more AMBA AXI buses.

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Document Name	Filename	Description
DesignWare DW_axi_gm Databook	DW_axi_gm_databook.pdf	Describes the DW_axi_gm, which is a configurable master module between a generic interface (GIF) and the AMBA AXI bus.
DesignWare DW_axi_gs Databook	DW_axi_gs_databook.pdf	Describes the DW_axi_gs, which is a configurable module between a generic interface (GIF) and the AMBA AXI bus.
DesignWare DW_axi_hmx Databook	DW_axi_hmx_databook.pdf	Describes the DW_axi_hmx, which is used for transfers from AHB masters to AXI slaves.
DesignWare DW_axi_rs Databook	DW_axi_rs_databook.pdf	Describes the DW_axi_rs, which implements a register slice as described by the AXI protocol to break long timing paths between AXI masters and AXI slaves.
DesignWare DW_axi_x2h Databook	DW_axi_x2h_databook.pdf	Describes the DW_axi_x2h, which is used to establish a communication link between an AXI bus and an AHB bus, allowing for data exchange between masters on the AXI bus and slaves on the AHB bus. For transfers from AHB masters to AXI slaves, see the DW_axi_hmx component.
DesignWare DW_axi_x2p Databook	DW_axi_x2p_databook.pdf	Describes the DW_axi_x2p, which is used to establish a communication link between an AXI and APB master or AXI interconnect subsystem to AMBA 3 APB or AMBA 2.0 APB peripheral components.
DesignWare DW_axi_x2x Databook	DW_axi_x2x_databook.pdf	Describes the DW_axi_x2x, which is used to establish a communication link between an AXI master and an AXI slave, or between incompatible AXI interconnect subsystems.
Application (Tool) Documents		
coreConsultant User Guide	coreconsultant_user.pdf	Provides information about how to perform configuration, simulation, and verification tasks with reusable synthesizable IP. All individual Synopsys synthesizable IP use coreConsultant.
coreAssembler User Guide	coreassembler_user.pdf	Provides information about how to perform connection, configuration, simulation, and verification tasks with multiple synthesizable IP. Helps to integrate synthesizable IP into simple and complex bus sub-systems.
coreTools Release Notes	relnotes.pdf	Version and notes for coreTools documentation set (includes coreConsultant and coreAssembler).
Using DesignWare Library IP in coreAssembler	tutorial	Provides an overview of DesignWare Library IP in coreAssembler.

Table 1-1 Document Descriptions

Document Name	Filename	Description
Synopsys Common Licensing (SCL) Documentation		
http://www.synopsys.com/keys	HTML pages	Helps you set up a licensing server and license key files to use Synopsys tools and DesignWare libraries. DesignWare license requirements are described in the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide*.

Web Resources

- DesignWare IP product information: https://www.synopsys.com/designware-ip.html
- Your custom DesignWare IP page: https://www.synopsys.com/dw/mydesignware.php
- Documentation through SolvNetPlus: https://solvnetplus.synopsys.com (Synopsys password required)
- Synopsys Common Licensing (SCL): https://www.synopsys.com/keys

Customer Support

Synopsys provides the following various methods for contacting Customer Support:

- Prepare the following debug information, if applicable:
  - For environment set-up problems or failures with configuration, simulation, or synthesis that occur within coreConsultant or coreAssembler, select the following menu:

    File > Build Debug Tar-file

    Check all the boxes in the dialog box that apply to your issue. This option gathers all the Synopsys product data needed to begin debugging an issue and writes it to the <*core tool startup directory*>/debug.tar.gz file.
  - For simulation issues outside of coreConsultant or coreAssembler:
    - Create a waveforms file (such as VPD or VCD).
    - Identify the hierarchy path to the DesignWare instance.
    - Identify the timestamp of any signals or locations in the waveforms that are not understood.
- *For the fastest response*, enter a case through SolvNetPlus:

  a. https://solvnetplus.synopsys.com

> **Note** SolvNetPlus does not support Internet Explorer. Use a supported browser such as Microsoft Edge, Google Chrome, Mozilla Firefox, or Apple Safari.

  b. Click the **Cases** menu and then click **Create a New Case** (below the list of cases).

  c. Complete the mandatory fields that are marked with an asterisk and click **Save**.

Ensure to include the following:

- **Product L1:** DesignWare Library IP
- **Product L2:** <name of L2>

d. After creating the case, attach any debug files you created.

For more information about general usage information, refer to the following article in SolvNetPlus:

https://solvnetplus.synopsys.com/s/article/SolvNetPlus-Usage-Help-Resources

- Or, send an e-mail message to support_center@synopsys.com (your email will be queued and then, on a first-come, first-served basis, manually routed to the correct support engineer):
  - Include the Product L1 and Product L2 names, and Version number in your e-mail so it can be routed correctly.
  - For simulation issues, include the timestamp of any signals or locations in waveforms that are not understood
  - Attach any debug files you created.
- Or, telephone your local support center:
  - North America:
    Call 1-800-245-8005 from 7 AM to 5:30 PM Pacific time, Monday through Friday.
  - All other countries:
    https://www.synopsys.com/support/global-support-centers.html