SYNOPSYS®

DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI

Release Notes

2020.12a AMBA 2 Release
2020.03a AMBA 3 AXI/AMBA 4 AXI Release

2020.12a
December 2020

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Contents

Preface

This manual describes release issues regarding DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI and contains information of interest to anyone using DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI.

Release Notes Organization

The chapters of this databook are organized as follows:

- Chapter 1, "AMBA 2 Release Notes" lists the features, issues, and past releases related to the DesignWare Synthesizable Components for AMBA 2.
- Chapter 2, "AMBA 3 AXI/AMBA 4 AXI Release Notes" lists the features, issues, and past releases related to the DesignWare Synthesizable Components for AMBA 3 AXI/AMBA 4 AXI.
- Chapter 3, "Pre-October 2007 AMBA 2 STARs" contains archived STAR tables for AMBA 2.
- Chapter 4, "Pre-October 2007 AMBA 3 AXI STARs" contains archived STAR tables for AMBA 3 AXI.

Related Documents

To see a complete listing of documentation available for the DesignWare synthesizable and verification components for AMBA/AXI, refer to the *Guide to Documentation for DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI (Documentation Overview)*.

To see installation instructions for all DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI, refer to the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide*.

Web Resources

- DesignWare IP product information: https://www.synopsys.com/designware-ip.html
- Your custom DesignWare IP page: https://www.synopsys.com/dw/mydesignware.php
- Documentation through SolvNetPlus: https://solvnetplus.synopsys.com (Synopsys password required)
- Synopsys Common Licensing (SCL): https://www.synopsys.com/keys

Customer Support

Synopsys provides the following various methods for contacting Customer Support:

- Prepare the following debug information, if applicable:
  - For environment set-up problems or failures with configuration, simulation, or synthesis that occur within coreConsultant or coreAssembler, select the following menu:

    File > Build Debug Tar-file

    Check all the boxes in the dialog box that apply to your issue. This option gathers all the Synopsys product data needed to begin debugging an issue and writes it to the <*core tool startup directory*>/debug.tar.gz file.
  - For simulation issues outside of coreConsultant or coreAssembler:
    - Create a waveforms file (such as VPD or VCD).
    - Identify the hierarchy path to the DesignWare instance.
    - Identify the timestamp of any signals or locations in the waveforms that are not understood.
- *For the fastest response*, enter a case through SolvNetPlus:

  a. https://solvnetplus.synopsys.com

  

  SolvNetPlus does not support Internet Explorer. Use a supported browser such as Microsoft Edge, Google Chrome, Mozilla Firefox, or Apple Safari.

  b. Click the **Cases** menu and then click **Create a New Case** (below the list of cases).

  c. Complete the mandatory fields that are marked with an asterisk and click **Save**.

  Ensure to include the following:
  - **Product L1:** DesignWare LIbrary IP
  - **Product L2:** AMBA

  d. After creating the case, attach any debug files you created.

  For more information about general usage information, refer to the following article in SolvNetPlus:

  https://solvnetplus.synopsys.com/s/article/SolvNetPlus-Usage-Help-Resources
- Or, send an e-mail message to support_center@synopsys.com (your email will be queued and then, on a first-come, first-served basis, manually routed to the correct support engineer):
  - Include the Product L1 and Product L2 names, and Version number in your e-mail so it can be routed correctly.
  - For simulation issues, include the timestamp of any signals or locations in waveforms that are not understood
  - Attach any debug files you created.
- Or, telephone your local support center:
  - North America:

    Call 1-800-245-8005 from 7 AM to 5:30 PM Pacific time, Monday through Friday.

- All other countries:
  https://www.synopsys.com/support/global-support-centers.html

1 AMBA 2 Release Notes

This chapter presents the latest release information about the DesignWare components for AMBA 2.

Refer to the *coreTools Release Notes* for a list of known problems and limitations in coreConsultant and coreAssembler.

Note Before invoking the coreConsultant GUI, you must set the VRO_CACHE_DIR variable to any local directory that is used to install the VIP-related VRO files.

1.1 STARs on the Web

You can view problem reports for components used in this release, including problems identified after product release, by accessing the STAR report on the Web. Note that you must have a SolvNetPlus ID in order to view STAR reports. You can access STAR reports for any verification or synthesizable IP component through the IP Directory:

http://www.synopsys.com/dw/ipsearch.php

1.2 Global AMBA 2 New Features and Changes

The following was new or had changed during various versions of DesignWare Synthesizable Components for AMBA 2.

Changes in 2020.12a

- Updated all AMBA components
- Removed support for the software drivers
- Removed support for synchronizer depth corresponding to 'first stage negative edge flipflop and second stage positive edge flipflop'.

Changes in 2018.07a

- Updated all AMBA components
- Removed support for NC Verilog Simulator and MTI Simulator

Changes in 2016.10a

- Updated all AMBA components

Changes in 2015.06a

- Updated all AMBA components
- Documentation for the dwh_update tool has been removed because the tool has been deprecated

Changes in 2014.06a

- Updated all AMBA components

Changes in 2013.05a

- Updated components:
  - DW_ahb_dmac
  - DW_ahb_ictl
  - DW_apb_i2c
  - DW_apb_i2s

Changes in 2012.06a

- Updated components:
  - DW_apb_gpio
  - DW_apb_i2c
  - DW_apb_timers
  - DW_apb_uart

Changes in 2012.03a

- Updated components:
  - DW_ahb_dmac
  - DW_ahb_eh2h
  - DW_ahb_icm
  - DW_ahb_ictl
  - DW_apb_gpio
  - DW_apb_i2c
  - DW_apb_i2s
  - DW_apb_ictl
  - DW_apb_rap
  - DW_apb_rtc
  - DW_apb_ssi

  - DW_apb_timers
  - DW_apb_uart
  - DW_apb_wdt
- Removed DW_memctl component from AMBA 2 image; DW_memctl now available in separate image

Changes in 2011.11a

- Updated components:
  - DW_ahb
  - DW_ahb_dmac
  - DW_ahb_eh2h
  - DW_ahb_ictl
  - DW_apb_gpio
  - DW_apb_i2c
  - DW_apb_i2s
  - DW_apb_ictl
  - DW_apb_rap
  - DW_apb_rtc
  - DW_apb_ssi
  - DW_apb_timers
  - DW_apb_uart
  - DW_apb_wdt

Changes in 2011.10a

- Updated all AMBA components
- Uses coreTools version 2010.09-SP2

Changes in 2011.06a

- Updated components:
  - DW_apb
  - DW_apb_uart
  - DW_memctl
- Enhanced “Related Documents” section in Preface of databooks.

Changes in 2011.04a

- Corrected syntax error in runtest.pm
- Updated components:
  - DW_ahb_dmac
  - DW_ahb_ictl
  - DW_apb
  - DW_apb_gpio
  - DW_apb_i2c
  - DW_apb_i2s
  - DW_apb_ictl
  - DW_apb_ssi
  - DW_apb_uart
  - DW_memctl

Changes in 2010.12a

- Updated components:
  - DW_ahb_dmac
  - DW_apb
  - DW_apb_i2c
  - DW_apb_ssi

Changes in 2010.10a

- Updated components:
  - DW_ahb_eh2h
  - DW_ahb_h2h
  - DW_apb_i2c
  - DW_apb_ssi

Changes in 2010.09a

- Updated all AMBA components
- Packaging now associates SPIRIT memory map of each component with relevant interface of component
- Description field of SPIRIT .xml memory map description of each component reviewed to remove variable and unnecessary information
- All component simulations now generate .vpd dump file
- Simulation scripts enhanced to supported new versions of VCS

- All components reviewed to ensure DW licenses pulled only if a source licence is not present
- Unnecessary Design Compiler scripts removed from all components
- Unconnected sub-module input and output ports removed from all components
- Defunct DesignWare connect scripts removed from AMBA image
- Internal Design Compiler script changed from Design Compiler shell to Design Compiler TCL
- Input/Output section of all databooks reviewed to correct “Registered” description
- Moved to coreTools 2010.03-SP1-1

Changes in 2010.02a

- Updated components:
  - DW_apb_i2c
  - DW_apb_i2s
  - DW_apb_ssi
- Moved to coreTools 2010.03

Changes in 2009.06a

- Updated components:
  - DW_apb_ssi component
- RTL changes:
  - No global changes

Changes in 2008.10a

- Updated components:
  - All AMBA 2 components
- RTL changes:
  - Added STAR-on-the-Web (SotW) note on Tetramax
  - Corrected coreConsultant and coreAssembler link to common release notes
  - Uses coreTools version 2008.06-SP2-2

Changes in 2008.09a

- Updates to the license copyright notice in the driver source files
- Updates to the version numbers of all driver user guides
  - DW_ahb_dmac – 1.01c
  - DW_apb_gpio – 1.00c
  - DW_apb_i2c – 1.01c

- DW_apb_uart – 1.01c
- DW_memctl – 1.00c

Changes in 2008.06a

- Updated components:
  - All AMBA 2 components
- Uses coreTools version 2007.06-SP4

Changes in 2008.04a

- Updated component:
  - DW_ahb_dmac

Changes in 2008.03a

- Updated component:
  - DW_memctl
- Hyperlinks to the coreTools documentation is now directed to the web instead of the local installation tree; refer to the *Guide to coreTools Documentation*.

Changes in 2008.02a

- Removed the "Global Issues for 2007.12a Release of AMBA 2" section from the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide (Documentation Overview)*.

There were no global features or changes for the 2007.12a version of DesignWare Synthesizable Components for AMBA 2.

Changes in 2007.11a

- All AMBA 2.0 and AMBA 3 AXI release notes are now consolidated into this single release notes document.

Changes in 2007.06a

- Update to use coreTools 2007.06-1 or later

Changes in 2007.04a

- New component: DW_apb_i2s (Inter-IC sound bus)
- coreAssembler flow in Chapter 2 of all AMBA 2 databooks
- Update to use coreTools 2006.03-SP5

Changes in 2005.04a

- Hierarchical design support in coreAssembler; Connect no longer supported
- Update to use coreTools version 6.0

1.3 Known Global AMBA 2 Issues

There are no known AMBA 2 issues.

1.4 Individual AMBA 2 Release Notes

The following subsections contain the latest component-specific information about the individual AMBA 2 components.

1.4.1 DW_ahb

The following sections list the new features and changes, and the fixed problems and enhancements, for the DW_ahb component. For DW_ahb-specific STARs, refer to:

https://www.synopsys.com/dw/star.php?c=DW_ahb

For detailed features description see the *DW_ahb databook*.

For information on known issues, refer to "DW_ahb Known Problems and Workarounds" on page 21.

1.4.1.1 DW_ahb New Features and Changes

This section describes what was new or had changed during the various versions of the DW_ahb:

Changed in 2.15a version of DW_ahb

- RTL Changes:
  - RTL compliance to SpyGlass Q-2020.03-SP1 and GuideWare 2020.03
  - Enhancement:
    - STAR 9001549439: The HRESP signal is updated to reflect as 1-bit when IP is used in AHB-Lite sub-system as per AMBA 3 AHB-Lite Protocol Specification 1.0. New configuration parameter is added to determine the width of the HRESP signal.
    - STAR 9001245185: AHB5 protocol support as per the specification AMBA 5 AHB Protocol Specification AHB5, AHB-Lite
- Documentation changes:
  - Refer to the Revision History chapter of the DW_ahb databook
- Packaging changes:
  - STAR 3115176: Updated sWork::evalInComponent to align with coreTools version Q-2020.03-SP4-2
  - Minor packaging updates

Changed in 2.14a version of DW_ahb

- RTL Changes:
  - RTL compliance to SpyGlass 2017.12-SP1 and GuideWare 2017.12
- Documentation and/or coreTools changes:
  - Version update
  - Updated Synthesis results in the Integration Considerations chapter of the databook
  - Published the first version of DesignWare Synthesizable Components for AMBA 2 User Guide
  - Removed Chapter 2 “Building and Verifying a Component or Subsystem” from the databook and added the content in the newly created user guide
  - Signals, Parameters, Registers and Internal parameters chapter auto-extracted with change bars from the RTL
  - Uses coreTools version N-2017.12-SP2
- Packaging changes:
  - coreAssembler packaging update to make sure that AHB_LITE parameter value from RTL is reflected to the interface parameter.
  - Minor packaging updates
- Removed support for NC Verilog Simulator and MTI Simulator

Changed in 2.13a version of DW_ahb

- RTL Changes:
  - Lint Cleanup
  - Enhanced to support maximum number of slaves from 16 to 32
- Documentation and/or coreTools changes:
  - Version update
  - Parameter Descriptions and Register Descriptions auto-extracted from the RTL
  - Removed references to Leda
  - Added “Non-Standard Master ID Sideband Signal”
  - Updated Area and Power numbers
  - Uses coreTools version 2016.09

Changed in 2.12a version of DW_ahb

- RTL Changes:
  - Lint Cleanup
- Documentation and/or coreTools changes:
  - Version update
  - Signal Descriptions chapter auto-extracted from the RTL
  - Added a note for AHB-Lite and EBT behaviors in the databook
  - Uses coreTools version 2014.12-SP1-1
- Packaging changes:
  - Minor packaging enhancements
  - Memory Map updates for defining access type to reserved fields

Changed in 2.11a version of DW_ahb

- RTL changes:
  - Lint cleanup
- Documentation and/or coreTools changes:
  - Version update
  - Uses coreTools version 2013.03-SP1-2
  - Updated a performance section in Integration considerations
  - Corrected the Default Input/Output Delay values in Signals chapter
- Packaging changes:
  - Minor packing enhancements
  - IP-XACT enhancement for enumeration and display names

Changed in 2.10c version of DW_ahb

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Updated the databook template
  - Uses coreTools version 2012.06-SP2
- Packaging changes:
  - Corrected file prefixing in the encrypted mode

Changed in 2.10b version of DW_ahb

- RTL changes:
  - Corrected inconsistencies in RAL files
- Documentation and/or coreTools changes:
  - None

Changed in 2.10a version of DW_ahb

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.09-SP2
  - Revised paragraph for Second Tier Arbitration explaining possibility of master being "starved" by bus

Changed in 2.09a version of DW_ahb

- RTL changes:
  - Ability to set slave as split-capable when DW_ahb is configured as AHB Lite has been removed, since it is an illegal scenario
- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.03 or later
  - Corrected names of include files and vcs command used for simulation in databook
  - Corrected syntax for undef directive
  - Updated system diagram in Figure 1-1
  - Enhanced "Related Documentation" section in Preface

Changed in 2.08a version of DW_ahb

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Updated description of DFT_MST register
  - Uses coreTools version 2008.06-SP2-2

Changed in 2.07a version of DW_ahb

- RTL changes:
  - SPLIT_CAPABLE_* dependency on AHB_LITE detailed in cC GUI
  - SPIRIT .xml address map generation fixed to take arbiter slave interface base address into account
  - Third party simulator tool version requirements aligned with DESIGNWARE verification IP requirements
  - Arbiter registers not part of XML register report if AHB_LITE =
  - Packaging fix to allow coreAssembler ping test to pass if REMAP enabled in DW_ahb instance
  - RTL change to select decoded slave outputs when HTRANS=IDLE
- Documentation and/or coreTools changes:
  - SPLIT_CAPABLE_* dependency on AHB_LITE detailed in databook
  - Uses coreTools version 2007.06-SP4

Changed in 2.06b version of DW_ahb

- RTL changes:
  - Packaging fixed to enable USE_FOUNDATION parameter for all configurations
  - Memory map now defined for its arbiter interface
- Documentation and/or coreTools changes:
  - Uses coreTools version 2007.06-1 or later

Changed in 2.06a version of DW_ahb

- Enhanced databook includes coreAssembler intent in Chapter 2.
- The coreAssembler or coreConsultant GUIs can now be used to select VIP/VMT versions.
- Register descriptions are now included in SPIRIT files.

Changed in 2.05a version of DW_ahb

- The DW_ahb now waits for the hlock/hbusreq to become active before driving hmastlock.
- Enhanced databook includes coreAssembler intent in Chapter 2

Changed in 2.04a version of DW_ahb

- A new flow tutorial based on DesignWare Connect now comprises Chapter 2, "Building and Verifying a Component or Subsystem," of the *DesignWare DW_ahb Databook*.
- The DW_ahb can now be used in the coreTools 5.*x* environment.
- The DW_ahb now supports the DC-FPGA environment.
- The size of the DesignWare Synthesizable Components image has been reduced to about 60 MB by removing the DesignWare Memory Model TSP and the QuickStart examples designs; these are now available through separate downloads. For more information, refer to the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide*.
- The DesignWare Synthesizable Components image is now self-extracting.

Changed in 2.03a version of DW_ahb

- Source code for this component is available on a per-project basis as a DesignWare Core. Please contact your local sales office for the details. For source licensing information, refer to "Licenses" in the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide*.

Changed in 2.02a version of DW_ahb

- AMBA Compliance Tool certification and recertification
- Data width support of 8 and 16 bits (in addition to 32, 64, 128, and 256).
- AHB monitoring for all simulators.
- DesignWare Connect – Enables you to construct, modify, and simulate any single- or multi-layer system in about an hour.
- The HP-UX platform is not supported.
- VHDL simulation is not supported.
- The Verilog-XL simulator is not supported.

Changed in 2.01a version of DW_ahb

- In the memory map, the name of the Version ID register, now known as the Component Version register, has changed from AHB_VERSION_ID to AHB_COMP_VERSION.

1.4.1.2 DW_ahb Releases

Table 1-1 lists the latest versions of the DW_ahb component, the releases in which they were included, and the corresponding AHB_COMP_VERSION register values.

Table 1-1 DesignWare for AMBA 2/DW_ahb Release

DesignWare Release for AMBA 2	DW_ahb Version	AHB_COMP_VERSION value	Databook Date
2020.12a	2.15a	32_31_35_2A	December 2020

DesignWare Release for AMBA 2	DW_ahb Version	AHB_COMP_VERSION value	Databook Date
2018.07a	2.14a	32_31_34_2A	July 2018
2016.10a	2.13a	32_31_33_2A	October 2016
2015.06a	2.12a	32_31_32_2A	June 2015
2014.06a	2.11a	32_31_31_2A	June 2014
2013.05a	2.10c	32_31_30_2A	May 2013
2011.11a	2.10b	32_31_30_2A	November 2011
2011.10a	2.10a	32_31_30_2A	October 2011
2010.09a	2.09a	32_30_39_2A	September 2010
2009.06a	2.08a	32_30_38_2A	June 2009
2008.10a	2.08a	32_30_38_2A	October 2008
2008.06a	2.07a	32_30_37_2A	June 2008
2007.06a	2.06b	32_30_36_2A	June 2007
2007.04a	2.06a	32_30_36_2A	April 2007
2005.04a	2.05a	32_30_35_2A	June 2006
2005.04a	2.04a	32_30_34_2A	April 2005
2004.11	2.03a	32_30_33_2A	November 2004
2004.06	2.02a	32_30_32_2A	June 21, 2004
2003.10	2.01a	32_30_31_2A	October 22, 2003
2003.02	2.00a	32_30_30_41	March 26, 2003
2002.08-SP1-4	1.13a	31_31_33_41	January 22, 2003
2002.08-SP1-2	1.12a	31_31_32_41	January 22, 2003
2002.08-SP1	1.11c	31_31_31_43	August 21, 2002
2002.08	1.11b	31_31_31_42	August 21, 2002

1.4.1.3 DW_ahb Known Problems and Workarounds

The following are known issues in this release of the DW_ahb:

- STAR 9000033105 – When a master (m1) which is a part of a multi-master environment starts a locked transfer and the previous transfer from another master (m2) receives an error response, the first transfer from m1 is transmitted as unlocked.

It is feasible for a master to transition from IDLE to NSEQ when hready is low. The DW_ahb is not handling this situation correctly when there is a locked transfer because it is relying on hready before driving the hmastlock.

- In coreAssembler with DW_ahb, "Specify Testbench" activity results in an error if "Close DUT Workspace" option is unchecked while creating Testbench workspace. The workaround for this issue is to check "Close DUT Workspace" option while creating Testbench workspace.

1.4.2 DW_ahb_dmac

The following sections list the new features and changes, and the fixed problems and enhancements, for the DW_ahb_dmac component. For DW_ahb_dmac-specific STARs, refer to:

https://www.synopsys.com/dw/star.php?c=DW_ahb_dmac

For the DW_ahb_dmac databook, refer to:

https://www.synopsys.com/dw/doc.php/iip/DW_ahb_dmac/latest/doc/DW_ahb_dmac_databook.pdf

For information on known issues, refer to "DW_ahb_dmac Known Problems and Workarounds" on page 31.

1.4.2.1 DW_ahb_dmac New Features and Changes

This section describes what was new or changed during the various versions of the DW_ahb_dmac:

Changed in 2.23a version of DW_ahb_dmac

- RTL Changes:
  - RTL compliance to SpyGlass Q-2020.03-SP1 and GuideWare 2020.03
  - Enhancement:
    - STAR 9001372810: Removal of reset port from the clock gating cell used in the IP when Low-power feature is enabled
    - STAR 9001549439: The HRESP signal is updated to reflect as 1-bit when IP is used in AHB-Lite sub-system, as per AMBA 3 AHB-Lite Protocol Specification 1.0. New configuration parameters are added which determine the width of the HRESP signal.
- Documentation changes:
  - Refer to the Revision History chapter of the DW_ahb_dmac databook
- Packaging changes:
  - STAR 3115176: Updated sWork::evalInComponent to align with coreTools version Q-2020.03-SP4-2
  - Minor packaging updates

Changed in 2.22a version of DW_ahb_dmac

- RTL Changes:
  - RTL compliance to SpyGlass 2017.12-SP1 and GuideWare 2017.12

  - Fixed Defects:
    - STAR 9001156903: The DMAC channel registers SSTATRx and DSTATRx upper bits [63:32] are read-only bits as per the register definition. In the RTL upper bits [63:32] are behaving as read-write. The RTL is updated to make upper bits [63:32] as read-only.
    - STAR 9001376121: Fixed an RTL issue in which the read value of CHx_FIFO_DEPTH field of DMA_COMP_PARAMS_x register is incorrect. When any channel of DW_ahb_dmac is configured with FIFO DEPTH as 256, the read value of CHx_FIFO_DEPTH field of DMA_COMP_PARAM_x register is not correct. It returns 0x4 instead of 0x5. The RTL is updated to return the correct read value (0x5 in case of CHx_FIO_DEPTH = 256).
- Documentation and/or coreTools changes:
  - Version update
  - Updated Synthesis results in the Integration Considerations chapter of the databook
  - Published the first version of DesignWare Synthesizable Components for AMBA 2 User Guide
  - Removed Chapter 2 “Building and Verifying a Component or Subsystem” from the databook and added the content in the newly created user guide
  - Signals, Parameters, Registers and Internal parameters chapter auto-extracted with change bars from the RTL
  - Uses coreTools version N-2017.12-SP2
  - Access type for ReqSrcReg.SRC_REQ_WE register field is updated to write-only instead of read-write to match the design intent. SRC_REQ_WE is write enable and it is a write-only field. Respective software handshaking registers such as ReqDstReg, SglRqSrcReg, SglRqDstReg, LstSrcReg, LstDstReg are updated.
- Packaging changes:
  - Minor packaging updates
- Removed support for NC Verilog Simulator and MTI Simulator

Changed in 2.21a version of DW_ahb_dmac

- RTL Changes:
  - Lint Cleanup
  - Enhancement:
    - Support for DMA level/Channel level clock gating
  - Fixed Issue:
    - Condition in which DMAC abruptly terminates the source transfer causing unpredictable behavior
- Documentation and/or coreTools changes:
  - Version update
  - Removed references to Leda
  - Parameter Descriptions and Register Descriptions auto-extracted from the RTL

- Added the “Low Power Modes – Global and Channel Clock Gating” section
- Uses coreTools version 2016.09

Changed in 2.20a version of DW_ahb_dmac

- RTL Changes:
  - Lint Cleanup
  - Fixed:
    - FIFO_EMPTY bit behavior changed to read-only
    - Unwanted dummy transfers when source asserts LAST before destination transfer starts
    - Incorrect reset value of CTLx and DMA_COMP_VERSION registers
- Documentation and/or coreTools changes:
  - Version update
  - Signal Descriptions chapter auto-extracted from the RTL
  - Uses coreTools version 2014.12-SP1-1
- Packaging changes:
  - Minor packaging enhancements
  - Memory Map updates for defining access type to reserved fields

Changed in 2.19a version of DW_ahb_dmac

- RTL changes:
  - Enhanced for the Big endian BE32 format for data transfer on AHB master interface
  - Lint cleanup
- Documentation and/or coreTools changes:
  - Version update
  - Enhancement for Big endian support
  - Updated the “Performance” section in “Integration Considerations” chapter
  - Uses coreTools version 2013.03-SP1-2
  - Corrected the Default Input/Output Delay values in Signals chapter
- Packaging changes:
  - Minor packing enhancements
  - IP-XACT enhancement for enumeration and display names
  - Corrected data description inconsistencies in RAL files.

Changed in 2.18b version of DW_ahb_dmac

- RTL changes:
  - Added an output signal dma_wlast on the AHB interface to indicate the last write data during burst transfers to destination peripherals.

  - Added a configuration parameter DMAH_WLAST_EN to enable this signal.
  - Added a channel suspend feature for fixed bursts.
- Documentation and/or coreTools changes:
  - Added the section "Last Beat of DMA Burst Indication" on page 108 of the DW_ahb_dmac Databook.
  - Removed a note stating that disabling the channel via software prior to completing a transfer is not supported when DW_ahb_dmac is configured to use defined length bursts. This feature is now supported.
  - Made a minor correction in the sequence of bits in the DMA_COMP_PARAMS_1 register.
  - Updated the databook template.
  - Uses coreTools version 2012.06-SP2
- Packaging changes:
  - Corrected file prefixing in the encrypted mode

Changed in 2.17a version of DW_ahb_dmac

- RTL changes:
  - Removed overlapping address blocks
  - Fixed mismatch between RAL/XML/databook for CFG*x* register
  - Fixed incorrect reset value of CTL*x*.SRC[DST]_TR_WIDTH fields in RAL and XML
- Documentation and/or coreTools changes:
  - Enhanced DW_ahb_dmac and DW_apb_i2c programming example
  - Clarified instructions for setting bit 0 of DmaCfgReg register
  - Enhanced descriptions of SSTATAR*x* and DSTATAR*x* registers
  - Enhanced information in Early-Terminated Burst Transaction section

Changed in 2.17c version of DW_ahb_dmac

- RTL changes:
  - Corrected inconsistencies in RAL files
- Documentation and/or coreTools changes:
  - None

Changed in 2.17b version of DW_ahb_dmac

- RTL changes:
  - None

- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.09-SP2

Changed in 2.17a version of DW_ahb_dmac

- RTL changes:
  - Corrected problem where false block interrupt is generated in linked-list-based multi-block transfers when interrupts for block are enabled while previous block has interrupts disabled
  - Corrected AHB slave interface so that DW_ahb_dmac can accept transfers received in the second cycle of a two-cycle response
  - New user configurable parameter added: DMAH_REVERSE_WB_OVERRIDE; when parameter is set, write back order is changed to: CTRLx, SSTATx, DSTATx
  - Added option to reduce latency (with potential trade-off in operating frequency)
  - Added C headers to component package
  - Corrected default value of COMP_PARAMS registers in RAL file generated by coreConsultant
  - Corrected LLP*n* entries in generated RAL file
- Testbench changes:
  - Testbench inactivity watchdog timeout extended to cover legitimate periods of inactivity in the simulations
  - Corrected false invalid transaction testbench error when channel is disabled while a transaction is ongoing
- Documentation and/or coreTools changes:
  - Added new "Latency" section to databook
  - New user-configurable parameter added: DMAH_REVERSE_WB_OVERRIDE. When this parameter is set, the write back order changes to: CTRL*x*, SSTAT*x*, DSTAT*x*
  - Added information to "Memory Peripherals" section about impact of CTLx.SRC_MSIZE, CTLx.DEST_MSIZE values on burst transfers to/from memory peripherals
  - Corrected access mode and field description for several registers in RAL file

Changed in 2.16a version of DW_ahb_dmac

- RTL changes:
  - Modified RTL to reverse the order of the status write back to LLI memory.
- Testbench changes:
  - Fixed root cause for the following warning message:

```
WARNING test_DW_ahb_dmac.vshell.ahb-command-monitor 1018850 [RECMDATAVALID]
Valid data does not appear on the correct byte lanes for the transfer...
```

- Documentation and/or coreTools changes:
  - None

Changed in 2.15a version of DW_ahb_dmac

- RTL changes:
  - Description of DEST_PER and SRC_PER fields of CFG*x* register fixed in generated memory map .xml; RTL enhanced to optimize away bits of these fields depending on number of hardware handshaking interfaces
  - Description of DMAH_INTR_POL parameter fixed in coreConsultant/coreAssembler GUI
- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.03 or later
  - Modified descriptions for dma_req signal to clarify that DMA hardware handshaking interface signals are level-sensitive, not edge-sensitive
  - Corrected names of include files and vcs command used for simulation in databook
  - Corrected syntax for undef directive
  - Corrected defaults for DMAH_CH*x*_SMS and DMAH_CH*x*_DMS

Changed in 2.14a version of DW_ahb_dmac

- RTL changes:
  - To prevent protocol violations, source pre-fetch that has not completed when the destination flow controller signals the transfer is complete is not canceled.
  - DMA correctly completes split transfer.
- Documentation and/or coreTools changes:
  - Uses coreTools version 2008.06-SP2-2

Changed in 2.13a version of DW_ahb_dmac

- RTL changes:
  - Added an undef file (./src/DW_ahb_Dmac_undef.v) to support multiple instances of the DW_ahb_dmac core
- Documentation and/or coreTools changes:
  - Changed version of databook

Changed in 2.12a version of DW_ahb_dmac

- RTL changes:
  - Added support for defined length bursts
  - Increased maximum configuration of FIFO depth to 256 bytes

- Resolved issue in the DW_ahb_dmac when:
  - destination peripheral is the flow controller,
  - src peripheral has pre-fetch enabled, and
  - src fails to complete a defined length burst
- Removed SCAN_MODE pin from component

- Documentation and/or coreTools changes:
  - Uses coreTools version 2007.06-SP4
  - Descriptions for software handshaking registers now say that channel must be enabled to allow writing to a bit
  - Corrected description of DMAH_CHx_MULTI_BLK_TYPE parameter
  - Corrected Figure 71
  - Corrected LLPx register field description
  - Removed redundant hyperlink
  - Updated description on stopping LLI transfers
  - Updated description of registers to indicate that the channel must be enabled
  - Enhanced descriptions for INT_EN register

Changed in 2.11a version of DW_ahb_dmac

- RTL changes:
  - FIFO_EMPTY register bit now resets to 1 to indicate that the FIFO is empty upon reset
  - Spirit XML generated now includes address space usage tags
  - Spirit XML generated no longer includes undefined register fields
  - Spirit XML generated no longer includes fields for unconfigured channels
  - Full support for defined length bursts (INCR4, INCR8, INCR16 and SINGLE) added and enabled with the DMAH_INCR_BURSTS parameter in coreConsultant
- Documentation and/or coreTools changes:
  - Changed CFGx.FIFO_EMPTY default to 0x1
  - Changed text to value of 1 for CFGx.FIFO_MODE

Changed in 2.10b version of DW_ahb_dmac

- RTL changes:
  - Packaging fixed to enable USE_FOUNDATION parameter for all configurations
- Documentation and/or coreTools changes:
  - Uses coreTools version 2007.06-1 or later

Changed in 2.10a version of DW_ahb_dmac

- Enhanced databook includes coreAssembler intent in Chapter 2.
- The coreAssembler or coreConsultant GUIs can now be used to select VIP/VMT versions.
- Register descriptions are now included in SPIRIT files.
- Clarification in databook regarding how the DW_ahb_dmac handles 1KB addressing boundary for AHB accesses.

Changed in 2.09a version of DW_ahb_dmac

- Fixed STAR 9000143503 regarding the DWF option working correctly with a DMAC source license.
- Fixed STAR 9000142830 regarding an incorrect warning when the user has a source license and selects the DWF option.
- Enhanced databook includes coreAssembler intent in Chapter 2

Changed in 2.08a version of DW_ahb_dmac

- Fixed STAR 9000117756, regarding the need for a new coreConsultant parameter, DMAH_STATIC_ENDIAN_SELECT, through which the endianness of the DW_ahb_dmac can be statically configured through coreConsultant or dynamically via pins on the I/O.
- While running coreConsultant simulations, under "Setup and Run Simulations," you can now choose the versions of the VIP models that you want to use in the testbench for VMT and AMBA.

Changed in 2.07a version of DW_ahb_dmac

- Fixed STAR 9000081528, regarding DW_ahb_dmac not responding to single requests under certain conditions.

The following changes occurred in the 2.06a version of DW_ahb_dmac:

- A new flow tutorial based on DesignWare Connect now comprises Chapter 2, "Building and Verifying a Component or Subsystem" of the *DesignWare DW_ahb_dmac Databook*.
- The DW_ahb_dmac can now be used in the coreTools 5.*x* environment.
- The DW_ahb_dmac now supports the DC-FPGA environment.
- The size of the DesignWare Synthesizable Components image has been reduced to about 60 MB by removing the DesignWare Memory Model TSP and the QuickStart examples designs; these are now available through separate downloads. For more information, refer to the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide*.
- The DesignWare Synthesizable Components image is now self-extracting.

Changed in 2.04a version of DW_ahb_dmac

- Source code for this component is available on a per-project basis as a DesignWare Core. Please contact your local sales office for the details. For source licensing information, refer to "Licenses" in the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide*.

Changed in 2.21a version of DW_ahb_dmac

- AMBA Compliance Tool certification and recertification
- DesignWare Connect – Enables you to construct, modify, and simulate any single- or multi-layer system in about an hour.
- The Verilog-XL simulator is not supported.
- The HP-UX platform is not supported.
- VHDL simulation is not supported.

Changed in 2.01a version of DW_ahb_dmac

- Area reduction and improved timing
- Added two configuration parameters:
  - Option to hardcode type of multi-block transfer (configuration parameter DMAH_CHx_MULTI_BLK_TYPE)
- Option to disable the writeback of the control register at the end of every block transfer (configuration parameter DMAH_CHx_CTRL_WB_EN)

Note

To get the exact same functionality as the previous release of DW_ahb_dmac, the new configuration parameters should be set to the following values:

- DMAH_CHx_MULTI_BLK_TYPE = NO_HARDCODE (0)
- DMAH_CHx_CTRL_WB_EN = True (1)

For a list of all the features of DW_ahb_dmac, refer to the "Features" section of the *DesignWare DW_ahb_dmac Databook*.

1.4.2.2 DW_ahb_dmac Releases

Table 1-2 lists the version information for the DW_ahb_dmac component, the releases in which they were included, and the corresponding DMA_COMP_VERSION register values.

Table 1-2 DesignWare for AMBA 2/DW_ahb_dmac Releases

DesignWare Release for AMBA 2	DW_ahb_dmac Version	DMA_COMP_VERSION value	Databook Date
2020.12a	2.23a	32_32_33_2A	December 2020
2018.07a	2.22a	32_32_32_2A	July 2018
2016.10a	2.21a	32_32_31_2A	October 2016
2015.06a	2.20a	32_32_30_2A	June 2015

DesignWare Release for AMBA 2	DW_ahb_dmac Version	DMA_COMP_VERSION value	Databook Date
2014.06a	2.19a	32_31_39_2A	June 2014
2013.05a	2.18b	32_31_38_2A	May 2013
2012.03a	2.17d	32_31_37_2A	March 2012
2011.11a	2.17c	32_31_37_2A	November 2011
2011.10a	2.17b	32_31_37_2A	October 2011
2011.04a	2.17a	32_31_37_2A	April 2011
2010.12a	2.16a	32_31_36_2A	December 2010
2010.09a	2.15a	32_31_35_2A	September 2010
2008.10a	2.14a	32_31_34_2A	October 2008
2008.09a	2.13a	32_31_33_2A	September 2008
2008.06a	2.12a	32_31_32_2A	June 2008
2008.04a	2.11a	32_31_31_2A	April 2008
2007.06a	2.10b	32_31_30_2A	June 2007
2007.04a	2.10a	32_31_30_2A	April 2007
2005.04a	2.09a	32_30_39_2A	November 2006
2005.04a	2.08a	32_30_38_2A	September 2006
2005.04a	2.07a	32_30_37_2A	December 2005
2005.04a	2.06a	32_30_36_2A	April 2005
2004.11	2.04a	32_30_34_2A	November, 2004
2004.06	2.03a	32_30_33_2A	July 27, 2004
2003.10	2.02a	32_30_32_2A	March 8, 2004
2003.10	2.01a	32_30_31_2A	December 16, 2003
2003.10	2.00b	32_30_30_2A	October 22, 2003

1.4.2.3 DW_ahb_dmac Known Problems and Workarounds

The following are the known problem(s) in this release of the DW_ahb_dmac:

- In the coreAssembler sub-system that involves DW_ahb_dmac, if the user choses the “Testbench Strategy and Language” as “UVM RAL Subsytem”, then the simulation fails.

1.4.3 DW_ahb_eh2h

The following sections list the new features and changes, and the fixed problems and enhancements, for the DW_ahb_eh2h component. For DW_ahb_eh2h-specific STARs, refer to:

https://www.synopsys.com/dw/star.php?c=DW_ahb_eh2h

For detailed features description see the *DW_ahb_eh2h databook*.

For information on known issues, refer to "DW_ahb_eh2h Known Problems and Workarounds" on page 38.

1.4.3.1 DW_ahb_eh2h New Features and Changes

This section describes what was new or changed during the various versions of the DW_ahb_eh2h:

Changed in 1.12a version of DW_ahb_eh2h

- RTL Changes:
  - RTL compliance to SpyGlass Q-2020.03-SP1 and GuideWare 2020.03
  - Enhancement:
    - STAR 9001245185: AHB5 protocol support as per the specification AMBA 5 AHB Protocol Specification AHB5, AHB-Lite
    - STAR 9001549439: The HRESP signal is updated to reflect as 1-bit when IP is used in AHB-Lite sub-system, as per AMBA 3 AHB-Lite Protocol Specification 1.0. New configuration parameters are added which determine the width of the HRESP signal.
- Documentation changes:
  - Refer to the Revision History chapter of the DW_ahb_eh2h databook
- Packaging changes:
  - STAR 3115176: Updated sWork::evalInComponent to align with coreTools version Q-2020.03-SP4-2
  - Minor packaging updates

Changed in 1.11a version of DW_ahb_eh2h

- RTL Changes:
  - RTL compliance to SpyGlass 2017.12-SP1 and GuideWare 2017.12
  - Fixed Defects:
    - STAR 9000444978: DW_ahb_eh2h IP is converting SINGLE or FIXED burst to undefined INCR burst with proper length, assuming a grant is lost during IDLE period on the Master side. The behavior is updated to avoid converting the transfers during normal scenarios.
  - Enhancement:
    - STAR 9001307186: Support to add MID sideband signals to transmit user specific information.
- Documentation and/or coreTools changes:
  - Version update

- Updated Synthesis results in the Integration Considerations chapter of the databook
- Published the first version of DesignWare Synthesizable Components for AMBA 2 User Guide
- Removed Chapter 2 "Building and Verifying a Component or Subsystem" from the databook and added the content in the newly created user guide
- Signals, Parameters, Registers and Internal parameters chapter auto-extracted with change bars from the RTL
- Uses coreTools version N-2017.12-SP2

- Packaging changes:
  - Minor packaging updates
- Removed support for NC Verilog Simulator and MTI Simulator
- Discontinued Support:
  - RAM synchronization parameter EH2H_RAM_SYNC has been deprecated as components have internal FIFO controllers to take care of clock domain crossing between the two domains. Hence, the RAM synchronization is not required.

Changed in 1.10a version of DW_ahb_eh2h

- RTL Changes:
  - Lint Cleanup
- Documentation and/or coreTools changes:
  - Version update
  - Parameter Descriptions and Register Descriptions auto-extracted from the RTL
  - Removed references to Leda
  - Uses coreTools version 2016.09

Changed in 1.09a version of DW_ahb_eh2h

- RTL Changes:
  - Lint and CDC Cleanup
  - Fixed:
    - DW_ahb_eh2h does not complete split response after read to register space
- Documentation and/or coreTools changes:
  - Version update
  - Signal Descriptions chapter auto-extracted from the RTL
  - Uses coreTools version 2014.12-SP1-1
- Packaging changes:
  - Minor packaging enhancements
  - Memory Map updates for defining access type to reserved fields

Changed in 1.08a version of DW_ahb_eh2h

- RTL changes:
  - Lint cleanup
- Documentation and/or coreTools changes:
  - Version update
  - Uses coreTools version 2013.03-SP1-2
  - Added the “Performance” section in “Integration Considerations” chapter
- Packaging changes:
  - Minor packing enhancements
  - IP-XACT enhancement for enumeration and display names

Changed in 1.07f version of DW_ahb_eh2h

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Updated the databook template
  - Uses coreTools version 2012.06-SP2
- Packaging changes:
  - Corrected file prefixing in the encrypted mode

Changed in 1.07e version of DW_ahb_eh2h

- RTL changes:
  - Updated copyright headers
- Documentation and/or coreTools changes:
  - Corrected offset values for EWS and MEWS registers in RAL description

Changed in 1.07d version of DW_ahb_eh2h

- RTL changes:
  - Corrected inconsistencies in RAL files
- Documentation and/or coreTools changes:
  - None

Changed in 1.07c version of DW_ahb_eh2h

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.09-SP2

Changed in 1.07b version of DW_ahb_eh2h

- RTL changes:
  - Updated and corrected copyright headers in RTL
  - Packaging changed such that SplitCapable default value is no longer changed on coreTools slave interface definition

Changed in 1.07a version of DW_ahb_eh2h

- RTL changes:
  - Corrected RAM_SYNC synchronization error
  - Fixed packaging to allow coreTools to correctly detect split-capable setting of attached slave
  - Enhanced packaging to allow connection of multiple hsel outputs to be connected in coreAssembler
  - Enhanced packaging to produce correct auto-connection on instantiation of DW_ahb_eh2h instance
- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.03 or later
  - Added material in databook about limitations with respect to defined length burst support
  - Corrected names of include files and vcs command used for simulation in databook
  - Corrected syntax for undef directive

Changed in 1.06a version of DW_ahb_eh2h

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Updated “Clock Adaptation” section in databook
  - Uses coreTools version 2008.06-SP2-2

Changed in 1.05b version of DW_ahb_eh2h

- RTL changes:
  - None

- Documentation and/or coreTools changes:
  - Uses coreTools version 2007.06-SP4
  - More information added DW_ahb_eh2h behavior when master interface loses bus ownership
  - Added more detail about transfer changing from a SINGLE to an INCR

Changed in 1.05a version of DW_ahb_eh2h

- RTL changes:
  - Corrected generation of minterrupt and EWS register setting
  - Corrected bug that causes local register accesses not to be executed, resulting in the bridge being deadlocked
  - Enhancement to correct an issue where poor buffer read selector implementations break the clock domain crossing scheme
- Documentation changes:
  - Clarified material regarding:
    - Both sides of DW_ahb_eh2h should be reset before any system traffic reaches it
    - A burst is rebuilt after DW_ahb_eh2h loses ownership of AHB bus
    - Upsizing wider secondary data width with regard to primary data width is not supported

Changed in 1.04b version of DW_ahb_eh2h

- RTL changes:
  - Corrected packaging issue for NumSelectSlots parameter on the slave interface
- Documentation and/or coreTools changes:
  - Uses coreTools version 2007.06-1 or later

Changed in 1.04a version of DW_ahb_eh2h

- Enhanced databook includes coreAssembler intent in Chapter 2.
- The coreAssembler or coreConsultant GUIs can now be used to select VIP/VMT versions.
- Register descriptions are now included in SPIRIT files.

Changed in 1.03a version of DW_ahb_eh2h

- SystemVerilog support was added, per STAR 9000126878.
- The USE_FOUNDATION parameter has been removed, per STAR 9000059928.
- While running coreConsultant simulations, under “Setup and Run Simulations,” you can now choose the versions of the VIP models that you want to use in the testbench for VMT and AMBA.
- Enhanced databook includes coreAssembler intent in Chapter 2.

Changed in 1.02a version of DW_ahb_eh2h

- A new flow tutorial based on DesignWare Connect now comprises Chapter 2, "Building and Verifying a Component or Subsystem" in the *DesignWare DW_ahb_eh2h Databook*.
- The DW_ahb_eh2h can now be used in the coreTools 5.*x* environment.
- The DW_ahb_eh2h now supports the DC-FPGA environment.
- The size of the DesignWare Synthesizable Components image has been reduced to about 60 MB by removing the DesignWare Memory Model TSP and the QuickStart examples designs; these are now available through separate downloads. For more information, refer to the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide*.
- The DesignWare Synthesizable Components image is now self-extracting.

Changed in 1.01a version of DW_ahb_eh2h

- Source code for this component is available on a per-project basis as a DesignWare Core. Please contact your local sales office for the details. For source licensing information, refer to "Licenses" in the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide*.

Changed in 1.00a version of DW_ahb_eh2h

- DesignWare Connect – Enables you to construct, modify, and simulate any single- or multi-layer systems in about an hour.
- The Verilog-XL simulator is not supported.
- The HP-UX platform is not supported.
- VHDL simulation is not supported.

1.4.3.2 DW_ahb_eh2h Releases

Table 1-3 lists the latest versions of the DW_ahb_eh2h component, the releases in which they were included, and the corresponding VERSION_ID register values.

Table 1-3 DesignWare for AMBA 2/DW_ahb_eh2h Releases

DesignWare Release for AMBA 2	DW_ahb_eh2h Version	VERSION_ID value	Databook Date
2020.12a	1.12a	31_31_32_2A	December 2020
2018.07a	1.11a	31_31_31_2A	July 2018
2016.10a	1.10a	31_31_30_2A	October 2016
2015.06a	1.09a	31_30_39_2A	June 2015
2014.06a	1.08a	31_30_38_2A	June 2014
2013.05a	1.07f	31_30_37_2A	May 2013
2012.03a	1.07e	31_30_37_2A	March 2012

DesignWare Release for AMBA 2	DW_ahb_eh2h Version	VERSION_ID value	Databook Date
2011.11a	1.07d	31_30_37_2A	November 2011
2011.10a	1.07c	31_30_37_2A	October 2011
2010.10a	1.07b	31_30_37_2A	October 2010
2010.09a	1.07a	31_30_37_2A	September 2010
2009.06a	1.06a	31_30_36_2A	June 2009
2008.10a	1.06a	31_30_36_2A	October 2008
2008.06a	1.05b	31_30_35_2A	June 2008
2007.11a	1.05a	31_30_35_2A	November 2007
2007.06a	1.04b	31_30_34_2A	June 2007
2007.04a	1.04a	31_30_34_2A	April 2007
2005.04a	1.03a	31_30_33_2A	September 2006
2005.04a	1.02a	31_30_32_2A	April 2005
2004.11	1.01a	31_30_31_2A	November 2004
2004.06	1.00a	31_30_30_2A	June 21, 2004
N/A	1.00a	31_30_30_2A	November 26, 2003

1.4.3.3 DW_ahb_eh2h Known Problems and Workarounds

There are no known problems in this release of DW_ahb_eh2h.

1.4.4 DW_ahb_h2h

The following sections list the new features and changes, and the fixed problems and enhancements, for the DW_ahb_h2h component. For DW_ahb_h2h-specific STARs, refer to:

https://www.synopsys.com/dw/star.php?c=DW_ahb_h2h

For detailed features description, see the *DW_ahb_h2h databook*.

For information on known issues, refer to "DW_ahb_h2h Known Problems and Workarounds" on page 43.

1.4.4.1 DW_ahb_h2h New Features and Changes

This section describes what was new or changed during the various versions of the DW_ahb_h2h:

Changed in 1.11a version of DW_ahb_h2h

- RTL Changes:

  - RTL compliance to SpyGlass Q-2020.03-SP1 and GuideWare 2020.03
  - Discontinued support for Synchronization depth parameter (H2H_NUM_SYNC_FLOPS) value corresponding to "1: Two stage synchronization with 1st stage negative-edge capturing and 2nd stage positive-edge capturing" (as cautioned in the previous GA).
  - Enhancement:
    - STAR 9001245185: AHB5 protocol support as per the specification AMBA 5 AHB Protocol Specification AHB5, AHB-Lite
    - STAR 9001549439: The HRESP signal is updated to reflect as 1-bit when IP is used in AHB-Lite sub-system, as per AMBA 3 AHB-Lite Protocol Specification 1.0. New configuration parameters are added which determine the width of the HRESP signal.
- Documentation changes:
  - Refer to the Revision History chapter of the DW_ahb_h2h databook
- Packaging changes:
  - STAR 3115176: Updated sWork::evalInComponent to align with coreTools version Q-2020.03-SP4-2
  - Minor packaging updates

Changed in 1.10a version of DW_ahb_h2h

- RTL Changes:
  - RTL compliance to SpyGlass 2017.12-SP1 and GuideWare 2017.12
- Enhancement:
  - STAR 9001307186: Support to add MID sideband signals to transmit user specific information.
  - STAR 9001189792: Added support for configurable synchronization depth through coreConsultant parameter H2H_NUM_SYNC_FLOPS.
- Documentation and/or coreTools changes:
  - Version update
  - Updated Synthesis results in the Integration Considerations chapter of the databook
  - Published the first version of DesignWare Synthesizable Components for AMBA 2 User Guide
  - Removed Chapter 2 "Building and Verifying a Component or Subsystem" from the databook and added the content in the newly created user guide
  - Signals, Parameters, Registers and Internal parameters chapter auto-extracted with change bars from the RTL
  - Uses coreTools version N-2017.12-SP2
- Packaging changes:
  - Minor packaging updates
- Removed support for NC Verilog Simulator and MTI Simulator

Changed in 1.09a version of DW_ahb_h2h

- RTL Changes:
  - Lint and CDC cleanup
- Documentation and/or coreTools changes:
  - Version update
  - Parameter Descriptions chapter auto-extracted from the RTL
  - Removed references to Leda
  - Uses coreTools version 2016.09

Changed in 1.08a version of DW_ahb_h2h

- RTL Changes:
  - Lint and CDC Cleanup
- Documentation and/or coreTools changes:
  - Version update
  - Signal Descriptions chapter auto-extracted from the RTL
  - Uses coreTools version 2014.12-SP1-1
- Packaging changes:
  - Minor packaging enhancements

Changed in 1.07a version of DW_ahb_h2h

- RTL changes:
  - Lint cleanup
  - Updated synchronization structures using bcm21 synchronizers
- Documentation and/or coreTools changes:
  - Version update
  - Uses coreTools version 2013.03-SP1-2
  - Added the “Performance” section in “Integration Considerations” chapter
- Packaging changes:
  - Minor packing enhancements

Changed in 1.06d version of DW_ahb_h2h

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Updated the databook template

    - Uses coreTools version 2012.06-SP2
- Packaging changes:
    - Corrected file prefixing in the encrypted mode

Changed in 1.06c version of DW_ahb_h2h

- RTL changes:
    - None
- Documentation and/or coreTools changes:
    - Uses coreTools version 2010.09-SP2

Changed in 1.06b version of DW_ahb_h2h

- RTL changes:
    - Packaging changed such that SplitCapable default value is no longer changed on coreTools slave interface definition

Changed in 1.06a version of DW_ahb_h2h

- RTL changes:
    - Fixed packaging to allow coreTools to correctly detect split-capable setting of attached slave
- Documentation and/or coreTools changes:
    - Uses coreTools version 2010.03 or later
    - Corrected names of include files and vcs command used for simulation in databook
    - Corrected syntax for undef directive

Changed in 1.05a version of DW_ahb_h2h

- RTL changes:
    - None
- Documentation and/or coreTools changes:
    - Updated description of shsplit connections
    - Uses coreTools version 2008.06-SP2-2

Changed in 1.04c version of DW_ahb_h2h

- RTL changes:
    - None
- Documentation and/or coreTools changes:
    - Uses coreTools version 2007.06-SP4

Changed in 1.04b version of DW_ahb_h2h

- RTL changes:
  - Corrected packaging issue for NumSelectSlots parameter on the slave interface
- Documentation and/or coreTools changes:
  - Uses coreTools version 2007.06-1 or later

Changed in 1.04a version of DW_ahb_h2h

- Enhanced databook includes coreAssembler intent in Chapter 2.
- The coreAssembler or coreConsultant GUIs can now be used to select VIP/VMT versions.
- Register descriptions are now included in SPIRIT files.

Changed in 1.03a version of DW_ahb_h2h

- A new flow tutorial based on DesignWare Connect now comprises Chapter 2, "Building and Verifying a Component or Subsystem" of the *DesignWare DW_ahb_h2h Databook*.
- The DW_ahb_h2h can now be used in the coreTools 5.*x* environment.
- The DW_ahb_h2h now supports the DC-FPGA environment.
- The size of the DesignWare Synthesizable Components image has been reduced to about 60 MB by removing the DesignWare Memory Model TSP and the QuickStart examples designs; these are now available through separate downloads. For more information, refer to the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide*.
- The DesignWare Synthesizable Components image is now self-extracting.
- Enhanced databook includes coreAssembler intent in Chapter 2

Changed in 1.02a version of DW_ahb_h2h

- Source code for this component is available on a per-project basis as a DesignWare Core. Please contact your local sales office for the details. For source licensing information, refer to "Licenses" in the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide*.

Changed in 1.01c version of DW_ahb_h2h

- DesignWare Connect – Enables you to construct, modify, and simulate any single- or multi-layer system in about an hour.
- The Verilog-XL simulator is not supported.
- The HP-UX platform is not supported.
- VHDL simulation is not supported.

For a list of the features for the DW_ahb_h2h, refer to the "Features" section in the *DesignWare DW_ahb_h2h Databook*.

1.4.4.2 DW_ahb_h2h Releases

Table 1-4 lists the latest versions of the DW_ahb_h2h component, the releases in which they were included, and the corresponding VERSION_ID register values.

Table 1-4 DesignWare for AMBA 2/DW_ahb_h2h Releases

DesignWare Release for AMBA 2	DW_ahb_h2h Version	VERSION_ID value	Databook Date
2020.12a	1.11a	31_31_31_2A	December 2020
2018.07a	1.10a	31_31_30_2A	July 2018
2016.10a	1.09a	31_30_39_2A	October 2016
2015.06a	1.08a	31_30_38_2A	June 2015
2014.06a	1.07a	31_30_37_2A	June 2014
2013.05a	1.06d	31_30_36_2A	May 2013
2011.10a	1.06c	31_30_36_2A	October 2011
2010.10a	1.06b	31_30_36_2A	October 2010
2010.09a	1.06a	31_30_36_2A	September 2010
2009.06a	1.05a	31_30_35_2A	June 2009
2008.10a	1.05a	31_30_35_2A	October 2008
2008.06a	1.04c	31_30_34_2A	June 2008
2007.06a	1.04b	31_30_34_2A	June 2007
2007.04a	1.04a	31_30_34_2A	April 2007
2005.04a	1.03a	31_30_33_2A	April 2005
2004.11	1.02a	31_30_32_2A	November, 2004
2004.06	1.01c	31_30_31_2A	July 28, 2004
2003.10	1.00b	31_30_30_2A	October 22, 2003
2003.02	1.00a	31_30_30_41	March 26, 2003

1.4.4.3 DW_ahb_h2h Known Problems and Workarounds

There are no known issues in this release of the DW_ahb_h2h.

1.4.5 DW_ahb_icm

The following sections list the new features and changes, and the fixed problems and enhancements, for the DW_ahb_icm component. For DW_ahb_icm-specific STARs, refer to:

https://www.synopsys.com/dw/star.php?c=DW_ahb_icm

For detailed features description, see the *DW_ahb_icm databook*.

For information on known issues, refer to "DW_ahb_icm Known Problems and Workarounds" on page 49.

1.4.5.1 DW_ahb_icm New Features and Changes

This section describes what was new or changed during the various versions of the DW_ahb_icm:

Changed in 1.18a version of DW_ahb_icm

- RTL Changes:
  - RTL compliance to SpyGlass Q-2020.03-SP1 and GuideWare 2020.03
  - Enhancement:
    - STAR 9001245185: AHB5 protocol support as per the specification AMBA 5 AHB Protocol Specification AHB5, AHB-Lite
    - STAR 9001549439: The HRESP signal is updated to reflect as 1-bit when IP is used in AHB-Lite sub-system, as per AMBA 3 AHB-Lite Protocol Specification 1.0. New configuration parameters are added which determine the width of the HRESP signal.
- Documentation changes:
  - Refer to the Revision History chapter of the DW_ahb_icm databook
- Packaging changes:
  - STAR 3115176: Updated sWork::evalInComponent to align with coreTools version Q-2020.03-SP4-2
  - Minor packaging updates

Changed in 1.17a version of DW_ahb_icm

- RTL Changes:
  - RTL compliance to SpyGlass 2017.12-SP1 and GuideWare 2017.12
  - Fixed Defects:
    - STAR 9001268396: For the configuration with AHB_MASK_PRIORITY=1 and ICM_HAS_XPRIORITY=1; AHB data loss is observed in Error, Retry, or Split transfer events where non -OKAY response is received.
- Documentation and/or coreTools changes:
  - Version update
  - Updated Synthesis results in the Integration Considerations chapter of the databook
  - Published the first version of DesignWare Synthesizable Components for AMBA 2 User Guide

  - Removed Chapter 2 "Building and Verifying a Component or Subsystem" from the databook and added the content in the newly created user guide
  - Signals, Parameters, Registers and Internal parameters chapter auto-extracted with change bars from the RTL
  - Uses coreTools version N-2017.12-SP2
- Packaging changes:
  - Minor packaging updates
- Removed support for NC Verilog Simulator and MTI Simulator

Changed in 1.16a version of DW_ahb_icm

- RTL Changes:
  - Lint Cleanup
  - Enhancement:
    - Support to increase the Number of Master layers from 8 to 16
- Documentation and/or coreTools changes:
  - Version update
  - Parameter Descriptions chapter auto-extracted from the RTL
  - Removed references to Leda
  - Updated the Features section and the Integration Considerations chapter
  - Updated Parameter Descriptions and Signals chapters
  - Uses coreTools version 2016.09

Changed in 1.15a version of DW_ahb_icm

- RTL Changes:
  - Lint Cleanup
  - Updated behavior for HADDR and HTRANS at ICM output when hready is low
- Documentation and/or coreTools changes:
  - Version update
  - Signal Descriptions chapter auto-extracted from the RTL
  - Uses coreTools version 2014.12-SP1-1
- Packaging changes:
  - Minor packaging enhancements

Changed in 1.14a version of DW_ahb_icm

- RTL changes:
  - Lint cleanup

- Documentation and/or coreTools changes:
  - Version update
  - Uses coreTools version 2013.03-SP1-2
  - Added the “Performance” section in “Integration Considerations” chapter
  - Corrected the External Input/Output Delay values in Signals chapter
- Packaging changes:
  - Minor packing enhancements

Changed in 1.13d version of DW_ahb_icm

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Updated the databook template
  - Uses coreTools version 2012.06-SP2
- Packaging changes:
  - Corrected file prefixing in the encrypted mode

Changed in 1.13c version of DW_ahb_icm

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Updated description of icm_priority signal
  - Added a dynamic-priority arbitration subsection

Changed in 1.13b version of DW_ahb_icm

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.09-SP2

Changed in 1.13a version of DW_ahb_icm

- RTL changes:
  - None

- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.03 or later
  - Corrected names of include files and vcs command used for simulation in databook
  - Corrected syntax for undef directive

Changed in 1.12a version of DW_ahb_icm

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2008.06-SP2-2

Changed in 1.11a version of DW_ahb_icm

- RTL changes:
  - Reference to support for up to 4 AHB layers, corrected to say 8 AHB layers
  - 64-bit HADDR support added
- Documentation and/or coreTools changes:
  - Uses coreTools version 2007.06-SP4

Changed in 1.10b version of DW_ahb_icm

The following was new or changed in the 1.10b version of the DW_ahb_icm:

- RTL changes:
  - Packaging fixed to enable USE_FOUNDATION parameter for all configurations
- Documentation and/or coreTools changes:
  - Uses coreTools version 2007.06-1 or later

Changed in 1.10a version of DW_ahb_icm

- Enhanced databook includes coreAssembler intent in Chapter 2.
- The coreAssembler or coreConsultant GUIs can now be used to select VIP/VMT versions.
- Register descriptions are now included in SPIRIT files.

Changed in 1.09a version of DW_ahb_icm

- A new flow tutorial based on DesignWare Connect now comprises Chapter 2, “Building and Verifying a Component or Subsystem” of the *DesignWare DW_ahb_icm Databook*.
- The DW_ahb_icm can now be used in the coreTools 5.*x* environment.
- The DW_ahb_icm now supports the DC-FPGA environment.
- Enhanced databook includes coreAssembler intent in Chapter 2.

- The size of the DesignWare Synthesizable Components image has been reduced to about 60 MB by removing the DesignWare Memory Model TSP and the QuickStart examples designs; these are now available through separate downloads. For more information, refer to the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide*.
- The DesignWare Synthesizable Components image is now self-extracting.

Changed in 1.07a/1.06a version of DW_ahb_icm

- Source code for this component is available on a per-project basis as a DesignWare Core. Please contact your local sales office for the details. For source licensing information, refer to "Licenses" in the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide*.

Changed in 1.05a version of DW_ahb_icm

- Increased the number of layers to a maximum of 8.
- DesignWare Connect – Enables you to construct, modify, and simulate any single- or multi-layer system in about an hour.
- The Verilog-XL simulator is not supported.
- The HP-UX platform is not supported.
- VHDL simulation is not supported.

Changed in 1.04a version of DW_ahb_icm

- Configurable external priority control for AHB layers.

1.4.5.2 DW_ahb_icm Releases

Table 1-5 lists the latest versions of the DW_ahb_icm component, the releases in which they were included, and the corresponding COMP_ID register values.

Table 1-5 DesignWare for AMBA 2/DW_ahb_icm Releases

DesignWare Release for AMBA 2	DW_ahb_icm Version	COMP_ID	Databook Date
2020.12a	1.18a	31_31_38_2A	December 2020
2018.07a	1.17a	31_31_37_2A	July 2018
2016.10a	1.16a	31_31_36_2A	October 2016
2015.06a	1.15a	31_31_35_2A	June 2015

DesignWare Release for AMBA 2	DW_ahb_icm Version	COMP_ID	Databook Date
2014.06a	1.14a	31_31_34_2A	June 2014
2013.05a	1.13d	31_31_33_2A	May 2013
2012.03a	1.13c	31_31_33_2A	March 2012
2011.10a	1.13b	31_31_33_2A	October 2011
2010.09a	1.13a	31_31_33_2A	September 2010
2009.06a	1.12a	31_31_32_2A	June 2009
2008.10a	1.12a	31_31_32_2A	October 2008
2008.06a	1.11a	31_31_31_2A	June 2008
2007.06a	1.10b	31_31_30_2A	June 2007
2007.04a	1.10a	31_31_30_2A	April 2007
2005.04a	1.09a	31_30_39_2A	April 2005
2004.11b	1.07a	31_30_37_2A	January, 2005
2004.11	1.06a	31_30_36_2A	November, 2004
2004.06	1.05a	31_30_35_2A	June 21, 2004
2003.10	1.04a	31_30_34_2A	October 20, 2003
2003.02	1.03b	31_30_33_42	March 26, 2003
2002.08-SP1-4	1.03a	—	January 22, 2003
2002.08-SP1-2	1.02a	—	January 22, 2003
2002.08-SP1	1.01b	—	September 25, 2002
2002.08	1.0a	—	August 20, 2002

1.4.5.3 DW_ahb_icm Known Problems and Workarounds

There are no known issues in this release of the DW_ahb_icm.

1.4.6 DW_ahb_ictl

The following sections list the new features and changes, and the fixed problems and enhancements, for the DW_ahb_ictl component. For DW_ahb_ictl-specific STARs, refer to:

https://www.synopsys.com/dw/star.php?c=DW_ahb_ictl

For detailed features description, see the *DW_ahb_ictl databook*.

For information on known issues, refer to "DW_ahb_ictl Known Problems and Workarounds" on page 56.

1.4.6.1 DW_ahb_ictl New Features and Changes

This section describes what was new or changed during the various versions of the DW_ahb_ictl:

Changed in 2.15a version of DW_ahb_ictl

- RTL Changes:
  - Design compliance to SpyGlass Q-2020.03-SP1 and GuideWare 2020.03
  - Enhancement
    - STAR 9001549439: The HRESP signal is updated to reflect as 1-bit when IP is used in AHB-Lite sub-system, as per AMBA 3 AHB-Lite Protocol Specification 1.0. New configuration parameters are added which determine the width of the HRESP signal.
- Documentation changes:
  - Refer to the Revision History chapter of the DW_ahb_ictl databook.
- Packaging changes:
  - STAR 3115176: Updated sWork::evalInComponent to align with coreTools version Q-2020.03-SP4-2
  - Minor packaging updates

Changed in 2.14a version of DW_ahb_ictl

- RTL Changes:
  - RTL compliance to SpyGlass 2017.12-SP1 and GuideWare 2017.12
  - Enhancement:
    - Added support for configurable synchronization depth through coreConsultant parameter ICT_ADD_VECTOR_PORT_SYNC_DEPTH
- Documentation and/or coreTools changes:
  - Version update
  - Updated Synthesis results in the Integration Considerations chapter of the databook
  - Published the first version of DesignWare Synthesizable Components for AMBA 2 User Guide
  - Removed Chapter 2 "Building and Verifying a Component or Subsystem" from the databook and added the content in the newly created user guide

  - Signals, Parameters, Registers and Internal parameters chapter auto-extracted with change bars from the RTL
  - Uses coreTools version N-2017.12-SP2
- Packaging changes:
  - Minor packaging updates
- Removed support for NC Verilog Simulator and MTI Simulator

Changed in 2.13a version of DW_ahb_ictl

- RTL Changes:
  - Lint and CDC Cleanup
- Documentation and/or coreTool changes:
  - Version update
  - Parameter Descriptions and Register Descriptions chapters auto-extracted from the RTL
  - Removed references to Leda
  - Uses coreTools version 2016.09

Changed in 2.12a version of DW_ahb_ictl

- RTL Changes:
  - Lint and CDC Cleanup
- Documentation and/or coreTools changes:
  - Version update
  - Signal Descriptions chapter auto-extracted from the RTL
  - Uses coreTools version 2014.12-SP1-1
- Packaging changes:
  - Minor packaging enhancements
  - Memory Map updates for defining access type to reserved fields

Changed in 2.11a version of DW_ahb_ictl

- RTL changes:
  - Lint cleanup
- Documentation and/or coreTools changes:
  - Version update
  - Added the “Performance” section in “Integration Considerations” chapter.
  - Uses coreTools version 2013.03-SP1-2
  - Corrected the Default Input/Output Delay values in Signals chapter

- Packaging changes:
  - Minor packing enhancements
  - IP-XACT enhancement for enumeration and display names
  - Corrected data description inconsistencies in RAL files
  - Fixed Defects:
    - If DW_ahb_ictl RTL is analyzed and elaborated, Design Compiler version G-2012.06-SP1 crashes while executing the compile_ultra command due to multiplex mapping error. Refer to Design Compiler STAR 9000594113.

Changed in 2.10a version of DW_ahb_ictl

- RTL changes:
  - Removed an unused signal, irq_vector_bus
- Documentation and/or coreTools changes:
  - Updated the databook template
  - Uses coreTools version 2012.06-SP2
- Packaging changes:
  - Corrected file prefixing in the encrypted mode

Changed in 2.09b version of DW_ahb_ictl

- RTL changes:
  - Updated copyright headers
- Documentation and/or coreTools changes:
  - None

Changed in 2.08b version of DW_ahb_ictl

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.09-SP2

Changed in 2.08a version of DW_ahb_ictl

- RTL changes:
  - Corrected AHB slave interface so that DW_ahb_ictl can accept transfers received in the second cycle of a two-cycle response
  - Corrected problem where wait cycle is inserted for write/read transfer to adjacent locations
  - Removed wrong input delay set on hclk port

- Documentation and/or coreTools changes:
  - Clarified Note in "Register Memory Map" section.
  - Corrected range for IRQ_INTEN_L register when generating RAL file

Changed in 2.07a version of DW_ahb_ictl

- RTL changes:
  - Fixed AHB_ICTL, TB, false simulation ERROR due to uninitialized variable
- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.03 or later
  - Corrected names of include files and vcs command used for simulation in databook
  - Corrected syntax for undef directive
  - Fixed AHB_ICTL, TB, simulation failure due to drive conflict in testbench

Changed in 2.06a version of DW_ahb_ictl

- RTL changes:
  - Testbench updated to removed Xs that cause encrypted simulation fails
- Documentation and/or coreTools changes:
  - Uses coreTools version 2008.06-SP2-2

Changed in 2.05c version of DW_ahb_ictl

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Incorrect chapters removed from databook
  - Uses coreTools version 2007.06-SP4

Changed in 2.05b version of DW_ahb_ictl

- RTL changes:
  - Vector port feature added to the DW_ahb_ictl
- Documentation and/or coreTools changes:
  - Enhancement to the databook to support the new vector port feature

Changed in 2.04b version of DW_ahb_ictl

- RTL changes:
  - Packaging fixed to enable USE_FOUNDATION parameter for all configurations

- Documentation and/or coreTools changes:
  - Uses coreTools version 2007.06-1 or later

Changed in 2.04a version of DW_ahb_ictl

- Enhanced databook includes coreAssembler intent in Chapter 2.
- The coreAssembler or coreConsultant GUIs can now be used to select VIP/VMT versions.
- Register descriptions are now included in SPIRIT files.
- Register references from irq_pN_offset to irq_pr_N corrected in databook.

Changed in 2.03a version of DW_ahb_ictl

- A new flow tutorial based on DesignWare Connect now comprises Chapter 2, "Building and Verifying a Component or Subsystem" of the *DesignWare DW_ahb_ictl Databook*.
- The DW_ahb_ictl can now be used in the coreTools 5.*x* environment.
- Enhanced databook includes coreAssembler intent in Chapter 2.
- The size of the DesignWare Synthesizable Components image has been reduced to about 60 MB by removing the DesignWare Memory Model TSP and the QuickStart examples designs; these are now available through separate downloads. For more information, refer to the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide*.
- The DW_ahb_ictl now supports the DC-FPGA environment.
- The DesignWare Synthesizable Components image is now self-extracting.

Changed in 2.02a version of DW_ahb_ictl

- Source code for this component is available on a per-project basis as a DesignWare Core. Please contact your local sales office for the details. For source licensing information, refer to "Licenses" in the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide*.

Changed in 2.01b version of DW_ahb_ictl

- DesignWare Connect – Enables you to construct, modify, and simulate any single- or multi-layer system in about an hour.
- The Verilog-XL simulator is not supported.
- The HP-UX platform is not supported.
- VHDL simulation is not supported.

Changed in 2.01a version of DW_ahb_ictl

- AMBA Compliance Tool (ACT) certification – You can run ACT certification on DW_ahb_ictl provided you have the required license (DesignWare-ACT-VIP) and the data width of the AHB bus is 32, 64, or 128 bits.

- Option to add encoded parameters – By adding the encoded parameters, gives firmware an easy and quick way of identifying the DesignWare component within an I/O memory map. Some critical design-time options determine how a driver should interact with the peripheral. There is a minimal area overhead by including these parameters. When set, it allows a single driver to be developed for each component, which is self-configurable.
- Component Parameter registers (ICTL_COMP_PARAMS_n) were added to the memory map; these registers allow software to query the configuration of the device.

Changed in 2.00a version of DW_ahb_ictl

- It is now possible to configure the DW_ahb_ictl to allow the priority levels of the interrupt sources be changed by reprogramming.
- In the memory map, the name of the Version ID register, now known as the Component Version register, has changed from ICTL_VERSION_ID to AHB_ICTL_COMP_VERSION.

1.4.6.2 DW_ahb_ictl Releases

Table 1-6 lists the latest versions of the DW_ahb_ictl component, the releases in which they were included, and the corresponding AHB_ICTL_COMP_VERSION register values.

Table 1-6 DesignWare for AMBA 2/DW_ahb_ictl Releases

DesignWare Release for AMBA 2	DW_ahb_ictl Version	AHB_ICTL_ COMP_VERSION value	Databook Date
2020.12a	2.15a	32_31_35_2A	December 2020
2018.07a	2.14a	32_31_34_2A	July 2018
2016.10a	2.13a	32_31_33_2A	October 2016
2015.06a	2.12a	32_31_32_2A	June 2015
2014.06a	2.11a	32_31_31_2A	June 2014
2013.05a	2.10a	32_31_30_2A	May 2013
2012.03a	2.09b	32_30_39_2A	March 2012
2011.11a	2.09a	32_30_39_2A	November 2011
2011.10a	2.08b	32_30_38_2A	October 2011
2011.04a	2.08a	32_30_38_2A	April 2011
2010.09a	2.07a	32_30_37_2A	September 2010
2009.06a	2.06a	32_30_36_2A	June 2009
2008.10a	2.06a	32_30_36_2A	October 2008
2008.06a	2.05c	32_30_35_2A	June 2008
2008.02a	2.05b	32_30_35_2A	February 2008

DesignWare Release for AMBA 2	DW_ahb_ictl Version	AHB_ICTL_ COMP_VERSION value	Databook Date
2007.06a	2.04b	32_30_34_2A	June 2007
2007.04a	2.04a	32_30_34_2A	April 2007
2005.04a	2.03a	32_30_33_2A	April 2005
2004.11	2.02a	32_30_32_2A	November 2004
2004.06	2.01b	32_30_31_2A	June 21, 2004
2003.10	2.01a	32_30_31_2A	December 16, 2003
2003.10	2.00a	32_30_30_2A	October 20, 2003
2003.02	1.00a	31_30_30_41	March 26, 2003
NOTE: The DW_ahb_ictl component evolved from DW_amba_ictl version 1.02c			

1.4.6.3 DW_ahb_ictl Known Problems and Workarounds

There are no known problem(s) in this release of the DW_ahb_ictl.

1.4.7 DW_apb

The following sections list the new features and changes, and the fixed problems and enhancements, for the DW_apb component. For DW_apb-specific STARs, refer to:

https://www.synopsys.com/dw/star.php?c=DW_apb

For detailed feature description, see the *DW_apb databook*.

For information on known issues, refer to "DW_apb Known Problems and Workarounds" on page 63.

1.4.7.1 DW_apb New Features and Changes

This section describes what was new or changed during the various versions of the DW_apb:

Changed in 3.03a version of DW_apb

RTL Changes:

- RTL compliance to SpyGlass Q-2020.03-SP1 and GuideWare 2020.03
- Enhancement
  - STAR 9001245185: AHB5 protocol support as per the specification AMBA 5 AHB Protocol Specification AHB5, AHB-Lite
  - STAR 9001549439: The HRESP signal is updated to reflect as 1-bit when IP is used in AHB-Lite sub-system, as per AMBA 3 AHB-Lite Protocol Specification 1.0. New configuration parameters are added which determine the width of the HRESP signal.
- Fixed
  - STAR 3253386: Incorrect mapping of the HPROT signal to the PPROT signal definition when IP is configured for APB4 slaves and back-to-back transfers are enabled. Data access as per hprot[0] is translated to instruction access as per pprot[2]. This mapping is corrected by keeping the protection attributes intent while translating from AHB to APB.
  - STAR 3460347: Incorrect values generated on pstrb and pwdata signals when back-to-back transfers are enabled. RTL is updated so that correct values on these signals are generated from corresponding AHB signals.

- Documentation changes:
  - Refer to the Revision History chapter of the DW_apb databook.
- Packaging changes:
  - STAR 3115176: Updated sWork::evalInComponent to align with coreTools version Q-2020.03-SP4-2
  - Minor packaging updates

Changed in 3.02a version of DW_apb

- RTL Changes:
  - RTL compliance to SpyGlass 2017.12-SP1 and GuideWare 2017.12
  - Fixed Defects:

        - STAR 9001149849: In case of back to back transactions, the DW_apb does not latch on the correct write address for the second transaction when the second transaction is a write transaction; and this write transaction is not accepted by the DW_apb bridge because of the data phase being extended for the first transaction. Due to this problem, the write transaction happens on a wrong address, thus corrupting the data. The RTL is updated to address this issue.
- Documentation and/or coreTools changes:
    - Version update
    - Updated Synthesis results in the Integration Considerations chapter of the databook
    - Published the first version of DesignWare Synthesizable Components for AMBA 2 User Guide
    - Removed Chapter 2 "Building and Verifying a Component or Subsystem" from the databook and added the content in the newly created user guide
    - Signals, Parameters, Registers and Internal parameters chapter auto-extracted with change bars from the RTL
    - Uses coreTools version N-2017.12-SP2
- Packaging changes:
    - Minor packaging updates
- Removed support for NC Verilog Simulator and MTI Simulator

Changed in 3.01a version of DW_apb

- RTL Changes:
    - Lint Cleanup
    - Enhancement:
        - Performance improvement for APB3 back-to-back write transfers
    - Fixed:
        - APB4 interface parameter propagation issue in coreAssembler
        - Packaging issue when the Start address and the End address match with each other
- Documentation and/or coreTools changes:
    - Version update
    - Parameter Descriptions chapter auto-extracted from the RTL
    - Removed references to Leda
    - Added "Back-to-Back Transfer Support on an APB Interface" section
    - Uses coreTools version 2016.09

Changed in 3.00a version of DW_apb

- RTL Changes:
    - Lint Cleanup

    - Enhanced to support APB4
- Documentation and/or coreTools changes:
    - Version update
    - Updated Signal Descriptions chapter for new format
    - Updated the “Performance” section in “Integration Considerations” chapter for APB4
    - Uses coreTools version 2014.12-SP1-1
- Packaging changes:
    - Minor packaging enhancements

Changed in 2.03a version of DW_apb

- RTL changes:
    - Fix for the incorrect ERROR response generated on AHB Interface for APB3 Slaves
    - Lint cleanup
- Documentation and/or coreTools changes:
    - Version update
    - Updated the “Performance” section in “Integration Considerations” chapter
    - Uses coreTools version 2013.03-SP1-2
    - Corrected the Default Input/Output Delay values in Signals chapter
- Packaging changes:
    - Minor packing enhancements

Changed in 2.02c version of DW_apb

- RTL changes:
    - None
- Documentation and/or coreTools changes:
    - Updated the databook template
    - Uses coreTools version 2012.06-SP2
- Packaging changes:
    - Corrected file prefixing in the encrypted mode

Changed in 2.02b version of DW_apb

- RTL changes:
    - None
- Documentation and/or coreTools changes:
    - Uses coreTools version 2010.09-SP2

Changed in 2.02a version of DW_apb

- RTL changes:
  - Corrected hrdata for transfers issued from AHB to AMBA 3 APB Slaves so that it is aligned with hready_resp
- Documentation and/or coreTools changes:
  - Updated Figure 3-14 to reflect current hrdata functionality; updated system graphic in Figure 1-1

Changed in 2.01a version of DW_apb

- RTL changes:
  - Packaging fixed so that start and end addresses are updated every time address map changes
- Documentation and/or coreTools changes:
  - None

Changed in 2.00a version of DW_apb

- RTL changes:
  - Enhancement to support AHB-to-APB3 bridge
- Documentation and/or coreTools changes:
  - Enhanced databook to include additional information about AMBA 3 APB protocol

Changed in 1.04a version of DW_apb

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.03 or later
  - Corrected names of include files and vcs command used for simulation in databook
  - Corrected syntax for undef directive

Changed in 1.03a version of DW_apb

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2008.06-SP2-2

Changed in 1.02e version of DW_apb

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Databook corrected to show correct pclk_en input
  - Uses coreTools version 2007.06-SP4

Changed in 1.02d version of DW_apb

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2007.06-1 or later
  - Enhanced databook to include additional information about clock behavior

Changed in 1.02c version of DW_apb

- Enhanced databook includes coreAssembler intent in Chapter 2.
- The coreAssembler or coreConsultant GUIs can now be used to select VIP/VMT versions.
- Two missing parameters—HADDR_WIDTH and PADDR_WIDTH—were added to the databook.
- Register descriptions are now included in SPIRIT files.

Changed in 1.02b version of DW_apb

- A new flow tutorial based on DesignWare Connect now comprises Chapter 2, "Building and Verifying a Component or Subsystem" of the *DesignWare DW_apb Databook*.
- The DW_apb can now be used in the coreTools 5.*x* environment.
- The DW_apb now supports the DC-FPGA environment.
- Enhanced databook includes coreAssembler intent in Chapter 2
- The size of the DesignWare Synthesizable Components image has been reduced to about 60 MB by removing the DesignWare Memory Model TSP and the QuickStart examples designs; these are now available through separate downloads. For more information, refer to the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide*.
- The DesignWare Synthesizable Components image is now self-extracting.

Changed in 1.02a version of DW_apb

- Source code for this component is available on a per-project basis as a DesignWare Core. Please contact your local sales office for the details. For source licensing information, refer to "Licenses" in the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide*.

Changed in 1.01e version of DW_apb

- DesignWare Connect – Enables you to construct, modify, and simulate any single- or multi-layer system in about an hour.
- The Verilog-XL simulator is not supported.
- The HP-UX platform is not supported.
- VHDL simulation is not supported.

1.4.7.2 DW_apb Releases

Table 1-7 lists the latest versions of the DW_apb component, the releases in which they were included, and the corresponding VERSION_ID register values.

Table 1-7 DesignWare for AMBA 2/ DW_apb Releases

DesignWare Release for AMBA 2	DW_apb Version	VERSION_ID Value	Databook Date
2020.12a	3.03a	33_30_33_2A	December 2020
2018.07a	3.02a	33_30_32_2A	July 2018
2016.10a	3.01a	33_30_31_2A	October 2016
2015.06a	3.00a	33_30_30_2A	June 2015
2014.06a	2.03a	32_30_33_3A	June 2014
2013.05a	2.02c	32_30_32_2A	May 2013
2011.10a	2.02b	32_30_32_2A	October 2011
2011.06a	2.02a	32_30_32_2A	June 2011
2011.04a	2.01a	32_30_31_2A	April 2011
2010.12a	2.00a	32_30_30_2A	December 2010
2010.09a	1.04a	31_30_34_2A	September 2010
2009.06a	1.03a	31_30_33_2A	June 2009
2008.10a	1.03a	31_30_33_2A	October 2008
2008.06a	1.02e	31_30_32_2A	June 2008
2007.06a	1.02d	31_30_32_2A	June 2007
2007.04a	1.02c	31_30_32_2A	April 2007
2005.04a	1.02b	31_30_32_2A	April 2005
2004.11	1.02a	31_30_32_2A	November, 2004
2004.06	1.01e	31_30_31_2A	June 21, 2004

DesignWare Release for AMBA 2	DW_apb Version	VERSION_ID Value	Databook Date
2003.10	1.01d	31_30_31_2A	October 20, 2003
2003.02	1.01c	31_30_31_43	March 27, 2003
2002.08-SP1	1.01b	31_30_31_42	September 24, 2002
2002.08	1.01a	31_30_31_41	August 27, 2002

1.4.7.3 DW_apb Known Problems and Workarounds

There are no known issues in this release of the DW_apb.

1.4.8 DW_apb_gpio

The following sections list the new features and changes, and the fixed problems and enhancements, for the DW_apb_gpio component. For DW_apb_gpio-specific STARs, refer to:

https://www.synopsys.com/dw/star.php?c=DW_apb_gpio

For detailed features description, see the *DW_apb_gpio databook*.

For information on known issues, refer to "DW_apb_gpio Known Problems and Workarounds" on page 69.

1.4.8.1 DW_apb_gpio New Features and Changes

This section describes what was new or changed during the various versions of the DW_apb_gpio:

Changed in 2.14a version of DW_apb_gpio

- RTL Changes:
  - RTL compliance to SpyGlass Q-2020.03-SP1 and GuideWare 2020.03
- Documentation changes:
  - Refer to the Revision History chapter of the DW_apb_gpio databook
- Packaging changes:
  - STAR 3115176: Updated sWork::evalInComponent to align with coreTools version Q-2020.03-SP4-2
  - Minor packaging updates

Changed in 2.13a version of DW_apb_gpio

- RTL Changes:
  - RTL compliance to SpyGlass 2017.12-SP1 and GuideWare 2017.12
  - Enhancement:

        - Added support for configurable synchronization depth through coreConsultant parameters GPIO_PA_SYNC_DEPTH, GPIO_PB_SYNC_DEPTH, GPIO_PC_SYNC_DEPTH, and GPIO_PD_SYNC_DEPTH
    - Documentation and/or coreTools changes:
        - Version update
        - References to the GPIO Component Type register is removed from the databook; no such register exist in the hardware
        - Updated Synthesis results in the Integration Considerations chapter of the databook
        - Published the first version of DesignWare Synthesizable Components for AMBA 2 User Guide
        - Removed Chapter 2 "Building and Verifying a Component or Subsystem" from the databook and added the content in the newly created user guide
        - Signals, Parameters, Registers and Internal parameters chapter auto-extracted with change bars from the RTL
        - Uses coreTools version N-2017.12-SP2
    - Packaging changes:
        - Minor packaging updates
    - Removed support for NC Verilog Simulator and MTI Simulator

Changed in 2.12a version of DW_apb_gpio

- RTL Changes:
    - Lint and CDC Cleanup
- Documentation and/or coreTools changes:
    - Version update
    - Parameter Descriptions and Register Descriptions chapters auto-extracted from the RTL
    - Removed references to Leda
    - Uses coreTools version 2016.09

Changed in 2.11a version of DW_apb_gpio

- RTL Changes:
    - Lint and CDC Cleanup
    - Includes synchronizers for port A, B, C, or D only if their respective parameter GPIO_P*x*_SYNC_EXT_DATA is set, where *x* denotes port A, B, C, or D.
- Documentation and/or coreTools changes:
    - Version update
    - Signal Descriptions chapter auto-extracted from the RTL
    - Uses coreTools version 2014.12-SP1-1

- Packaging changes:
  - Minor packaging enhancements
  - Memory Map updates for defining access type to reserved fields

Changed in 2.10a version of DW_apb_gpio

- RTL changes:
  - Lint cleanup
  - RTL changed for the enhancement of Interrupt detection on both posedge/negedge
- Documentation and/or coreTools changes:
  - Version update
  - Updates for Interrupt detection on both posedge/negedge.
  - Added the “Performance” section in “Integration Considerations” chapter
  - Uses coreTools version 2013.03-SP1-2
  - Corrected the External Input/Output Delay values in Signals chapter
- Packaging changes:
  - Minor packing enhancements
  - IP-XACT enhancement for enumeration and display names.

Changed in 2.09e version of DW_apb_gpio

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Updated the databook template
  - Uses coreTools version 2012.06-SP2
- Packaging changes:
  - Corrected inconsistencies in RAL files
  - Corrected file prefixing in the encrypted mode

Changed in 2.09d version of DW_apb_gpio

- RTL changes:
  - Version change for updated databook
- Documentation and/or coreTools changes:
  - Corrected errors in the dependencies listed for Port C and Port D signals

Changed in 2.09c version of DW_apb_gpio

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Clarified name of gpio_ext_portxN_rb signal in Control RTL block diagram
  - Corrected read/write information for gpio_ls_sync register.

Changed in 2.09b version of DW_apb_gpio

- RTL changes:
  - Corrected inconsistencies in RAL files
- Documentation and/or coreTools changes:
  - None

Changed in 2.09a version of DW_apb_gpio

- RTL changes:
  - Enhancement to replace clock domain synchonizer logic with standard BCM synchronizers
- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.09-SP2

Changed in 2.08b version of DW_apb_gpio

- RTL changes:
  - Added C headers to component package
  - Corrected base addresses in IP-XACT file
- Documentation and/or coreTools changes:
  - None

Changed in 2.08a version of DW_apb_gpio

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.03 or later
  - Corrected names of include files and vcs command used for simulation in databook
  - Corrected syntax for undef directive

Changed in 2.07a version of DW_apb_gpio

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2008.06-SP2-2

Changed in 2.06c version of DW_apb_gpio

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Corrections to databook figures explaining debounce logic
  - Register description corrections to databook (gpio_swporta_ddr and gpio_porta_ctl)
  - Information added recommended interrupt clearing procedure
  - Uses coreTools version 2007.06-SP4

Changed in 2.06b version of DW_apb_gpio

- RTL changes:
  - Removed GPIO_REV_ID_CODE, GPIO_VERSION_ID, and GPIO_PERIPH_ID from header files
- Documentation and/or coreTools changes:
  - Uses coreTools version 2007.06-1 or later
  - Derived values for gpio_config_reg1 and gpio_config_reg2 corrected in databook

Changed in 2.06a version of DW_apb_gpio

- Enhanced databook includes coreAssembler intent in Chapter 2.
- The coreAssembler or coreConsultant GUIs can now be used to select VIP/VMT versions.
- Register descriptions are now included in SPIRIT files.
- Documentation changes:
  - Addresses 0x78 and 0x7c are now described in the databook
  - References for GPIO_PWIDTH and GPIO_ID_WIDTH corrected
  - RTL changed so that address values for gpio_config_reg1 and gpio_config_reg2 are correct in databook

Changed in 2.04a version of DW_apb_gpio

- A new flow tutorial based on DesignWare Connect now comprises Chapter 2, “Building and Verifying a Component or Subsystem” of the *DesignWare DW_apb_gpio Databook*.

- The DW_apb_gpio Driver Kit is available, which allows you to easily program the DW_apb_gpio and integrate it into your higher-level application. For information about the DW_apb_gpio Driver Kit, refer to the *DesignWare DW_apb_gpio Driver Kit User Guide.*
- The DW_apb_gpio can now be used in the coreTools 5.*x* environment.
- The DW_apb_gpio now supports the DC-FPGA environment.
- The size of the DesignWare Synthesizable Components image has been reduced to about 60 MB by removing the DesignWare Memory Model TSP and the QuickStart examples designs; these are now available through separate downloads. For more information, refer to the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide*.
- The DesignWare Synthesizable Components image is now self-extracting.
- Enhanced databook includes coreAssembler intent in Chapter 2.

Changed in 2.03a version of DW_apb_gpio

- Source code for this component is available on a per-project basis as a DesignWare Core. Please contact your local sales office for the details. For source licensing information, refer to “Licenses” in the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide*.

Changed in 2.02b version of DW_apb_gpio

- DesignWare Connect – Enables you to construct, modify, and simulate any single- or multi-layer system in about an hour.
- The Verilog-XL simulator is not supported.
- The HP-UX platform is not supported.
- VHDL simulation is not supported.

Changed in 2.02a version of DW_apb_gpio

- The operating mode for each bit of a port can be controlled individually.
- Configurable reset values on output ports.
- Configurable synchronization of interrupt signals.
- In the memory map, the name of the Version ID register, now known as the Component Version register, has changed from GPIO_VERSION_ID to GPIO_COMP_VERSION.

1.4.8.2 DW_apb_gpio Releases

Table 1-8 lists the latest versions of the DW_apb_gpio component, the releases in which they were included, and the corresponding GPIO_VER_ID_CODE register values.

Table 1-8 DesignWare for AMBA 2/DW_apb_gpio Releases

DesignWare Release for AMBA 2	DW_apb_gpio Version	GPIO_VER_ID_CODE Value	Databook Date
2020.12a	2.14a	32_31_34_2A	December 2020
2018.07a	2.13a	32_31_33_2A	July 2018
2016.10a	2.12a	32_31_32_2A	October 2016
2015.06a	2.11a	32_31_31_2A	June 2015
2014.06a	2.10a	32_31_30_2A	June 2014
2013.05a	2.09e	32_30_39_2A	May 2013
2012.06a	2.09d	32_30_39_2A	June 2012
2012.03a	2.09c	32_30_39_2A	March 2012
2011.11a	2.09b	32_30_39_2A	November 2011
2011.10a	2.09a	32_30_39_2A	October 2011
2011.04a	2.08b	32_30_38_2A	April 2011
2010.09a	2.08a	32_30_38_2A	September 2010
2009.06a	2.07a	32_30_37_2A	June 2009
2008.10a	2.07a	32_30_37_2A	October 2008
2008.06a	2.06c	32_30_36_2A	June 2008
2007.06a	2.06b	32_30_36_2A	June 2007
2007.04a	2.06a	32_30_36_2A	April 2007
2005.04a	2.04a	32_30_34_2A	April 2005
2004.11	2.03a	32_30_33_2A	November 2004
2004.06	2.02b	32_30_32_2A	June 21, 2004
2003.10	2.02a	32_30_32_2A	October 20, 2003
2003.02 overlay	2.01a	32_30_31_41	
2003.02	2.00a	32_30_30_41	March 26, 2003
2002.08-SP1	1.00b	31_30_31_42	

1.4.8.3 DW_apb_gpio Known Problems and Workarounds

There are no known issues in this release of the DW_apb_gpio.

1.4.9 DW_apb_i2c

The following sections list the new features and changes, and the fixed problems and enhancements, for the DW_apb_i2c component. For DW_apb_i2c-specific STARs, refer to:

http://www.synopsys.com/dw/star.php?c=DW_apb_i2c

For detailed features description, see the *DW_apb_i2c databook*.

For information on known issues, refer to "DW_apb_i2c Known Problems and Workarounds" on page 83.

1.4.9.1 DW_apb_i2c New Features and Changes

This section describes what was new or changed during the various versions of the DW_apb_i2c:

Changed in 2.03a version of DW_apb_i2c

- RTL Changes:
  - Design compliance to SpyGlass Q-2020.03-SP1 and GuideWare 2020.03
  - Enhancement
    - STAR 9001438537: Support for selecting Multiple Slave Address in the SMBus Slave mode of operation. The DW_apb_i2c supports maximum four Slave addresses in this release.
    - STAR 3172204: SMBus 3.1 specification support.
    - STAR 3146026: Support for programmable UDID feature for all slaves (IC_SAR, IC_SAR2, IC_SAR3 and IC_SAR4).
    - STAR 9001554517: Documentation update to reflect the description of the intr(_n) signal and associated parameter IC_INTR_IO as per the design support.
  - Fixed
    - STAR 3253200: APB Slave pready and pslverr signals declarations inside the DW_apb_i2c_regfile are guarded as per the APB3 configuration; no functional impact.
    - STAR 3354339: Removed the usage of duplicate declaration of the mst_tx_scl_hld_low_en_r in the DW_apb_i2c_tx_shift module; no functional impact.
    - STAR 9001449405: The IP behavior is updated to respect the programming bit IC_CON.SMBUS_PERSISTENT_SLV_ADDR_EN. The IP does not expect the address to be resolved if this field is programmed to 1. The address valid (AV) flag is set and DW_apb_i2c Slave is ready to receive non-ARP commands.
    - STAR 9001525475: Alert Response Address is supported when IC_CON.SMBUS_ARP_EN=0. When ARP is enabled (IC_CON.SMBUS_ARP_EN = 1), the SMBUS Slave device (DW_apb_i2c slave) does not respond to the Alert Response Address (ARA) sent from the SMBus Host.

      The IP behavior is updated to respond to the ARA when ARP is enabled (IC_CON.SMBUS_ARP_EN=1).
    - STAR 9001555511: The DW_apb_i2c slave does not release the SCL line after detecting the SMBus SCL stuck at low timeout interrupt, when transmitting the data as per the SMBus Host read request.

      This behavior is updated to release the SCL line post the SCL stuck at low interrupt.

        - STAR 3196386: When SMBus ARP is enabled (IC_CON.SMBUS_ARP_EN = 1), the DW_apb_i2c SMBus Slave device responds with incorrect PEC byte to the Alert Response Address (ARA) sent from the SMBus Host - which is received in response to the assertion of SMBus Alert signal (SMBALERT#) from the SMBus Slave device.

          This behavior is updated to respond with correct PEC information.
        - STAR 3285667: During SMBus operation, if the SMBus Host stretches the clock resulting in the timeout and never resumes the clock, then DW_apb_i2c Slave device holds the SDA line. This behavior is observed during SMBus write or during Slave ACK/NACK phase.

          The behavior is updated in the Slave mode of operation to release the SDA line during these erroneous conditions.
- Documentation changes:
  - Refer to the Revision History chapter of the DW_apb_i2c databook
- Packaging changes:
  - STAR 3385296: Register field IC_ENABLE.TX_CMD_BLOCK existence condition is update to only if configuration parameter IC_TX_CMD_BLOCK is set to 1.
  - STAR 3115176: Updated sWork::evalInComponent to align with coreTools version Q-2020.03-SP4-2
  - Minor packaging updates

Changed in 2.02a version of DW_apb_i2c

- RTL Changes:
  - RTL compliance to SpyGlass 2017.12-SP1 and GuideWare 2017.12
  - Fixed Defect:
    - STAR 9001201697: RTL is not respecting TX_CMD_BLOCK setting after receiving a TX_ABRT (and FIFO Not empty). The I2C commands are not being blocked due to the last address, data NACK'ed, or aborted I2C transfer. RTL is updated to make sure the commands are blocked in this scenario.
  - Enhancements:

    STAR 9001375074:
    - UDID MSB 96-bits are software programmable and firmware can update them as per the requirement
    - Support for the APB3.0 and APB4.0 protocol
    - Generate NACK on RX-FIFO full condition in Slave mode of operation
- Documentation and/or coreTools changes:
  - Version update
  - Updated Synthesis results in the Integration Considerations chapter of the databook
  - Published the first version of DesignWare Synthesizable Components for AMBA 2 User Guide
  - Removed Chapter 2 “Building and Verifying a Component or Subsystem” from the databook and added the content in the newly created user guide

- Signals, Parameters, Registers and Internal parameters chapter auto-extracted with change bars from the RTL
- Uses coreTools version N-2017.12-SP2

- Packaging changes:
  - Minor packaging updates
- Removed support for NC Verilog Simulator and MTI Simulator

Changed in 2.01a version of DW_apb_i2c

- RTL Changes:
  - Lint and CDC Cleanup
  - Enhancements:
    - An IP that supports a serial clock to be slower than or equal to the APB clock
    - I2C cannot be disabled using IC_ENABLE when IC_EMPTYFIFO_HOLD_MASTER_EN = 1
  - Fixed:
    - Difference in generated SCL Clock frequency when used as a Master Tx and Rx
    - Restriction on supported pclk and ic_clk ratios in case of asynchronous clocks
    - I2C Master generates erroneous transfer on the I2C bus after a loss in arbitration
    - Previous SDA RX_HOLD value is considered for detecting START condition
    - Incorrect Generation of TX_EMPTY Interrupt
    - STOP Detect interrupt not generated in Slave mode for Device ID Transfer
- Documentation and/or coreTools changes:
  - Version update
  - Parameter Descriptions and Register Descriptions chapters auto-extracted from the RTL
  - Updated description for SMBus
  - Updated the ic_smbalert_oe signal description
  - Removed references to Leda
  - Uses coreTools version 2016.09

Changed in 2.00a version of DW_apb_i2c

- RTL Changes:
  - Lint and CDC Cleanup
  - Enhanced to support:
    - Bus Clear Feature
    - SMBus and PMBus features
    - Ultra-Fast Mode
    - Clock Frequency Optimization
  - Fixed:

        - The TX_EMPTY interrupt generation problem when TX_EMPTY_CTRL=1.
- Documentation and/or coreTools changes:
    - Version update
    - Signal Descriptions chapter auto-extracted from the RTL
    - Added:
        - Feature for Bus Clear Feature
        - Feature for SMBus, PMBus
        - Feature for Ultra-Fast Mode
        - Feature for Clock Frequency Optimization
    - Updated the "Performance" section in "Integration Considerations" chapter for Bus Clear feature, PMBus, SMBus, and Ultra-Fast mode
    - Uses coreTools version 2014.12-SP1-1
- Packaging changes:
    - Minor packaging enhancements
    - Memory Map updates for defining access type to reserved fields

Changed in 1.22a version of DW_apb_i2c

- RTL changes:
    - Lint cleanup
    - Updated synchronization structures using bcm21 synchronizers
    - Resolved Frequency Limitation in High-Speed Mode
    - Fixed:
        - Multi master clock synchronization issue
        - TX_FLUSH_CNT bit of IC_TX_ABRT_SOURCE register captures a wrong value
        - RX_OVER interrupt consider both the programmable and configurable option
        - Bus idle time in HS mode is too low
        - High Speed RESTART & STOP Generated at Fast Speed timings
    - Removed risk of violation of tHD;STA and tSU;STO when SCL high/low count programmed to minimum value
    - Enhanced:
        - I^2C Master should not generate STOP DET interrupt when inactive
        - Register status bits indicating the device and reason for clock stretching
        - Avoiding RX FIFO flush during TX Abort (coreConsultant parameter IC_AVOID_RX_FIFO_FLUSH_ON_TX_ABRT is introduced to select this functionality)
    - Added Programmable bit to control transmit data manually
- Documentation and/or coreTools changes:
    - Version update

- Added:
  - Feature for Blocking the Tx FIFO commands using IC_TX_CMD_BLOCK field in IC_ENABLE register
  - Feature to indicate first data byte received after the address in IC_DATA_CMD register
  - Bits in IC_STATUS register for Indicating a reason for bus holding
  - Feature to detect the STOP interrupt only if master is active
  - Performance section in Integration considerations
  - coreConsultant parameter (IC_AVOID_RX_FIFO_FLUSH_ON_TX_ABRT) introduced to avoid flushing of RX FIFO during TX Abort
  - Replaced the two-flop synchronizer used for SCL and SDA signals with standard component BCM41
- IC_TX_ABRT_SOURCE register changed the width of the field TX_FLUSH_CNT.
- Corrected register width in many register descriptions
- Uses coreTools version 2013.03-SP1-2
- Corrected the Default Input/Output Delay in the Signals chapter

- Packaging changes:
  - Minor packing enhancements.
  - IP-XACT enhancement for enumeration and display names
  - Corrected data description inconsistencies in RAL files
  - Parameter override removal, instead of overriding its gives an error now

Changed in 1.21a version of DW_apb_i2c

- RTL changes:
  - Added a new configuration parameter, IC_RX_FULL_HLD_BUS_EN.
  - Modified the IC_CON register and the IC_RAW_INTR_STAT register.
  - Modified the IC_SDA_HOLD register.
  - Added a new bit RESTART_DET to the IC_INTR_STAT, IC_INTR_MASK, and IC_RAW_INTR_STAT registers. This bit detects a repeated start when the DW_apb_i2c is the addressed slave.
  - Added the register IC_CLR_RESTART_DET to clear the RESTART_DET interrupt. Added the coreConsultant parameter IC_SLV_RESTART_DET_EN and the signal ic_restart_det_intr(_n) to enable restart detect in slave mode.
  - Added a new bit MST_ON_HOLD to the IC_INTR_STAT, IC_INTR_MASK, and IC_RAW_INTR_STAT registers. This bit indicates whether a master is holding the bus and the TX FIFO is empty. Added the signal ic_mst_on_hold_intr(_n)
  - Added a new feature to generate a TX_EMPTY interrupt when the transmit buffer level goes below IC_TX_TL and the TX_SHIFTER is empty. This feature can be enabled and disabled by using the IC_CON register.
  - Removed unused signal min_hld_cmplt.

- Corrected a situation in which a User Abort caused an I2C protocol violation.
- Fixed a problem that caused the DW_apb_i2c master to drop a read command after user abort, when the IC_EMPTYFIFO_HOLD_MASTER_EN configuration parameter was enabled.
- Enhanced the DW_apb_i2c to generate an interrupt in the slave mode only when it is the addressed slave. This feature can be enabled and disabled by using the IC_CON register.

- Documentation and/or coreTools changes:
  - Added a section on Fast Mode Plus and updated the document for references to Fast Mode Plus. Removed text stating that Fast Mode Plus is not supported.
  - Removed a note in the IC_TX_ABRT_SOURCE register description stating that the DW_apb_i2c can be a master and slave at the same time.
  - Made a minor correction to the description of TX_FLUSH_CNT field of the IC_TX_ABRT_SOURCE register and the TX_ABRT field of the IC_RAW_INTR_STAT register.
  - Updated the programming flow for DW_apb_i2c as master in standard or fast mode.
  - Corrected the active state of the ic_current_src_en signal.
  - Updated the method for deriving ic_clk values in high-speed modes.
  - Added a programming flow for DW_apb_i2c master with TAR update.
  - Updated the template.
  - Uses coreTools version 2012.06-SP2
- Packaging changes:
  - Corrected inconsistencies in RAL files
  - Corrected file prefixing in the encrypted mode

Changed in 1.20a version of DW_apb_i2c

- RTL changes:
  - Added control bit to initiate I2C transfer abort
  - Corrected situation in which DMA request asserts irrespective of Tx FIFO reset
  - Corrected CDC violations
  - Corrected situation in which Rx data is pushed to Rx FIFO only after Tx FIFO is not empty
- Documentation changes:
  - Edited calculations for driving SDA in “High-Speed Modes” section
  - Updated IC_ENABLE and IC_TX_ABRT_SOURCE registers

Changed in 1.17a version of DW_apb_i2c

- RTL changes:
  - RTL updated to enhance guard for SDA_HOLD and SDA_SETUP registers
  - Fixed problem causing false bus idle indication in multiple-master situations
  - Fix for generated XML/RAL files to have correct reset value for IC_TAR register

- Documentation changes:
  - Updated definition of IC_FS_SPKLEN and IC_HS_SPKLEN register descriptions
  - Enhanced programming example with bulleted descriptions
  - Corrected programming values for dma_tx_req and dma_rx_req signals

Changed in 1.16b version of DW_apb_i2c

- RTL changes:
  - Corrected problem when High Speed Mode is not selected in configuration, access mode of IC_HS_MADDR register in RAL file should be “ro” instead of “rw”
- Documentation changes:
  - None

Changed in 1.16a version of DW_apb_i2c

- RTL changes:
  - Enhancement to replace clock domain synchonizer logic with standard BCM synchronizers
- Documentation changes:
  - Uses coreTools version 2010.09-SP2

Changed in 1.15a version of DW_apb_i2c

- RTL changes:
  - Spike suppression now complies to I2C specification
- Documentation changes:
  - Added spike suppression material
  - Corrected access type attribute for individual register fields in RAL file
  - Corrected R/W locations in timing diagrams in “Tx FIFO Management and START, STOP and RESTART Generation” section

Changed in 1.14a version of DW_apb_i2c

- RTL changes:
  - Enhancement for controlling START and STOP conditions regardless of FIFO status.
  - Corrected behavior of ic_current_src_en.
- Testbench changes:
  - Fixed test_9000076847 so that it correctly emulates arbitration conflicts between two I^2C masters when there are fixed delays
  - Corrected packaged testbench so that when ic_clk is asynchronous to pclk and its period is 3ns or less the following error message is not reported:

```
"FAILED: ERROR : [<time>] {i2c TestLib} In I2C Module #1 the read data is not
correct; Expected= <data>, Read= 0
```

- Documentation changes:
  - Corrected subsection numbering in “Registers” chapter

Changed in 1.13a version of DW_apb_i2c

- RTL changes:
  - Changed default value of IC_CLOCK_PERIOD from 500ns to 100ns when IC_MAX_SPEED_MODE is 1 to comply with restriction that ic_clk period cannot be larger than pclk period
  - Changed condition for SDA hold time check in order to prevent false SDA hold time errors in arbitration loss events
  - Updated random generation of IC_SAR and IC_TAR values in testbench to ensure no invalid addresses are generated
  - Corrected testbench to ensure value of IC_CLK_TYPE parameter is correctly propagated to all relevant tasks
  - Corrected behavior of component when disabled while ACK bit is being generated (there was a possibility the component would continuously drive the SDA line and deadlock the bus)
- Documentation changes:
  - Added information to databook on calculating the maximum admissible value for the IC_DEFAULT_SDA_HOLD parameter and IC_SDA_HOLD register; “SDA Hold Time” section and the description of IC_DEFAULT_SDA_HOLD parameter and the IC_SDA_HOLD register were updated.

Changed in 1.12a version of DW_apb_i2c

- RTL changes:
  - Fixed bug in testbench which resulted in test failure
- Documentation changes:
  - Uses coreTools version 2010.03 or later
  - Corrected names of include files and vcs command used for simulation in databook
  - Corrected syntax for undef directive
  - Databook updated to clarify connection between IC_DATA_CMD register and generation of ACK/NACK responses
  - Databook updated to note that in HS mode, RESTART and STOP conditions are sent at FS speed

Changed in 1.11a version of DW_apb_i2c

- RTL changes:
  - Added SDA hold time according to specification

- Documentation changes:
  - Corrected equations for avoiding underflow when programming a source burst transaction
  - Corrected dependencies for IC_SS_SCL_HIGH_COUNT, IC_SS_SCL_LOW_COUNT, IC_FS_SCL_HIGH_COUNT, and IC_FS_SCL_LOW_COUNT parameters
  - Clarified clock behavior for multiple master arbitration
  - Corrected IC_RESTART_EN parameter description
  - Modified description of IC_SDA_SETUP register
  - Updated databook to new template for consistency with other IIP/VIP/PHY databooks
  - Removed reference to I2C protocol created by Philips (NXP)
  - Corrected information regarding how DW_apb_i2c communicates with slaves when operating in master mode
  - Corrected default value for IC_DEFAULT_SDA_SETUP parameter
  - Added SDA hold time information
  - Added IC_SDA_HOLD register description
  - Removed references to 300ns hold time in integration considerations
  - Removed DW_apb_i2c Application Notes appendix
- coreTools changes:
  - Uses coreTools version 2009.06-SP1-1

Changed in 1.10a version of DW_apb_i2c

- RTL changes:
  - IC_SDA_SETUP_DEFAULT may not be programmed to an illegal value
  - Packaging corrected to enable use of NC Verilog
  - Testbench updated to correctly use IC_TAR register value
  - Corrected reset value of IC_TAR
  - IC_HS_MASTER_CODE parameter is now enabled only if the IC_MAX_SPEED_MODE is set to High speed
- Documentation and/or coreTools changes:
  - IC_RX_FULL_GEN_NACK parameter removed
  - IC_INTR_MASK is active low
  - Dependency changed for IC_HS_MASTER_CODE parameter
  - IC_SLAVE_DISABLE default changed to 1
  - Values for HS mode corrected in Table 8
  - debug_* signal default values corrected
  - Uses coreTools version 2008.06-SP2-2

Changed in 1.09a version of DW_apb_i2c

- RTL changes:
  - Redundant clock type option removed
  - Reset of IC_TAR[12] now controlled by IC_10BIT_ADDR_MASTER parameter
  - Support for multi I2C master arbitration added with limitation that a single DW_apb_i2c instance may not function as both a master and slave in the system
  - General call interrupts now masked if IC_ACK_GENERAL_CALL register is 0
- Documentation and/or coreTools changes:
  - Uses coreTools version 2007.06-SP4
  - Removed Synchronous value from IC_CLK_TYPE parameter
  - Clarified that putting data into FIFO generates START, and emptying FIFO generates STOP
  - Clarified description of I2C_DYNAMIC_TAR_UPDATE parameter
  - More detail and clarifications added to ic_clk configuration section of databook
  - Register r/w attributes corrected in databook (IC_TX_ABRT_SOURCE, IC_DATA_CMD, IC_SLV_DATA_NACK_ONLY and IC_STATUS[6])
  - Table describing setting/clearing of ACTIVITY interrupt corrected in databook
  - Databook description of IC_SDA_SETUP implementation corrected
  - Removed reference to non-existent debug mode in databook
  - Clock domain crossing limitations explained in databook
  - Limitations of DW_apb_i2c combined format support now clearly detailed in databook
  - Clarification of IC_TAR description

Changed in 1.08b version of DW_apb_i2c

- RTL changes:
  - Corrected IC_10BITADDR_SLAVE parameter name for 10-bit addressing in slave mode.
- Documentation and/or coreTools changes:
  - Uses coreTools version 2007.06-1 or later

Changed in 1.08a version of DW_apb_i2c

- Removed IC_RX_FULL_GEN_NACK configuration parameter.
- RTL bug fixes.
- Fixed a “glitch” that was found when the DW_apb_i2c generated a RESTART.
- Enhanced databook includes coreAssembler intent in Chapter 2.
- The coreAssembler or coreConsultant GUIs can now be used to select VIP/VMT versions.
- Register descriptions are now included in SPIRIT files.

- Size for IC_DMA_TDLR register corrected to TX_ABW–1:0
- Reserved bits for IC_DMA_TDLR corrected to 31:TX_ABW

Changed in 1.06a version of DW_apb_i2c

- Added three software registers: IC_SDA_SETUP (STAR 9000076182), IC_ACK_GENERAL_CALL (STARs 9000075092 and 9000068233), and IC_ENABLE_STATUS.
- Added four hardware configuration parameters: IC_SLAVE_DATA_NACK_ONLY, IC_RX_FULL_GEN_NACK, IC_DEFAULT_SDA_SETUP, and IC_DEFAULT_ACK_GENERAL_CALL (STARs 9000076182, 9000075092, and 9000068233).
- Updated databook significantly to describe functional features in more detail. STARs 9000062223, 9000062677, 9000074883, 9000075267, and 9000075671.

Changed in 1.05a version of DW_apb_i2c

- A new flow tutorial based on DesignWare Connect now comprises Chapter 2, "Building and Verifying a Component or Subsystem" of the *DesignWare DW_apb_i2c Databook*.
- The DW_apb_i2c now supports a dynamic IC_TAR update. For more information on this functionality, refer to "Dynamic IC_TAR or IC_10BITADDR_MASTER Update" section in the *DesignWare DW_apb_i2c Databook*.
- The DW_apb_i2c can now be used in the coreTools 5.*x* environment.
- The size of the DesignWare Synthesizable Components image has been reduced to about 60 MB by removing the DesignWare Memory Model TSP and the QuickStart examples designs; these are now available through separate downloads. For more information, refer to the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide*.
- The DW_apb_i2c now supports the DC-FPGA environment.
- The DesignWare Synthesizable Components image is now self-extracting.

Changed in 1.04a version of DW_apb_i2c

- Source code for this component is available on a per-project basis as a DesignWare Core. Please contact your local sales office for the details. For source licensing information, refer to "Licenses" in the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide*.
- The DW_apb_i2c Driver Kit is available, which allows you to easily program the DW_apb_i2c and integrate it into your higher-level application. For information about the DW_apb_i2c Driver Kit, refer to the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide*.

Changed in 1.03a version of DW_apb_i2c

- DesignWare Connect – Enables you to construct, modify, and simulate any single- or multi-layer system in about an hour.
- The Verilog-XL simulator is not supported.

- The HP-UX platform is not supported.
- VHDL simulation is not supported.

For a list of all the features of the DW_apb_i2c, refer to the "Features" section of the *DesignWare DW_apb_i2c Databook*.

1.4.9.2 DW_apb_i2c Releases

Table 1-9 lists the latest versions of the DW_apb_i2c component, the releases in which they were included, and the corresponding I2C_COMP_VERSION register values.

Table 1-9 DesignWare for AMBA 2/DW_apb_i2c Releases

DesignWare Release for AMBA 2	DW_apb_i2c Version	I2C_COMP_VERSION value	Databook Date
2020.12a	2.03a	32_30_33_2A	December 2020
2018.07a	2.02a	32_30_32_2A	July 2018
2016.10a	2.01a	32_30_31_2A	October 2016
2015.06a	2.00a	32_30_30_2A	June 2015
2014.06a	1.22a	31_32_32_2A	June 2014
2013.05a	1.21a	31_32_31_2A	May 2013
2012.06a	1.20a	31_32_30_2A	June 2012
2012.03a	1.17a	31_31_37_2A	March 2012
2011.11a	1.16b	31_31_36_2A	November 2011
2011.10a	1.16a	31_31_36_2A	October 2011
2011.04a	1.15a	31_31_35_2A	April 2011
2010.12a	1.14a	31_31_34_2A	December 2010
2010.10a	1.13a	31_31_33_2A	October 2010
2010.09a	1.12a	31_31_32_2A	September 2010
2010.03a	1.11a	31_31_31_2A	March 2010
2009.06a	1.10a	31_31_30_2A	June 2009
2008.10a	1.10a	31_31_30_2A	October 2008
2008.06a	1.09a	31_30_39_2A	June 2008
2007.06a	1.08b	31_30_38_2A	June 2007
2007.04a	1.08a	31_30_38_2A	April 2007
2005.04a	1.08a	31_30_38_2A	January 2007

DesignWare Release for AMBA 2	DW_apb_i2c Version	I2C_COMP_VERSION value	Databook Date
2005.04a	1.06a	31_30_36_2A	October 5, 2005
2005.04a	1.05a	31_30_35_2A	April 2005
2004.11	1.04a	31_30_34_2A	November 2004
2004.06	1.03a	31_30_33_2A	July 27, 2004
2003.10	1.03a	31_30_33_2A	January 20, 2004
2003.10	1.02a	31_30_32_2A	November 4, 2003
N/A	1.01a	31_30_31_41	April 17, 2002
2003.02	1.00a	31_30_30_41	March 26, 2003

1.4.9.3 DW_apb_i2c Known Problems and Workarounds

The following are known issues in this release:

- UVM RAL Subsystem (coreAssembler) Ping test is not supported for DW_apb_i2c.

The following are known issues in 1.06a and are addressed during 1.08a release:

- Master-Transmit Attempt Becomes a Slave-Transmit Operation (STAR 9000105354)

  Workaround: This requires the DW_apb_i2c to operate in a "reduced" mode, that is, setting the DW_apb_i2c to operate either as a master OR slave but not both. This means that setting bit 6 of the IC_SLAVE_DISABLE register to '0' and bit 0 of the IC_MASTER_MODE register to '1' in the IC_CON register is an unsupported use of the component.

- DW_apb_i2c Releases SCL Prematurely During Slave-Transmit (STAR 9000093708)

  Workaround: This requires the DW_apb_i2c to operate in a "reduced" mode, that is, setting the DW_apb_i2c to operate either as a master OR slave but not both. This means that setting bit 6 of the IC_SLAVE_DISABLE register to '0' and bit 0 of the IC_MASTER_MODE register to '1' in the IC_CON register is an unsupported use of the component.

- Due to issues related with STARs 9000093709 and 9000093730, the configuration parameter IC_RX_FULL_GEN_NACK is now permanently set to False (0).

  Resolution in 1.08a: This feature is deprecated and not visible in the coreConsultant GUI. The operation is the same as the setting of IC_RX_FULL_GEN_NACK to False (0).

- Multiple Instantiations Cause Simulation Error (STAR 9000091999)

  When multiple instantiations of the DW_apb_i2c are used in a single environment at the RTL/design stage, including simulations, the macro definitions are repeated for the subsequent parsing of the files for DW_apb_i2c. This results in warnings on macro re-definitions and lead to simulation failures.

  Workaround: If there is more than one instantiation of the DW_apb_i2c, then insert the following two lines just before the endmodule Verilog keyword:

```
`undef IC_SLV_DATA_NACK_ONLY_EN
`undef IC_RX_FULL_GEN_NACK_EN
```

Resolution in 1.08a: Fixed in design

- Interrupts Asserted Briefly Just After Hardware Reset (STAR 9000092958)

  One-cycle-wide pulses on the interrupt lines are observed when the reset input of DW_apb_i2c is asserted. This may have the risk of erroneously triggering an interrupt response by the system's CPU.

  Workaround: None.

  Resolution in 1.08a: Fixed in design.

- No CPU Indication of Flushed FIFO for Slave-Transmit Operation (STAR 9000093545)

  On responding to a Slave-Transmit operation, two bytes were written into the transmit FIFO. The remote I^2C master, however, NACKs the first data byte, causing the DW_apb_i2c to flush the transmit FIFO. However, there is no interrupt indication via the status registers or interrupts that this has happened.

  Workaround: None.

  Resolution in 1.08a: Fixed in design

- General Call Interrupt Generated Even Though Transfer NACKed (STAR 9000093547)

  The IC_ACK_GENERAL_CALL register was added to allow the DW_apb_i2c, under software control, to either ACK or NACK an I^2C general call address. A unique status and interrupt, associated with the general call, is also provided. When set to NACK, however, the DW_apb_i2c continues to generate this interrupt, while not indicating the reception of a general call. This interrupt generation is not necessary

  Workaround: All interrupts in the DW_apb_i2c have their own interrupt masks, and the bit M_GEN_CALL of the IC_INTR_MASK register should be set to "1" when IC_ACK_GENERAL_CALL is set to "0". This is a viable workaround in software because the settings of the IC_INTR_MASK and IC_ACK_GENERAL_CALL registers are static.

  Resolution in 1.08a: Behavior is not modified in the design. If required, use workaround.

- DW_apb_i2c Transmit Stalls After Transmit Abort Event (STAR 9000108249)

  If continuous CPU writes are made to the IC_DATA_CMD register for I^2C bulk transfers, in either Master or Slave mode, then it is possible that such writes coincide with the occurrence of a transmit event. This causes the internal FSMs to ignore the fact that the transmit FIFO is not empty while staying in the idle states. That is, IC_TXFLR is non-zero, while IC_STATUS bit 0 is '0'. This is incorrect because the DW_apb_i2c is supposed to be active if the transmit FIFO is not empty.

  Workaround: Software can detect this stall condition when _TXFLR is non-zero, while the IC_STATUS bit 0 is '0'. As a workaround, the IC_ENABLE register is required to be toggled before the DW_apb_i2c resumes normal operation. This is done by writing a '0', then followed by writing a '1' to the IC_ENABLE register. Effectively, this removes all contents in the transmit FIFO and forces all internal states in the DW_apb_i2c to be in the idle state.

  Resolution in 1.08a: Fixed in design.

- Glitch Generated when Moving from FS Mode to HS Mode (STAR 9000093198)

  When moving from an FS mode to HS mode of operation, the DW_apb_i2c is required to generate a RESTART condition on the I^2C bus. In doing so, it is observed that a one cycle glitch on the ic_data_oe output is observed on the succeeding falling edge of SCL (ic_clk_oe goes to '0').

  Workaround: None

  Resolution: RTL fix.

The following have been known issues since DW_apb_i2c 1.05a:

- A new feature has been enabled in Design Compiler (W-2004.12 and later) that removes any registers that Design Compiler identifies as being a constant value.; this can save a lot of area. The new register removal capability being on by default in Design Compiler may cause Formality to fail for the DW_apb_i2c, depending on the configuration.

  The workaround is to disable this feature by setting the Design Compiler variable compile_seqmap_propagate_constants to false. You can set the variable through your .synopsys_dc.setup file or from the coreConsultant command line. To set the variable from within coreConsultant, issue the following command before running the Synthesize activity:

  ```
  set_design_attribute {dc_shellVariable[compile_seqmap_propagate_constants]}
  false
  ```

- STAR 9000049061 – In the DW_apb_i2c databook (1.02a), while using the DW_apb_i2c as the master when it writes to a slave or addressing, the hold time between SDA and the falling edge of SCL does not conform to the protocol of I2C, which says that tHD:DAT should be 300-900ns (for fast mode devices).
- Error: Not enough memory for new VM_code using NC-Verilog or MTI-Verilog on Linux O/S.

  Description: This problem is caused by the Linux BigMem (BM) patch on Linux systems in RH 7, 8 or E3.0, which limit dynamically linked libraries to about 100MB in size. Additional linked libraries required for the DW_apb_i2c Driver can exceed this limit, and prevent the Vera dynamic library from loading.

  Workaround 1: Switch off bus monitors ("monitor = OFF" makefile argument) if verification monitors are not needed. This workaround may not work if software Driver option is used.

  Workaround 2: Use a Linux machine that does not have the BM patch applied.

- The DW_apb_i2c Driver Kit currently does not function correctly when a processor is in big-endian mode.

  Workaround: Ensure that the processor operates in little-endian mode when using the DW_apb_i2c Driver Kit.

1.4.10 DW_apb_i2s

The following sections list the new features and changes, and the fixed problems and enhancements, for the DW_apb_i2s component. For DW_apb_i2s-specific STARs, refer to:

https://www.synopsys.com/dw/star.php?c=DW_apb_i2s

For detailed features description, see the *DW_apb_i2s databook*.

For information on known issues, refer to "DW_apb_i2s Known Problems and Workarounds" on page 91.

1.4.10.1 DW_apb_i2s New Features and Changes

This section describes what was new or changed during the various versions of the DW_apb_i2s:

Changed in 1.12a version of DW_apb_i2s

- RTL Changes:
  - Design compliance to SpyGlass Q-2020.03-SP1 and GuideWare 2020.03
  - Enhancement
    - STAR 9001419227: Support for the Time Division Multiplexing (TDM) support in the IP.
- Documentation changes:
  - Refer to the Revision History chapter of the DW_apb_i2s databook.
- Packaging changes:
  - STAR 3115176: Updated sWork::evalInComponent to align with coreTools version Q-2020.03-SP4-2
  - Minor packaging updates

Changed in 1.11a version of DW_apb_i2s

- RTL Changes:
  - RTL compliance to SpyGlass 2017.12-SP1 and GuideWare 2017.12
  - Enhancement:
    - STAR 9000437163: Hardware handshaking interface support for DMA mode of operation. Combined and Dedicated handshaking interface per channel is supported.
- Documentation and/or coreTools changes:
  - Version update
  - Updated Synthesis results in the Integration Considerations chapter of the databook
  - Published the first version of DesignWare Synthesizable Components for AMBA 2 User Guide
  - Removed Chapter 2 "Building and Verifying a Component or Subsystem" from the databook and added the content in the newly created user guide
  - Signals, Parameters, Registers and Internal parameters chapter auto-extracted with change bars from the RTL
  - Uses coreTools version N-2017.12-SP2

- Packaging changes:
  - Minor packaging updates
- Removed support for NC Verilog Simulator and MTI Simulator

Changed in 1.10a version of DW_apb_i2s

- RTL Changes:
  - Lint and CDC Cleanup
  - Fixed:
    - Offset values for TOR1/2/3 are corrected
- Documentation and/or coreTools changes:
  - Version update
  - Parameter Descriptions and Register Descriptions chapters auto-extracted from the RTL
  - Removed references to Leda
  - Uses coreTools version 2016.09

Changed in 1.09a version of DW_apb_i2s

- RTL Changes:
  - Lint and CDC Cleanup
- Documentation and/or coreTools changes:
  - Version update
  - Signal Descriptions chapter auto-extracted from the RTL
  - Uses coreTools version 2014.12-SP1-1
- Packaging changes:
  - Minor packaging enhancements
  - Memory Map updates for defining access type to reserved fields

Changed in 1.08a version of DW_apb_i2s

- RTL changes:
  - Lint cleanup
- Documentation and/or coreTools changes:
  - Version update
  - Added:
    - “Transaction Example” section in the “Functional Description” chapter
    - “Performance” section in “Integration Considerations” chapter
  - Uses coreTools version 2013.03-SP1-2

- Packaging changes:
  - Minor packing enhancements
  - IP-XACT enhancement for enumeration and display names
  - Corrected data description inconsistencies in RAL files

Changed in 1.07a version of DW_apb_i2s

- RTL changes:
  - Made code changes to avoid Leda violations
- Documentation and/or coreTools changes:
  - Made minor corrections in the description of the ws_out, sw_slv, and sdox signals.
  - Removed a note regarding DesignWare Verification IP (VIP) in the "Verification" section of the DW_apb_i2s databook, as this component does not use DesignWare VIP.
  - Removed references to VIP from the coreTools GUI.
  - Updated the databook template
  - Uses coreTools version 2012.06-SP2
- Packaging changes:
  - Corrected file prefixing in the encrypted mode

Changed in 1.06e version of DW_apb_i2s

- RTL changes:
  - RAL-related fix for generated XML/RAL files
- Documentation and/or coreTools changes:
  - None

Changed in 1.06d version of DW_apb_i2s

- RTL changes:
  - Corrected inconsistencies in RAL files
- Documentation and/or coreTools changes:
  - None

Changed in 1.06c version of DW_apb_i2s

- RTL changes:
  - None

- Documentation changes:
  - Uses coreTools version 2010.09-SP2

Changed in 1.06b version of DW_apb_i2s

- RTL changes:
  - Removed wrong input delay set on pclk port
- Testbench changes:
  - Corrected behavior of intr signal in test_DW_apb_i2s.v
- Documentation changes:
  - Removed signals starting with dma_*, which are not implemented in RTL
  - Clarification added on the use of the sclk_en and sclk_gate outputs
  - Corrected conditions for programmed gating value in SCLKG field of CCR register

Changed in 1.06a version of DW_apb_i2s

- RTL changes:
  - None
- Documentation changes:
  - Uses coreTools version 2010.03 or later
  - Corrected names of include files and vcs command used for simulation in databook
  - Corrected syntax for undef directive
  - Corrections in databook to text that specifies FIFO depth

Changed in 1.05a version of DW_apb_i2s

- RTL changes:
  - Corrected period of sclk_n to be constrained to one-half of sclk period
  - Clock domain crossing fixed to ensure sclk and pclk domain signals were not mixed in asynchronous clock mode configurations
  - Updated synchronization structures using bcm21 synchronizers
- Documentation changes:
  - Corrected usage flow diagrams for DW_apb_i2s as a receiver and as a transmitter
  - Enhanced information on writing to a transmit channel and reading from a receive channel
  - Modified procedures in the “Programming the DW_apb_i2s chapter
  - Modified parameter descriptions
  - Updated databook to new template for consistency with other IIP/VIP/PHY databooks

- coreTools changes:
  - Uses coreTools version 2009.06-SP1-1
  - CoreConsultant configuration updated so that VIP model selection is available in Simulation activity

Changed in 1.04a version of DW_apb_i2s

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2008.06-SP2-2

Changed in 1.03a version of DW_apb_i2s

- RTL changes:
  - Redundant false path constraint removed
  - Reset pin added for sclk domain
  - Clock gating testing enabled in testbench
  - Clock gating signal now asserts after I2_SCLK_GATE+1 cycles
  - Generation of the sclk_gate signal now changes in line with WS on the falling edge of sclk
- Documentation and/or coreTools changes:
  - Uses coreTools version 2007.06-SP4

Changed in 1.02b version of DW_apb_i2s

- RTL changes: none
- Documentation and/or coreTools changes:
  - Uses coreTools version 2007.06-1 or later

Changed in 1.01a version of DW_apb_i2s

- Uses coreTools version 2007.06-1 or later.
- Enhanced databook includes coreAssembler intent in Chapter 2.
- The coreAssembler or coreConsultant GUIs can now be used to select VIP/VMT versions.
- Register descriptions are now included in SPIRIT files.

1.4.10.2 DW_apb_i2s Releases

Table 1-10 lists the latest versions of the DW_apb_i2s component, the releases in which they were included, and the corresponding I2S_COMP_VERSION register values.

Table 1-10 DesignWare for AMBA 2/DW_apb_i2s Releases

DesignWare Release for AMBA 2	DW_apb_i2s Version	I2S_COMP_VERSION value	Databook Date
2020.12a	1.12a	31_31_32_2A	December 2020
2018.07a	1.11a	31_31_31_2A	July 2018
2016.10a	1.10a	31_31_30_2A	October 2016
2015.06a	1.09a	31_30_39_2A	June 2015
2014.06a	1.08a	31_30_38_2A	June 2014
2013.05a	1.07a	31_30_37_2A	May 2013
2012.03a	1.06e	31_30_36_2A	March 2012
2011.11a	1.06d	31_30_36_2A	November 2011
2011.10a	1.06c	31_30_36_2A	October 2011
2011.04a	1.06b	31_30_36_2A	April 2011
2010.09a	1.06a	31_30_36_2A	September 2010
2010.03a	1.05a	31_30_35_2A	March 2010
2009.06a	1.04a	31_30_34_2A	June 2009
2008.10a	1.04a	31_30_34_2A	October 2008
2008.06a	1.03a	31_30_33_2A	June 2008
2007.06a	1.02b	31_30_32_2A	June 2007
2007.04a	1.02a	31_30_32_2A	April 2007
2005.04a	1.01a	31_30_31_2A	August 12, 2005

1.4.10.3 DW_apb_i2s Known Problems and Workarounds

There are no known issues in this release of the DW_apb_i2s.

1.4.11 DW_apb_ictl

The following sections list the new features and changes, and the fixed problems and enhancements, for the DW_apb_ictl component. For DW_apb_ictl-specific STARs, refer to:

https://www.synopsys.com/dw/star.php?c=DW_apb_ictl

For detailed feature description, see the *DW_apb_ictl databook*.

For information on known issues, refer to "DW_apb_ictl Known Problems and Workarounds" on page 97.

1.4.11.1 DW_apb_ictl New Features and Changes

This section describes what was new or changed during the various versions of the DW_apb_ictl:

Changed in 2.10a version of DW_apb_ictl

- RTL Changes:
  - RTL compliance to SpyGlass Q-2020.03-SP1 and GuideWare 2020.03
- Documentation changes:
  - Refer to the Revision History chapter of the DW_apb_ictl databook.
- Packaging changes:
  - STAR 3115176: Updated sWork::evalInComponent to align with coreTools version Q-2020.03-SP4-2
  - Minor packaging updates

Changed in 2.09a version of DW_apb_ictl

- RTL Changes:
  - RTL compliance to SpyGlass 2017.12-SP1 and GuideWare 2017.12
  - Enhancement:
    - STAR 9001103749: Vectored interrupt support. It allows a processor to quickly sample the vector address associated with a currently pending IRQ.
- Documentation and/or coreTools changes:
  - Version update
  - Updated Synthesis results in the Integration Considerations chapter of the databook
  - Published the first version of DesignWare Synthesizable Components for AMBA 2 User Guide
  - Removed Chapter 2 "Building and Verifying a Component or Subsystem" from the databook and added the content in the newly created user guide
  - Signals, Parameters, Registers and Internal parameters chapter auto-extracted with change bars from the RTL
  - Uses coreTools version N-2017.12-SP2
- Packaging changes:

  - Minor packaging updates
- Removed support for NC Verilog Simulator and MTI Simulator

Changed in 2.08a version of DW_apb_ictl

- RTL Changes:
  - Lint Cleanup
- Documentation and/or coreTools changes:
  - Version update
  - Parameter Descriptions and Register Descriptions chapters auto-extracted from the RTL
  - Removed references to Leda
  - Uses coreTools version 2016.09

Changed in 2.07a version of DW_apb_ictl

- RTL Changes:
  - Lint Cleanup
- Documentation and/or coreTools changes:
  - Version update
  - Signal Descriptions chapter auto-extracted from the RTL
  - Uses coreTools version 2014.12-SP1-1
- Packaging changes:
  - Minor packaging enhancements
  - Memory Map updates for defining access type to reserved fields

Changed in 2.06a version of DW_apb_ictl

- RTL changes:
  - Lint cleanup
- Documentation and/or coreTools changes:
  - Version update
  - Uses coreTools version 2013.03-SP1-2
  - Added the “Performance” section in “Integration Considerations” chapter
  - Corrected the Default Input/Output Delay in the Signals chapter
- Packaging changes:
  - Minor packing enhancements
  - IP-XACT enhancement for enumeration and display names
  - Corrected data description inconsistencies in RAL files

Changed in 2.05f version of DW_apb_ictl

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Updated the databook template
  - Uses coreTools version 2012.06-SP2
- Packaging changes:
  - Corrected file prefixing in the encrypted mode

Changed in 2.05e version of DW_apb_ictl

- RTL changes:
  - RAL-related fix for generated XML/RAL files
- Documentation and/or coreTools changes:
  - None

Changed in 2.05d version of DW_apb_ictl

- RTL changes:
  - Corrected IRQ_VECTOR_*i* register designations in RAL file generated by coreConsultant
- Documentation and/or coreTools changes:
  - None

Changed in 2.05c version of DW_apb_ictl

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.09-SP2

Changed in 2.05b version of DW_apb_ictl

- RTL changes:
  - Removed wrong input delay set on hclk port
- Documentation and/or coreTools changes:
  - Corrected range for IRQ_INTEN_L register when generating RAL file
  - Generated RAL file no longer includes registers not present in the selected configuration

Changed in 2.05a version of DW_apb_ictl

- RTL changes:
  - Corrected volatile property of register locations in generated SPIRIT .xml memory map description
  - Removed old header files
- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.03 or later
  - Corrected names of include files and vcs command used for simulation in databook
  - Corrected syntax for undef directive

Changed in 2.04a version of DW_apb_ictl

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2008.06-SP2-2

Changed in 2.03c version of DW_apb_ictl

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2007.06-SP4

Changed in 2.03b version of DW_apb_ictl

- RTL changes:
  - Packaging fixed to enable USE_FOUNDATION parameter for all configurations
- Documentation and/or coreTools changes:
  - Uses coreTools version 2007.06-1 or later

Changed in 2.03a version of DW_apb_ictl

- Enhanced databook includes coreAssembler intent in Chapter 2.
- The coreAssembler or coreConsultant GUIs can now be used to select VIP/VMT versions.
- Register descriptions are now included in SPIRIT files.
- Register references from irq_pN_offset to irq_pr_N corrected in databook.

Changed in 2.02a version of DW_apb_ictl

- A new flow tutorial based on DesignWare Connect now comprises Chapter 2, "Building and Verifying a Component or Subsystem" of the *DesignWare DW_apb_ictl Databook*.
- Enhanced databook includes coreAssembler intent in Chapter 2.

Changed in 2.01a version of DW_apb_ictl

- Source code for this component is available on a per-project basis as a DesignWare Core. Please contact your local sales office for the details. For source licensing information, refer to "Licenses" in the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide*.
- The DW_apb_ictl can now be used in the coreTools 5.*x* environment.
- The size of the DesignWare Synthesizable Components image has been reduced to about 60 MB by removing the DesignWare Memory Model TSP and the QuickStart examples designs; these are now available through separate downloads. For more information, refer to the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide*.
- The DW_apb_ictl now supports the DC-FPGA environment.
- The DesignWare Synthesizable Components image is now self-extracting.

Changed in 2.00b version of DW_apb_ictl

- DesignWare Connect – Enables you to construct, modify, and simulate any single- or multi-layer system in about an hour.
- The Verilog-XL simulator is not supported.
- The HP-UX platform is not supported.
- VHDL simulation is not supported.

Changed in 2.00a version of DW_apb_ictl

- It is now possible to configure the DW_apb_ictl to allow the priority levels of the interrupt sources be changed by reprogramming.
- In the memory map, the name of the Version ID register, now known as the Component Version register, has changed from ICTL_VERSION_ID to APB_ICTL_COMP_VERSION.

For a list of all the features of the DW_apb_ictl, refer to the "Features" section of the *DesignWare DW_apb_ictl Databook*.

1.4.11.2 DW_apb_ictl Releases

Table 1-11 lists the latest versions of the DW_apb_ictl component, the releases in which they were included, and the corresponding APB_ICTL_COMP_VERSION register values.

Table 1-11 DesignWare for AMBA 2/DW_apb_ictl Releases

DesignWare Release for AMBA 2	DW_apb_ictl Version	APB_ICTL_ COMP_VERSION value	Databook Date
2020.12a	2.10a	32_31_30_2A	December 2020
2018.07a	2.09a	32_30_39_2A	July 2018
2016.10a	2.08a	32_30_38_2A	October 2016
2015.06a	2.07a	32_30_37_2A	June 2015
2014.06a	2.06a	32_30_36_2A	June 2014
2013.05a	2.05f	32_30_35_2A	May 2013
2012.03a	2.05e	32_30_35_2A	March 2012
2011.11a	2.05d	32_30_35_2A	November 2011
2011.10a	2.05c	32_30_35_2A	October 2011
2011.04a	2.05b	32_30_35_2A	April 2011
2010.09a	2.05a	32_30_35_2A	September 2010
2009.06a	2.04a	32_30_34_2A	June 2009
2008.10a	2.04a	32_30_34_2A	October 2008
2008.06a	2.03c	32_30_33_2A	June 2008
2007.06a	2.03b	32_30_33_2A	June 2007
2007.04a	2.03a	32_30_33_2A	April 2007
2005.04a	2.02a	32_30_32_2A	April 2005
2004.11	2.01a	32_30_31_2A	November 2004
2004.06	2.00b	32_30_30_2A	June 21, 2004
2003.10	2.00a	32_30_30_2A	October 20, 2003
2003.02	1.00a	31_30_30_41	March 26, 2003
NOTE: This component evolved from DW_amba_ictl version 1.02c.			

1.4.11.3 DW_apb_ictl Known Problems and Workarounds

There are no known issues in this release of the DW_apb_ictl.

1.4.12 DW_apb_rap

The following sections list the new features and changes, and the fixed problems and enhancements, for the DW_apb_rap component. For DW_apb_rap-specific STARs, refer to:

https://www.synopsys.com/dw/star.php?c=DW_apb_rap

For the DW_apb_rap databook, refer to:

https://www.synopsys.com/dw/doc.php/iip/DW_apb_rap/latest/doc/DW_apb_rap_databook.pdf

For information on known issues, refer to "DW_apb_rap Known Problems and Workarounds" on page 103.

1.4.12.1 DW_apb_rap New Features and Changes

This section describes what was new or changed during the various versions of the DW_apb_rap:

Changed in 2.09a version of DW_apb_rap

- RTL Changes:
  - RTL compliance to SpyGlass Q-2020.03-SP1 and GuideWare 2020.03
- Documentation changes:
  - Refer to the Revision History chapter of the DW_apb_rap databook
- Packaging changes:
  - STAR 3115176: Updated sWork::evalInComponent to align with coreTools version Q-2020.03-SP4-2
  - Minor packaging updates

Changed in 2.08a version of DW_apb_rap

- RTL Changes:
  - RTL compliance to SpyGlass 2017.12-SP1 and GuideWare 2017.12
- Documentation and/or coreTools changes:
  - Version update
  - Updated Synthesis results in the Integration Considerations chapter of the databook
  - Published the first version of DesignWare Synthesizable Components for AMBA 2 User Guide
  - Removed Chapter 2 "Building and Verifying a Component or Subsystem" from the databook and added the content in the newly created user guide
  - Signals, Parameters, Registers and Internal parameters chapter auto-extracted with change bars from the RTL
  - Added new verification testbench chapter
  - Uses coreTools version N-2017.12-SP2
- Packaging changes:

  - Minor packaging updates
- Removed support for NC Verilog Simulator and MTI Simulator

Changed in 2.07a version of DW_apb_rap

- RTL Changes:
  - Lint Cleanup
- Documentation and/or coreTools changes:
  - Version update
  - Signal Descriptions and Register Descriptions chapters auto-extracted from the RTL
  - Uses coreTools version 2016.09

Changed in 2.06a version of DW_apb_rap

- RTL Changes:
  - Lint Cleanup
- Documentation and/or coreTools changes:
  - Version update
  - Signal Descriptions chapter auto-extracted from the RTL
  - Uses coreTools version 2014.12-SP1-1
- Packaging changes:
  - Minor packaging enhancements
  - Memory Map updates for defining access type to reserved fields

Changed in 2.05a version of DW_apb_rap

- RTL changes:
  - Lint cleanup
- Documentation and/or coreTools changes:
  - Version update
  - Uses coreTools version 2013.03-SP1-2
  - Added the “Performance” section in “Integration Considerations” chapter
  - Corrected the External Input/Output Delay in the Signals chapter
- Packaging changes:
  - Minor packing enhancements
  - IP-XACT enhancement for enumeration and display names
  - Corrected data description inconsistencies in RAL files

Changed in 2.04e version of DW_apb_rap

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Updated the databook template
  - Uses coreTools version 2012.06-SP2
- Packaging changes:
  - Corrected file prefixing in the encrypted mode

Changed in 2.04d version of DW_apb_rap

- RTL changes:
  - RAL-related fix for generated XML/RAL files
- Documentation and/or coreTools changes:
  - Corrected reset value for IdCode register.

Changed in 2.04c version of DW_apb_rap

- RTL changes:
  - Corrected inconsistencies in RAL files
- Documentation and/or coreTools changes:
  - None

Changed in 2.04b version of DW_apb_rap

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.09-SP2

Changed in 2.04a version of DW_apb_rap

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.03 or later
  - Corrected names of include files and vcs command used for simulation in databook
  - Corrected syntax for undef directive

Changed in 2.03a version of DW_apb_rap

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2008.06-SP2-2

Changed in 2.02e version of DW_apb_rap

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2007.06-SP4

Changed in 2.02d version of DW_apb_rap

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2007.06-1 or later

Changed in 2.02c version of DW_apb_rap

- Enhanced databook includes coreAssembler intent in Chapter 2.
- The coreAssembler or coreConsultant GUIs can now be used to select VIP/VMT versions.
- Register descriptions are now included in SPIRIT files.

Changed in 2.02b version of DW_apb_rap

- A new flow tutorial based on DesignWare Connect now comprises Chapter 2, "Building and Verifying a Component or Subsystem" of the *DesignWare DW_apb_rap Databook*.
- The DW_apb_rap can now be used in the coreTools 5.*x* environment.
- The DW_apb_rap now supports the DC-FPGA environment.
- Enhanced databook includes coreAssembler intent in Chapter 2
- The size of the DesignWare Synthesizable Components image has been reduced to about 60 MB by removing the DesignWare Memory Model TSP and the QuickStart examples designs; these are now available through separate downloads. For more information, refer to the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide*.
- The DesignWare Synthesizable Components image is now self-extracting.

Changed in 2.02a version of DW_apb_rap

- Source code for this component is available on a per-project basis as a DesignWare Core. Please contact your local sales office for the details. For source licensing information, refer to "Licenses" in the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide*.

Changed in 2.01a version of DW_apb_rap

- DesignWare Connect – Enables you to construct, modify, and simulate any single- or multi-layer system in about an hour.
- The Verilog-XL simulator is not supported.
- The HP-UX platform is not supported.
- VHDL simulation is not supported.

Changed in 2.00b version of DW_apb_rap

- In the memory map, the name of the Version ID register, now known as the Component Version register, has changed from RAP_VERSION_ID to RAP_COMP_VERSION.

For a list of all the features of the DW_apb_rap, refer to the "Features" section of the *DesignWare DW_apb_rap Databook*.

1.4.12.2 DW_apb_rap Releases

Table 1-12 lists the latest versions of the DW_apb_rap component, the releases in which they were included, and the corresponding RAP_COMP_VERSION register values.

Table 1-12 DesignWare for AMBA 2/DW_apb_rap Releases

DesignWare Release for AMBA 2	DW_apb_rap Version	RAP_COMP_VERSION value	Databook Date
2020.12a	2.09a	32_30_39_2A	December 2020
2018.07a	2.08a	32_30_38_2A	July 2018
2016.10a	2.07a	32_30_37_2A	October 2016
2015.06a	2.06a	32_30_36_2A	June 2015
2014.06a	2.05a	32_30_35_2A	June 2014
2013.05a	2.04e	32_30_34_2A	May 2013
2012.03a	2.04d	32_30_34_2A	March 2012
2011.11a	2.04c	32_30_34_2A	November 2011
2011.10a	2.04b	32_30_34_2A	October 2011

DesignWare Release for AMBA 2	DW_apb_rap Version	RAP_COMP_VERSION value	Databook Date
2010.09a	2.04a	32_30_34_2A	September 2010
2009.06a	2.03a	32_30_33_2A	June 2009
2008.10a	2.03a	32_30_33_2A	October 2008
2008.06a	2.02e	32_30_32_2A	June 2008
2007.06a	2.02d	32_30_32_2A	June 2007
2007.04a	2.02c	32_30_32_2A	April 2007
2005.04a	2.02b	32_30_32_2A	April 2005
2004.11	2.02a	32_30_32_2A	November 2004
2004.06	2.01a	32_30_31_2A	June 21, 2004
2003.10	2.00b	32_30_30_2A	October 20, 2003
2003.02	2.00a	32_30_30_41	March 26, 2003
2002.08-SP1-1	1.02c	31_30_32_43	October 25, 2002
2002.08-SP1	1.01b	31_30_31_42	October 2, 2002
2002.08	1.01a	31_30_31_41	August 20, 2002

1.4.12.3 DW_apb_rap Known Problems and Workarounds

There are no known issues in this release of the DW_apb_rap.

1.4.13 DW_apb_rtc

The following sections list the new features and changes, and the fixed problems and enhancements, for the DW_apb_rtc component. For DW_apb_rtc-specific STARs, refer to:

https://www.synopsys.com/dw/star.php?c=DW_apb_rtc

For detailed feature description, see the *DW_apb_rtc databook*.

For information on known issues, refer to "DW_apb_rtc Known Problems and Workarounds" on page 109.

1.4.13.1 DW_apb_rtc New Features and Changes

This section describes what was new or changed during the various versions of the DW_apb_rtc:

Changed in 2.08a version of DW_apb_rtc

- RTL Changes:
  - Design compliance to SpyGlass Q-2020.03-SP1 and GuideWare 2020.03
- Documentation changes:
  - Refer to the Revision History chapter of the DW_apb_rtc databook
- Packaging changes:
  - STAR 3115176: Updated sWork::evalInComponent to align with coreTools version Q-2020.03-SP4-2
  - Minor packaging updates

Changed in 2.07a version of DW_apb_rtc

- RTL Changes:
  - RTL compliance to SpyGlass 2017.12-SP1 and GuideWare 2017.12
- Documentation and/or coreTools changes:
  - Version update
  - Updated Synthesis results in the Integration Considerations chapter of the databook
  - Published the first version of DesignWare Synthesizable Components for AMBA 2 User Guide
  - Removed Chapter 2 "Building and Verifying a Component or Subsystem" from the databook and added the content in the newly created user guide
  - Signals, Parameters, Registers and Internal parameters chapter auto-extracted with change bars from the RTL
  - Uses coreTools version N-2017.12-SP2
- Packaging changes:
  - Minor packaging updates
- Removed support for NC Verilog Simulator and MTI Simulator

Changed in 2.06a version of DW_apb_rtc

- RTL Changes:
  - Lint and CDC Cleanup
  - Prescalar for RTC counter
  - APB3 and APB4 protocol support
- Documentation and/or coreTools changes:
  - Version update
  - Signal Descriptions and Register Descriptions chapters auto-extracted from the RTL
  - Removed references to Leda
  - Uses coreTools version 2016.09

Changed in 2.05a version of DW_apb_rtc

- RTL Changes:
  - Lint and CDC Cleanup
- Documentation and/or coreTools changes:
  - Version update
  - Signal Descriptions chapter auto-extracted from the RTL
  - Uses coreTools version 2014.12-SP1-1
- Packaging changes:
  - Minor packaging enhancements
  - Memory Map updates for defining access type to reserved fields

Changed in 2.04a version of DW_apb_rtc

- RTL changes:
  - Lint cleanup
  - Updated synchronization structures using bcm21 synchronizers
- Documentation and/or coreTools changes:
  - Version update
  - Added the “Performance” section in “Integration Considerations” chapter
  - Uses coreTools version 2013.03-SP1-2
  - Corrected the External Input/Output Delay in the Signals chapter
- Packaging changes:
  - Minor packing enhancements
  - IP-XACT enhancement for enumeration and display names
  - Corrected data description inconsistencies in RAL files

Changed in 2.03e version of DW_apb_rtc

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Updated the databook template
  - Uses coreTools version 2012.06-SP2
- Packaging changes:
  - Corrected file prefixing in the encrypted mode

Changed in 2.03d version of DW_apb_rtc

- RTL changes:
  - RAL-related fix for generated XML/RAL files
- Documentation and/or coreTools changes:
  - None

Changed in 2.03c version of DW_apb_rtc

- RTL changes:
  - Corrected inconsistencies in RAL files
- Documentation and/or coreTools changes:
  - None

Changed in 2.03b version of DW_apb_rtc

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.09-SP2

Changed in 2.03a version of DW_apb_rtc

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.03 or later
  - Corrected names of include files and vcs command used for simulation in databook
  - Corrected syntax for undef directive

Changed in 2.02a version of DW_apb_rtc

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2008.06-SP2-2

Changed in 2.01e version of DW_apb_rtc

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2007.06-SP4

Changed in 2.01d version of DW_apb_rtc

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2007.06-1 or later

Changed in 2.01c version of DW_apb_rtc

- Enhanced databook includes coreAssembler intent in Chapter 2.
- The coreAssembler or coreConsultant GUIs can now be used to select VIP/VMT versions.
- Register descriptions are now included in SPIRIT files.

Changed in 2.01b version of DW_apb_rtc

- A new flow tutorial based on DesignWare Connect now comprises Chapter 2, "Building and Verifying a Component or Subsystem" of the *DesignWare DW_apb_rtc Databook*.
- The DW_apb_rtc can now be used in the coreTools 5.*x* environment.
- Enhanced databook includes coreAssembler intent in Chapter 2.
- The DW_apb_rtc now supports the DC-FPGA environment.
- The size of the DesignWare Synthesizable Components image has been reduced to about 60 MB by removing the DesignWare Memory Model TSP and the QuickStart examples designs; these are now available through separate downloads. For more information, refer to the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide*.
- The DesignWare Synthesizable Components image is now self-extracting.

Changed in 2.01a version of DW_apb_rtc

- Source code for this component is available on a per-project basis as a DesignWare Core. Please contact your local sales office for the details. For source licensing information, refer to "Licenses" in the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide*.

Changed in 2.00c version of DW_apb_rtc

- DesignWare Connect – Enables you to construct, modify, and simulate any single- or multi-layer system in about an hour.
- The Verilog-XL simulator is not supported.
- The HP-UX platform is not supported.
- VHDL simulation is not supported.

Changed in 2.00b version of DW_apb_rtc

The following was new or changed in the 2.00b version of the DW_apb_rtc.

- In the memory map, the name of the Version ID register, now known as the Component Version register, has changed from RTC_VERSION_ID to RTC_COMP_VERSION.

For a list of all the features of the DW_apb_rtc, refer to the "Features" section of the *DesignWare DW_apb_rtc Databook*.

1.4.13.2 DW_apb_rtc Releases

Table 1-13 lists the latest versions of the DW_apb_rtc component, the releases in which they were included, and the corresponding RTC_COMP_VERSION register values.

Table 1-13 DesignWare for AMBA 2/DW_apb_rtc Releases

DesignWare Release for AMBA 2	DW_apb_rtc Version	RTC_COMP_VERSION value	Databook Date
2020.12a	2.08a	32_30_38_2A	December 2020
2018.07a	2.07a	32_30_37_2A	July 2018
2016.10a	2.06a	32_30_36_2A	October 2016
2015.06a	2.05a	32_30_35_2A	June 2015
2014.06a	2.04a	32_30_34_2A	June 2014
2013.05a	2.03e	32_30_33_2A	May 2013
2012.03a	2.03d	32_30_33_2A	March 2012
2011.11a	2.03c	32_30_33_2A	November 2011
2011.10a	2.03b	32_30_33_2A	October 2011
2010.09a	2.03a	32_30_33_2A	September 2010

DesignWare Release for AMBA 2	DW_apb_rtc Version	RTC_COMP_VERSION value	Databook Date
2009.06a	2.02a	32_30_32_2A	June 2009
2008.10a	2.02a	32_30_32_2A	October 2008
2008.06a	2.01e	32_30_31_2A	June 2008
2007.06a	2.01d	32_30_31_2A	June 2007
2007.04a	2.01c	32_30_31_2A	April 2007
2005.04a	2.01b	32_30_31_2A	April 2005
2004.11	2.01a	32_30_31_2A	November 2004
2004.06	2.00c	32_30_30_2A	June 21, 2004
2003.10	2.00b	32_30_30_2A	October 20, 2003
2003.02	2.00a	32_30_30_41	March 27, 2003
2002.08-SP1-1	1.01c	31_30_31_43	November 1, 2002
2002.08-SP1	1.0b	N/A	October 2, 2002
2002.08	1.0a	N/A	August 20, 2002

1.4.13.3 DW_apb_rtc Known Problems and Workarounds

There are no known issues in this release of the DW_apb_rtc.

1.4.14 DW_apb_ssi

The following sections list the new features and changes, and the fixed problems and enhancements, for the DW_apb_ssi component. For DW_apb_ssi-specific STARs, refer to:

https://www.synopsys.com/dw/star.php?c=DW_apb_ssi

For detailed features description, see the *DW_apb_ssi databook*.

For information on known issues, refer to "DW_apb_ssi Known Problems and Workarounds" on page 120.

1.4.14.1 DW_apb_ssi New Features and Changes

This section describes what was new or changed during the various versions of the DW_apb_ssi:

Changed in 4.03a version of DW_apb_ssi

- RTL Changes:
  - Design compliance to SpyGlass Q-2020.03-SP1 and GuideWare 2020.03
  - Enhancement:
    - STAR 3140853: Updated the behavior in the IP for the first bit transfer, TXD line toggles after two ssi_clk cycles from detecting first posedge of sclk_in. With updated behavior, TXD line should change with the falling edge of sclk_in.
    - STAR 9001549443: Added support for endian conversion for the XIP reads or the Data register read.
  - Fixed:
    - STAR 3218027: Fixed an issue where DW_apb_ssi provides an ERROR response upon data register and data is consumed within the IP. The issue is observed when data space just becomes available and at the same time APB is in data phase.
    - STAR 3213874: If data read is attempted from the Receive FIFO while the receive FIFO is empty, and the Receive data is pushed inside the FIFO from the serial interface at the same time, DW_apb_ssi provides underflow error. Since the data was not ready to be sent on APB interface at that moment, the internal register which keeps track of data entries does not increment the counter. This creates a mismatch between the actual FIFO level and the RXFLR register.
    - STAR 9001425441: The Microwire transfer concludes when transmit FIFO is empty, and a READY notification is received from the slave. The end of transmission is communicated by sending a START bit, and resuming the clock for one clock period. The READY notification comes at any point of time, however if the READY signal arrives earlier than ({Baud Rate}/2) ssi_clk cycles, then DW_apb_ssi master ends up transmitting the START bit and the clock at same time. Due to this the slave is unable to sample the STAR bit and may end up in the undefined state.
    - STAR 3393057: Updated SLV_OE bit in the CTRLR0 register to be read-only in master mode.
- Documentation changes:
  - Refer to the Revision History chapter of the DW_apb_ssi databook.
- Packaging changes:

- STAR 3115176: Updated sWork::evalInComponent to align with coreTools version Q-2020.03-SP4-2
- Minor packaging updates

Changed in 4.02a version of DW_apb_ssi

- RTL Changes:
  - RTL compliance to SpyGlass 2017.12-SP1 and GuideWare 2017.12
  - Fixed Defects:
    - STAR 9001125361: As per the intended functionality, RX Overflow interrupt should be generated when the RX FIFO has an additional entry after the FIFO Full condition. But the RX Overflow interrupt is incorrectly generated by the controller on FIFO Full condition. As a result, the application gets an incorrect information but there is no functional impact to the system.
    - STAR 9001167205: During Enhanced SPI transfers if the register field SCPH is set to 1, then DW_apb_ssi provides an extra SCLK edge after completing the transfer. The problem occurs in any configuration with Select SPI mode set to Dual, Quad, or Octal (SSI_SPI_MODE != 0).
    - STAR 9001225071: The problem occurs when RX FIFO underflow interrupt is generated, and this interrupt is cleared and the transfer process is resumed without disabling DW_apb_ssi. After this, underflow interrupt is generated on any RX POP till DW_apb_ssi is disabled. This problem occurs when (SSI_SYNC_CLK = 0).
    - STAR 9001232596: Slave not deselected after transmitting the start bit in microwire mode when Handshaking Interface is enabled. In the Microwire mode of operation during transmit with handshake enabled – at the end of the transfer, the DW_apb_ssi tries to deselect the slave; however, at the same time the FIFO is becoming non-empty. This causes the DW_apb_ssi to continue further without deselecting the slave. This problem occurs when SSI_HC_FRF = 0 OR SSI_HC_FRF=1 && SSI_DFLT_FRF=Microwire.
    - STAR 9001239835: During the Enhanced SPI read transfer, when RX_SAMPLE_DLY feature is used to delay the sampling point of the incoming data, the ssi_oe_n signal toggles after DW_apb_ssi sends the required amount of clock cycles. The toggle period of ssi_oe_n signal is equal to (BAUDR/2) -1. During this toggle period, the data on RX pin is not visible by DW_apb_ssi, which creates problem in sampling the incoming data. This problem occures when SSI_SPI_MODE != 0 and SSI_HAS_RX_SAMPLE_DELAY=1.
  - Enhancement:
    - STAR 9001176763: Added a ssi_busy signal that displays a debug status on whether SSI module is busy doing active transfers or is IDLE.
    - STAR 9001368664: Support for back to back transmit operation in Slave configuration. This update enables user to perform back to back transfers by loading the FIFO only once.
    - Added support for configurable synchronization depth through coreConsultant parameter SSI_P2S_SYNC_DEPTH, and SSI_S2P_SYNC_DEPTH.
- Documentation and/or coreTools changes:
  - Version update
  - Updated the Figures to reflect the 'ssi_oe_n' signal behavior in the SSI enhanced mode of operation (Dual/Quad/Octal) during wait cycles.

- Clock ration relationship between ssi_clk and sclk_out/sclk_in is updated to match the design intent.
- Updated Synthesis results in the Integration considerations chapter of the databook
- Published first version of DesignWare Synthesizable Components for AMBA 2 user guide
- Removed Chapter 2 Building and Verifying a Component or Subsystem from the databook and added the content in the newly created user guide
- Signals, Parameters, Registers and Internal parameters chapter auto-extracted with change bars from the RTL
- Uses coreTools version N-2017.12-SP2

- Packaging changes:
  - RTL packaging update to make sure in the Synchronous mode of operation the FIFO that gets generated is as per the chosen the FIFO DEPTH. In the previous version, the RTL allocates FIFO DEPTH + 2, in the Synchronous which is not intended.
  - Minor packaging updates
- Removed support for NC Verilog Simulator and MTI Simulator

Changed in 4.01a version of DW_apb_ssi

- RTL Changes:
  - Lint and CDC Cleanup
  - Enhancements:
    - Octal SPI mode
    - DDR and Read-Data-Strobe
    - Data Mask mode
    - eXecute-In-Place mode
    - Remove frequency restriction between ssi_clk and pclk
    - IO mapping for Enhanced SPI modes
    - Programming Slave select toggle in SPI mode
    - APB3 and APB4 protocol support
  - Fixed:
    - The ss_in_n signal not considered by Master in Dual/Quad mode
    - The rxd signal used as handshake in Microwire mode is used asynchronously
    - MSB of the txd line is corrupted in FIFO empty conditions (SSI_ENH_CLK_RATIO=1)
    - SPI Slave gets a 'Transmission error' after successful transfer
    - Using ss_in_n signal synchronously in SPI mode
- Documentation and/or coreTools changes:
  - Version updated
  - Parameter Descriptions and Register Descriptions chapters auto-extracted from the RTL
  - Removed references to Leda

- Uses coreTools version 2016.09
- Added following sections:
  - Advanced I/O Mapping for Enhanced SPI Modes
  - Dual Data-Rate (DDR) Support in SPI Operation
  - Read Data Strobe Signal Support
  - XIP Mode Support in SPI Mode
  - APB 3.0 Support
  - APB 4.0 Support
  - Data Mask Support for SPI
- Added following parameters for XIP and APB 4.0 support:
  - SSI_APBIF_TYPE
  - SSI_APB3_ERR_RESP_EN
  - SSI_XIP_EN
- Added following signals for XIP support:
  - xip_en
  - pready
  - pslverr
- Modified "Write Operation in Enhanced SPI Modes" and "Read Operation in Enhanced SPI Modes" sections
- Updated Appendix "Synchronizer 2: Synchronous (Dual-clock) FIFO Controller With Static Flags"

Changed in 4.00a version of DW_apb_ssi

- RTL Changes:
  - Lint and CDC Cleanup
  - Enhanced:
    - Slave Clock Ratio to support 4 and 6
    - Dual and Quad SPI features
  - Fixed:
    - Transmit of garbage data for BAUD=2 and CFS=1 in Microwire format
    - Slave select does not assert for full sclk_out in SSP format
- Documentation and/or coreTools changes:
  - Version update
  - Signal Descriptions chapter auto-extracted from the RTL
  - Added:
    - Slave Clock Ratio to support 4 and 6
    - Dual and Quad SPI modes

- Updated the “Performance” section in “Integration Considerations” chapter for Slave Clock Ratio and Dual/Quad features
- Updated description for Interrupt Polarity
- Uses coreTools version 2014.12-SP1-1

- Packaging changes:
  - Minor packaging enhancements
  - Memory Map updates for defining access type to reserved fields

Changed in 3.23a version of DW_apb_ssi

- RTL changes:
  - Lint cleanup
  - 32-bit Frame Size support
- Documentation and/or coreTools changes:
  - Version update
  - 32-bit Frame Size support
  - Fixed RX_SAMPLE_DELAY offset value
  - Uses coreTools version 2013.03-SP1-2
  - Added the “Performance” section in “Integration Considerations” chapter
  - Corrected the External Input/Output Delay in the Signals chapter
- Packaging changes:
  - Minor packing enhancements
  - IP-XACT enhancement for enumeration and display names
  - Corrected data description inconsistencies in RAL files

Changed in 3.22b version of DW_apb_ssi

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Added a section in the DW_apb_ssi databook to describe reset signals
  - Updated the databook template
  - Uses coreTools version 2012.06-SP2
- Packaging changes:
  - Corrected inconsistencies in RAL files
  - Corrected file prefixing in the encrypted mode

Changed in 3.22a version of DW_apb_ssi

- RTL changes:
  - RAL-related fix for generated XML/RAL files
- Documentation and/or coreTools changes:
  - Clarified conditions for asserting and clearing dma_tx_single and dma_rx_single signals
  - Added notes in Verification chapter clarifying that SSI master and slave BFMs are not VMT VIP models

Changed in 3.21b version of DW_apb_ssi

- RTL changes:
  - Corrected inconsistencies in RAL files
- Documentation and/or coreTools changes:
  - None

Changed in 3.21a version of DW_apb_ssi

- RTL changes:
  - Enhancement to replace clock domain synchonizer logic with standard BCM synchronizers
- Documentation changes:
  - Uses coreTools version 2010.09-SP2

Changed in 3.20a version of DW_apb_ssi

- RTL changes:
  - DW_apb_ssi databook says that in Slave mode and with microwire frame format, DW_apb_ssi sends dummy “0” bit before sending the data frame; however, RTL does not implement this, but instead sends MSB value of previous frame

    RTL updated to ensure SSI slave transmits logic 0 prior to transmitting data frame
  - Programming added to mode SCPH=0 to avoid slave select toggling between frames
  - Following list of signals that cross clock domains have been changed from combinatorial logic outputs to registered outputs:
    - DW_apb_ssi_mstfsm.fsm_sleep
    - DW_apb_ssi_mstfsm.fsm_busy
    - DW_apb_ssi_mstfsm.fsm_multi_mst
    - DW_apb_ssi_slvfsm.fsm_sleep
    - DW_apb_ssi_slvfsm.fsm_busy
    - DW_apb_ssi_slvfsm.tx_error
    - DW_apb_ssi_shift.rx_sr_busy

- DW_apb_ssi_intctl.mst_contention
- DW_apb_ssi_regfile.baudr_we

All synchronizer logic in RTL has been replaced with Synopsys DesignWare foundation synchronizers.

- Testbench changes:
  - Corrected stalling when a combination of short control words and fast baud rates is used in microwire control mode
- Documentation changes:
  - None

Changed in 3.18a version of DW_apb_ssi

- RTL changes:
  - None
- Testbench changes:
  - Corrected testbench to eliminate potential false data mismatch error at the start of DMA transfer tests
  - Fixed root cause for testbench failure with following error message:

    `"ERROR : [<time>] { ssi_TestLib } Detected txd toggle during EEPROM Read mode"`

    This error affected GTECH simulations and NCSim RTL simulations.
- Documentation changes:
  - None

Changed in 3.17a version of DW_apb_ssi

- RTL changes:
  - Logic added to the master state machine to prevent the txd output from toggling when only receiving data frame. This change impacts both Receive Only and EEPROM read operation modes. During Receive Only mode, the txd output is held constant. During EEPROM Read mode the txd output is held constant after all control data has been transmitted
- Documentation changes:
  - Changes in databook to clarify above RTL enhancement; sections “Receive Only”, “EEPROM Read”, “Master SPI and SSP Serial Transfers”, and “Motorola Serial Peripheral Interface (SPI)”

Changed in 3.16a version of DW_apb_ssi

- RTL changes:
  - None

- Documentation changes:
  - Uses coreTools version 2010.03 or later
  - Corrected names of include files and vcs command used for simulation in databook
  - Corrected syntax for undef directive

Changed in 3.15a version of DW_apb_ssi

- RTL changes:
  - Added programmable delay register used to sample incoming data
  - Corrected name of address block in memorymap.tcl file
  - Corrected CFS offset in IPXACT XML file
  - Corrected bit ranges for CFS and SRL in generated reports
  - SSI_DFLT_SS_N and SSI_DFLT_SCLK_OUT are now managed by cc_constants.v file
- Documentation changes:
  - Corrected equations for avoiding underflow when programming a source burst transaction
  - Updated databooks to new template for consistency with other IIP/VIP/PHY databooks
  - Enhanced features, parameters table, register chapter, and functional description with RXD Sample Delay information
- coreTools changes:
  - Uses coreTools version 2009.06-SP1-1

Changed in 3.13a version of DW_apb_ssi

- RTL changes:
  - Corrected data corruption of continuous SPI serial transfers caused by timing of DR write
- Documentation and/or coreTools changes:
  - None

Changed in 3.12a version of DW_apb_ssi

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Changed address offset and note for Data Register (DR)
  - Uses coreTools version 2008.06-SP2-2

Changed in 3.11c version of DW_apb_ssi

- RTL changes:
  - None

- Documentation and/or coreTools changes:
  - Bit numbers in MWCR diagram corrected
  - Correction in description of RXTFLR register
  - Correction in description of derived parameters TX_ABW and RX_ABW
  - Correction in table “DMATDL Decode Value”
  - Correction to description of DR register address offsets
  - Uses coreTools version 2007.06-SP4

Changed in 3.11b version of DW_apb_ssi

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2007.06-1 or later

Changed in 3.11a version of DW_apb_ssi

- Enhanced databook includes coreAssembler intent in Chapter 2.
- The coreAssembler or coreConsultant GUIs can now be used to select VIP/VMT versions.
- Register descriptions are now included in SPIRIT files.
- Databook now states EEPROM read mode not supported when the DW_apb_ssi is configured in SSP mode

Changed in 3.10a version of DW_apb_ssi

- Fixed STAR 9000075679, regarding microwire timing not matching the documentation.
- Enhanced databook includes coreAssembler intent in Chapter 2.

Changed in 3.04a version of DW_apb_ssi

- A new flow tutorial based on DesignWare Connect now comprises Chapter 2, “Building and Verifying a Component or Subsystem” of the *DesignWare DW_apb_ssi Databook*.
- The DW_apb_ssi can now be used in the coreTools 5.*x* environment.
- The size of the DesignWare Synthesizable Components image has been reduced to about 60 MB by removing the DesignWare Memory Model TSP and the QuickStart examples designs; these are now available through separate downloads. For more information, refer to the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide*.
- The DW_apb_ssi now supports the DC-FPGA environment.
- The DesignWare Synthesizable Components image is now self-extracting.

Changed in 3.03a version of DW_apb_ssi

- Source code for this component is available on a per-project basis as a DesignWare Core. Please contact your local sales office for the details. For source licensing information, refer to "Licenses" in the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide*.

Changed in 3.02a version of DW_apb_ssi

- DW_ahb_dmac Interface – The databook now describes the optional built-in DMA capability that can be selected during configuration.
- DesignWare Connect – Enables you to construct, modify, and simulate any single- or multi-layer system in about an hour.
- The Verilog-XL simulator is not supported.
- The HP-UX platform is not supported.
- VHDL simulation is not supported.

Changed in 3.00a version of DW_apb_ssi

- DW_ahb_dmac Interface – The databook now describes the optional built-in DMA capability that can be selected during configuration.
- In the memory map, the name of the Version ID register, now known as the Component Version register, has changed from SSI_VERSION_ID to SSI_COMP_VERSION.

For a list of all the features of the DW_apb_ssi, refer to the "Features" section of the *DesignWare DW_apb_ssi Databook*.

1.4.14.2 DW_apb_ssi Releases

Table 1-14 lists the latest versions of the DW_apb_ssi component, the releases in which they were included, and the corresponding SSI_COMP_VERSION register values.

Table 1-14 DesignWare for AMBA 2/DW_apb_ssi Releases

DesignWare Release for AMBA 2	DW_apb_ssi Version	SSI_COMP_VERSION value	Databook Date
2020.12a	4.03a	34_30_33_2A	December 2020
2018.07a	4.02a	34_30_32_2A	July 2018
2016.10a	4.01a	34_30_31_2A	October 2016
2015.06a	4.00a	34_30_30_2A	June 2015
2014.06a	3.23a	33_32_33_2A	June 2014
2013.05a	3.22b	33_32_32_2A	May 2013
2012.03a	3.22a	33_32_32_2A	March 2012
2011.11a	3.21b	33_32_31_2A	November 2011

DesignWare Release for AMBA 2	DW_apb_ssi Version	SSI_COMP_VERSION value	Databook Date
2011.10a	3.21a	33_32_31_2A	October 2011
2011.04a	3.20a	33_32_30_2A	April 2011
2010.12a	3.18a	33_31_38_2A	December 2010
2010.10a	3.17a	33_31_37_2A	October 2010
2010.09a	3.16a	33_31_36_2A	September 2010
2010.03a	3.15a	33_31_35_2A	March 2010
2009.06a	3.13a	33_31_33_2A	June 2009
2008.10a	3.12a	33_31_32_2A	October 2008
2008.06a	3.11c	33_31_31_2A	June 2008
2007.06a	3.11b	33_31_31_2A	June 2007
2007.04a	3.11a	33_31_31_2A	April 2007
2005.04a	3.10a	33_31_30_2A	July 26, 2005
2005.04	3.04a	33_30_34_2A	April 29, 2005
2004.11	3.03a	33_30_33_2A	November 2004
2004.06	3.02a	33_30_32_2A	August 11, 2004
2003.10	3.01a	33_30_31_2A	November 12, 2003
2003.10	3.00a	33_30_30_2A	October 20, 2003
2003.02	2.00a	32_30_30_41	March 26, 2003
2002.08-SP1-1	1.01b	31_30_31_42	October 25, 2002 (databook updated for patch release)
2002.08-SP1	1.01b	31_30_31_42	August 20, 2002
2002.08	1.01a	31_30_31_41	August 20, 2002

1.4.14.3 DW_apb_ssi Known Problems and Workarounds

There are no known issues in this release of the DW_apb_ssi.

1.4.15 DW_apb_timers

The following sections list the new features and changes, and the fixed problems and enhancements, for the DW_apb_timers component. For DW_apb_timers-specific STARs, refer to:

https://www.synopsys.com/dw/star.php?c=DW_apb_timers

For detailed features description, see the *DW_apb_timers databook*.

For information on known issues, refer to "DW_apb_timers Known Problems and Workarounds" on page 127.

1.4.15.1 DW_apb_timers New Features and Changes

This section describes what was new or changed during the various versions of the DW_apb_timers:

Changed in 2.13a version of DW_apb_timers

- RTL Changes:
  - Design compliance to SpyGlass Q-2020.03-SP1 and GuideWare 2020.03
  - Fixed:
    - STAR 9001539693: Fixed an issue when TIM_NEWMODE is set to 1 the read value is 32'hFFFF_FFFF - when the DW_apb_timers is in disabled state.
    - STAR 9001533989: Addressed a documentation issue where TIMER1EOI is shown as TIMERNEOI and RSVD_TimerNEOI, instead it has to be RSVD_Timer1EOI and TIMER1EOI. However, it is correct for any other value of N in the register TimerNEOI (for N = 1; N <= NUM_TIMERS).
- Documentation changes:
  - Refer to the Revision History chapter of the DW_apb_timers databook.
- Packaging changes:
  - STAR 3115176: Updated sWork::evalInComponent to align with coreTools version Q-2020.03-SP4-2
  - Minor packaging updates

Changed in 2.12a version of DW_apb_timers

- RTL Changes:
  - RTL compliance to SpyGlass 2017.12-SP1 and GuideWare 2017.12
  - Enhancement:
    - Added support for configurable synchronization depth through coreConsultant parameters TIM_SYNC_DEPTH_1, TIM_SYNC_DEPTH_2, TIM_SYNC_DEPTH_3, TIM_SYNC_DEPTH_4, TIM_SYNC_DEPTH_5, TIM_SYNC_DEPTH_6, TIM_SYNC_DEPTH_7, and TIM_SYNC_DEPTH_8.
- Documentation and/or coreTools changes:
  - Version update
  - Updated Synthesis results in the Integration Considerations chapter of the databook
  - Published the first version of DesignWare Synthesizable Components for AMBA 2 User Guide
  - Removed Chapter 2 "Building and Verifying a Component or Subsystem" from the databook and added the content in the newly created user guide

- Signals, Parameters, Registers and Internal parameters chapter auto-extracted with change bars from the RTL
- Uses coreTools version N-2017.12-SP2

- Packaging changes:
  - Minor packaging updates
- Removed support for NC Verilog Simulator and MTI Simulator

Changed in 2.11a version of DW_apb_timers

- RTL Changes:
  - Lint and CDC Cleanup
  - Enhancements:
    - APB3 and APB4 protocol
    - PWM duty cycle 0% and 100% modes
- Documentation and/or coreTools changes:
  - Version update
  - Parameter Descriptions and Register Descriptions chapters auto-extracted from the RTL
  - Removed references to Leda
  - Uses coreTools version 2016.09

Changed in 2.10a version of DW_apb_timers

- RTL Changes:
  - Lint and CDC Cleanup
- Documentation and/or coreTools changes:
  - Version update
  - Modified default value for TimerNCurrentValue
  - Signal Descriptions chapter auto-extracted from the RTL
  - Uses coreTools version 2014.12-SP1-1
- Packaging changes:
  - Minor packaging enhancements
  - Memory Map updates for defining access type to reserved fields

Changed in 2.09a version of DW_apb_timers

- RTL changes:
  - Lint cleanup
  - Corrected:

        - Behavior of RAW interrupt status register in TIM_NEWMODE =1
        - Toggle signal behavior in TIM_NEWMODE=1
    - Documentation and/or coreTools changes:
        - Updated:
            - Version
            - Section “Controlling Clock Boundaries and Metastability”
            - “Performance” section of “Integration Considerations” chapter
        - Added a new parameter INTR_SYNC2PCLK for interrupt synchronization
        - Uses coreTools version 2013.03-SP1-2
        - Corrected the External Input/Output Delay in the Signals chapter
    - Packaging changes:
        - Minor packing enhancements
        - IP-XACT enhancement for enumeration and display names
        - Corrected data description inconsistencies in RAL files

Changed in 2.08b version of DW_apb_timers

- RTL changes:
    - None
- Documentation and/or coreTools changes:
    - Updated the databook template
    - Uses coreTools version 2012.06-SP2
- Packaging changes:
    - Corrected file prefixing in the encrypted mode

Changed in 2.08a version of DW_apb_timers

- RTL changes:
    - Verified interrupt masking functionality
    - Corrected situation in which modification to timer loading caused erroneous behavior
- Documentation and/or coreTools changes:
    - None

Changed in 2.06c version of DW_apb_timers

- RTL changes:
    - RAL-related fix for generated XML/RAL files

- Documentation and/or coreTools changes:
  - None

Changed in 2.06b version of DW_apb_timers

- RTL changes:
  - Corrected inconsistencies in RAL files
- Documentation and/or coreTools changes:
  - None

Changed in 2.06a version of DW_apb_timers

- RTL changes:
  - Enhancement to replace clock domain synchonizer logic with standard BCM synchronizers
  - Enhancement to allow operation without pclk
- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.09-SP2

Changed in 2.05a version of DW_apb_timers

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.03 or later
  - Corrected names of include files and vcs command used for simulation in databook
  - Corrected syntax for undef directive

Changed in 2.03a version of DW_apb_timers

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2008.06-SP2-2

Changed in 2.02e version of DW_apb_timers

The following was new or changed in the 2.02e version of the DW_apb_timers:

- RTL changes:
  - None

- Documentation and/or coreTools changes:
  - Width for TimersIntStatus, TimersEOI, and TimersRawIntStatus register corrected
  - Width of Timers* registers corrected in memory map section
  - Uses coreTools version 2007.06-SP4

Changed in 2.02d version of DW_apb_timers

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2007.06-1 or later

Changed in 2.02c version of DW_apb_timers

- Enhanced databook includes coreAssembler intent in Chapter 2.
- The coreAssembler or coreConsultant GUIs can now be used to select VIP/VMT versions.
- Register descriptions are now included in SPIRIT files.
- TIMER_WIDTH corrected in databook for TIMER_WIDTH_1 and TIMER_WIDTH_*N* (where *N* = 1-8)
- Address offsets corrected for TimerNLoadCount, TimerNCurrenValue, TimerNControlReg, and TimerNEOI

Changed in 2.02b version of DW_apb_timers

- A new flow tutorial based on DesignWare Connect now comprises Chapter 2, "Building and Verifying a Component or Subsystem" of the *DesignWare DW_apb_timers Databook*.
- The DW_apb_timers can now be used in the coreTools 5.*x* environment.
- Enhanced databook includes coreAssembler intent in Chapter 2.
- The DW_apb_timers now supports the DC-FPGA environment.
- The size of the DesignWare Synthesizable Components image has been reduced to about 60 MB by removing the DesignWare Memory Model TSP and the QuickStart examples designs; these are now available through separate downloads. For more information, refer to the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide*.
- The DesignWare Synthesizable Components image is now self-extracting.

Changed in 2.02a version of DW_apb_timers

- Source code for this component is available on a per-project basis as a DesignWare Core. Please contact your local sales office for the details. For source licensing information, refer to "Licenses" in the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide*.

Changed in 2.01a version of DW_apb_timers

- DesignWare Connect – Enables you to construct, modify, and simulate any single- or multi-layer system in about an hour.
- The Verilog-XL simulator is not supported.
- The HP-UX platform is not supported.
- VHDL simulation is not supported.

Changed in 2.00b version of DW_apb_timers

- In the memory map, the name of the Version ID register, now known as the Component Version register, has changed from TIMERS_VERSION_ID to TIMERS_COMP_VERSION.

For a list of all the features of the DW_apb_timers, refer to the "Features" section of the *DesignWare DW_apb_timers Databook*.

1.4.15.2 DW_apb_timers Releases

Table 1-15 lists the latest versions of the DW_apb_timers component, the releases in which they were included, and the corresponding TIMERS_COMP_VERSION register values.

Table 1-15 DesignWare for AMBA 2/DW_apb_timers Releases

DesignWare Release for AMBA 2	DW_apb_timers Version	TIMERS_COMP_VERSION Value	Databook Date
2020.12a	2.13a	32_31_33_2A	December 2020
2018.07a	2.12a	32_31_32_2A	July 2018
2016.10a	2.11a	32_31_31_2A	October 2016
2015.06a	2.10a	32_31_30_2A	June 2015
2014.06a	2.09a	32_30_39_2A	June 2014
2013.05a	2.08b	32_30_38_2A	May 2013
2012.06a	2.08a	32_30_38_2A	June 2012
2012.03a	2.06c	32_30_36_2A	March 2012
2011.11a	2.06b	32_30_36_2A	November 2011
2011.10a	2.06a	32_30_36_2A	October 2011
2010.09a	2.05a	32_30_35_2A	September 2010
2009.06a	2.03a	32_30_33_2A	June 2009
2008.10a	2.03a	32_30_33_2A	October 2008
2008.06a	2.02e	32_30_32_2A	June 2008
2007.06a	2.02d	32_30_32_2A	June 2007

DesignWare Release for AMBA 2	DW_apb_timers Version	TIMERS_COMP_VERSION Value	Databook Date
2007.04a	2.02c	32_30_32_2A	April 2007
2005.04a	2.02b	32_30_32_2A	July 22, 2005
2004.11	2.02a	32_30_32_2A	November 2004
2004.06	2.01a	32_30_31_2A	July 2, 2004
2003.10	2.00b	32_30_30_2A	October 20, 2003
2003.02	2.00a	32_30_30_41	March 26, 2003
2002.08-SP1-1	1.02c	31_30_32_43	October 25, 2002
2002.08-SP1	1.01b	31_30_31_42	November 14, 2002
2002.08	1.01a	31_30_31_41	August 20, 2002

1.4.15.3 DW_apb_timers Known Problems and Workarounds

There are no known issues in this release of the DW_apb_timers.

1.4.16 DW_apb_uart

The following sections list the new features and changes, and the fixed problems and enhancements, for the DW_apb_uart component. For DW_apb_uart-specific STARs, refer to:

https://www.synopsys.com/dw/star.php?c=DW_apb_uart

For detailed features description, see the *DW_apb_uart databook*.

For information on known issues, refer to "DW_apb_uart Known Problems and Workarounds" on page 136.

1.4.16.1 DW_apb_uart New Features and Changes

This section describes what was new or changed during the various versions of the DW_apb_uart:

Changed in 4.03a version of DW_apb_uart

- RTL Changes:
  - Design compliance to SpyGlass Q-2020.03-SP1 and GuideWare 2020.03
- Documentation changes:
  - Refer to the Revision History chapter of the DW_apb_uart databook.
  - Updated the documentation for the LSR_STATUS_CLEAR usage for better understanding of the usage.
- Packaging changes:
  - STAR 3115176: Updated sWork::evalInComponent to align with coreTools version Q-2020.03-SP4-2
  - Minor packaging updates

Changed in 4.02a version of DW_apb_uart

- RTL Changes:
  - Design compliance to SpyGlass 2017.12-SP1 and GuideWare 2017.12
  - Fixed Defects:
    - STAR 9001187512: DW_apb_uart character timeout interrupt is active even after RBR read in CLOCK_MODE=1.
  - Enhancement:
    - STAR 9001171999: Support for the APB3.0 and APB4.0 protocol
    - Added support for configurable synchronization depth through coreConsultant parameter SYNC_DEPTH.
- Documentation and/or coreTools changes:
  - Version update
  - Updated Synthesis results in the Integration Considerations chapter of the databook
  - Published the first version of DesignWare Synthesizable Components for AMBA 2 User Guide

  - Removed Chapter 2 “Building and Verifying a Component or Subsystem” from the databook and added the content in the newly created user guide
  - Signals, Parameters, Registers and Internal parameters chapter auto-extracted with change bars from the RTL
  - Uses coreTools version N-2017.12-SP2
- Packaging changes:
  - Minor packaging updates
- Removed support for NC Verilog Simulator and MTI Simulator

Changed in 4.01a version of DW_apb_uart

- RTL Changes:
  - Lint and CDC Cleanup
  - Enhancements:
    - UART PE/FE/BI must not be cleared on reading RX FIFO and can clear only on an LSR read
    - dma_tx_req is not asserted on reset and waits till FCR is written
  - Fixed:
    - FIFO SW reset tied to async reset pin of TX/RX FIFO flops
    - Incorrect generation of Busy Signal in FIFO Access Mode
- Documentation and/or coreTools changes:
  - Version update
  - Parameter Descriptions and Register Descriptions chapters auto-extracted from the RTL
  - Removed references to Leda
  - Uses coreTools version 2016.09

Changed in 4.00a version of DW_apb_uart

- RTL Changes:
  - Lint and CDC Cleanup
  - Enhanced:
    - Support for RS485 Interface
    - Support for Fractional Baud Rate
    - Support for 9-bit serial data transfers
- Documentation and/or coreTools changes:
  - Version update
  - Signal Descriptions chapter auto-extracted from the RTL
  - Added:
    - Support for RS485 Interface

        - Support for Fractional Baud Rate
        - Support for 9-bit serial data transfers
        - Updated programming flow for RS485, Fractional Baud and 9-bit features.
    - Updated the "Performance" section in "Integration Considerations" chapter for RS485, Fractional Baud Rate and 9-bit features
    - Uses coreTools version 2014.12-SP1-1
- Packaging changes:
    - Minor packaging enhancements
    - Memory Map updates for defining access type to reserved fields

Changed in 3.15a version of DW_apb_uart

- RTL changes:
    - Lint cleanup
    - Modified the single-flop synchronization on reset-de-assertion to Double-flop synchronization to avoid Metastability condition for CLK_GATE_EN=1 configuration
- Documentation and/or coreTools changes:
    - Version update
    - Added "Performance" section in "Integration Considerations" chapter
    - Few minor mistakes corrected in databook
    - Uses coreTools version 2013.03-SP1-2
    - Corrected the Default Input/Output Delay in the Signals chapter
- Packaging changes:
    - Minor packing enhancements
    - IP-XACT enhancement for enumeration and display names
    - Corrected data description inconsistencies in RAL files

Changed in 3.14c version of DW_apb_uart

- RTL changes:
    - None
- Documentation and/or coreTools changes:
    - Corrected the de-assert sequence for reset signals in the DW_apb_uart databook
    - Corrected the label of the UART_ADD_ENCODED_PARAMS parameter in the DW_apb_uart databook and changed references to Component Identification register and Configuration Identification register to Component Parameter register in coreConsultant and in the databook.
    - Updated the databook template
    - Uses coreTools version 2012.06-SP2

- Packaging changes:
  - Corrected inconsistencies in RAL files
  - Corrected file prefixing in the encrypted mode

Changed in 3.14b version of DW_apb_uart

- RTL changes:
  - Added new feature RTC Flow Trigger threshold level, which uses independent thresholds for DMA Request and handshake signal (rts_n)
  - Replaced flip-flop-based synchronizer with BCM synchronizers
- Documentation and/or coreTools changes:
  - Added new RTC_FCT coreConsultant parameter

Changed in 3.13a version of DW_apb_uart

- RTL changes:
  - Fixed mismatch between RAL/XML/databook for MSR[3:0] register bits
  - Fixed problem in which value of MSR[3:2] changes to 1 after reset without any change on dcd_n or ri_n
  - Corrected description of DLH register in RAL, header, Register Map files
  - Fixed problem in which TET and RT descriptions in IIR register contain non-ASCII characters
  - Updated CPR register description
- Documentation and/or coreTools changes:
  - Enhanced timing information for serial clock modules
  - Corrected reset values for MSR[3:0] bits
  - Added note to write MCR before LCR for SIR mode

Changed in 3.12c version of DW_apb_uart

- RTL changes:
  - Corrected inconsistencies in RAL files
- Documentation and/or coreTools changes:
  - None

Changed in 3.12b version of DW_apb_uart

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.09-SP2

Changed in 3.12a version of DW_apb_uart

- RTL changes:
  - Added Stick Parity feature
- Documentation and/or coreTools changes:
  - Updated material for Stick Parity bit of Line Control Register; updated system graphic in Figure 1-1

Changed in 3.11a version of DW_apb_uart

- RTL changes:
  - Undeclared nets now identified and declared before being used
  - Fix made to avoid leaving input of DW_apb_uart_regfile or DW_apb_uart_sync floating when FIFO_MODE=0 and CLK_GATE_EN=0
  - Corrected clock domain crossing violations (combinational logic before synchronization flip-flops)
  - Corrected timeout interrupt generation for sclk frequencies 4x or more lower than pclk
  - Added C headers to component package
  - Corrected data loss in data synchronizer module
  - Corrected conditions that cause false overrun error if RBR is read as Rx completes
  - Fixed C and Verilog header files that were missing address offset for some registers
- Documentation and/or coreTools changes:
  - Corrected description of APB_DATA_WIDTH parameter
  - Added sections for “Potential Deadlock Conditions in DW_apb_uart/DW_ahb_dmac Systems” and “Reset Signals”
  - Edited descriptions for Parity Error and Framing Error bits in LSR register.
  - Corrected dma* signals in Figure 3-25
  - Added register in acknowledge page in “RTL Diagram of Data Synchronization Module” diagram

Changed in 3.10a version of DW_apb_uart

- RTL changes:
  - Enhanced packaging to prevent illegal default component connections
  - Updated packaging to change name of user-visible auto-flow control parameter to AFCE_MODE to match databook
- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.03 or later
  - Enhanced USR[0] busy description in databook to explain non-busy conditions

- Corrected synchronous description from "pclk" to "N/A" for cts_n, dsr_n, dcd_n and ri_n signals
- Added syntax for include files in database tables
- Added +v2k option in vcs command syntax
- Added information for back-to-back character stream transmission
- Corrected flow control diagram describing operation of component
- Corrected names of include files and vcs command used for simulation in databook
- Corrected syntax for undef directive
- Updated the ADDITIONAL_PARAMETERS description

Changed in 3.08a version of DW_apb_uart

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2008.06-SP2-2

Changed in 3.07b version of DW_apb_uart

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Correction in description of MSR register
  - Uses coreTools version 2007.06-SP4

Changed in 3.07a version of DW_apb_uart

- RTL changes:
  - A change was made to the timing of the Line Status Interrupt, which now asserts one cycle earlier to match the timing of the RX Data Available Interrupt.
- Documentation and/or coreTools changes:
  - Corrected a waveform in Figure 8.
  - Updated release notes to match the version number in the UART_COMP_VERSION RTL parameter.

Changed in 3.06b version of DW_apb_uart

- RTL changes:
  - None

- Documentation and/or coreTools changes:
  - Uses coreTools version 2007.06-1 or later

Changed in 3.06a version of DW_apb_uart

- Enhanced databook includes coreAssembler intent in Chapter 2.
- The coreAssembler or coreConsultant GUIs can now be used to select VIP/VMT versions.
- Register descriptions are now included in SPIRIT files.
- Enhanced databook to specify that in LP IrDA mode, sclk frequency must always be a multiple of 1.8432 MHz in order to achieve the 115.2K baud requirement
- Bit 1 of FCR register now resets control portion of receive FIFO and de-asserts DMA RX request in same clock cycle

Changed in 3.05a version of DW_apb_uart

- Added the UART_16550_COMPATIBLE parameter in order to allow the UART to be configured without the busy functionality.
- Enhanced databook includes coreAssembler intent in Chapter 2.

Changed in 3.04a version of DW_apb_uart

- Added support for IrDA 1.0 SIR low-power reception capabilities (fixed STAR 9000090005).
- Value for UCV register corrected in release notes.

Changed in 3.03a version of DW_apb_uart

- Fixed STAR 9000073306, regarding the transmit holding register empty (THRE) interrupt after it has been cleared by reading the Interrupt Identity Register for the same empty status.
- Fixed STAR 9000071348, concerning the use of a reserved word in System Verilog that caused an error during simulations.

Changed in 3.02a version of DW_apb_uart

- A new flow tutorial based on DesignWare Connect now comprises Chapter 2, "Building and Verifying a Component or Subsystem" of the *DesignWare DW_apb_uart Databook*.
- The DW_apb_uart can now be used in the coreTools 5.*x* environment.
- The DW_apb_uart now supports the DC-FPGA environment.
- The size of the DesignWare Synthesizable Components image has been reduced to about 60 MB by removing the DesignWare Memory Model TSP and the QuickStart examples designs; these are now available through separate downloads. For more information, refer to the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide*.
- The DesignWare Synthesizable Components image is now self-extracting.

Changed in 3.01a version of DW_apb_uart

- Source code for this component is available on a per-project basis as a DesignWare Core. Please contact your local sales office for the details. For source licensing information, refer to "Licenses" in the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide*.
- The DW_apb_uart Driver Kit is available, which allows you to easily program the DW_apb_uart and integrate it into your higher-level application. For information about the DW_apb_uart Driver Kit, refer to the *DesignWare DW_apb_uart Driver Kit User Guide.*

Changed in 3.00a version of DW_apb_uart

The following was new or changed in the 3.00a version of the DW_apb_uart.

- The DW_apb_uart supports source licensing and has a number of new signals, parameters and registers.
- DesignWare Connect – Enables you to construct, modify, and simulate any single- or multi-layer system in about an hour.
- Previous versions of the DW_apb_uart (2.00e and earlier) used two coreConsultant parameters to set the periods of the sclk and pclk. The new 3.00a version of the DW_apb_uart doesn't need these parameters because the clock periods are now defined in the "Specify Clock" step in coreConsultant, which coincides with the methodology used by other Synopsys IP components. These legacy parameters are still included in the coreConsultant constants file for the 3.00a version of the DW_apb_uart so that legacy scripts that you may have from earlier versions runs without error.
- The HP-UX platform is not supported.
- VHDL simulation is not supported.

1.4.16.2 DW_apb_uart Releases

Table 1-16 lists the latest versions of the DW_apb_uart component, the releases in which they were included, and the corresponding UCV register values.

Table 1-16 DesignWare for AMBA 2/DW_apb_uart Releases

DesignWare Release for AMBA 2	DW_apb_uart Version	UCV Value	Databook Date
2020.12a	4.03a	34_30_33_2A	December 2020
2018.07a	4.02a	34_30_32_2A	July 2018
2016.10a	4.01a	34_30_31_2A	October 2016
2015.06a	4.00a	34_30_30_2A	June 2015
2014.06a	3.15a	33_31_35_2A	June 2014
2013.05a	3.14c	33_31_34_2A	May 2013
2012.06a	3.14b	33_31_34_2A	June 2012

DesignWare Release for AMBA 2	DW_apb_uart Version	UCV Value	Databook Date
2012.03a	3.13a	33_31_33_2A	March 2012
2011.11a	3.12c	33_31_32_2A	November 2011
2011.10a	3.12b	33_31_32_2A	October 2011
2011.06a	3.12a	33_31_32_2A	June 2011
2011.04a	3.11a	33_31_31_2A	April 2011
2010.09a	3.10a	33_31_30_2A	September 2010
2009.06a	3.08a	33_30_38_2A	June 2009
2008.10a	3.08a	33_30_38_2A	October 2008
2008.06a	3.07b	33_30_37_2A	June 2008
2007.12a	3.07a	33_30_37_2A	December 2007
2007.06a	3.06b	33_30_36_2A	June 2007
2007.04a	3.06a	33_30_36_2A	April 2007
2005.04a	3.05a	33_30_35_2A	June 9, 2006
2005.04a	3.04a	33_30_34_2A	January 20, 2006
2005.04a	3.03a	33_30_33_2A	July 7, 2005
2005.04a	3.02a	33_30_32_2A	April 29, 2005
2004.11	3.01a	—	November 2004
2004.06	3.00a	—	Updated: August 26, 2004
2003.10	2.00e	—	October 20, 2003
2003.02	2.00d	—	March 27, 2003
2002.08-SP1	2.0c	—	November 14, 2002
2002.08	2.0a	—	August 20, 2002

1.4.16.3 DW_apb_uart Known Problems and Workarounds

The following are known issues in this release of the DW_apb_uart:

- Error: Not enough memory for new VM_code using NC-Verilog or MTI-Verilog on Linux O/S.

  Description: This problem is caused by the Linux BigMem (BM) patch on Linux systems in RH 7, 8 or E3.0, which limit dynamically linked libraries to about 100MB in size. Additional linked libraries required for the DW_apb_uart Driver can exceed this limit, and prevent the Vera dynamic library from loading.

Workaround 1: Switch off bus monitors (“monitor = OFF” makefile argument) if verification monitors are not needed. This workaround may not work if software Driver option is used.

Workaround 2: Use a Linux machine that does not have the BM patch applied.

1.4.17 DW_apb_wdt

The following sections list the new features and changes, and the fixed problems and enhancements, for the DW_apb_wdt component. For DW_apb_wdt-specific STARs, refer to:

http://www.synopsys.com/dw/star.php?c=DW_apb_wdt

For detailed features description, see the *DW_apb_wdt databook*.

For information on known issues, refer to "DW_apb_wdt Known Problems and Workarounds" on page 143.

1.4.17.1 DW_apb_wdt New Features and Changes

This section describes what was new or changed during the various versions of the DW_apb_wdt:

Changed in 1.12a version of DW_apb_wdt

- RTL Changes:
  - Design compliance to SpyGlass Q-2020.03-SP1 and GuideWare 2020.03
- Documentation changes:
  - Refer to the Revision History chapter of the DW_apb_wdt databook.
- Packaging changes:
  - STAR 3115176: Updated sWork::evalInComponent to align with coreTools version 2018.09-SP2 and later
  - STAR 3328634: Fixed a packaging issue where pclk time period is used instead of tclk time period in set_max_delay constraint.
  - STAR 9001498624: Enhanced packaging to have unique registers and parameters names.
  - Minor packaging updates

Changed in 1.11a version of DW_apb_wdt

- RTL Changes:
  - Design compliance to SpyGlass 2017.12-SP1 and GuideWare 2017.12
  - Enhancement:
    - Added support for configurable synchronization depth through coreConsultant parameter WDT_ASYNC_CLK_SYNC_DEPTH.
- Documentation and/or coreTools changes:
  - Version update
  - Updated Synthesis results in the Integration Considerations chapter of the databook
  - Published the first version of DesignWare Synthesizable Components for AMBA 2 User Guide
  - Removed Chapter 2 "Building and Verifying a Component or Subsystem" from the databook and added the content in the newly created user guide

- Signals, Parameters, Registers and Internal parameters chapter auto-extracted with change bars from the RTL
- Uses coreTools version N-2017.12-SP2

- Packaging changes:
  - Register memory map updates to reflect proper memory access for register fields
  - Minor packaging updates
- Removed support for NC Verilog Simulator and MTI Simulator

Changed in 1.10a version of DW_apb_wdt

- RTL Changes:
  - Lint and CDC Cleanup
  - Enhancements:
    - System Reset generation after Second timeout
    - APB3 and APB4 protocol support
  - Fixed:
    - WDT_COMP_PARAM_1.CP_WDT_PAUSE remains 0 even if WDT_PAUSE parameter is selected
- Documentation and/or coreTools changes:
  - Version update
  - Parameter Descriptions and Register Descriptions chapters auto-extracted from the RTL
  - Removed references to Leda
  - Uses coreTools version 2016.09
  - Added following sections:
    - Support for AMBA APB3 and AMBA APB4 Protocols
    - System Restart

Changed in 1.09a version of DW_apb_wdt

- RTL Changes:
  - Lint and CDC Cleanup
- Documentation and/or coreTools changes:
  - Version update
  - Signal Descriptions chapter auto-extracted from the RTL
  - Uses coreTools version 2014.12-SP1-1
- Packaging changes:
  - Minor packaging enhancements
  - Memory Map updates for defining access type to reserved fields

Changed in 1.08a version of DW_apb_wdt

- RTL changes:
  - Lint cleanup
- Documentation and/or coreTools changes:
  - Version update
  - Added "Performance" section in "Integration Considerations"
  - Uses coreTools version 2013.03-SP1-2
  - Corrected the External Input/Output Delay in the Signals chapter
- Packaging changes:
  - Minor packing enhancements
  - IP-XACT enhancement for enumeration and display names

Changed in 1.07d version of DW_apb_wdt

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Made a minor correction in the description of WDT_EN bit of the WDT_CR register.
  - Updated the databook template
  - Uses coreTools version 2012.06-SP2
- Packaging changes:
  - Corrected file prefixing in the encrypted mode

Changed in 1.07c version of DW_apb_wdt

- RTL changes:
  - Fixed mismatch between RAL/XML/databook for WDT_COMP_PARAMS_1 register
- Documentation and/or coreTools changes:
  - None

Changed in 1.07b version of DW_apb_wdt

- RTL changes:
  - Corrected inconsistencies in RAL files
- Documentation and/or coreTools changes:
  - None

Changed in 1.07a version of DW_apb_wdt

- RTL changes:
  - Enhancement to replace clock domain synchonizer logic with standard BCM synchronizers
  - Added support for asynchronous clocks
- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.09-SP2
  - Added material for newly supported asynchronous clocks

Changed in 1.06a version of DW_apb_wdt

- RTL changes:
  - Corrected errors generated by coreTools for illegal configurations instead of silent corrections
- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.03 or later
  - Corrected Figure 7-1 of databook
  - Corrected paddr[4:0] description in databook
  - Corrected names of include files and vcs command used for simulation in databook
  - Corrected syntax for undef directive

Changed in 1.04a version of DW_apb_wdt

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2008.06-SP2-2

Changed in 1.03e version of DW_apb_wdt

- RTL changes:
  - Redundant bit removed from WDT_CR register
- Documentation and/or coreTools changes:
  - Uses coreTools version 2007.06-SP4
  - Clarification to dependencies of parameter WDT_USER_TOP_(i)

Changed in 1.03d version of DW_apb_wdt

- RTL changes:
  - None

- Documentation and/or coreTools changes:
  - Uses coreTools version 2007.06-1 or later

Changed in 1.03c version of DW_apb_wdt

- Enhanced databook includes coreAssembler intent in Chapter 2.
- The coreAssembler or coreConsultant GUIs can now be used to select VIP/VMT versions.
- Register descriptions are now included in SPIRIT files.

Changed in 1.03b version of DW_apb_wdt

- A new flow tutorial based on DesignWare Connect now comprises Chapter 2, "Building and Verifying a Component or Subsystem" of the *DesignWare DW_apb_wdt Databook*.
- The DW_apb_wdt can now be used in the coreTools 5.*x* environment.
- Enhanced databook includes coreAssembler intent in Chapter 2.
- The DW_apb_wdt now supports the DC-FPGA environment.
- The size of the DesignWare Synthesizable Components image has been reduced to about 60 MB by removing the DesignWare Memory Model TSP and the QuickStart examples designs; these are now available through separate downloads. For more information, refer to the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide*.
- The DesignWare Synthesizable Components image is now self-extracting.

Changed in 1.03a version of DW_apb_wdt

- Source code for this component is available on a per-project basis as a DesignWare Core. Please contact your local sales office for the details. For source licensing information, refer to "Licenses" in the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide*.

Changed in 1.02a version of DW_apb_wdt

- DesignWare Connect – Enables you to construct, modify, and simulate any single- or multi-layer system in about an hour.
- The Verilog-XL simulator is not supported.
- The HP-UX platform is not supported.
- VHDL simulation is not supported.

Changed in 1.01a version of DW_apb_wdt

- Several new component parameter registers (WDT_COMP_PARAMS_n) were added to the memory map; these registers allow software to query the configuration of the device.
- The redundant WDT_VID register was removed. Use the WDT_COMP_VERSION register to obtain the component version.

For a list of all the features of the DW_apb_wdt, refer to the "Features" section of the *DesignWare DW_apb_wdt Databook*.

1.4.17.2 DW_apb_wdt Releases

Table 1-17 lists the latest versions of the DW_apb_wdt component, the releases in which they were included, and the corresponding WDT_COMP_VERSION register values.

Table 1-17 DesignWare for AMBA 2/DW_apb_wdt Releases

DesignWare Release for AMBA 2	DW_apb_wdt Version	WDT_COMP_VERSION Register Value	Databook Date
2020.12a	1.12a	31_31_32_2A	December 2020
2018.07a	1.11a	31_31_31_2A	July 2018
2016.10a	1.10a	31_31_30_2A	October 2016
2015.06a	1.09a	31_30_39_2A	June 2015
2014.06a	1.08a	31_30_38_2A	June 2014
2013.05a	1.07d	31_30_37_2A	May 2013
2012.03a	1.07c	31_30_37_2A	March 2012
2011.11a	1.07b	31_30_37_2A	November 2011
2011.10a	1.07a	31_30_37_2A	October 2011
2010.09a	1.06a	31_30_36_2A	September 2010
2009.06a	1.04a	31_30_34_2A	June 2009
2008.10a	1.04a	31_30_34_2A	October 2008
2008.06a	1.03e	31_30_33_2A	June 2008
2007.06a	1.03d	31_30_33_2A	June 2007
2007.04a	1.03c	31_30_33_2A	April 2007
2005.04a	1.03b	31_30_33_2A	April 2005
2004.11	1.03a	31_30_33_2A	November 2004
2004.06	1.02a	31_30_32_2A	June 21, 2004
2003.10	1.01a	31_30_31_2A	October 21, 2003
2003.02	1.00a	31_30_30_41	March 26, 2003

1.4.17.3 DW_apb_wdt Known Problems and Workarounds

There are no known issues in this release of the DW_apb_wdt.

2 AMBA 3 AXI/AMBA 4 AXI Release Notes

This chapter presents the latest release information about the DesignWare components for AMBA 3 AXI/AMBA 4 AXI.

2.1 STARs on the Web

You can view problem reports for components used in this release, including problems identified after product release, by accessing the STAR report on the Web. Note that you must have a SolvNetPlus ID in order to view STAR reports. You can access STAR reports for any verification or synthesizable IP component through the IP Directory:

http://www.synopsys.com/dw/ipsearch.php

2.2 Global AMBA 3 AXI/AMBA 4 AXI New Features and Changes

The following was new or had changed during various versions of DesignWare Synthesizable Components for AMBA 3 AXI/AMBA 4 AXI.

Changes in 2020.03a

- Updated all AXI components
- Uses coreTools version P-2019.06-SP3

Changes in 2018.02a

- Updated all AXI components:
- Removed support for NC Verilog Simulator and MTI Simulator
- Uses coreTools version N-2017.12-SP1-3

Changes in 2016.03a

- Updated all AXI components:
- Uses coreTools version 2015.06-SP3-1

Changes in 2014.10a

- Added the new DW_axi_dmac component
- Updated all AXI components:
- Uses coreTools version 2014.03-SP1-1

Changes in 2013.06a

- Updated components:
  - DW_axi
  - DW_axi_a2x
  - DW_axi_gm
  - DW_axi_gs
  - DW_axi_rs
  - DW_axi_x2h
  - DW_axi_x2p
- Uses coreTools version 2013.03-SP1-1

Changes in 2013.05a

- Updated components:
  - DW_axi
  - DW_axi_a2x
  - DW_axi_gm
  - DW_axi_gs
  - DW_axi_hmx
  - DW_axi_x2h
  - DW_axi_x2p

- Uses coreTools version 2012.06-SP2

Changes in 2012.01a

- Added a new DW_axi_a2x component

Changes in 2011.10a

- Updated all AXI components:
- Uses coreTools version 2010.09-SP2

Changes in 2011.01a

- Updated components:
  - DW_axi
  - DW_axi_gm
  - DW_axi_gs
  - DW_axi_x2h
  - DW_axi_x2p
  - DW_axi_x2x
- Updated copyright headers for all components in the release for 2011

Changes in 2010.11a

- Updated the following components:
  - DW_axi
  - DW_axi_x2p
  - DW_axi_x2x

Changes in 2010.09a

- Updated all components
- Packaging now associates SPIRIT memory map of each component with relevant interface of component
- Description field of SPIRIT .xml memory map description of each component reviewed to remove variable and unnecessary information
- All component simulations now generate .vpd dump files
- Simulation scripts enhanced to supported new versions of VCS
- All components reviewed to ensure DW licenses pulled only if a source licence is not present
- Unnecessary Design Compiler scripts removed from all components
- Unconnected sub-module input and output ports removed from all components

- Defunct DesignWare connect scripts removed from AXI image
- Internal Design Compiler script changed from Design Compiler shell to Design Compiler TCL
- Input/Output section of all databooks reviewed to correct “Registered” description
- Moved to coreTools 2010.03-SP1-1
- Added AXI protocol, low-power handshaking interface for the following components:
  - DW_axi
  - DW_axi_gm
  - DW_axi_gs
  - DW_axi_x2h
  - DW_axi_x2p
  - DW_axi_x2x

Changes in 2010.04a

- Updated components:
  - DW_axi
  - DW_axi_x2p

Changes in 2010.02a

- Updated components:
  - DW_axi
  - Moved to coreTools 2009.06-SP1-1

Changes in 2009.08a

- Updated components:
  - DW_axi

Changes in 2009.07a

- Updated components:
  - DW_axi

Changes in 2009.03a

- Updated components:
  - DW_axi
  - DW_axi_rs
  - DW_axi_x2p
  - DW_axi_x2x

Changes in 2009.01a

- Updated components:
  - DW_axi
  - DW_axi_gs
  - DW_axi_hmx
  - DW_axi_x2x

Changes in 2008.12a

- Updated components:
  - DW_axi
- *DesignWare for AMBA 2 QuickStart_MultiLayer Guide* and *DesignWare for AMBA 2 QuickStart_SingleLayer Guide* are no longer supported

Changes in 2008.10a

- Updated components:
  - All AMBA 2 components
- RTL changes:
  - Added STAR-on-the-Web (SotW) note on Tetramax
  - Corrected coreConsultant and coreAssembler link to common release notes
  - Uses coreTools version 2008.06-SP2-2

Changes in 2008.06a

- Updated components:
  - All AMBA 3 AXI components
- Uses coreTools version 2007.06-SP4

Changes after 2007.10a

After the 2007.10a version of DesignWare Synthesizable Components for AMBA 3 occurred:

- All AMBA 2.0 and AMBA 3 AXI release notes were consolidated into this single release notes document.
- The "Global Issues for 2007.10a Release of AMBA 3 AXI" section was removed from the *DesignWare Synthesizable Components for AMBA 2, AMBA 3 AXI, and AMBA 4 AXI Installation Guide* for the 2008.02 release of AMBA 2.

Changes in 2007.10a

- Multi-cycle arbitration was added to the DW_axi component; associated parameters were added to the coreConsultant GUI.

- An additional subsection was made to the DW_axi databook for the multi-cycle arbitration options.
- Individual product release notes have been consolidated in this release notes document, and the databooks now link to this document.

Changes in 2007.08a

- New Pipeline Channel Arbiter and External Register Slice functionalities were added to the component, and corresponding parameters were added to the coreConsultant GUI.
- Additions were made to the databook for the Forward Registered and Fully Registered timing mode options. Additional subsections were added for the new Pipeline Channel Arbiter and External Register Slice functionalities.

Changes in 2007.07a

- STAR 9000186649 enhances the HMX_BLOCK_WRITE parameter in the DW_axi_hmx in order to allow strong ordering for read/write sequence when the same address is targeted. The "Block Writes" section in the databook has been changed to "Transaction Blocking," which describes the new functionality of this parameter.

Changes in 2007.06a

- Update to use coreTools 2007.06-1 or later

Changes in 2007.04a

- Update to use coreTools 2006.03-SP5

Changes in 2007.02a

- New component: DW_axi_x2x (AXI-to-AXI bridge, including frequency adaptation, data width adaptation and endian conversion)
- Increased the number of outstanding transactions supported by DW_axi
- Added bi-directional command support for DW_axi
- Updated component configuration parameters to have a common set of supported AXI configurations (addr width, data width, burst length, ID width)
- coreAssembler flow in Chapter 2 of all AMBA 3 AXI databooks

Changes in 2006.10a

- New component: DW_axi_x2p (bridge connecting an AXI subsystem to an APB 3.0 subsystem)
- DW_axi updated to fix illegal verilog statement and simulation failures with support Vera and VCS versions.

Changes in 2006.07b

- DW_axi_hmx (single AHB master to DW_axi or any AXI slave) .run file updated for source license correction

Changes in 2006.07a

- New component: DW_axi_hmx (single AHB master to DW_axi or any AXI slave)

Changes in 2006.05a

- DW_axi updated to fix potential deadlock issue

Changes in 2006.04a

- Full coreAssembler support, including subsystem creation, auto-connection of AXI/AHB buses, and automatic subsystem testing
- New component: DW_axi_rs (Register Slice)
- DW_axi feature updates, including locked access support and timing mode options
- Updated support for newer tools and DesignWare Verification IP
- AXI interface definitions 2.0 support

2.3 Known Global AMBA 3 AXI/AMBA 4 AXI Issues and Workarounds

The following are known global issues and workarounds for this AMBA 3 AXI/AMBA 4 AXI release:

- When using coreAssembler, if a DW_axi instance is connected to another DW_axi instance—known as interconnect tiling—automatic Interface Parameter inheritance does not occur. During the Add Subsystem Components activity, the DW_axi Interface Parameters for all tiled DW_axi instances must be manually configured to be consistent.
- In the coreAssembler for AXI components, if the user configures the subsystem for AXI4, then automatic parameter propagation for QoS and Region signals do not happen. The user must access the “Configure Components” tab in coreAssembler to manually enable/disable QoS and Region for individual components.
- When the USE_FOUNDATION parameter is set to True, the coreConsultant activity “Run VCS XPROP Analyzer” might give XPROP instrumentation percentage less than 100%. The DesignWare Building Block used in this case (DW_minmax.v) is only a simulation model. Hence, it can be ignored.
- The following DW_axi parameter values in Table 2-1 are not globally supported by all other DW_axi_* components. Use the following table to help determine which parameter values are available for your specific subsystem.
- When using coreAssembler, if a DW_axi_x2h AHB Master port is connected to DW_axi_hmx AHB Master port without AHB LITE is enabled in the DW_axi_x2h (X2H_AHB_LITE=0). Then there will be a mismatch, as there is no hgrant in the DW_axi_hmx and but DW_axi_x2h has mhgrant. In this scenario, the following error occurs:

  Information: Auto-connect subsystem design: start (0%) (CMDS-243)

  Error: Interface port '/i_axi_hmx/AHB_Master/hgrant' with association '<open>' has no design port linkage but a design port is required. (INTF-54)

  Warning: Reason is an interface versus design mismatch inside component 'i_axi_hmx'. (INTF-40)

Warning: No connection made between provider interface port '/i_axi_hmx/AHB_Master/hgrant' (<open>) and consumer interface port '/i_axi_x2h/AHB_Master/hgrant' (mhgrant) due to recently reported error. (INTF-49)

Error: Aborting Auto-Connect: Did not create any connections.

Use error_info for more info. (CMD-013)

In order to make them consistent, set_interface_port_attribute <DW_axi_hmx instance name>/AHB_Master hgrant DefaultConstantPort one (for example, set_interface_port_attribute i_axi_hmx/AHB_Master hgrant DefaultConstantPort one) command has to be run manually on the coreAssembler, which creates the connection ".mhgrant (1'b1)" for DW_axi_x2h in the subsystem.

Table 2-1 DesignWare AXI Component Parameter Inconsistencies

Component	Address Width (bits)	Data Width (bits)	Burst Length Width (bits)	ID Width (bits)	Sideband Support
DW_axi	32 to 64	8, 16, 32, 64, 128, 256, 512	4 to 8	1 to 12 Master Port ID 1 to 20 Slave Port ID	Yes (1 to 256)
DW_axi_a2x	32 to 64	8, 16, 32, 64, 128, 256, 512, 1024	4 to 8	1 to 16	Yes (1 to 256)
DW_axi_gs	32 to 64	8, 16, 32, 64, 128, 256, 512	4 to 8	1 to 16	Yes (1 to 256)
DW_axi_gm	32 to 64	8, 16, 32, 64, 128, 256, 512	4 to 8	1 to 12	Yes (1 to 256)
DW_axi_hmx	32 to 64	8, 16, 32, 64, 128, 256, 512	4 to 8	1 to 12	No
DW_axi_rs	32 to 64	8, 16, 32, 64, 128, 256, 512	4 to 8	1 to 16	Yes (1 to 256)
DW_axi_x2h	32 to 64	32, 64, 128, 256	4	1 to 16	No
DW_axi_x2p	32 to 64	8, 16, 32, 64, 128, 256, 512	4 to 8	1 to 16	No
DW_axi_x2x	32 to 64	8, 16, 32, 64, 128, 256, 512	4 to 8	1 to 16	Yes (1 to 64)
DW_axi_dmac	32 to 64	32, 64, 128, 256, 512	4 to 8	1 to 12	No

2.4 Individual AMBA 3 AXI/AMBA 4 AXI Component Release Notes

The following subsections contain the latest component-specific information about the individual AMBA 3 AXI/AMBA 4 AXI components.

2.4.1 DW_axi

The following sections list the new features and changes, and the fixed problems and enhancements, for the DW_axi component. For DW_axi-specific STARs, refer to:

https://www.synopsys.com/dw/star.php?c=DW_axi

For detailed features description, see the *DW_axi databook*.

For information on known issues, refer to "DW_axi Known Problems and Workarounds" on page 166.

2.4.1.1 DW_axi New Features and Changes

This section describes what was new or had changed during the various versions of the DW_axi:

Changes in 4.04a version of DW_axi

- RTL Changes:
  - Design compliance to SpyGlass 2019.06-SP2 and GuideWare 2019.06
  - Fixed Issue:
    - STAR 9001485484: IP-XACT generated from coreConsultant is failing in coreAssembler because of an improperly defined label for the AXI_PRIORITY_M* parameters. The label text includes a "}" as part of the label. This issue has been fixed.
- Documentation changes:
  - Refer to the Revision History of the DW_axi databook.
- Packaging changes:
  - STAR 3115176: Updated sWork::evalInComponent to align with coreTools version 2018.09-SP2
  - Minor packaging updates

Changes in 4.03a version of DW_axi

- RTL changes:
  - RTL compliance to SpyGlass 2017.03-SP-1 and GuideWare 2017.03
  - Fixed Defects
    - STAR 9001129396: An RTL issue in which signals enable_i and init_n_i are missing from the port list of DW_axi_arb_user module. This causes problem when user instantiates his own arbiter, which makes use of these signals.
  - Enhancements
    - STAR 9001080101: Early write data support. This feature enables the DW_axi to support masters that issue early write data in all AXI configurations.
    - STAR 9001299220: In forward timing mode, the clock gating efficiency is improved by considering the valid signal for loading payload. Read data toggling efficiency is improved.
- Documentation and/or coreTools changes:
  - Version update
  - Updated synthesis results in Integration Considerations chapter of the databook
  - Published the first version of DesignWare Synthesizable Components for AMBA 3 AXI, and AMBA 4 AXI user guide
  - Removed chapter 2 Building and Verifying a Component or Subsystem from the databook and added the content in the newly created user guide
  - Signals, Parameters, Registers and Internal Parameters chapters auto-extracted with change bars from the RTL
  - Uses coreTools version N-2017.12-SP1-3
- Packaging changes:
  - STAR 9001058881: An issue in the packaging due to which the generated RALF file is not reflecting the base address offset selected through the AXI_IC_REG_BASE_ADDR parameter.
  - Minor packaging enhancements
- Removed support for NC Verilog Simulator and MTI Simulator

Changes in 4.02a version of DW_axi

- RTL changes:
  - Lint cleanup
  - Fixed issue related to bus width of “act_ids_buffer_pointer” that was causing issues in the FPGA implementation
  - Fixed issue related to AXI QOS arbitration
- Documentation and/or coreTools changes:
  - Version update
  - Signals chapter auto-extracted from the RTL

- Parameters chapter auto-extracted from the RTL
- Registers chapter auto-extracted from the RTL
- Databook is updated to mention that the AWID and slave number are stored in the lookup table when a DW_axi master port receives a write command.
- Uses coreTools version 2015.06-SP3-1
- Updated the performance section in the Integration Consideration chapter

- Packaging changes:
  - Minor packaging enhancements

Changes in 4.01a version of DW_axi

- RTL changes:
  - Lint cleanup
  - Fixed issue of missing single beat write transfer while coming out of Low power in AXI4 mode
  - Fixed the problem of HwConfigReg[2] AXI4En register bit tied to 1'b0 even if the AXI4 interface selected
- Documentation and/or coreTools changes:
  - Version update
  - Slave memory map is updated to 64 bits
  - Uses coreTools version 2014.03-SP1-1
  - Updated the performance section in the Integration Considerations chapter
  - Updated the Shared Layer to Dedicated Layer Link section
  - Updated the data book to include the following note:

    AXI_REG_AW_W_PATHS=0 is NA for slaves visible to multiple masters
- Packaging changes:
  - Minor packing enhancements
  - IP-XACT enhancement for enumeration and display names

Changes in 4.00a version of DW_axi

- RTL changes:
  - Implemented support for the AMBA 4 AXI and ACE-Lite interface
  - Added QoS, user, and region signals in the AMBA 4 AXI and ACE-Lite mode
  - Added snoop, domain, and barrier signals in the ACE-Lite mode
- Documentation and/or coreTools changes:
  - Updated the databook with new signals and parameters added in the AMBA 4 AXI andACE-Lite mode
  - Enhanced the section on SystemVerilog Test Environment
  - Uses coreTools version 2013.03-SP1-1
- Packaging changes:
  - None

Changes in 3.01a version of DW_axi

- RTL changes:
  - Added a Quality of Service (QoS) controller, along with required signals and parameters
  - Enhanced the maximum limit of the AXI_MAX_URIDA_M(x) and AXI_MAX_UWIDA_M(x) parameters
  - Enhanced sideband signal width to 256 bits
  - Enhanced the maximum limit of the AXI_MAX_FARC_S(j), AXI_MAX_FAWC_S(j), AXI_MAX_RCA_ID_M(i), and AXI_MAX_WCA_ID_M(i) parameters.
  - Corrected errors in the code that prevented priority from being assigned for the master port arbiter on the read data and write response channels.
  - Fixed the code to avoid a bus width mismatch.
- Documentation and/or coreTools changes:
  - Updated the databook for QoS functionality. Added a section to describe the QoS Controller and Added a section in the Parameters chapter for QoS Options and APB Configurations. Added QoS

signals and APB configuration signals in the Signals chapter. Added a section regarding QoS integration in the Integration Considerations chapter.

- Added two chapters, Chapter 6, Registers, and Chapter 7, Programming the DW_axi in the DW_axi databook
- Enhanced the User-Defined Arbitration Type section in the databook.
- Added a note about connecting a slave to a single master in the Multi-CyleArbitration section.
- Enhanced the Latency subsection.
- Added a section for integration with an external register slice in the Integration Consideration chapter.
- Updated the databook template
- Uses coreTools version 2012.06-SP2

- Packaging changes:
  - Corrected file prefixing in the encrypted mode

Changes in 2.13a version of DW_axi

- RTL changes:
  - Fixed problem whereby undriven inputs were not sampled by sub-modules
  - Ensured all signals appear in event list of always statement
  - Fixed problem of controlling priority of shared layers when requesting dedicated layer in hybrid configurations
- Testbench changes:
  - Fixed failure in lock sequence of arbitration checker
- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.09-SP2
  - Removed inappropriate mention of debug “mode” in Signals chapter
  - Removed number-specific region statement in “Slave Address Map” section
  - Updated system diagram in Figure 1-1
  - Enhanced “Related Documents” section in Preface
  - Made master and slave variable designations consistent

Changes in 2.12a version of DW_axi

- RTL changes:
  - Added new deadlock notification feature
  - Removed combinatorial loop in bi-directional connection with hybrid mode
  - Fixed problem where DesignWare or DesignWare-Foundation license was required for source-only features; source license alone allows access to these features

- Fix to RTL in low-power controller to avoid ELAB-985 synthesis warnings (no logic in always process)
- Fixed naming of generate block
- Low-power control module now named uniquely for every component with a low-power interface to avoid compilation errors

- Testbench changes:
  - Update to timing arbiter checker to fix generation of false errors
- Documentation and/or coreTools changes:
  - Added information for new deadlock notification feature
  - Corrected title for Figure 3-4

Changes in 2.11a version of DW_axi

- RTL changes:
  - Overlapping slave addresses now allowed in cases where no master is visible to any two or more slaves with overlapping addresses
  - Fair-among-equals arbiter now enabled correctly in non-pipelined arbiter mode (AXI_*_PL_ARB)
  - Fix to enabling of fair among equals arbiter fixes deadlock scenario bug during arbitration of locked sequences
  - Fix for address map checker to check regions 3 to 8 for slaves 2 to 16
  - Named previously unnamed generate blocks in RTL
  - Fixed number of parameters passed to module instantiation
- Testbench
  - Fixed simulation failure due to a race condition in Cadence simulations on GTECH
- Documentation and/or coreTools changes:
  - Added information for:
    - Overlapping addresses
    - Avoiding combinatorial loops between two or more DW_axi instances connected in a bi-directional command flow manner
    - "No outstanding transactions counter" field updated to consider decimal values

Changes in 2.09a version of DW_axi

- RTL changes:
  - AXI_POW2_MIDW parameter changed to read-only
  - Clarified when license checking is done for hybrid architecture
  - Default value of maximum number of unique ID parameter (AXI_MAX_U[R/W]IDA_M*n*) now tracks 2^{AXI_MIDW} if AXI_MIDW < 3

- Redundancy checking on AXI_MAX_U[R/W]IDA_M*n* parameters corrected for ICM ports in bi-directional command-enabled configurations
- ID width of master ports 1 through 4 now correctly calculated after first configuration in coreAssembler
- Hybrid-specific code that caused index out of range now used only in hybrid instances of address block module
- Added AXI protocol, low-power handshaking interface
- Fix added to enabling of timing based arbiter when multi cycle arbitration is enabled
- Fixed issue with enabling of timing based arbiter on cycle after locked sequence ends, which caused bus deadlock
- Fixed issue where grants from timing based arbiter were missed when multi-cycle arbitration was enabled
- Improved enabling of arbiter in multi cycle arbitration mode, if the arbiter pipeline stage is not enabled

- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.03 or later
  - Clarification added to databook that fair-among-equals arbitration does not imply first-come-first-serve among equals
  - Added labels for shared-layer multi-cycle arbitration parameters
  - Clarified AXI_MAX_UWIDA_M(i) and AXI_MAX_URIDA_M(i) descriptions in databook
  - Details added to databook on when license checking is done
  - Corrected names of include files and vcs command used for simulation in databook
  - Corrected syntax for undef directive
  - Added material for low-power interface functionality, signals, and parameters in databook
  - Locking sequences section updated to match new functionality of a previous version
  - Support for user arbiters on address channels with locking sequences enabled has been dropped
  - Corrected value for AXI_REG_AW_W_PATHS when operating frequency reduced
- Testbench
  - Fixed false test failure in multi-tile deadlock avoidance test
  - Fixed false test failure due to bug in testbench slave address look up task

Changes in 2.07a version of DW_axi

- RTL changes:
  - Usage of timing arbiters fixed so that selected arbitration algorithm is applied to locked sequences
  - Multi-tile (bi-directional) deadlock prevention feature improved to use WLAST to detect transaction completion - improved latency

- Bi-directional deadlock avoidance feature extended to cover all multi-tile configurations, not just bi-directional

- Documentation and/or coreTools changes:
  - Enhanced “Bi-Directional Deadlock Prevention” section

Changes in 2.05a version of DW_axi

- RTL changes:
  - Packaging fixed to block configurations where no slaves visible to any masters in boot or normal address mode
  - Fixed problem where a write data channel deadlock was possible when two or more DW_axi interconnects were used to build a multi-tile AXI bus system in a bi-directional command flow configuration (AXI_HAS_BICMD=1)
  - Fixed problem where latches and a combinatorial feedback loop occurred in the logic when the DW_axi was being used in hybrid mode with only one master present on the shared write data layer
  - Fixed latency problem introduced by inter channel communication in the DW_axi fabric when wready toggled in spite of the fact that the Slave wready was set to 1
  - Brackets used to clarify intent of RTL containing “| |(*boolean_expression*)” syntax that may be interpreted differently by different simulators
  - Uses coreTools version 2009.06-SP1-1
- Documentation and/or coreTools changes:
  - Removed demux in valid path of shared layer illustrations
  - Added Master3 and Master4 information in “Hybrid Shared and Dedicated Layers Configuration” table
  - Updated databook to new template for consistency with other IIP/VIP/PHY databooks

Changes in 2.01a version of DW_axi

- RTL changes:
  - Fixed problem where deadlock of interconnect was possible on W channel for some hybrid configurations.
  - Fixed problem with checker specific to hybrid configurations that flagged error if two or more valid signals for master slave paths configured to pass through shared layer were asserted at any one time.
  - Fixed problem when two DW_axi 2.0a instances were connected in coreAssembler that caused errors during configuration.
  - Fixed problem where shared layer pipelining parameters—AXI_AR_SHARED_PL, AXI_R_SHARED_PL, AXI_AW_SHARED_PL, AXI_W_SHARED_PL, AXI_B_SHARED_PL—were always enabled.
  - Fixed deadlock condition that occurred in any configuration with shared write address channel when AXI_AW_SHARED_PL=1.

  - Fixed condition in a configuration containing shared and dedicated layers in which a false error can occur due to insufficient stimulus.
  - Enhanced packaging for improved performance during component configuration in coreTools.
  - Fix made to synchronization between address channels in initiating locked sequences when timing arbiters exist (first-come-first-serve or fair-among-equals) and the arbiter pipeline stage is enabled on one address channel only.
- Documentation and/or coreTools changes:
  - None

Changes in 2.00a version of DW_axi

- RTL changes:
  - Hybrid Architecture functionality added
- Documentation and/or coreTools changes:
  - Slave priority signal width changed to log2(AXI_NUM_SLAVES + 1)
  - Enhanced “Pipeline Channel Arbiter” section for dead cycle after wlast with pipelined arbiters

Changes in 1.18a version of DW_axi

- RTL changes:
  - Changed default slave interleaving depth from 2 to 1
  - Removed non-blocking assigns from dynamic priority arbiter module
  - Removed valid_src to ready_src paths when channel pipelining is enabled
  - Connected previously unconnected sub-module output ports to correctly sized dummy wires; removes tool warnings related to unconnected output ports
  - Default slave visibility parameters are now disabled because default slave should always be visible to all masters
- Documentation and/or coreTools changes:
  - None

Changes in 1.17a version of DW_axi

- RTL changes:
  - Timing-based arbiters are disabled while a transaction is being masked
- Documentation and/or coreTools changes:
  - None

Changes in 1.16a version of DW_axi

- RTL changes:
  - Read data, burst response, and write data channels now drive DW_axi_arb.init_n_i to 1'b1

- Documentation and/or coreTools changes:
  - None

Changes in 1.15a version of DW_axi

- RTL changes:
  - Corrected generation of RVALID
- Documentation and/or coreTools changes:
  - Note text changed in “Read Data Interleaving” section
  - Uses coreTools version 2008.06-SP2-2

Changes in 1.14a version of DW_axi

- RTL changes:
  - Added the option of limiting read interleaving at a master port to a depth of one, independent of the number of outstanding unique ID values configured
- Documentation and/or coreTools changes:
  - New section on read data interleaving
  - Added text to coreConsultant parameter description to clarify how to set AXI_MAX_FA(R/W)C_S parameters
  - Corrected default value and enhanced AXI_ALLOW_MST*n*_ICM(*i*) parameter
  - Enhanced section on interconnecting masters

Changes in 1.13a version of DW_axi

- RTL changes:
  - Support added for VCSi simulator
  - AXI_HAS_XDCDR is now an interface parameter
  - Bug resolved in back-to-back locking with multi-cycle arbitration enabled on slave
  - Minimum value of AXI_ALLOW_MSTn_ICMi is now 1 instead of 0
  - Provided remap_n interface parameter to resolve coreAssembler simulation issues
  - Resolved synthesis bug with bi-directional mode when AXI_NUM_MASTERS is power of 2
  - Added support for up to 64 system masters in bi-directional command mode
  - Width of external master priority ports now derived from number of local masters for bi-directional command flow-enabled configurations; was previously derived from number of system masters
  - The number of slave regions is now configured in the Slave Address Map tab of coreConsultant

- Documentation and/or coreTools changes:
  - Databook updated to highlight combinatorial paths from payload_src to ready_src
  - Databook updated to indicate all slaves can have eight regions in both boot and normal modes
  - Figure 24 updated in databook
  - Uses coreTools version 2007.06-SP4

Changes in 1.10a version of DW_axi

- Multi-cycle arbitration was added to the component; associated parameters were added to the coreConsultant GUI.
- An additional subsection was made to the databook for the multi-cycle arbitration options.

Changes in 1.08a version of DW_axi

- New Pipeline Channel Arbiter functionality and a re-architected internal register slice were added to the component; corresponding parameters were added to the coreConsultant GUI.
- Additions were made to the databook for the Forward Registered and Fully Registered timing mode options. Additional subsections were added for the new Pipeline Channel Arbiter and External Register Slice functionalities.

Changes in 1.07a version of DW_axi

- Added the ability to select between priority, first-come-first-served, fair-among-equals, and user-defined arbitration at every arbitration point in the design.
- Uses coreTools version 2007.06-1 or later.
- STAR 9000178727: AXI_HAS_BICMD parameter description updated.
- STAR 9000186924: The “Use DesignWare foundation synthesis library” option does not work as expected with DesignWare and source license.

Changes in 1.05a version of DW_axi

- Added bi-directional command support
- Error message for invalid value of AXI_MAX_UWID is corrected
- Increase limits for number of outstanding read or write transactions at Slave Ports from 16 to 32
- Enhanced databook to include coreAssembler intent in Chapter 2
- Boot mode parameter name corrected in databook
- AXI_NUM_RN_S(j) and AXI_NUM_RB_S(j) parameters now have address regions from 1 to 8
- Default values for port constraints are now available in coreConsultant
- Increased the valid range of the AXI_MAX_URIDA_M and AXI_MAX_UWIDA_M parameters from 1-16 to 1-32

Changes in 1.04a version of DW_axi

- Update to fix illegal verilog statement and simulation failures with support Vera and VCS versions.

Changes in 1.03a version of DW_axi

- Update to fix potential deadlock issue.

Changes in 1.02a version of DW_axi

- Added support for locked transactions
- Added support for fully registered timing mode option
- Increased the maximum AXI data bus width to 512 bits
- Added support for AR/AWLEN width up to 8 bits (previous maximum was 4 bits); now allow data bursts up to 256
- Changed the legal value of the AXI address bus width to be a value between 32 and 64 bits
- Added support to dynamically control arbitration priorities via user-controlled inputs
- Removed external decoder inputs xdcdr_awaddr_m(*i*) and xdcdr_araddr_m(*i*) from the I/O
- Full coreAssembler support, including subsystem creation, auto-connection of AXI/AHB buses, and automatic subsystem testing
- Updated support for newer tools and DesignWare Verification IP
- AXI interface definitions 2.0 support

Changes in 1.01a version of DW_axi

- Master AXI ID width configuration parameter support increased to 12 bits (slave ID width to 16)
- Changed the maximum value of the AXI data bus width configuration parameter to 512 bits
- Support for forward registered timing mode

For a list of product features, refer to "Features" in the *DesignWare DW_axi Databook*.

2.4.1.2 DW_axi Releases

Table 2-2 lists the latest versions of the DW_axi component.

Table 2-2 DesignWare for AMBA 3 AXI/DW_axi Releases

DesignWare Release for AMBA 2/AMBA 3 AXI	DW_axi Version	AXICompVerIdReg Value	Databook Date
2020.03a (AXI-only) with 2018.07a AMBA	4.04a	34_30_34_2A	March 2020
2018.02a (AXI-only) with 2016.10a AMBA	4.03a	34_30_33_2A	February 2018

DesignWare Release for AMBA 2/AMBA 3 AXI	DW_axi Version	AXICompVerIdReg Value	Databook Date
2016.03a (AXI-only) with 2015.06a AMBA	4.02a	34_30_32_2A	March 2016
2014.10a (AXI-only) with 2014.06a AMBA	4.01a	34_30_31_2A	October 2014
2013.06a (AXI-only) with 2013.05a AMBA	4.00a	34_30_30_2A	June 2013
2013.05a (AXI-only) with 2013.05a AMBA	3.01a	33_30_31_2A	May 2013
2011.10a (AXI-only) with 2011.10a AMBA	2.13a	N/A	October 2011
2011.01a (AXI-only) with 2010.12a AMBA	2.12a	N/A	January 2011
2010.11a (AXI-only) with 2010.09a AMBA	2.11a	N/A	November 2010
2010.09a (AXI-only) with 2010.09a AMBA	2.09a	N/A	September 2010
2010.04a (AXI-only) with 2010.03a AMBA	2.07a	N/A	April 2010
2010.02a (AXI-only) with 2009.06a AMBA	2.05a	N/A	February 2010
2009.08a (AXI-only) with 2009.06a AMBA	2.01a	N/A	August 2009
2009.07a (AXI-only) with 2009.06a AMBA	2.00a	N/A	July 2009
2009.03a (AXI-only) with 2008.10a AMBA	1.18a	N/A	March 2009
2009.01a (AXI-only) with 2008.10a AMBA	1.17a	N/A	January 2009
2008.12a (AXI-only) with 2008.10a AMBA	1.16a	N/A	December 2008
2008.10a (AXI-only) with 2008.10a AMBA	1.15a	N/A	October 2008
2008.07a (AXI-only)	1.14a	N/A	July 2008
2008.06a (AXI-only) with 2008.06a AMBA	1.13a	N/A	June 2008

DesignWare Release for AMBA 2/AMBA 3 AXI	DW_axi Version	AXICompVerIdReg Value	Databook Date
2007.10a (AXI-only)	1.10a	N/A	September 2007
2007.08a (AXI-only)	1.08a	N/A	August 2007
2007.06a (AXI-only) with 2007.06a AMBA	1.07a	N/A	June 2007
2007.04a (AXI-only) with 2007.04a AMBA	1.06a	N/A	April 2007
2007.02a (AXI-only)	1.06a	N/A	February 2007
2006.10a (AXI-only)	1.04a	N/A	October 2006
2006.05a (AXI-only)	1.03a	N/A	May 2006
2006.04a (AXI-only)	1.02a	N/A	April 2006
2005.04a	1.01a	N/A	December 2005
2005.04a	1.00a	N/A	October 2005

2.4.1.3 DW_axi Known Problems and Workarounds

The following is a known limitation with the 4.00a, 4.01a, 4.02a versions of the DW_axi:

- Discovery SVT VIP for AMBA does not support the MTI simulator, so sim_svte is not supported in the MTI simulator.

The following are known issues in the 3.01a version of the DW_axi:

- Supports only APB2 slave interface when programming QoS registers
- APB data bus width can be configured for 32 bits only
- AXI low-power functionality not supported in QoS feature

2.4.2 DW_axi_a2x

The following sections list the new features and changes, and the fixed problems and enhancements, for the DW_axi_a2x component. For DW_axi_a2x-specific STARs, refer to:

https://www.synopsys.com/dw/star.php?c=DW_axi_a2x

For detailed features description, see the *DW_axi_a2x databook*.

For information on known issues, refer to "DW_axi_a2x Known Problems and Workarounds" on page 170.

2.4.2.1 DW_axi_a2x New Features and Changes

This section describes what was new or had changed during the various versions of the DW_axi_a2x:

Changes in 2.04a version of DW_axi_a2x

- RTL Changes:

- Design compliance to SpyGlass 2019.06-SP2 and GuideWare 2019.06
- Discontinued Support:
  - Removed support for Synchronization depth parameters A2X_PP_SYNC_DEPTH = 1 and A2X_SP_SYNC_DEPTH = 1 (as cautioned in the previous GA).
- Enhancement:
  - STAR 9001167489: Support for maximum ID width to 16 bits is added.

- Documentation changes:
  - Refer to the Revision History of the DW_axi_a2x databook.
- Packaging changes:
  - STAR 9001473189: Unable to export Interface parameter SplitCapable in the coreAssembler while using DW_axi_a2x. The packaging is updated to consider the SplitCapable value.

    Migrate to the latest coreTools version, which will address this issue. Contact Synopsys Support to receive the specific coreTools version.
  - STAR 9001473193: hmaster remains unconnected when a2x slave is configured as non-split capable, and in AHB-Lite. In the AHB system, if the user is working in the Lite mode or in the full AHB mode, and if the user does not want to SplitCapable, then in the configure interfaces the user can set the SplitCapable parameter to 0. This causes the hmaster output from DW_ahb to not auto-connect to the DW_axi_a2x. User needs to connect them manually. The user guide is updated with the relevant information.
  - STAR 3115176: Updated sWork::evalInComponent to align with coreTools version 2018.09-SP2
  - Minor packaging updates

Changes in 2.03a version of DW_axi_a2x

- RTL changes:
  - RTL compliance to SpyGlass 2017.03-SP-1 and GuideWare 2017.03
  - Fixed Defects
    - STAR 9001116519: An RTL issue in which if the first read receives an SLVERR response, and the second read receives an OKAY response on the secondary port. However, for primary port the second read receives SLVERR response.
    - STAR 9001289398: An RTL issue in which the rlast signal is not asserted at the primary port at the correct time. When an unaligned read transaction is issued at the primary port, the rlast signal is not asserted at the primary port at the correct time. This is due to the incorrect calculation of remaining transaction length after the first beat at the secondary port. This results in the data and control signals mismatch.
    - STAR 9001289412: An RTL issue in which parameters A2X_AR_SP_PIPELINE and A2X_AW_SP_PIPELINE values are ineffectual. When the Write Address channel timing pipeline is disabled (A2X_AW_SP_PIPELINE = 0), Read Address channel timing pipeline cannot be enabled.
  - Enhancements
    - STAR 9001167489: Increased the ID width to support up to 16 bits

- Documentation and/or coreTools changes:
  - Version update
  - Updated synthesis results in Integration Considerations chapter of the databook
  - Published the first version of DesignWare Synthesizable Components for AMBA 3 AXI, and AMBA 4 AXI user guide
  - Removed chapter 2 Building and Verifying a Component or Subsystem from the databook and added the content in the newly created user guide
  - Signals, Parameters, and Internal Parameters chapters auto-extracted with change bars from the RTL
  - Uses coreTools version N-2017.12-SP1-3
- Packaging changes:
  - Minor packaging enhancements
- Removed support for NC Verilog Simulator and MTI Simulator

Changes in 2.02a version of DW_axi_a2x

- RTL changes:
  - Lint cleanup
  - Enhanced to support:
    - 1024 data bus width
  - Fixed following bugs:
    - Bridge could not handle rebuild using FIXED transfer on split recall of INCR Transfer
    - Write command corruption if INCR to FIX burst after split and buffer is full
- Documentation and/or coreTools changes:
  - Version update
  - Signals chapter auto-extracted from the RTL
  - Parameters chapter auto-extracted from the RTL
  - Databook is updated for 1024 data bus width support
  - Uses coreTools version 2015.06-SP3-1
  - Updated the performance section in the Integration Consideration chapter
- Packaging changes:
  - Minor packaging enhancements

Changes in 2.01a version of DW_axi_a2x

- RTL changes:
  - Lint cleanup
  - Fixed a bug for incorrect sampling of WRITE data by A2X bridge during BUSY transfers

- Documentation and/or coreTools changes:
  - Added busy_status port in the signal description section of the data book
  - Version update
  - Uses coreTools version 2014.03-SP1-1
  - Updated the performance section in the Integration Considerations chapter
- Packaging changes:
  - Minor packing enhancements

Changes in 2.00a version of DW_axi_a2x

- RTL changes:
  - Implemented support for the AMBA 4 AXI and ACE-Lite interface
  - Added QoS, user, and region signals in the AMBA 4 AXI and ACE-Lite mode
  - Added snoop, domain, and barrier signals in the ACE-Lite mode
- Documentation and/or coreTools changes:
  - Updated the databook with new signals and parameters added in the AMBA 4 AXI and ACE-Lite mode
  - Uses coreTools version 2013.03-SP1-1
- Packaging changes:
  - None

Changes in 1.01a version of DW_axi_a2x

- RTL changes:
  - Fixed a bug which caused write address and write data channel to be mis-aligned, resulting in loss of data
- Documentation and/or coreTools changes:
  - Updated the databook template
  - Uses coreTools version 2012.06-SP2
- Packaging changes:
  - Corrected file prefixing in the encrypted mode

Changes in 1.00a version of DW_axi_a2x

- Initial release version of DW_axi_a2x is 1.00a

2.4.2.2 DW_axi_a2x Releases

Table 2-3 lists the latest versions of the DW_axi_a2x component.

Table 2-3 DesignWare for AMBA 3 AXI/DW_axi_a2x Releases

DesignWare Release for AMBA 2/AMBA 3 AXI	DW_axi_a2x Version	Databook Date
2020.03a (AXI-only) with 2018.07a AMBA	2.04a	March 2020
2018.02a (AXI-only) with 2016.10a AMBA	2.03a	February 2018
2016.03a (AXI-only) with 2015.06a AMBA	2.02a	March 2016
2014.10a (AXI-only) with 2014.06a AMBA	2.01a	October 2014
2013.06a (AXI-only) with 2013.05a AMBA	2.00a	June 2013
2013.05a (AXI-only) with 2013.05a AMBA	1.01a	May 2013
2012.01a (AXI-only) with 2011.11a AMBA	1.00a	January 2012

2.4.2.3 DW_axi_a2x Known Problems and Workarounds

When DW_axi_a2x is used in coreAssembler, then a user cannot configure the data width to 1024 as coreAssembler does not support a data width of 1024. However, data of width equal to or less than 512 is still supported.

2.4.3 DW_axi_dmac

The following sections list the new features and changes, and the fixed problems and enhancements, for the DW_axi_dmac component. For DW_axi_dmac-specific STARs, refer to:

https://www.synopsys.com/dw/star.php?c=DW_axi_dmac

For detailed featires description, see the *DW_axi_dmac databook*.

For information on known issues, refer to "DW_axi_dmac Known Problems and Workarounds" on page 174.

2.4.3.1 DW_axi_dmac New Features and Changes

This section describes what was new or had changed during the various versions of the DW_axi_dmac:

Changes in 2.00a version of DW_axi_dmac

- RTL Changes:
  - Design compliance to SpyGlass 2019.06-SP2 and GuideWare 2019.06
  - Fixed Issue:

        - STAR 9001320797: Transient data loss while accessing registers on AHB slave interface. DW_axi_dmac accepts the AHB read or write transfer based on the hready_resp output signal instead of hready input signal from the AHB subsystem. This issue has been fixed.
        - STAR 9001353518: LLP Status - DMA Transfer Done update issue.

          After the completion of the last block of the LLI based multi-block transfer, and during LLI status write back, the CHx_LLP_STATUS[63] = CHx_IntStatus needs to be asserted indicating that DMA transfer is completed (DMA_TFR_DONE = 1). But CHx_LLP_STATUS[63] is not set because the RTL logic that generates this condition is reset when the last block is being trasfered (ch_ctl_shadowreg_or_lli_valid_rd_c). This issue has been fixed.
        - STAR 9001571601: Synchronization scheme issue when hclk is faster than dmac_core_clock.

          In some cases when hclk signal is faster than the dmac_core_clock signal, incorrect data is being written into the dmac_core_clock registers due to the synchronization scheme issue. This issue has been fixed.
        - STAR 3145979: Write Strobe Asserted Incorrectly When Destination is a Flow Controller

          This write strobe behavior is observed under the following scenario:

          - The DW_axi_dmac Channel is configured (DMAX_CH(x)_TT_FC)/programmed (CHx_CFG.TT_FC) with Destination as the flow controller.

          - Programmed Transfer Widths is as follows: CHx_CTL.SRC_TR_WIDTH > CHx_CTL.DST_TR_WIDTH.

          - Block Size (in terms of CHx_CTL.DST_TR_WIDTH in bytes) / Source Transfer Width in bytes != integer

          Under the mentioned scenario, the DW_axi_dmac asserts the write strobes for more bytes than the Destination Transfer width (for last AXI write transfer of the DMA block).
    - Enhancement:
        - STAR 9001343696: APB4 Interface enhancement
        - STAR 9001350357: External Memory Interface enhancement
        - STAR 9001369004: Clock Gating Cell reset port removal
        - STAR 9001432079: DW_axi_dmac Safety Features (Slave Interface Parity, ECC Protection, and Lock Step Protection) and Unique ID Support
        - STAR 9001559974: Timing Optimization - Context Sensitive Clock Gating
        - STAR 9001566576: Synchronizer Cell init and test port are made configurable
- Documentation changes:
    - Please refer the Revision History of the DW_axi_dmac databook.
- Packaging changes:
    - STAR 9001535144: Conflicting constraints in SDC file
    - STAR 3115176: Updated sWork::evalInComponent to align with coreTools version 2018.09-SP2
    - Minor packaging updates

Changes in 1.02a version of DW_axi_dmac

- RTL changes:

- RTL compliance to SpyGlass 2017.03-SP-1 and GuideWare 2017.03
- Fixed Defects:
  - STAR 9001170117: An RTL issue in which reset in Master Interface Module of DW_axi_dmac does not get generated. When DW_axi_dmac is configured to have asynchronous clock for the core clock (dmac_core_clock) and the master interface clock (aclk_m1/aclk_m2), then DW_axi_dmac_bcm37 module is used to synchronize the soft reset in two domains. DW_axi_dmac_bcm37 module takes asynchronous reset from both the clock domains to reset the respective domain registers inside the module. These signals are connected to the fixed value of 1, thereby making the reset synchronizer module not see reset by the respective reset signals. So the module output is not initialized during reset, which leads to an unpredictable behavior at a system level.
- Enhancements:

  STAR 9001289389: The following enhancements have been made in DW_axi_dmac 1.02a release:
  - RTL is updated for Clock Gating efficiency in the FIFO module during channel disable. When the channel is disabled, soft reset is issued to the FIFO of all the channels. This soft reset is level sensitive and is used as synchronous reset to the available FIFOs in the channels. When DC inserted clock gating is used, the clock gating cell always sees the synchronous reset in place and cannot gate the clock to the FIFO module. This result in more power consumption during channel disable. This is enhanced to save the power and gate the clock properly during channel disable to the FIFO module.
  - Channel multi arbitration support to improve the QoR for the design
  - Unaligned Transfer Support.
  - Context Sensitive Low Power support to reduce the overall power consumption of DW_axi_dmac.
  - 32 DMA channels and 64 handshake interfaces support.
  - Asynchronous Hardware Handshake support to ease the integration of DW_axi_dmac into user subsystem, where the DMA Hardware Handshake signals are asynchronous.

- Documentation and/or coreTools changes:
  - Version update
  - Updated synthesis results in Integration Considerations chapter of the databook
  - AXI Unaligned Transfer support, Context Sensitive Low Power Option support, Asynchronous Hardware Handshake Support, Single Arbiter Scheme support, Multi-Arbiter Scheme support are added in the Databook
  - Signals, Parameters, and Internal Parameters chapters auto-extracted with change bars from the RTL
  - Published the first version of DesignWare Synthesizable Components for AMBA 3 AXI, and AMBA 4 AXI user guide
  - Removed chapter 2 Building and Verifying a Component or Subsystem from the databook and added the content in the newly created user guide
  - Uses coreTools version N-2017.12-SP1-3
- Packaging changes:

- Minor packaging enhancements
- Removed support for NC Verilog Simulator and MTI Simulator

Changes in 1.01a version of DW_axi_dmac

- RTL changes:
  - Lint cleanup
  - Fixed following bugs:
    - Bug in LLI Write Back Feature
    - AXI4 output ports awqos, arqos present in RTL with DMAX_MSTIF_MODE = 0 (AXI3)
    - QoS output ports (awqos/arqos) related to AXI4 are now not available in AXI3 mode. Therefore, the DMAX_HAS_QOS parameter is added in DW_axi_dmac to decide whether QoS output ports is available. This parameter is enabled only when the AXI4 mode (DMAX_MSTIF_MODE==1) is selected.
    - DW_axi_dmac Write bursts have stalls on sync master interface
    - LLI prefetch error not reported when the ongoing block completes early
    - AXI decoder error not cleared even after the interrupt is cleared
    - Channel aborted intr not generated when channel is being disabled due to AXI err
- Documentation and/or coreTools changes:
  - Version update
  - Signals chapter auto-extracted from the RTL
  - Parameters chapter auto-extracted from the RTL
  - Registers chapter auto-extracted from the RTL
  - Databook updated to include programming flow for Single Block Transfer
  - Updated the “Unsupported Features” section
  - Uses coreTools version 2015.06-SP3-1
  - Updated the performance section in the Integration Consideration chapter
- Packaging changes:
  - Minor packaging enhancements

Changes in 1.00a version of DW_axi_dmac

The following is new or has changed in the 1.00a version of the DW_axi_dmac:

- Initial release version of DW_axi_dmac is 1.00a

2.4.3.2 DW_axi_dmac Releases

Table 2-4 lists the latest versions of the DW_axi_dmac component.

Table 2-4 DesignWare for AMBA 3 AXI/DW_axi_dmac Releases

DesignWare Release for AMBA 2/AMBA 3 AXI	DW_axi_dmac Version	Databook Date
2020.03a (AXI-only) with 2018.07a AMBA	2.00a	March 2020
2018.02a (AXI-only) with 2016.10a AMBA	1.02a	February 2018
2016.03a (AXI-only) with 2015.06a AMBA	1.01a	March 2016
2014.10a (AXI-only) with 2014.06a AMBA	1.00a	October 2014

2.4.3.3 DW_axi_dmac Known Problems and Workarounds

The following are known limitations with the DW_axi_dmac:

- Discovery SVT VIP for AMBA AHB bus does not support the MTI simulator, so DW_axi_dmac is not supported in the MTI simulator.
- Discovery SVT VIP for AMBA AHB bus does not support the NC-Verilog simulator, so DW_axi_dmac is not supported in the NC-Verilog simulator.

2.4.4 DW_axi_gm

The following sections list the new features and changes, and the fixed problems and enhancements, for the DW_axi_gm component. For DW_axi_gm-specific STARs, refer to:

https://www.synopsys.com/dw/star.php?c=DW_axi_gm

For detailed features description, see the *DW_axi_gm databook*.

For information on known issues, refer to "DW_axi_gm Known Problems and Workarounds" on page 179.

2.4.4.1 DW_axi_gm New Features and Changes

This section describes what was new or had changed during the various versions of the DW_axi_gm:

Changes in 2.04a version of DW_axi_gm

- RTL Changes:
  - Design compliance to SpyGlass 2019.06-SP2 and GuideWare 2019.06
- Documentation changes
  - Refer to the Revision History of the DW_axi_gm databook.
- Packaging changes:
  - STAR 3115176: Update sWork::evalInComponent to align with coreTools version 2018.09-SP2.
  - Minor packaging updates.

Changes in 2.03a version of DW_axi_gm

- RTL changes:
  - RTL compliance to SpyGlass 2017.03-SP-1 and GuideWare 2017.03
- Documentation and/or coreTools changes:
  - Version update
  - Updated synthesis results in Integration Considerations chapter of the databook
  - Published the first version of DesignWare Synthesizable Components for AMBA 3 AXI, and AMBA 4 AXI user guide
  - Removed chapter 2 Building and Verifying a Component or Subsystem from the databook and added the content in the newly created user guide
  - Signals, Parameters, and Internal Parameters chapters auto-extracted with change bars from the RTL
  - Uses coreTools version N-2017.12-SP1-3
- Packaging changes:
  - Minor packaging enhancements
- Removed support for NC Verilog Simulator and MTI Simulator

Changes in 2.02a version of DW_axi_gm

- RTL changes:
  - Lint cleanup
- Documentation and/or coreTools changes:
  - Version update
  - Signals chapter auto-extracted from the RTL
  - Parameters chapter auto-extracted from the RTL
  - Uses coreTools version 2015.06-SP3-1
  - Updated the performance section in the Integration Consideration chapter
- Packaging changes:
  - Minor packaging enhancements

Changes in 2.01a version of DW_axi_gm

- RTL changes:
  - Lint cleanup
- Documentation and/or coreTools changes:
  - Version update
  - Uses coreTools version 2014.03-SP1-1

    - Added a new chapter on Integration Considerations in the data book
- Packaging changes:
    - Minor packing enhancements

Changes in 2.00a version of DW_axi_gm

- RTL changes:
    - Implemented support for the AMBA 4 AXI interface
    - Added QoS and user signals in the AMBA 4 AXI mode
- Documentation and/or coreTools changes:
    - Updated the databook with new signals and parameters added in the AMBA 4 AXI mode
    - Uses coreTools version 2013.03-SP1-1
- Packaging changes:
    - None

Changes in 1.06a version of DW_axi_gm

- RTL changes:
    - Added sideband signals on AXI and GIF channels
    - Fixed a bug which causes GTECH model failure
- Documentation and/or coreTools changes:
    - Added sideband signals and timing diagrams
    - Added coreConsultant parameters for sideband signals
    - Corrected the parameter names for AXI and GIF address width, data width, and ID width
    - Updated the databook template
    - Uses coreTools version 2012.06-SP2
- Packaging changes:
    - Corrected file prefixing in the encrypted mode

Changes in 1.04b version of DW_axi_gm

- RTL changes:
    - Fixed problem whereby simulations failed in coreConsultant with VCS 2010.06-3
    - Fixed problem whereby Vera license was pulled due to out-of-date pragma in .vri file
    - Corrected gclken input delay

- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.09-SP2
  - Updated system diagram in Figure 1-1
  - Enhanced "Related Documents" section in Preface
  - Modified information on unlimited outstanding transactions
  - Modified graphics for gclk signal being derived from gclken
  - Corrected gclken input delay

Changes in 1.04a version of DW_axi_gm

- RTL changes:
  - Fix to RTL in low-power controller to avoid ELAB-985 synthesis warnings (no logic in always process)
  - Fixed naming of generate block
  - Low-power control module now named uniquely for every component with a low-power interface to avoid compilation errors
  - Removed mread/mwrite to saccept combinatorial path when low-power interface included
  - Default input delay of GIF request channel input signals and low-power interface output signals reduced to feasible values
- Documentation and/or coreTools changes:
  - Corrected sresp waveform for Figure 3-3

Changes in 1.03a version of DW_axi_gm

- RTL changes:
  - Enhanced packaging to generate error if request FIFO depth > 1 if both read and write blocking parameters set to 1
  - Low-power handshaking interface changed to be consistent with new interface specification
  - GIF interfaces now automatically exported in coreAssembler
- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.03 or later
  - Added information in databook for locked sequence support
  - Corrected names of include files and vcs command used for simulation in databook
  - Corrected syntax for undef directive
  - Added material for low-power interface functionality, signals, and parameters in databook
  - Corrected names of GM_BLOCK_READ and GM_BLOCK_WRITE parameters in databook

Changes in 1.02a version of DW_axi_gm

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2008.06-SP2-2

Changes in 1.01c version of DW_axi_gm

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2007.06-SP4

Changes in 1.01b version of DW_axi_gm

- Uses coreTools version 2007.06-1 or later.

Changes in 1.01a version of DW_axi_gm

- Enhanced DW_axi_gm databook to include coreAssembler intent in Chapter 2
- Corrected information about monitors in the DW_axi_gm databook
- Corrected timing diagram in Figure 5 of the DW_axi_gm databook
- Log information written to the test.log file instead of gmon.log and gif.log
- Low-power and GIF-master interfaces are now automatically exported
- Data width updated for compatibility with other AXI components
- Address range updated for compatibility with other AXI components
- ID range updated to 12 bits for compatibility with other AXI components
- Burst length updated for compatibility with other AXI components
- Added information in the DW_axi_gm databook about the GIF Request Channel

Changes in 1.00c version of DW_axi_gm

- Full coreAssembler support, including subsystem creation, auto-connection of AXI/AHB buses, and automatic subsystem testing
- Updated support for newer tools and DesignWare Verification IP
- AXI interface definitions 2.0 support

For a list of product features, refer to “Features” in the *DesignWare DW_axi_gm Databook*.

2.4.4.2 DW_axi_gm Releases

Table 2-5 lists the latest versions of the DW_axi_gm component.

Table 2-5 DesignWare for AMBA 3 AXI/DW_axi_gm Releases

DesignWare Release for AMBA 2/AMBA 3 AXI	DW_axi_gm Version	Databook Date
2020.03a (AXI-only) with 2018.07a AMBA	2.04a	March 2020
2018.02a (AXI-only) with 2016.10a AMBA	2.03a	February 2018
2016.03a (AXI-only) with 2015.06a AMBA	2.02a	March 2016
2014.10a (AXI-only) with 2014.06a AMBA	2.01a	October 2014
2013.06a (AXI-only) with 2013.05a AMBA	2.00a	June 2013
2013.05a (AXI-only) with 2013.05a AMBA	1.06a	May 2013
2011.10a (AXI-only) with 2011.10a AMBA	1.04b	October 2011
2011.01a (AXI-only) with 2010.12a AMBA	1.04a	January 2011
2010.09a (AXI-only) with 2010.09a AMBA	1.03a	September 2010
2008.10a (AXI-only) with 2008.10a AMBA	1.02a	October 2008
2008.06a (AXI-only) with 2008.06a AMBA	1.01c	June 2008
2007.06a (AXI-only) with 2007.06a AMBA	1.01b	June 2007
2007.04a (AXI-only) with 2007.04a AMBA	1.01a	April 2007
2007.02a (AXI-only)	1.01a	February 2007
2006.04a (AXI-only)	1.00c	April 14, 2006
2005.04a (AXI-only)	1.00a	September 2005
2005.04a (AXI-only) with 2005.04a AMBA	1.00b	October 2005

2.4.4.3 DW_axi_gm Known Problems and Workarounds

There are no known issues in this release of the DW_axi_gm.

2.4.5 DW_axi_gs

The following sections list the new features and changes, and the fixed problems and enhancements, for the DW_axi_gs component. For DW_axi_gs-specific STARs, refer to:

- https://www.synopsys.com/dw/star.php?c=DW_axi_gs

For detailed feature description, see the *DW_axi_gs databook*.

For information on known issues, refer to "DW_axi_gs Known Problems and Workarounds" on page 185.

2.4.5.1 DW_axi_gs New Features and Changes

This section describes what was new or had changed during the various versions of the DW_axi_gs:

Changes in 2.04a version of DW_axi_gs

- RTL Changes:
  - Design compliance to SpyGlass 2019.06-SP2 and GuideWare 2019.06
- Documentation changes
  - Refer to the Revision History of the DW_axi_gs databook.
- Packaging changes:
  - STAR 9001421138: Fixed the issue related to configuring Sideband signals in the coreAssembler for AXI3 configuration.
  - STAR 3115176: Update sWork::evalInComponent to align with coreTools version 2018.09-SP2.
  - Minor packaging updates.

Changes in 2.03a version of DW_axi_gs

- RTL changes:
  - RTL compliance to SpyGlass 2017.03-SP-1 and GuideWare 2017.03
  - Enhancements:
    - STAR 9001062228: RTL quality improvement for 100% VCS Xprop instrumentation
- Documentation and/or coreTools changes:
  - Version update
  - Updated synthesis results in Integration Considerations chapter of the databook
  - Published the first version of DesignWare Synthesizable Components for AMBA 3 AXI, and AMBA 4 AXI user guide
  - Removed chapter 2 Building and Verifying a Component or Subsystem from the databook and added the content in the newly created user guide
  - Signals, Parameters, and Internal Parameters chapters auto-extracted with change bars from the RTL
  - Uses coreTools version N-2017.12-SP1-3
- Packaging changes:

  - Minor packaging enhancements
- Removed support for NC Verilog Simulator and MTI Simulator

Changes in 2.02a version of DW_axi_gs

- RTL changes:
  - Lint cleanup
- Documentation and/or coreTools changes:
  - Version update
  - Signals chapter auto-extracted from the RTL
  - Parameters chapter auto-extracted from the RTL
  - Uses coreTools version 2015.06-SP3-1
  - Updated the performance section in the Integration Consideration chapter
- Packaging changes:
  - Minor packaging enhancements

Changes in 2.01a version of DW_axi_gs

- RTL changes:
  - Lint cleanup
- Documentation and/or coreTools changes:
  - Version update
  - Uses coreTools version 2014.03-SP1-1
  - Added a new chapter Integration Considerations in the data book
- Packaging changes:
  - Minor packing enhancements

Changes in 2.00a version of DW_axi_gs

- RTL changes:
  - Implemented support for the AMBA 4 AXI interface
  - Added QoS, user, and region signals in the AMBA 4 AXI mode
- Documentation and/or coreTools changes:
  - Updated the databook with new signals and parameters added in the AMBA 4 AXI mode
  - Uses coreTools version 2013.03-SP1-1
- Packaging changes:
  - None

Changes in 1.11a version of DW_axi_gs

- RTL changes:
  - Added sideband signals on AXI and GIF channels
  - Added transaction ID support (Extended GIF mode)
  - Increased the maximum number of outstanding requests to 64
  - Implemented support for unlimited outstanding transactions in Extended GIF mode (limited to 128 when Low Power mode is enabled with Extended GIF mode)
  - Fixed a bug which causes GTECH model failure
- Documentation and/or coreTools changes:
  - Added sideband signals and mid, sid, and slast signals
  - Added coreConsultant parameters for sideband signals
  - Added a section to describe the Extended GIF mode
  - Corrected the width of the awlen, arlen, and mlen signals.
  - Corrected the parameter names for AXI and GIF address width, data width, and ID width.
  - Updated the databook template
  - Uses coreTools version 2012.06-SP2
- Packaging changes:
  - Corrected file prefixing in the encrypted mode

Changes in 1.09a version of DW_axi_gs

- RTL changes:
  - Fixed problem whereby failed exclusive writes cleared matching addresses from exclusive monitor
  - Corrected gclken input delay
  - Fixed problem whereby arbiter always selects reads or writes, thus starving writes or reads
- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.09-SP2
  - Updated system diagram in Figure 1-1
  - Enhanced “Related Documents” section in Preface
  - Corrected gclken input delay

Changes in 1.07a version of DW_axi_gs

- RTL changes:
  - Fix to RTL in low-power controller to avoid ELAB-985 synthesis warnings (no logic in always process)
  - Fixed naming of generate block

    - Low-power control module now named uniquely for every component with a low-power interface to avoid compilation errors
- Documentation and/or coreTools changes:
    - None

Changes in 1.06a version of DW_axi_gs

- RTL changes:
    - GIF interfaces now automatically exported in coreAssembler
    - Low-power handshaking interface changed to be consistent with new interface specification
- Documentation and/or coreTools changes:
    - Uses coreTools version 2010.03 or later
    - Corrected names of include files and vcs command used for simulation in databook
    - Added material for low-power interface functionality, signals, and parameters in databook
    - Corrected syntax for undef directive
    - Corrected incorrect text related to Figure 3-3

Changes in 1.05a version of DW_axi_gs

- RTL changes:
    - If GS_AXI_EX_ACCESS = 0, RTL no longer declares some variables with widths of [-1:0]
- Documentation and/or coreTools changes:
    - None

Changes in 1.04a version of DW_axi_gs

- RTL changes:
    - None
- Documentation and/or coreTools changes:
    - Uses coreTools version 2008.06-SP2-2

Changes in 1.03c version of DW_axi_gs

- RTL changes:
    - None
- Documentation and/or coreTools changes:
    - Uses coreTools version 2007.06-SP4

Changes in 1.03b version of DW_axi_gs

- Uses coreTools version 2007.06-1 or later.

Changes in 1.03a version of DW_axi_gs

- Enhanced DW_axi_gs databook to include coreAssembler intent in Chapter 2
- Log information written to the test.log file instead of gmon.log and gif.log
- Data width updated to match other AXI components
- Address range updated to match other AXI components
- ID range extended to match other AXI components
- Burst length extended to match other AXI components
- Low-power and GIF-slave interfaces are now automatically exported.
- Figure 5 corrected in DW_axi_gs databook

Changes in 1.02a version of DW_axi_gs

- Full coreAssembler support, including subsystem creation, auto-connection of AXI/AHB buses and automatic subsystem testing
- Updated support for newer tools and DesignWare Verification IP
- AXI interface definitions 2.0 support

For a list of product features, refer to "Features" in the *DesignWare DW_axi_gs Databook*.

2.4.5.2 DW_axi_gs Releases

Table 2-6 lists the latest versions of the DW_axi_gs component.

Table 2-6 DesignWare for AMBA 3 AXI/DW_axi_gs Releases

DesignWare Release for AMBA 2/AMBA 3 AXI	DW_axi_gs Version	Databook Date
2020.03a (AXI-only) with 2018.07a AMBA	2.04a	March 2020
2018.02a (AXI-only) with 2016.10a AMBA	2.03a	February 2018
2016.03a (AXI-only) with 2015.06a AMBA	2.02a	March 2016
2014.10a (AXI-only) with 2014.06a AMBA	2.01a	October 2014
2013.06a (AXI-only) with 2013.05a AMBA	2.00a	June 2013
2013.05a (AXI-only) with 2013.05a AMBA	1.11a	May 2013
2011.10a (AXI-only) with 2011.10a AMBA	1.09a	October 2011

DesignWare Release for AMBA 2/AMBA 3 AXI	DW_axi_gs Version	Databook Date
2011.01a (AXI-only) with 2010.12a AMBA	1.07a	January 2011
2010.09a (AXI-only) with 2010.09a AMBA	1.06a	September 2010
2009.01a (AXI-only) with 2008.10a AMBA	1.05a	January 2009
2008.10a (AXI-only) with 2008.10a AMBA	1.04a	October 2008
2008.06a (AXI-only) with 2008.06a AMBA	1.03c	June 2008
2007.06a (AXI-only) with 2007.06a AMBA	1.03b	June 2007
2007.04a (AXI-only) with 2007.04a AMBA	1.03a	April 2007
2007.02a (AXI-only)	1.03a	February 2007
2006.04a (AXI-only)	1.02a	April 14, 2006
2005.04a (AXI-only)	1.01a	October 2005
2005.04a (AXI-only) with 2005.04a AMBA	1.00a	September 2005

2.4.5.3 DW_axi_gs Known Problems and Workarounds

There are no known issues in this release of the DW_axi_gs.

2.4.6 DW_axi_hmx

The following sections list the new features and changes, and the fixed problems and enhancements, for the DW_axi_hmx component. For DW_axi_hmx-specific STARs, refer to:

https://www.synopsys.com/dw/star.php?c=DW_axi_hmx

For detailed feature description, see the *DW_axi_hmx databook*.

For information on known issues, refer to "DW_axi_hmx Known Problems and Workarounds" on page 190.

2.4.6.1 DW_axi_hmx New Features and Changes

This section describes what was new or had changed during the various versions of the DW_axi_hmx:

Changes in 2.03a version of DW_axi_hmx

- RTL Changes:
  - Design compliance to SpyGlass 2019.06-SP2 and GuideWare 2019.06

- Documentation changes
  - Refer to the Revision History of the DW_axi_hmx databook.
- Packaging changes:
  - STAR 3115176: Update sWork::evalInComponent to align with coreTools version 2018.09-SP2.
  - Minor packaging updates.

Changes in 2.02a version of DW_axi_hmx

- RTL changes:
  - RTL compliance to SpyGlass 2017.03-SP-1 and GuideWare 2017.03
- Documentation and/or coreTools changes:
  - Version update
  - Updated synthesis results in Integration Considerations chapter of the databook
  - Published the first version of DesignWare Synthesizable Components for AMBA 3 AXI, and AMBA 4 AXI user guide
  - Removed chapter 2 Building and Verifying a Component or Subsystem from the databook and added the content in the newly created user guide
  - Signals, Parameters, and Internal Parameters chapters auto-extracted with change bars from the RTL
  - Uses coreTools version N-2017.12-SP1-3
- Packaging changes:
  - Minor packaging enhancements

Changes in 2.01a version of DW_axi_hmx

- RTL changes:
  - Lint cleanup
- Documentation and/or coreTools changes:
  - Version update
  - Signals chapter auto-extracted from the RTL
  - Parameters chapter auto-extracted from the RTL
  - Uses coreTools version 2015.06-SP3-1
  - Updated the performance section in the Integration Consideration chapter
- Packaging changes:
  - Minor packaging enhancements
- Removed support for NC Verilog Simulator and MTI Simulator

Changes in 2.00a version of DW_axi_hmx

- RTL changes:
  - Added AXI 4 protocol support
  - Lint cleanup
- Documentation and/or coreTools changes:
  - Version update
  - Uses coreTools version 2014.03-SP1-1
  - Updated the performance section in Integration Considerations chapter
  - Updated AHB INCR Writes section in Functional Description chapter
- Packaging changes:
  - Minor packing enhancements

Changes in 1.08b version of DW_axi_hmx

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2013.03-SP1-1
- Packaging changes:
  - None

Changes in 1.08a version of DW_axi_hmx

- RTL changes:
  - Fixed a bug that caused the DW_axi_hmx to de-assert the wvalid signal before the wready signal was asserted by the slave, which is a protocol violation
- Documentation and/or coreTools changes:
  - Updated the databook template
  - Uses coreTools version 2012.06-SP2
- Packaging changes:
  - Corrected file prefixing in the encrypted mode

Changes in 1.07b version of DW_axi_hmx

- RTL changes:
  - None

- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.09-SP2

Changes in 1.07a version of DW_axi_hmx

- RTL changes:
  - Fixed bug in automatic generation of AXI unlocking command after an AHB locked sequence
  - Fixed issue where an AXI unlock command was issued after an AHB lock sequence consisting only of IDLE transfers
- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.03 or later
  - Added material in databook about limitations with respect to defined length burst support
  - Corrected names of include files and vcs command used for simulation in databook
  - Corrected syntax for undef directive
  - Improvements to documentation of clock enable timing

Changes in 1.04a version of DW_axi_hmx

- RTL changes:
  - Multiple error responses in the same AXI burst or an AHB master not aborting the transfer after an error response no longer break the operation of the DW_axi_hmx.
- Documentation and/or coreTools changes:
  - DW_axi_hmx databook
    - Corrected description for HMX_BLOCK_WRITE in “Transaction Blocking” section

Changes in 1.03a version of DW_axi_hmx

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2008.06-SP2-2

Changes in 1.02b version of DW_axi_hmx

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Added default value for HMX_BLOCK_WRITE to databook
  - Corrected system diagram in databook to highlight DW_axi_hmx component

- Vera version 2006.12-17 or 2007.12-2 required for coreConsultant simulation to avoid Vera core dump
- Uses coreTools version 2007.06-SP4

Changes in 1.02a version of DW_axi_hmx

- STAR 9000186649 enhances the HMX_BLOCK_WRITE parameter in order to allow strong ordering for read/write sequence when the same address is targeted. The "Block Writes" section in the databook has been changed to "Transaction Blocking," which describes the new functionality of this parameter.

Changes in 1.01b version of DW_axi_hmx

- Uses coreTools version 2007.06-1 or later.

Changes in 1.01a version of DW_axi_hmx

- Enhanced DW_axi_hmx databook to include coreAssembler intent in Chapter 2
- Missing hlock signal added to Figure 11 of DW_axi_hmx databook
- Design prefix in coreConsultant now correctly propagates to the testbench
- Removed combinatorial timing paths between hready and hlock/htrans
- DW_axi_hmx databook now states that there cannot be more than 32 outstanding transactions at any time

Changes in 1.00b version of DW_axi_hmx

- For source customers, the .run file generation was checking for the DWC-AMBA feature instead of the DWC-AMBA-Fabric-Source. This has been corrected in the 2006.07b .run file.

For a list of product features, refer to "Features" in the *DesignWare DW_axi_hmx Databook*.

2.4.6.2 DW_axi_hmx Releases

Table 2-7 lists the latest versions of the DW_axi_hmx component.

Table 2-7 DesignWare for AMBA 3 AXI/DW_axi_hmx Releases

DesignWare Release for AMBA 2/AMBA 3 AXI	DW_axi_hmx Version	Databook Date
2020.03a (AXI-only) with 2018.07a AMBA	2.03a	March 2020
2018.02a (AXI-only) with 2016.10a AMBA	2.02a	February 2018
2016.03a (AXI-only) with 2015.06a AMBA	2.01a	March 2016

DesignWare Release for AMBA 2/AMBA 3 AXI	DW_axi_hmx Version	Databook Date
2014.10a (AXI-only) with 2014.06a AMBA	2.00a	October 2014
2013.06a (AXI-only) with 2013.05a AMBA	1.08b	June 2013
2013.05a (AXI-only) with 2013.05a AMBA	1.08a	May 2013
2011.10a (AXI-only) with 2011.10a AMBA	1.07b	October 2011
2010.09a (AXI-only) with 2010.09a AMBA	1.07a	September 2010
2009.01a (AXI-only) with 2008.10a AMBA	1.04a	January 2009
2008.10a (AXI-only) with 2008.10a AMBA	1.03a	October 2008
2008.06a (AXI-only) with 2008.06a AMBA	1.02b	June 2008
2007.07a (AXI-only)	1.02a	July 2007
2007.06a (AXI-only) with 2007.06a AMBA	1.01b	June 2007
2007.04a (AXI-only) with 2007.04a AMBA	1.01a	April 2007
2007.02a (AXI-only)	1.01a	February 2007
2006.07b (AXI-only)	1.00b	August 2006
2006.07a (AXI-only) with 2005.04a AMBA	1.00a	July 2006

2.4.6.3 DW_axi_hmx Known Problems and Workarounds

There are no known issues for this version of the DW_axi_hmx.

2.4.7 DW_axi_rs

The following sections list the new features and changes, and the fixed problems and enhancements, for the DW_axi_rs component. For DW_axi_rs-specific STARs, refer to:

https://www.synopsys.com/dw/star.php?c=DW_axi_rs

For detailed feature description, see the *DW_axi_rs databook*.

For information on known issues, refer to "DW_axi_rs Known Problems and Workarounds" on page 195.

2.4.7.1 DW_axi_rs New Features and Changes

This section describes what was new or had changed during the various versions of the DW_axi_rs:

Changes in 2.04a version of DW_axi_rs

- RTL Changes:
  - Design compliance to SpyGlass 2019.06-SP2 and GuideWare 2019.06
- Documentation changes:
  - Refer to the Revision History of the DW_axi_rs databook.
- Packaging changes:
  - STAR 3115176: Updated sWork::evalInComponent to align with coreTools version 2018.09-SP2
  - Minor packaging updates

Changes in 2.03a version of DW_axi_rs

- RTL changes:
  - RTL compliance to SpyGlass 2017.03-SP-1 and GuideWare 2017.03
  - Enhancement:
    - STAR 9001299220: In forward timing mode, the clock gating efficiency is improved by considering the valid signal for loading payload.
- Documentation and/or coreTools changes:
  - Version update
  - Updated synthesis results in Integration Considerations chapter of the databook
  - Published the first version of DesignWare Synthesizable Components for AMBA 3 AXI, and AMBA 4 AXI user guide
  - Removed chapter 2 Building and Verifying a Component or Subsystem from the databook and added the content in the newly created user guide
  - Signals, Parameters, and Internal Parameters chapters auto-extracted with change bars from the RTL
  - Uses coreTools version N-2017.12-SP1-3
- Packaging changes:
  - Minor packaging enhancements
- Removed support for NC Verilog Simulator and MTI Simulator

Changes in 2.02a version of DW_axi_rs

- RTL changes:
  - Lint cleanup
- Documentation and/or coreTools changes:

- Version update
- Signals chapter auto-extracted from the RTL
- Parameters chapter auto-extracted from the RTL
- Uses coreTools version 2015.06-SP3-1
- Updated the performance section in the Integration Consideration chapter

- Packaging changes:
  - Minor packaging enhancements

Changes in 2.01a version of DW_axi_rs

- RTL changes:
  - Lint cleanup
- Documentation and/or coreTools changes:
  - Version update
  - Uses coreTools version 2014.03-SP1-1
  - Added a new chapter Integration Considerations in the data book
- Packaging changes:
  - Minor packing enhancements
  - Fixed issue of sideband signal propagation in cA in AXI4 mode

Changes in 2.00a version of DW_axi_rs

- RTL changes:
  - Implemented support for the AMBA 4 AXI and ACE-Lite interface
  - Added QoS, user, and region signals in the AMBA 4 AXI and ACE-Lite mode
  - Added snoop, domain, and barrier signals in the ACE-Lite mode
- Documentation and/or coreTools changes:
  - Updated the databook with new signals and parameters added in the AMBA 4 AXI and ACE-Lite mode
  - Uses coreTools version 2013.03-SP1-1
- Packaging changes:
  - None

Changes in 1.02c version of DW_axi_rs

- RTL changes:
  - None

- Documentation and/or coreTools changes:
  - Updated the databook template
  - Uses coreTools version 2012.06-SP2
- Packaging changes:
  - Corrected file prefixing in the encrypted mode

Changes in 1.02b version of DW_axi_rs

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.09-SP2

Changes in 1.02a version of DW_axi_rs

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.03 or later
  - Corrected names of include files and vcs command used for simulation in databook
  - Corrected syntax for undef directive
  - Fixed issue where both interfaces of DW_axi_rs would be auto connected to the same DW_axi tile on initial import into a coreAssembler workspace

Changes in 1.01b version of DW_axi_rs

- RTL changes:
  - Changed synthesis intent to work around coreTools bug in order to allow synthesis constraints to be applied from within coreTools
- Documentation and/or coreTools changes:
  - Corrected Figure 16 with a register in combinatorial path for payload multiplexer

Changes in 1.01a version of DW_axi_rs

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2008.06-SP2-2

Changes in 1.00d version of DW_axi_rs

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2007.06-SP4

Changes in 1.00c version of DW_axi_rs

- Uses coreTools version 2007.06-1 or later.

Changes in 1.00b version of DW_axi_rs

The following changes and/or new features were included in the 1.00b version of the DW_axi_rs:

- Enhanced databook to include coreAssembler intent in Chapter 2
- Hardcoded path in verpp script corrected to avoid crash/hang in the DW_axi_rs

For a list of product features, refer to "Features" in the *DesignWare DW_axi_rs Databook*.

2.4.7.2 DW_axi_rs Releases

Table 2-8 lists the latest versions of the DW_axi_rs component.

Table 2-8 DesignWare for AMBA 3 AXI/DW_axi_rs Releases

DesignWare Release for AMBA 2/AMBA 3 AXI	DW_axi_rs Version	Databook Date
2020.03a (AXI-only) with 2018.07a AMBA	2.04a	March 2020
2018.02a (AXI-only) with 2016.10a AMBA	2.03a	February 2018
2016.03a (AXI-only) with 2015.06a	2.02a	March 2016
2014.10a (AXI-only) with 2014.06a AMBA	2.01a	October 2014
2013.06a (AXI-only) with 2013.05a AMBA	2.00a	June 2013
2013.05a (AXI-only) with 2013.05a AMBA	1.02c	May 2013
2011.10a (AXI-only) with 2011.10a AMBA	1.02b	October 2011
2010.09a (AXI-only) with 2010.09a AMBA	1.02a	September 2010

DesignWare Release for AMBA 2/AMBA 3 AXI	DW_axi_rs Version	Databook Date
2009.03a (AXI-only) with 2008.10a AMBA	1.01b	March 2009
2008.10a (AXI-only) with 2008.10a AMBA	1.01a	October 2008
2008.06a (AXI-only) with 2008.06a AMBA	1.00d	June 2008
2007.06a (AXI-only) with 2007.06a AMBA	1.00c	June 2007
2007.04a (AXI-only) with 2007.04a AMBA	1.00b	April 2007
2007.02a (AXI-only)	1.00b	February 2007
2006.05a (AXI-only)	1.00a	April 14, 2006
2006.04a (AXI-only) with 2005.04a AMBA	1.00a	April 14, 2006

2.4.7.3 DW_axi_rs Known Problems and Workarounds

There are no known issues in this release of the DW_axi_rs.

2.4.8 DW_axi_x2h

The following sections list the new features and changes, and the fixed problems and enhancements, for the DW_axi_x2h component. For DW_axi_x2h-specific STARs, refer to:

https://www.synopsys.com/dw/star.php?c=DW_axi_x2h

For detailed feature description, see the *DW_axi_x2h databook*.

For information on known issues, refer to "DW_axi_x2h Known Problems and Workarounds" on page 200.

2.4.8.1 DW_axi_x2h New Features and Changes

This section describes what was new or had changed during the various versions of the DW_axi_x2h:

Changes in 2.04a version of DW_axi_x2h

- RTL Changes:
  - Design compliance to SpyGlass 2019.06-SP2 and GuideWare 2019.06
  - Enhancement:
    - STAR 9001443539: Support to add MID sideband signals to convey user specific information.
    - STAR 3170369: The CMD FIFO synchronization scheme is updated to improve QoR.
- Documentation changes:

  - Refer to the Revision History of the DW_axi_x2h databook.
- Packaging changes:
  - STAR 3115176: Updated sWork::evalInComponent to align with coreTools version 2018.09-SP2
  - Minor packaging updates

Changes in 2.03a version of DW_axi_x2h

- RTL changes:
  - RTL compliance to SpyGlass 2017.03-SP-1 and GuideWare 2017.03
  - Enhancements
    - RTL quality improvement for 100% VCS Xprop instrumentation
- Documentation and/or coreTools changes:
  - Version update
  - Updated synthesis results in Integration Considerations chapter of the databook
  - Published the first version of DesignWare Synthesizable Components for AMBA 3 AXI, and AMBA 4 AXI user guide
  - Removed chapter 2 Building and Verifying a Component or Subsystem from the databook and added the content in the newly created user guide
  - Signals, Parameters, and Internal Parameters chapters auto-extracted with change bars from the RTL
  - Uses coreTools version N-2017.12-SP1-3
- Packaging changes:
  - Minor packaging enhancements
- Removed support for NC Verilog Simulator and MTI Simulator

Changes in 2.02a version of DW_axi_x2h

- RTL changes:
  - Lint cleanup
- Documentation and/or coreTools chnages:
  - Version update
  - Signals chapter auto-extracted from the RTL
  - Parameters chapter auto-extracted from the RTL
  - Uses coreTools version 2015.06-SP3-1
  - Updated the performance section in the Integration Consideration chapter
- Packaging changes:
  - Minor packaging enhancements

Changes in 2.01a version of DW_axi_x2h

- RTL changes:
  - Lint cleanup
- Documentation and/or coreTools changes:
  - Version update
  - Uses coreTools version 2014.03-SP1-1
  - Updated the performance section in the Integration Considerations chapter
- Packaging changes:
  - Minor packing enhancements

Changes in 2.00a version of DW_axi_x2h

- RTL changes:
  - Implemented support for the AMBA 4 AXI interface
- Documentation and/or coreTools changes:
  - Updated the databook with new and modified signals and parameters implemented for the AMBA 4 AXI interface
  - Uses coreTools version 2013.03-SP1-1
- Packaging changes:
  - None

Changes in 1.07a version of DW_axi_x2h

- RTL changes:
  - The value of Burst Length Width, which was fixed at 4, is now replaced with the parameter name X2H_AXI_BLW.
- Documentation and/or coreTools changes:
  - Updated the databook template
  - Uses coreTools version 2012.06-SP2
- Packaging changes:
  - Corrected file prefixing in the encrypted mode

Changes in 1.06b version of DW_axi_x2h

- RTL changes:
  - None
- Testbench changes:
  - Fixed problem whereby BCM21 inserted missamples with DW_MODEL_MISSAMPLES defined

- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.09-SP2
  - Updated system diagram in Figure 1-1
  - Enhanced “Related Documents” section in Preface

Changes in 1.06a version of DW_axi_x2h

- RTL changes:
  - Fix to RTL in low-power controller to avoid ELAB-985 synthesis warnings (no logic in always process)
  - Fixed naming of generate block
  - Low-power control module now named uniquely for every component with a low-power interface to avoid compilation errors
- Documentation and/or coreTools changes:
  - None

Changes in 1.05a version of DW_axi_x2h

- RTL changes:
  - hgrant and hbusreq top-level signals now removed in AHB Lite mode; tied off correctly internally
  - Low-power handshaking interface changed to be consistent with new interface specification
- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.03 or later
  - Corrected names of include files and vcs command used for simulation in databook
  - Corrected syntax for undef directive
  - Added material for low-power interface functionality, signals, and parameters in databook
- Testbench
  - Packaged more testcases

Changes in 1.04a version of DW_axi_x2h

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Updated “Two Synchronous Clocks” section
  - Uses coreTools version 2008.06-SP2-2

Changes in 1.03d version of DW_axi_x2h

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2007.06-SP4

Changes in 1.03c version of DW_axi_x2h

- Uses coreTools version 2007.06-1 or later.
- Packaging fixed to enable USE_FOUNDATION parameter for all configurations.

Changes in 1.03b version of DW_axi_x2h

- Packaging issue that gives errors in the Configure Components step in cA if the user has only a source license has been corrected

Changes in 1.03a version of DW_axi_x2h

- Enhanced DW_axi_x2h databook to include coreAssembler intent in Chapter 2
- Legacy code was removed so that the DW_axi_x2h can use DC-Ultra
- Address range changed to a range of values from 32 to 64

Changes in 1.02a version of DW_axi_x2h

- Support for ID width up to 16 bits
- Full coreAssembler support, including subsystem creation, auto-connection of AXI/AHB buses and automatic subsystem testing
- Updated support for newer tools and DesignWare Verification IP
- AXI interface definitions 2.0 support
- Use of DesignWare BCM components (replaces DesignWare Building Blocks)

For a list of product features, refer to "Features" in the *DesignWare DW_axi_x2h Databook*.

2.4.8.2 DW_axi_x2h Releases

Table 2-9 lists the latest versions of the DW_axi_x2h component.

Table 2-9 DesignWare for AMBA 3 AXI/DW_axi_x2h Releases

DesignWare Release for AMBA 2/AMBA 3 AXI	DW_axi_x2h Version	Databook Date
2020.03a (AXI-only) with 2018.07a AMBA	2.04a	March 2020

DesignWare Release for AMBA 2/AMBA 3 AXI	DW_axi_x2h Version	Databook Date
2018.02a (AXI-only) with 2016.10a AMBA	2.03a	February 2018
2016.03a (AXI-only) with 2015.06a AMBA	2.02a	March 2016
2014.10a (AXI-only) with 2014.06a AMBA	2.01a	October 2014
2013.06a (AXI-only) with 2013.05a AMBA	2.00a	June 2013
2013.05a (AXI-only) with 2013.05a AMBA	1.07a	May 2013
2011.10a (AXI-only) with 2011.10a AMBA	1.06b	October 2011
2011.01a (AXI-only) with 2010.12a AMBA	1.06a	January 2011
2010.09a (AXI-only) with 2010.09a AMBA	1.05a	September 2010
2008.10a (AXI-only) with 2008.10a AMBA	1.04a	October 2008
2008.06a (AXI-only) with 2008.06a AMBA	1.03d	June 2008
2007.06a (AXI-only) with 2007.06a AMBA	1.03c	June 2007
2007.04a (AXI-only) with 2007.04a AMBA	1.03b	April 2007
2007.02a (AXI-only)	1.03a	February 2007
2006.04a (AXI-only)	1.02a	April 2006
with 2005.04a	1.01b	October 2005
with 2005.04a	1.01a	September 2005
with 2005.04a	1.00a	July 2005

2.4.8.3 DW_axi_x2h Known Problems and Workarounds

There are no known issues in this release of the DW_axi_x2h.

2.4.9 DW_axi_x2p

The following sections list the new features and changes, and the fixed problems and enhancements, for the DW_axi_x2p component. For DW_axi_x2p-specific STARs, refer to:

https://www.synopsys.com/dw/star.php?c=DW_axi_x2p

For detailed features description, see the *DW_axi_x2p databook*.

For information on known issues, refer to "DW_axi_x2p Known Problems and Workarounds" on page 207.

2.4.9.1 DW_axi_x2p New Features and Changes

This section describes what was new or had changed during the various versions of the DW_axi_x2p:

Changes in 2.04a version of DW_axi_x2p

- RTL Changes:
  - Design compliance to SpyGlass 2019.06-SP2 and GuideWare 2019.06
  - Discontinued Support for Synchronization depth parameter X2P_DUAL_CLK_SYNC_DEPTH = 1 (as cautioned in previous GA)
- Documentation changes
  - Refer to the Revision History of the DW_axi_x2p databook.
- Packaging changes:
  - STAR 3115176: Update sWork::evalInComponent to align with coreTools version 2018.09-SP2.
  - Minor packaging updates.

Changes in 2.03a version of DW_axi_x2p

- RTL changes:
  - RTL compliance to SpyGlass 2017.03-SP-1 and GuideWare 2017.03
- Documentation and/or coreTools changes:
  - Version update
  - Updated synthesis results in Integration Considerations chapter of the databook
  - Published the first version of DesignWare Synthesizable Components for AMBA 3 AXI, and AMBA 4 AXI user guide
  - Removed chapter 2 Building and Verifying a Component or Subsystem from the databook and added the content in the newly created user guide
  - Signals, Parameters, and Internal Parameters chapters auto-extracted with change bars from the RTL
  - Uses coreTools version N-2017.12-SP1-3
- Packaging changes:
  - Minor packaging enhancements

- Removed support for NC Verilog Simulator and MTI Simulator

Changes in 2.02a version of DW_axi_x2p

- RTL changes:
  - Lint cleanup
- Documentation and/or coreTools changes:
  - Version update
  - Signals chapter auto-extracted from the RTL
  - Parameters chapter auto-extracted from the RTL
  - Uses coreTools version 2015.06-SP3-1
  - Updated the performance section in the Integration Consideration chapter
- Packaging changes:
  - Minor packaging enhancements

Changes in 2.01a version of DW_axi_x2p

- RTL changes:
  - Lint cleanup
  - Added the new X2P_ALLOW_SPARSE_TRANSFER parameter
  - Enhanced to support AXI transactions size less than APB data bus width and sparse write data transfers
  - Fixed address increment logic when AXI data width is set to 8
- Documentation and/or coreTools changes:
  - Version update
  - Uses coreTools version 2014.03-SP1-1
  - Updated the performance section in the Integration Considerations chapter
  - Added the new AXI-to-APB Sparse Transfers section
- Packaging changes:
  - Minor packing enhancements

Changes in 2.00a version of DW_axi_x2p

- RTL changes:
  - Implemented support for the AMBA 4 AXI interface
- Documentation and/or coreTools changes:
  - Updated the databook with new and modified signals and parameters implemented for the AMBA 4 AXI interface
  - Uses coreTools version 2013.03-SP1-1
- Packaging changes:
  - None

Changes in 1.08c version of DW_axi_x2p

- RTL changes:
  - Fixed a bug to ensure that the pslverr signal is sampled only when the penable and pready signals are high
- Documentation and/or coreTools changes:
  - Made a minor correction in the description of the X2P_APB_ADDR_WIDTH parameter
  - Corrected the penable signal in two figures
  - Updated the databook template
  - Uses coreTools version 2012.06-SP2
- Packaging changes:
  - Corrected file prefixing in the encrypted mode

Changes in 1.07b version of DW_axi_x2p

- RTL changes:
  - Fixed problem whereby unused parameters were visible in coreConsultant GUI
  - Fixed problem whereby start and end address did not update when address map changed
- Testbench changes:
  - Fixed problem whereby BCM21 inserted missamples with DW_MODEL_MISSAMPLES defined
- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.09-SP2
  - Updated system diagram in Figure 1-1
  - Enhanced “Related Documents” section in Preface

Changes in 1.07a version of DW_axi_x2p

- RTL changes:
  - Fix to RTL in low-power controller to avoid ELAB-985 synthesis warnings (no logic in always process)
  - Fixed naming of generate block
  - Low-power control module now named uniquely for every component with a low-power interface to avoid compilation errors
- Documentation and/or coreTools changes:
  - None

Changes in 1.06a version of DW_axi_x2p

- RTL changes:
  - Fixed support for configuring APB slaves with up to 64-bit addresses
  - Parameters X2P_AXI_START_ADDR and X2P_AXI_END_ADDR removed because they are redundant
- Documentation and/or coreTools changes:
  - Added support for address range configuration of APB Slaves attached to DW_axi_x2p in 64-bit format

Changes in 1.05a version of DW_axi_x2p

- RTL changes:
  - Low-power handshaking interface changed to be consistent with new interface specification
  - Fixed command queue depth to be set by X2P_CMD_QUEUE_DEPTH instead of X2P_WRITE_RESP_BUFFER_DEPTH
- Documentation and/or coreTools changes:
  - Uses coreTools version 2010.03 or later
  - Removed bullet at beginning of chapter one in databook saying that DW_axi_x2p supports APB master
  - Corrected names of include files and vcs command used for simulation in databook
  - Corrected syntax for undef directive
  - Added material for low-power interface functionality, signals, and parameters in databook

Changes in 1.04a version of DW_axi_x2p

- Testbench changes:
  - Fixed issue with testbench address variables defined as integers, which caused false failures when they were interpreted as signed numbers

- RTL changes:
  - PSLVERR_Sx is no longer sampled in order to detect error when PREADY_Sx = 0
- Documentation and/or coreTools changes:
  - Uses coreTools version 2009.06-SP1-1

Changes in 1.02b version of DW_axi_x2p

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Text removed relating to generation of a decode error from the address of the next APB beat

Changes in 1.02a version of DW_axi_x2p

- RTL changes:
  - Corrected operation to prevent ERROR response on reads to last location in address space
- Documentation and/or coreTools changes:
  - Uses coreTools version 2008.06-SP2-2

Changes in 1.01b version of DW_axi_x2p

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2007.06-SP4

Changes in 1.01a version of DW_axi_x2p

- The X2P_AXI_ENDIANNESS parameter in coreAssembler was corrected from read only to read/write, and was associated with the AXI interface instead of the APB interface.
- The RTL has been cleaned up to remove warnings reported by the Leda Lint tool.

Changes in 1.00c version of DW_axi_x2p

- Uses coreTools version 2007.06-1 or later.

Changes in 1.00b version of DW_axi_x2p

- Enhanced DW_axi_x2p databook to include coreAssembler intent in Chapter 2
- DW_axi_x2p databook now clearly states that the DW_axi_x2p can connect from 1 to 16 APB slaves; Figure 13 corrected

- Endian diagram improved in databook
- DW_axi_x2p no longer requires a Vera license

For a list of product features, refer to "Features" in the *DesignWare DW_axi_x2p Databook*.

2.4.9.2 DW_axi_x2p Releases

Table 2-10 lists the latest versions of the DW_axi_x2p component.

Table 2-10 DesignWare for AMBA 3 AXI/DW_axi_x2p Releases

DesignWare Release for AMBA 2/AMBA 3 AXI	DW_axi_x2p Version	Databook Date
2020.03a (AXI-only) with 2018.07a AMBA	2.04a	March 2020
2018.02a (AXI-only) with 2016.10a AMBA	2.03a	February 2018
2016.03a (AXI-only) with 2015.06a AMBA	2.02a	March 2016
2014.10a (AXI-only) with 2014.06a AMBA	2.01a	October 2014
2013.06a (AXI-only) with 2013.05a AMBA	2.00a	June 2013
2013.05a (AXI-only) with 2013.05a AMBA	1.08c	May 2013
2011.10a (AXI-only) with 2011.10a AMBA	1.07b	October 2011
2011.01a (AXI-only) with 2010.12a AMBA	1.07a	January 2011
2010.11a (AXI-only) with 2010.09a AMBA	1.06a	November 2010
2010.09a (AXI-only) with 2010.09a AMBA	1.05a	September 2010
2010.04a (AXI-only) with 2010.03a AMBA	1.04a	April 2010
2009.03a (AXI-only) with 2008.10a AMBA	1.02b	March 2009
2008.10a (AXI-only) with 2008.10a AMBA	1.02a	October 2008
2008.06a (AXI-only) with 2008.06a AMBA	1.01b	June 2008

DesignWare Release for AMBA 2/AMBA 3 AXI	DW_axi_x2p Version	Databook Date
2007.10a	1.01a	October 2007
2007.06a (AXI-only) with 2007.06a AMBA	1.00c	June 2007
2007.04a (AXI-only) with 2007.04a AMBA	1.00b	April 2007
2007.02a (AXI-only)	1.00b	February 2007
2006.10a (AXI-only) with 2005.04a AMBA	1.00a	October 2006

2.4.9.3 DW_axi_x2p Known Problems and Workarounds

There are no known issues in this release of the DW_axi_x2p.

2.4.10 DW_axi_x2x

The following sections list the new features and changes, and the fixed problems and enhancements, for the DW_axi_x2x component. For DW_axi_x2x-specific STARs, refer to:

https://www.synopsys.com/dw/star.php?c=DW_axi_x2x

For detailed feature description, see the *DW_axi_x2x databook*.

For information on known issues, refer to "DW_axi_x2x Known Problems and Workarounds" on page 213.

2.4.10.1 DW_axi_x2x New Features and Changes

This section describes what was new or had changed during the various versions of the DW_axi_x2x:

Changes in 1.08a version of DW_axi_x2x

- RTL Changes:
  - Design compliance to SpyGlass 2019.06-SP2 and GuideWare 2019.06
    - Discontinued Support for Synchronization depth parameters X2X_MP_SYNC_DEPTH = 1 and X2X_SP_SYNC_DEPTH = 1 (as cautioned in previous GA)
- Documentation changes
  - Refer to the Revision History of the DW_axi_x2x databook.
- Packaging changes:
  - STAR 3115176: Update sWork::evalInComponent to align with coreTools version 2018.09-SP2.
  - Minor packaging updates.

Changes in 1.07a version of DW_axi_x2x

- RTL changes:
  - RTL compliance to SpyGlass 2017.03-SP-1 and GuideWare 2017.03
- Documentation and/or coreTools changes:
- Updated synthesis results in Integration Considerations chapter of the databook
  - Version update
  - Published the first version of DesignWare Synthesizable Components for AMBA 3 AXI, and AMBA 4 AXI user guide
  - Removed chapter 2 Building and Verifying a Component or Subsystem from the databook and added the content in the newly created user guide
  - Signals, Parameters, and Internal Parameters chapters auto-extracted with change bars from the RTL
  - Uses coreTools version N-2017.12-SP1-3
- Packaging changes:
  - Minor packaging enhancements
- Removed support for NC Verilog Simulator and MTI Simulator

Changes in 1.06a version of DW_axi_x2x

- RTL changes:
  - Lint cleanup
- Documentation and/or coreTools changes:
  - Version update
  - Signals chapter auto-extracted from the RTL
  - Parameters chapter auto-extracted from the RTL
  - Uses coreTools version 2015.06-SP3-1
  - Updated the performance section in the Integration Consideration chapter
- Packaging changes:
  - Minor packaging enhancements

Changes in 1.05a version of DW_axi_x2x

- RTL changes:
  - Lint cleanup
- Documentation and/or coreTools changes:
  - Version update
  - Uses coreTools version 2014.03-SP1-1

  - Updated the performance section in the Integration Considerations chapter
- Packaging changes:
  - Minor packing enhancements
  - Fixed slave ID width dependency issue of X2X causing integration issues in coreAssembler

Changes in 1.04d version of DW_axi_x2x

- RTL changes:
  - None
- Documentation changes:
  - Uses coreTools version 2013.03-SP1-1
- Packaging changes:
  - None

Changes in 1.04c version of DW_axi_x2x

- RTL changes:
  - None
- Documentation changes:
  - Updated the databook template
  - Uses coreTools version 2012.06-SP2
- Packaging changes:
  - Corrected file prefixing in the encrypted mode

Changes in 1.04b version of DW_axi_x2x

- RTL changes:
  - Fixed problem whereby slave port ID width appeared to be editable when it was not
  - Fixed problem whereby for Extended Burst mode parameters were not enabled when needed
- Testbench changes:
  - Fixed problem whereby BCM21 inserted missamples with DW_MODEL_MISSAMPLES defined
- Documentation changes:
  - Uses coreTools version 2010.09-SP2
  - Updated system diagram in Figure 1-1
  - Enhanced “Related Documents” section in Preface
  - Added material for extended burst mode
  - Revised material regarding fan-out and burst length translation

Changes in 1.04a version of DW_axi_x2x

- RTL changes:
  - Fix to RTL in low-power controller to avoid ELAB-985 synthesis warnings (no logic in always process)
  - Fixed naming of generate block
  - Low-power control module now named uniquely for every component with a low-power interface to avoid compilation errors
  - Corrected Leda rule violations
  - Outstanding unique read and write ID limit increased from 32 to 64
  - Initial blocks wrapped in synopsys translate off pragmas removed from the RTL
- Documentation changes:
  - Increased legal X2X_MAX_UWIDA and X2X_MAX_URIDA values from 32 to 64

Changes in 1.03b version of DW_axi_x2x

- RTL changes:
  - Testbench fixed to remove clock correctly in testing of low-power interface
- Packaging changes:
  - Synthesis intent updated to fix bug with Waveform attribute setting on aclk_m
  - X2X_HAS_PIPELINE parameter now disabled when not required in coreTools
- Documentation changes:
  - Corrected value of X2X_CLK_MODE from 0 to 1 in “Quasi-Synchronous Clocking” section of databook
  - Equations for recommended minimum channel buffer depths fixed in “Channel Buffers” section
  - Documentation fixed to correctly describe when X2X_HAS_PIPELINE parameter is disabled

Changes in 1.03a version of DW_axi_x2x

- RTL changes:
  - Added low-power handshaking interface
  - Enhanced packaging to prevent illegal default component connections
  - Fixed synthesis constraints for quasi-synchronous clock configurations
  - Fixed RTL bug with respect to downsizing WRAP bursts, which wrap on a 4k boundary
- Documentation changes:
  - Uses coreTools version 2010.03 or later
  - Added discussion for X2X_HAS_WRAP_BURST regarding performance impact of supporting wrapped busts for resize configurations
  - Enhanced material for latency calculations

- names of include files and vcs command used for simulation in databook
- Corrected syntax for undef directive
- Added material for low-power interface functionality, signals, and parameters in databook
- Corrected typo in overview for Remap and Pause from Random Access Peripheral

Changes in 1.02c version of DW_axi_x2x

- RTL changes:
  - None
- Documentation changes:
  - Removed references to X2X_HAS_WI_FAN_OUT and X2X_HAS_NOPX parameters

Changes in 1.02b version of DW_axi_x2x

The following was new or changed in the 1.02b version of the DW_axi_x2x:

- RTL changes:
  - Grammatical changes to What's This descriptions in GUI
- Documentation changes:
  - DW_axi_x2x databook:
    - Matched Sideband Signals descriptions in parameters table with GUI descriptions
    - Added "Locking Sequences" section
    - Grammatical fix in X2X_MAX_UWIDA and X2X_MAX_URIDA descriptions

Changes in 1.02a version of DW_axi_x2x

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2008.06-SP2-2

Changes in 1.01d version of DW_axi_x2x

- RTL changes:
  - None
- Documentation and/or coreTools changes:
  - Uses coreTools version 2007.06-SP4

Changes in 1.01c version of DW_axi_x2x

- Uses coreTools version 2007.06-1 or later.

Changes in 1.01b version of DW_axi_x2x

- Design are now prefixed properly and simulate correctly within coreAssembler.

Changes in 1.01a version of DW_axi_x2x

- Enhanced databook includes coreAssembler intent in Chapter 2
- When the Master Port data width is less than the Slave Port data width, the DW_axi_x2x performs transaction upsizing or burst consolidation
- X2X_MAX_UWIDA and X2X_MAX_URIDA parameters maximum increased from 16 to 32 bits

For a list of product features, refer to "Features" in the *DesignWare DW_axi_x2x Databook*.

2.4.10.2 DW_axi_x2x Releases

Table 2-11 lists the latest versions of the DW_axi_x2x component.

Table 2-11 DesignWare for AMBA 3 AXI/DW_axi_x2x Releases

DesignWare Release for AMBA 2/AMBA 3 AXI	DW_axi_x2x Version	Databook Date
2020.03 (AXI-only) with 2018.07a AMBA	1.08a	March 2020
2018.02 (AXI-only) with 2016.10a AMBA	1.07a	February 2018
2016.03a (AXI-only) with 2015.06a AMBA	1.06a	March 2016
2014.10a (AXI-only) with 2014.06a AMBA	1.05a	October 2014
2013.06a (AXI-only) with 2013.05a AMBA	1.04d	June 2013
2013.05a (AXI-only) with 2013.05a AMBA	1.04c	May 2013
2011.10a (AXI-only) with 2011.10a AMBA	1.04b	October 2011
2011.01a (AXI-only) with 2010.12a AMBA	1.04a	January 2011
2010.11a (AXI-only) with 2010.09a AMBA	1.03b	November 2010
2010.09a (AXI-only) with 2010.09a AMBA	1.03a	September 2010
2009.03a (AXI-only) with 2008.10a AMBA	1.02c	March 2009

DesignWare Release for AMBA 2/AMBA 3 AXI	DW_axi_x2x Version	Databook Date
2009.01a (AXI-only) with 2008.10a AMBA	1.02b	January 2009
2008.10a (AXI-only) with 2008.10a AMBA	1.02a	October 2008
2008.06a (AXI-only) with 2008.06a AMBA	1.01d	June 2008
2007.06a (AXI-only) with 2007.06a AMBA	1.01c	June 2007
2007.04a (AXI-only) with 2007.04a AMBA	1.01b	April 2007
2007.02a (AXI-only)	1.01a	February 2007
2006.10a (AXI-only) with 2005.04a AMBA	1.00a	November 2006

2.4.10.3 DW_axi_x2x Known Problems and Workarounds

There are no known issues in this release of the DW_axi_x2x.

3 Pre-October 2007 AMBA 2 STARs

This appendix contains archived STAR tables for AMBA 2.

3.1 AMBA 2 STAR Archives

The following subsections contain archived STAR tables for the individual AMBA 2 components.

3.1.1 DW_ahb—Fixed Problems/Enhancements

The following tables describe the DW_ahb STARs that were fixed in each of the versions prior to October 2007.

Table 3-1 STAR(s) Fixed in DW_ahb Version 2.06b

STAR ID	Type	Description
9000186924	Bug	The “Use DesignWare foundation synthesis library” option does not work as expected with DesignWare and source license.

Table 3-2 STAR(s) Fixed in DW_ahb Version 2.06a

STAR ID	Type	Description
9000107668	Enhancement	Register descriptions included in SPIRIT files

Table 3-3 STAR(s) Fixed in DW_ahb Version 2.05a

STAR ID	Type	Description
9000122563	Bug	During a locked transfer sequence, if the last locked transfer is given a RETRY and the master that has removed the hbusreq and hlock fails to make them active during the RETRY command, the arbiter in the DW_ahb incorrectly generates a hmastlock transfer on the following cycle. This DW_ahb 2.05a release fixes this issue and correctly waits for the hlock/hbusreq to become active before driving hmastlock.
9000096835	Bug	When using Design Compiler 2005.09-SP1 and Formality 2005.09-SP1, Formality produces the following error when using DW_ahb version 2.04a in both coreConsultant and coreAssembler. FM-089 (error) RTL interpretation messages were produced during %s. Verification results may disagree with a logic simulator. Workaround: Add the following variable to the beginning of the Formality script to treat the message as a warning instead of an error: `set hdlin_warn_on_mismatch_message FMR_VLOG-091` When you run Formality again, it passes in both coreConsultant and coreAssembler with only a warning message.
9000071543	Bug	When weighted token arbitration is turned on (off by default), it is possible to configure the Master Token Counts feature in coreConsultant such that test_10_token fails with a DW VIP AHB Master timeout. The configured RTL is functionally correct, but the test time-outs are set too short. Workaround: To work around this problem and verify functionality, you can temporarily reduce the Master Token Counts to smaller values. This change ensures that test_10_token confirms that the weighted token arbitration configuration is functioning correctly (the timeout is no longer reached). You can then reset the Master Token Counts to the desired (higher) values to generate the RTL for use in the final design.

STAR ID	Type	Description
9000113073	Bug	DW_ahb reads back incorrect values for the AHB_TCL and AHB_CL_M(i) registers when the configuration parameters AHB_WTEN (include weighted token arbitration) and EBTEN (include early burst termination) are set to False (0). However, when these parameters are set to False, writing to the Early Burst Termination Count registers (EBTCOUNT, EBT_EN, and EBT) and Weighted-token Arbitration registers (WTEN, AHB_TCL, and AHB_CL_M[i]) should have no affect and read back as 0. When DW_ahb reads back AHB_TCL, it returns the default value of the AHB_TCL configuration parameter. Similarly, when the component reads back AHB_CL_M[i] registers, it returns the default values of AHB_CL_M(i) (i=1 to NUM_AHB_MASTERS) configuration parameter. This is incorrect behavior.

Table 3-4 STAR(s) Fixed in DW_ahb Version 2.04a

STAR ID	Type	Description
9000051190	Bug	The following error occurs when you use the 2004.06 version of DC-FPGA synthesis for DW_ahb 2.03a and coreTools 4.3.1 with Xilinx library: Error: The state vector cell current_state_reg[1] is not in the design. (FSM_GRP-59) Workaround: Upgrade coreTools to version 4.4.1 to resolve this issue.

Table 3-5 STAR(s) Fixed in DW_ahb Version 2.03a

STAR ID	Type	Description
There are no customer STARs fixed in this version of DW_ahb.		

Table 3-6 STAR(s) Fixed in DW_ahb Version 2.02a

STAR ID	Type	Description
9000005294	Bug	If a user selects 64 bit addressing for the DW_ahb, coreConsultant doesn't allow for the creation of 64 bit memory maps. The GUI limits memory map entries to 32 bits. This bug is fixed for release 2.02a

STAR ID	Type	Description
STS0180555	Enhancement	DW_ahb “Lite” has floating outputs. The wires hready_resp_s0, hresp_s0, and hrdata_s0, have been removed at the top component level for the “Lite” configuration.
STS0181156	Bug	Running DW_ahb batch files in coreConsultant can fail. There is a bug in coreConsultant (STAR 180984), which can cause the configuration of the DW_ahb to fail. There are many workarounds (see below). The reason why this duplicate STAR is being filed is to allow users to see the technical note on the internet. The problem can show up when you source a batch script with the GUI open to a dialog that is being modified by the batch script. The problem is fixed in version 4.1.5 of coreConsultant. Following are a number of possible workarounds. 1) Run the whole script in batch instead of the GUI. 2) Separate the workspace creation from the rest of the script. If the workspace is created with the GUI, switch back to the prefixing activity and source the batch script. Since the configuration GUI is not shown, the problem would not be present. 3) Manual completion of Specify Configuration. Remove everything after (and including) the auto-complete of SpecifyConfiguration and do that part interactively. 4) Add the line “gui_start” after “autocomplete_activity SpecifyConfiguration”. Start the tool in batch mode and source the script (coreConsultant -f dw_ahb.config). The GUI starts up after the configuration has been generated and works fine

Table 3-7 STAR(s) Fixed in Release 2003.10 (DW_ahb 2.01a)

STAR ID	Type	Description
165636	Bug	Large configurations of DW_ahb fail the test_10_token. This test failure is due to a timeout on the test that is too small.
167505	Bug	Simulation fails with gtech netlist. Description: When simulating with the gtech netlist produced by coreConsultant with clk set to 10ns, simulation fails with timing violations. Users should use the “zero_delay_mode” switch to get a zero-delay simulation, and not rely on the netlist to set this mode because some users may want to use unit delay mode.
169470	Bug	DW_ahb arbiter grants the bus to a different master which is in the middle of a burst transfer if the last transfer from the previous bus master receives a split response and then the current master drives a busy transfer.
169788	Bug	DW_ahb simulations fail if boot/normal memory maps overlap.

STAR ID	Type	Description
171204 (168318)	Bug	DW_ahb configuration error. When configuring the AHB without enabling the “support AMBA Memory remap feature”, there is an error message if the “total number of slave select lines” in the system is less than 4 because the default number of “AHB slave ports in Normal mode” is 4. This can be worked around by temporarily enabling the Memory remap feature, and changing the Number of AHB Slave ports in Normal mode to desire value.
173497	Bug	Ability to change frequency in verification activity causing problems. Description: the ability to change the clock frequency in the simulation activity is meaningless because the simulation does not take timing into account. This option was removed altogether.

Table 3-8 STAR(s) Fixed in 2003.02 Release (DW_ahb 2.00a)

STAR ID	Type	Description
143029	Enhancement	Endianness should be bootable (controlled by an external pin so that endianness can be set at boot time).
149865	Enhancement	Want pause mode to hold off until end of current transaction.
155458	Enhancement	Need Revision ID registers in DesignWare IIP components.

Table 3-9 STAR(s) Fixed in 2002.08-SP1-4 Release (DW_ahb 1.13a)

STAR ID	Type	Description
161698	Bug	This error affects users running formal verification with certain configurations of the DW_ahb. Due to a coding error, Formality cannot read in the RTL in certain configurations of the DW_ahb. The coding error does not produce bad logic, but it inhibits users from running formal verification.

Table 3-10 STAR(s) Fixed in 2002.08-SP1-2 (DW_ahb 1.12a)

STAR ID	Type	Description
154678	Bug	Problems with C header files (for all DesignWare IIP components). What Happens: Valid C constructs are not being used in the header files and are causing compile problems. Some of the components do not have C or Verilog header files. Need to be consistent throughout platform.

STAR ID	Type	Description
159465	Bug	This error only applies if Early Burst Termination is enabled within the DW_ahb, AND you perform locked transfers. What Happens: A master that is performing a locked transfer has its grant incorrectly removed by the arbiter if a previous unlocked transfer had exceeded the permitted burst length on the bus. Additionally, the unlocked transfer that exceeds the permitted burst length must complete successfully before the arbiter has a chance to remove its grant. The sequence of events that show this problem are the following: 1)Master A initiates a burst transfer in a system where EBT is enabled. 2)Master A exceeds permitted burst length. 3)It takes the DW_ahb arbiter a cycle to recognize that the permitted burst length has been surpassed and remove the grant to Master A. During this cycle, Master A successfully finishes its burst transfer and initiates a locked transfer. 4)The DW_ahb arbiter now incorrectly removes the grant to Master A and gives it to the dummy master since Master A previously had exceeded the permitted burst length on the bus.
159467	Bug	This error only affects you if you have split/retry transfers AND perform back-to-back transfers of the types unlocked to locked with the same master. What happens: A single master is performing back-to-back transfers on the bus where the first transfer is unlocked (split) and the following transfer is locked. At the beginning of the locked transfer the DW_ahb arbiter correctly asserts hmastlock. If the last beat of the unlocked transfer is split or retried then the DW_ahb arbiter incorrectly maintains hmastlock for the locked transfer. The DW_ahb arbiter should remove the lock (de-assert hmastlock) until the split/retry transaction is completed. The maintaining of hmastlock is incorrect behavior only if a single master is driving the back-to-back transfers. If one master drives the unlocked transfer and another master drives the subsequent locked transfer, the DW_ahb arbiter is correct in maintaining the hmastlock signal.

3.1.2 DW_ahb_dmac—Fixed Problems/Enhancements

The following tables describe the DW_ahb_dmac STARs that were fixed in each of the versions prior to October 2007.

Table 3-11 STAR(s) Fixed in DW_ahb_dmac Version 2.10b

STAR ID	Type	Description
9000186924	Bug	The “Use DesignWare foundation synthesis library” option does not work as expected with DesignWare and source license.

Table 3-12 STAR(s) Fixed in DW_ahb_dmac Version 2.10a

STAR ID	Type	Description
9000168967	Enhancement	User can select a VIP/VMT version from a pull-down menu in the coreConsultant GUI
9000107668	Enhancement	Register descriptions included in SPIRIT files

STAR ID	Type	Description
9000163151	Bug	More clarification added in the databook on dmac handling of 1KB addressing boundary for AHB accesses

Table 3-13 STARs Fixed in DW_ahb_dmac Version 2.09a

STAR ID	Type	Description
9000143503	Bug	In cA, with DMAC source license, DWF option (USE_FOUNDATION) is grey'd out. If you do not want to use DesignWare Foundation Building Block Library parts in your design, you cannot change this option, which is not the expected behavior with source license.
9000142830	Bug	When the user has a DesignWare license or source license and the DWF option is selected, DW_ahb_dmac gives the following VCS warning during compilation: Warning-[PCWM] Port connection width mismatch

Table 3-14 STARs Fixed in DW_ahb_dmac Version 2.08a

STAR ID	Type	Description
9000117756	Enhancement	Request for endianness port in DW_ahb_dmac. Endianness can now be statically configured through coreConsultant or dynamically via pins on the I/O. For static configurations, the new coreConsultant DMAH_STATIC_ENDIAN_SELECT parameter controls the endianness of all AHB master interfaces and the AHB slave interface. For dynamic configurations, individual pins for each of the AHB master interfaces and one for the AHB slave interface control the endianness; the pins are, dma_big_endian_m1 … dma_big_endian_m4 and dma_big_endian_slv.

Table 3-15 STARs Fixed in DW_ahb_dmac Version 2.06a

STAR ID	Type	Description
9000027236	Bug	DW_ahb_dmac RTL has SystemVerilog keywords. DW_ahb_dmac top-level module has an output called “int”, a SystemVerilog keyword. SystemVerilog enables compilation stops as soon as it sees this. There are several possible workarounds for this issue. ■ You can create a wrapper module to convert SystemVerilog port to Verilog names. ■ You should not “mix” SystemVerilog .sv files and Verilog .v files together. They need to be kept separate. Therefore, the following VCS compile time options forces VCS to use the Verilog 1995 and/or Verilog 2001 namespace: +systemverilogext+.sv +verilog2001ext+.v +verilog1995ext+.v ■ When instantiating, use pass-by-position instead of pass-by-dot notation.

STAR ID	Type	Description
9000046843	Bug	If you have the DesignWare source license for the DW_ahb_dmac and you choose to clear the configuration check-box for Use DW Foundation Synthesis Library, not all the required DesignWare Building Block (DWBB) files are written out; the DWbb_ram_r_w_s_dff.v file is missing. If you need this file for your design, you should contact the Support Center. Reference this STAR through the following: https://solvnet.synopsys.com/EnterACall Product: DW Library IP Sub-Product: AMBA
9000050218	Bug	There is a script conflict that causes the following: ■ Crashes Design Compiler if you try (in TCL mode) to synthesize using “Parallel job CPU limit” with more than one processor ■ Might cause Formality to fail If you encounter this problem, try using this suggested workaround: 1. Before running synthesis or formal verification, go to *installation_area*/syn/auxScripts/DW_ahb_dmac/pkg/pkg_script 2. Modify the following files by removing the line referring to set_svf: set_parameter_template_variable.tcl set_parameter_template_variable.dcsh 3. Save the file(s); then you can run synthesis or formal verification. You can do the same modification from any workspace, since these files in the workspace are soft links to the installation area.

Table 3-16 STARs Fixed in DW_ahb_dmac Version 2.04a

STAR ID	Type	Description
9000016301	Bug	(Databook) Read-only registers in AHB Slave Test Mode The databook description for DmaTestReg[TEST_SLV_IF] says that when this bit is set to 1, it puts the AHB slave interface into a test mode where the reaack value of all registers always match the value written. The above description is true only for writable registers; it is not true for read-only registers of DW_ahb_dmac. The read-only registers cannot be written even in this test mode. This has been corrected in the databook.
9000016757	Bug	(Databook) Interrupt Raw Status registers are R/W, not read-only. The databook mentions that the RawBlock, RawDstTran, RawErr, RawSrcTran, and RawTfr registers are read-only registers, whereas they are actually implemented as R/W in the DW_ahb_dmac core. The databook has been corrected.

STAR ID	Type	Description
9000017758	Bug	DMA transaction length error. For multi-block transfers where the peripheral is not flow controller and is a non-memory peripheral, then for the second and subsequent blocks of the multi-block transfer, single transactions are executed instead of burst transactions if dma_single signal is asserted before dma_req (For s/w handshaking the condition is if the single register is written to before the request register). Correct functional behavior is now implemented, that ONLY a burst transaction be executed when the device is not the flow controller when it is outside the 'end of block' region.
9000019231	Bug	No effect on CTL[INT_EN] bit disable. The DW_ahb_dmac channel interrupt enable bit (CTL0.INT_EN) had no effect on the output interrupt signal when disabled. When the CTL[INT_EN] bit is high, it is supposed to enable all interrupts, according to their respective mask bits; when low, it is supposed to disable all interrupts. This behavior, when low, was not happening correctly.
9000020073	Bug	(Databook) DMAH_CHx_LMS value. There is no entry for the DMAH_CHx_LMS parameter in Table 38, Appendix F of the databook. The databook has been fixed--parameter value is 4 (NO_HARDCODE).
9000020952	Bug	Possible Deadlock When Destination Is Flow Controller. Under the following corner case conditions, the source and destination block transfers sometimes completed with no data corruption, but the source state machine got stuck depending on these type of transfer: * Source and destination are on different layers; * Destination is not memory; * Destination is flow controller; * Prefetching is enabled (fcmode = 0); and * Source status fetching is disabled If a single block transfer, then the transfer did not move on to the next block transfer. If this is the last block in the DMA transfer, then the channel enable bit remained asserted.

Table 3-17 STARs Fixed in DW_ahb_dmac Version 2.03a

STAR ID	Type	Description
9000011731	Bug	DW_ahb_dmac fails to complete the block transfer when destination peripheral is flow controller and data prefetching is disabled When the destination peripheral is the flow controller and data prefetching is disabled – that is, CFG[fcmode] = 1) – then once the destination peripheral asserts dma_last (hardware handshaking) or the software writes to the last register, then the DW_ahb_dmac immediately assumes that it has completed the block transfer from the source, even though more data must to be fetched from the source to complete the block transfer to the destination. This bug occurs only when there is more than one hclk cycle between the assertion of dma_last and the assertion of dma_req. The overall effect of this is that the DMA block transfer stalls.
9000013278	Enhancement	In order to make DW_ahb_dmac consistent with other DesignWare IIP components, the coreConsultant parameter for DW_ahb_dmac for the interrupt polarity DMAH_INTR_POL has been changed. * The coreConsultant GUI label is now “Are interrupts active high?” * The parameter value of 0 means active-low, and a value of 1 means active-high. (Previously, a value of 1 was active-low, and a value of 0 was active-high.)
STS0185535	Bug	Missing coreConsultant parameter in C and Verilog header files: The DMAH_CHx_MULTI_BLK_TYPE (x = 0 to 7) parameters are missing in the C and Verilog header files. DMAH_CHx_CTL_WB_EN x = 0 to 7 and DMAH_ADD_ENCODED_PARAMS are also missing. These parameters are now available in the C and Verilog header files.

Table 3-18 STARs Fixed in DW_ahb_dmac Version 2.02a

STAR ID	Type	Description
183949	Bug	Data is lost when dma_last and error response occur on the same cycle. This bug only occurs when: ■ Destination of any channel is flow controller; for example, Channel *x*. ■ Data prefetching is enabled for Channel *x*; for example, fcmode = 0. ■ Error response can be returned to a different channel; for example, channel y. DMAH_CHy_NON_OK = True This bug appears when: ■ Channel *y* is active on the bus and an ERROR response for channel *y* is on the AHB bus. ■ On the SAME cycle, the handshaking interface assigned to the destination of Channel *x* asserts dma_last. ■ If this is the last transaction in the DMA transfer of Channel *x* and source of Channel *x* has prefetched enough data to complete DMA transfer on Channel *x* then: ■ Bug: The error response for Channel *y* causes Channel *x*'s DMA transfer to complete before the last transaction to the destination has completed; therefore, data is lost on Channel *x*. Workaround: Do not program DMAC prefetching when the destination is flow controller.

STAR ID	Type	Description
183951	Bug	DMA transfer may stall if destination is flow controller and prefetching is enabled. Bug only occurs if DMAH_NUM_CHANNELS >= 3. Description: For instance, if you have a 3-channel device, channels 0, 1, and 2. This bug occurs under the following conditions: ■ If destination is flow controller of Channel 0 and Channel 0 has data prefetching enabled, for example, fcmode = 0. ■ If, when the source of Channel 0 is active on the AHB bus, the handshaking interface assigned to the destination of Channel 0 asserts dma_last on the same cycle as the last beat of the INCR burst belonging to the source of Channel 0. ■ The source has prefetched enough data to complete the transfer on channel-0. ■ Channel-1 gains ownership of the master interface and requests a INCR burst of length 1. (No idle cycle on master bus handover between channel-0 and channel-1). ■ The data phase of the last beat from channel-0 is wait-stated by a single cycle. ■ The address phase of the INCR burst of length 1 for channel-1 completes and channel-2 gains ownership of the master bus interface (Again no idle cycle on master bus handover between channel-0 and channel-1). Bug: The master bus interface cancels this request from Channel 2 but Channel 2 state machines are unaware of this and are awaiting some response from the master bus interface, which never comes because Channel 2 is in deadlock and the DMA transfer cannot complete on Channel 2. Workaround: Do not program the DW_ahb_dmac to enable prefetching when the destination is flow controller.
184318	Bug	The hlock signal is incorrectly asserted. When an active channel that has bus locking enabled is disabled by software over the slave interface, the hlock signal remains asserted until a burst belonging to a different channel is started over the master bus interface. This bug occurs only if the active channel is disabled over the slave interface on the same cycle that the channel is granted the master bus interface to perform a burst.
184959	Bug	Incorrect reset values for CTL register are documented incorrectly in the DW_ahb_dmac Databook dated December 4, 2003. The databook lists the values as: TT_FC[0] = 1'b0 TT_FC[1] = DMAH_CH*x*_FC[1] & (!DMAH_CH*x*_FC[0]) TT_FC[2] = DMAH_CH*x*_FC[1] ^ DMAH_CH*x*_FC[0] The correct values are: TT_FC[0] = 1'b1 TT_FC[1] = DMAH_CH*x*_FC[1] || (!DMAH_CH*x*_FC[0]) TT_FC[2] = DMAH_CH*x*_FC[1] ^ DMAH_CH*x*_FC[0]

Table 3-19 STARs Fixed in DW_ahb_dmac Version 2.04a

STAR ID	Type	Description
9000011731	Bug	DW_ahb_dmac fails to complete the block transfer when destination peripheral is flow controller and data prefetching is disabled When the destination peripheral is the flow controller and data prefetching is disabled – that is, CFG[fcmode] = 1) – then once the destination peripheral asserts dma_last (hardware handshaking) or the software writes to the last register, then the DW_ahb_dmac immediately assumes that it has completed the block transfer from the source, even though more data must to be fetched from the source to complete the block transfer to the destination. This bug occurs only when there is more than one hclk cycle between the assertion of dma_last and the assertion of dma_req. The overall effect of this is that the DMA block transfer stalls.
9000013278	Enhancement	In order to make DW_ahb_dmac consistent with other DesignWare IIP components, the coreConsultant parameter for DW_ahb_dmac for the interrupt polarity DMAH_INTR_POL has been changed. * The coreConsultant GUI label is now “Are interrupts active high?” * The parameter value of 0 means active-low, and a value of 1 means active-high. (Previously, a value of 1 was active-low, and a value of 0 was active-high.)
STS0185535	Bug	Missing coreConsultant parameter in C and Verilog header files: The DMAH_CHx_MULTI_BLK_TYPE (x = 0 to 7) parameters are missing in the C and Verilog header files. DMAH_CHx_CTL_WB_EN x = 0 to 7 and DMAH_ADD_ENCODED_PARAMS are also missing. These parameters are now available in the C and Verilog header files.

Table 3-20 STARs Fixed in DW_ahb_dmac Version 2.02a

STAR ID	Type	Description
183949	Bug	Data is lost when dma_last and error response occur on the same cycle. This bug only occurs when: ■ Destination of any channel is flow controller; for example, Channel *x*. ■ Data prefetching is enabled for Channel *x*; for example, fcmode = 0. ■ Error response can be returned to a different channel; for example, channel y. DMAH_CHy_NON_OK = True This bug appears when: ■ Channel *y* is active on the bus and an ERROR response for channel *y* is on the AHB bus. ■ On the SAME cycle, the handshaking interface assigned to the destination of Channel *x* asserts dma_last. ■ If this is the last transaction in the DMA transfer of Channel *x* and source of Channel *x* has prefetched enough data to complete DMA transfer on Channel *x* then: ■ Bug: The error response for Channel *y* causes Channel *x*'s DMA transfer to complete before the last transaction to the destination has completed; therefore, data is lost on Channel *x*. Workaround: Do not program DMAC prefetching when the destination is flow controller.

STAR ID	Type	Description
183951	Bug	DMA transfer may stall if destination is flow controller and prefetching is enabled. Bug only occurs if DMAH_NUM_CHANNELS >= 3. Description: For instance, if you have a 3-channel device, channels 0, 1, and 2. This bug occurs under the following conditions: ■ If destination is flow controller of Channel 0 and Channel 0 has data prefetching enabled, for example, fcmode = 0. ■ If, when the source of Channel 0 is active on the AHB bus, the handshaking interface assigned to the destination of Channel 0 asserts dma_last on the same cycle as the last beat of the INCR burst belonging to the source of Channel 0. ■ The source has prefetched enough data to complete the transfer on channel-0. ■ Channel-1 gains ownership of the master interface and requests a INCR burst of length 1. (No idle cycle on master bus handover between channel-0 and channel-1). ■ The data phase of the last beat from channel-0 is wait-stated by a single cycle. ■ The address phase of the INCR burst of length 1 for channel-1 completes and channel-2 gains ownership of the master bus interface (Again no idle cycle on master bus handover between channel-0 and channel-1). Bug: The master bus interface cancels this request from Channel 2 but Channel 2 state machines are unaware of this and are awaiting some response from the master bus interface, which never comes because Channel 2 is in deadlock and the DMA transfer cannot complete on Channel 2. Workaround: Do not program the DW_ahb_dmac to enable prefetching when the destination is flow controller.
184318	Bug	The hlock signal is incorrectly asserted. When an active channel that has bus locking enabled is disabled by software over the slave interface, the hlock signal remains asserted until a burst belonging to a different channel is started over the master bus interface. This bug occurs only if the active channel is disabled over the slave interface on the same cycle that the channel is granted the master bus interface to perform a burst.
184959	Bug	Incorrect reset values for CTL register are documented incorrectly in the DW_ahb_dmac Databook dated December 4, 2003. The databook lists the values as: TT_FC[0] = 1'b0 TT_FC[1] = DMAH_CH*x*_FC[1] & (!DMAH_CH*x*_FC[0]) TT_FC[2] = DMAH_CH*x*_FC[1] ^ DMAH_CH*x*_FC[0] The correct values are: TT_FC[0] = 1'b1 TT_FC[1] = DMAH_CH*x*_FC[1] || (!DMAH_CH*x*_FC[0]) TT_FC[2] = DMAH_CH*x*_FC[1] ^ DMAH_CH*x*_FC[0]

Table 3-21 STARs Fixed in DW_ahb_dmac Version 2.01a

STAR ID	Type	Description
178639	Enhancement	This release has significant performance (approximately 30-40% area reduction and improved timing) over the previous release.

Table 3-22 STARs Fixed in 2002.08-SP1-4 Release (DW_ahb_dmac 1.03a)

STAR ID	Type	Description
161849	Bug	Affects locked transfers through DW_ahb_icm. When a locked transfer is retried because the layer is held off too long by a transfer on another layer, the input stage stores an IDLE transfer when it should not store anything. Because of this, it is unable to store the following NSEQ transfer, so it misses this transfer completely. Storing the IDLE transfer causes the DW_ahb_icm to allow a burst start with a SEQ transfer rather than a NSEQ transfer, which is a violation. The IDLE transfer is stored because the hmastlock is not cancelled until the second phase of the RETRY transfer and the hmastlock is used to keep the input stage held until the layer gets access to the shared slave. This bug has been in all previous versions of the DW_ahb_icm. Workaround: There is no work around apart from upgrading the device to version 1.03a.

3.1.3 DW_ahb_eh2h—Fixed Problems/Enhancements

The following tables describe the DW_ahb_eh2h STARs that were fixed in each of the versions prior to October 2007.

Table 3-23 STAR(s) Fixed in DW_ahb_eh2h Version 1.04b

STAR ID	Type	Description
9000170890	Bug	DW_ahb interface needs to be exported in coreAssembler to modify NumSelectSlots.

Table 3-24 STAR(s) Fixed in DW_ahb_eh2h Version 1.04a

STAR ID	Type	Description
9000168967	Enhancement	User can select a VIP/VMT version from a pull-down menu in the coreConsultant GUI
9000107668	Enhancement	Register descriptions included in SPIRIT files

Table 3-25 STAR(s) Fixed in DW_ahb_eh2h Version 1.03a

STAR ID	Type	Description
9000059928	Bug	The USE_FOUNDATION parameter was removed, since equivalent DWBB parts are used by default.
9000126878	Enhancement	SystemVerilog support was added.

Table 3-26 STAR(s) Fixed in DW_ahb_eh2h Version 1.02a

STAR ID	Type	Description
There are no customer STARs fixed in this version of DW_ahb_eh2h		

Table 3-27 STAR(s) Fixed in DW_ahb_eh2h Version 1.01a

STAR ID	Type	Description
There are no customer STARs fixed in this version of DW_ahb_eh2h		

3.1.4 DW_ahb_h2h—Fixed Problems/Enhancements

3.1.4.1 Fixed Problems/Enhancements

The following tables describe the DW_ahb_h2h STARs that were fixed in each of the versions prior to October 2007.

Table 3-28 STAR(s) Fixed in DW_ahb_h2h Version 1.04b

STAR ID	Type	Description
9000170890	Bug	DW_ahb interface needs to be exported in coreAssembler to modify NumSelectSlots.

Table 3-29 STAR(s) Fixed in DW_ahb_h2h Version 1.04a

STAR ID	Type	Description
9000168967	Enhancement	User can select a VIP/VMT version from a pull-down menu in the coreConsultant GUI
9000107668	Enhancement	Register descriptions included in SPIRIT files

Table 3-30 STAR(s) Fixed in DW_ahb_h2h Version 1.03a

STAR ID	Type	Description
There are no customer STARs fixed in this version of DW_ahb_h2h		

Table 3-31 STAR(s) Fixed in DW_ahb_h2h Version 1.02a

STAR ID	Type	Description
9000020968	Bug	"General Product Description" on page 13 of databook says this is a "configurable, vectored interrupt controller". This is a bridge, not an interrupt controller.

Table 3-32 STAR(s) Fixed in DW_ahb_h2h Version 1.01c

STAR ID	Type	Description
There are no customer STARs fixed in this version of DW_ahb_h2h		

Table 3-33 STAR(s) Fixed in DW_ahb_h2h Version 1.00b

STAR ID	Type	Description
167505	Bug	Simulation fails with gtech netlist. Description: When simulating with the gtech netlist produced by coreConsultant with clk set to 10ns, simulation fails with timing violations. Users should use the “zero_delay_mode” switch to get a zero-delay simulation, and not rely on the netlist to set this mode because some users may want to use unit delay mode.
173497	Bug	Ability to change frequency in verification activity causing problems. Description: The ability to change the clock frequency in the simulation activity is meaningless because the simulation does not take timing into account. This option has been removed.

Table 3-34 STAR(s) Resolved in Version 1.00a

STAR ID	Type	Description
152726	Bug	Incorrect signal naming convention. The interrupt outputs (ssi_intr, ssi_txe_intr, ssi_txo_intr, ssi_rxf_intr, ssi_rxo_intr, ssi_rxu_intr, ssi_mst_intr) are of configurable polarity, however, their names do not change to *_n convention to signify their polarity, which is a common approach in all other coreKits. For this release the output interrupt pin(s) are appended with "_n" if the user configures the interrupts with an active low polarity (SSI_INTR_POL=0). For example, when SSI_INTR_POL=1, the output pins appear as ssi_txo_intr, ssi_txe_intr, ssi_rxo_intr, and so on. When SSI_INTR_POL=0, the output pins appear as ssi_txo_intr_n, ssi_txe_intr_n, ssi_rxo_intr_n, and so on. Batch scripts from the previous release of DW_ahb_h2h still works with this release of the product.
152727	Bug	NOTE: Version 1.00a is NOT a drop-in replacement for version 1.0a. The 1.00a version is not pin-for-pin compatible with the 1.0a version. 1. The parameter ADDR_SLICE_LHS, which is used to define the width of the 'paddr' signal in the top-level DW_apb_ssi design is renamed to be SSI_ADDR_SLICE_LHS. 2. The 'scan_mode' top-level input port has been removed. This input port was not used. If you are using the 1.0a version of DW_apb_ssi and now plan to use the newer version, you must do the following: 1. Change any reference to ADDR_SLICE_LHS that may have been in your testbench environment to SSI_ADDR_SLICE_LHS. 2. Any instantiation of the SSI needs to be modified to remove the 'scan_mode' port.

3.1.5 DW_ahb_icm—Fixed Problems/Enhancements

The following tables describe the DW_ahb_icm STARs that were fixed in each of the versions prior to October 2007.

Table 3-35 STAR(s) Fixed in DW_ahb_icm Version 1.10b

STAR ID	Type	Description
9000186924	Bug	The "Use DesignWare foundation synthesis library" option does not work as expected with DesignWare and source license.

Table 3-36 STAR(s) Fixed in DW_ahb_icm Version 1.10a

STAR ID	Type	Description
9000168967	Enhancement	User can select a VIP/VMT version from a pull-down menu in the coreConsultant GUI
9000107668	Enhancement	Register descriptions included in SPIRIT files

Table 3-37 STAR(s) Fixed in DW_ahb_icm Version 1.09a

STAR ID	Type	Description
9000046703	Bug	The following code in the DW_ahb_icm top level RTL file (DW_ahb_icm.v) has been removed because it has not been fully verified. It has changed from: always @(hlayer_data or hresp) begin full_hlayer_data = 'b0; if (hresp != `IDLE) full_hlayer_data[hlayer_data] = 1'b1; end assign num_hlayer_data = full_hlayer_data[`ICM_NUM_LAYERS-1:0]; assign revised_bus_lock = bus_lock | num_hlayer_data; to: assign revised_bus_lock = bus_lock;

Table 3-38 STAR(s) Fixed in DW_ahb_icm Version 1.07a

STAR ID	Type	Description
9000036019	Bug	The DW_ahb_icm is not currently capable of supporting a slave that pulls its slave's hready_resp (hreadyout) low when there is NOT a transfer presented to the slave. The DW_ahb_icm works fine when hready_resp is high when the slave is idle.
9000044105	Bug	Traffic Scenario: Layer A does a write transfer to slave 1, which inserts many delays. Layer A does a write transfer directly to the DW_ahb_icm slave when hready is low. Layer B starts a burst transfer in parallel to the DW_ahb_icm slave. When the transfer from Layer B completes, the hready from Layer A could be low. In such cases when the data phase of the last beat from the Layer B transfer completes, if the slave design requires hready to be high to complete the data phase, then the data written for the last beat from Layer B is the data from Layer A. This behavior is incorrect.

Table 3-39 STAR(s) Fixed in DW_ahb_icm Version 1.06a

STAR ID	Type	Description
There are no customer STARs fixed in this version of DW_ahb_icm.		

Table 3-40 STAR(s) Fixed in DW_ahb_icm Version 1.05a

STAR ID	Type	Description
STS0176236	Enhancement	The number of layers was expanded from 4 to 8.

3.1.6 DW_ahb_ictl—Fixed Problems/Enhancements

The following tables describe the DW_ahb_ictl STARs that were fixed in each of the versions prior to October 2007.

Table 3-41 STAR(s) Fixed in DW_ahb_ictl Version 2.04b

STAR ID	Type	Description
9000186924	Bug	The “Use DesignWare foundation synthesis library” option does not work as expected with DesignWare and source license.

Table 3-42 STAR(s) Fixed in DW_ahb_ictl Version 2.04a

STAR ID	Type	Description
9000168967	Enhancement	User can select a VIP/VMT version from a pull-down menu in the coreConsultant GUI
9000107668	Enhancement	Register descriptions included in SPIRIT files
9000143208	Bug	Register and parameter descriptions changed from irq_pN_offset to irq_pr_N in databook.

Table 3-43 STAR(s) Fixed in DW_ahb_ictl Version 2.03a

STAR ID	Type	Description
There are no customer STARs fixed in this version of DW_ahb_ictl		

Table 3-44 STAR(s) Fixed in DW_ahb_ictl Version 2.02a

STAR ID	Type	Description
There are no customer STARs fixed in this version of DW_ahb_ictl.		

Table 3-45 STAR(s) Fixed in DW_ahb_ictl Version 2.01b

STAR ID	Type	Description
There are no customer STARs fixed in this version of DW_ahb_ictl		

Table 3-46 STAR(s) Fixed in DW_ahb_ictl Versions 2.00a and 2.01a

STAR ID	Type	Description
176630	Bug	Simulation fails if dw_vip_setup isn't run manually. This has been fixed by removing references to unneeded apb files in test_DW_ahb_ictl_shell.v file.
174532	Bug	Default Value of Interrupt Polarity parameters should change to reflect configuration. The default values of the ICT_IRQSRC_POL_*n* parameters depend on the Polarity Type, which if set to "All-active-low," causes the default values of the ICT_IRQSRC_POL_*n* parameters to change to 0. The same holds for the ICT_FIQSRC_POL_*n* parameters.
173497	Bug	Ability to change frequency in verification activity causing problems. Description: the ability to change the clock frequency in the simulation activity is meaningless because the simulation does not take timing into account. This option was removed altogether.
172405	Enhancement	Priority level of interrupts programmable after configuration time.
167505	Bug	Simulation fails with gtech netlist. Description: When simulating with the gtech netlist produced by coreConsultant with clk set to 10ns, simulation fails with timing violations. Users should use the "zero_delay_mode" switch to get a zero-delay simulation, and not rely on the netlist to set this mode because some users may want to use unit delay mode.

Table 3-47 STAR(s) Fixed in DW_ahb_ictl Version 1.00a

STAR ID	Type	Description
152286	Enhancement	Top-level parameter "Individual fiq enables on reset" must be disabled when "Install Fast Interrupt Generation?" is deselected.
155458	Enhancement	Need Revision ID registers in DesignWare IIP components.
157787	Bug	Testability issue on DW_amba_ictl. While doing ATPG coverage analysis on an updated version of the DW_amba_ictl, some gaps in coverage were attributed to a long combinational path in the vmgen module. For the updates of the DW_amba_ictl (DW_ahb_ictl and DW_apb_ictl), this combinational path has been split with four shadow registers that is multiplexed into the data path for scan mode. These shadow registers noticeably improve the ATPG coverage in the vmgen module.
161855	Enhancement	Software Interrupts should be polarity immune. A new configuration parameter has been added, ICT_FORCEREG_ACTIVE_HIGH. When this parameter is set to True, the irq_intforce and fiq_intforce registers become active high. Writing a '1' to the corresponding interrupt source bit forces an interrupt to occur on that source, regardless of the interrupt source's configured polarity.

3.1.7 DW_apb—Fixed Problems/Enhancements

The following tables describe the DW_apb STARs that were fixed in each of the versions prior to October 2007.

Table 3-48 STAR(s) Fixed in DW_apb Version 1.02d

STAR ID	Type	Description
9000182269	Enhancement	Additional information added to databook about clock behavior.

Table 3-49 STAR(s) Fixed in DW_apb Version 1.02c

STAR ID	Type	Description
9000168967	Enhancement	User can select a VIP/VMT version from a pull-down menu in the coreConsultant GUI
9000107668	Enhancement	Register descriptions included in SPIRIT files

Table 3-50 STAR(s) Fixed in DW_apb Version 1.02b

STAR ID	Type	Description
9000047161	Bug	In the 1.02a version of the DesignWare DW_apb Databook, the relationship of PCLK_EN to HCLK described on page 31 contradicts the timing diagram on page 35, which is incorrect. Workaround: To correct the timing diagram in the databook, pclk_en needs to be flipped on the horizontal axis and then moved to the left by one hclk cycle. There should be one cycle where pclk_en is high, which should be in the hclk cycle prior to the rising edge of pclk.

Table 3-51 STAR(s) Fixed in DW_apb Version 1.02a

STAR ID	Type	Description
There are no customer STARs fixed in this version of DW_apb.		

Table 3-52 STAR(s) Fixed in DW_apb Version 1.01e

STAR ID	Type	Description
9000010235	Bug	DW_apb synthesis sets up a setup timing requirement on a multicycle path without setting a corresponding hold time requirement. The necessary hold time requirement was added.

Table 3-53 STAR(s) Fixed in DW_apb Version 1.01d

STAR ID	Type	Description
167505	Bug	Simulation fails with gtech netlist. Description: When simulating with the gtech netlist produced by coreConsultant with clk set to 10ns, simulation fails with timing violations. Users should use the “zero_delay_mode” switch to get a zero-delay simulation, and not rely on the netlist to set this mode because some users may want to use unit delay mode.
173497	Bug	Ability to change frequency in verification activity causing problems. Description: the ability to change the clock frequency in the simulation activity is meaningless because the simulation does not take timing into account. This option was removed altogether.

Table 3-54 STAR(s) Fixed in Version (DW_apb 1.01c)

STAR ID	Type	Description
154678	Bug	Problems with C header files (for all DesignWare IIP components). Valid C constructs are not being used in the header files and are causing compile problems. Some of the components do not have C or Verilog header files. Need to be consistent throughout platform.

Table 3-55 STAR(s) Fixed in Version (DW_apb 1.01b)

STAR ID	Type	Description
152148	Bug	‘runtest’ fails in infinite loop if AMBA VIP 2.0b is installed.
152248	Bug	In general, ‘runtest’ does not work with VMT 2.01a releases.

Table 3-56 STAR(s) Fixed in Version (DW_apb 1.01a)

STAR ID	Type	Description
144230	Bug	MTI-Verilog simulation requires write access to DESIGNWARE_HOME tree, but this is incorrect behavior.
144374	Bug	Error accessing simulator plug-in during Simulate activity of the installed coreKit.
144460	Bug	NC-Verilog simulation failure.

3.1.8 DW_apb_gpio—Fixed Problems/Enhancements

The following tables describe the DW_apb_gpio STARs that were fixed in each of the versions prior to October 2007.

Table 3-57 STAR(s) Fixed in DW_apb_gpio Version 2.06b

STAR ID	Type	Description
9000180681	Bug	DW_apb_gpio header files have extra registers.
9000180683	Enhancement	Derivations of gpio_config_reg1 and gpio_config_reg2 corrected.

Table 3-58 STAR(s) Fixed in DW_apb_gpio Version 2.06a

STAR ID	Type	Description
9000168967	Enhancement	User can select a VIP/VMT version from a pull-down menu in the coreConsultant GUI
9000107668	Enhancement	Register descriptions included in SPIRIT files
9000144097	Bug	Remove invalid addresses (0x78 and 0x7C) from Verilog and C header files
9000144098	Bug	Document configuration parameter GPIO_ADD_ENCODED_PARAMS and registers gpio_config_reg1/gpio_config_reg2
9000144375	Bug	Address values for gpio_config_reg1 and gpio_config_reg2 corrected

Table 3-59 STAR(s) Fixed in DW_apb_gpio Version 2.04a

STAR ID	Type	Description
9000037871	Bug	For DW_apb_gpio (2.02b), the set_false_path is missing from clk to pclk in the synthesis scripts generated by coreConsultant.

Table 3-60 STAR(s) Fixed in DW_apb_gpio Version 2.03a

STAR ID	Type	Description
9000030228	Bug	On synthesizing DW_apb_gpio (2.02b) using FCII, the following error massage: Error: The net '/DW_apb_gpio/gpio_ext_portd_rb0' has more than one driver. (FPGA-CHECK-5) This error goes if presto is turned on. Default presto is turned off for FCII.

Table 3-61 STAR(s) Fixed in DW_apb_gpio Version 2.02b

STAR ID	Type	Description
There are no customer STARs fixed in this version of DW_apb_gpio		

Table 3-62 STAR(s) Fixed in This Release (DW_apb_gpio 2.02a)

STAR ID	Type	Description
167505	Bug	Simulation fails with gtech netlist. Description: When simulating with the gtech netlist produced by coreConsultant with clk set to 10ns, simulation fails with timing violations. Users should use the “zero_delay_mode” switch to get a zero-delay simulation, and not rely on the netlist to set this mode because some users may want to use unit delay mode.
170625	Bug	Wrong path is read back when port is configured as output in S/W mode. Resolution: Now an APB read to the gpio_ext_porta register yields a value equal to a value on the gpio_ext_port*x* port regardless of direction or mode (hardware or software)
170715	Bug	Top-level RTL signal clk_res renamed clk_res_n (in the RTL), to accurately identify its polarity.
173423	Enhancement	Port power on reset values are configurable. Resolution: The data registers for ports A, B, C, and D have been assigned the coreConsultant power-on-reset default values GPIO_SWPORTx_RESET where x = A, B, C or D.
173497	Bug	Ability to change frequency in verification activity causing problems. Description: the ability to change the clock frequency in the simulation activity is meaningless because the simulation does not take timing into account. This option was removed altogether.
173728	Enhancement	Inclusion of metastability made optional for the detection of interrupts. Description: The metastability flip-flops for the Port A interrupt can be removed when the design is configured using GPIO_PA_SYNC_INTERRUPTS parameter.
176892	Enhancement	Control of Hardware/Software operating mode for each bit of each port. The component can now be configured so that each bit of ports A, B, C and D can be individually placed under Hardware or Software control (four new parameters: GPIO_PORT*n*_SINGLE_CTL)

Table 3-63 STAR(s) Fixed in Previous Releases (DW_apb_gpio 2.01a)

STAR ID	Type	Description
172844	Bug	Level-sensitive interrupts are not detected under certain conditions. Description: If port A is configured to support interrupts and has some pins configured as inputs and others as outputs, the input pins that are enabled as level-sensitive interrupts may not work. This problem affects level-sensitive interrupts only; edge-sensitive interrupts work properly. Also, this problem does not affect the generation of the interrupt if all pins on the port are configured as inputs. Workaround: The only way to work around this problem is to place the level-sensitive interrupts in the upper positions of port A. For example, if you have 16 pins on port A with 4 pins configured as level-sensitive interrupts, these interrupts need to be placed on pins[15:12]. This problem affects versions 1.0a, 1.01a, 1.01b, and 2.00a of the DW_apb_gpio.

Table 3-64 STAR(s) Fixed in the Previous Release (DW_apb_gpio 2.00a)

STAR ID	Type	Description
154678	Bug	Problems with C header files (for all DesignWare IIP components). What Happens: Valid C constructs are not being used in the header files and are causing compile problems. Some of the components do not have C or Verilog header files. Need to be consistent throughout platform.
155458	Enhancement	Need Revision ID registers in DesignWare IIP components.

3.1.9 DW_apb_i2c—Fixed Problems/Enhancements

The following tables describe the DW_apb_i2c STARs that were fixed in each of the versions prior to October 2007.

Table 3-65 STAR(s) Fixed in DW_apb_i2c Version 1.08b

STAR ID	Type	Description
There are no customer STARs fixed in this version of DW_apb_i2c		

Table 3-66 STARs Fixed in DW_apb_i2c Version 1.08a

STAR	Type	Description
9000168967	Enhancement	User can select a VIP/VMT version from a pull-down menu in the coreConsultant GUI
9000107668	Enhancement	Register descriptions included in SPIRIT files
9000160810	Bug	Databook error for size of IC_DMA_TDLR register
9000160811	Bug	Databook error for reserved bits in IC_DMA_TDLR register
9000091999	Bug	**Issue:** When using two instances of the DesignWare I^2C 1.06a component in the design with different parameter settings, simulating (using VCS) both components gives the following warning: Warning – [TMR] Text macro redefined Text macro (IC_MAX_SPEED_MODE) redefined. The DW_apb_i2c simulation fails for multi-byte read operations.
9000092958	Bug	**Issue:** The interrupt outputs are driven to a value of 1 out of reset by DW_apb_i2c until clocks to DW_apb_i2c are enabled. Once the clocks to DW_apb_i2c are enabled, the DW_apb_i2c interrupt outputs transition from 1 to 0. There is no reason for these values to be active during reset (and until the clocks start). This has a negative impact on power consumption, as well. This appears to be a by-product of an RTL change that first appeared in the 1.06a version of the component.
9000093545	Bug	**Issue:** There is no CPU indication of slave TX FIFO flush in DW_apb_i2c version 1.06a. Using DW_apb_i2c version 1.06a in an RTL simulation, a remote master performs a slave-transmitter operation on DW_apb_i2c. The slave CPU responds to the read request by writing two bytes to the TX FIFO. The remote master NACKs the first data byte and generates a STOP condition on the bus. As expected, the slave I^2C flushes its TX FIFO as a result of the NACK'd data byte. However, there is no interrupt indication to the CPU that a tx fifo flush occurred.
9000093709	Bug	**Issue:** DW_apb_i2c fails to terminate transfers after the RX FIFO is full. **Workaround for pre-1.08a versions of DW_apb_i2c**: To ensure that this failure does not occur, set the IC_RX_FULL_GEN_NACK parameter to False.
9000093730	Bug	**Issue:** Problem with I^2C NACK generation when RX FIFO is full.
9000093198	Enhancement	**Issue:** When moving from a Fast Speed mode to a High Speed mode of operation, DW_apb_i2c is required to generate a RESTART condition on the I^2C bus. In doing so, there appears to be a one-cycle glitch on the output signal ic_data_oe on the succeeding falling edge of SCL (ic_clk_oe goes to 1).

STAR	Type	Description
9000105354	Bug	**Issue:** I^2C master-transmit and slave-transmit collisions. Beginning with version 1.08a, using the DW_apb_i2c in simultaneous Master / Slave modes is no longer allowed/supported. This automatically means that a write to the TX FIFO (intended as an I^2C Master-Transmit operation) can no longer occur while the DW_apb_i2c requires servicing due to a Read-Request event (Slave-Transmit operation). This prevents the situation, described in this STAR, from happening.
9000108249	Bug	**Issue:** I^2C failed to transmit after a TX abort.

Table 3-67 STARs Fixed in DW_apb_i2c Version 1.06a

STAR	Type	Description
9000062223	Bug	**Issue:** Multiple errors found in 1.05a version of the *DesignWare DW_apb_i2c Databook*, warranting a significant update to the manual.
9000062677	Bug	**Issue:** Multiple errors found in 1.05a version of the *DesignWare DW_apb_i2c Databook*, warranting a significant update to the manual.
9000068233	Enhancement	**Issue:** Request to add a bit to control (enable/disable) ACK for the general call address. **Solution:** This STAR is associated with STAR 9000075092. The RTL fix for the latter is the introduction of a software register that allows either an ACK or NACK when DW_apb_i2c (as an I^2C slave) receives an I^2C general call.
9000075092	Bug	**Issue:** DW_apb_i2c ACKs general calls when master and slave enabled. When slave mode is enabled and the module generates a general call, the module acknowledges the general call address byte and the general call data bytes. This is a violation of the *I2C-Bus Specification* from Philips because transmitters are required to release the SDA line during acknowledge clock pulses. **Solution:** Created the IC_ACK_GENERAL_CALL register, which when written to, forces a response of an ACK or NACK when the I^2C slave is hit with a general call. Also created new configuration parameter, IC_DEFAULT_ACK_GENERAL_CALL, that is used to set the default reset value of the IC_ACK_GENERAL_CALL register. This STAR also fixes issues raised in STAR 9000068233.
9000075243	Bug	**Issue:** When DW_apb_i2c (1.04a) is operating in slave-transmitter mode, low pulses (glitches) are seen on the SCL output. These glitches occur only as a response to ACK SCL falling edges generated by the remote master. The width of the glitches was 93ns. The ic_clk and pclk inputs are being clocked at 32MHz. The glitches occur 187.5ns after falling edges of SCL. **Solution:** Modified RTL resolve this issue.

STAR	Type	Description
9000076182	Bug	**Issue:** The *I2C-Bus Specification* from Philips requires a minimum data set-up time of 250ns for standard mode and 100ns for fast mode. In addition, Note 4 in the Philips specification states that when a device stretches the LOW period of the SCL signal, it must output the next data bit to the SDA line 1250ns before the SCL line is released. **Solution:** The new IC_SDA_SETUP register enforces the timing requirement $t_{[SU;DAT]}$ (see page 32 of *I2C-Bus Specification* 2.1). Also, the new configuration parameter IC_DEFAULT_SDA_SETUP is used to reset the IC_SDA_SETUP register to a default value in hardware.
9000076503	Bug	**Issue:** The ABRT_SLVFLUSH_TXFIFO bit of the IC_TX_ABRT_SOURCE register does not cover all conditions in which a slave TX FIFO is flushed. Therefore, the CPU is not aware of all cases of TX FIFO flushing. **Solution:** Fixed RTL.
9000076630	Bug	**Issue: DW_apb_i2c** fails to reset bus logic on STARTs. The Philips specification version 2.1, on page 28, states the following in Note 4: “I2C-bus compatible devices must reset their bus logic on receipt of a START or repeated START condition such that they all anticipate the sending of a slave address.” DW_apb_i2c 1.05a does not meet this specification requirement. In other words, DW_apb_i2c does not reset its bus logic on receipt of a START or repeated START condition. **Solution:** Fixed RTL.
9000076846	Bug	**Issue:** DW_apb_i2c fails to detect loss of the arbiter. Arbitration is not happening over the acknowledge bit when a master has finished transmitting its last byte. Another master could be generating the acknowledge, which should be flagged as an abort. **Solution:** Fixed RTL.
9000076847	Bug	**Issue:** DW_apb_i2c generates illegal start and stop. Arbitration should happen when SCL is high. Masters starting their START conditions around the same time can both generate the START condition. DW_apb_i2c checks the state of SCL before pulling it low when it completes the hold time for the START condition. DW_apb_i2c should not do this check but bring SCL low, even if it is low, and arbitrate for the bus by extending SCL low. DW_apb_i2c backs off without informing CPU it did. **Solution:** Fixed RTL.
9000076849	Bug	**Issue:** DW_apb_i2c does not restrict you from using reserved SAR addresses for the slave that are specified in the *I2C Bus Specification* from Philips. **Solution:** Included more information in the databook that explains that it is illegal to use these reserved addresses. If you do use these reserved addresses, then you may run into incompatibilities with other I2C components.
9000078774	Enhancement	**Issue:** The description of clearing IC_TX_ABRT_SOURCE register need to be explained better in the databook. **Solution:** Revised description of this register in the databook.

STAR	Type	Description
9000082775	Bug	**Issue:** ACKing continues after ic_enable bit has been set to 0. the behavior of the slave is not consistent when software programs the IC_ENABLE register (offset 0x6C). When there is a slave-receiver operation in progress and the IC_ENABLE is set to 0, DW_apb_i2c continues to ACK all bytes sent by the I^2C master for the entire transfer. After the last byte, DW_apb_i2c then react according to the IC_ENABLE bit being set to 0. This means that the I^2C master, which began the transfer, does NOT know that data transmitted has been discarded. **Solution:** Fixed RTL. Created IC_ENABLE_STATUS register. Bit 0 reflects ic_en; bit 1 is slv_rx_aborted (indicates that a slave-receive operation was aborted by NACKing); and bit 2 is slv_fifo_filled_and_flushed (indicates that at least 1 data byte has been transferred, including that which was NACK'd, but discarded).
9000083225	Bug	**Issue:** When DW_apb_i2c acts as a master, in the reading operation, the falling edge of SCL and rising edge of SDA occur simultaneously. However, the expected behavior is for SDA to go high after one ic_clk clock from the falling edge of SCL. **Solution:** Fixed RTL.
9000083270, 9000084529	Enhancement	**Issue:** Databook enhancements for 1.06a version. Several issues need to be addressed further: ■ Disabling DW_apb_i2c for both 1.05a and 1.06a versions of the component. ■ Explanation of polling instead of interrupts for both slave and master mode operations ■ State what interrupts are involved with individual operation modes and when they are asserted ■ More information about the TX_ABRT bit in the IC_RAW_INTR_STAT register **Solution:** Updated databook.
9000084952	Bug	**Issue:** DW_apb_i2c prematurely releases SCL in the slave TX abort. **Solution:** Fixed RTL. Also updated databook to reflect current behavior of component. when a read-request occurs, and the IC_DATA_CMD is erroneously written in with bit 8 is set to 1, then a TX_ABRT occurs, but ic_clk_oe is held low (instead of high, releasing SCL).
9000085866	Bug	**Issue:** DW_apb_i2c transmits on a non-idle bus. **Solution:** Added note in databook for users not to program the IC_SS_SCL_HCNT register to a value higher than 65525, because DW_apb_i2c uses a 16-bit counter to flag an I^2C bus idle condition when this counter reaches a value of IC_SS_SCL_HCNT + 10.

Table 3-68 STARs Fixed in DW_apb_i2c Version 1.05a

STAR	Type	Description
9000052315	Bug	In Table 2 (License Requirements) of the installation guide at http://www.synopsys.com/products/designware/docs/doc/amba/latest/dw_amba_install.pdf, the information about the source license required for DW_apb_i2c is incorrect. The source license required for I2C is DWC-APB-Advanced-Source and not DWC-APB-Periph-Source.

Table 3-69 STARs Fixed in DW_apb_i2c Version 1.04a

STAR	Type	Description
9000015925	Bug	DW_apb_uart, DW_apb_i2c, DW_apb_ssi and DW_apb_wdt all have a module called DW_apb_biu. If these blocks are created separately using coreConsultant and then integrated into the same higher-level design, the user should provide a unique design prefix to each of these blocks in coreTools. Without this unique prefix, there is a naming clash between sub-blocks of these components. These modules now have unique module names; no prefix is required.

Table 3-70 STARs Fixed in Version 1.03a

STAR	Type	Description
9000012744	Bug	**Issue**: The upper 16 bits of the IC_DATA_CMD register are aliased to the lower 16 bits. This created the following problem: In an 8-bit APB: Accessing any of the three upper bytes in the IC_DATA_CMD register causes a tx_push for a write when it should only be for byte1. Accessing any of the two upper bytes in the IC_DATA_CMD register causes an rx_pop for a read when it should only be for byte0. In a 16-bit APB: Accessing the upper half-word in the IC_DATA_CMD register causes a tx_push for a write when it should only be for the lower half-word. Accessing the upper half-word in the IC_DATA_CMD register causes an rx_pop for a read when it should only be for the lower half-word. **Solution**: The DW_apb_i2c code is modified to prevent aliasing in both 16-bit and 8-bit modes.
STS0185946	Enhancement	**Issue**: IC_INTR_STAT and IC_RAW_INTR_STAT offsets are correct in Table 6 but reversed on pages 61-66. **Solution**: Both descriptions now match and are correct.
STS0182105	Bug	**Issue:** Software Reset can leave I2C slave in control of the I2C bus. **Solution:** Removed Software Reset completely, as its not useful the way it was implemented. Also removed the description from the documentation.

3.1.10 DW_apb_i2s—Fixed Problems/Enhancements

The following tables describe the DW_apb_i2s STARs that were fixed in each of the versions prior to October 2007.

Table 3-71 STAR(s) Fixed in DW_apb_i2s Version 1.02b

STAR ID	Type	Description
There are no customer STARs fixed in this version of DW_apb_i2s		

Table 3-72 STAR(s) Fixed in DW_apb_i2s Version 1.02a

STAR ID	Type	Description
9000168967	Enhancement	User can select a VIP/VMT version from a pull-down menu in the coreConsultant GUI
9000107668	Enhancement	Register descriptions included in SPIRIT files

3.1.11 DW_apb_ictl—Fixed Problems/Enhancements

The following tables describe the DW_apb_ictl STARs that were fixed in each of the versions prior to October 2007.

Table 3-73 STAR(s) Fixed in DW_apb_ictl Version 2.03b

STAR ID	Type	Description
9000186924	Bug	The “Use DesignWare foundation synthesis library” option does not work as expected with DesignWare and source license.

Table 3-74 STAR(s) Fixed in DW_apb_ictl Version 2.03a

STAR ID	Type	Description
9000168967	Enhancement	User can select a VIP/VMT version from a pull-down menu in the coreConsultant GUI
9000107668	Enhancement	Register descriptions included in SPIRIT files
9000143208	Bug	Register and parameter descriptions changed from irq_pN_offset to irq_pr_N in databook.

Table 3-75 STAR(s) Fixed in DW_apb_ictl Version 2.02a

STAR ID	Type	Description
There are no customer STARs fixed in this version of DW_apb_ictl		

Table 3-76 STAR(s) Fixed in DW_apb_ictl Version 2.01a

STAR ID	Type	Description
9000029087	Bug	In DW_apb_ictl (2.00b), the generated c_header file DW_apb_ictl_defs.h has the following items reversed. IRQ_P4_OFFSET is 0x0fc should be 0x0f8 IRQ_P5_OFFSET is 0x0f8 should be 0x0fc This is also the case for verilog_headers file.

Table 3-77 STAR(s) Fixed in DW_apb_ictl Version 2.00b

STAR ID	Type	Description
There are no customer STARs fixed in this version of DW_apb_ictl		

Table 3-78 STAR(s) Fixed in DW_apb_ictl Version 2.00a

STAR ID	Type	Description
174532	Bug	Default value of Interrupt Polarity parameters should change to reflect configuration. Resolution: The default values of the ICT_IRQSRC_POL_*n* parameters now depend on the Polarity Type, which if set to “All-active-low,” causes the default values of the ICT_IRQSRC_POL_*n* parameters to change to 0. The same holds for the ICT_FIQSRC_POL_*n* parameters.
173497	Bug	Ability to change frequency in verification activity causing problems. Description: the ability to change the clock frequency in the simulation activity is meaningless because the simulation does not take timing into account. This option was removed altogether.
172406	Enhancement	Priority level of interrupts programmable after configuration time.
167505	Bug	Simulation fails with gtech netlist. Description: When simulating with the gtech netlist produced by coreConsultant with clk set to 10ns, simulation fails with timing violations. Users should use the “zero_delay_mode” switch to get a zero-delay simulation, and not rely on the netlist to set this mode because some users may want to use unit delay mode.

Table 3-79 STAR(s) Fixed in DW_apb_ictl Version 1.00a

STAR ID	Type	Description
152286	Enhancement	Top-level parameter "Individual fiq enables on reset" must be disabled when "Install Fast Interrupt Generation?" is deselected.
155458	Enhancement	Need Version ID registers in DesignWare IIP components.

STAR ID	Type	Description
157787	Bug	Testability issue on DW_amba_ictl. While doing ATPG coverage analysis on an updated version of the DW_amba_ictl, some gaps in coverage were attributed to a long combinational path in the vmgen module. For the updates of the amba_ictl (DW_ahb_ictl and DW_apb_ictl), this combinational path has been split with four shadow registers that is multiplexed into the data path for scan mode. These shadow registers noticeably improve the ATPG coverage in the vmgen module.
161855	Enhancement	Software Interrupts should be polarity immune. A new configuration parameter has been added, ICT_FORCEREG_ACTIVE_HIGH. When this parameter is set to True, the irq_intforce and fiq_intforce registers become active high. Writing a '1' to the corresponding interrupt source bit forces an interrupt to occur on that source, regardless of the interrupt source's configured polarity.

3.1.12 DW_apb_rap—Fixed Problems/Enhancements

The following tables describe the DW_apb_rap STARs that were fixed in each of the versions prior to October 2007.

Table 3-80 STAR(s) Fixed in DW_apb_rap Version 2.02d

STAR ID	Type	Description
There are no customer STARs fixed in this version of DW_apb_rap		

Table 3-81 STAR(s) Fixed in DW_apb_rap Version 2.02c

STAR ID	Type	Description
9000107668	Enhancement	Register descriptions included in SPIRIT files

Table 3-82 STAR(s) Fixed in DW_apb_rap Version 2.02b

STAR ID	Type	Description
There are no customer STARs fixed in this version of DW_apb_rap		

Table 3-83 STAR(s) Fixed in DW_apb_rap Version 2.02a

STAR ID	Type	Description
There are no customer STARs fixed in this version of DW_apb_rap.		

Table 3-84 STAR(s) Fixed in DW_apb_rap Version 2.01a

STAR ID	Type	Description
There are no customer STARs fixed in this version of DW_apb_rap.		

Table 3-85 STAR(s) Fixed in Version DW_apb_rap 2.00b

STAR ID	Type	Description
167505	Bug	Simulation fails with gtech netlist. Description: When simulating with the gtech netlist produced by coreConsultant with clk set to 10ns, simulation fails with timing violations. Users should use the “zero_delay_mode” switch to get a zero-delay simulation, and not rely on the netlist to set this mode because some users may want to use unit delay mode.
173497	Bug	Ability to change frequency in verification activity causing problems. Description: the ability to change the clock frequency in the simulation activity is meaningless because the simulation does not take timing into account. This option was removed altogether.

Table 3-86 STAR(s) Fixed in Version DW_apb_rap 2.00a

STAR ID	Type	Description
155458	Enhancement	Need Revision ID registers in DesignWare IIP components.

Table 3-87 STAR(s) Fixed in 2002.08-SP1-1 Release (DW_apb_rap 1.02c)

STAR ID	Type	Description
154045	bug	Polarity of interrupts is incorrectly prompted in the DW_apb_rap coreKit. The setting for the configuration parameter “Active Low Interrupts” is misleading. When this option is checked, active high interrupts are generated instead of active low interrupts. **Workaround:** If you are using DW_apb_rap version 1.0a, 1.01a, or 1.01b, to get Active Low interrupts, leave this box unchecked; if you want Active High interrupts check this box.
154678	bug	Problems encountered with C header files. 1. There needs to be design name prefixes in front of all of the C definitions. This helps for multiple instantiations. 2. Header files should compile once the <base address> is set.

3.1.13 DW_apb_rtc—Fixed Problems/Enhancements

The following tables describe the DW_apb_rtc STARs that were fixed in each of the versions prior to October 2007.

Table 3-88 STAR(s) Fixed in DW_apb_rtc Version 2.01d

STAR ID	Type	Description
There are no customer STARs fixed in this version of DW_apb_rtc		

Table 3-89 STAR(s) Fixed in DW_apb_rtc Version 2.01c

STAR ID	Type	Description
9000107668	Enhancement	Register descriptions included in SPIRIT files

Table 3-90 STAR(s) Fixed in DW_apb_rtc Version 2.01b

STAR ID	Type	Description
There are no customer STARs fixed in this version of DW_apb_rtc		

Table 3-91 STAR(s) Fixed in DW_apb_rtc Version 2.01a

STAR ID	Type	Description
9000044303	Bug	Synthesis of the DW_apb_rtc component may fail in certain circumstances. To see these failures, you must be in coreConsultant using the non-default Design Compiler shell mode DCSH/EQN. The default synthesis in coreConsultant uses the Design Compiler TCL-mode, which synthesizes correctly.

Table 3-92 STAR(s) Fixed in DW_apb_rtc Version 2.00c

STAR ID	Type	Description
There are no customer STARs fixed in this version of DW_apb_rtc.		

Table 3-93 STAR(s) Fixed in Version DW_apb_rtc 2.00b

STAR ID	Type	Description
167505	Bug	Simulation fails with gtech netlist. Description: When simulating with the gtech netlist produced by coreConsultant with clk set to 10ns, simulation fails with timing violations. Users should use the “zero_delay_mode” switch to get a zero-delay simulation, and not rely on the netlist to set this mode because some users may want to use unit delay mode.
173497	Bug	Ability to change frequency in verification activity causing problems. Description: the ability to change the clock frequency in the simulation activity is meaningless because the simulation does not take timing into account. This option was removed altogether.

Table 3-94 STAR(s) Fixed in 2003.02 Release (DW_apb_rtc 2.00a)

STAR ID	Type	Description
149735	Enhancement	A mode should be added that wraps on RTC_CMR instead of maximum count.
154678	Bug	Problems with C header files (for all DesignWare IIP components). Valid C constructs are not being used in the header files and are causing compile problems. Some of the components do not have C or Verilog header files. Need to be consistent throughout platform.
155458	Enhancement	New Version ID registers in DesignWare IIP components.

Table 3-95 STAR(s) Fixed in 2002.08-SP1-1 Release (DW_apb_rtc 1.01c)

STAR ID	Type	Description
155706	Bug	If the external enable mode is selected (RTC_EN_MODE = 1), the rtc_en output must follow what is written to the counter control register (RTC_CCR) rtc_en bit. Currently, the rtc_en output follows the rtc_mask bit of the RTC_CCR register. **Workaround:** If you have decided to use the external enable mode with RTC_EN_MODE = 1, modify the following line in DW_apb_rtc.v: assign rtc_en = rtc_cr[1] to assign rtc_en = rtc_cr[2] This mode has rtc_en as an output and would be used to gate the RTC clock as the block is disabled. If you are not using this mode, then there is no issue and no change is required because this line is removed.

3.1.14 DW_apb_ssi—Fixed Problems/Enhancements

The following tables describe the DW_apb_ssi STARs that were fixed in each of the versions prior to October 2007.

Table 3-96 STAR(s) Fixed in DW_apb_ssi Version 3.11b

STAR ID	Type	Description
There are no customer STARs fixed in this version of DW_apb_ssi		

Table 3-97 STAR(s) Fixed in DW_apb_ssi Version 3.11a

STAR ID	Type	Description
9000107668	Enhancement	Register descriptions included in SPIRIT files
9000145088	Bug	Databook clarified for EEPROM read mode

Table 3-98 STAR(s) Fixed in DW_apb_ssi Version 3.10a

STAR ID	Type	Description
9000075679	Bug	In the *DesignWare DW_apb_ssi Databook*, for Microwire transfers with MHS (bit 2), MDD (bit 1), and MWMOD (bit 0) in the Microwire Control Register (MWCR) set to low, the waveforms in databook show ssi_oe_n low until the rising edge during the turn-around clock cycle. However, in the RTL simulations, ssi_oe_n is high on the rising edge of the LSB of the control word, one cycle before the turnaround. **Resolution:** Changed the component to match the documented behavior.

Table 3-99 TBD

STAR ID	Type	Description
There are no customer STARs fixed in this version of DW_apb_ssi		

Table 3-100 STAR(s) Fixed in DW_apb_ssi Version 3.03a

STAR ID	Type	Description
9000015925	Bug	DW_apb_uart, DW_apb_i2c, DW_apb_ssi and DW_apb_wdt all have a module called DW_apb_biu. If these blocks are created separately using coreConsultant and then integrated into the same higher-level design, the user should provide a unique design prefix to each of these blocks in coreTools. Without this unique prefix, there is a naming clash between subblocks of these components. These modules now have unique module names; a prefix is not needed.

STAR ID	Type	Description
STS0168091	Enhancement	Description: When the DW_apb_ssi MASTER configuration is interfacing with an SPI EEPROM slave device for a read access, there is currently a requirement to service the TX FIFO on the MASTER. For read operations, it is necessary to write the same amount of dummy data frames into the TX FIFO as you expect to receive from the EEPROM. This is because the transfer is stopped in “transmit and receive” mode when the TX FIFO is empty. This enhancement has been filed to resolve this issue and reduce the overhead of servicing the TX FIFO during read operations when accessing SPI EEPROMs.

Table 3-101 STAR(s) Fixed in DW_apb_ssi Version 3.02a

STAR ID	Type	Description
STS0168091	Enhancement	Description: When the DW_apb_ssi MASTER configuration interfaces with an SPI EEPROM slave device for a read access, there is a requirement to service the TX FIFO. If the user wants to read 4 frames from the EEPROM, the TX FIFO must contain the opcode, followed by the address, followed by four dummy data frames. For an application note on exactly how to service the TX FIFO, refer to the appendix of the DW_apb_ssi databook (version 3.00a and newer).

Table 3-102 STAR(s) Fixed in DW_apb_ssi Version 3.01a

STAR ID	Type	Description
179686	Bug	**Description**: See Bug 178625 in Table 3-99. The original fix for this STAR reduced the “error window” for the Transmit (TX) FIFO write, however, subsequent regression tests have shown that a TX-FIFO write into an empty TX FIFO near the end of a data frame transmission can still cause the garbage data frame to be transmitted. **Workaround**: Same workaround used for Bug 178625 (Table 3-99).

Table 3-103 STAR(s) Fixed in DW_apb_ssi Version 3.00a

STAR ID	Type	Description
178625	Bug	**Description**: If one writes to the Transmit (TX) FIFO (and the TX FIFO is empty) between the transmission of the last bit of the data frame and one sclk_out cycle later, an additional (garbage) data frame is sent by the DW_apb_ssi master. The (correct) data written into the TX FIFO is then transmitted after the garbage frame has been transmitted. This bug is only present in the DW_apb_ssi MASTER configuration when the serial protocol is SPI with SCPH=0 and SCPOL=0. **New behavior for version 3.00a:** The DW_apb_ssi starts a new serial transfer rather than attempting a continuous back-to-back transfer as described above. The garbage data is no longer transmitted. **Workaround for earlier versions (prior to 3.00a)**: Never let TX FIFO go emtpy (go below 1). Set the TXFTLR register high enough that the system ensures that the Tx-FIFO does not empty during continuous transfers. - Write the Tx-FIFO with enough data frames that the number of entries is above the TXFTLR register value. - Enable the slave select output (SER). Transfer begins at this point. - Use the ssi_txe_intr to ensure that the TX FIFO does not empty until all data frames have been given to the DW_apb_ssi.
173497	Bug	Ability to change frequency in verification activity causing problems. **Description**: The ability to change the clock frequency in the simulation activity is meaningless because the simulation does not take timing into account. This option was removed altogether.
168832	Enhancement	Bit fields in the Status Register (SR) relating to the empty/full status of the TX FIFO and the RX FIFO required 2 pclk cycles to be updated. This caused problems when a read of the FIFO status bits occurred one pclk cycle after a FIFO access (push/pop). The returned status is incorrect because the status bits are not updated until the next pclk cycle. **New behavior**: The registering of these bit fields in the Status Register has been removed to allow the correct FIFO status to be returned under all conditions.
168784	Bug	The default value (reset value) of the chip select, rather than being always low, is controlled by the default frame format. When the default frame format is Motorola SPI or Microwire, the default value is high; otherwise it is low. This can be problematic for EEPROMs and could have caused power-up erasures.
167505	Bug	Simulation fails with gtech netlist. **Description**: When simulating with the gtech netlist produced by coreConsultant with clk set to 10ns, simulation fails with timing violations. Users should use the “zero_delay_mode” switch to get a zero-delay simulation, and not rely on the netlist to set this mode because some users may want to use unit delay mode.

Table 3-104 STAR(s) Fixed in 2003.03 Release (DW_apb_ssi 2.00a)

STAR ID	Type	Description
155458	Enhancement	Need Revision ID registers in DesignWare IIP components.
155568	Enhancement	Need to be able to transmit only a control word.
155570	Enhancement	Need busy/ready handshaking signal for Microwire protocol.
153699	Bug	FC2 Synthesis fails when Presto is not enabled for number of slaves equal to 1. What Happens: This is a result of a coding style/coreBuilder database issue that a non-presto/FC2 combination cannot understand. Workaround: Enable Presto (which is the default) or upgrade to 2003.02 release of the component.
153906	Bug	If the Transmit FIFO Threshold Level register is set to FIFO_DEPTH – 1, the interrupt always is active. **What Happens**: The Threshold level for the TX FIFO controls the number of FIFO entries needed to generate the FIFO empty interrupt (ssi_txe_intr/_n). For example, if the threshold is set to 4, the empty interrupt is active when there are four or less than four entries in the TX FIFO. The TX FIFO threshold is set by writing to the TXFTLR register. If you set a value of SSI_TX_FIFO_DEPTH-1 into this register, the ssi_txe_intr/_n interrupt always is active, even if the FIFO is full. **Workaround**: You should never set the TXFTLR register with a value of one less than the FIFO depth. (It is not possible to write a value of the FIFO depth into this register). The maximum value you should write into this register is SSI_TX_FIFO_DEPTH–2.
154678	Bug	Problems with C header files (for all DesignWare IIP components). **What Happens**: Valid C constructs are not being used in the header files and are causing compile problems. Some of the components do not have C or Verilog header files. Need to be consistent throughout platform.
161862	Bug	DW_apb_ssi Master configuration generates extra clock pulse on sclk_out for the ss_n (SSP frame indicator output). The serial output clock (sclk_out) from the DW_apb_ssi Master should not begin to toggle until the ss_n signal has been de-asserted (logic 0). This extra pulse on the sclk_out from the master at the beginning of an SSP frame should not affect communication with the user's SSP slave peripheral because the slave is waiting for an active frame indicator (ss_n) from the master before using the sclk_out signal.

Table 3-105 STAR(s) Fixed in 2002.08-SP1 (DW_apb_ssi 1.01b)

STAR ID	Type	Description
150683	Bug	Simulations failed with Verilog-XL and when the configuration parameter SSI_NUM_SLAVES was set to '1'. The simulator reported an error when attempting to make a Vera to HDL connection on the ss_n signal. However, the simulation still ran successfully even though the log file reported an error.

STAR ID	Type	Description
152075	Bug	Problems with the Microwire protocol. The previous release of the DW_apb_ssi (version 1.0a) encountered the following known issues with the Microwire protocol: ■ If the Microwire control word is less than 4-bits wide the wrong control word is sent by the DW_apb_ssi master. ■ If the Microwire control or data word is 16-bits wide the incorrect data is sent/received by the DW_apb_ssi master. ■ Loopback support for the Microwire protocol is not operating correctly in the DW_apb_ssi master. ■ When the baud rate is set to 2, a failure occurs due to a bug in the internal state machine.
152726	Bug	Incorrect signal naming convention. The interrupt outputs (ssi_intr, ssi_txe_intr, ssi_txo_intr, ssi_rxf_intr, ssi_rxo_intr, ssi_rxu_intr, ssi_mst_intr) are of configurable polarity, however, their names do not change to *_n convention to signify their polarity, which is a common approach in all other DesignWare IIP components. For this release the output interrupt pin(s) are appended with “_n” if the user configures the interrupts with an active low polarity (SSI_INTR_POL=0). For example, when SSI_INTR_POL=1, the output pins appear as ssi_txo_intr, ssi_txe_intr, ssi_rxo_intr, and so on. When SSI_INTR_POL=0, the output pins appear as ssi_txo_intr_n, ssi_txe_intr_n, ssi_rxo_intr_n, and so on. Batch scripts from the previous release of DW_apb_ssi still works with this release of the product.
152727	Bug	Version 1.01b is NOT a drop-in replacement for version 1.0a. Version 1.01b is not pin-for-pin compatible with version 1.0a. 1. The parameter ADDR_SLICE_LHS, which is used to define the width of the 'paddr' signal in the top-level DW_apb_ssi design is renamed to be SSI_ADDR_SLICE_LHS. 2. The scan_mode top-level input port has been removed. This input port was not used. If you are using the 1.0a version of DW_apb_ssi and now plan to use the newer 1.01b version, you must do the following: 1. Change any reference to ADDR_SLICE_LHS that may have been in your testbench environment to SSI_ADDR_SLICE_LHS. 2. Modify any instantiation of the SSI to remove the scan_mode port.

3.1.15 DW_apb_timers—Fixed Problems/Enhancements

The following tables describe the DW_apb_timers STARs that were fixed in each of the versions prior to October 2007.

Table 3-106 tbd

STAR ID	Type	Description
There are no customer STARs fixed in this version of DW_apb_timers		

Table 3-107 STAR(s) Fixed in DW_apb_timers Version 2.02c

STAR ID	Type	Description
9000168967	Enhancement	User can select a VIP/VMT version from a pull-down menu in the coreConsultant GUI
9000107668	Enhancement	Register descriptions included in SPIRIT files
9000151929	Bug	TIMER_WIDTH_1 and TIMER_WIDTH_*n* corrected in databook
9000167104	Bug	Address Offsets incorrect in databook

Table 3-108 STAR(s) Fixed in Version DW_apb_timers 2.02b

STAR ID	Type	Description
There are no customer STARs fixed in this version of DW_apb_timers		

Table 3-109 STAR(s) Fixed in Version DW_apb_timers 2.02a

STAR ID	Type	Description
9000028226	Bug	In $DESIGNWARE_HOME/examples/QuickStart_SingleLayer/latest/sim/stimulus/DW_apb_timers/*, there are 2 files called test_timers.c and test_timers.v in which TimerNControlReg description is wrong. In test_timers.c file, in lines 194, 211 and 225, it should be: Timer1ControlReg[0] -> Setting to Disabled -> (1'b0) instead of Timer1ControlReg[1] -> Setting to Disabled -> (1'b0) In test_timers.v file, the description is wrong in lines 192, 209 and 223. This problem also exists in the QuickStart_MultiLayer example tree.

Table 3-110 STAR(s) Fixed in Version DW_apb_timers 2.01a

STAR ID	Type	Description
9000017080	Bug	In the databook (2.01a version), normal operation of the timer in 'Enabling/Disabling aTimer' and 'Setting a timer in Operating Mode' is not explained clearly. This and other various databook corrections were made.

Table 3-111 STAR(s) Fixed in Version DW_apb_timers 2.00b

STAR ID	Type	Description
167505	Bug	Simulation fails with gtech netlist. Description: When simulating with the gtech netlist produced by coreConsultant with clk set to 10ns, simulation fails with timing violations. Users should use the “zero_delay_mode” switch to get a zero-delay simulation, and not rely on the netlist to set this mode because some users may want to use unit delay mode.
173497	Bug	Ability to change frequency in verification activity causing problems. Description: the ability to change the clock frequency in the simulation activity is meaningless because the simulation does not take timing into account. This option was removed altogether.

Table 3-112 STAR(s) Fixed in Version DW_apb_timers 2.00a

STAR ID	Type	Description
155458	Enhancement	Need Revision ID registers in DesignWare IIP components.

Table 3-113 STAR(s) Fixed in DW_apb_timers 1.02c

STAR ID	Type	Description
154492	bug	Interrupts are cleared one APB cycle later than expected. This design error concerns the operation of the Timers End of Interrupt Registers. These registers automatically clear their interrupts when they are read. This is done so that the interrupt is cleared before control is given back to the CPU/master. Unfortunately, this interrupt is cleared one clock (pclk) later than expected. So, the reason for having the interrupts cleared by a read is compromised by not performing it in the first APB clock cycle. The CPU/master thinks it has cleared the interrupt when in fact it is not cleared until another pclk cycle has passed. **Workaround:** If you are using the DesignWare DW_apb_timers (version 1.0a, 1.01a, or 1.01b), perform a dummy APB read after the interrupt clear is read if you want to make sure that the interrupt is cleared before any other instructions are exercised.
154678	bug	Problems encountered with C header files. 1. There needs to be design name prefixes in front of all of the C definitions. This helps for multiple instantiations. 2. Header files should compile once the <base address> is set.

STAR ID	Type	Description
154916	bug	TimersIntStatus and TimersEOI Register addresses are incorrect in databook. **Workaround:** Table 6 in the databook describes the memory map for the system level registers. This table incorrectly lists the TimersEOI register at location (Base+0xa0) and the TimersIntStatus at location (Base+0xa4). The TimersEOI resister is located at (Base+0xa4) and the TimersIntStatus at location (Base+0xa0). If you are using previous versions of the DesignWare DW_apb_timers (1.0a, 1.01a, or 1.01b), please make note of the correct address locations for these registers.

3.1.16 DW_apb_uart—Fixed Problems/Enhancements

The following tables describe the DW_apb_uart STARs that were fixed in each of the versions prior to October 2007.

Table 3-114 STAR(s) Fixed in DW_apb_uart Version 3.06b

STAR ID	Type	Description
There are no customer STARs fixed in this version of DW_apb_uart		

Table 3-115 STAR(s) Fixed in DW_apb_uart Version 3.06a

STAR ID	Type	Description
9000168967	Enhancement	User can select a VIP/VMT version from a pull-down menu in the coreConsultant GUI
9000107668	Enhancement	Register descriptions included in SPIRIT files
9000111674	Bug	FCR[1] not working properly
9000091011	Bug	Release notes has the wrong value for the UCV register
9000149997	Enhancement	Configuration of DLL and DLH registers in low power
9000155694	Bug	Reception problems in LP IrDA mode

Table 3-116 STARs Fixed in DW_apb_uart 3.05a

STAR #	Type	Description
9000120470	Bug	The busy interrupt implementation (IIR[3:0]=0x07) in DW_apb_uart makes it incompatible with the National 16550 specification and fails to work with standard Linux drivers.

Table 3-117 STARs Fixed in DW_apb_uart 3.04a

STAR #	Type	Description
9000090005	Bug	In IrDA mode, DW_apb_uart supports a nominal (3/16) pulse duration but not a minimal pulse duration. For a 115.2 Kbaud data rate, the 3/16 pulse duration is 1.63usec and for 9600 Kbaud rate, the duration is 19.53usec. However, DW_apb_uart does not support a minimal pulse duration of 1.41usec.

Table 3-118 STARs Fixed in DW_apb_uart 3.03a

STAR #	Type	Description
9000073306	Bug	An incompatibility exists between DW_apb_uart and standard 16550 drivers. The scenario involves the generation of the transmit holding register empty (THRE) interrupt (bits 3:0 = 0010 of the Interrupt Identity Register (IIR)) and how the interrupt is cleared and re-enabled. When bit 1 of the Interrupt Enable Register (IER) is set and there are no characters to transmit, an interrupt is generated. When the IIR is read to check the source of the interrupt, the interrupt is reset as per the specification. DW_apb_uart can only generate a new THRE interrupt once a character is written to the Transmit Holding Register (THR) and is then sent out. The expected behavior of the 16550 driver is that once the THRE interrupt is cleared, it can be generated again simply by disabling IER[1] and then re-enabling IER[1] without having to write a character to THR. **Resolution:** DW_apb_uart has been modified to allow the THRE to be regenerated again by disabling/re-enabling IER[1]. The following describes the corrected behavior: 1) An interrupt is generated due to a THRE. 2) The IIR[3:0] is read, which indicates a THRE interrupt has occurred (0010). 3) The interrupt is masked even if the THR/TX FIFO is still empty or below the threshold until the THRE interrupt enable (IER[1]) is set to 0. 4) If the THRE interrupt enable bit (IER[1]) is set to 1 (high), then the interrupt is seen again (if it is the highest priority interrupt pending).
9000071348	Bug	DW_apb_uart uses the word “break” for some of its wires, which is a reserved word in System Verilog.

Table 3-119 STARs Fixed in DW_apb_uart 3.02a

STAR #	Type	Description
9000061700	Bug	The *DesignWare DW_apb_uart Databook* incorrectly states that the default/reset value for the IIR register is 0xCF in the memory map table in Chapter 6. In the detailed description, the reset value for different bit widths is listed as 0x1, which is also incorrect. The correct reset value for the IIR register is 0x01.

Table 3-120 STARs Fixed in DW_apb_uart 3.01a

STAR #	Type	Description
9000015925	Bug	DW_apb_uart, DW_apb_i2c, DW_apb_ssi and DW_apb_wdt all have a module called DW_apb_biu. If these blocks are created separately using coreConsultant and then integrated into the same higher-level design, the user should provide a unique design prefix to each of these blocks in coreTools. Without this unique prefix, there is a naming clash between subblocks of these components. These modules now have unique module names.
9000040119	Bug	When the DW_apb_uart (version 3.00a) operates in IrDA 1.0 SIR mode it samples each data pulse at the beginning of the pulse. Since the width of a pulse in SIR mode is only 3/16th of a normal serial bit time, it makes the reception logic sensitive to errors induced by jitter. The DW_apb_uart version 3.01a is able to accurately receive characters with more jitter since the data pulse is sampled in the middle instead of the beginning of the pulse.
9000044123	Bug	Synthesis of the DW_apb_uart component may fail in certain circumstances. To see these failures, you must be in coreConsultant using the non-default Design Compiler shell mode DCSH/EQN. The default synthesis in coreConsultant uses the Design Compiler TCL-mode, which synthesizes correctly.

Table 3-121 STARs Fixed in DW_apb_uart 3.00a

STAR #	Type	Description
9000008273	Bug	Due to a synchronization problem, the CTO interrupt may not always be cleared by a read of the Rx Buffer Register. This problem only occurs in the DW_apb_uart version 2.00e and earlier with a 2 clock configuration. A software workaround to this problem is to read the Rx Buffer Register as many times as needed to clear the interrupt. The maximum number of reads necessary must never be more than the depth of the Rx FIFO. Version 3.00a of the DW_apb_uart fixes the problem.
STS0174631	Enhancement	The DW_apb_uart does not support Power Compiler clock gate insertion using the `-gate_clock` option. Workaround: There is no workaround for this problem.
STS0179449	Bug	Extra scan cells inserted when no scan is chosen
STS0181566	Bug	Using 2003.12 DC produces a bad gtech netlist. In order to simulate the DW_apb_uart, you must create a gtech simulation model. For correct creation of this model, you must use the DesignWare Building Block IP release DWF_0307 (not DWF_0312). Using Design Compiler version 2003.12 with the corresponding DWF_0312 release creates an incorrect gtech simulation model. Workaround: Do not use Design Compiler 2003.12 to synthesize the DW_apb_uart. Use an earlier version with the appropriate DWF_0307 overlay.

Table 3-122 STARs Fixed in DW_apb_uart 2.00e

STAR #	Type	Description
165764	Enhancement	Add Verilog and C header files.
167505	Bug	Simulation fails with gtech netlist. Description: When simulating with the gtech netlist produced by coreConsultant with clk set to 10ns, simulation fails with timing violations. Users should use the “zero_delay_mode” switch to get a zero-delay simulation, and not rely on the netlist to set this mode because some users may want to use unit delay mode.
173497	Bug	Ability to change frequency in verification activity causing problems. Description: the ability to change the clock frequency in the simulation activity is meaningless because the simulation does not take timing into account. This option was removed altogether.

Table 3-123 STARs Fixed in Release 2003.02 (DW_apb_uart 2.00d)

STAR #	Type	Description
172578	Bug	The two serial inputs cts_n and dsr_n of the DW_16550 UART are not synchronized. Due to this, there may be timing violations on the serial interface of the UART. All other serial inputs are synchronized.

Table 3-124 STARs Fixed in DWF_0212 and 2003.02 (DW_apb_uart 2.00d)

STAR #	Type	Description
148414	Bug	The transmitter portion of the DW_16550 appears to transition from the last data bit (the most significant bit) to the parity bit one system clock cycle earlier than it should. This results in the MSb of data being slightly short. In most cases, this should not pose any problem because there is usually a generous amount of margin for data rate differences. However, in the presence of interesting differences in data rates when operating with small baud rate divisors (especially with a divisor of 1) the problem could become critical.

3.1.17 DW_apb_wdt—Fixed Problems/Enhancements

The following tables describe the DW_apb_wdt STARs that were fixed in each of the versions prior to October 2007.

Table 3-125 STAR(s) Fixed in DW_apb_wdt Version 1.03d

STAR ID	Type	Description
There are no customer STARs fixed in this version of DW_apb_wdt		

Table 3-126 STAR(s) Fixed in DW_apb_wdt Version 1.03c

STAR ID	Type	Description
9000168967	Enhancement	User can select a VIP/VMT version from a pull-down menu in the coreConsultant GUI
9000107668	Enhancement	Register descriptions included in SPIRIT files

Table 3-127 STAR(s) Fixed in DW_apb_wdt Version 1.03b

STAR ID	Type	Description
There are no customer STARs fixed in this version of DW_apb_wdt.		

Table 3-128 STAR(s) Fixed in DW_apb_wdt Version 1.03a

STAR ID	Type	Description
9000015925	Bug	DW_apb_uart, DW_apb_i2c, DW_apb_ssi and DW_apb_wdt all have a module called DW_apb_biu. If these blocks are created separately using coreConsultant and then integrated into the same higher-level design, the user should provide a unique design prefix to each of these blocks in coreTools. Without this unique prefix, there is a naming clash between subblocks of these components. These modules now have unique module names.
9000044304	Bug	Synthesis of the DW_apb_wdt component may fail in certain circumstances. To see these failures, you must be in coreConsultant using the non-default Design Compiler shell mode DCSH/EQN. The default synthesis in coreConsultant uses the Design Compiler TCL-mode, which synthesizes correctly.

Table 3-129 STAR(s) Fixed in DW_apb_wdt Version 1.02a

STAR ID	Type	Description
STS0177910	Enhancement	Added a 1-bit register called WDT_PING_1BIT_WR that always is W/R and always exists.

Table 3-130 STAR(s) Fixed in DW_apb_wdt Version 1.01a

STAR ID	Type	Description
167505 (167517)	Bug	Simulation fails with gtech netlist. Description: When simulating with the gtech netlist produced by coreConsultant with clk set to 10ns, simulation fails with timing violations. Users should use the “zero_delay_mode” switch to get a zero-delay simulation, and not rely on the netlist to set this mod because some users may want to use unit delay mode.
173497 (168039)	Bug	Ability to change frequency in verification activity causing problems. Description: the ability to change the clock frequency in the simulation activity is meaningless because the simulation does not take timing into account. This option was removed altogether.
176596	Enhancement	Identification Registers added to this component. NOTE: The redundant WDT_VID register was removed from the memory map. Use the WDT_COMP_VERSION register for this function.

Table 3-131 STAR(s) Fixed in DW_apb_wdt Version 1.00a

STAR ID	Type	Description
Because this is the first release of DW_apb_wdt, there were no bugs filed against this version of the product.		

4 Pre-October 2007 AMBA 3 AXI STARs

This appendix contains archived STAR tables for AMBA 3 AXI.

4.1 AMBA 3 STAR Archives

The following subsections contain archived STAR tables for the individual AMBA 3 AXI components.

4.1.1 DW_axi—Fixed Problems/Enhancements

There were no STAR tables contained in the previous DW_axi release notes.

4.1.2 DW_axi_gm—Fixed Problems/Enhancements

The following tables describe the DW_axi_gm STARs that were fixed in each of the versions prior to October 2007.

Table 4-1 STAR(s) Fixed in DW_axi_gm Version 1.01b

STAR ID	Type	Description
There are no customer STARs fixed in this version of DW_axi_gm.		

Table 4-2 STARs Fixed in DW_axi_gm Version 1.01a

STAR	Type	Description
9000139658	Bug	Rewrote information on monitors in DW_axi_gm databook saying that a GIF monitor logs transactions only on the bus.
9000156056	Bug	In the timing diagram in Figure 5 of the DW_axi_gm databook, the sresp and svalid signals were corrected.
9000117773	Enhancement	Improve logged information by writing log information to the test.log file.
9000124629	Enhancement	Added information about the GIF Request Channel.
900097205	Enhancement	Low-power and GIF-master interfaces are not automatically exported
9000105149	Enhancement	Data bus width updated to include 8, 16, 32, 64, 128, 256, and 512, which is compatible with other AXI components.
9000105160	Enhancement	Address range updated to a continuum of 32 to 64 bits, which is compatible with other AXI components.
9000105161	Enhancement	ID range updated to extended to 12 bits, which is compatible with other AXI components.
9000105398	Enhancement	Burst length updated to extended to 8 bits, which is compatible with other AXI components.

4.1.3 DW_axi_gs—Fixed Problems/Enhancements

The following tables describe the DW_axi_gs STARs that were fixed in each of the versions prior to October 2007.

Table 4-3 STAR(s) Fixed in DW_axi_gs Version 1.03b

STAR ID	Type	Description
There are no customer STARs fixed in this version of DW_axi_gs		

Table 4-4 STARs Fixed in DW_axi_gs Version 1.03a

STAR	Type	Description
9000129519	Bug	svalid signal in Figure 5 corrected in DW_axi_gs databook.
9000105162	Enhancement	Data bus width updated to include 8, 16, 32, 64, 128, 256, and 512, which is compatible with other AXI components.
9000105163	Enhancement	Address range updated to a continuum of 32 to 64 bits, which is compatible with other AXI components.

STAR	Type	Description
9000105164	Enhancement	ID range updated to extended to 16 bits, which is compatible with other AXI components.
9000105399	Enhancement	Burst length updated to extended to 8 bits, which is compatible with other AXI components.
9000117774	Enhancement	Improve logged information by writing log information to the test.log file.
900097205	Enhancement	Low-power and GIF-slave interfaces are not automatically exported

4.1.4 DW_axi_hmx—Fixed Problems/Enhancements

The following tables describe the DW_axi_hmx STARs that were fixed in each of the versions prior to October 2007.

Table 4-5 STARs Fixed in DW_axi_hmx Version 1.02a

STAR	Type	Description
9000186649	Enhancement	DW_axi_hmx should maintain ordering read/write sequence

Table 4-6 STAR(s) Fixed in DW_axi_hmx Version 1.01b

STAR ID	Type	Description
There are no customer STARs fixed in this version of DW_axi_hmx		

Table 4-7 STARs Fixed in DW_axi_hmx Version 1.01a

STAR	Type	Description
9000155602	Bug	Missing hlock signal to Figure 11 in DW_axi_hmx databook.
9000149712	Bug	Design prefix in coreConsultant does not propagate to the testbench.
9000150514	Bug	Combinatorial timing paths exist between hready and hlock/htrans.
9000155641	Enhancement	DW_axi_hmx databook did not make clear that there cannot be more than 32 outstanding transactions at any time.

4.1.5 DW_axi_rs—Fixed Problems/Enhancements

The following tables describe the DW_axi_rs STARs that were fixed in each of the versions prior to October 2007.

Table 4-8 STAR(s) Fixed in DW_axi_rs Version 1.00c

STAR ID	Type	Description
There are no customer STARs fixed in this version of DW_axi_rs		

Table 4-9 STARs Fixed in DW_axi_rs Version 1.00b

STAR	Type	Description
9000120529	Bug	Hardcoded path in verpp script causes DW_axi_rs to crash/hang

4.1.6 DW_axi_x2h—Fixed Problems/Enhancements

The following tables describe the DW_axi_x2h STARs that were fixed in each of the versions prior to October 2007.

Table 4-10 tbd

STAR ID	Type	Description
9000186924	Bug	The “Use DesignWare foundation synthesis library” option does not work as expected with DesignWare and source license.

Table 4-11 STARs Fixed in DW_axi_x2h Version 1.03b

STAR	Type	Description
9000169761	Bug	There is a packaging issue in the DW_axi_x2h, which gives errors in the Configure Components step in cA if the user has only a source license.

Table 4-12 STARs Fixed in DW_axi_x2h Version 1.03a

STAR	Type	Description
9000134491	Bug	Legacy code switched off the use of DC-Ultra with the DW_axi_x2h.
9000106321	Enhancement	Address range now supports a continuum range 32…64.

Table 4-13 STARs Fixed in DW_axi_x2h Version 1.02a

STAR	Type	Description
9000106320	Enhancement	Increase ID width support to 16 bits.

4.1.7 DW_axi_x2p—Fixed Problems/Enhancements

The following tables describe the DW_axi_x2p STARs that were fixed in each of the versions prior to October 2007.

Table 4-14 STAR(s) Fixed in DW_axi_x2p Version 1.00c

STAR ID	Type	Description
There are no customer STARs fixed in this version of DW_axi_x2p		

Table 4-15 STARs Fixed in DW_axi_x2p Version 1.00b

STAR	Type	Description
9000155651	Bug	Corrected the number of APB slaves to which a DW_axi_x2p can connect
9000158831	Bug	1.00a DW_axi_x2p required a Vera license
9000126477	Enhancement	Clarification that read data beats on AXI side return SLVERR.
9000162425	Bug	Endian diagram corrected.

4.1.8 DW_axi_x2x—Fixed Problems/Enhancements

The following tables describe the DW_axi_x2x STARs that were fixed in each of the versions prior to October 2007.

Table 4-16 tbd

STAR ID	Type	Description
There are no customer STARs fixed in this version of DW_axi_x2x		

Table 4-17 STAR(s) Fixed in DW_axi_x2x Version 1.01b

STAR ID	Type	Description
There are no customer STARs fixed in this version of DW_axi_x2x		

Table 4-18 tbd

STAR	Type	Description
9000170378	Bug	Design prefixing not working in testbench; coreAssembler fails.

Table 4-19 STARs Fixed in DW_axi_x2x Version 1.01a (November 2006)

STAR	Type	Description
9000158639	Enhancement	Limits for the number of outstanding read or write transactions were increased from 16 unique transaction IDs (X2X_MAX_UWIDA and X2X_MAX_URIDA) to 32.
9000118920	Enhancement	Add support for transaction upsizing and burst consolidation when Master Port data width is less than Slave Port data width