Table 1

Table 1											
		s0[1]	**s0[0]**	**s1**	**s2**	**s3**	**s4**	**reg_write**	**mem_word**	**mem_write**	**mem_read**
000000	pc_reg_enable=0			-	-	-	-	0	-	0	0
000001		0	0	0	0	0	1	1	-	0	0
000010		0	0	0	0	0	1	1	-	0	0
000011		0	0	0	0	0	1	1	-	0	0
000100		0	0	0	0	0	1	1	-	0	0
000101		0	0	0	0	0	1	1	-	0	0
000110		0	0	0	0	0	1	1	-	0	0
000111		0	0	0	0	0	1	1	-	0	0
001000		0	0	-	0	0	-	1	-	0	0
001001		0	0	0	0	0	1	1	-	0	0
001010		0	0	0	0	0	1	1	-	0	0
001011		0	0	-	0	0	-	1	-	0	0
001100		0	0	-	0	0	-	1	-	0	0
001101		0	0	-	0	0	-	1	-	0	0
001110		0	0	-	0	0	-	1	-	0	0
001111		0	0	0	0	0	1	1	-	0	0
010000		1	0	-	0	1	0	1	-	0	0
010001		1	0	-	0	1	0	1	-	0	0
010010		0	0	-	0	0	0	1	-	0	0
010011		0	0	-	0	0	0	1	-	0	0
010100		0	0	-	0	0	0	1	-	0	0
010101		0	0	-	0	0	0	1	-	0	0
010110		0	0	-	0	0	0	1	-	0	0
010111		0	0	-	0	0	0	1	-	0	0
011000		0	0	1	1	0	0	1	1	0	1
011001		0	0	1	-	0	0	0	1	1	0
011010		0	0	1	1	0	0	1	0	0	1
011011		0	0	1	-	0	0	0	0	1	0
011100		1	0	-	-	-	-	0	-	0	0
011101		1	1	-	-	-	-	0	-	0	0
011110	if branch	0	1	-	-	-	-	0	-	0	0
011111	if branch	0	1	-	-	-	-	0	-	0	0