

		pc_src	reg_src	reg_dst	alu_src1	alu_src2	reg_write	mem_word	mem_write	mem_read
ALU (000001 - 001111)		0	0	0	0	1	1	0	0	0
IMM1 (010000 - 010001)		0	1	0	1	0	1	0	0	0
IMM2 (010010 - 010111)		0	0	0	0	0	1	0	0	0
LW (011000)		0	1	1	0	0	1	1	0	1
SW (011001)		0	1	0	0	0	0	1	1	0
LB (011010)		0	1	1	0	0	1	0	0	1
SB (011011)		0	1	0	0	0	0	0	1	0
JMP (011100)		2	0	0	0	0	0	0	0	0
JR (011101)		3	1	0	0	1	0	0	0	0
BEQ (011110)		1 & branch	1	0	0	1	0	0	0	0
BLT (011111)		1 & branch	1	0	0	1	0	0	0	0
HLT (000000)	pc_enable = 0	0	0	0	0	0	0	0	0	0