Table of Content

Introduction of Full Adder:

Full Adder is the adder which adds three inputs and produces two outputs. The first two inputs are A and B and the third input is an input carry as C-IN.

The output carry is designated as C-OUT and the normal output is designated as S which is SUM.

A full adder logic is designed in such a manner that can take eight inputs together to create a byte-wide adder and cascade the carry bit from one adder to the another.

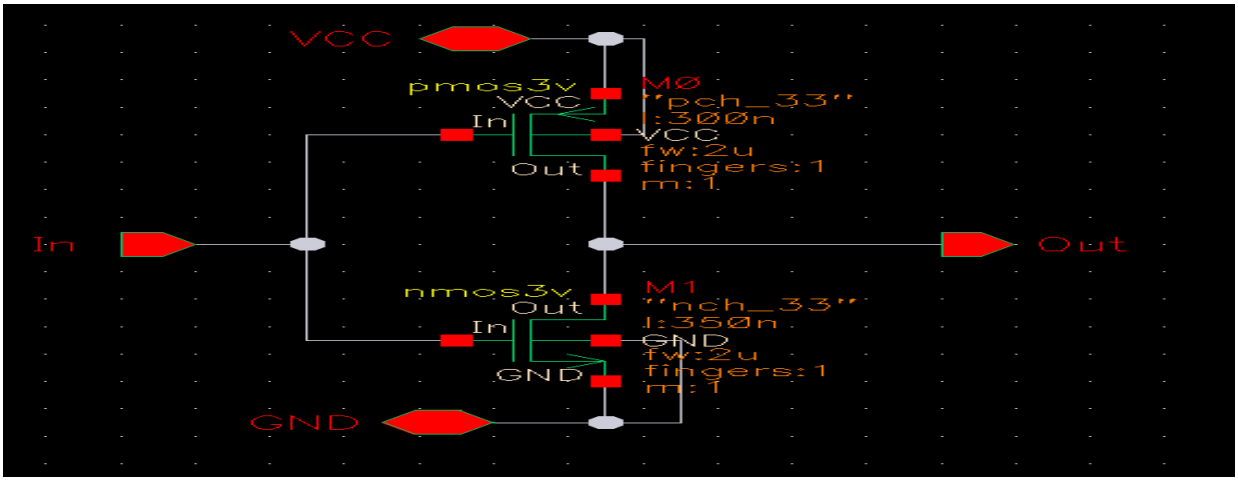
Inputs			Outputs	
A	B	C – IN	Sum	C - Out
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

Inverter :

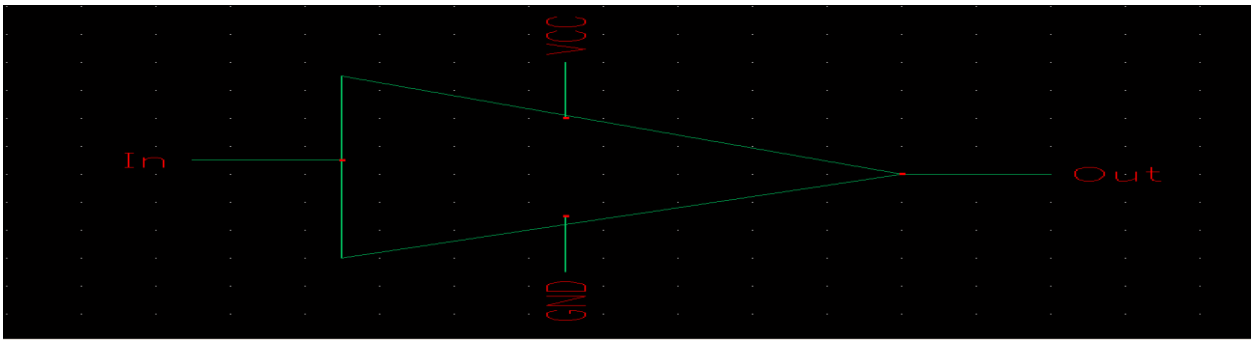
It is device that complement the output if the input is one , the output will be is zero , and verse versa.

Input	Output
1	0
0	1

Schematic :

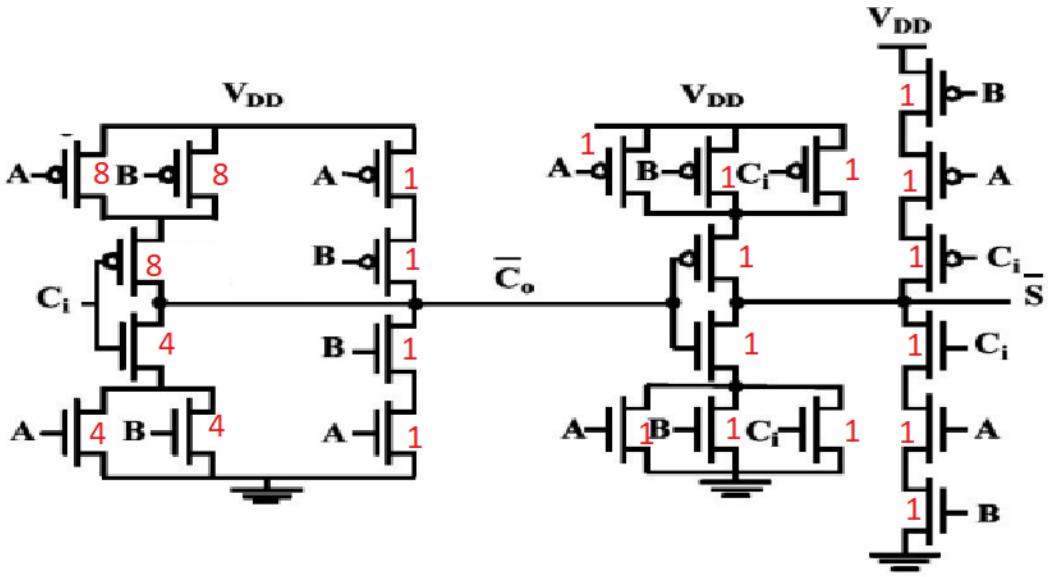


Symbol :



Full Adder :

Design strategy:



To design the Full adder , we split the inputs to two types :

1- Critical input : Ci(carry input)
2- Non critical input : A, B

Second step we design carry output as the mirror design (self dual function : when invert the inputs , the output will be inverted) , and design the sum as self dual function in carry out term

After design the transistor level , we will arrange the input , we put carry input in inner output because it is critical input like as the first and third stage

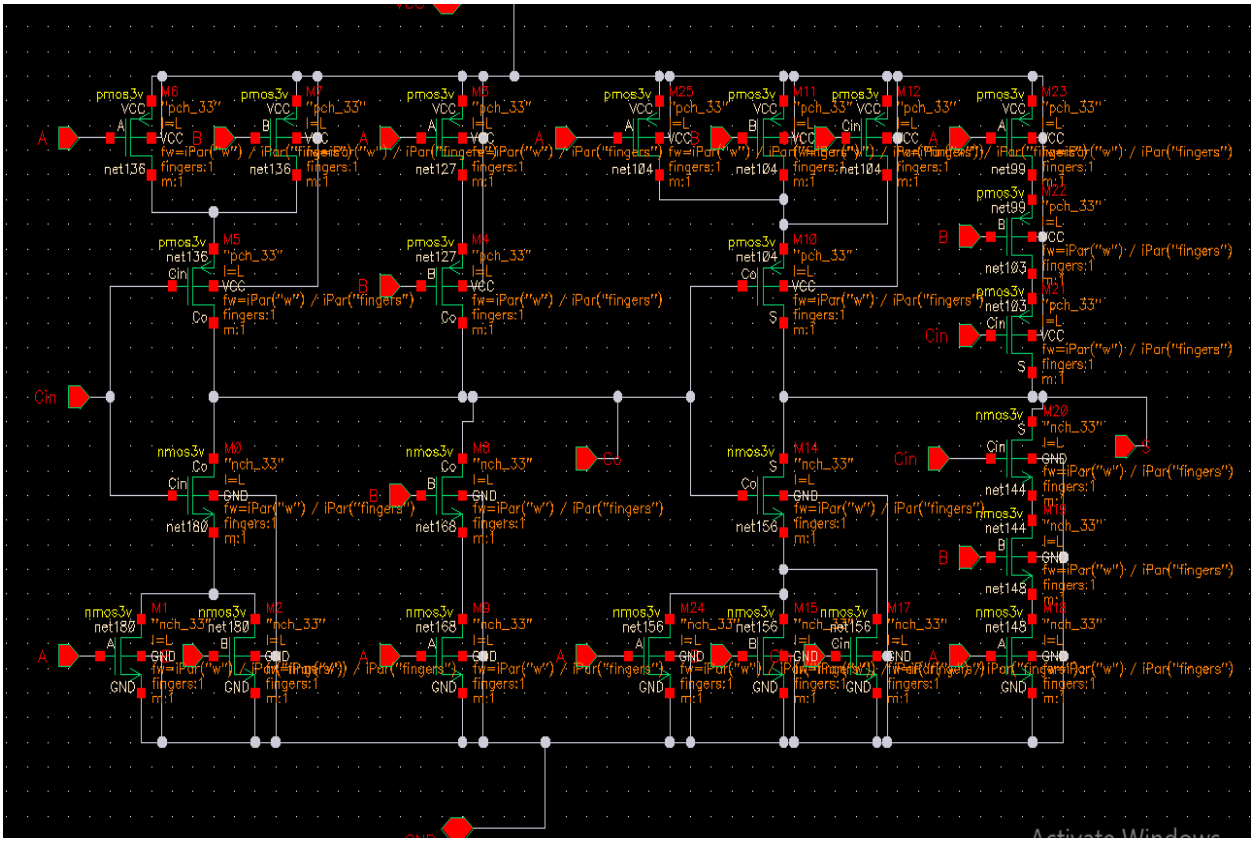
We care the path of carry output because it is the critical path , because the carry output will be the carry input in the second stage of another full adder

Sizing :

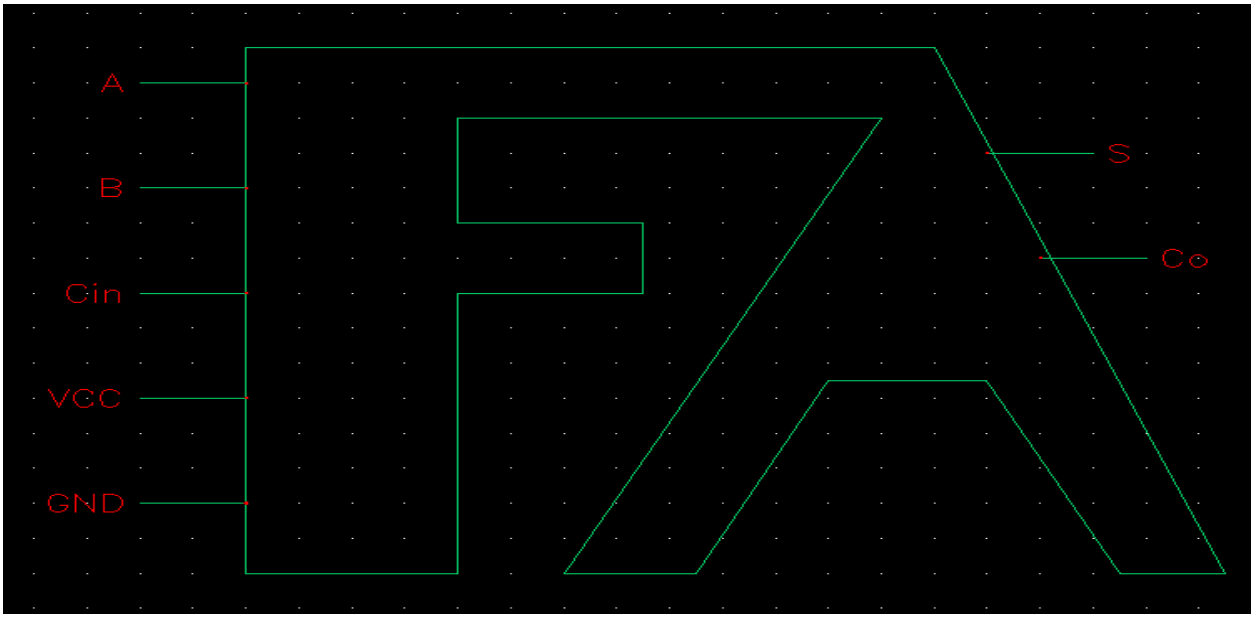
The first stage , we size the NMOS by 4 (NMOS sizing by 2) and PMOS by 8 (PMOS sizing by 4)

The second stage and The third stage, we size the NMOS and PMOS by the minimum sizing by 1 (NMOS sizing by ½) and (PMOS sizing by ½) , I made this because A and B are not critical path but I stage in path of the carry ,then I need to decrease the capacitance to decrease of delay of the path

Schematic :

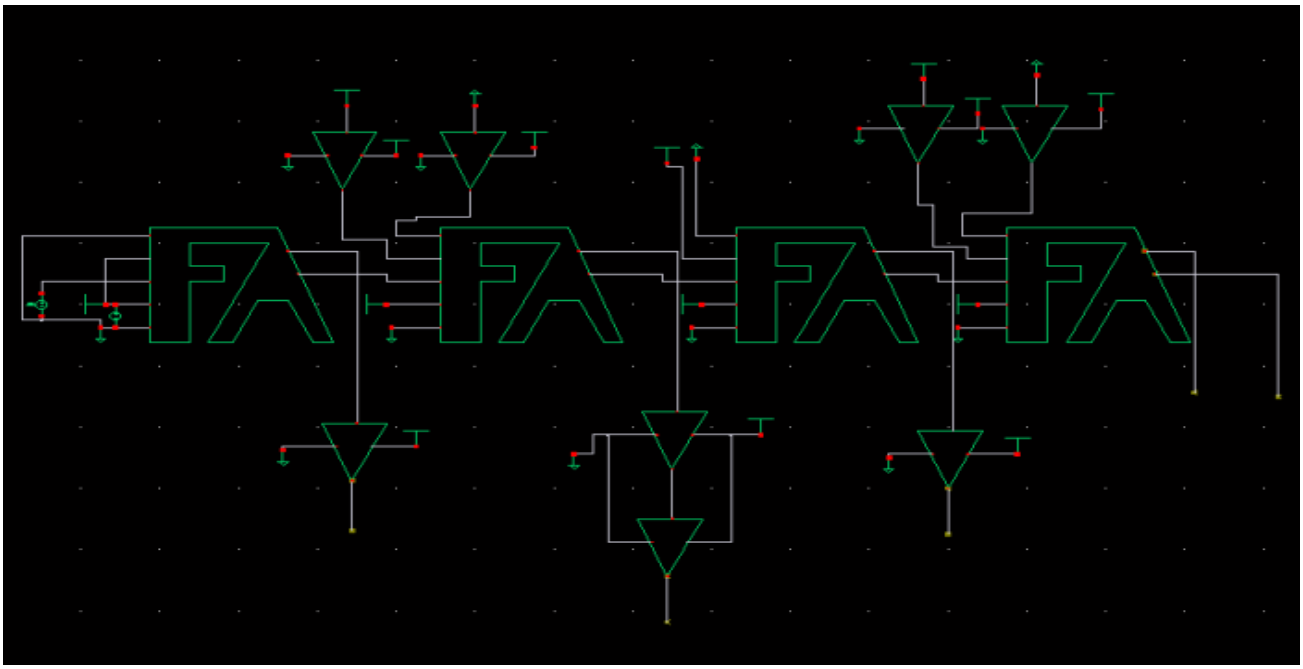


Symbol :



4-Bit Full Adder :

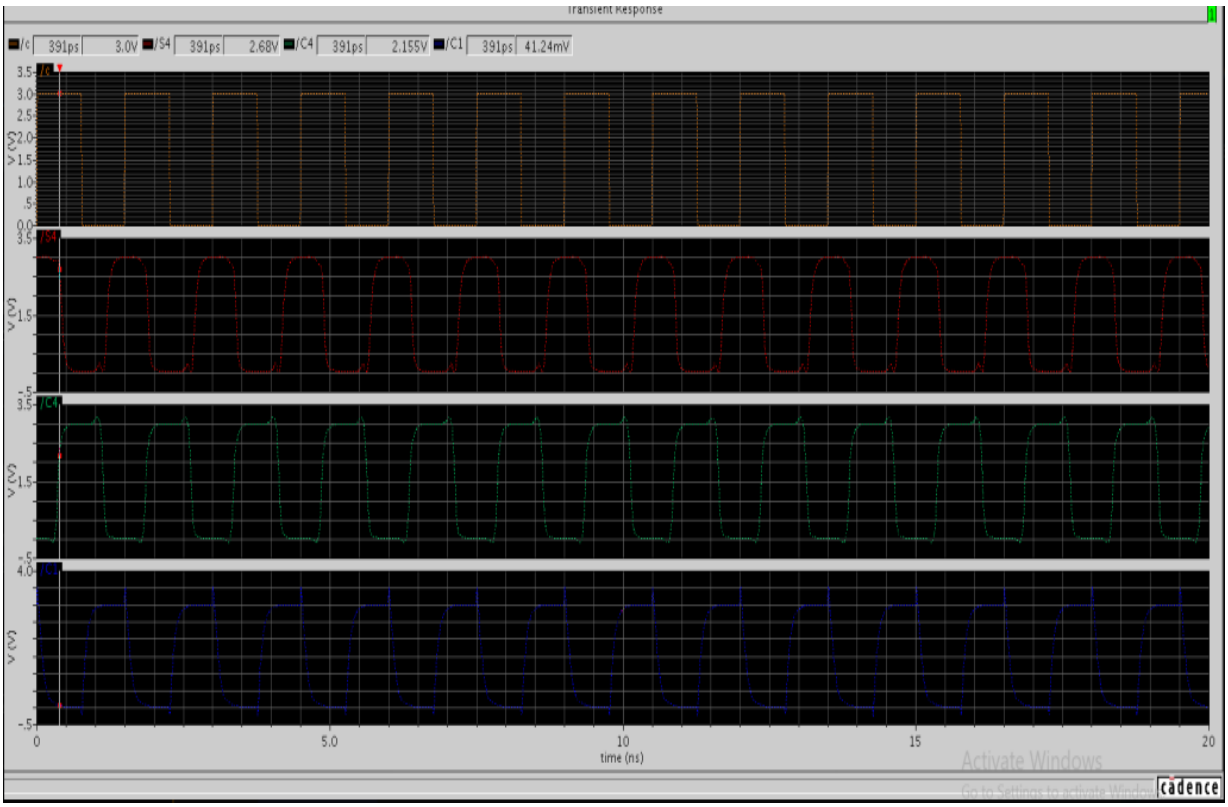
Schematic :



Design strategy:

To design 4-bit adder , the first stage out the inverted carry and inverted sum to decrease the logic gate (inverter to invert the c out from stage 1 to become c input in stage two) we inverted A , B input and no inverted the carry out from previous stage then the carry out from stage two is not inverted and sum from stage two is not inverted .

Operation:



Delay of 4-bit Adder:

In this design of full adder , we interested the delay of the carry path , because the carry output from any full adder will enter to next full adder

From previous tricks of design like as the asymmetric gates (put carry input in inner output) , using self dual function