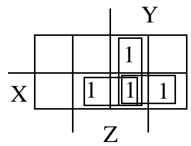
CHAPTER 3

3-1.

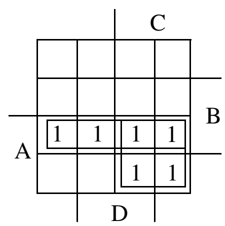
Place a 1 in each K-map cell where 2 or more inputs are equal to 1.



$F = XZ + XY + YZ$

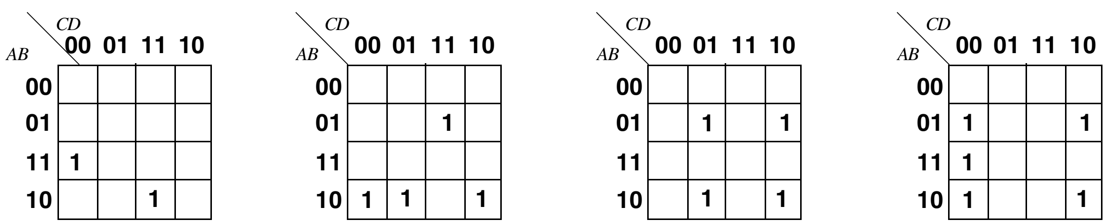
This is the same function as the carry for the full adder.

3-2.*



$F = AB + AC$

3-3.



$W = A B \overline{C}\,\overline{D} + A \overline{B} C D$ $X = \overline{A} B C D + A \overline{B}\,\overline{C} + A \overline{B}\,\overline{D}$ $Y = \overline{A} B (\overline{C} D + C \overline{D}) + A \overline{B}(\overline{C} D + C \overline{D})$ $Z = \overline{A} B \overline{D} + B \overline{C}\,\overline{D} + A \overline{B}\,\overline{D}$

3-4. a) For the 3 x 3 pattern, there are exactly three row, three column and two diagonal combinations that represent a win for the X player: W = X1 X2 X3 + X4 X5 X6 + X7 X8 X9 + X1 X4 X7 + X2 X5 X8 + X3 X6 X9 + X1 X5 X9 + X3 X5 X7 Gate Input cost = 32

b) W = X5 (X1 X9 + X2 X8 + X3 X7 + X4 X6) + X1 X2 X3 + X1 X4 X7 + X7 X8 X9 + X3 X6 X9 Gate Input Cost = 30

3-5. a) For the 4 x 4 pattern, there are exactly four row, four column and two diagonal combinations that represent a win for the X player: W = X1 X2 X3 X4 + X5 X6 X7 X8 + X9 X10 X11 X12 + X13 X14 X15 X16 + X1 X5 X9 X13 X2 X6 X10 X14 + X3 X7 X11 X15 + X4 X8 X12 X16 + X1 X6 X11 X16 + X4 X7 X10 X13 Gate Input cost = 50

b) W = X1(X2 X3 X4 + X5 X9 X13 + X6 X11 X15) + X7(X5 X6 X8 + X3 X11 X15 + X4 X10 X13) + X9 X10 X 11 X12 + X13 X14 X15 X16 + X2 X6 X10 X14 + X4 X8 X12 X16 Gate Input Cost = 48

3-6.

a) Detecting a change in one-out-of-three inputs can be done using a parity function as Z. The truth table shown is for even parity. For this case,

$$Z = X1 \oplus X2 \oplus X3$$

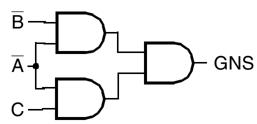
If odd parity is chosen, then an alternative result for Z is:

$$Z = \overline{X1 \oplus X2 \oplus X3}$$

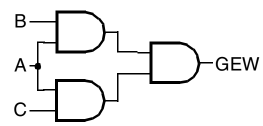
X1	X2	X3	Z
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

3-7.+

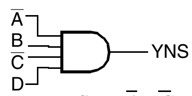
ABCD	GNS	YNS	RNS	GEW	YEW	REW
0000	1	0	0	0	0	1
0001	1	0	0	0	0	1
0011	1	0	0	0	0	1
0010	1	0	0	0	0	1
0110	1	0	0	0	0	1
0111	1	0	0	0	0	1
0101	0	1	0	0	0	1
0100	0	0	1	0	0	1
1100	0	0	1	1	0	0
1101	0	0	1	1	0	0
1111	0	0	1	1	0	0
1110	0	0	1	1	0	0
1010	0	0	1	1	0	0
1011	0	0	1	1	0	0
1001	0	0	1	0	1	0
1000	0	0	1	0	0	1



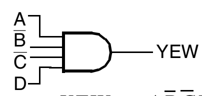
$$GNS = \overline{A}C + \overline{A}\,\overline{B}$$



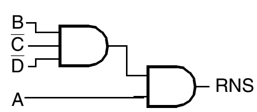
$$GEW = AB + AC$$



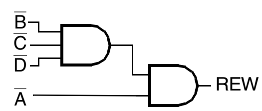
$$YNS = \overline{A}B\overline{C}D$$



$$YEW = A\overline{B}\,\overline{C}D$$



$$RNS = A + B\overline{C}\,\overline{D}$$



$$REW = \overline{A} + \overline{B}\,\overline{C}\,\overline{D}$$

3-8.

A	B	C	S5	S4	S3	S2	S1	S0
0	0	0	0	0	0	0	0	0
0	0	1	0	0	0	0	0	1
0	1	0	0	0	0	1	0	0
0	1	1	0	0	1	0	0	1
1	0	0	0	1	0	0	0	0
1	0	1	0	1	1	0	0	1
1	1	0	1	0	0	1	0	0
1	1	1	1	1	0	0	0	1

$S0 = C$

$S1 = 0$

$S2 = \overline{A}B\overline{C} + AB\overline{C}$

$S3 = \overline{A}BC + A\overline{B}C$

$S4 = A\overline{B} + AC$

$S5 = AB$

3-9.+

A	B	C	D	S2	S1	S0
0	0	0	0	0	0	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	1	0
0	1	0	0	0	1	0
0	1	0	1	0	1	0
0	1	1	0	0	1	0
0	1	1	1	0	1	1
1	0	0	0	0	1	1
1	0	0	1	0	1	1
1	0	1	0	0	1	1
1	0	1	1	0	1	1
1	1	0	0	0	1	1
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	1	0	0

$S0 = \overline{B}\,\overline{C}\,D + \overline{B}\,C\,\overline{D} + A\overline{B} + A\overline{C}\,\overline{D} + \overline{A}BCD$

$S1 = \overline{A}B + A\overline{B} + \overline{A}CD + B\overline{C}\,\overline{D}$

$S2 = ABC + ABD$

3-10.

A	B	C	D	W	X	Y	Z
0	0	0	0	0	1	1	0
0	0	0	1	0	1	1	1
0	0	1	0	1	0	0	0
0	0	1	1	1	0	0	1
0	1	0	0	1	0	1	0
0	1	0	1	1	0	1	1
0	1	1	0	1	1	0	0
0	1	1	1	1	1	0	1
1	0	0	0	1	1	1	0
1	0	0	1	1	1	1	1
1010 to 1111				XXXX			

$W = A + B + C$

$X = \overline{B}\,\overline{C} + BC$

$Y = \overline{C}$

$Z = D$

3-11.

a)

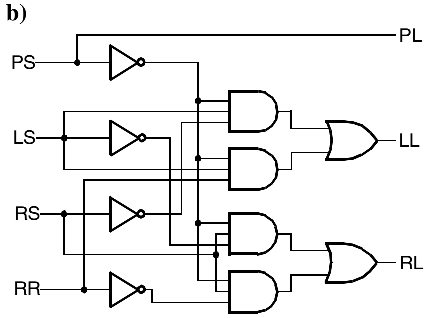
PS	LS	RS	RR	PL	LL	RL
0	0	0	0	0	0	0
0	0	0	1	0	0	0
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	0	1	0
0	1	0	1	0	1	0
0	1	1	0	0	0	1
0	1	1	1	0	1	0
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	1	0	0
1	0	1	1	1	0	0
1	1	0	0	1	0	0
1	1	0	1	1	0	0
1	1	1	0	1	0	0
1	1	1	1	1	0	0

$PL = PS$

$LL = \overline{PS}\;LS\;\overline{RS} + \overline{PS}\;LS\;RR$

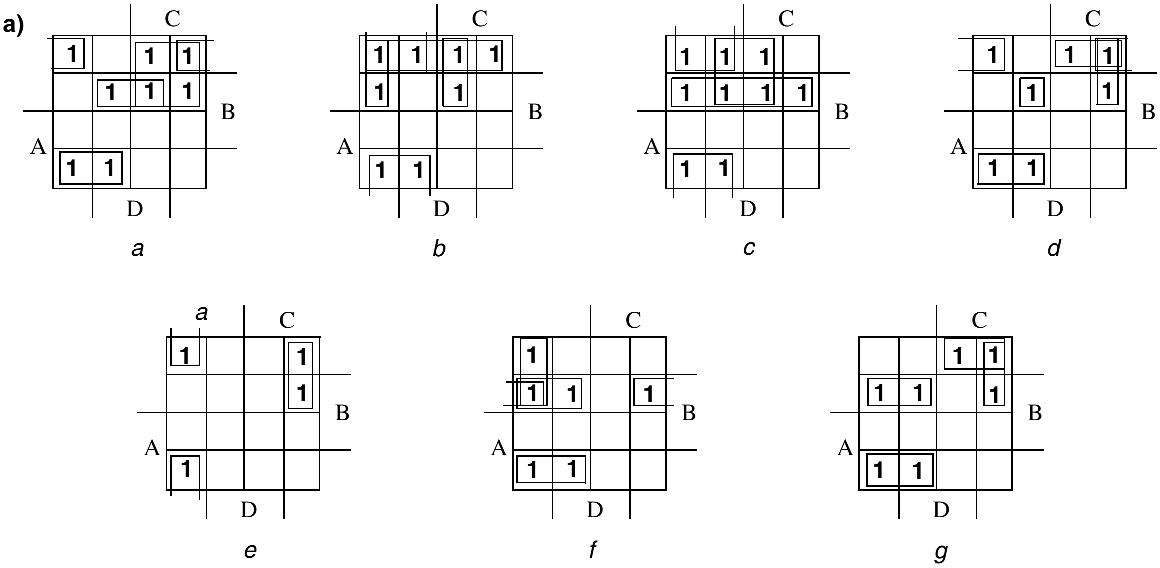
$RL = \overline{PS}\;\overline{LS}\;RS + \overline{PS}\;RS\;\overline{RR}$

b)



3-12.

a)



b)

$a = \overline{A}C + \overline{A}\,\overline{B}\,\overline{D} + \overline{A}BD + A\overline{B}\,\overline{C}$

$b = \overline{A}\,\overline{B} + \overline{B}\,\overline{C} + \overline{A}\,\overline{C}\,\overline{D} + \overline{A}CD$

$c = \overline{A}B + \overline{B}\,\overline{C} + \overline{A}D$

$d = \overline{A}B\overline{C}D + A\overline{B}\,\overline{C} + \overline{A}\,\overline{B}\,\overline{D} + \overline{A}\,\overline{B}C + \overline{A}C\overline{D}$

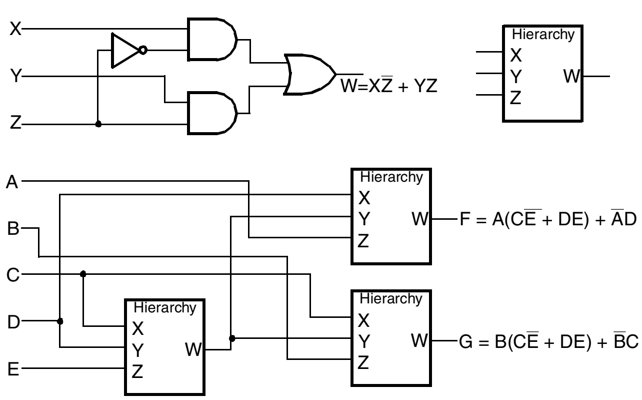
$e = \overline{B}\,\overline{C}\,\overline{D} + \overline{A}C\overline{D}$

$f = A\overline{B}\,\overline{C} + \overline{A}B\overline{D} + \overline{A}B\overline{C} + \overline{A}\,\overline{C}\,\overline{D}$

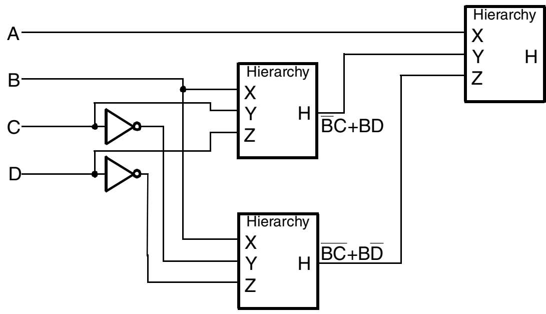
$g = A\overline{B}\,\overline{C} + \overline{A}B\overline{C} + \overline{A}\,\overline{B}C + \overline{A}C\overline{D}$

c) The following gate input counts include input inverters and share AND gates.
Total gate inputs for this solutions = 74. Total gate inputs for book solution is 70. The book solution is better by 4 gate inputs.

3-13.



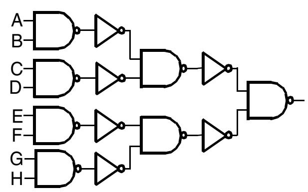
3-14.



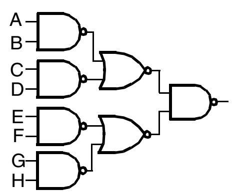
$$G = \bar{A}(\bar{B}C + BD) + A(B\bar{C} + B\bar{D})$$
$$= \bar{A}\bar{B}C + \bar{A}BD + AB\bar{C} + AB\bar{D}$$

3-15.+

a)



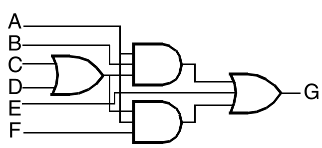
b)



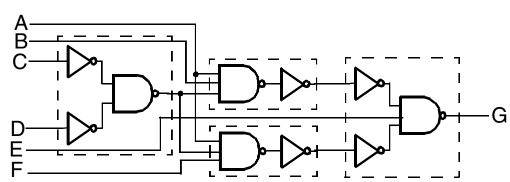
c)

Part b requires 6 fewer gates.

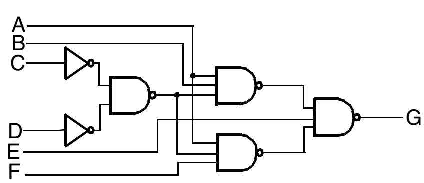
3-16.



a) Original circuit

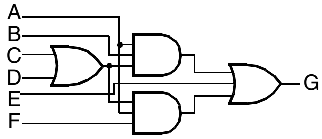


b) Replacement with equivalents

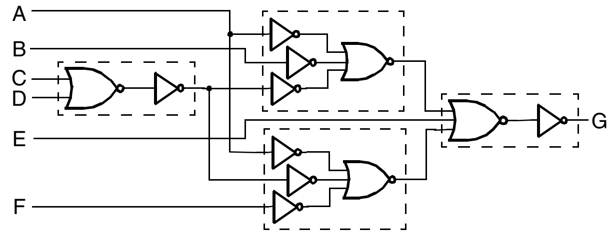


c) Cancel inverters

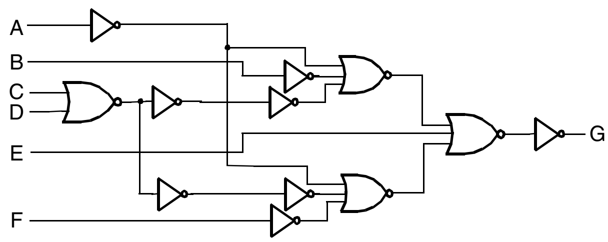
3-17.



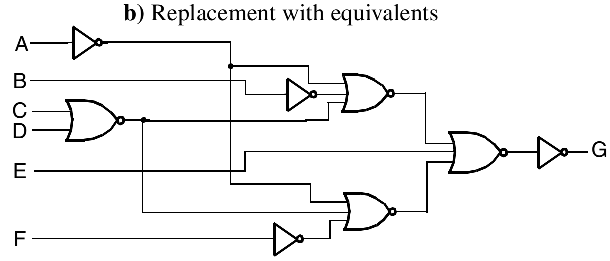
a) Original circuit



b) Replacement with equivalents

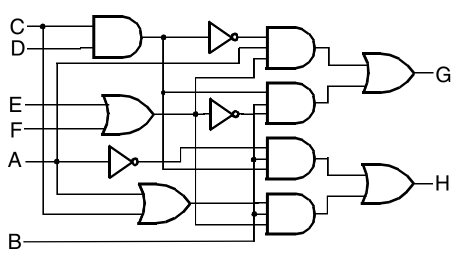


c) Manipulate inverters

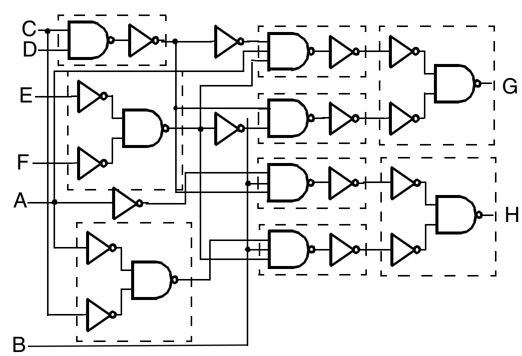


d) Cancel inverters

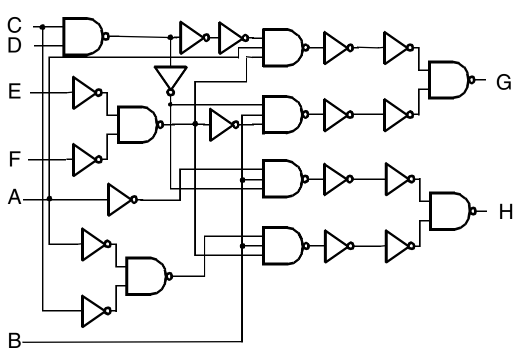
3-18.



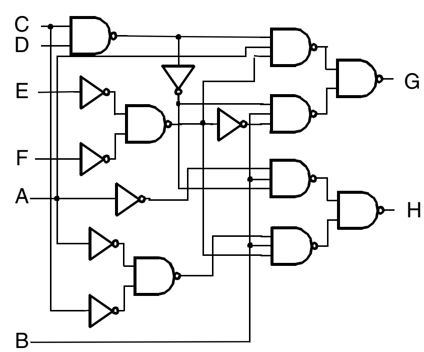
a) Original circuit



b) Replacement with equivalents

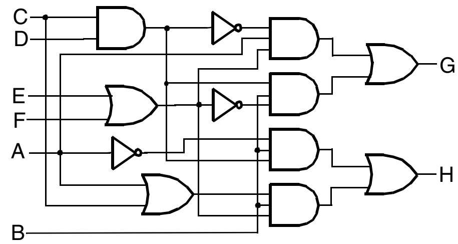


c) Manipulate inverters

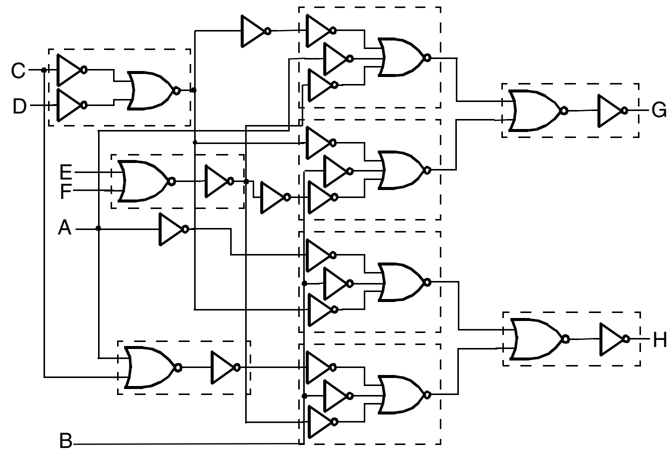


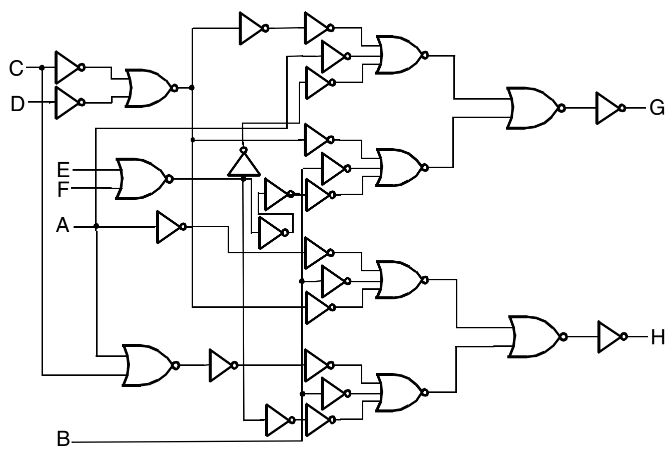
d) Cancel inverters

3-19.

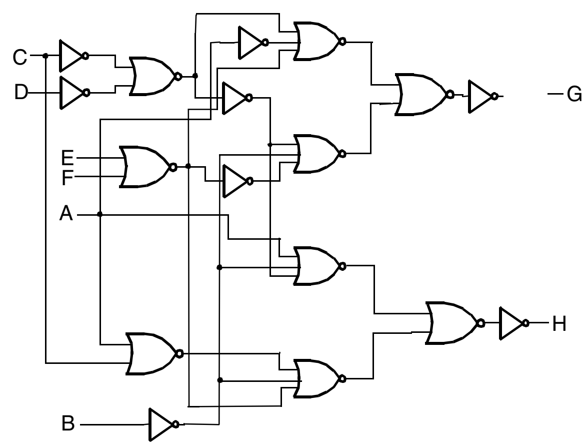


a) Original circuit



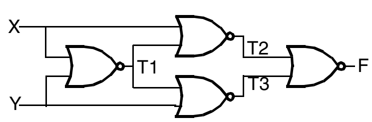


c) Manipulate inverters



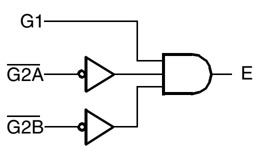
d) Cancel and minimize inverters

3-20.



$T1 = \overline{X}\,\overline{Y}$
$T2 = \overline{X}\,Y$
$T3 = X\,\overline{Y}$
$F = XY + \overline{X}\,\overline{Y}$

3-21.



$E = G1 \cdot \overline{G2A} \cdot \overline{G2B}$

$Y0 = \overline{\overline{A}\,\overline{B}\,\overline{C}E}$

$Y1 = \overline{A\overline{B}\,\overline{C}E}$

$Y2 = \overline{\overline{A}B\overline{C}E}$

$Y3 = \overline{AB\overline{C}E}$

$Y4 = \overline{\overline{A}\,\overline{B}CE}$

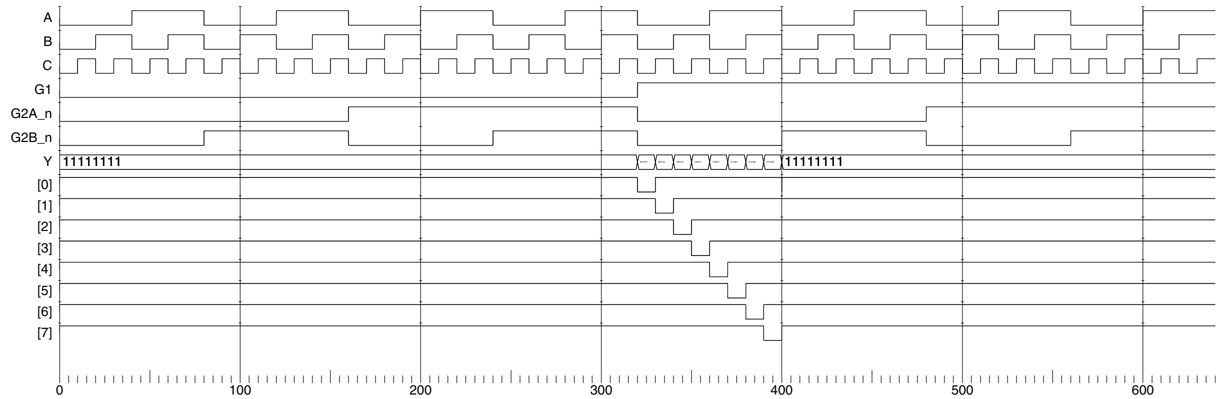
$Y5 = \overline{A\overline{B}CE}$

$Y6 = \overline{\overline{A}BCE}$

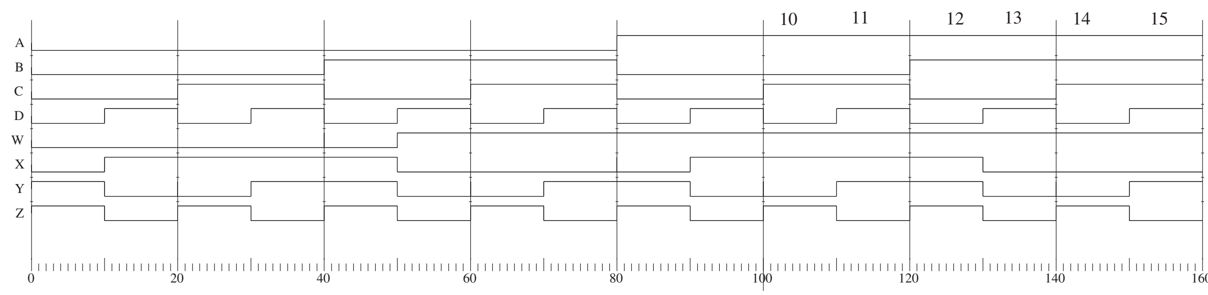
$Y7 = \overline{ABCE}$

Except for G1 = 1 and G2A and G2B = 0, the outputs Y0 through Y7 are all 1's. Otherwise, one of Y0 through Y7 is equal to 0 with all others equal to 1. The output that is equal to 0 has index i = decimal value of the values of (A,B,C) in binary. E.g., if (A,B,C) = (1,1,0), then Y6 = 0.

3-22.

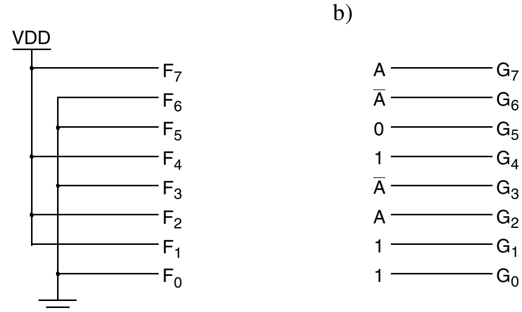


3-23.



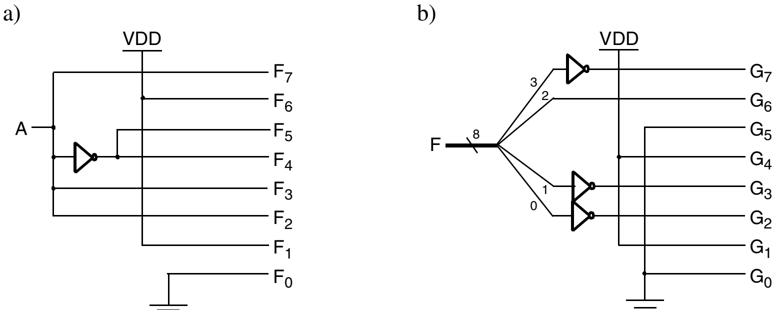
3-24.*

a) b)



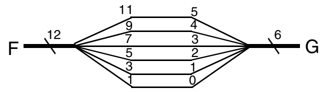
3-25.

a) b)

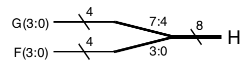


3-26.

a)

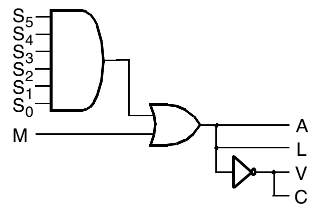


b)

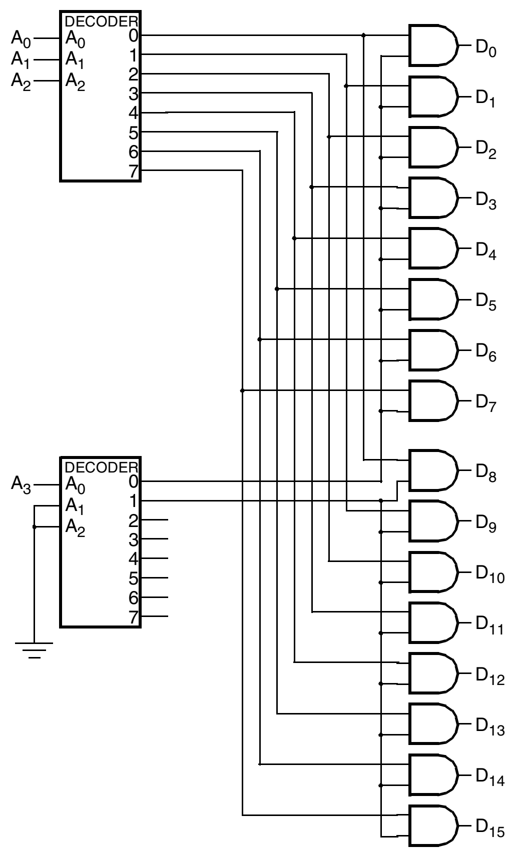


3-27.

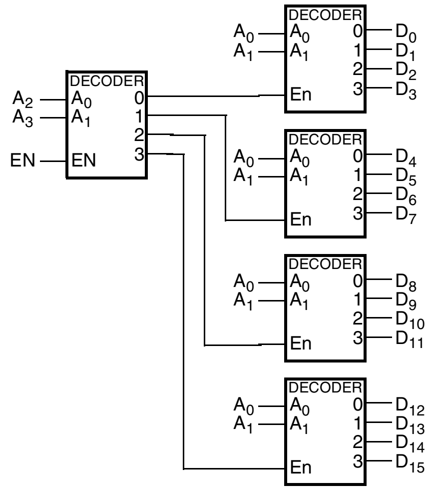
$$A = (S_0 \cdot S_1 \cdot S_2 \cdot S_3 \cdot S_4 \cdot S_5) + M$$
$$L = A$$
$$V = \overline{A} = \overline{(S_0 \cdot S_1 \cdot S_2 \cdot S_3 \cdot S_4 \cdot S_5) + M}$$
$$C = V$$



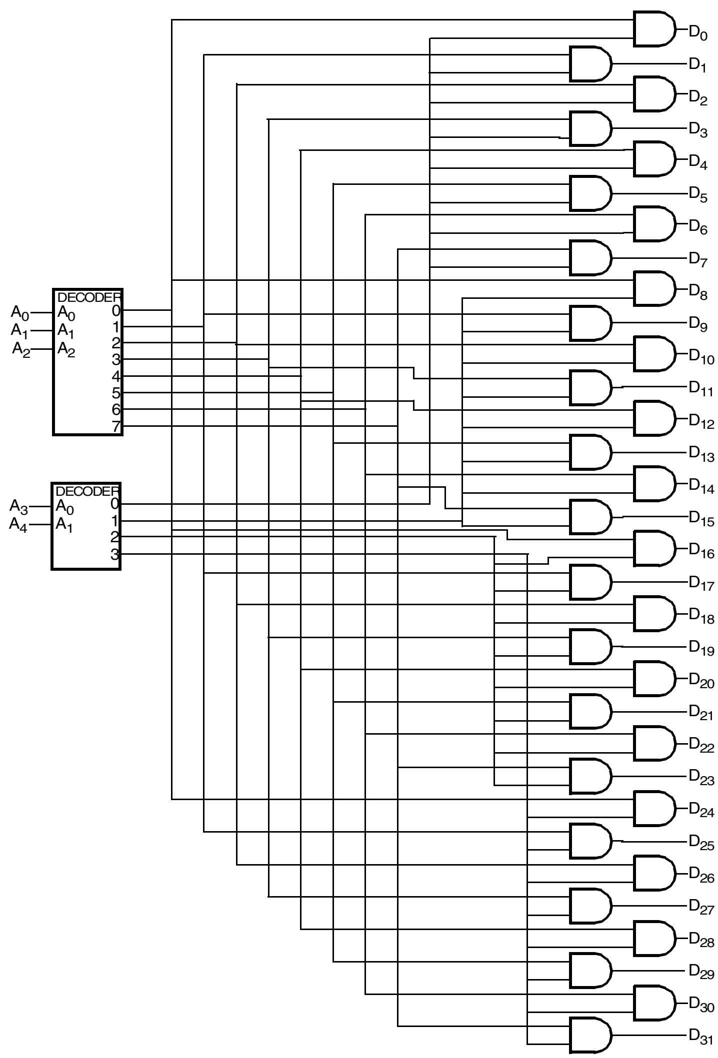
3-28.



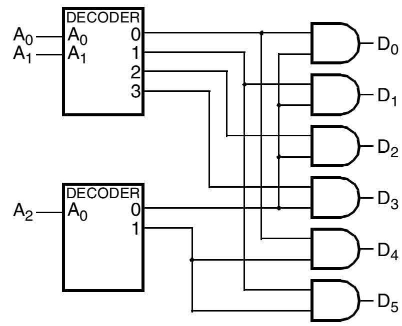
3-29.


DECODER
A2
A3
EN
A0
A1
EN
0
1
2
3
En
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15

3-30.*


DECODER
A0
A1
A2
A3
A4
0
1
2
3
4
5
6
7
D0
D31

3-31. (Errata: Replace “4” with “3” in “4-to-6-line decoder”)

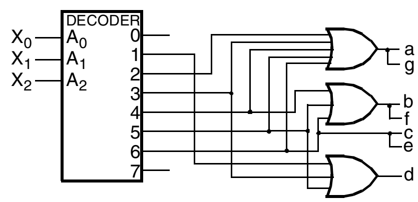


3-32.

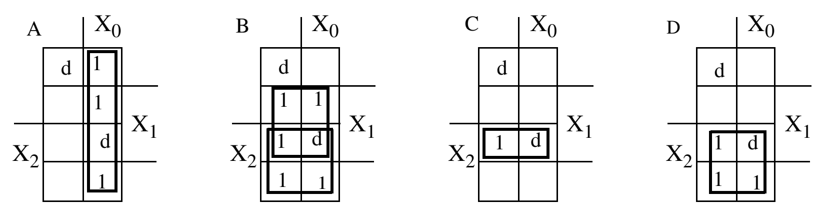
a) The Truth Table:

Note: a = g, b = f, and c = e.

X_2	X_1	X_0	a	b	c	d	e	f	g
0	0	0	d	d	d	d	d	d	d
0	0	1	0	0	0	1	0	0	0
0	1	0	1	0	0	0	0	0	1
0	1	1	1	0	0	1	0	0	1
1	0	0	1	1	0	0	0	1	1
1	0	1	1	1	0	1	0	1	1
1	1	0	1	1	1	0	1	1	1
1	1	1	d	d	d	d	d	d	d



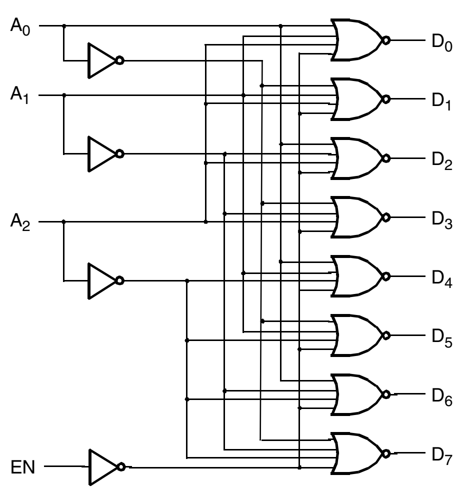
b) A = {d}
B = {a,g}
C = {c. e}
D = {b, f}



$A = X_0$ $B = X_1 + X_2$ $C = X_1X_2$ $D = X_2$

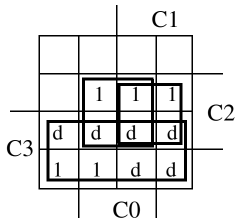
Gate input cost: b = 4 compared to a = 27 + 11 = 38

3-33.

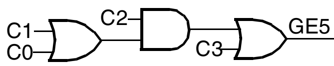


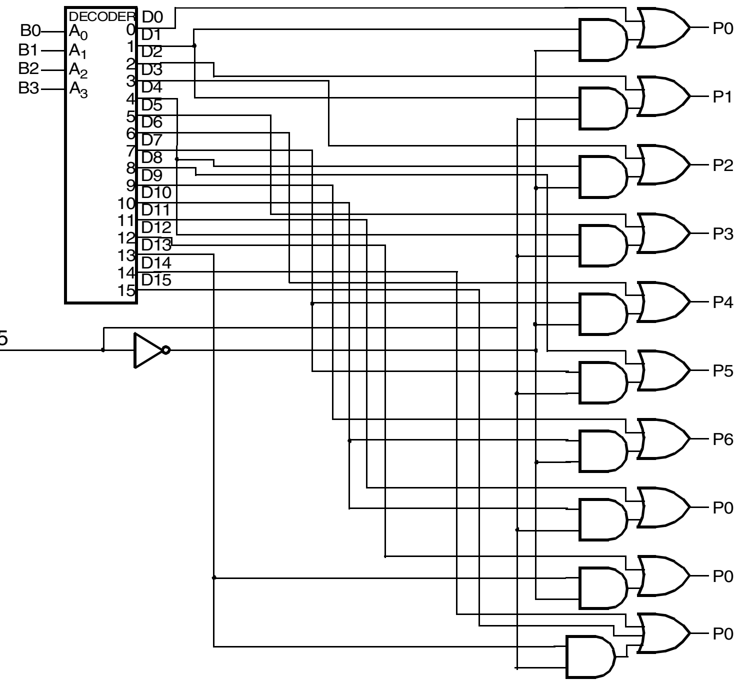
3-34.

K-Map for GE5: BCD = (C3,C2, C1, C0)



GE5 = C3 + C2 (C1 + C0)





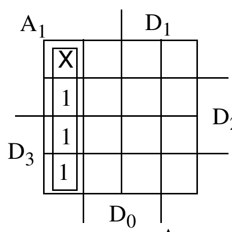
Equations for output logic:

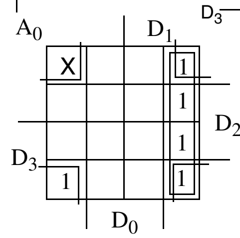
$P0 = D0 + \overline{GE5}\cdot D1$
$P1 = D2 + GE5\cdot D1$
$P2 = D3 + \overline{GE5}\cdot D4$
$P3 = D5 + GE5\cdot D4$
$P4 = D6 + \overline{GE5}\cdot D7$
$P5 = D8 + GE5\cdot D7$
$P6 = D9 + \overline{GE5}\cdot D10$
$P7 = D11 + GE5\cdot D10$
$P8 = D12 + \overline{GE5}\cdot D13$
$P9 = D14 + D15 + GE5\cdot D13$

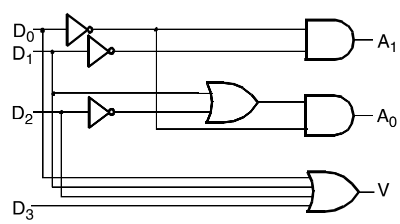
3-35.*

D_3	D_2	D_1	D_0	A_1	A_0	V
0	0	0	0	X	X	0
X	X	X	1	0	0	1
X	X	1	0	0	1	1
X	1	0	0	1	0	1
1	0	0	0	1	1	1

$$V = D_0 + D_1 + D_2 + D_3$$
$$A_0 = \overline{D}_0(D_1 + \overline{D}_2)$$
$$A_1 = \overline{D}_0\overline{D}_1$$





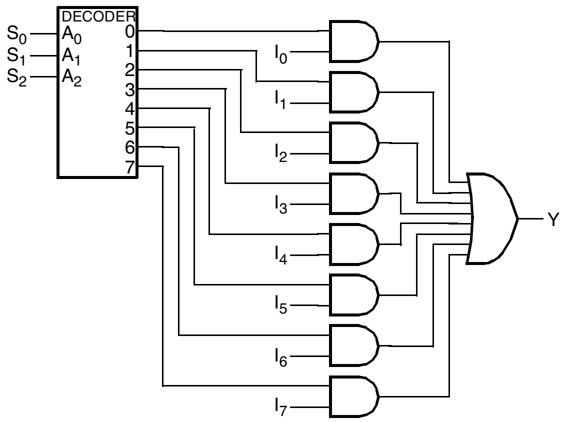


3-36.

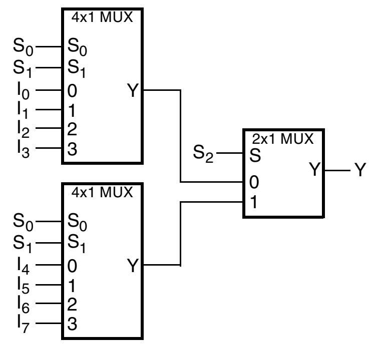
Decimal Inputs										Binary Outputs				
9	8	7	6	5	4	3	2	1	0	A_3	A_2	A_1	A_0	V
0	0	0	0	0	0	0	0	0	0	X	X	X	X	0
0	0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	0	0	0	0	0	1	X	0	0	0	1	1
0	0	0	0	0	0	0	1	X	X	0	0	1	0	1
0	0	0	0	0	0	1	X	X	X	0	0	1	1	1
0	0	0	0	0	1	X	X	X	X	0	1	0	0	1
0	0	0	0	1	X	X	X	X	X	0	1	0	1	1
0	0	0	1	X	X	X	X	X	X	0	1	1	0	1
0	0	1	X	X	X	X	X	X	X	0	1	1	1	1
0	1	X	X	X	X	X	X	X	X	1	0	0	0	1
1	X	X	X	X	X	X	X	X	X	1	0	0	1	1

3-37.

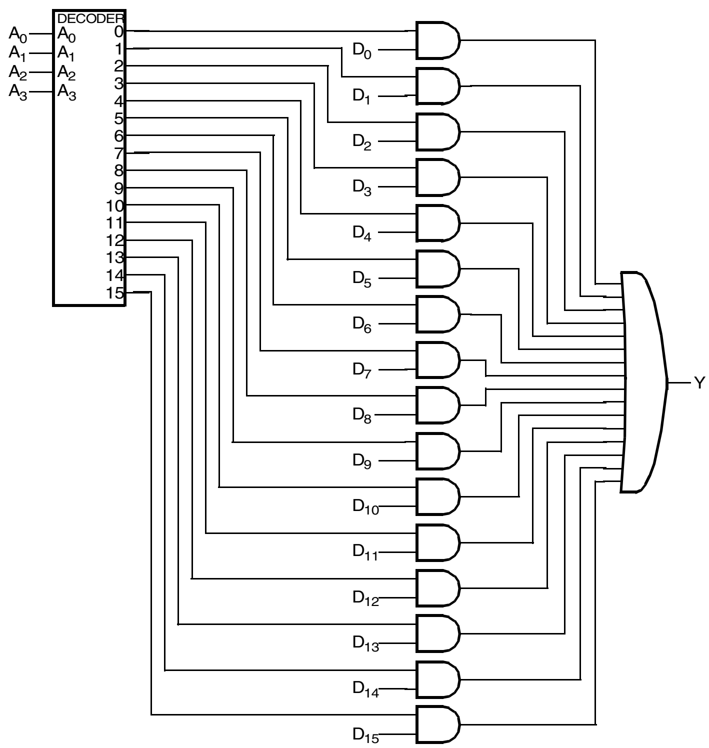
a)


DECODER
S0 A0 0
S1 A1 1
S2 A2 2
3
4
5
6
7
I0
I1
I2
I3
I4
I5
I6
I7
Y

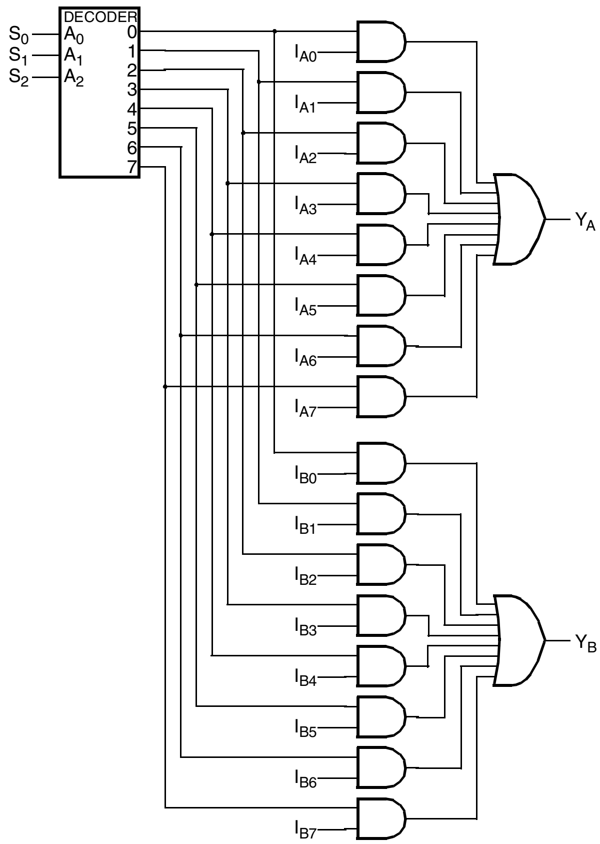
b)


4x1 MUX
S0 S0
S1 S1
I0 0 Y
I1 1
I2 2
I3 3
4x1 MUX
S0 S0
S1 S1
I4 0 Y
I5 1
I6 2
I7 3
2x1 MUX
S2 S
0 Y Y
1

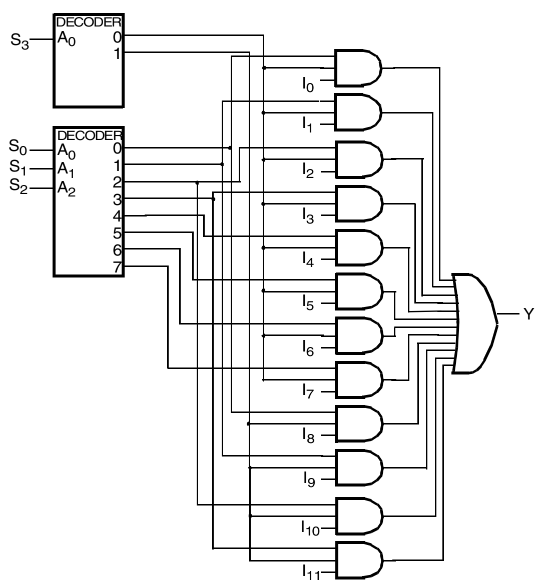
3-38.


DECODER
A0 A0 0
A1 A1 1
A2 A2 2
A3 A3 3
4
5
6
7
8
9
10
11
12
13
14
15
D0
D1
D2
D3
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
Y

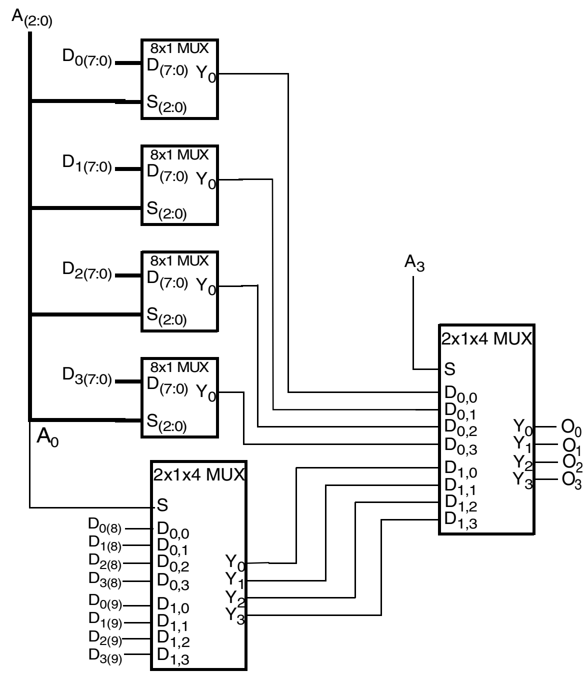
3-39.


DECODER
S_0
S_1
S_2
A_0
A_1
A_2
0
1
2
3
4
5
6
7
I_{A0}
I_{A1}
I_{A2}
I_{A3}
I_{A4}
I_{A5}
I_{A6}
I_{A7}
Y_A
I_{B0}
I_{B1}
I_{B2}
I_{B3}
I_{B4}
I_{B5}
I_{B6}
I_{B7}
Y_B

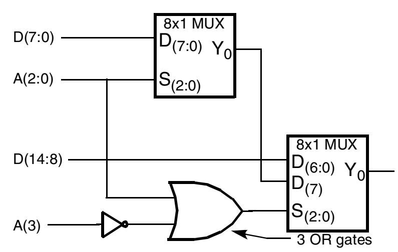
3-40.


DECODER
S_3
A_0
0
1
DECODER
S_0
S_1
S_2
A_0
A_1
A_2
0
1
2
3
4
5
6
7
I_0
I_1
I_2
I_3
I_4
I_5
I_6
I_7
I_8
I_9
I_{10}
I_{11}
Y

3-41.



3-42.*

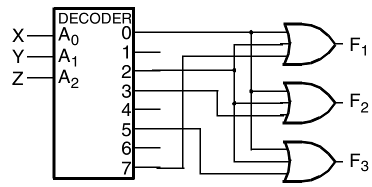


3-43.*

A_1	A_0	E	D_0	D_1	D_2	D_3
0	0	0	0	0	0	0
0	0	1	1	0	0	0
0	1	0	0	0	0	0
0	1	1	0	1	0	0
1	0	0	0	0	0	0
1	0	1	0	0	1	0
1	1	0	0	0	0	0
1	1	1	0	0	0	1

Consider E as the data input and A0, A1 as the select lines. For a given combination on (A1, A0), the value of E is distributed to the corresponding D output. For example for (A1, A0) = (10), the value of E appears on D2, while all other outputs have value 0.

3-44.

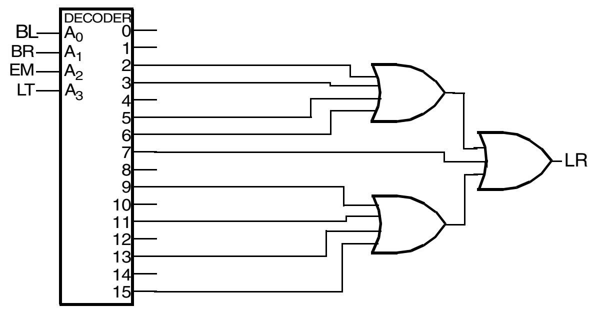


3-45.

a) LR = LT·BL + $\overline{\text{LT}}$·BR + EM·BL = BL·(LT + EM) + $\overline{\text{LT}}$·BR
RR = RT·BL + $\overline{\text{RT}}$·BR + EM·BL = BR·(RT + EM) + $\overline{\text{RT}}$·BR

b) Maximum of four inputs on OR gates assumed.

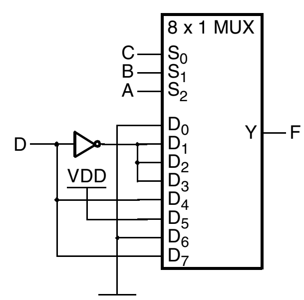
LT	EM	BR	BL	LR
0	0	0	0	0
0	0	0	1	0
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1



For RR, same circuit with LT replace by RT.

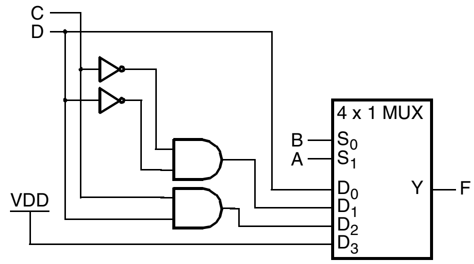
3-46.

A	B	C	D	F	
0	0	0	0	0	F = 0
0	0	0	1	0	
0	0	1	0	1	F = $\overline{D}$
0	0	1	1	0	
0	1	0	0	1	F = $\overline{D}$
0	1	0	1	0	
0	1	1	0	1	F = $\overline{D}$
0	1	1	1	0	
1	0	0	0	0	F = D
1	0	0	1	1	
1	0	1	0	1	F = 1
1	0	1	1	1	
1	1	0	0	0	F = 0
1	1	0	1	0	
1	1	1	0	0	F = D
1	1	1	1	1	



3-47.*

A	B	C	D	F	
0	0	0	0	0	
0	0	0	1	1	F=D
0	0	1	0	0	
0	0	1	1	1	
0	1	0	0	1	
0	1	0	1	0	F=$\overline{C}\ \overline{D}$
0	1	1	0	0	
0	1	1	1	0	
1	0	0	0	0	
1	0	0	1	0	
1	0	1	0	0	F=C D
1	0	1	1	1	
1	1	0	0	1	
1	1	0	1	1	
1	1	1	0	1	F=1
1	1	1	1	1	



3-48.