

# GREENPAK TECHNICAL INTRODUCTION WEBINAR

GREENPAK™

PROGRAMMABLE MIXED-SIGNAL MATRIX TECHNOLOGY  
CONFIGURABLE MIXED-SIGNAL IC (CMIC)



# AGENDA

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## GreenPAK Basics

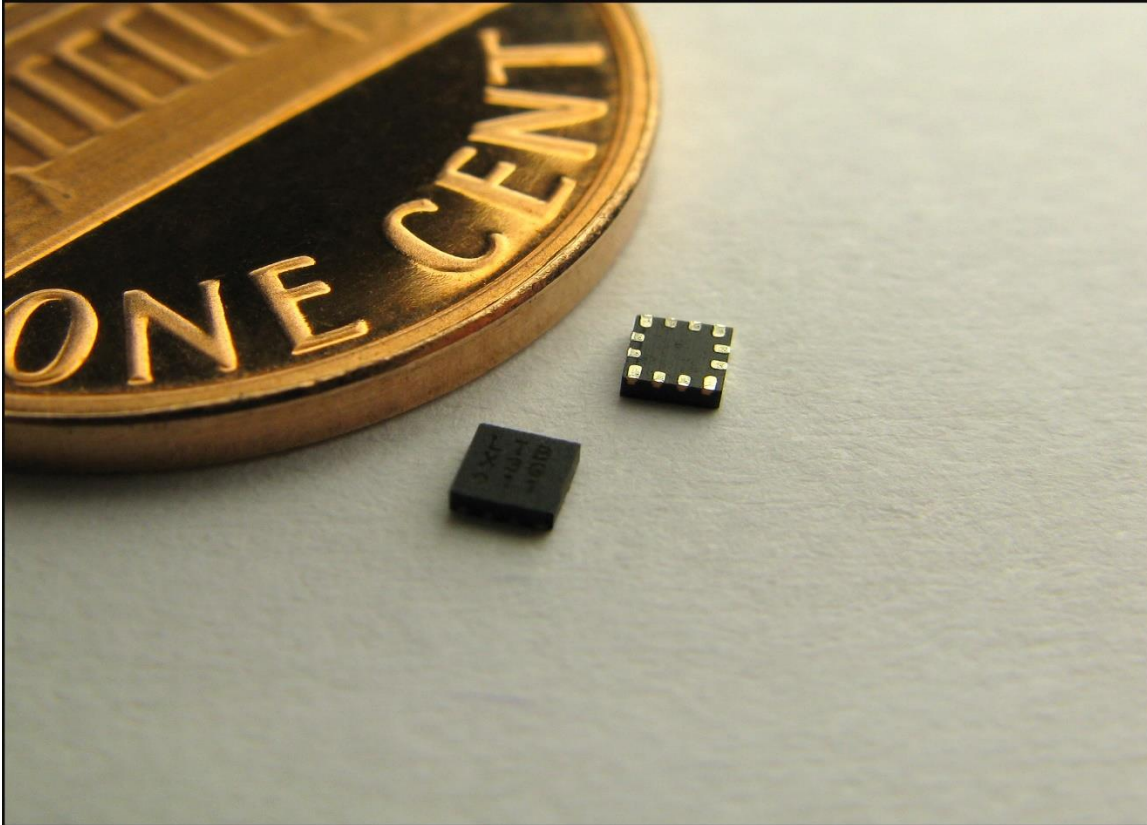
- PAD modes and its usage
- Combinational Logic. Standard and customized macrocell

# GREENPAK DESIGN BASICS

# WHAT IS GREENPAK?

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The World's 1<sup>st</sup> Custom Mixed-signal IC (CMIC) Family



- Roughly 70 ICs, each with a unique set of features
- Customizable with simple, free software
- Very small package, down to 1.2mm<sup>2</sup>
- Low power solution
- Can be used in a myriad of applications...

# WHAT CAN I DO WITH GREENPAK™

## GreenPAK Functions



Level Translation



ADC



Glue Logic



Pulse Width Modulator



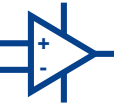
Voltage Monitor



H-/Half-Bridge\*



Finite State Machine



Op Amp



Counters / Delays



Rheostat / Potentiometer



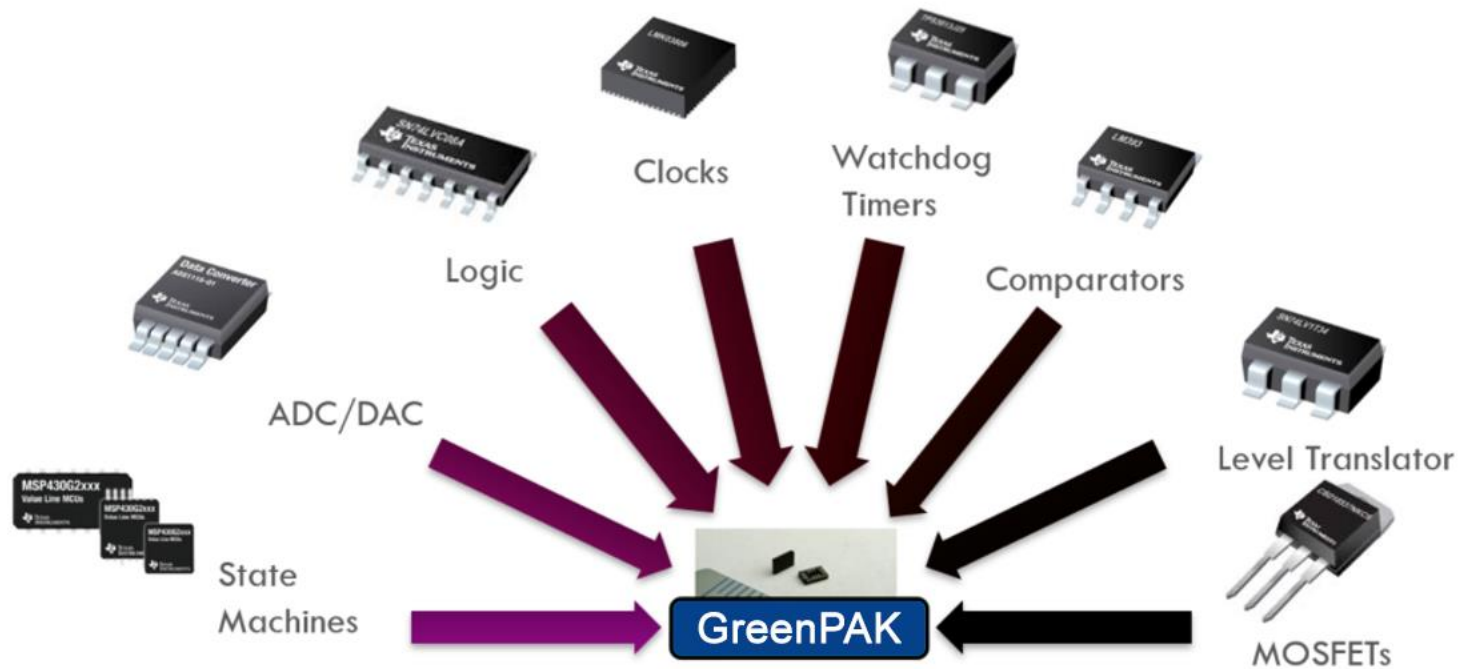
## Applications

- Supervisory Circuits
- System Reset
- LED Control
- Motor & Fan Control\*
- Power Sequencing
- Voltage Detection
- Frequency Detection
- Sensor Interface
- Port Detection
- Temperature Control
- Battery Monitor

*\*Not for Automotive qualified GreenPAK*

# WHAT DOES GREENPAK REPLACE?

GreenPAK can replace simple discrete logic , analog comparators, low end 8-bit ADC's, etc. It can be used to implement non-standard variations of reset IC's and other ASSP's without tooling or NRE. This can support new variations of applications for customers who run into design issues.



# GREENPAK DEVELOPMENT SOFTWARE

## Go Configure Software Hub

Welcome

Recent files

Develop

Demo

Application notes

Recovery files

Datasheets

User guide

Software Tool

All

Part Family

All

SLG47125V

Filter...

| Part Number        | DS                         | VDD (V)      | VDD2 (V)      | Temperature (°C) | GPI/GPO/GPIO | AEC-Q100 |
|--------------------|----------------------------|--------------|---------------|------------------|--------------|----------|
| SLG47125V          | <a href="#">Contact us</a> | 2.30 to 5.50 | 3.00 to 26.40 | -40 to 125       | 1 3 12       | -        |
| SLG47004-AP        | <a href="#">PDF</a>        | 2.40 to 5.50 | -             | -40 to 125       | 1 0 7        | Grade 1  |
| SLG47525V          | <a href="#">PDF</a>        | 1.71 to 5.50 | 0.95 to 1.98  | -40 to 85        | 1 0 10       | -        |
| SLG47528V          | <a href="#">PDF</a>        | 1.71 to 5.50 | 0.95 to 1.98  | -40 to 85        | 1 0 16       | -        |
| SLG51003V          | <a href="#">PDF</a>        | 2.80 to 5.00 | 1.20 to 5.00  | -40 to 85        | 1 0 4        | -        |
| SLG47003V          | <a href="#">PDF</a>        | 2.30 to 5.50 | -             | -40 to 85        | 5 0 10       | -        |
| SLG47001V          | <a href="#">PDF</a>        | 2.30 to 5.50 | -             | -40 to 85        | 5 0 6        | -        |
| SLG47011V          | <a href="#">PDF</a>        | 1.71 to 3.60 | -             | -40 to 85        | 1 0 13       | -        |
| SLG51000C          | <a href="#">PDF</a>        | 2.80 to 5.00 | -             | -40 to 85        | 1 0 5        | -        |
| SLG51001C          | <a href="#">PDF</a>        | 2.80 to 5.00 | -             | -40 to 85        | 1 0 3        | -        |
| SLG47011V (Rev RR) | <a href="#">PDF</a>        | 1.05 to 1.15 | 1.71 to 3.30  | -40 to 85        | 0 0 14       | -        |

Details

[\[ Contact us for Datasheet \]](#) [\[ Product page \]](#) [\[ Application notes \]](#) [\[ Resources \]](#) [\[ Get samples \]](#) [\[ Contact us \]](#)

Package:

QFN-24

Supported Development Platforms:

- Software Simulation
- GreenPAK DIP Development Board (SLG4DVKDIP) + 2x DIP Proto Board SLG47125V (SLG47125V-DIP)
- GreenPAK Advanced Development Board (SLG4DVKADV) + SLG47125V Evaluation Board (SLG47125V-EVB), is optional + GreenPAK LQFN-24 #1 (SLG4SA24LQ\_1-40x40)
- GreenPAK Lite Development Board (SLG4DVKLITE) + SLG47125V Evaluation Board (SLG47125V-EVB), is optional + GreenPAK LQFN-24 #1 (SLG4SA24LQ\_1-40x40) + 2x DIP Proto Board SLG47125V (SLG47125V-DIP), is optional

Description:

The SLG47125V provides a small, low idle power component for commonly used Mixed-Signal, BLDC motor driver, and H-Bridge functions. The user creates their circuit design by programming the one time programmable (OTP) Non-Volatile Memory (NVM) to configure the interconnect logic, the IO Pins, the High Voltage Pins, and the macrocells of the SLG47125V.

Configurable BLDC macrocells in combination with Special High Voltage outputs are used for a BLDC motor drive, as a driver for FOC controllers or load drive applications. High Voltage pins allow to design smart level translators or to drive the high voltage high current load like LED matrix. The

New

Open

Close

### Tabs

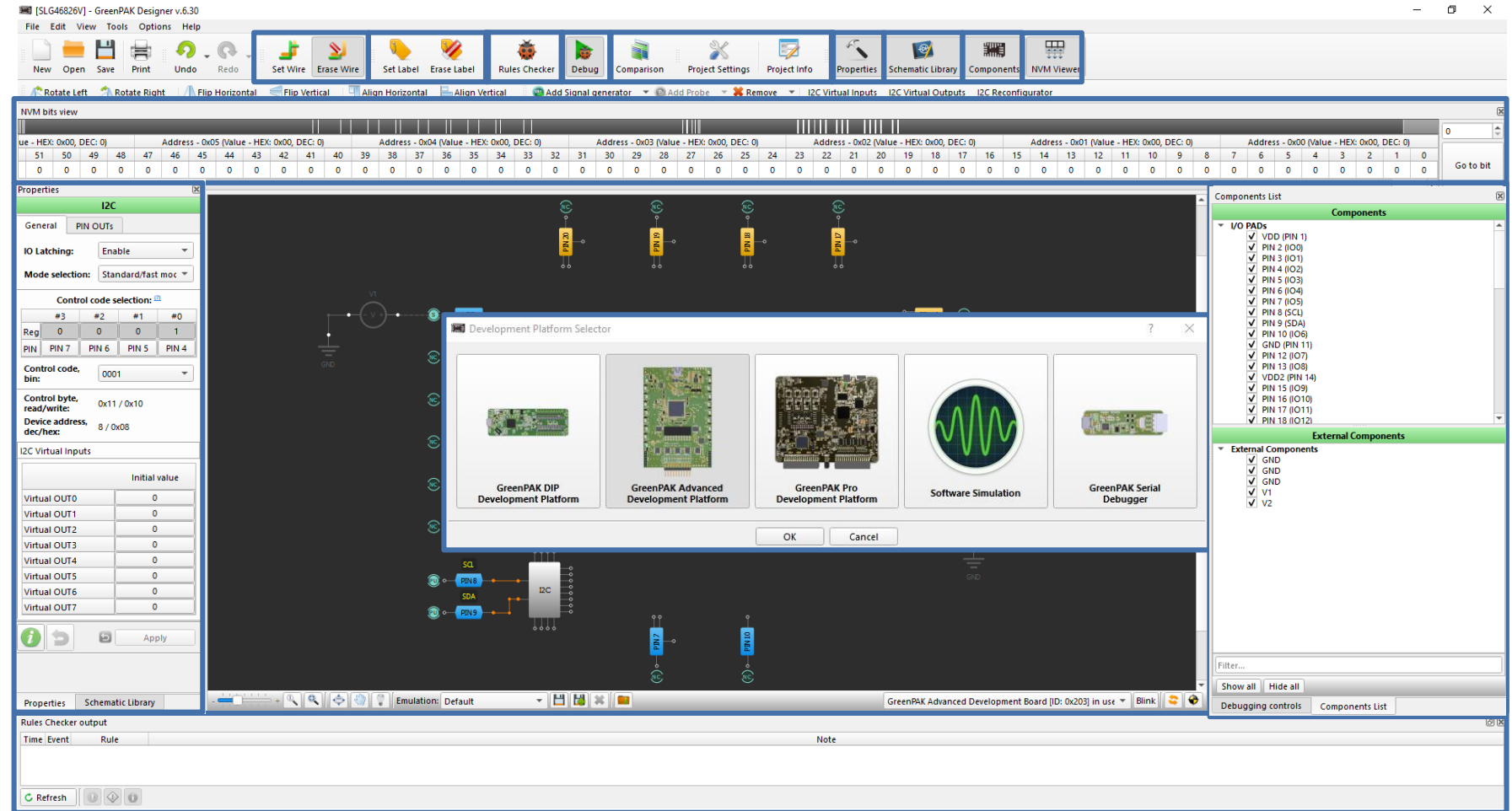
- Welcome: Design Tips, Links to Product Brochures, Application Notes, and Training Videos
- Develop: Table of GreenPAK ICs with their PCB Footprint and Logic Resource Availability
- Demo: List of Common GreenPAK Applications
- Datasheets
- User Guides

# GREENPAK DEVELOPMENT SOFTWARE

## GreenPAK Designer

### Tool Bar

- Set / Erase Wire
- Set / Erase Label
- Rules Checker
- Debug
- Project Settings
- Project Info
- Properties
- Schematic Library
- Components
- NVM Viewer
- Change platform

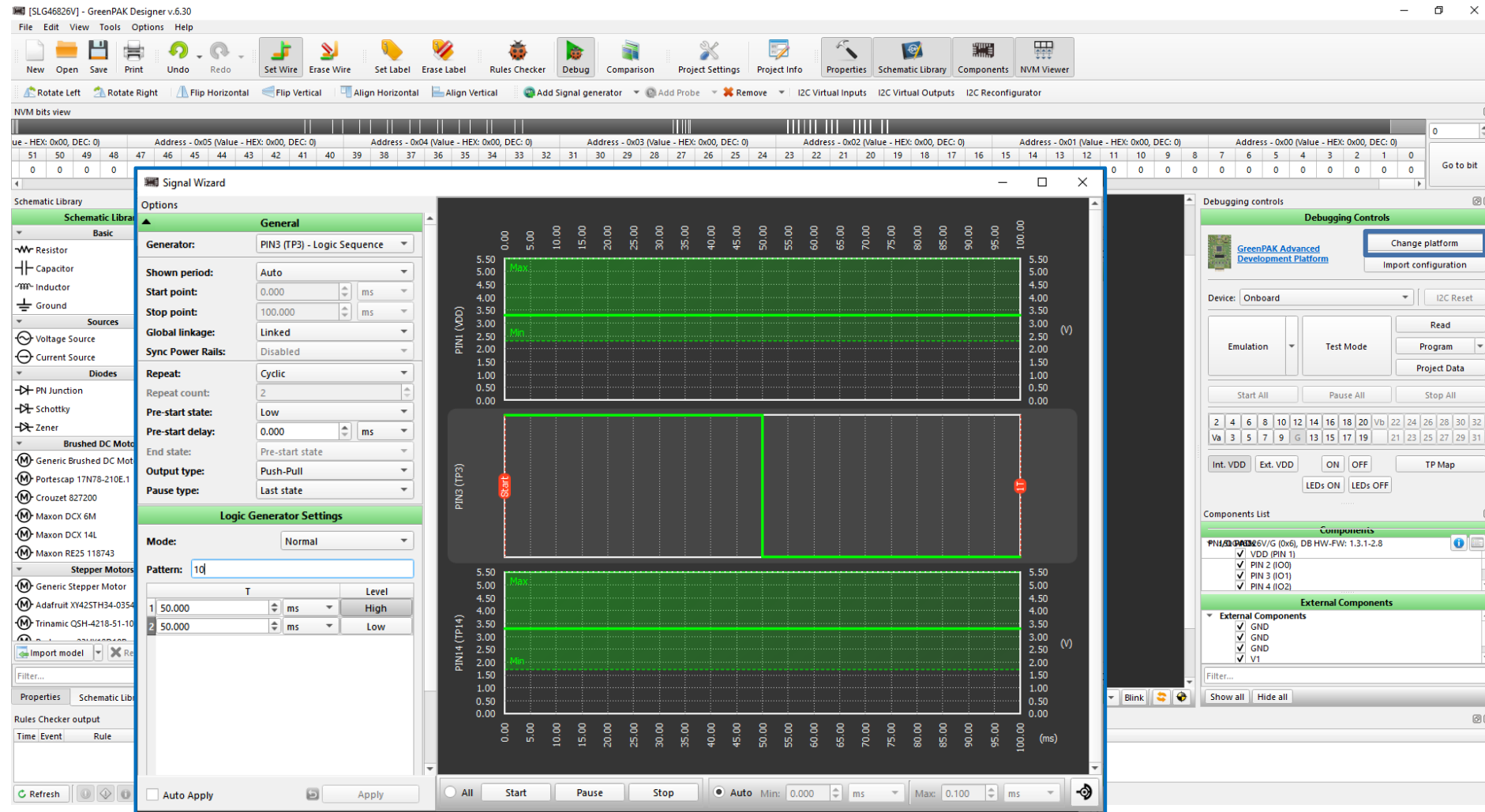


# GREENPAK DEVELOPMENT SOFTWARE

## GreenPAK Designer

### Debug with Hardware

- Logic generator
- Signal generator
- I2C generator

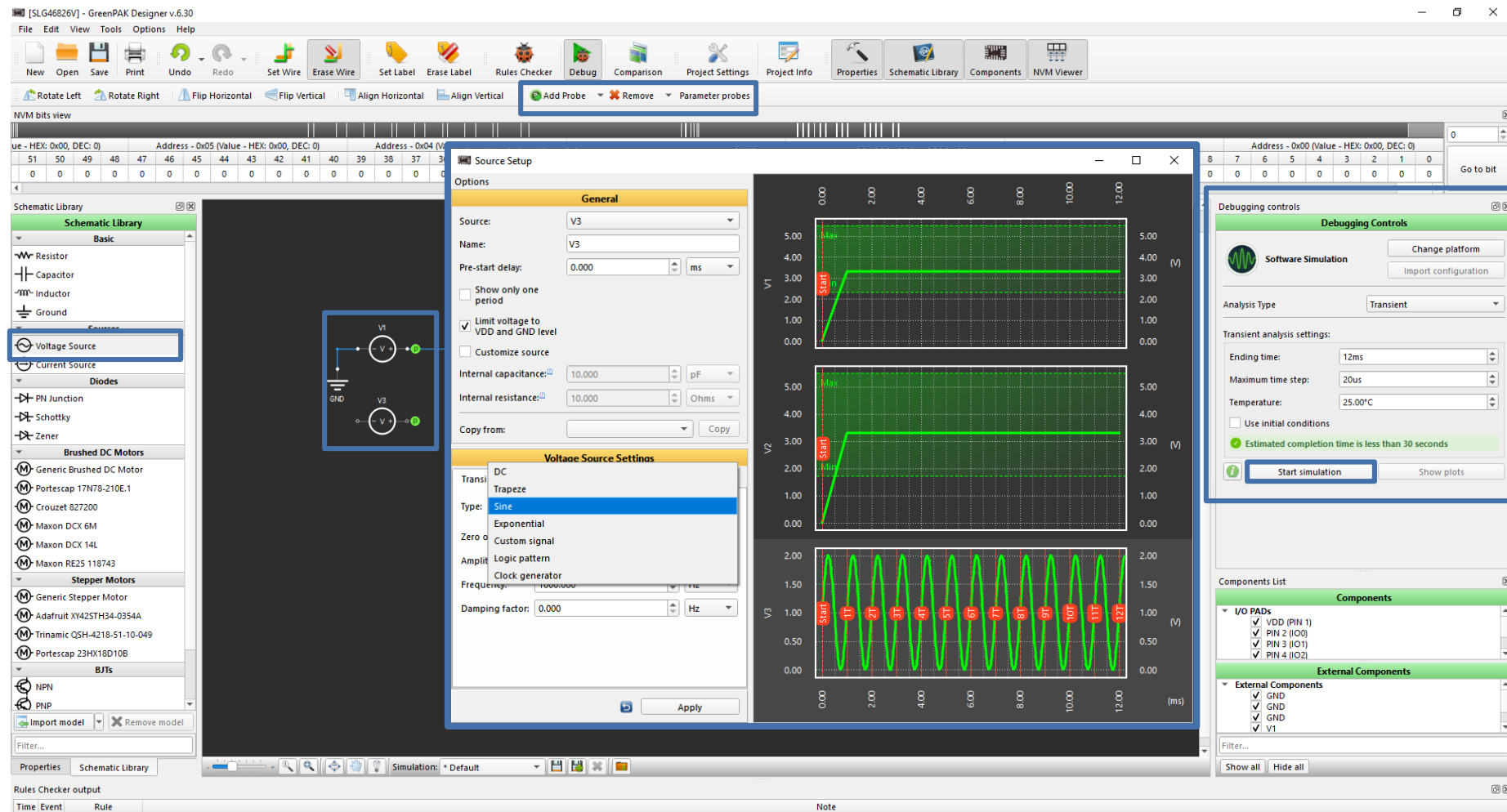


# GREENPAK DEVELOPMENT SOFTWARE

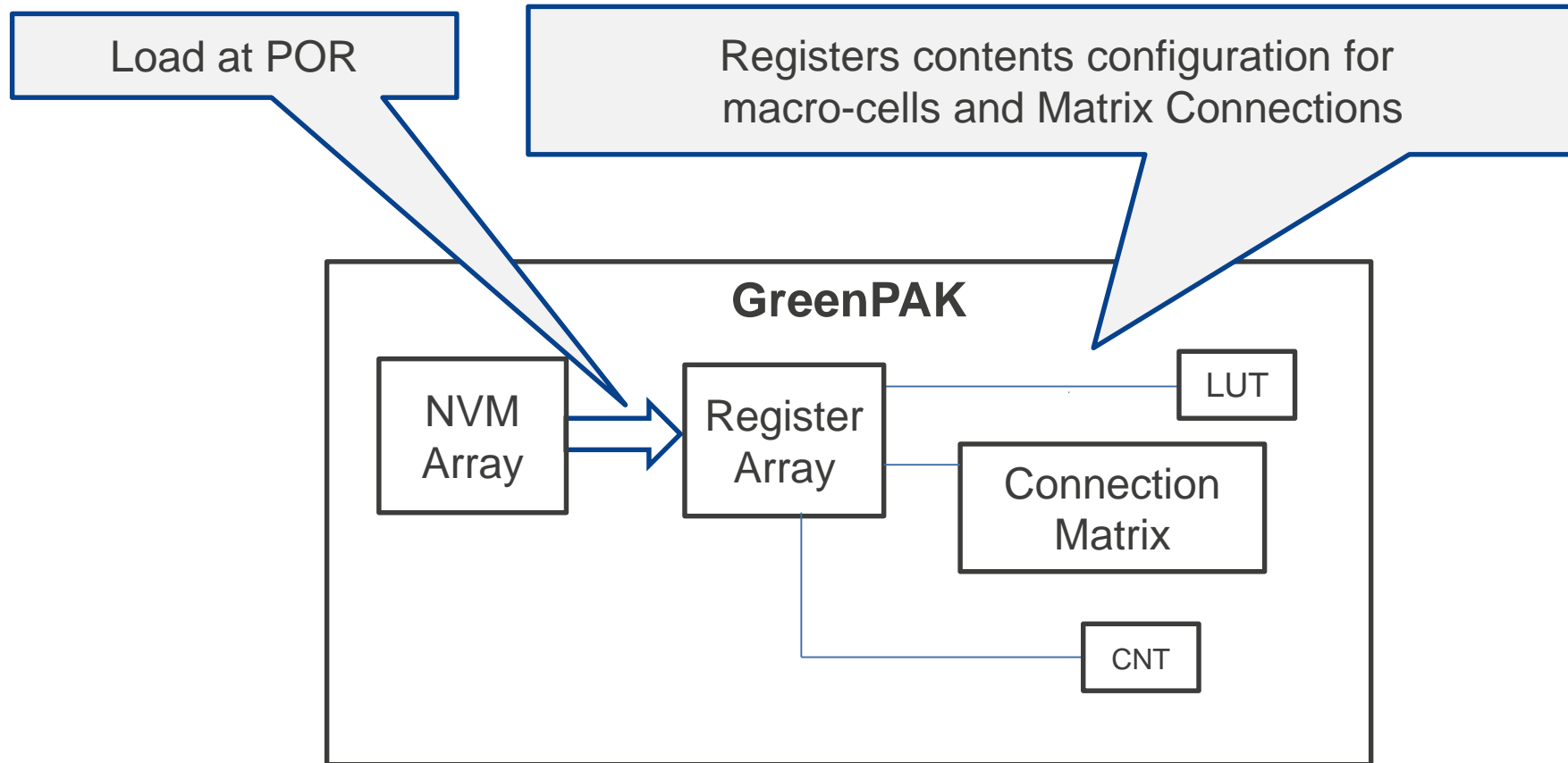
## GreenPAK Designer

### Software Simulation

- Voltage Source
- Add Probe
- Remove
- Debugging Controls

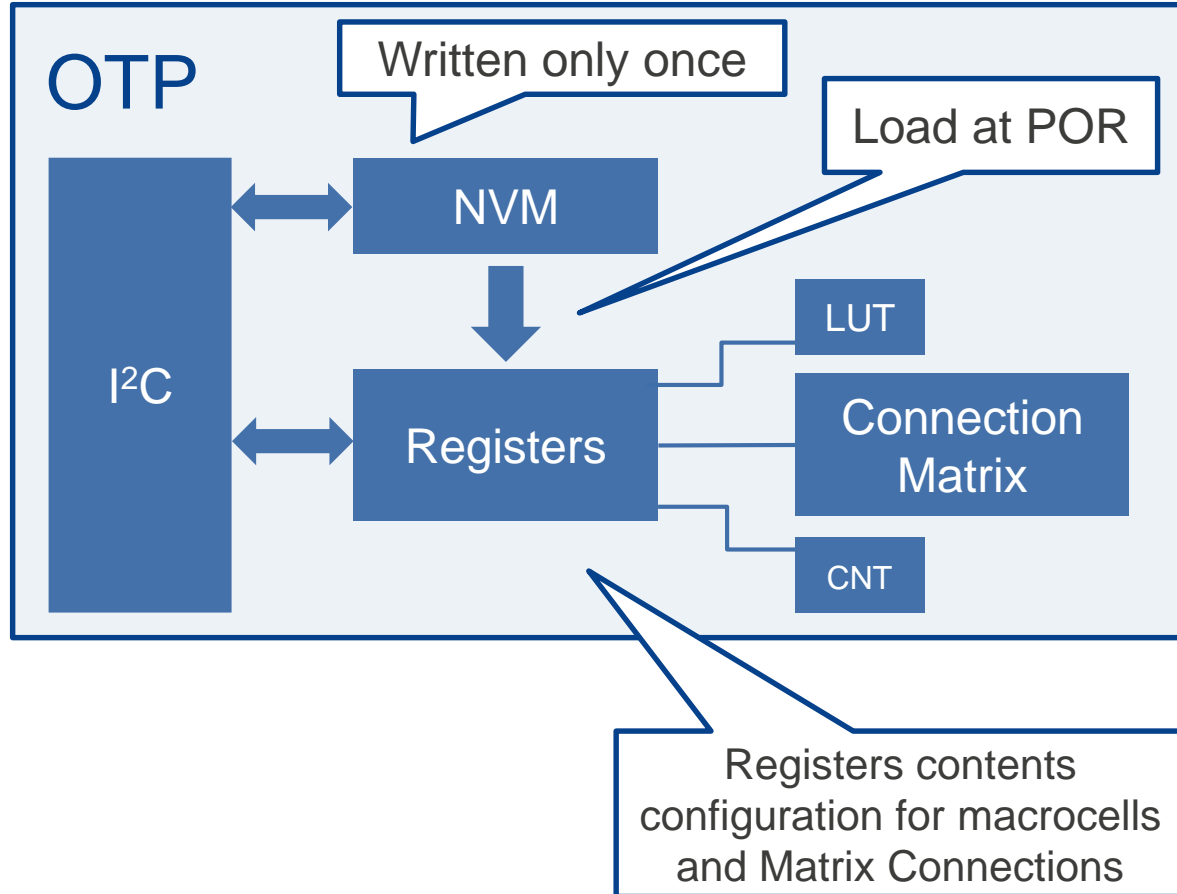


# BASIC GREENPAK ARCHITECTURE



# STRUCTURE OF THE GREENPAK IC MEMORY

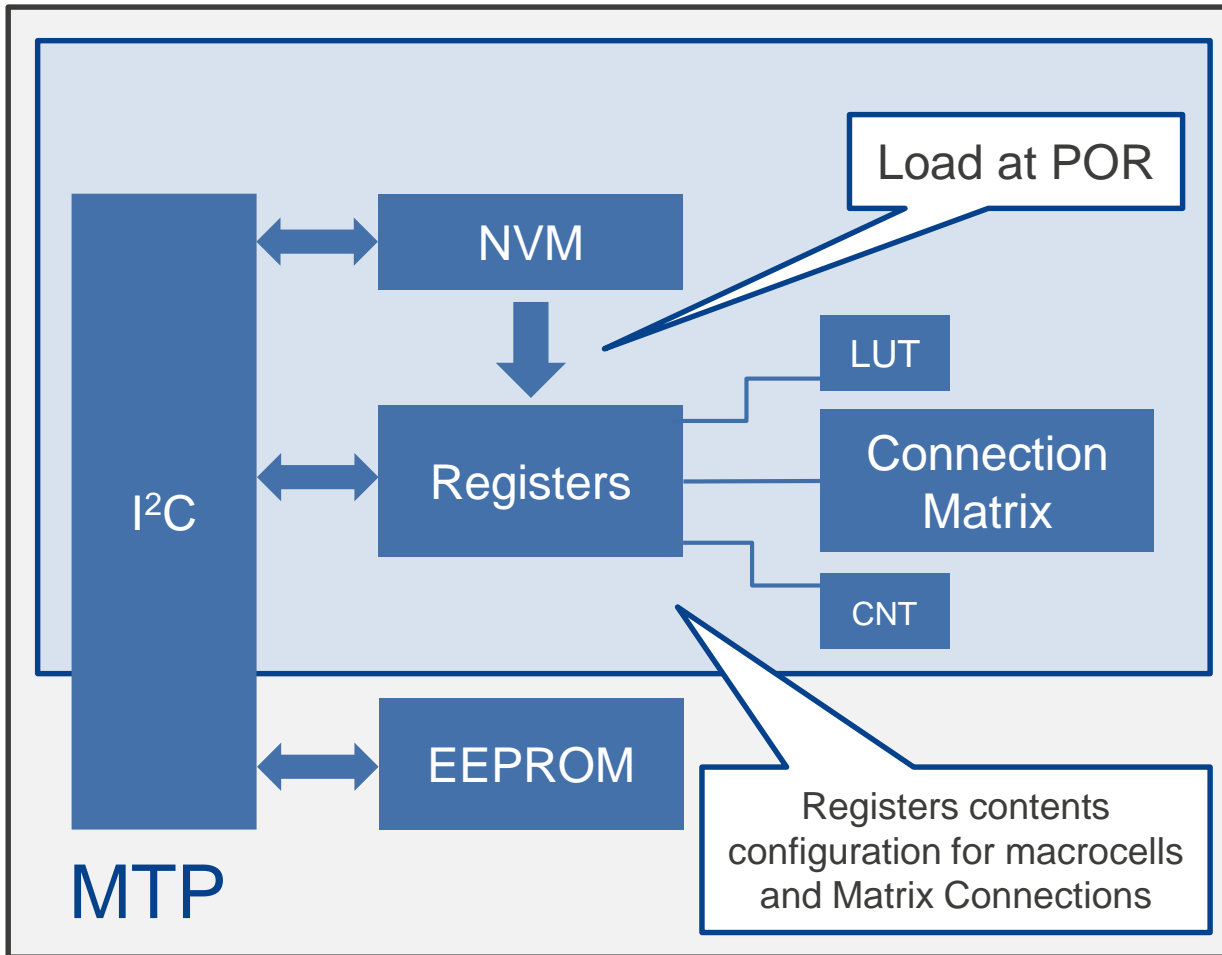
## How IC Memory Works in OTP and MTP/ISP Circuits



- During start NVM memory is emulated to Registers.
- Inside the NVM, there is a specifically dedicated protection page, MTP enables to change security settings.

# STRUCTURE OF THE GREENPAK IC MEMORY

## How IC Memory Works in OTP and MTP/ISP Circuits



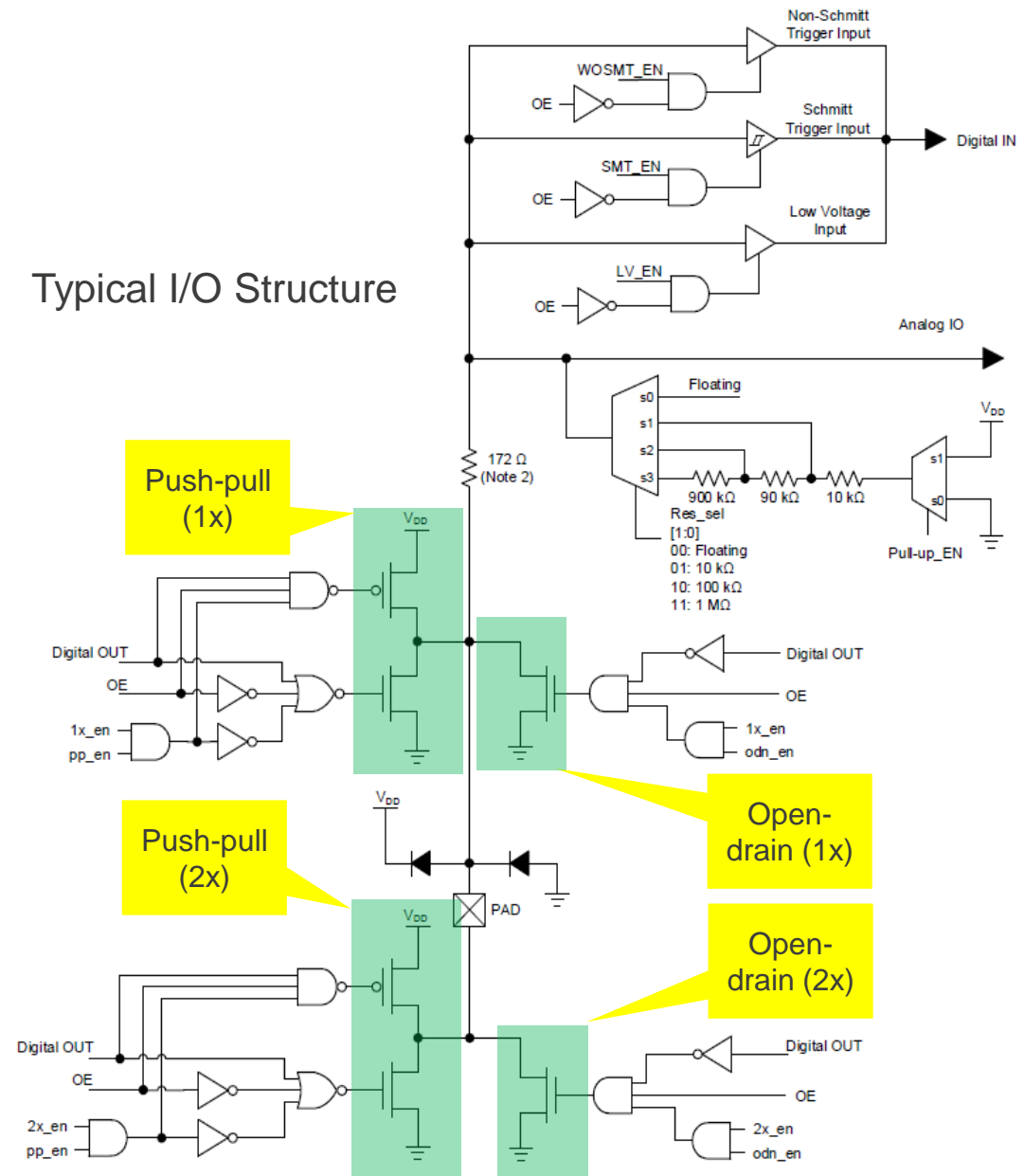
- During start NVM memory is emulated to Registers.
- Inside the NVM, there is a specifically dedicated protection page, MTP enables to change security settings.
- SLG46826 is a representative of MTP devices

# PAD MODES AND ITS USAGE

Most I/Os in GreenPAK devices are very flexible

- Various output modes [Push-pull (1x or 2x), Open-drain (1x or 2x) or Analog-Output]
- Various input modes [Digital-In, Digital-In with Schmitt trigger, Low Voltage Digital-In and Analog-In]
- Some I/Os support Output Enable
- Some I/Os support level shifting

Typical I/O Structure

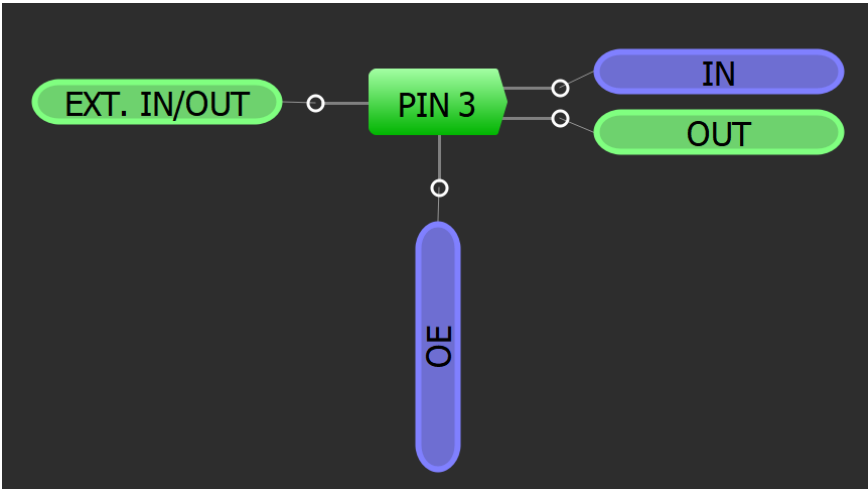


# PAD MODES AND ITS USAGE

## DIGITAL INPUT MODE

Difference between input PINs in different modes:

- 1. Threshold level
- 2. Switching speed(propagation delay)
- 3. Current consumption



Properties ✕

PIN 3 (IO1)

I/O selection: Digital input

Input mode: OE = 0 Digital in without

Output mode: OE = 1 None

Resistor: Floating

Resistor value: Floating

100uA pullup on input: None

Information

Electrical Specifications

|                     | 2.3 V<br>min/max | 3.3 V<br>min/max | 5.0 V<br>min/max |
|---------------------|------------------|------------------|------------------|
| V <sub>IH</sub> (V) | 1.247/-          | 1.693/-          | 2.494/-          |
| V <sub>IL</sub> (V) | -/1.021          | -/1.463          | -/2.227          |
| -                   | -/-              | -/-              | -/-              |
| -                   | -/-              | -/-              | -/-              |
| -                   | -/-              | -/-              | -/-              |
| -                   | -/-              | -/-              | -/-              |

Properties ✕

PIN 3 (IO1)

I/O selection: Digital input

Input mode: OE = 0 Digital in with Sch

Output mode: OE = 1 None

Resistor: Floating

Resistor value: Floating

100uA pullup on input: None

Information

Electrical Specifications

|                     | 2.3 V<br>min/max | 3.3 V<br>min/max | 5.0 V<br>min/max |
|---------------------|------------------|------------------|------------------|
| V <sub>IH</sub> (V) | 1.475/-          | 1.978/-          | 2.884/-          |
| V <sub>IL</sub> (V) | -/0.876          | -/1.356          | -/2.095          |
| -                   | -/-              | -/-              | -/-              |
| -                   | -/-              | -/-              | -/-              |
| -                   | -/-              | -/-              | -/-              |
| -                   | -/-              | -/-              | -/-              |

Properties ✕

PIN 3 (IO1)

I/O selection: Digital input

Input mode: OE = 0 Low voltage digit

Output mode: OE = 1 None

Resistor: Floating

Resistor value: Floating

100uA pullup on input: None

Information

Electrical Specifications

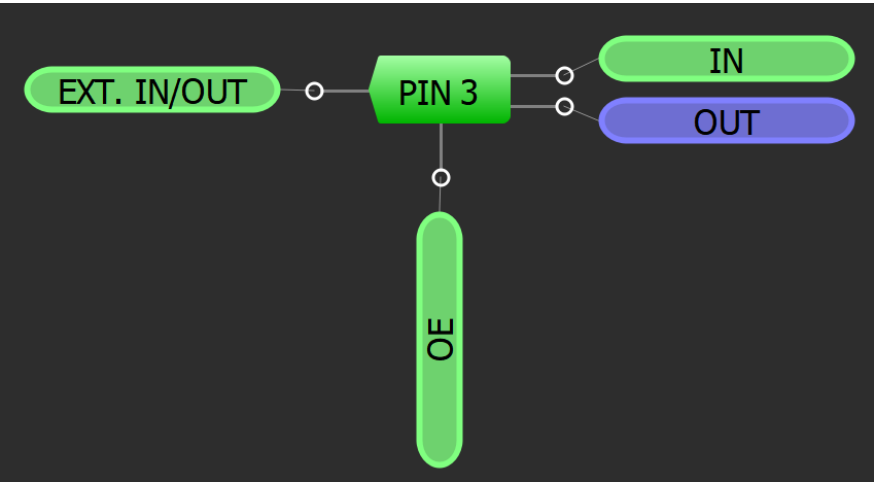
|                     | 2.3 V<br>min/max | 3.3 V<br>min/max | 5.0 V<br>min/max |
|---------------------|------------------|------------------|------------------|
| V <sub>IH</sub> (V) | 0.957/-          | 1.042/-          | 1.127/-          |
| V <sub>IL</sub> (V) | -/0.647          | -/0.722          | -/0.814          |
| -                   | -/-              | -/-              | -/-              |
| -                   | -/-              | -/-              | -/-              |
| -                   | -/-              | -/-              | -/-              |
| -                   | -/-              | -/-              | -/-              |

# PAD MODES AND ITS USAGE

## DIGITAL OUTPUT MODE

Difference between output PINs in different modes:

- 1. Maximum current that PIN can pass
- 2. Possibility to make parallel connection
- 3. Possibility to make Hi-Z state



Properties

PIN 3 (IO1)

I/O selection: Digital output

Input mode: OE = 0 None

Output mode: OE = 1 1x push pull

Resistor: Floating

Resistor value: Floating

100uA pullup on input: None

Information

Electrical Specifications

|           | 2.3 V min/max | 3.3 V min/max | 5.0 V min/max |
|-----------|---------------|---------------|---------------|
| V_OH (V)  | 1.693/-       | 2.703/-       | 4.149/-       |
| V_OL (V)  | -/0.013       | -/0.184       | -/0.243       |
| I_OH (mA) | 1.034/-       | 5.498/-       | 20.007/-      |
| I_OL (mA) | 1.190/-       | 5.358/-       | 7.227/-       |
| -         | -/-           | -/-           | -/-           |
| -         | -/-           | -/-           | -/-           |

Properties

PIN 3 (IO1)

I/O selection: Digital output

Input mode: OE = 0 None

Output mode: OE = 1 1x open drain NM

Resistor: Floating

Resistor value: Floating

100uA pullup on input: None

Information

Electrical Specifications

|           | 2.3 V min/max | 3.3 V min/max | 5.0 V min/max |
|-----------|---------------|---------------|---------------|
| V_OH (V)  | -/0.008       | -/0.093       | -/0.124       |
| I_OL (mA) | 2.384/-       | 10.557/-      | 14.128/-      |
| -         | -/-           | -/-           | -/-           |
| -         | -/-           | -/-           | -/-           |
| -         | -/-           | -/-           | -/-           |
| -         | -/-           | -/-           | -/-           |

Properties

PIN 3 (IO1)

I/O selection: Digital output

Input mode: OE = 0 None

Output mode: OE = 1 1x 3-State Output

Resistor: Floating

Resistor value: Floating

100uA pullup on input: None

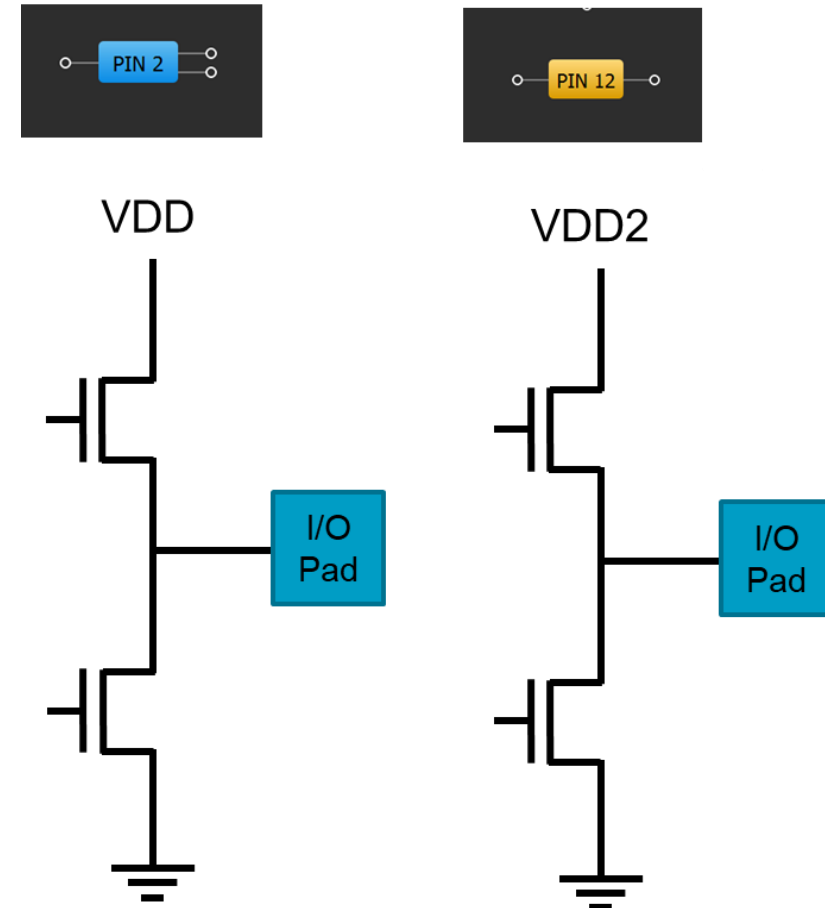
Information

Electrical Specifications

|           | 2.3 V min/max | 3.3 V min/max | 5.0 V min/max |
|-----------|---------------|---------------|---------------|
| V_OH (V)  | 1.693/-       | 2.703/-       | 4.149/-       |
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| I_OH (mA) | 1.034/-       | 5.498/-       | 20.007/-      |
| I_OL (mA) | 1.190/-       | 5.358/-       | 7.227/-       |
| -         | -/-           | -/-           | -/-           |
| -         | -/-           | -/-           | -/-           |

# LEVEL SHIFTING

- GreenPAK devices with VDD2 have some I/O pins tied to VDD2
  - You can see this by the color of the Pin icon
- This makes level shifting applications very easy to implement
- Some of the devices have VDD2

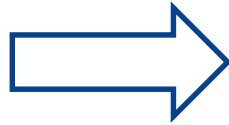


# COMBINATIONAL LOGIC. STANDARD AND CUSTOMIZED MICROCELL

## CUSTOMIZED LUT BASED

Таблиця з практичної роботи №2 легко формується в SLG46826 (4bit LUT) повторюючи функціонал логічної схеми

|   |   |   |   | Отримане число ↓ |  |
|---|---|---|---|------------------|--|
| A | B | C | D | OUT              | Combination                                |
| 0 | 0 | 0 | 0 | 0                | -  |
| 0 | 0 | 0 | 1 | 0                | -  |
| 0 | 0 | 1 | 0 | 0                | -  |
| 0 | 0 | 1 | 1 | 1                | $\overline{A} \overline{B} C D$            |
| 0 | 1 | 0 | 0 | 1                | $\overline{A} B \overline{C} \overline{D}$ |
| 0 | 1 | 0 | 1 | 0                | -  |
| 0 | 1 | 1 | 0 | 1                | $\overline{A} B C \overline{D}$            |
| 0 | 1 | 1 | 1 | 1                | $\overline{A} B C D$                       |
| 1 | 0 | 0 | 0 | 1                | $A \overline{B} \overline{C} \overline{D}$ |
| 1 | 0 | 0 | 1 | 1                | $A \overline{B} \overline{C} D$            |
| 1 | 0 | 1 | 0 | 0                | -  |
| 1 | 0 | 1 | 1 | 1                | $A \overline{B} C D$                       |
| 1 | 1 | 0 | 0 | 1                | $A B \overline{C} \overline{D}$            |
| 1 | 1 | 0 | 1 | 1                | $A B \overline{C} D$                       |
| 1 | 1 | 1 | 0 | 0                | -  |
| 1 | 1 | 1 | 1 | 0                | -  |



4-bit LUT0/CNT2/DLY2/FSM0

Type: LUT

| IN3 | IN2 | IN1 | IN0 | OUT |
|-----|-----|-----|-----|-----|
| 0   | 0   | 0   | 0   | 0   |
| 0   | 0   | 0   | 1   | 0   |
| 0   | 0   | 1   | 0   | 0   |
| 0   | 0   | 1   | 1   | 1   |
| 0   | 1   | 0   | 0   | 1   |
| 0   | 1   | 0   | 1   | 0   |
| 0   | 1   | 1   | 0   | 1   |
| 0   | 1   | 1   | 1   | 1   |
| 1   | 0   | 0   | 0   | 1   |
| 1   | 0   | 0   | 1   | 1   |
| 1   | 0   | 1   | 0   | 0   |
| 1   | 0   | 1   | 1   | 1   |
| 1   | 1   | 0   | 0   | 1   |
| 1   | 1   | 0   | 1   | 1   |
| 1   | 1   | 1   | 0   | 0   |
| 1   | 1   | 1   | 1   | 0   |

Standard gates
 

All to 0

Defined by user

All to 1

☐ Regular shape

Invert

i

↺

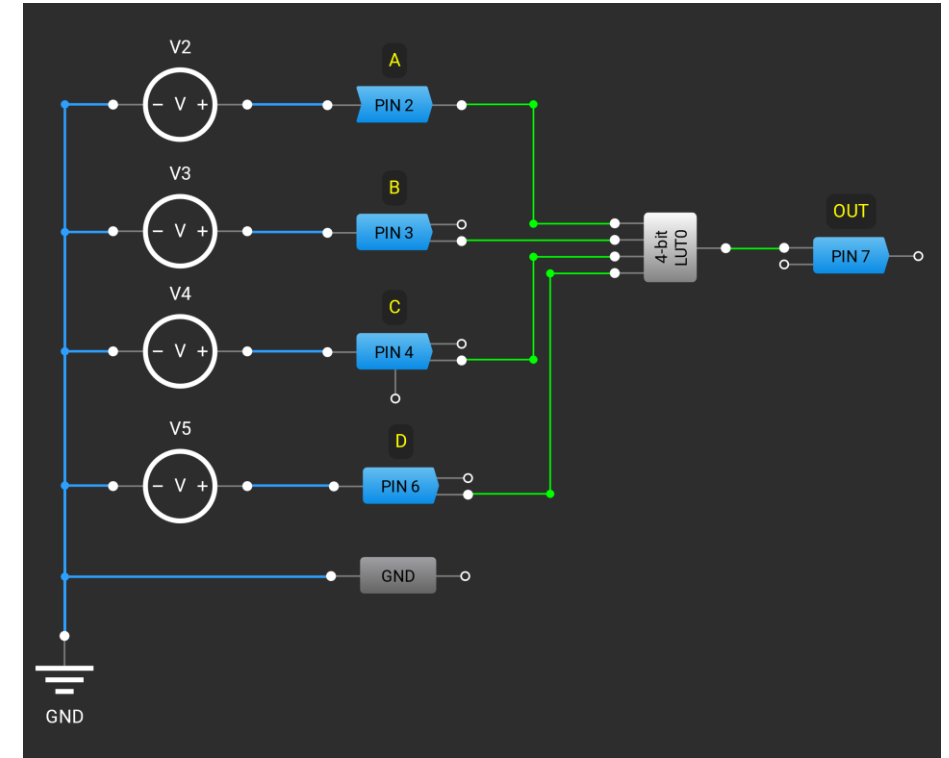
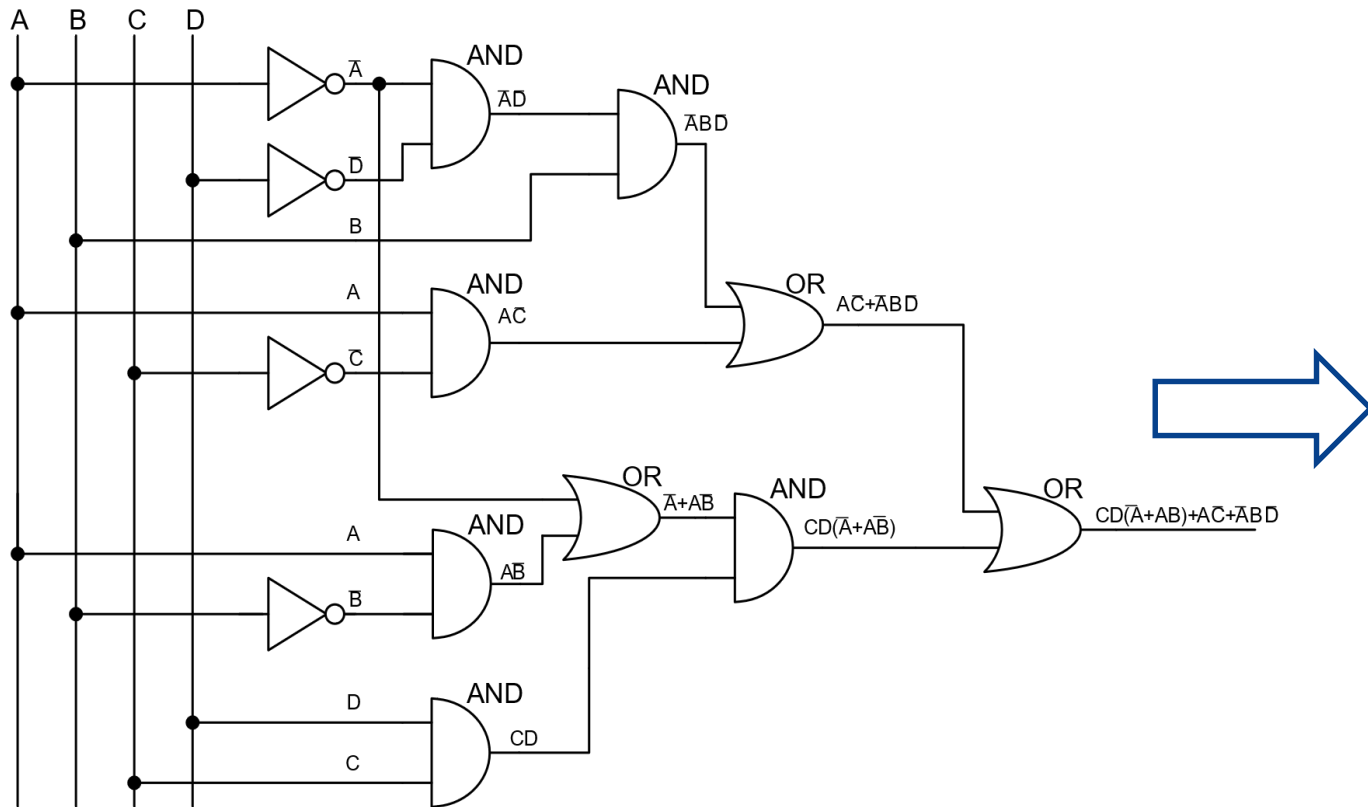
↻

Apply

# COMBINATIONAL LOGIC. STANDARD AND CUSTOMIZED MICROCELL

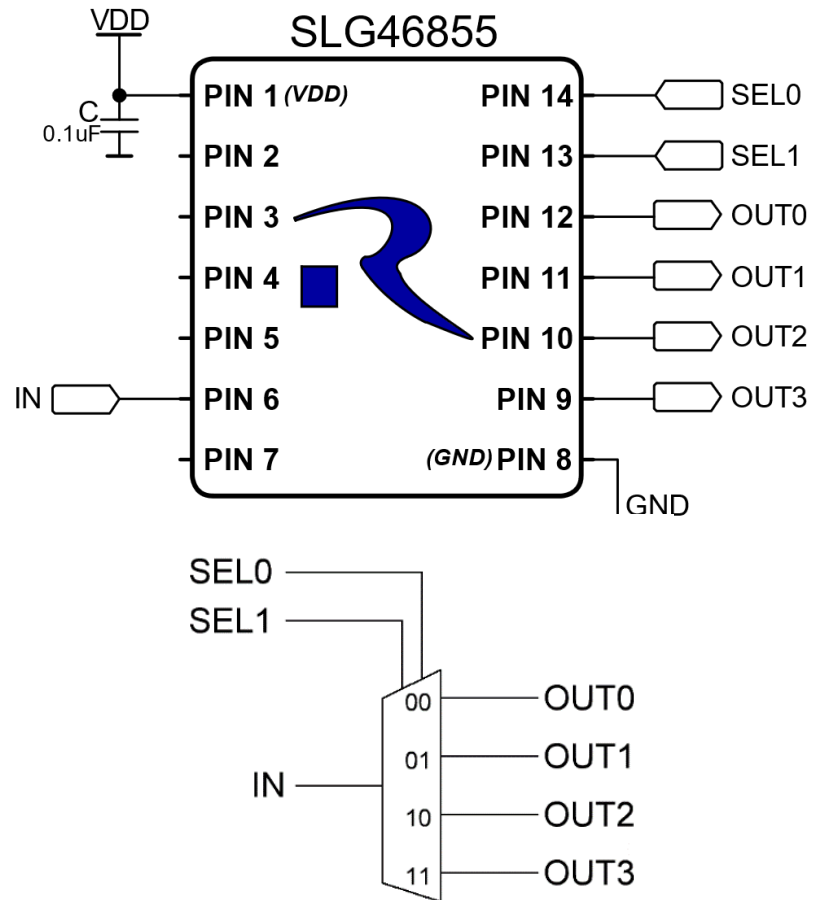
## CUSTOMIZED LUT BASED

Відтак логічна функція, котру реалізовували 4 мікросхеми (1x7404 (NOT), 2x7408 (AND), 1x7432 (OR))  
тепер

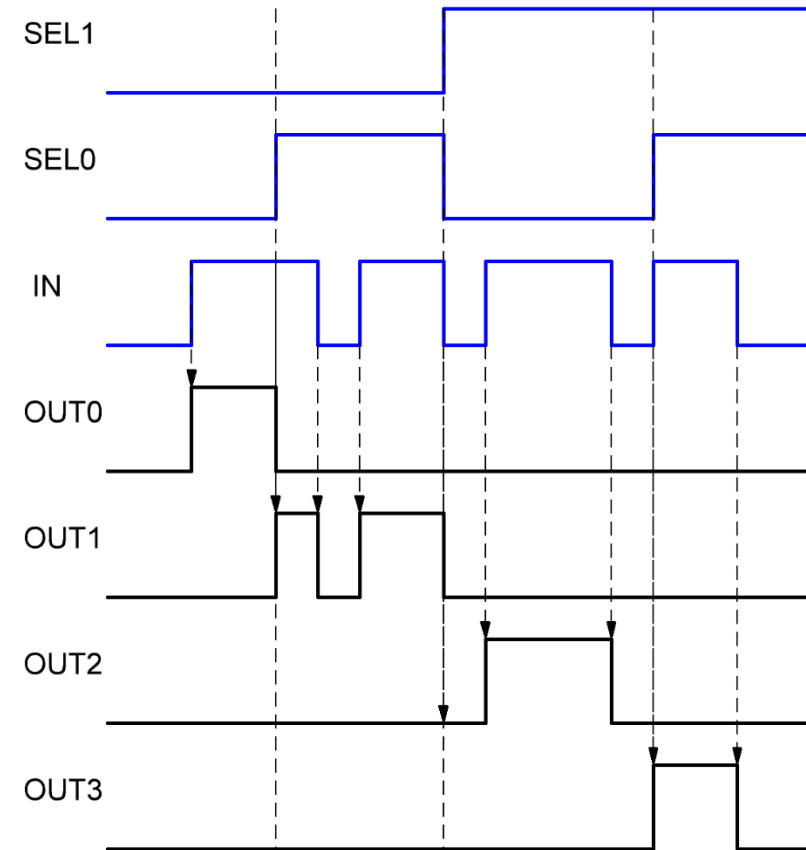


# GREENPAK APPLICATION OPPORTUNITIES. HANDS-ON

## Demultiplexer (DEMUX)

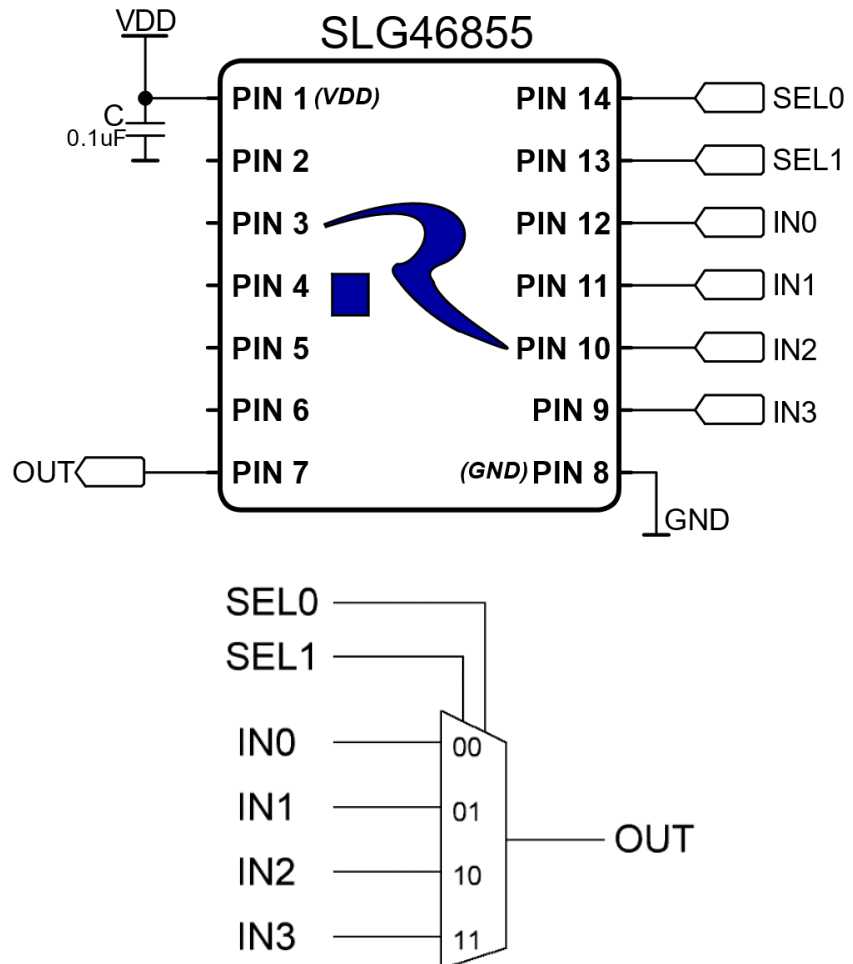


- Chosen by SELx code output copies input

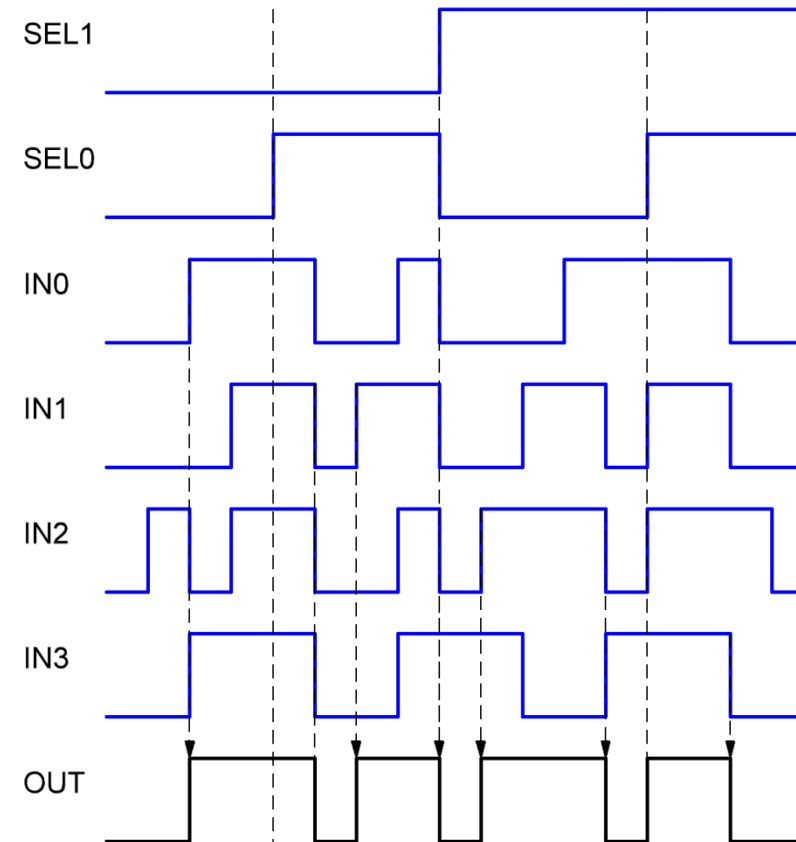


# GREENPAK APPLICATION OPPORTUNITIES. HANDS-ON

## Multiplexer (MUX)



- Output copies one of inputs depending on the SELx code



# COMBINATIONAL LOGIC. STANDARD AND CUSTOMIZED MICROCELL

## STANDARD LUTS (LOOK-UP TABLES)

Properties

3-bit LUT0

| IN3 | IN2 | IN1 | IN0 | OUT |
|-----|-----|-----|-----|-----|
| 0   | 0   | 0   | 0   | 0   |
| 0   | 0   | 0   | 1   | 1   |
| 0   | 0   | 1   | 0   | 0   |
| 0   | 0   | 1   | 1   | 1   |
| 0   | 1   | 0   | 0   | 0   |
| 0   | 1   | 0   | 1   | 1   |
| 0   | 1   | 1   | 0   | 0   |
| 0   | 1   | 1   | 1   | 1   |
| 1   | 0   | 0   | 0   | 0   |
| 1   | 0   | 0   | 1   | 0   |
| 1   | 0   | 1   | 0   | 0   |
| 1   | 0   | 1   | 1   | 0   |
| 1   | 1   | 0   | 0   | 0   |
| 1   | 1   | 0   | 1   | 0   |
| 1   | 1   | 1   | 0   | 0   |
| 1   | 1   | 1   | 1   | 0   |

Standard gates

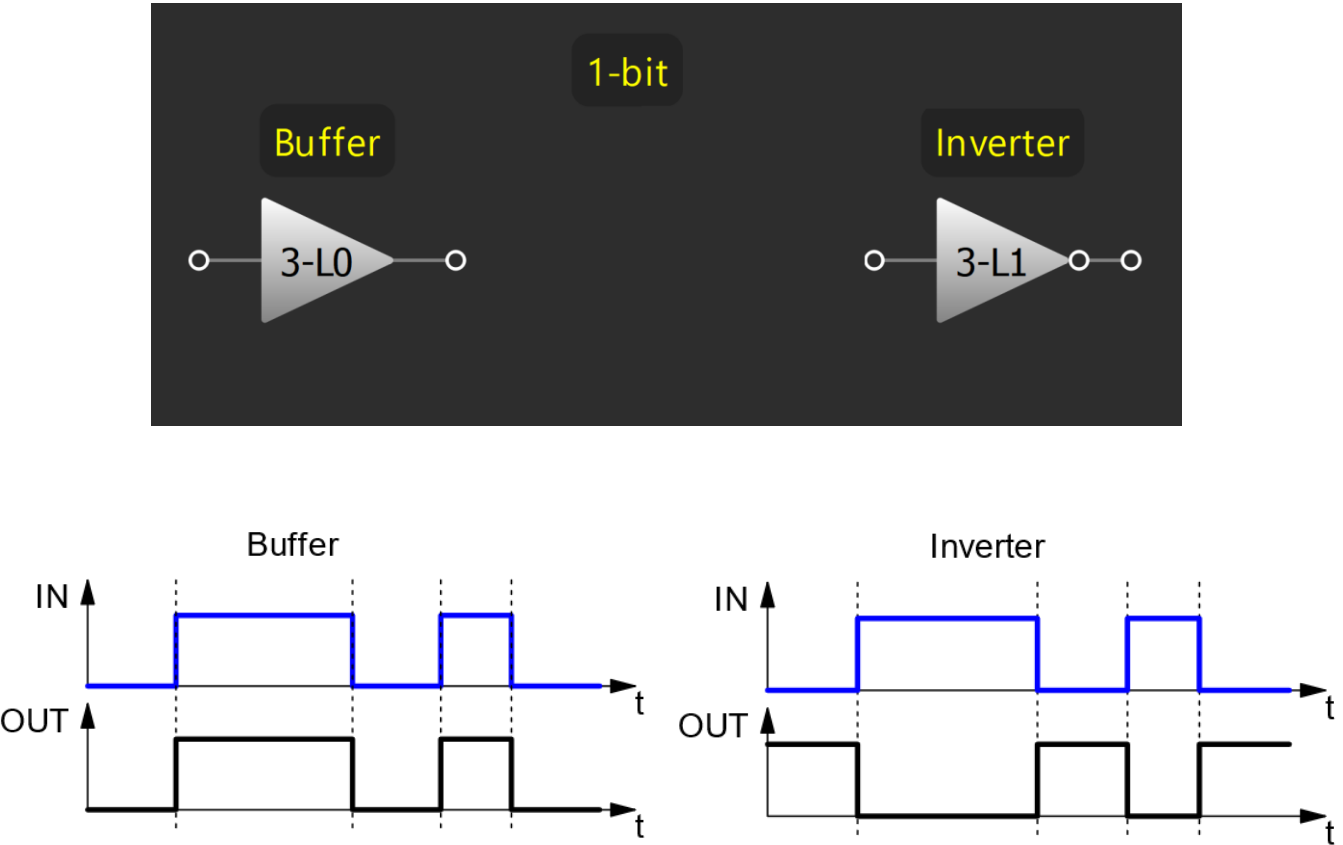
Buffer

☐ Regular shape

All to 0

All to 1

Invert



Properties

3-bit LUT1

| IN3 | IN2 | IN1 | IN0 | OUT |
|-----|-----|-----|-----|-----|
| 0   | 0   | 0   | 0   | 1   |
| 0   | 0   | 0   | 1   | 0   |
| 0   | 0   | 1   | 0   | 1   |
| 0   | 0   | 1   | 1   | 0   |
| 0   | 1   | 0   | 0   | 1   |
| 0   | 1   | 0   | 1   | 0   |
| 0   | 1   | 1   | 0   | 1   |
| 0   | 1   | 1   | 1   | 0   |
| 1   | 0   | 0   | 0   | 0   |
| 1   | 0   | 0   | 1   | 0   |
| 1   | 0   | 1   | 0   | 0   |
| 1   | 0   | 1   | 1   | 0   |
| 1   | 1   | 0   | 0   | 0   |
| 1   | 1   | 0   | 1   | 0   |
| 1   | 1   | 1   | 0   | 0   |
| 1   | 1   | 1   | 1   | 0   |

Standard gates

Inverter

☐ Regular shape

All to 0

All to 1

Invert

# COMBINATIONAL LOGIC. STANDARD AND CUSTOMIZED MICROCELL

## STANDARD LUTS (LOOK-UP TABLES)

Properties

2-bit LUT0

| IN3 | IN2 | IN1 | IN0 | OUT |
|-----|-----|-----|-----|-----|
| 0   | 0   | 0   | 0   | 0   |
| 0   | 0   | 0   | 1   | 0   |
| 0   | 0   | 1   | 0   | 0   |
| 0   | 0   | 1   | 1   | 1   |
| 0   | 1   | 0   | 0   | 0   |
| 0   | 1   | 0   | 1   | 0   |
| 0   | 1   | 1   | 0   | 0   |
| 0   | 1   | 1   | 1   | 0   |
| 1   | 0   | 0   | 0   | 0   |
| 1   | 0   | 0   | 1   | 0   |
| 1   | 0   | 1   | 0   | 0   |
| 1   | 0   | 1   | 1   | 0   |
| 1   | 1   | 0   | 0   | 0   |
| 1   | 1   | 0   | 1   | 0   |
| 1   | 1   | 1   | 0   | 0   |
| 1   | 1   | 1   | 1   | 0   |

Standard gates

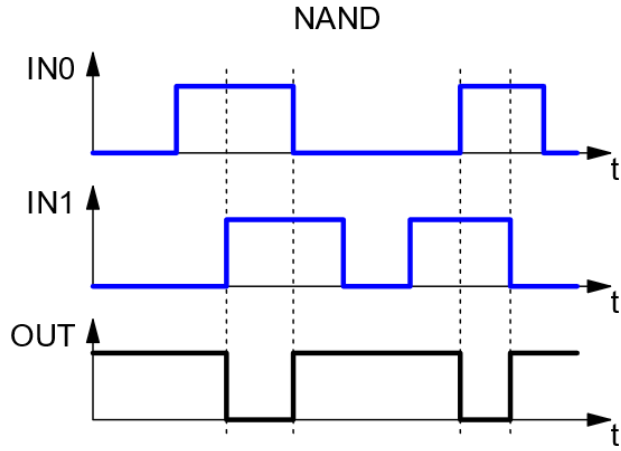
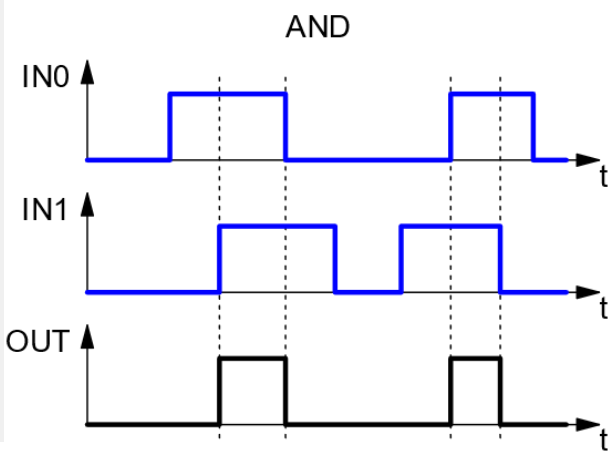
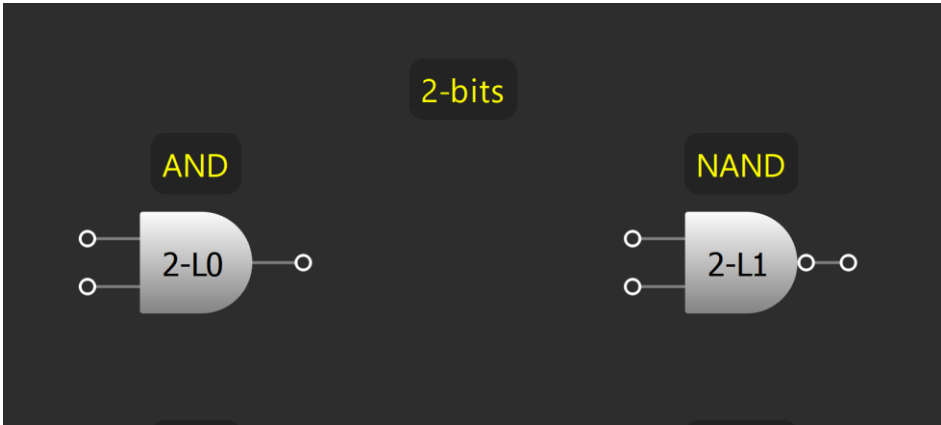
AND

☐ Regular shape

All to 0

All to 1

Invert



Properties

2-bit LUT1

| IN3 | IN2 | IN1 | IN0 | OUT |
|-----|-----|-----|-----|-----|
| 0   | 0   | 0   | 0   | 1   |
| 0   | 0   | 0   | 1   | 1   |
| 0   | 0   | 1   | 0   | 1   |
| 0   | 0   | 1   | 1   | 0   |
| 0   | 1   | 0   | 0   | 0   |
| 0   | 1   | 0   | 1   | 0   |
| 0   | 1   | 1   | 0   | 0   |
| 0   | 1   | 1   | 1   | 0   |
| 1   | 0   | 0   | 0   | 0   |
| 1   | 0   | 0   | 1   | 0   |
| 1   | 0   | 1   | 0   | 0   |
| 1   | 0   | 1   | 1   | 0   |
| 1   | 1   | 0   | 0   | 0   |
| 1   | 1   | 0   | 1   | 0   |
| 1   | 1   | 1   | 0   | 0   |
| 1   | 1   | 1   | 1   | 0   |

Standard gates

NAND

☐ Regular shape

All to 0

All to 1

Invert

# COMBINATIONAL LOGIC. STANDARD AND CUSTOMIZED MICROCELL

## STANDARD LUTS (LOOK-UP TABLES)

Properties

3-bit LUT2

| IN3 | IN2 | IN1 | IN0 | OUT |
|-----|-----|-----|-----|-----|
| 0   | 0   | 0   | 0   | 0   |
| 0   | 0   | 0   | 1   | 0   |
| 0   | 0   | 1   | 0   | 0   |
| 0   | 0   | 1   | 1   | 0   |
| 0   | 1   | 0   | 0   | 0   |
| 0   | 1   | 0   | 1   | 0   |
| 0   | 1   | 1   | 0   | 0   |
| 0   | 1   | 1   | 1   | 1   |
| 1   | 0   | 0   | 0   | 0   |
| 1   | 0   | 0   | 1   | 0   |
| 1   | 0   | 1   | 0   | 0   |
| 1   | 0   | 1   | 1   | 0   |
| 1   | 1   | 0   | 0   | 0   |
| 1   | 1   | 0   | 1   | 0   |
| 1   | 1   | 1   | 0   | 0   |
| 1   | 1   | 1   | 1   | 0   |

Standard gates

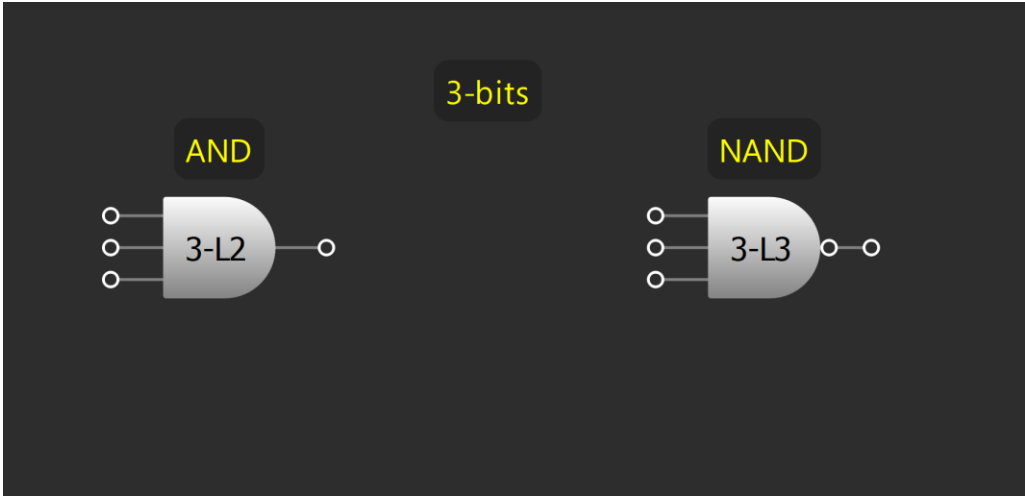
AND

☐ Regular shape

All to 0

All to 1

Invert



Properties

3-bit LUT3

| IN3 | IN2 | IN1 | IN0 | OUT |
|-----|-----|-----|-----|-----|
| 0   | 0   | 0   | 0   | 1   |
| 0   | 0   | 0   | 1   | 1   |
| 0   | 0   | 1   | 0   | 1   |
| 0   | 0   | 1   | 1   | 1   |
| 0   | 1   | 0   | 0   | 1   |
| 0   | 1   | 0   | 1   | 1   |
| 0   | 1   | 1   | 0   | 1   |
| 0   | 1   | 1   | 1   | 0   |
| 1   | 0   | 0   | 0   | 0   |
| 1   | 0   | 0   | 1   | 0   |
| 1   | 0   | 1   | 0   | 0   |
| 1   | 0   | 1   | 1   | 0   |
| 1   | 1   | 0   | 0   | 0   |
| 1   | 1   | 0   | 1   | 0   |
| 1   | 1   | 1   | 0   | 0   |
| 1   | 1   | 1   | 1   | 0   |

Standard gates

NAND

☐ Regular shape

All to 0

All to 1

Invert

# COMBINATIONAL LOGIC. STANDARD AND CUSTOMIZED MICROCELL

## STANDARD LUTS (LOOK-UP TABLES)

Properties

2-bit LUT2

| IN3 | IN2 | IN1 | IN0 | OUT |
|-----|-----|-----|-----|-----|
| 0   | 0   | 0   | 0   | 0   |
| 0   | 0   | 0   | 1   | 1   |
| 0   | 0   | 1   | 0   | 1   |
| 0   | 0   | 1   | 1   | 1   |
| 0   | 1   | 0   | 0   | 0   |
| 0   | 1   | 0   | 1   | 0   |
| 0   | 1   | 1   | 0   | 0   |
| 0   | 1   | 1   | 1   | 0   |
| 1   | 0   | 0   | 0   | 0   |
| 1   | 0   | 0   | 1   | 0   |
| 1   | 0   | 1   | 0   | 0   |
| 1   | 0   | 1   | 1   | 0   |
| 1   | 1   | 0   | 0   | 0   |
| 1   | 1   | 0   | 1   | 0   |
| 1   | 1   | 1   | 0   | 0   |
| 1   | 1   | 1   | 1   | 0   |

Standard gates

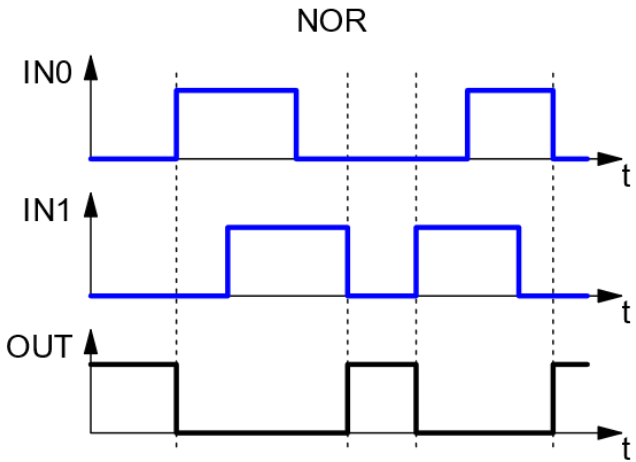
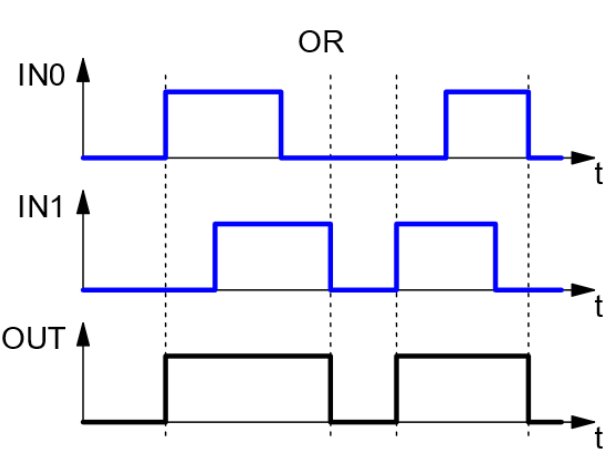
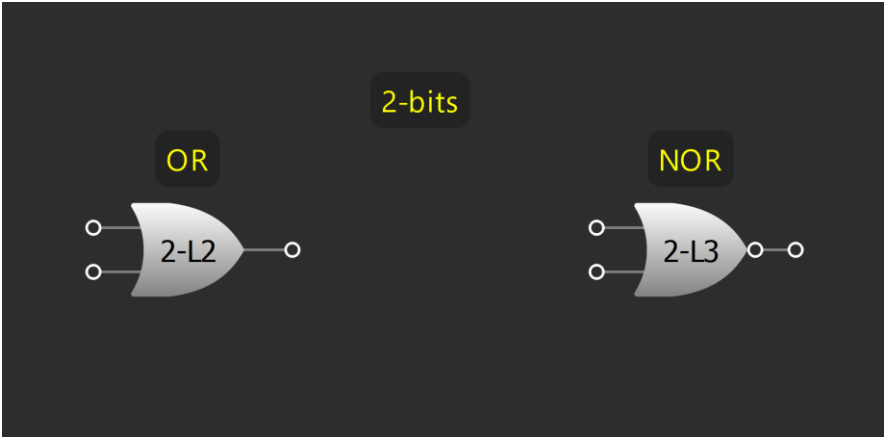
OR

☐ Regular shape

All to 0

All to 1

Invert



Properties

2-bit LUT3

| IN3 | IN2 | IN1 | IN0 | OUT |
|-----|-----|-----|-----|-----|
| 0   | 0   | 0   | 0   | 1   |
| 0   | 0   | 0   | 1   | 0   |
| 0   | 0   | 1   | 0   | 0   |
| 0   | 0   | 1   | 1   | 0   |
| 0   | 1   | 0   | 0   | 0   |
| 0   | 1   | 0   | 1   | 0   |
| 0   | 1   | 1   | 0   | 0   |
| 0   | 1   | 1   | 1   | 0   |
| 1   | 0   | 0   | 0   | 0   |
| 1   | 0   | 0   | 1   | 0   |
| 1   | 0   | 1   | 0   | 0   |
| 1   | 0   | 1   | 1   | 0   |
| 1   | 1   | 0   | 0   | 0   |
| 1   | 1   | 0   | 1   | 0   |
| 1   | 1   | 1   | 0   | 0   |
| 1   | 1   | 1   | 1   | 0   |

Standard gates

NOR

☐ Regular shape

All to 0

All to 1

Invert

# COMBINATIONAL LOGIC. STANDARD AND CUSTOMIZED MICROCELL

## STANDARD LUTS (LOOK-UP TABLES)

Properties

3-bit LUT4

| IN3 | IN2 | IN1 | IN0 | OUT |
|-----|-----|-----|-----|-----|
| 0   | 0   | 0   | 0   | 0   |
| 0   | 0   | 0   | 1   | 1   |
| 0   | 0   | 1   | 0   | 1   |
| 0   | 0   | 1   | 1   | 1   |
| 0   | 1   | 0   | 0   | 1   |
| 0   | 1   | 0   | 1   | 1   |
| 0   | 1   | 1   | 0   | 1   |
| 0   | 1   | 1   | 1   | 1   |
| 1   | 0   | 0   | 0   | 0   |
| 1   | 0   | 0   | 1   | 0   |
| 1   | 0   | 1   | 0   | 0   |
| 1   | 0   | 1   | 1   | 0   |
| 1   | 1   | 0   | 0   | 0   |
| 1   | 1   | 0   | 1   | 0   |
| 1   | 1   | 1   | 0   | 0   |
| 1   | 1   | 1   | 1   | 0   |

Standard gates

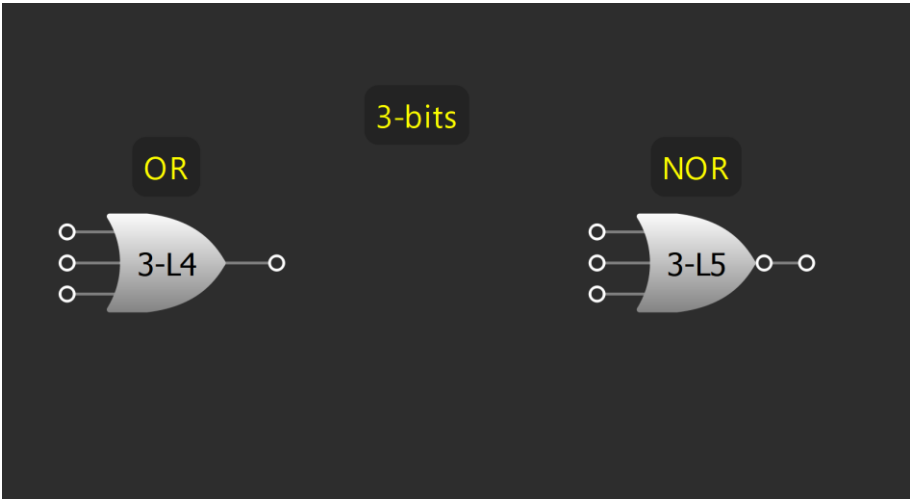
OR

☐ Regular shape

All to 0

All to 1

Invert



Properties

3-bit LUT5

| IN3 | IN2 | IN1 | IN0 | OUT |
|-----|-----|-----|-----|-----|
| 0   | 0   | 0   | 0   | 1   |
| 0   | 0   | 0   | 1   | 0   |
| 0   | 0   | 1   | 0   | 0   |
| 0   | 0   | 1   | 1   | 0   |
| 0   | 1   | 0   | 0   | 0   |
| 0   | 1   | 0   | 1   | 0   |
| 0   | 1   | 1   | 0   | 0   |
| 0   | 1   | 1   | 1   | 0   |
| 1   | 0   | 0   | 0   | 0   |
| 1   | 0   | 0   | 1   | 0   |
| 1   | 0   | 1   | 0   | 0   |
| 1   | 0   | 1   | 1   | 0   |
| 1   | 1   | 0   | 0   | 0   |
| 1   | 1   | 0   | 1   | 0   |
| 1   | 1   | 1   | 0   | 0   |
| 1   | 1   | 1   | 1   | 0   |

Standard gates

NOR

☐ Regular shape

All to 0

All to 1

Invert

# COMBINATIONAL LOGIC. STANDARD AND CUSTOMIZED MICROCELL

## STANDARD LUTS (LOOK-UP TABLES)

Properties

2-bit LUT4

| IN3 | IN2 | IN1 | IN0 | OUT |
|-----|-----|-----|-----|-----|
| 0   | 0   | 0   | 0   | 0   |
| 0   | 0   | 0   | 1   | 1   |
| 0   | 0   | 1   | 0   | 1   |
| 0   | 0   | 1   | 1   | 0   |
| 0   | 1   | 0   | 0   | 0   |
| 0   | 1   | 0   | 1   | 0   |
| 0   | 1   | 1   | 0   | 0   |
| 0   | 1   | 1   | 1   | 0   |
| 1   | 0   | 0   | 0   | 0   |
| 1   | 0   | 0   | 1   | 0   |
| 1   | 0   | 1   | 0   | 0   |
| 1   | 0   | 1   | 1   | 0   |
| 1   | 1   | 0   | 0   | 0   |
| 1   | 1   | 0   | 1   | 0   |
| 1   | 1   | 1   | 0   | 0   |
| 1   | 1   | 1   | 1   | 0   |

Standard gates

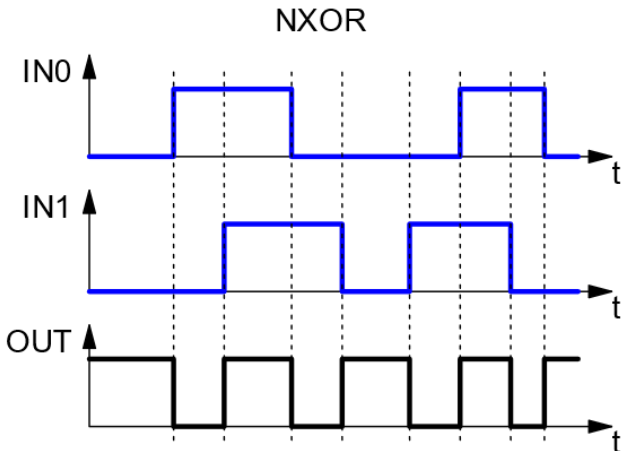
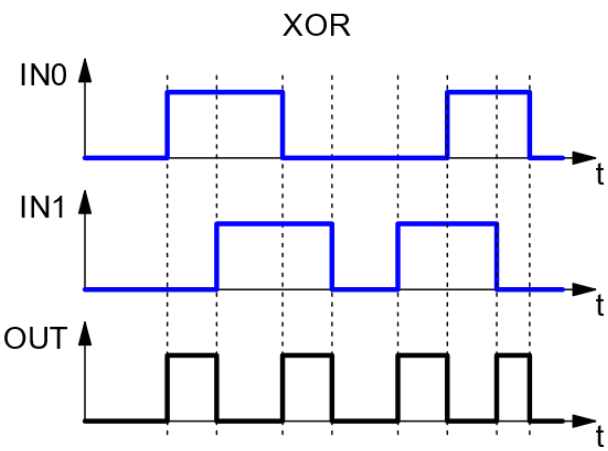
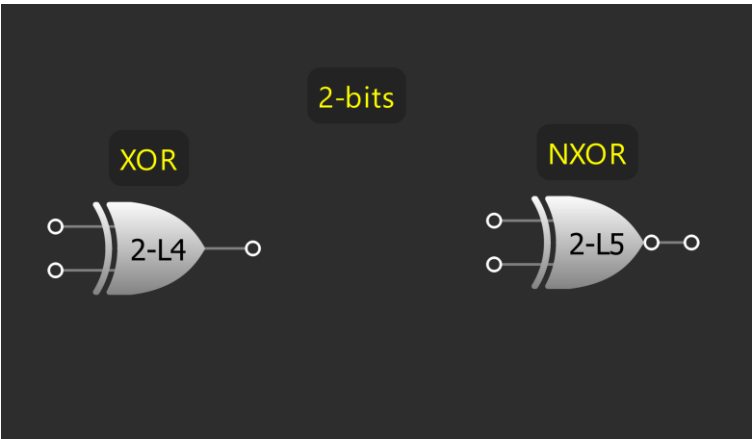
XOR

☐ Regular shape

All to 0

All to 1

Invert



Properties

2-bit LUT5

| IN3 | IN2 | IN1 | IN0 | OUT |
|-----|-----|-----|-----|-----|
| 0   | 0   | 0   | 0   | 1   |
| 0   | 0   | 0   | 1   | 0   |
| 0   | 0   | 1   | 0   | 0   |
| 0   | 0   | 1   | 1   | 1   |
| 0   | 1   | 0   | 0   | 0   |
| 0   | 1   | 0   | 1   | 0   |
| 0   | 1   | 1   | 0   | 0   |
| 0   | 1   | 1   | 1   | 0   |
| 1   | 0   | 0   | 0   | 0   |
| 1   | 0   | 0   | 1   | 0   |
| 1   | 0   | 1   | 0   | 0   |
| 1   | 0   | 1   | 1   | 0   |
| 1   | 1   | 0   | 0   | 0   |
| 1   | 1   | 0   | 1   | 0   |
| 1   | 1   | 1   | 0   | 0   |
| 1   | 1   | 1   | 1   | 0   |

Standard gates

NXOR

☐ Regular shape

All to 0

All to 1

Invert

# COMBINATIONAL LOGIC. STANDARD AND CUSTOMIZED MICROCELL

## STANDARD LUTS (LOOK-UP TABLES)

Properties

3-bit LUT8

| IN3 | IN2 | IN1 | IN0 | OUT |
|-----|-----|-----|-----|-----|
| 0   | 0   | 0   | 0   | 0   |
| 0   | 0   | 0   | 1   | 1   |
| 0   | 0   | 1   | 0   | 1   |
| 0   | 0   | 1   | 1   | 0   |
| 0   | 1   | 0   | 0   | 1   |
| 0   | 1   | 0   | 1   | 0   |
| 0   | 1   | 1   | 0   | 0   |
| 0   | 1   | 1   | 1   | 1   |
| 1   | 0   | 0   | 0   | 0   |
| 1   | 0   | 0   | 1   | 0   |
| 1   | 0   | 1   | 0   | 0   |
| 1   | 0   | 1   | 1   | 0   |
| 1   | 1   | 0   | 0   | 0   |
| 1   | 1   | 0   | 1   | 0   |
| 1   | 1   | 1   | 0   | 0   |
| 1   | 1   | 1   | 1   | 0   |

Standard gates

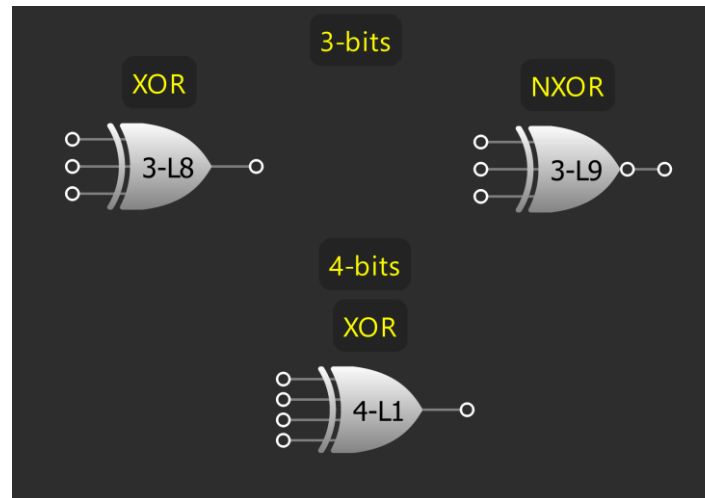
XOR

☐ Regular shape

All to 0

All to 1

Invert



Properties

3-bit LUT9

| IN3 | IN2 | IN1 | IN0 | OUT |
|-----|-----|-----|-----|-----|
| 0   | 0   | 0   | 0   | 1   |
| 0   | 0   | 0   | 1   | 0   |
| 0   | 0   | 1   | 0   | 0   |
| 0   | 0   | 1   | 1   | 1   |
| 0   | 1   | 0   | 0   | 0   |
| 0   | 1   | 0   | 1   | 1   |
| 0   | 1   | 1   | 0   | 1   |
| 0   | 1   | 1   | 1   | 0   |
| 1   | 0   | 0   | 0   | 0   |
| 1   | 0   | 0   | 1   | 0   |
| 1   | 0   | 1   | 0   | 0   |
| 1   | 0   | 1   | 1   | 0   |
| 1   | 1   | 0   | 0   | 0   |
| 1   | 1   | 0   | 1   | 0   |
| 1   | 1   | 1   | 0   | 0   |
| 1   | 1   | 1   | 1   | 0   |

Standard gates

NXOR

☐ Regular shape

All to 0

All to 1

Invert