

GREENPAK TECHNICAL INTRODUCTION WEBINAR

GREENPAK™
PROGRAMMABLE MIXED-SIGNAL MATRIX TECHNOLOGY
CONFIGURABLE MIXED-SIGNAL IC (CMIC)



AGENDA

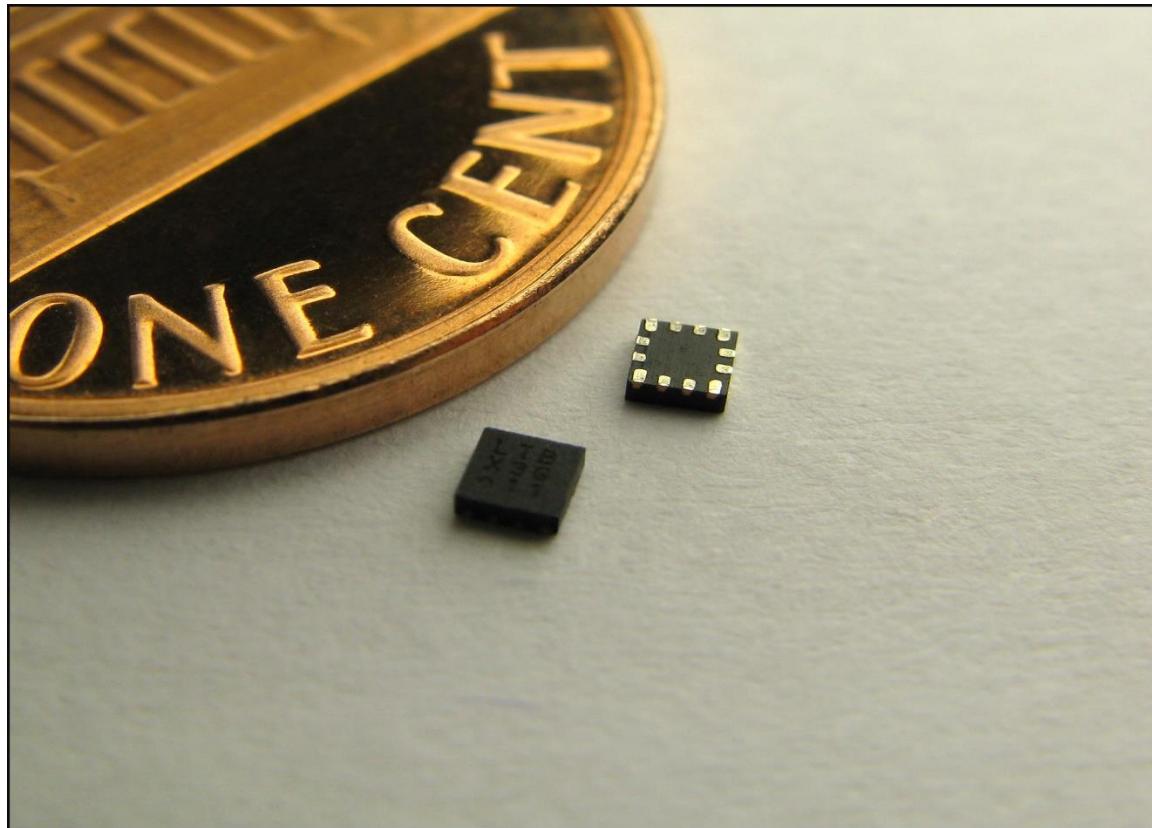
GreenPAK Basics

- PAD modes and its usage
- Combinational Logic. Standard and customized macrocell

GREENPAK DESIGN BASICS

WHAT IS GREENPAK?

The World's 1st Custom Mixed-signal IC (CMIC) Family



- Roughly 70 ICs, each with a unique set of features
- Customizable with simple, free software
- Very small package, down to 1.2mm²
- Low power solution
- Can be used in a myriad of applications...

WHAT CAN I DO WITH GREENPAK™

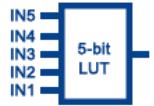
GreenPAK Functions



Level Translation



ADC



Glue Logic



Pulse Width Modulator



Voltage Monitor



H-/Half-Bridge*



Finite State Machine



Op Amp



Counters / Delays



Rheostat /
Potentiometer



Applications

- Supervisory Circuits
- System Reset
- LED Control
- Motor & Fan Control*
- Power Sequencing
- Voltage Detection
- Frequency Detection
- Sensor Interface
- Port Detection
- Temperature Control
- Battery Monitor

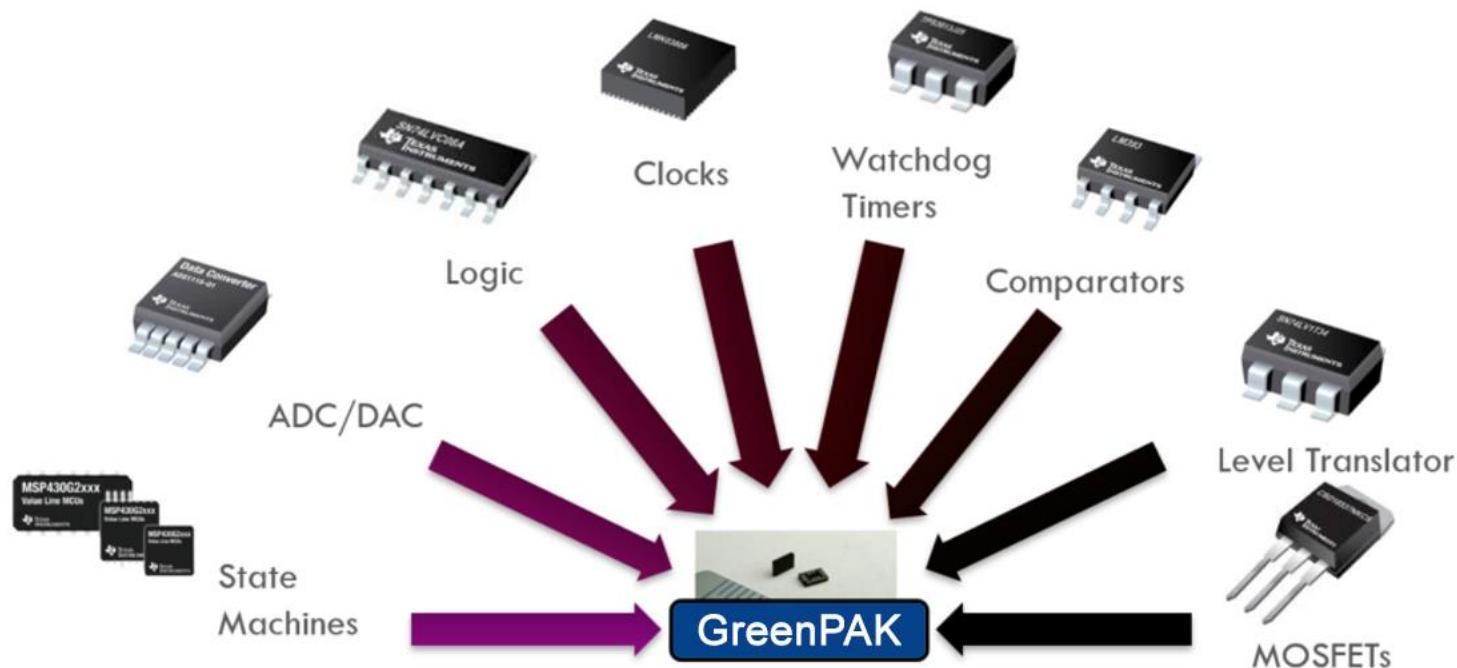
*Not for Automotive qualified GreenPAK

WHAT DOES GREENPAK REPLACE?

GreenPAK can replace simple discrete logic , analog comparators, low end 8-bit ADC's, etc.

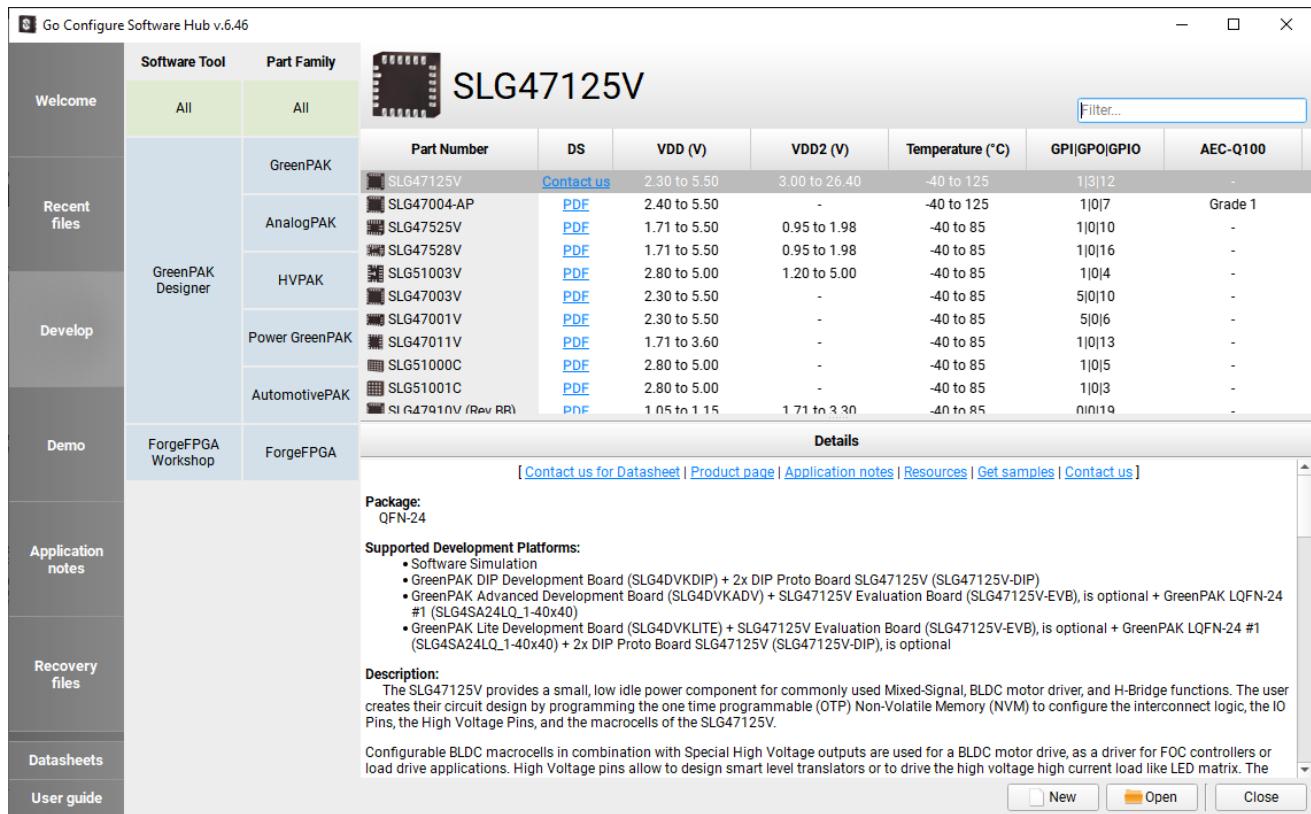
It can be used to implement non-standard variations of reset IC's and other ASSP's without tooling or NRE.

This can support new variations of applications for customers who run into design issues.



GREENPAK DEVELOPMENT SOFTWARE

Go Configure Software Hub



Tabs

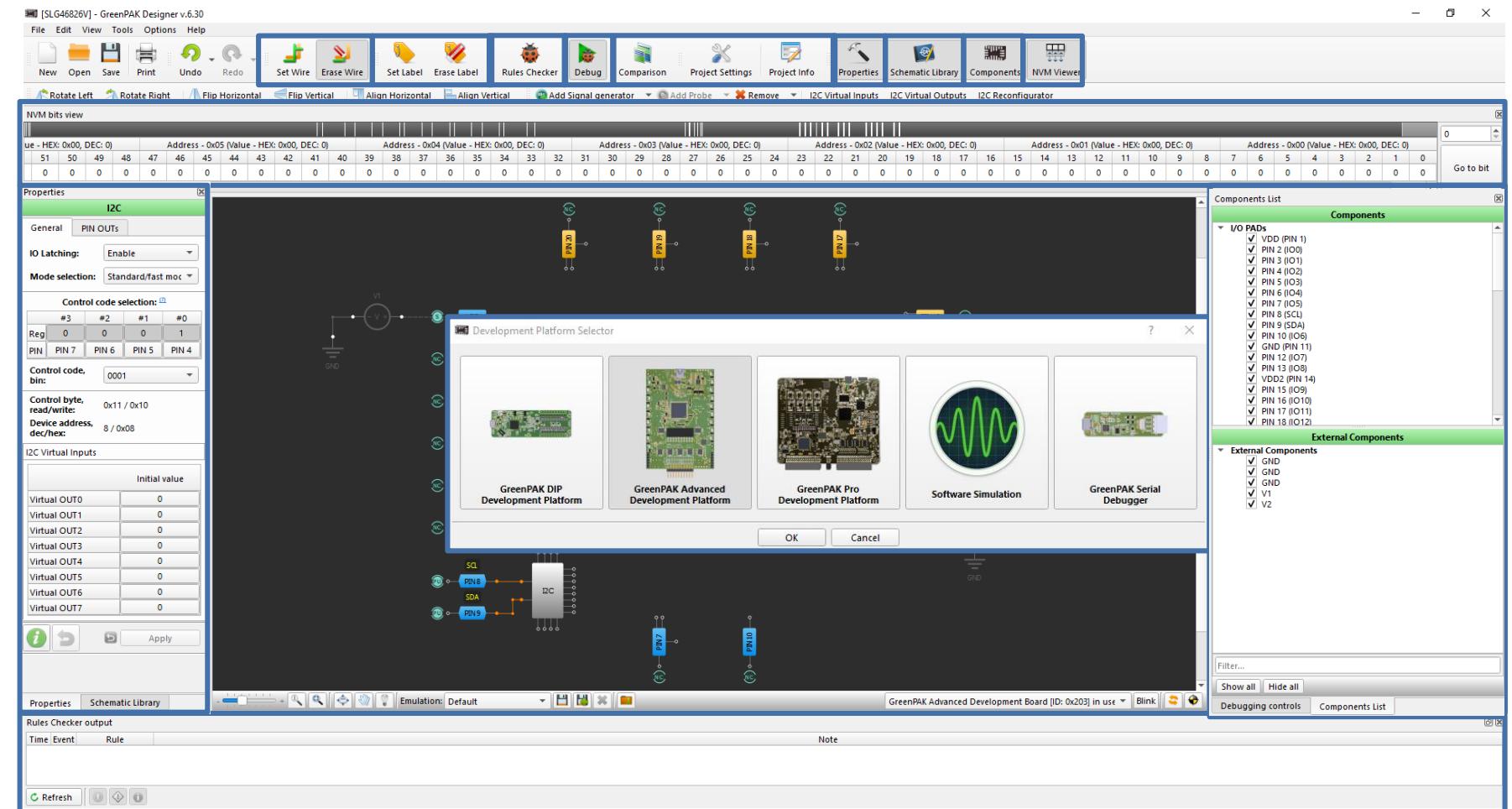
- Welcome: Design Tips, Links to Product Brochures, Application Notes, and Training Videos
- Develop: Table of GreenPAK ICs with their PCB Footprint and Logic Resource Availability
- Demo: List of Common GreenPAK Applications
- Datasheets
- User Guides

GREENPAK DEVELOPMENT SOFTWARE

GreenPAK Designer

Tool Bar

- Set / Erase Wire
- Set / Erase Label
- Rules Checker
- Debug
- Project Settings
- Project Info
- Properties
- Schematic Library
- Components
- NVM Viewer
- Change platform

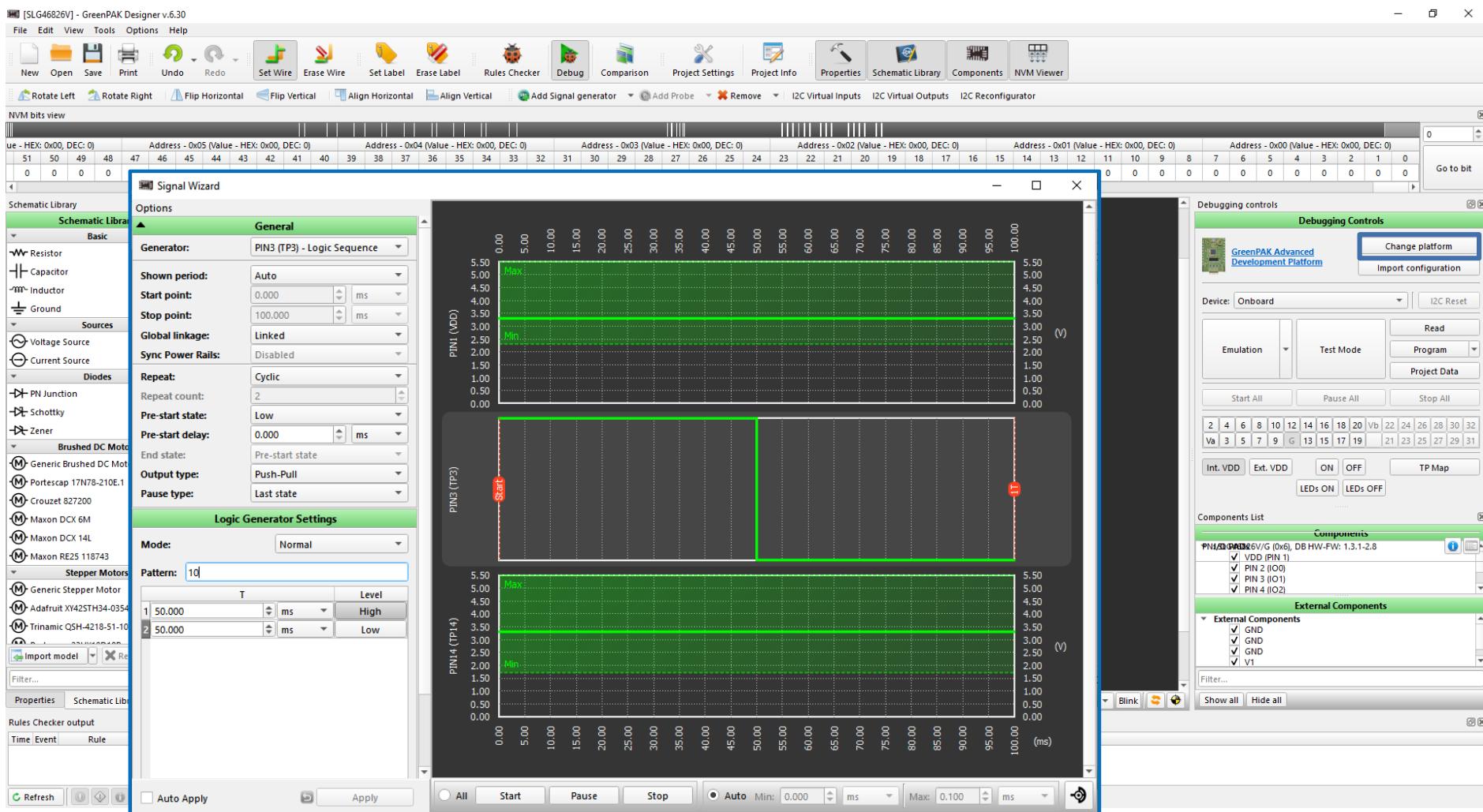


GREENPAK DEVELOPMENT SOFTWARE

GreenPAK Designer

Debug with Hardware

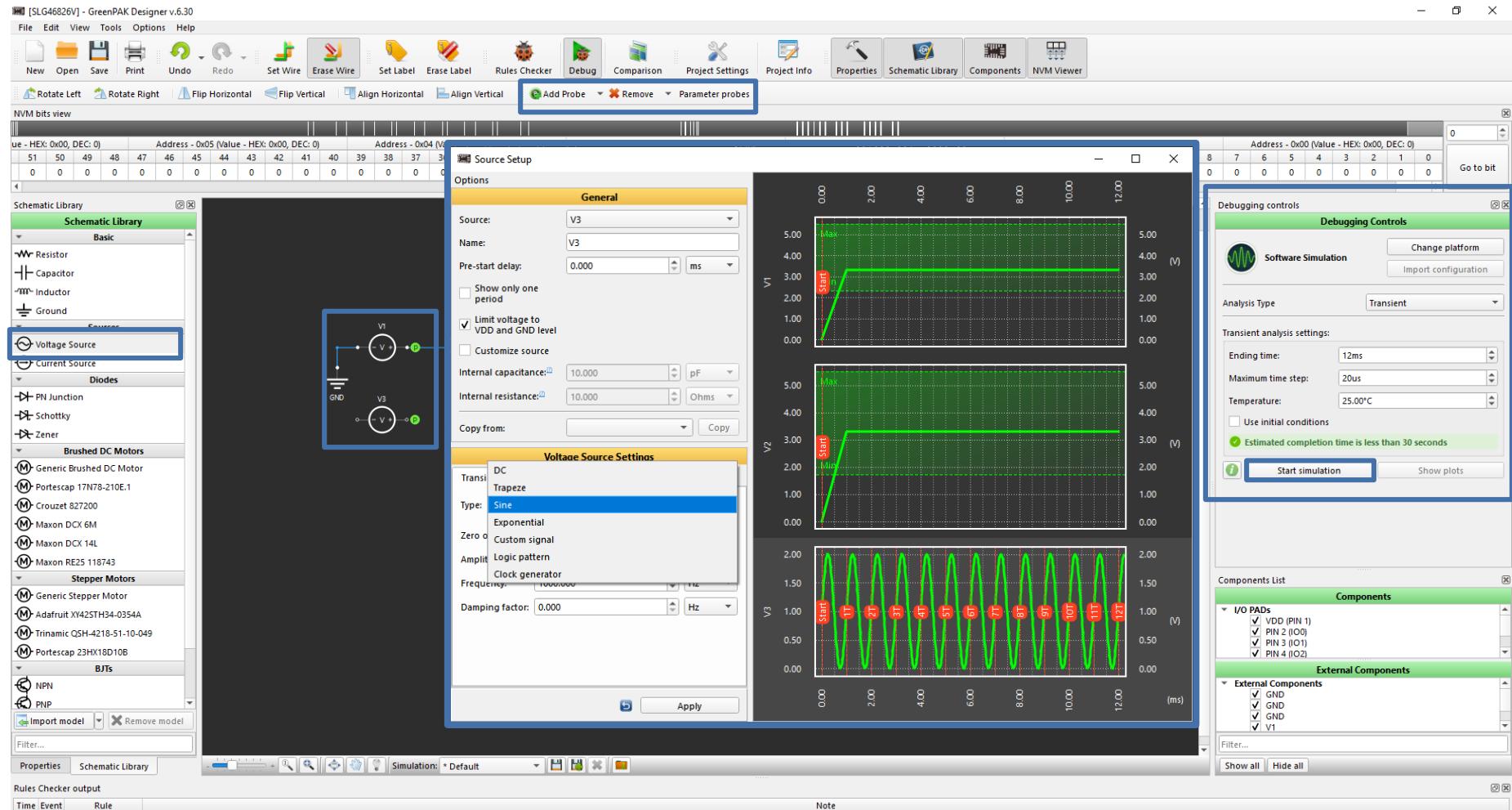
- Logic generator
- Signal generator
- I2C generator



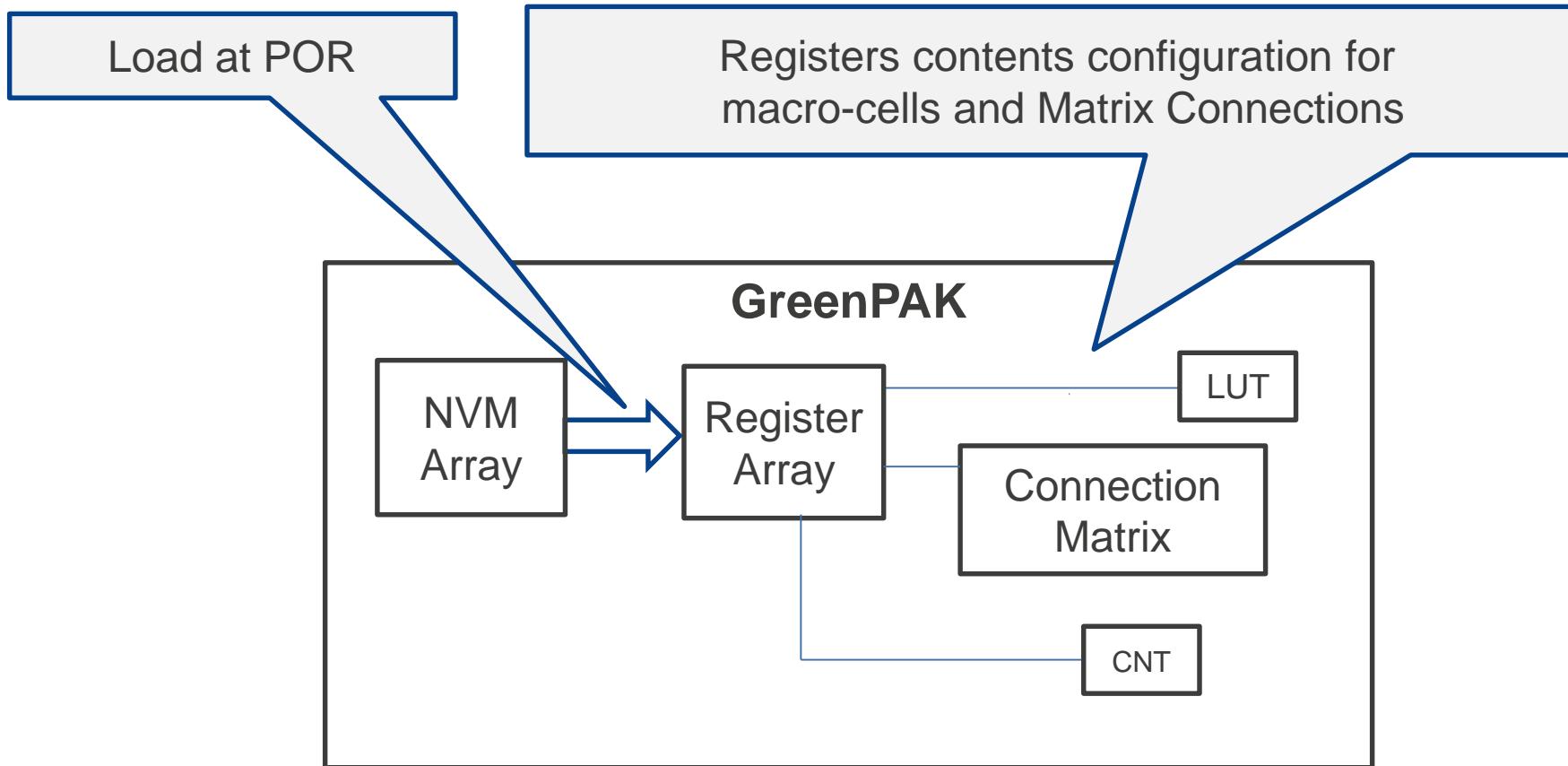
GREENPAK DEVELOPMENT SOFTWARE

GreenPAK Designer

- Voltage Source
- Add Probe
- Remove
- Debugging Controls

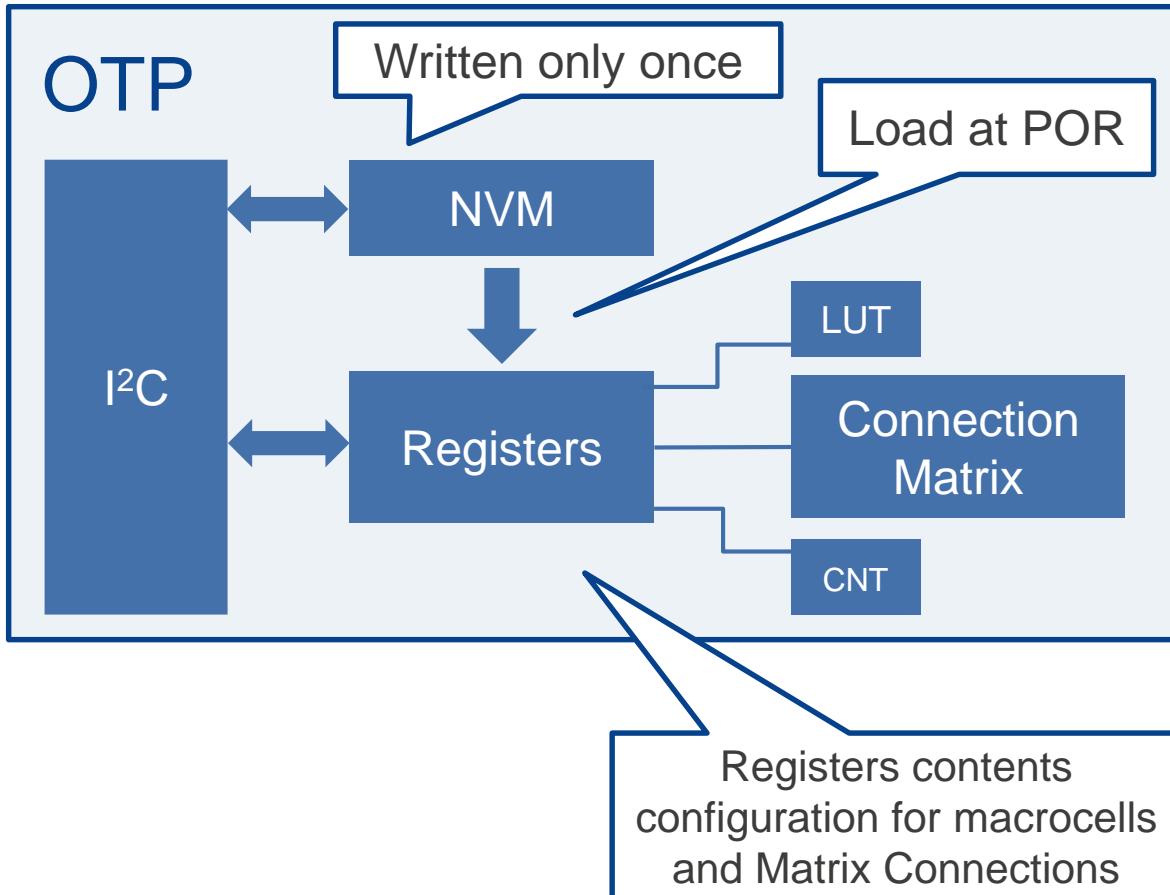


BASIC GreenPAK ARCHITECTURE



STRUCTURE OF THE GREENPAK IC MEMORY

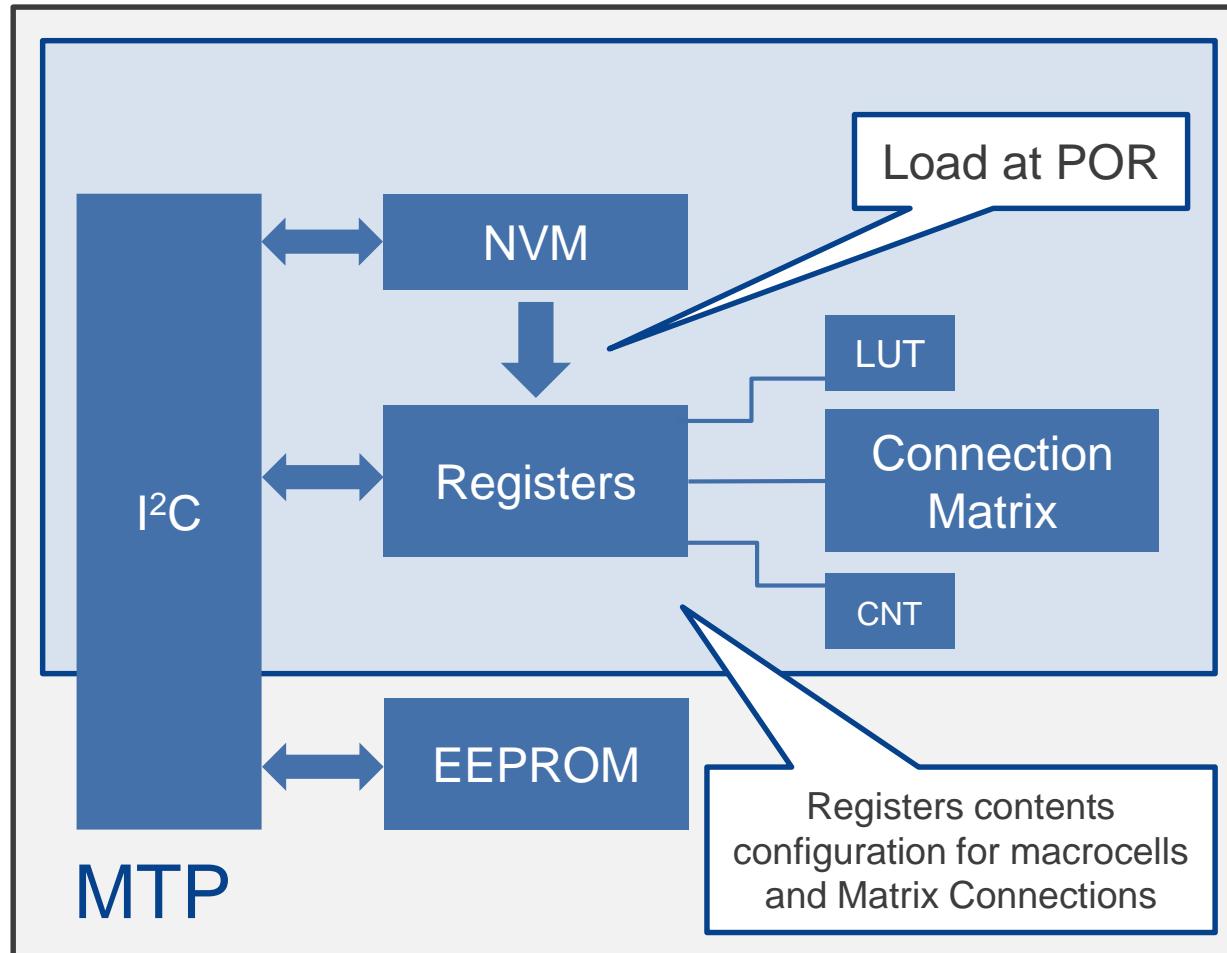
How IC Memory Works in OTP and MTP/ISP Circuits



- During start NVM memory is emulated to Registers.
- Inside the NVM, there is a specifically dedicated protection page, MTP enables to change security settings.

STRUCTURE OF THE GREENPAK IC MEMORY

How IC Memory Works in OTP and MTP/ISP Circuits



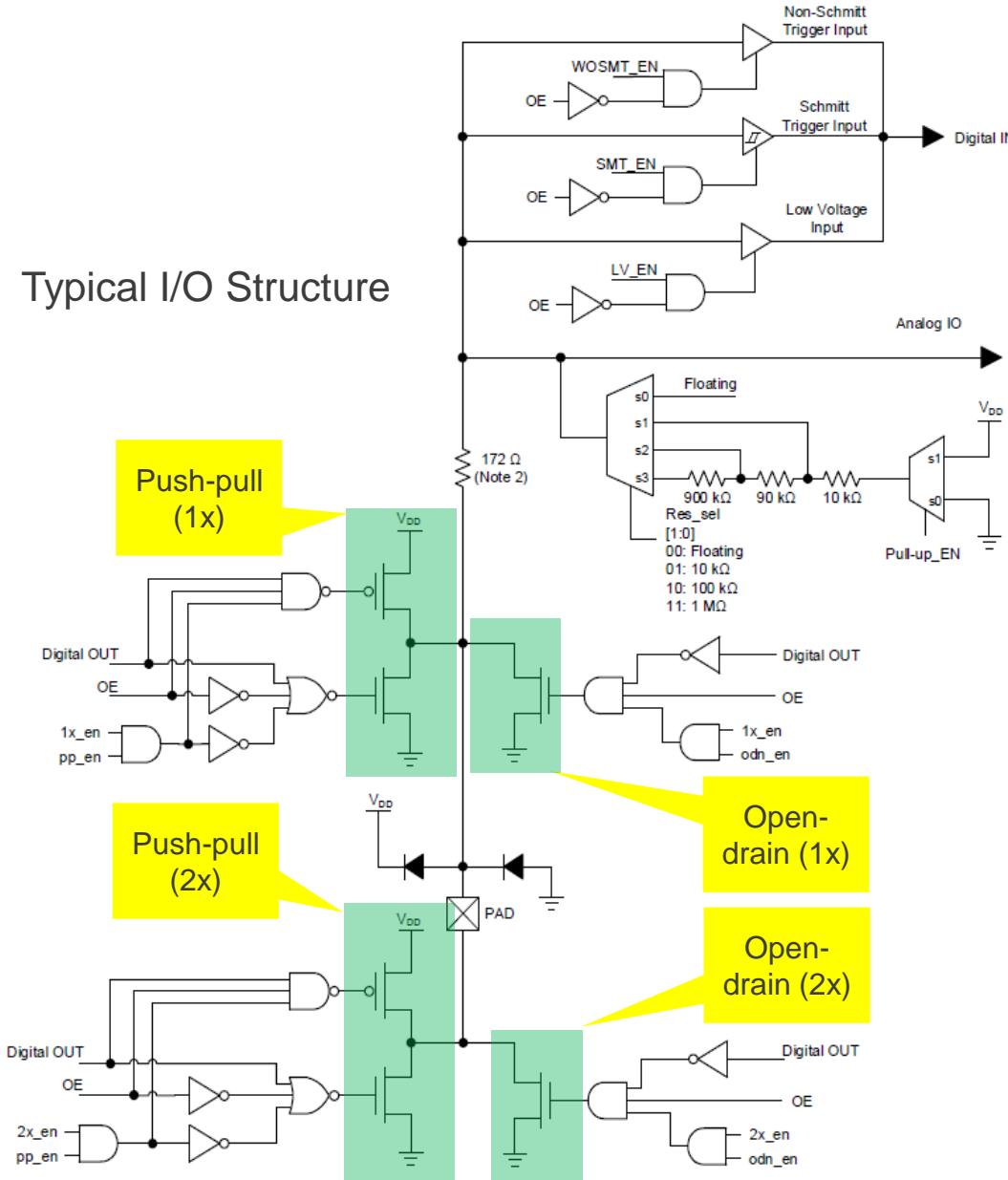
- During start NVM memory is emulated to Registers.
- Inside the NVM, there is a specifically dedicated protection page, MTP enables to change security settings.
- SLG46826 isSLG46826 is a representative of MTP devices

PAD MODES AND ITS USAGE

Most I/Os in GreenPAK devices are very flexible

- Various output modes [Push-pull (1x or 2x), Open-drain (1x or 2x) or Analog-Output]
- Various input modes [Digital-In, Digital-In with Schmitt trigger, Low Voltage Digital-In and Analog-In]
- Some I/Os support Output Enable
- Some I/Os support level shifting

Typical I/O Structure

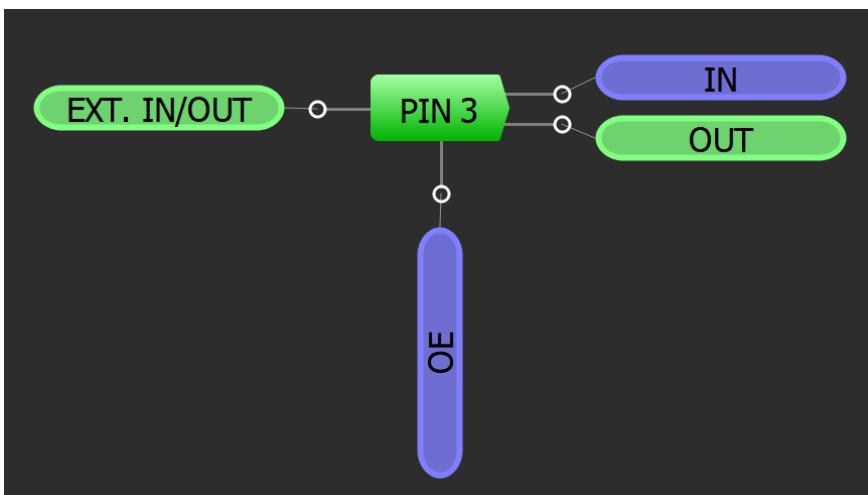


PAD MODES AND ITS USAGE

DIGITAL INPUT MODE

Difference between input PINs in different modes:

1. Threshold level
2. Switching speed(propagation delay)
3. Current consumption



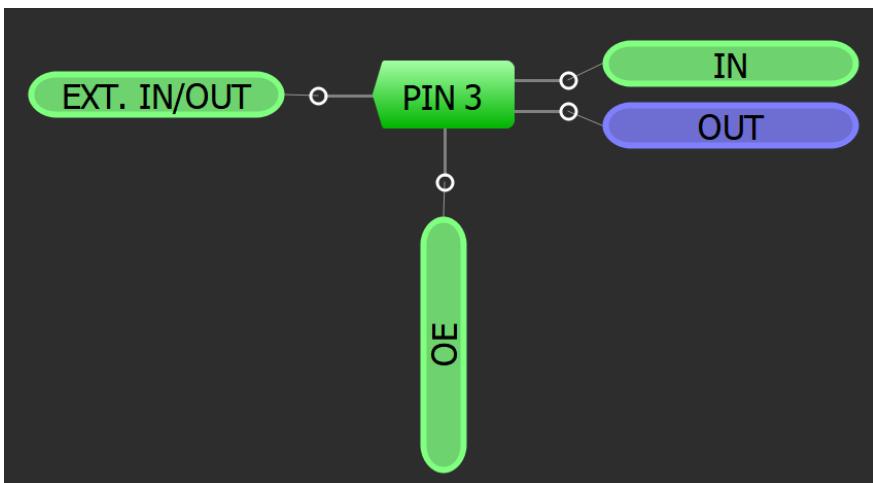
Properties			
PIN 3 (IO1)			
I/O selection:			Digital input
Input mode: OE = 0			Digital in without
Output mode: OE = 1			None
Resistor:			Floating
Resistor value:			Floating
100uA pullup on input:			None
Information			
Electrical Specifications			
	2.3 V min/max	3.3 V min/max	5.0 V min/max
V_IH (V)	1.247/-	1.693/-	2.494/-
V_IL (V)	-/1.021	-/1.463	-/2.227
-	-/-	-/-	-/-
-	-/-	-/-	-/-
-	-/-	-/-	-/-
-	-/-	-/-	-/-
Properties			
PIN 3 (IO1)			
I/O selection:			Digital input
Input mode: OE = 0			Digital in with Sch
Output mode: OE = 1			None
Resistor:			Floating
Resistor value:			Floating
100uA pullup on input:			None
Information			
Electrical Specifications			
	2.3 V min/max	3.3 V min/max	5.0 V min/max
V_IH (V)	1.475/-	1.978/-	2.884/-
V_IL (V)	-/0.876	-/1.356	-/2.095
-	-/-	-/-	-/-
-	-/-	-/-	-/-
-	-/-	-/-	-/-
-	-/-	-/-	-/-
Properties			
PIN 3 (IO1)			
I/O selection:			Digital input
Input mode: OE = 0			Low voltage digital
Output mode: OE = 1			None
Resistor:			Floating
Resistor value:			Floating
100uA pullup on input:			None
Information			
Electrical Specifications			
	2.3 V min/max	3.3 V min/max	5.0 V min/max
V_IH (V)	0.957/-	1.042/-	1.127/-
V_IL (V)	-/0.647	-/0.722	-/0.814
-	-/-	-/-	-/-
-	-/-	-/-	-/-
-	-/-	-/-	-/-
-	-/-	-/-	-/-

PAD MODES AND ITS USAGE

DIGITAL OUTPUT MODE

Difference between output PINs in different modes:

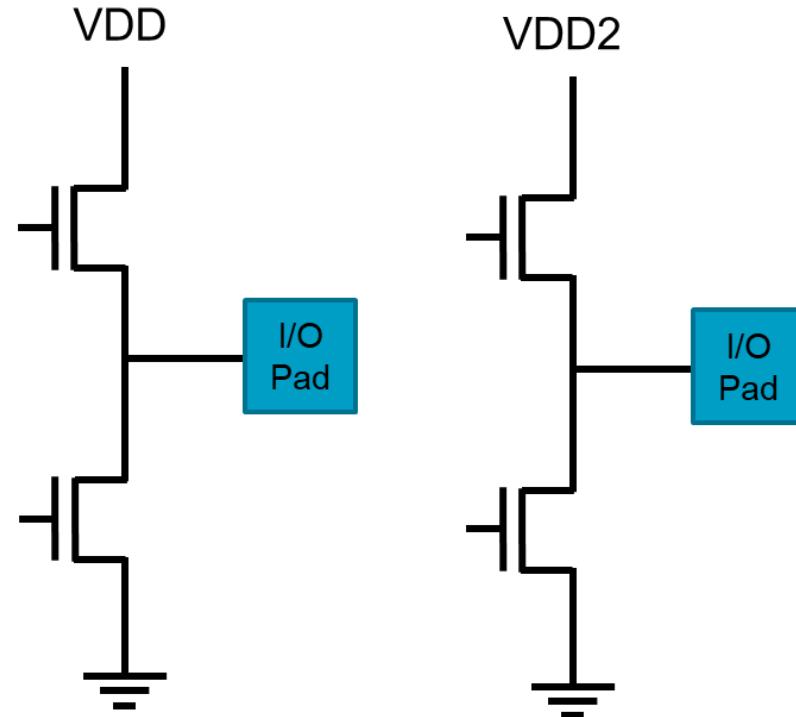
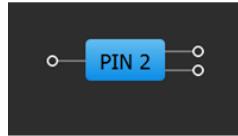
1. Maximum current that PIN can pass
2. Possibility to make parallel connection
3. Possibility to make Hi-Z state



Properties			
PIN 3 (IO1)			
I/O selection:			Digital output
Input mode: OE = 0			None
Output mode: OE = 1			1x push pull
Resistor:			Floating
Resistor value:			Floating
100uA pullup on input:			None
Information			
Electrical Specifications			
	2.3 V min/max	3.3 V min/max	5.0 V min/max
V _{OH} (V)	1.693/-	2.703/-	4.149/-
V _{OL} (V)	-/0.013	-/0.184	-/0.243
I _{OH} (mA)	1.034/-	5.498/-	20.007/-
I _{OL} (mA)	1.190/-	5.358/-	7.227/-
-	-/-	-/-	-/-
-	-/-	-/-	-/-
-	-/-	-/-	-/-
Properties			
PIN 3 (IO1)			
I/O selection:			Digital output
Input mode: OE = 0			None
Output mode: OE = 1			1x open drain NM
Resistor:			Floating
Resistor value:			Floating
100uA pullup on input:			None
Information			
Electrical Specifications			
	2.3 V min/max	3.3 V min/max	5.0 V min/max
V _{OH} (V)	-/0.008	-/0.093	-/0.124
V _{OL} (V)	2.384/-	10.557/-	14.128/-
-	-/-	-/-	-/-
-	-/-	-/-	-/-
-	-/-	-/-	-/-
Properties			
PIN 3 (IO1)			
I/O selection:			Digital output
Input mode: OE = 0			None
Output mode: OE = 1			1x 3-State Output
Resistor:			Floating
Resistor value:			Floating
100uA pullup on input:			None
Information			
Electrical Specifications			
	2.3 V min/max	3.3 V min/max	5.0 V min/max
V _{OH} (V)	1.693/-	2.703/-	4.149/-
V _{OL} (V)	-/0.013	-/0.184	-/0.243
I _{OH} (mA)	1.034/-	5.498/-	20.007/-
I _{OL} (mA)	1.190/-	5.358/-	7.227/-
-	-/-	-/-	-/-
-	-/-	-/-	-/-

LEVEL SHIFTING

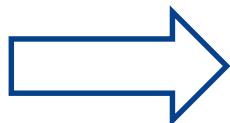
- GreenPAK devices with VDD2 have some I/O pins tied to VDD2
 - You can see this by the color of the Pin icon
- This makes level shifting applications very easy to implement
- Some of the devices have VDD2



COMBINATIONAL LOGIC. STANDARD AND CUSTOMIZED MICROCELL CUSTOMIZED LUT BASED

Таблиця з практичної роботи №2 легко формується в SLG46826 (4bit LUT) повторюючи функціонал логічної схеми

				Отримане число ↓	
A	B	C	D	OUT	Combination
0	0	0	0	0	-
0	0	0	1	0	-
0	0	1	0	0	-
0	0	1	1	1	$\bar{A}\bar{B}CD$
0	1	0	0	1	$\bar{A}\bar{B}\bar{C}\bar{D}$
0	1	0	1	0	-
0	1	1	0	1	$\bar{A}\bar{B}\bar{C}\bar{D}$
0	1	1	1	1	$\bar{A}\bar{B}CD$
1	0	0	0	1	$A\bar{B}\bar{C}\bar{D}$
1	0	0	1	1	$A\bar{B}\bar{C}D$
1	0	1	0	0	-
1	0	1	1	1	$A\bar{B}CD$
1	1	0	0	1	$A\bar{B}\bar{C}\bar{D}$
1	1	0	1	1	$A\bar{B}\bar{C}D$
1	1	1	0	0	-
1	1	1	1	0	-



4-bit LUT0/CNT2/DLY2/FSM0

Type: LUT

IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	1
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

Standard gates

All to 0

Defined by user

All to 1

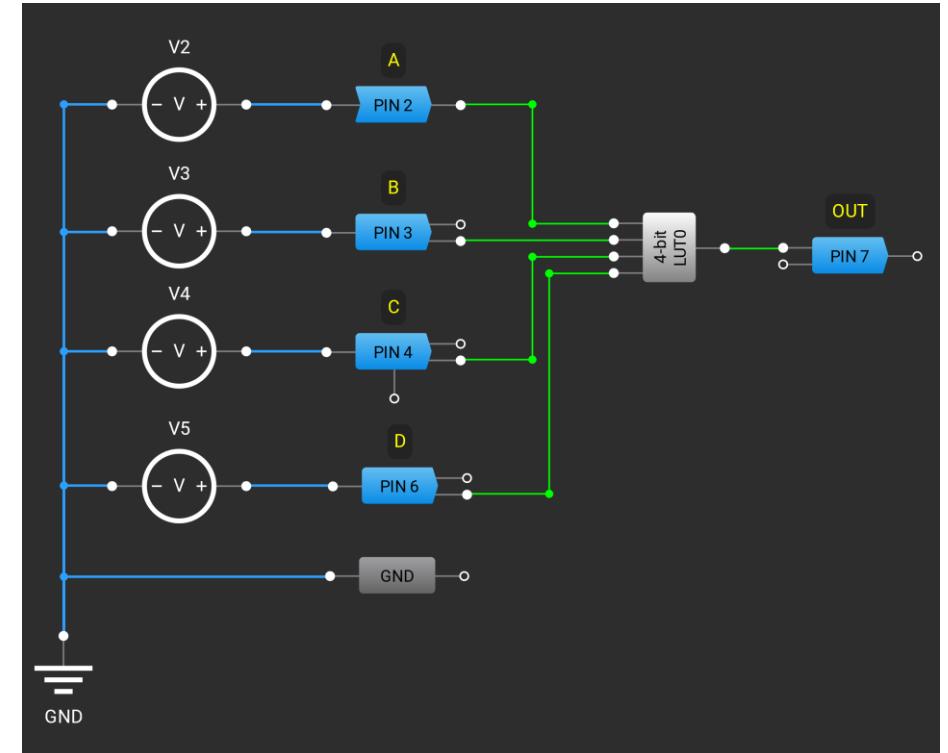
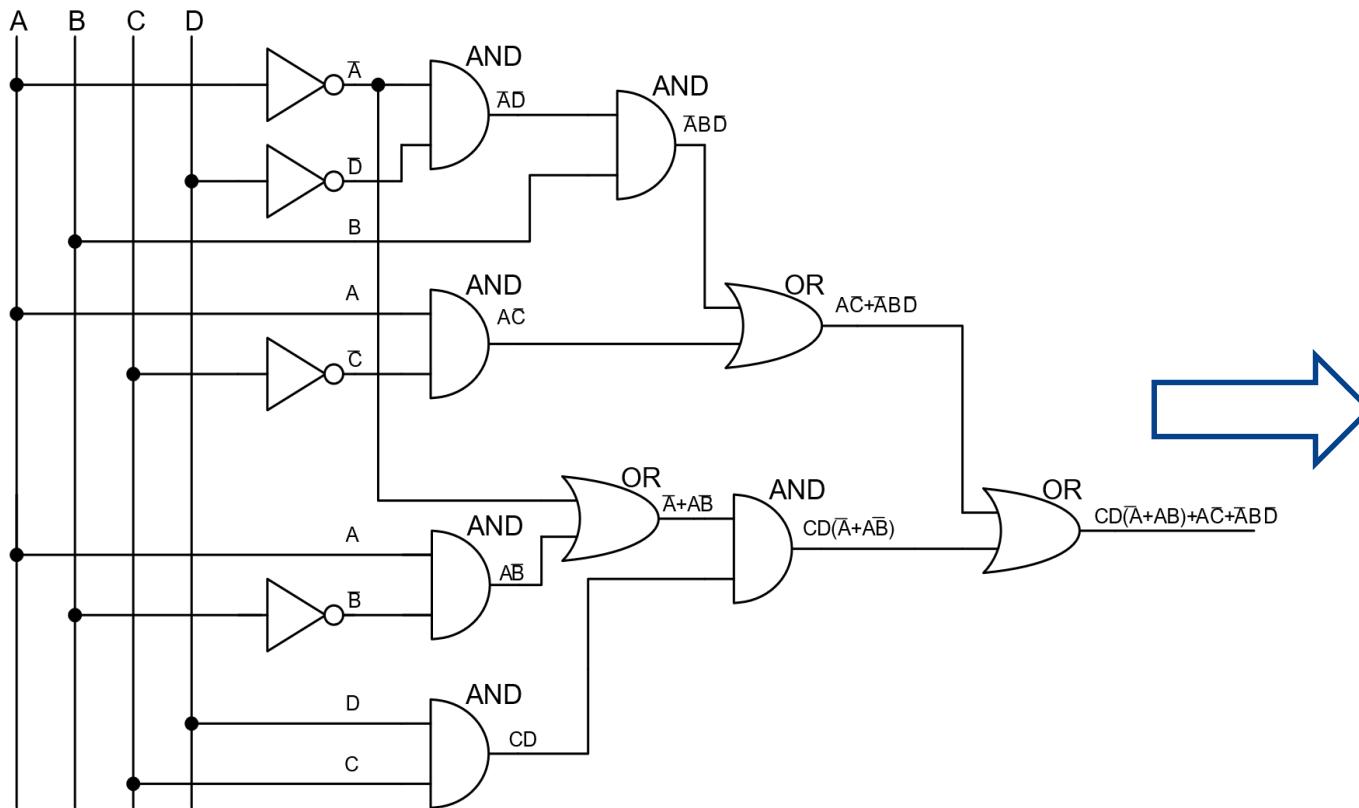
Regular shape

Invert

Apply

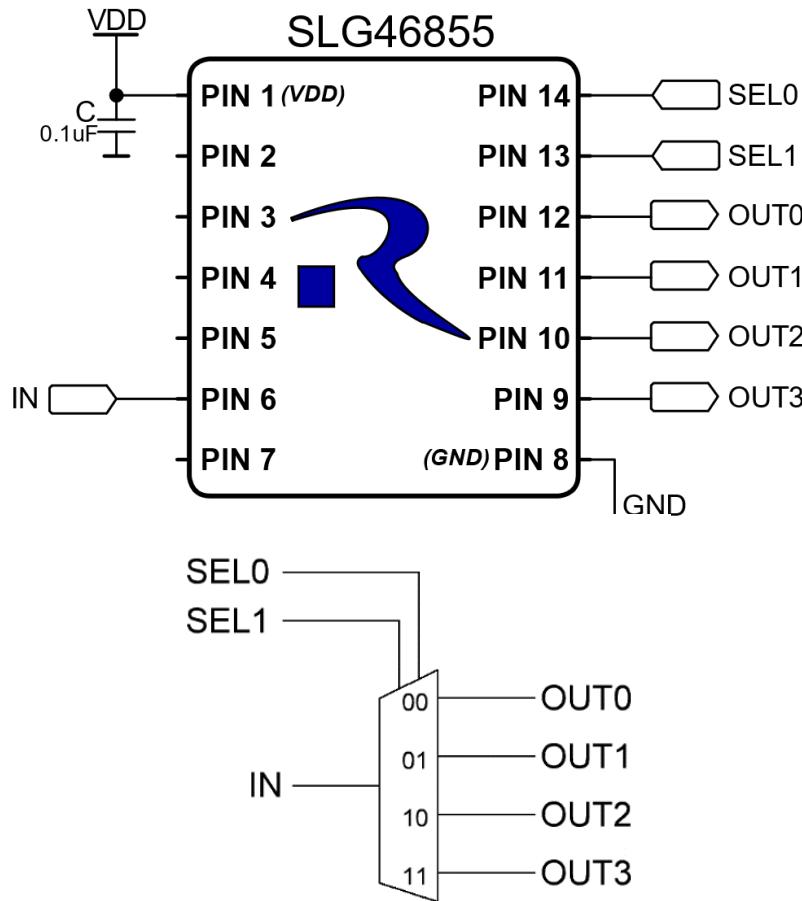
COMBINATIONAL LOGIC. STANDARD AND CUSTOMIZED MICROCELL CUSTOMIZED LUT BASED

Відтак логічна функція, котру реалізовували 4 мікросхеми (1x7404 (NOT), 2x7408 (AND), 1x7432 (OR))
тепер

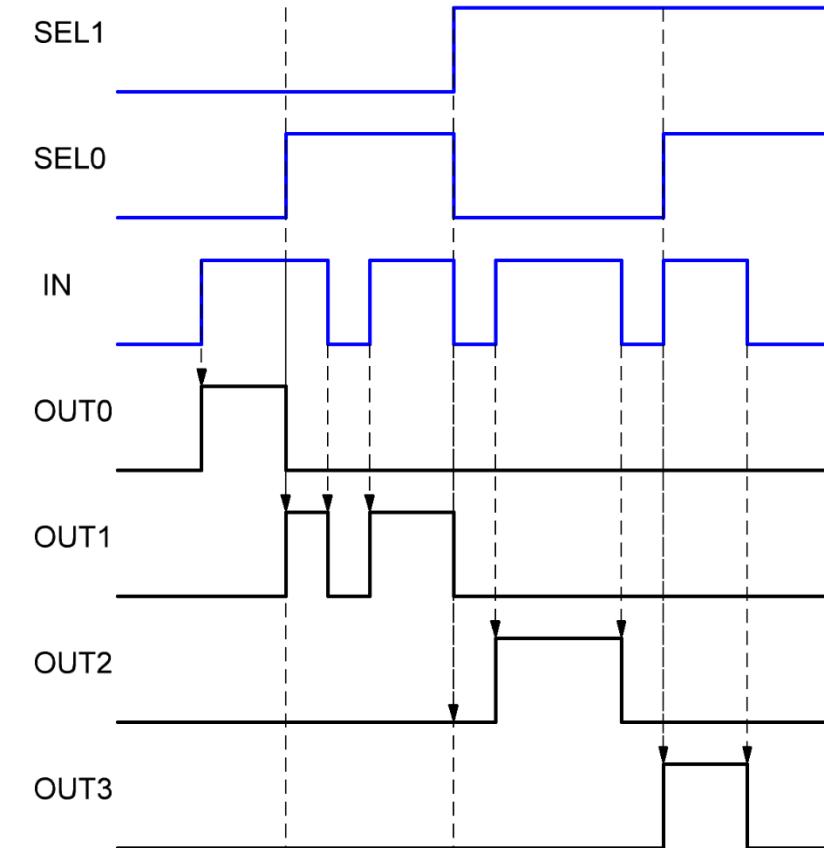


GREENPAK APPLICATION OPPORTUNITIES. HANDS-ON

Demultiplexer (DEMUX)



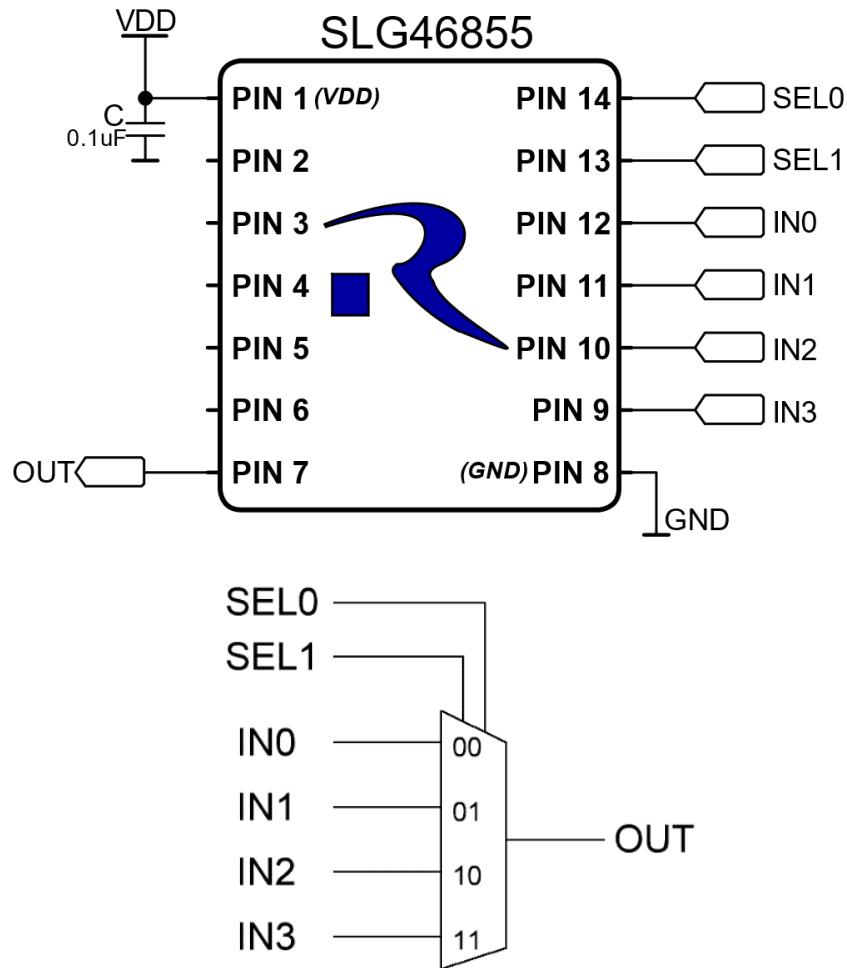
- Chosen by SELx code output copies input



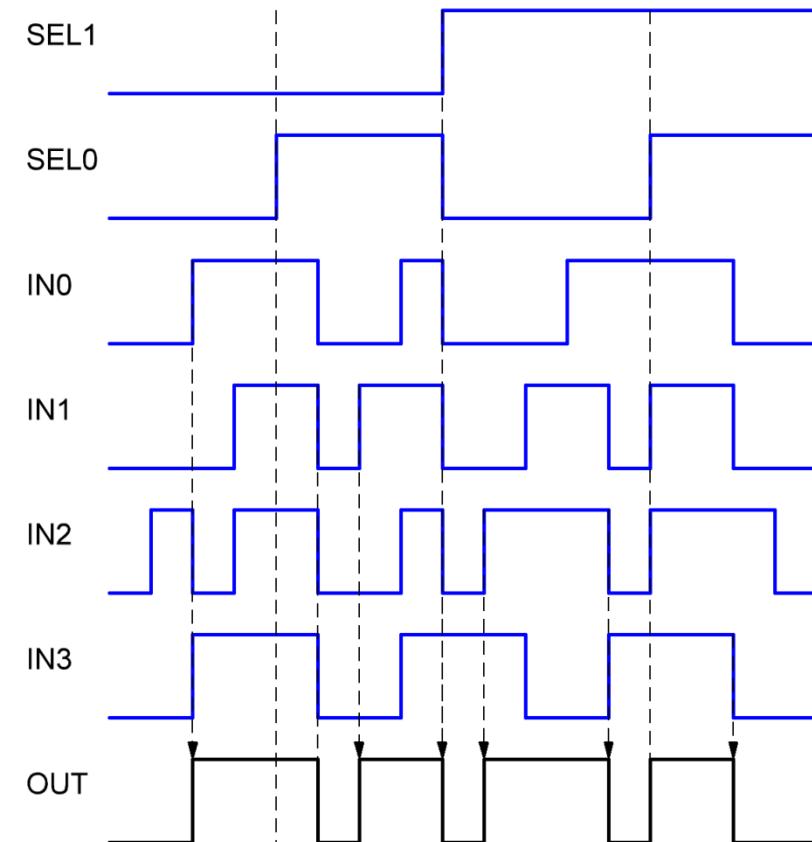
1.6 x 2.0 mm STQFN
14-pin package

GREENPAK APPLICATION OPPORTUNITIES. HANDS-ON

Multiplexer (MUX)



- Output copies one of inputs depending on the SELx code



COMBINATIONAL LOGIC. STANDARD AND CUSTOMIZED MICROCELL

STANDARD LUTS (LOOK-UP TABLES)

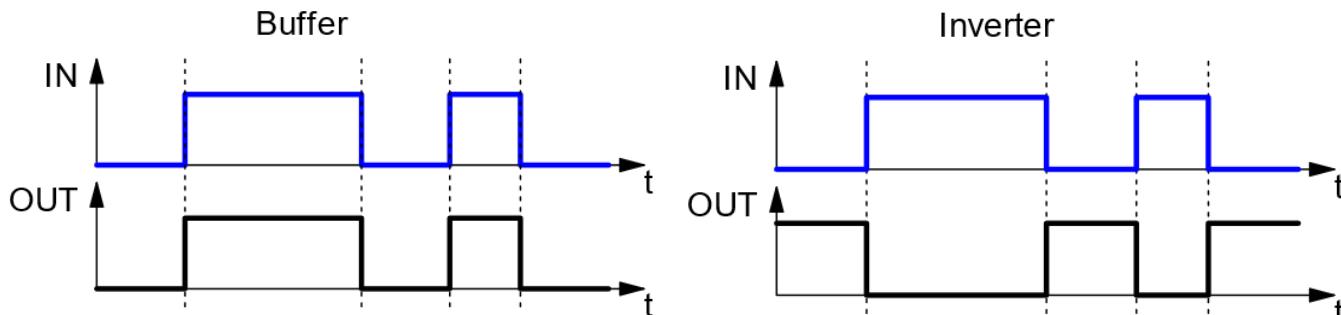
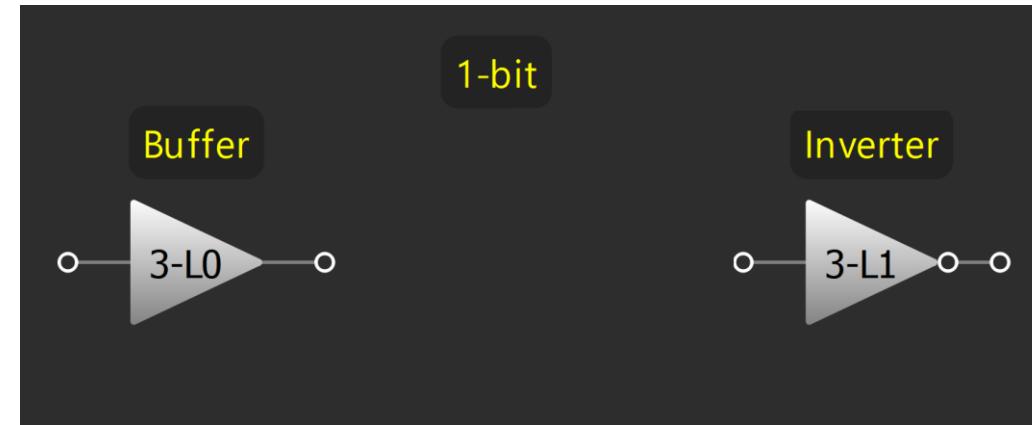
Properties

3-bit LUT0

IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	1
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Standard gates

Buffer All to 0
 Regular shape Invert



Properties

3-bit LUT1

IN3	IN2	IN1	IN0	OUT
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	1	0	0
1	1	1	1	0

Standard gates

Inverter All to 0
 Regular shape Invert

COMBINATIONAL LOGIC. STANDARD AND CUSTOMIZED MICROCELL

STANDARD LUTS (LOOK-UP TABLES)

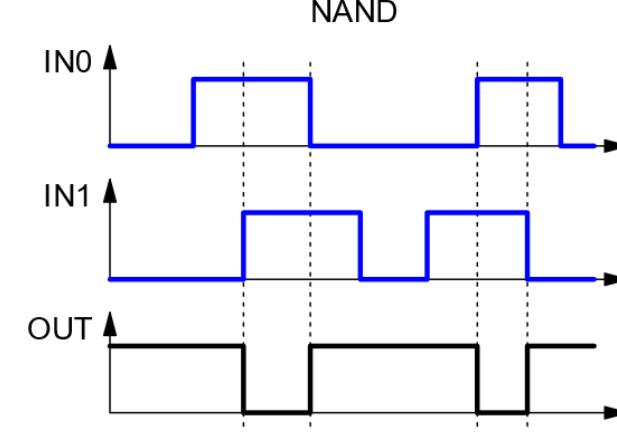
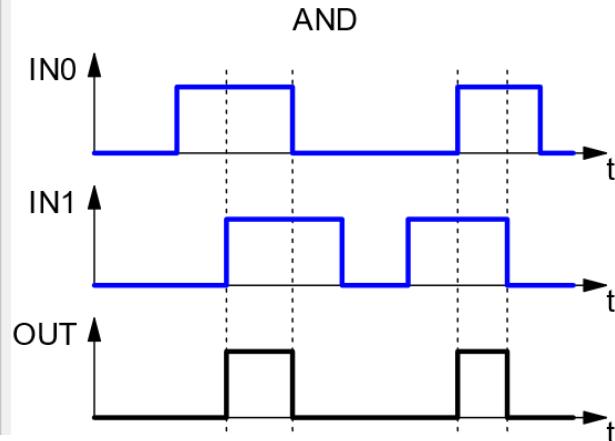
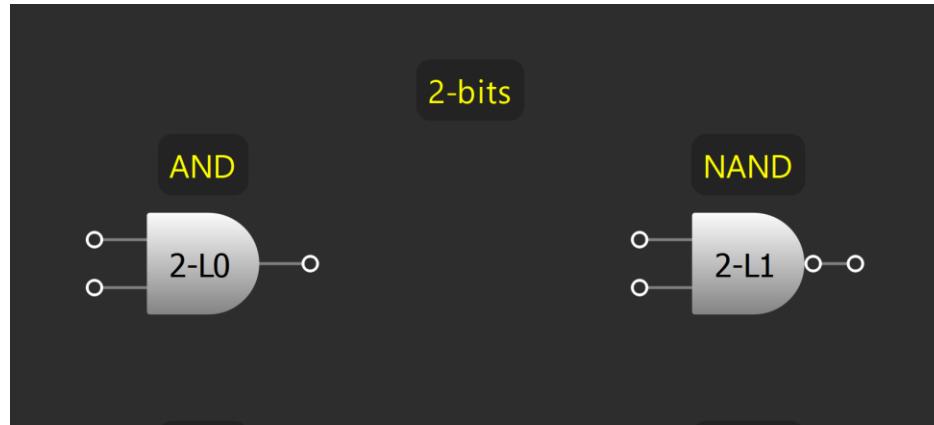
Properties

2-bit LUT0

IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Standard gates

AND Regular shape All to 0 All to 1 Invert



Properties

2-bit LUT1

IN3	IN2	IN1	IN0	OUT
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	0

Standard gates

NAND Regular shape All to 0 All to 1 Invert

COMBINATIONAL LOGIC. STANDARD AND CUSTOMIZED MICROCELL

STANDARD LUTS (LOOK-UP TABLES)

Properties				
3-bit LUT2				
IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Standard gates

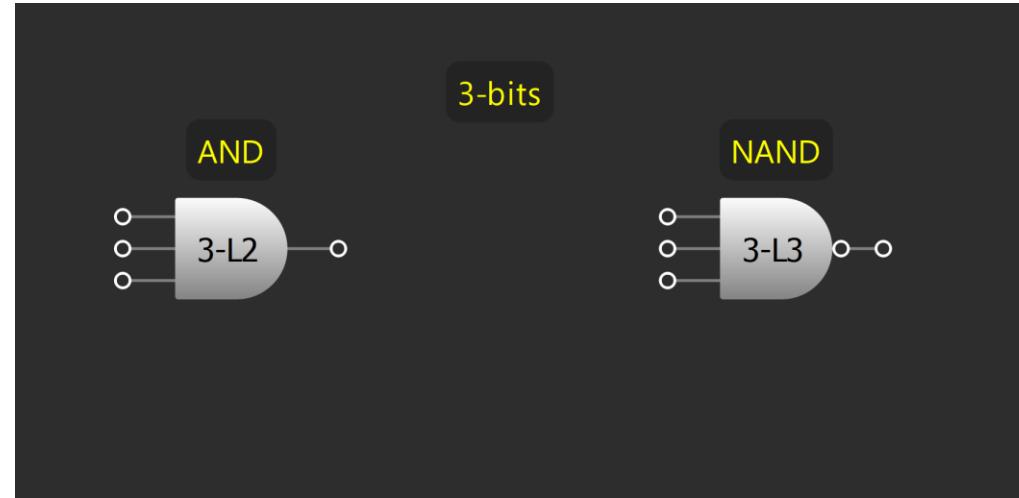
AND

Regular shape

All to 0

All to 1

Invert



Properties				
3-bit LUT3				
IN3	IN2	IN1	IN0	OUT
0	0	0	0	1
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

Standard gates

NAND

Regular shape

All to 0

All to 1

Invert

COMBINATIONAL LOGIC. STANDARD AND CUSTOMIZED MICROCELL

STANDARD LUTS (LOOK-UP TABLES)

Properties

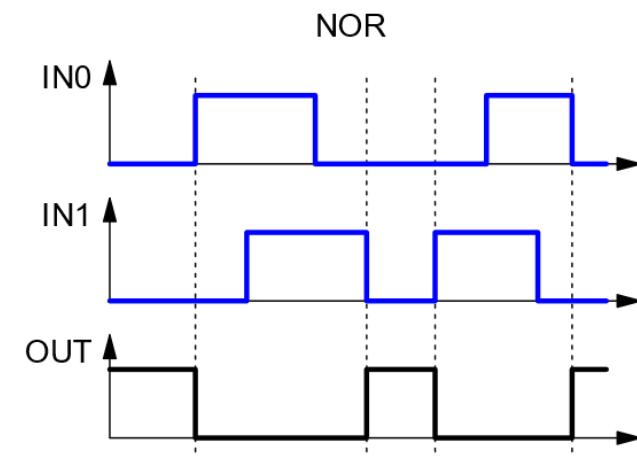
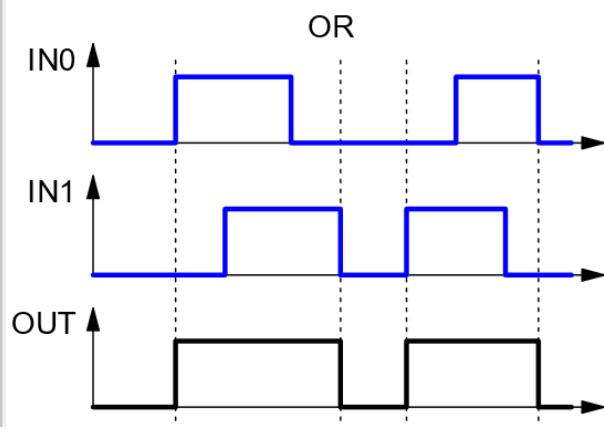
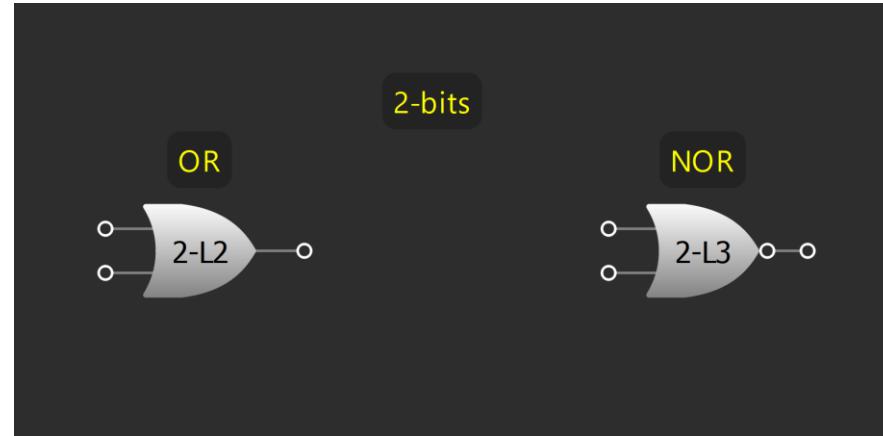
2-bit LUT2

IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	1	0	0
1	1	1	1	0

Standard gates

OR Regular shape

All to 0 All to 1 Invert



Properties

2-bit LUT3

IN3	IN2	IN1	IN0	OUT
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Standard gates

NOR Regular shape

All to 0 All to 1 Invert

COMBINATIONAL LOGIC. STANDARD AND CUSTOMIZED MICROCELL

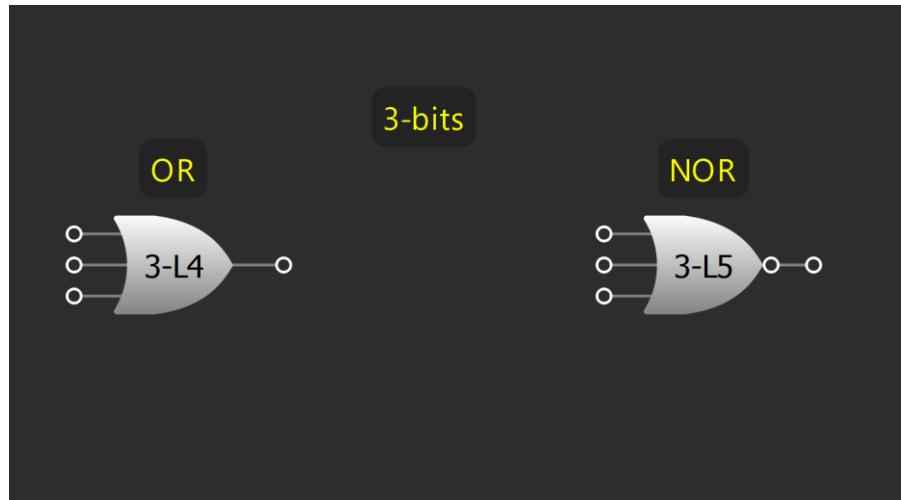
STANDARD LUTS (LOOK-UP TABLES)

Properties				
3-bit LUT4				
IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	1
0	1	0	0	1
0	1	0	1	1
0	1	1	0	1
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Standard gates

OR All to 0

Regular shape Invert



Properties				
3-bit LUT5				
IN3	IN2	IN1	IN0	OUT
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Standard gates

NOR All to 1

Regular shape Invert

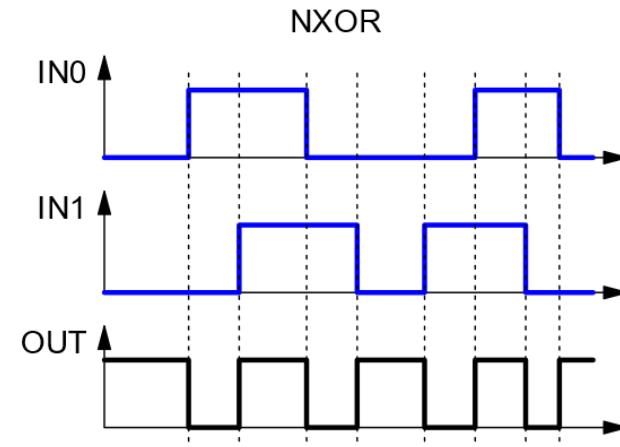
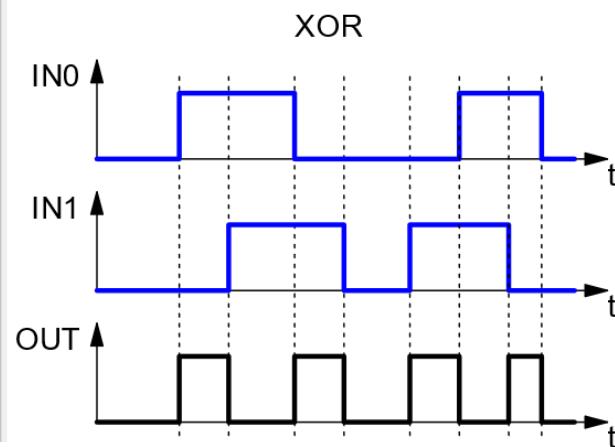
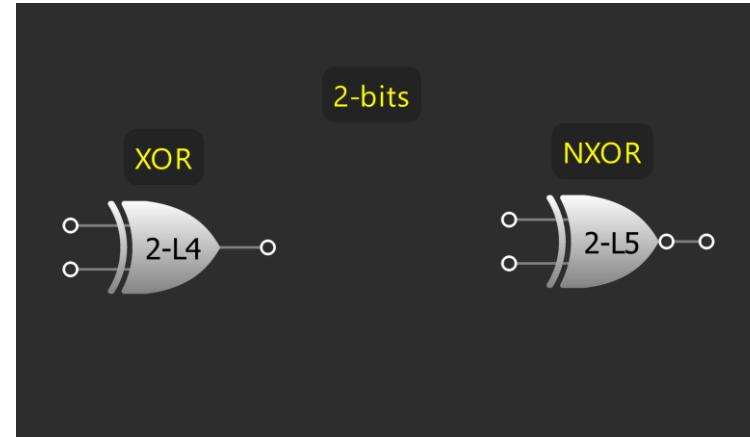
COMBINATIONAL LOGIC. STANDARD AND CUSTOMIZED MICROCELL

STANDARD LUTS (LOOK-UP TABLES)

Properties				
2-bit LUT4				
IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Standard gates

XOR All to 0
Regular shape All to 1
Invert



Properties				
2-bit LUT5				
IN3	IN2	IN1	IN0	OUT
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	0
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Standard gates

NXOR All to 0
Regular shape All to 1
Invert

COMBINATIONAL LOGIC. STANDARD AND CUSTOMIZED MICROCELL

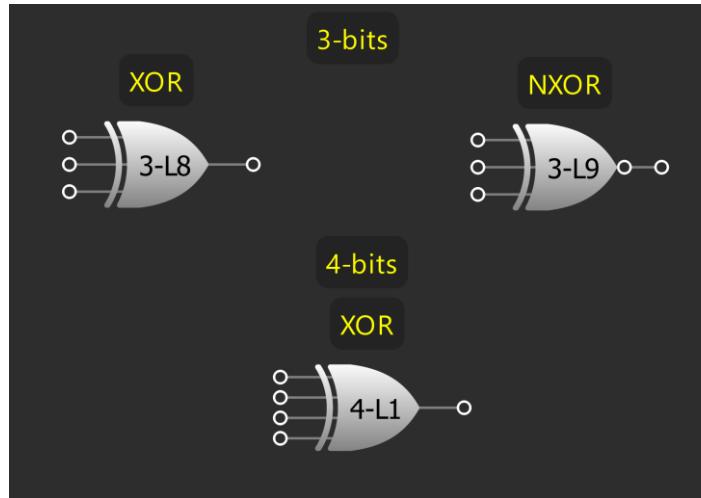
STANDARD LUTS (LOOK-UP TABLES)

Properties				
3-bit LUT8				
IN3	IN2	IN1	IN0	OUT
0	0	0	0	0
0	0	0	1	1
0	0	1	0	1
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	0
0	1	1	1	1
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Standard gates

XOR All to 0

Regular shape Invert



Properties				
3-bit LUT9				
IN3	IN2	IN1	IN0	OUT
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	1
0	1	0	0	0
0	1	0	1	1
0	1	1	0	1
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	0
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	0

Standard gates

NXOR All to 0

Regular shape Invert