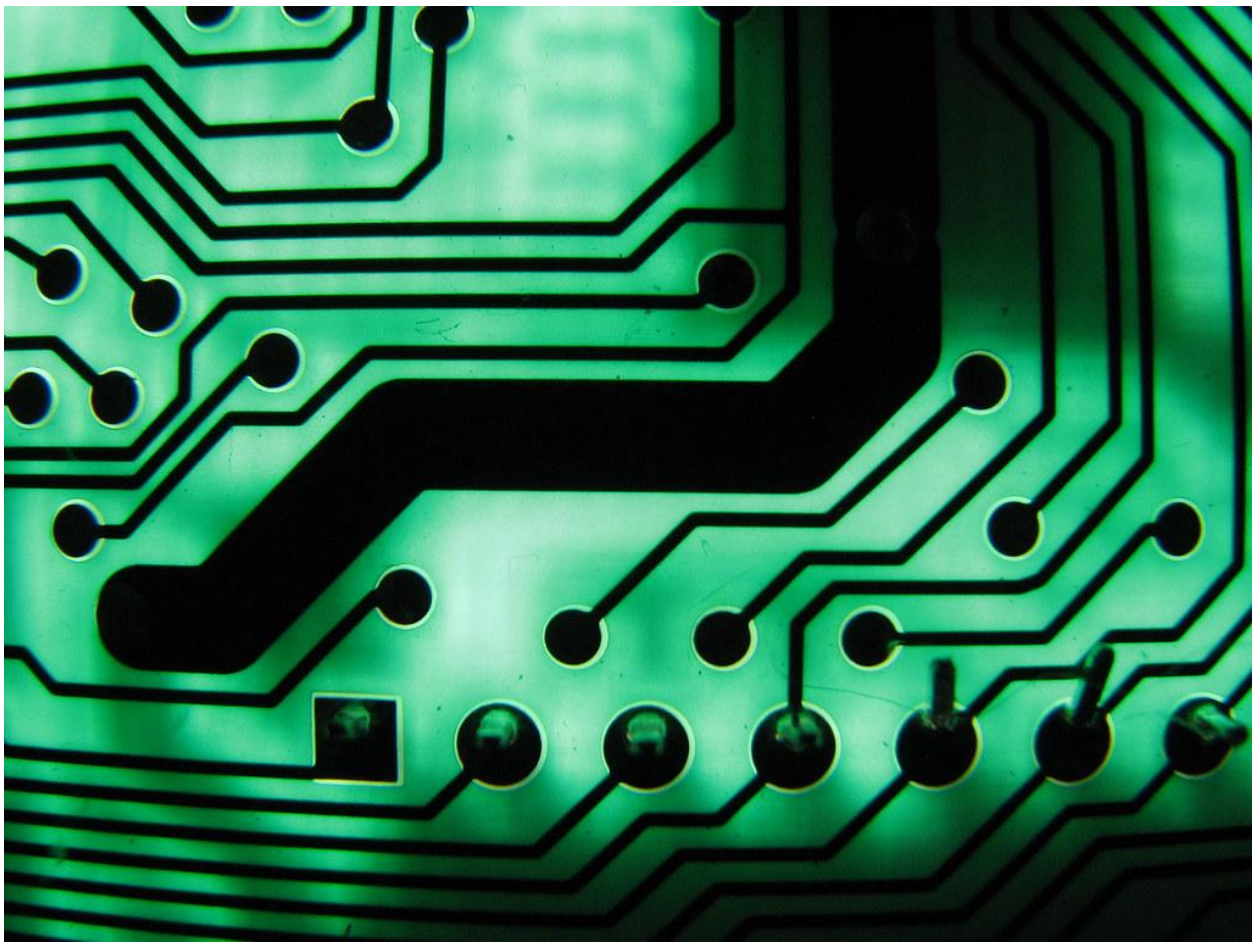
EEC 180 DIGITAL SYSTEMS II

Lab #2
Lab Report



Introduction

The purpose of this lab is to program an FPGA to do arithmetic and use the LCD display.

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Results

1 Prelab

Part 1.1 seg7.v Draft

```
//Verilog seg7.v module.
module seg7(bcd, seg);

     //Declare inputs, outputs, and internal variables.
     input [3:0] bcd;
     output [6:0] seg;
     reg [6:0] seg;

    //always block
    always @(bcd)
    Begin
        //case statement
        case (bcd)
            0 : seg = 7'b0000001;
            1 : seg = 7'b1001111;
            2 : seg = 7'b0010010;
            3 : seg = 7'b0000110;
            4 : seg = 7'b1001100;
            5 : seg = 7'b0100100;
            6 : seg = 7'b0100000;
            7 : seg = 7'b0001111;
            8 : seg = 7'b0000000;
            9 : seg = 7'b0000100;
            //if not a bcd number, switch off 7 segment display.
```

```
            default : seg = 7'b1111111;
        endcase
    end

endmodule
```

Figure 1.1.1 seg7.v Draft Code.

Part 1.2 fa.v Draft

```
//Verilog fa.v module.
module fa (in1, in2, cin, sum, cout);

      //Declare inputs, outputs, and internal variables.
      input in1,
            in2,
            cin;
      output sum,
            Cout;

      // use Boolean expressions
      assign Sum  = (in1 ^ in2) ^ cin;
      assign Cout = (in1 & in2) | (in2 & cin) | (cin & in1);
endmodule
```

Figure 1.2.1 fa.v Draft Code.

1.3 add4bit.v Draft

```
//Verilog add4bit.v module.
module add4bit(a,b,cin,sum,cout);

	//Declare inputs, outputs, and internal variables.
	input [3:0]a,b;
	input cin;
	output wire [3:0]sum;
	output cout;

	// instantiating four full-adder circuits - ripple carry
	fa FA1(a[0],b[0],cin,sum[0],cout1);
	fa FA2(a[1],b[1],cout1,sum[1],cout2);
	fa FA3(a[2],b[2],cout2,sum[2],cout3);
	fa FA4(a[3],b[3],cout3,sum[3],cout);
endmodule
```

Discussion

When we ...

Conclusion

We can see ...