UNIVERSITY OF CALIFORNIA—DAVIS

DEPARTMENT OF ELECTRICAL AND COMPUTER ENGINEERING

EEC180 — DIGITAL SYSTEMS II — WINTER 2023

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HOMEWORK 1

1.

```
module cubic(x,cube);
	input [9:0] x;
	output wire [0:0] cube;
	reg [0:0] cubex;

	// 0, 1, 8, 27, 64, 125, 216, 343, 512, 729, 1000
	always @(x)
	begin
		case (x)
			0 : cubex = 1'b1;
			1 : cubex = 1'b1;
			8 : cubex = 1'b1;
			27 : cubex = 1'b1;
			64 : cubex = 1'b1;
			125 : cubex = 1'b1;
			216 : cubex = 1'b1;
			343 : cubex = 1'b1;
			512 : cubex = 1'b1;
			729 : cubex = 1'b1;
			1000 : cubex = 1'b1;
			default: cubex = 1'b0;
		endcase
	end

	assign cube = cubex;

endmodule
```

2.

A.

```
module rev4case(x,y);
	input [3:0] x;
	output wire [3:0] y;
	reg [3:0] xcase;

	always @(x)
	begin
		case (x)
			4'b0001 : xcase = 4'b1000;
			4'b0010 : xcase = 4'b0100;
			4'b0011 : xcase = 4'b1100;
			4'b0100 : xcase = 4'b0010;
			4'b0101 : xcase = 4'b1010;
			4'b0111 : xcase = 4'b1110;
			4'b1000 : xcase = 4'b0001;
			4'b1010 : xcase = 4'b0101;
			4'b1011 : xcase = 4'b1101;
			4'b1100 : xcase = 4'b0011;
			4'b1101 : xcase = 4'b1011;
			4'b1110 : xcase = 4'b0111;
			default : xcase = x;
		endcase
	end

	assign y[3:0] = xcase[3:0];

endmodule
```

B.

```
module rev4assert(x,y);
	input [3:0] x;
	output wire [3:0] y;

	assign y[3:0] = {x[0],x[1],x[2],x[3]};

endmodule
```

3.

```
module mult3(a,b,prod);

	input [2:0]a,b;
	output wire [5:0]prod;
	reg [5:0]accum;

	initial
		begin
			accum = 6'b000000;
			case (b)
				1 : accum = accum + a;
				2 : accum = accum + a + a;
				3 : accum = accum + a + a + a;
				4 : accum = accum + a + a + a + a;
				5 : accum = accum + a + a + a + a + a;
				6 : accum = accum + a + a + a + a + a + a;
				7 : accum = accum + a + a + a + a + a + a +a;
				default : accum = 6'b000000;
			endcase
		end

	assign prod = accum;

endmodule
```