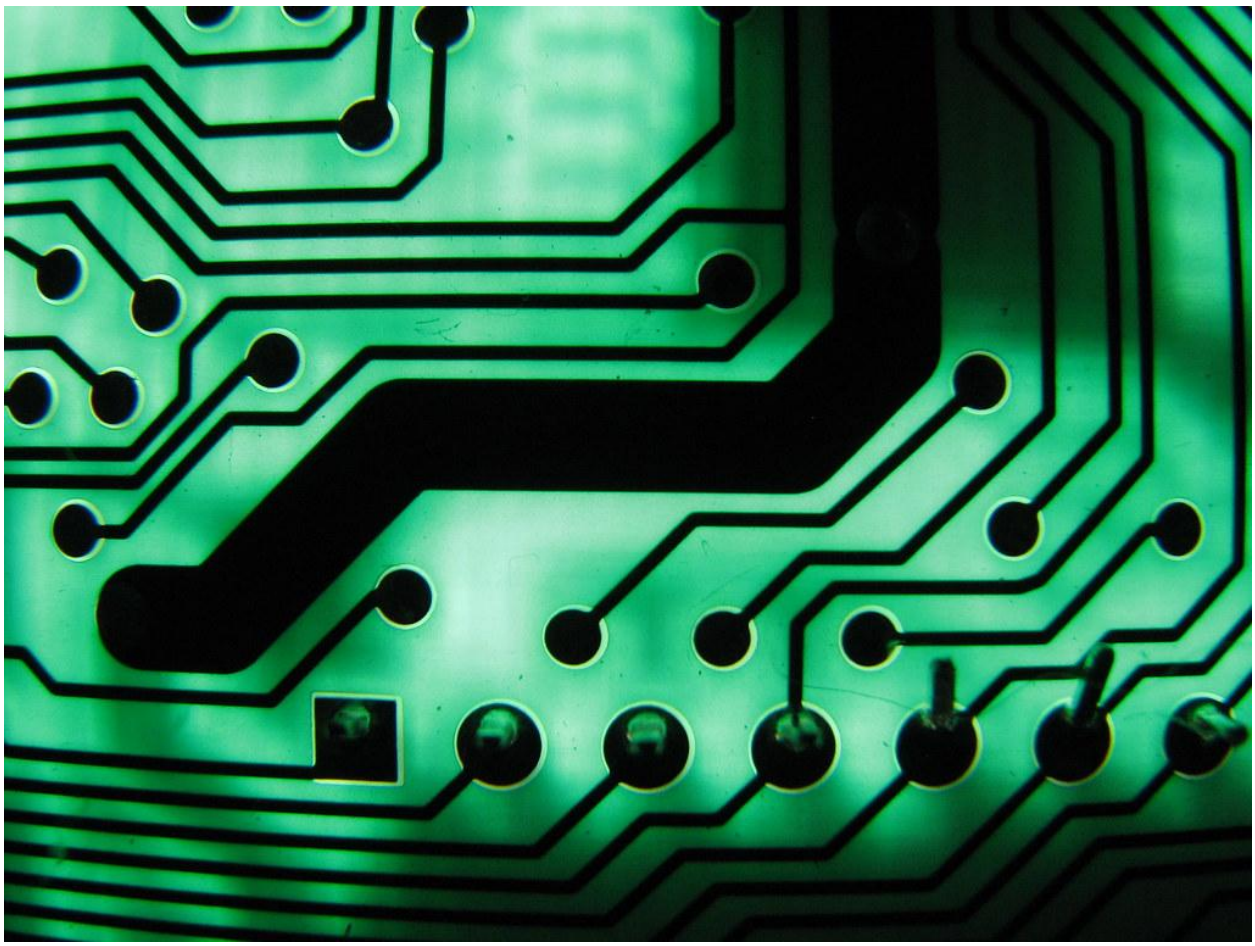
EEC 111 Digital Electronics

Lab #6

Lab Report



Introduction

The purpose of this lab is to simulate and experimentally characterize inverters based on integrated circuit PMOS and NMOS devices. We find that there are differences between transistors we design with these and discrete MOS components. These integrated circuit models, once tested, can be used to expand on CMOS digital logic design. If speed is considered, different design techniques should be considered to handle increased fan-in.

Tobin Joseph - Mohammad Linjawi

Results

1 CMOS Inverter Voltage Transfer Characteristics

Part 1.1 Inverter Circuit

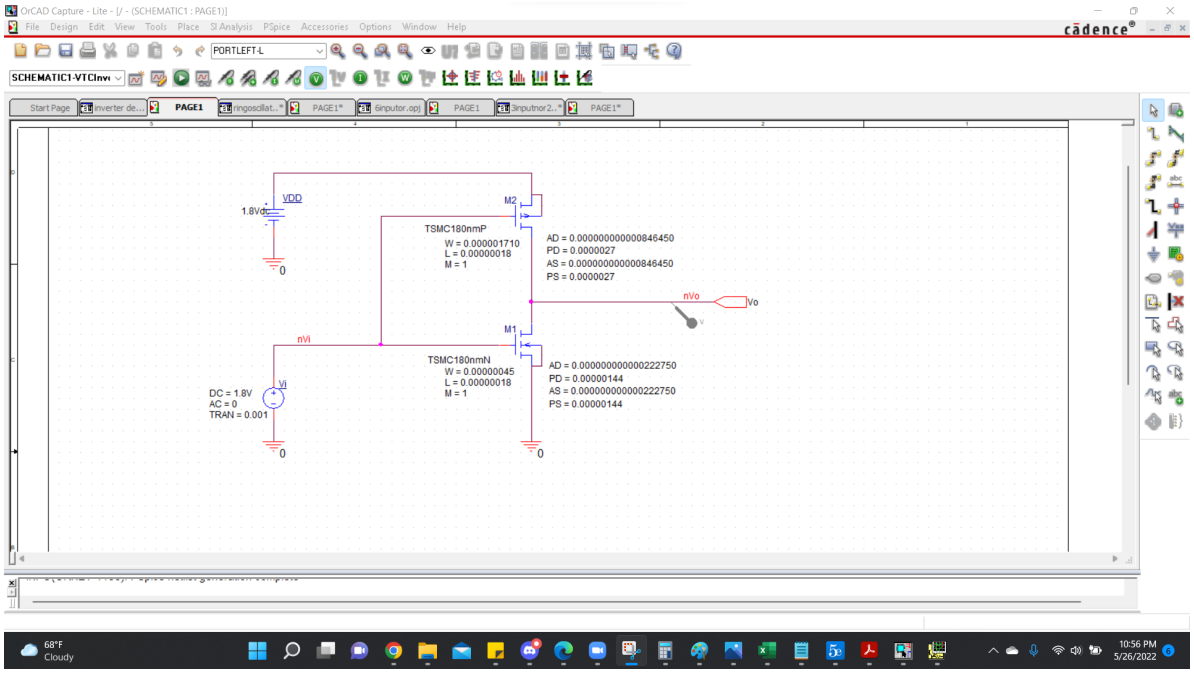


Figure 1.1.1 Screen capture of the schematic, and the date and time.

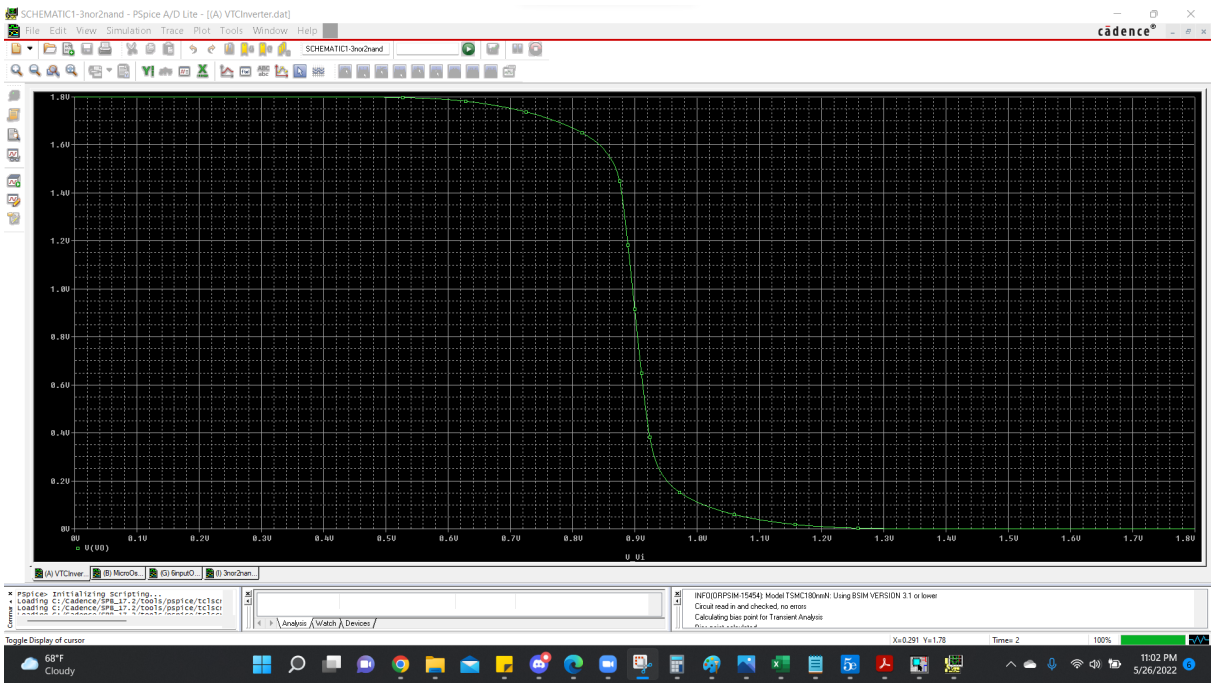


Figure 1.1.2 Simulation VTC

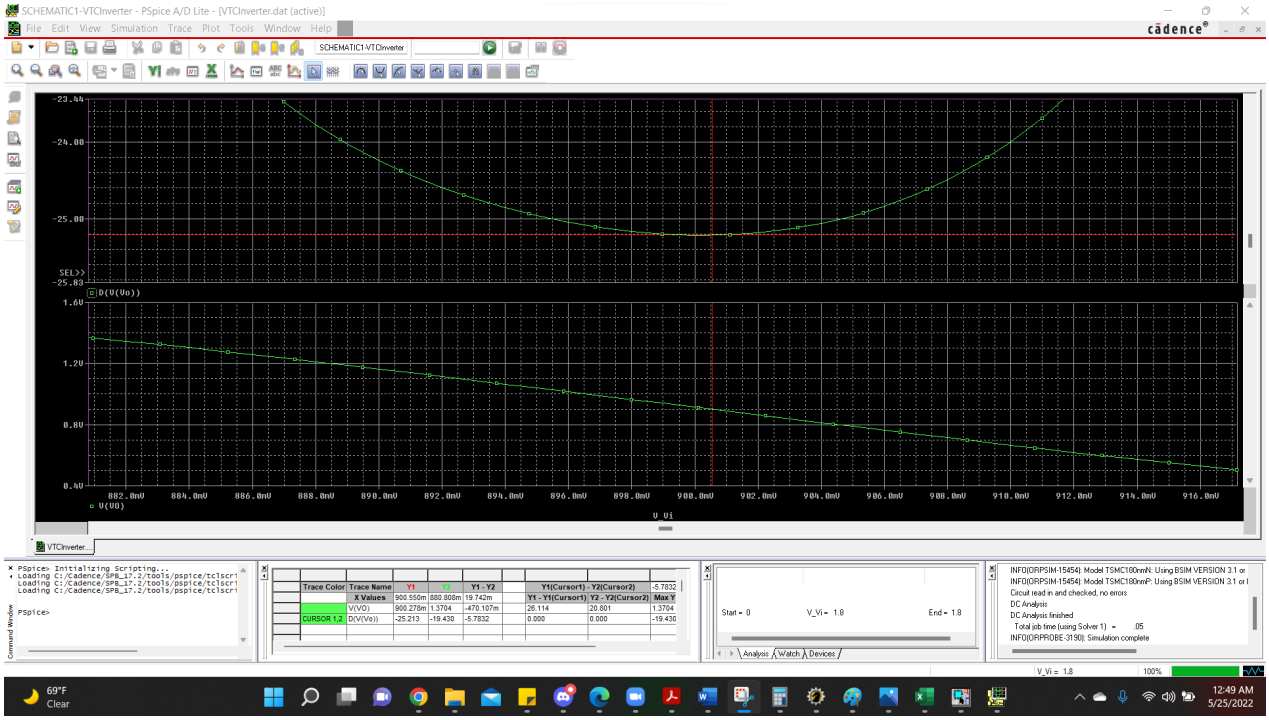


Figure 1.1.3 Measuring V_M

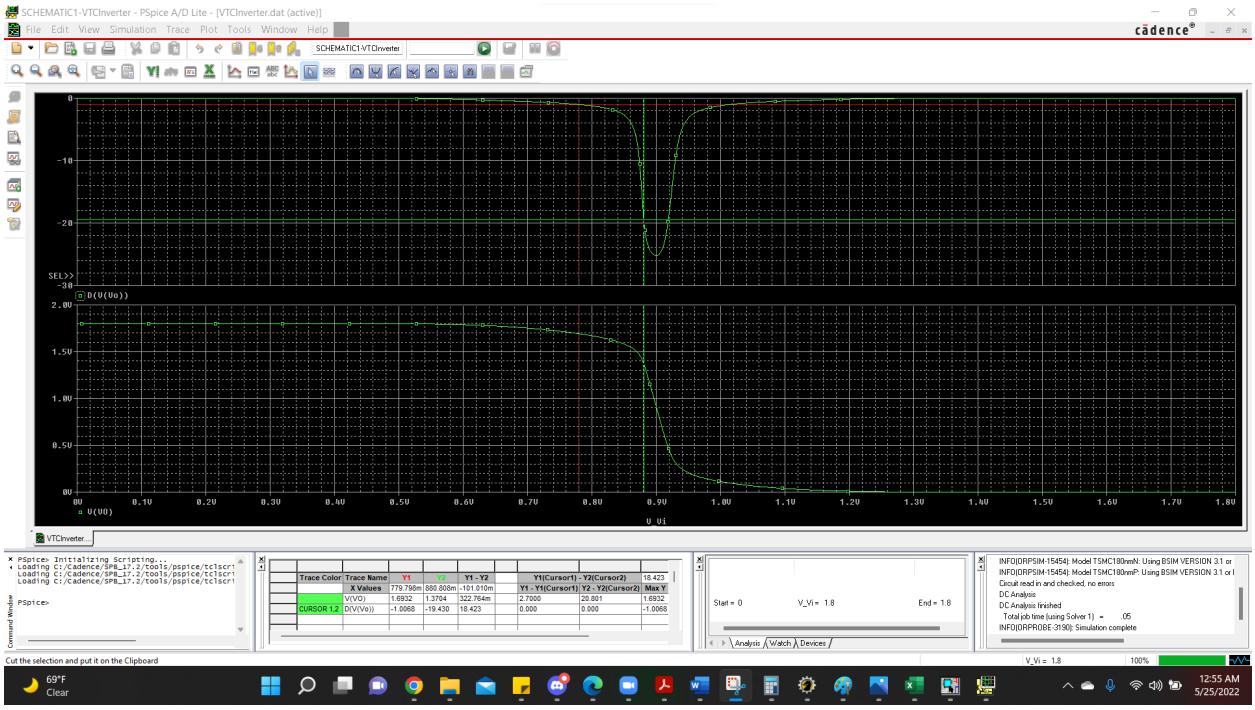


Figure 1.1.4 Measuring V_{IL}

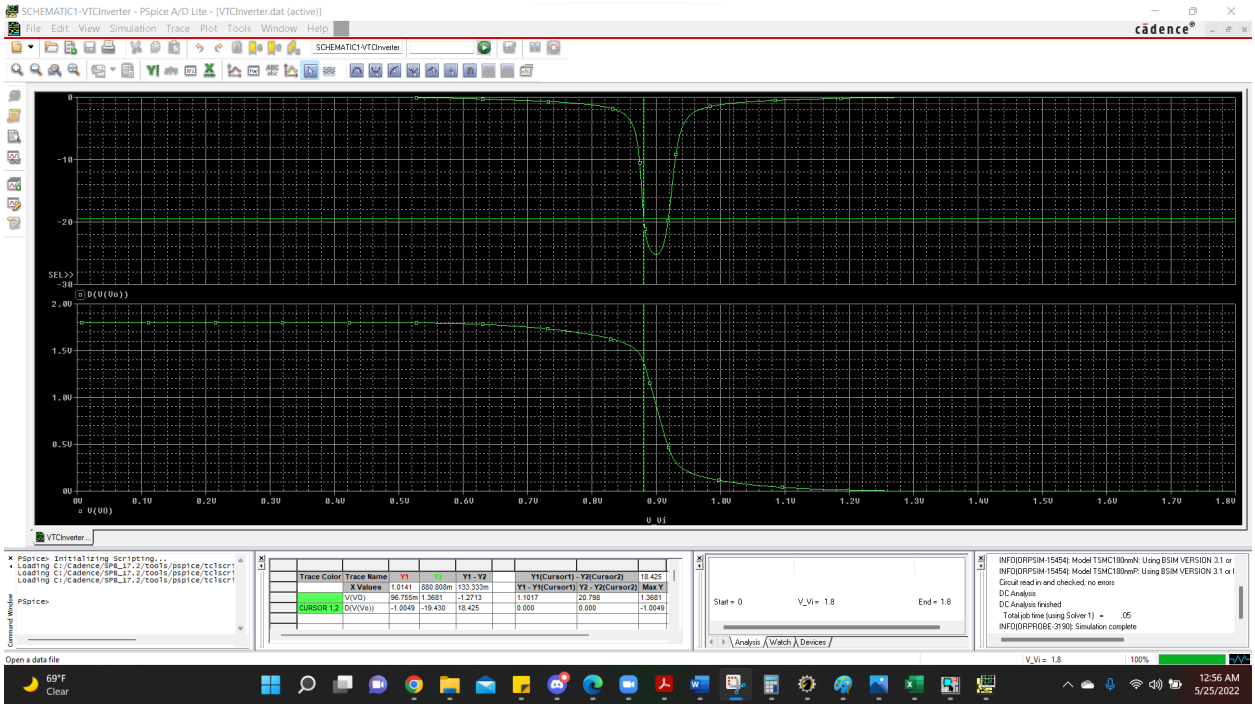


Figure 1.1.5 Measuring V_{IH}

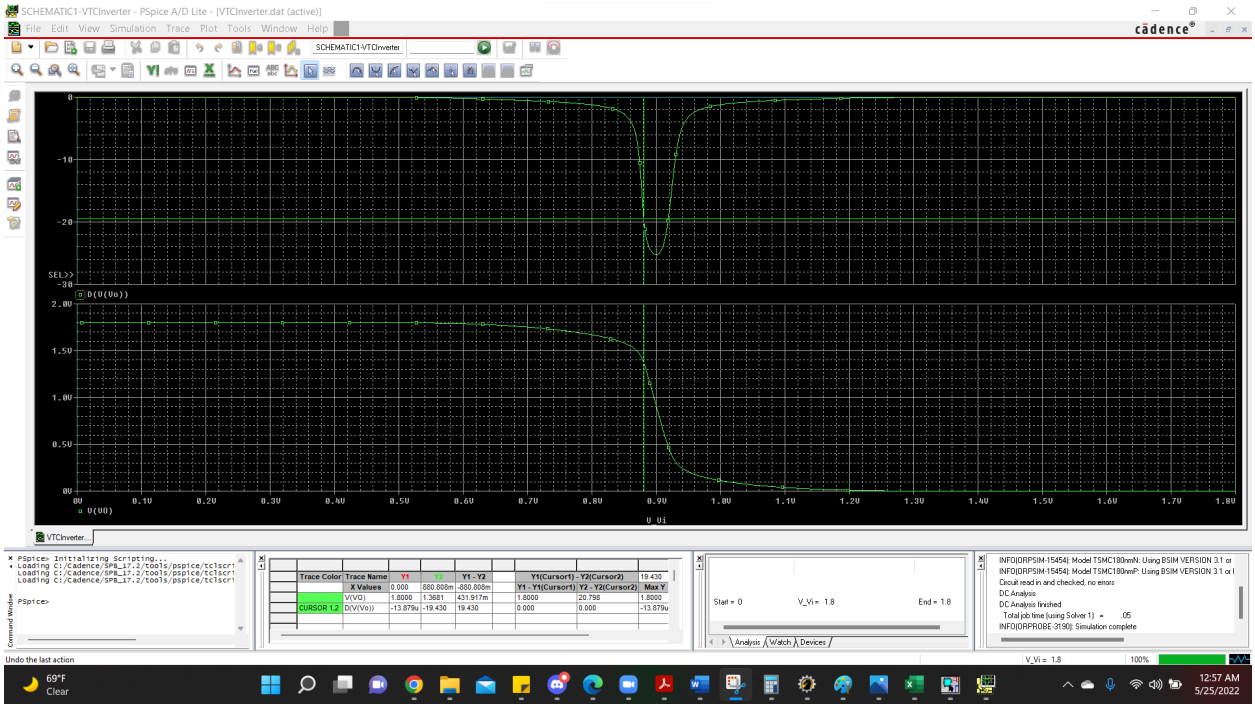


Figure 1.1.6 Measuring V_{OH}

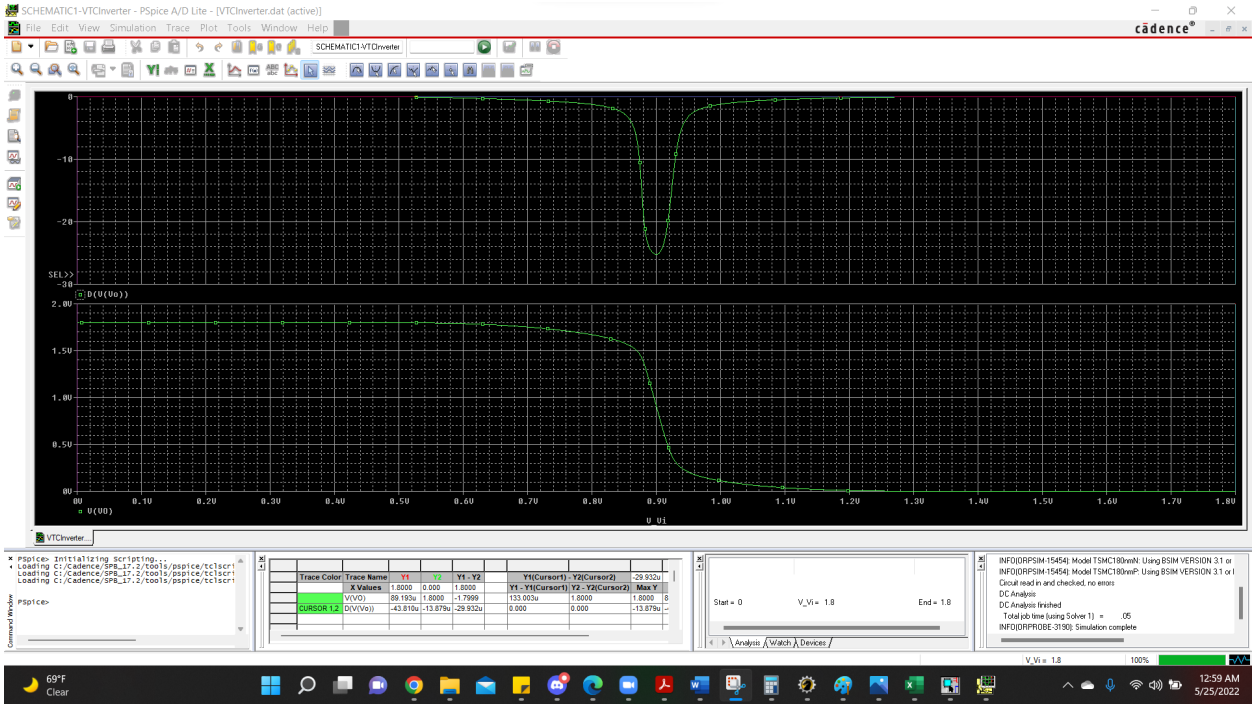


Figure 1.1.7 Measuring V_{OL}

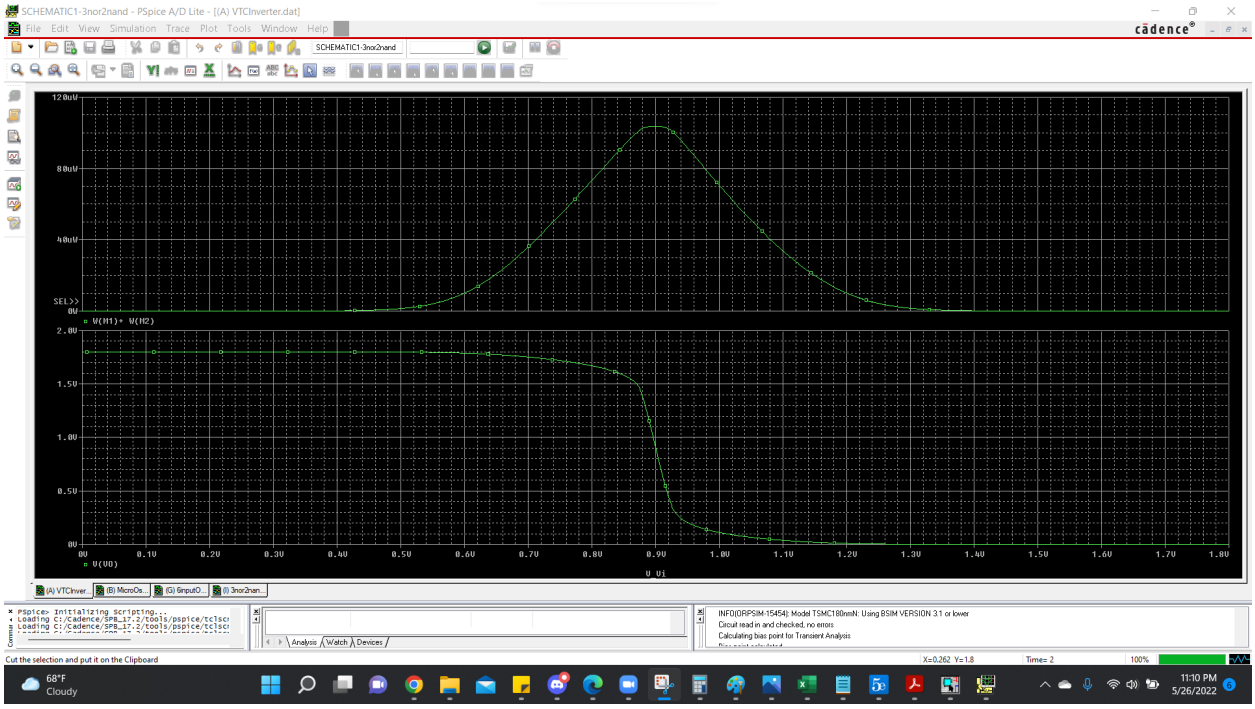


Figure 1.1.8 Measuring power function

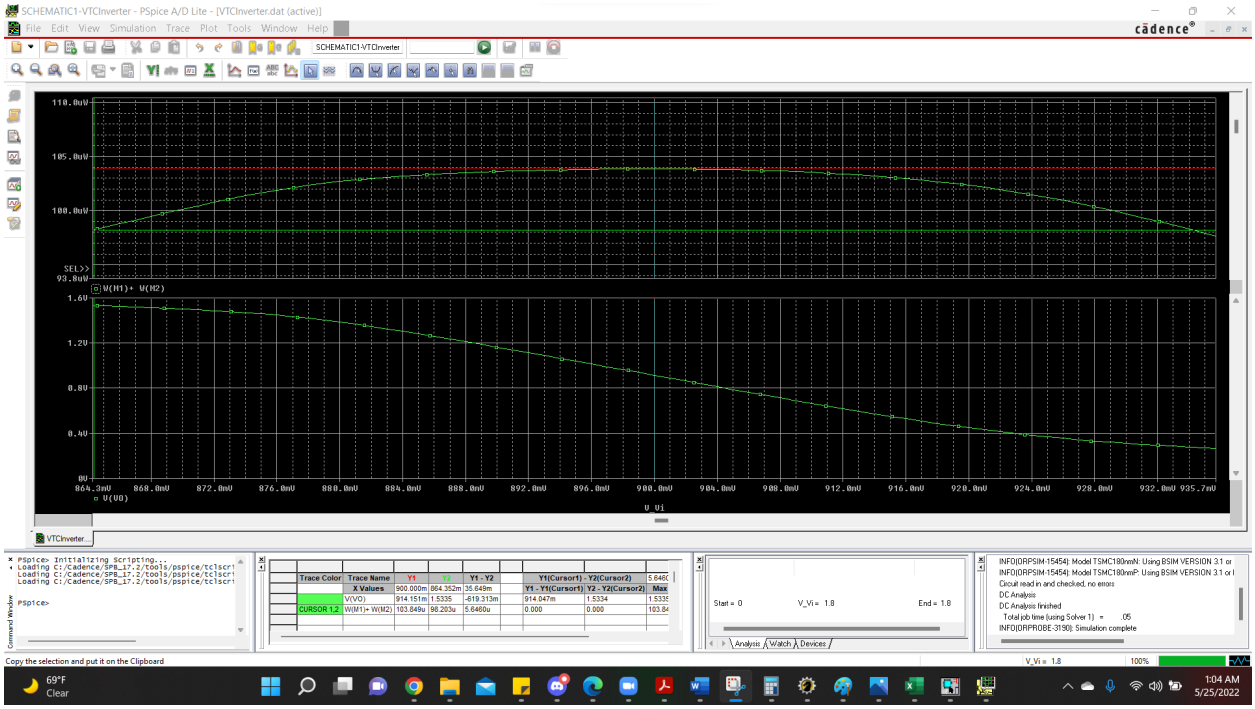


Figure 1.1.9 Measuring Peak Power

Parameter	Value
V_M	0.900 V
V_{OH}	1.800 V
V_{oL}	0.000 V
V_{IH}	1.014 V
V_{IL}	0.780 V
NM_H	0.786 V
NM_L	0.780 V
P_{peak}	0.104 mW

Table 1.1.1 Simulation measurements

2 Ring Oscillator

Part 2.1 Ring Oscillator Circuit

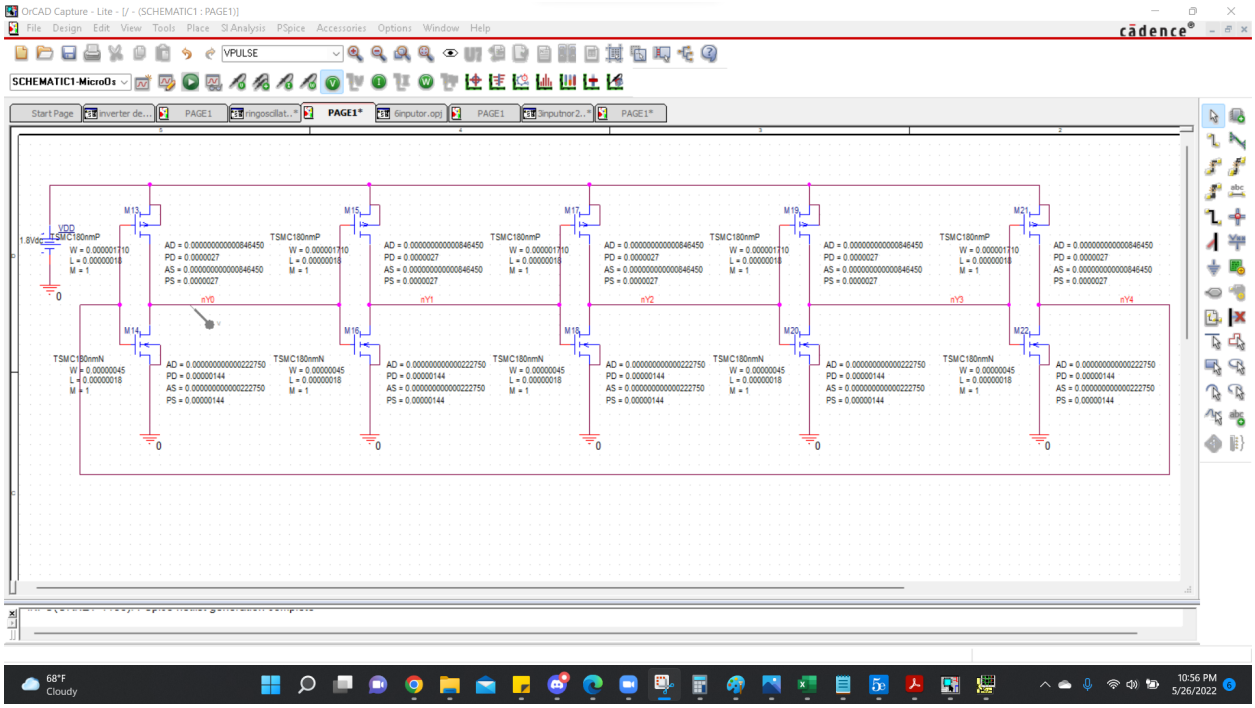


Figure 2.1.1 Ring Oscillator Circuit

Part 2.2 Ring Oscillator Circuit Simulation

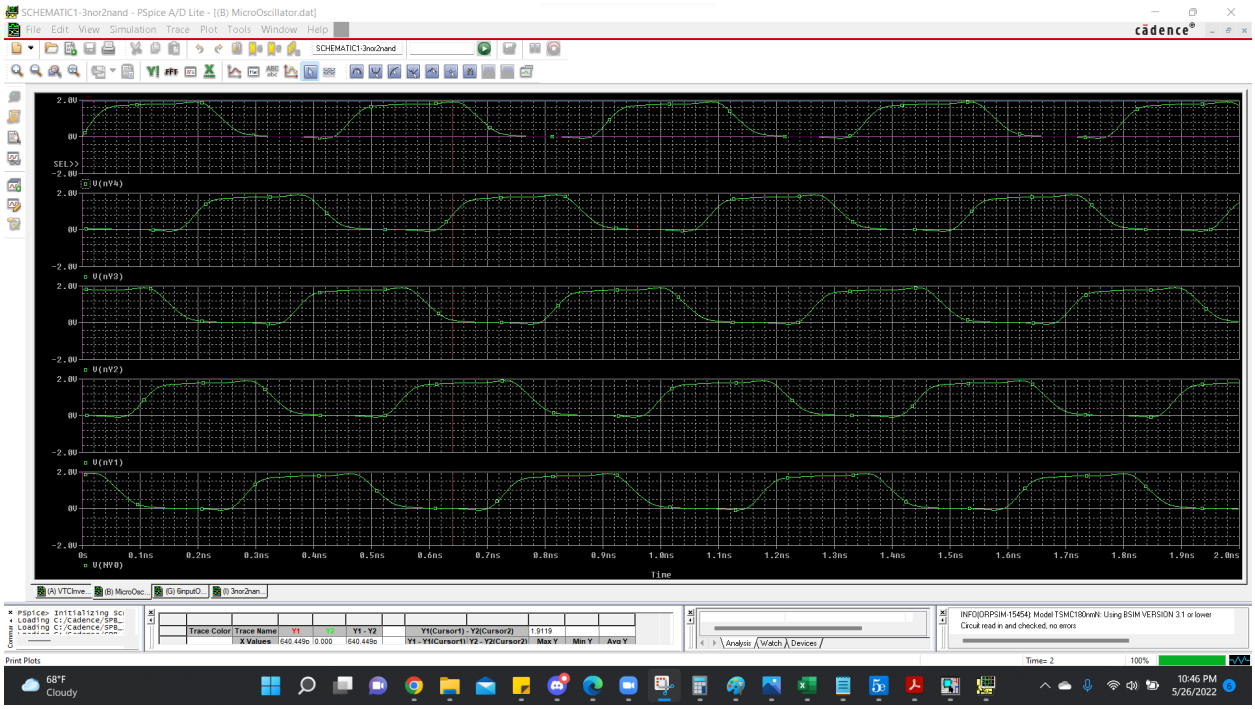


Figure 2.2.1 Ring Oscillator working

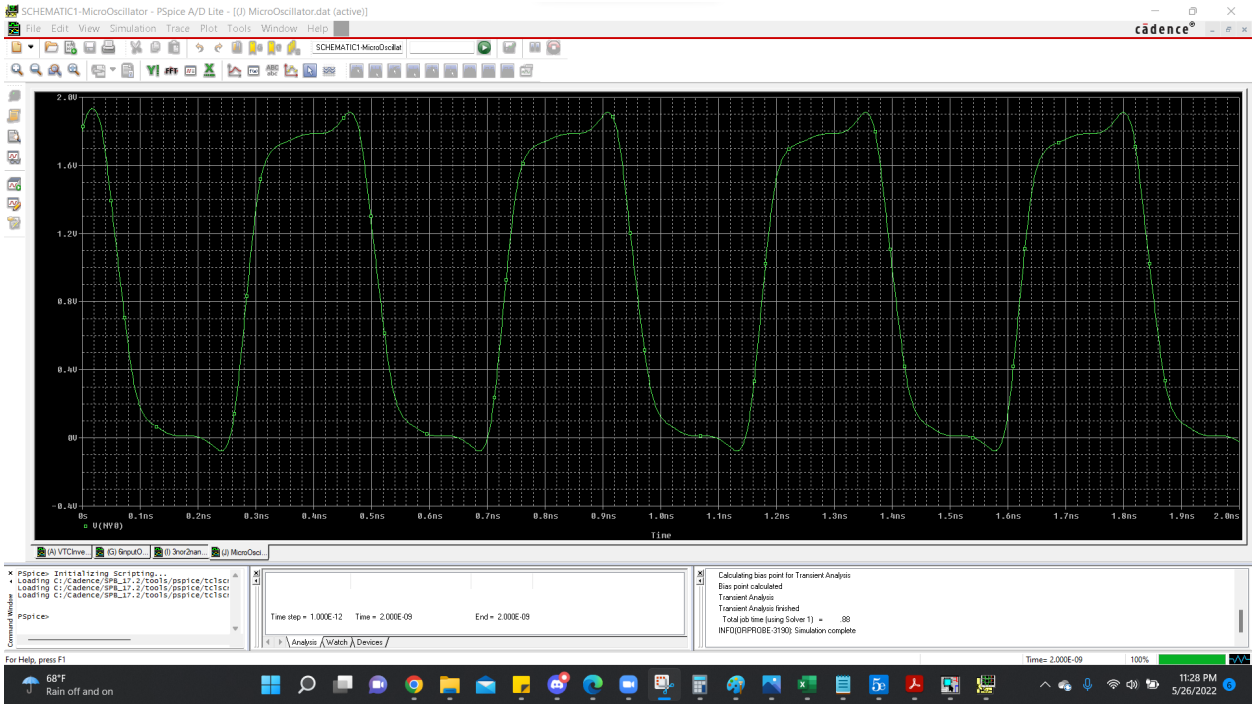


Figure 2.2.2 Measure t_r, t_f, t_{PHL}, t_{PLH}, and T.

Parameter	Value
t_r (t_{TLH})	52.31ps
t_f (t_{THL})	58.79ps
t_{PHL}	49.69ps
t_{PLH}	44.32ps
t_p	47.00ps
T	445ps

Table 2.2.1 Simulation measurements

Part 2.3 Ring Oscillator Circuit Experimentation

Figure 2.3.1 Measurement of real circuit signals

Parameter	Simulated Values	Experimental Values
t_r (t_{TLH})	52.31ps	1.321us
t_f (t_{THL})	58.79ps	1.137us
t_{PHL}	49.69ps	772.743ns
t_{PLH}	44.32ps	1.137us
t_p	47.00ps	0.945 us
T	445ps	7.051us

Table 2.3.1 Measurements comparison.

3 Ring Oscillator

Part 3.1 6 input OR Circuit

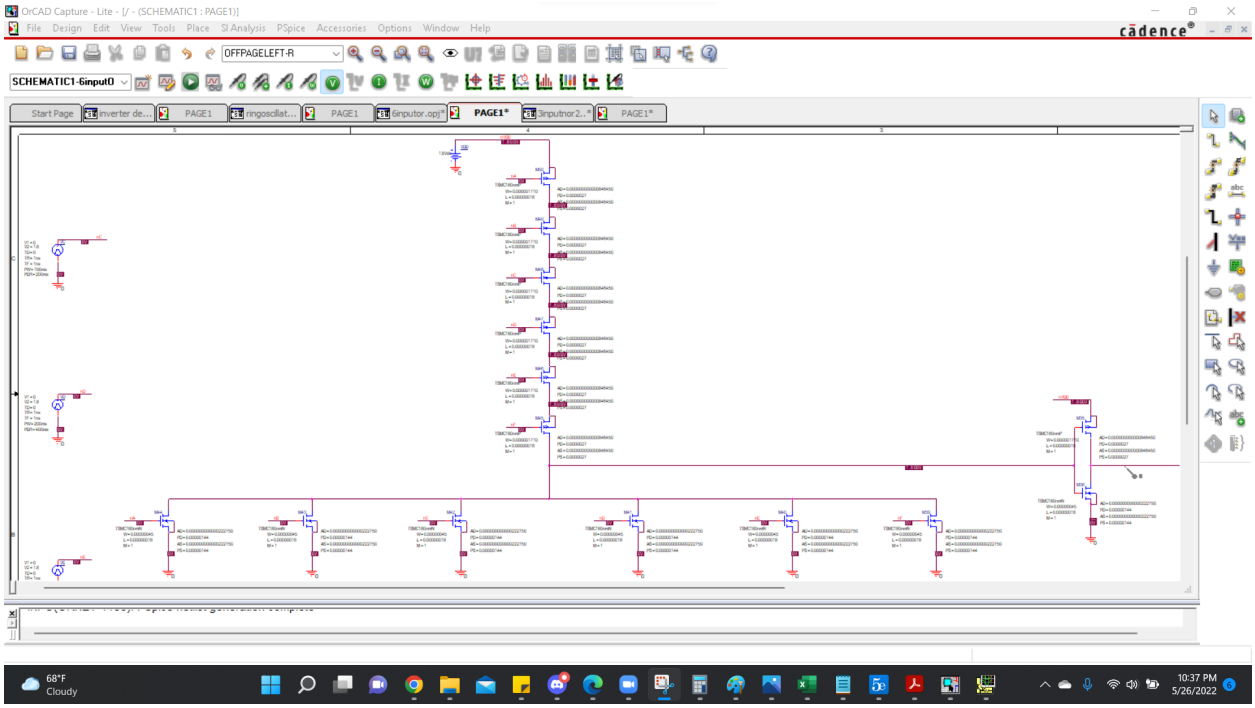


Figure 3.1.1 6 input OR circuit schematic

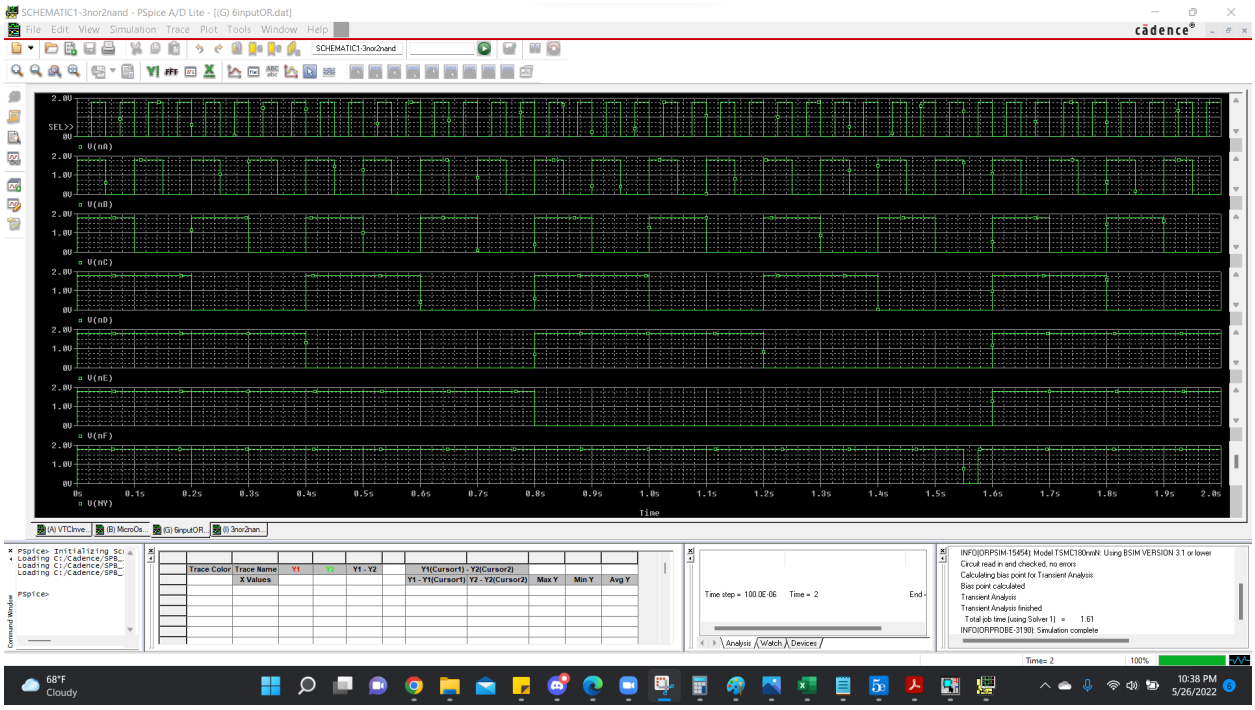


Figure 3.1.2 6 input OR circuit results

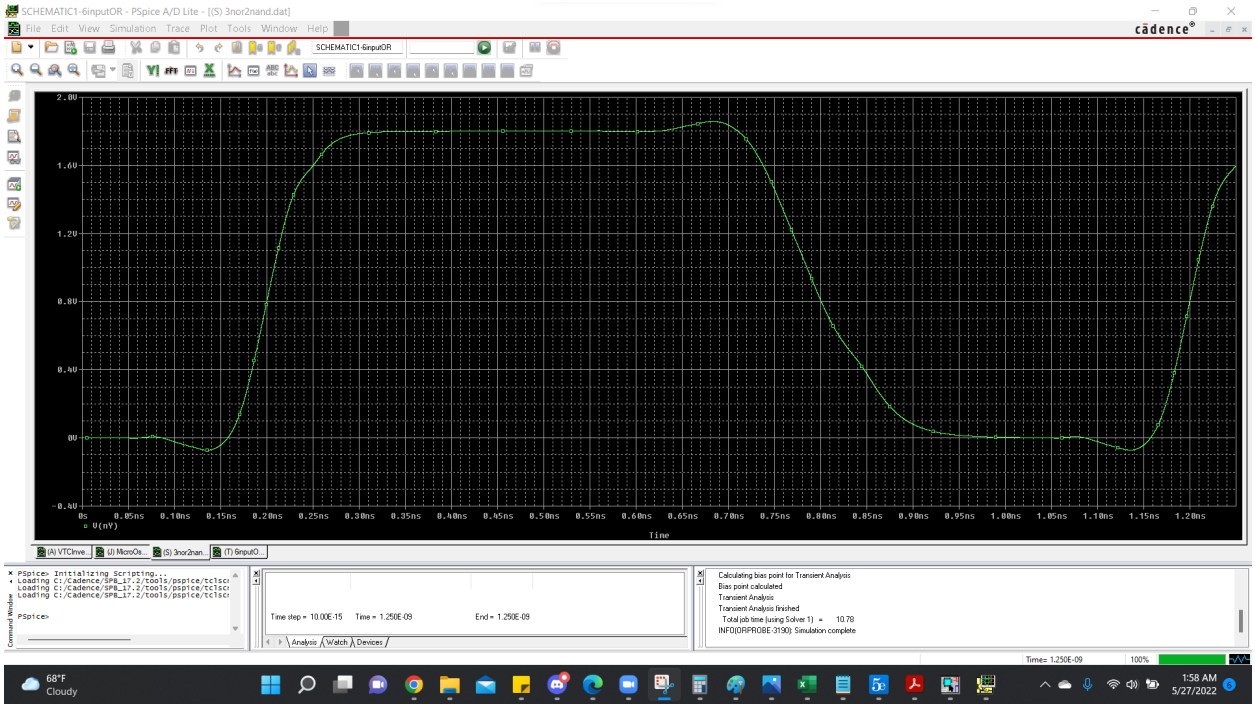


Figure 3.1.3 6 input OR circuit simulation to measure delays.

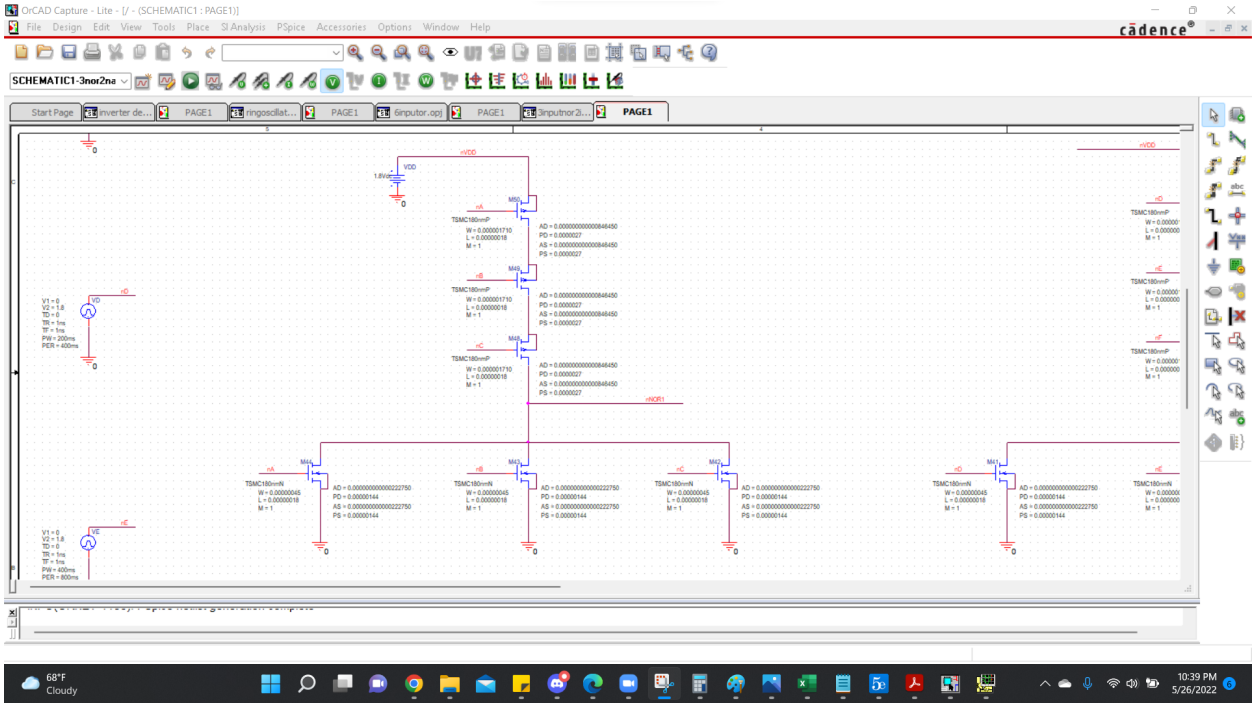


Figure 3.1.4 3 input NOR circuit schematic for 6 input OR implementation

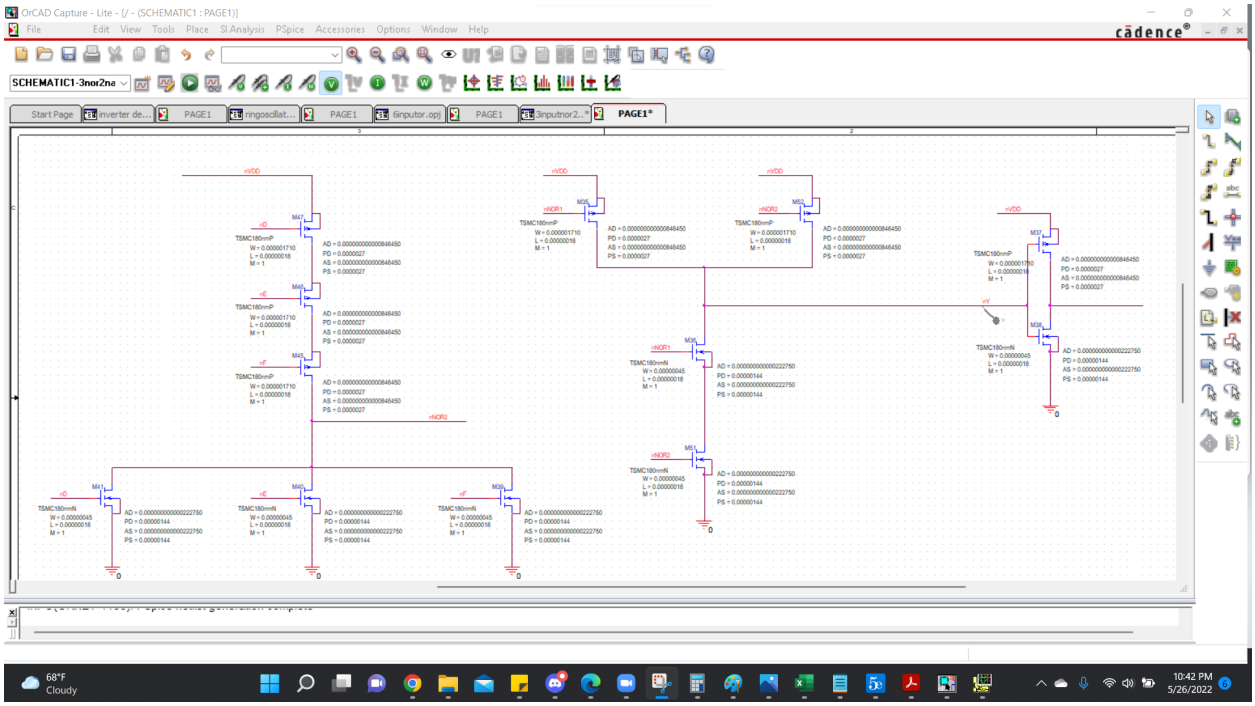


Figure 3.1.5 3 input NOR circuit with 2 input NAND circuit schematic for 6 input OR implementation

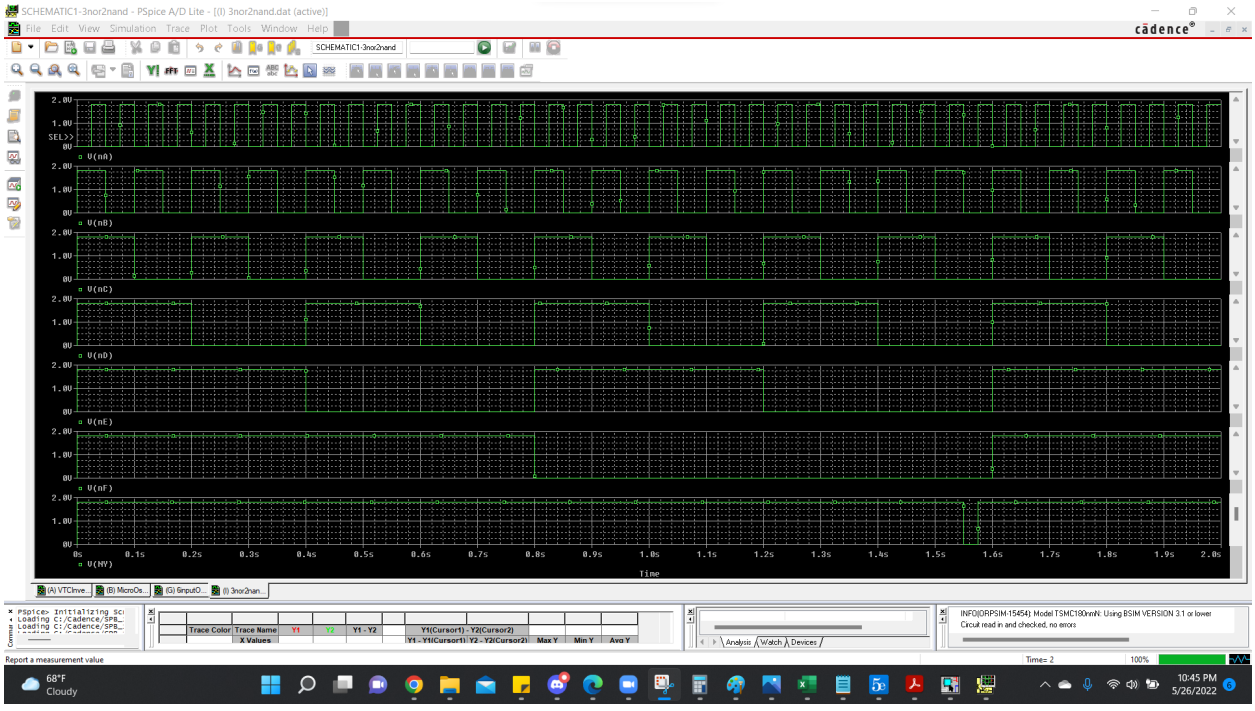


Figure 3.1.6 2 x 3 input NOR circuit results, 1 x 2input NAND - 6 input OR implementation results

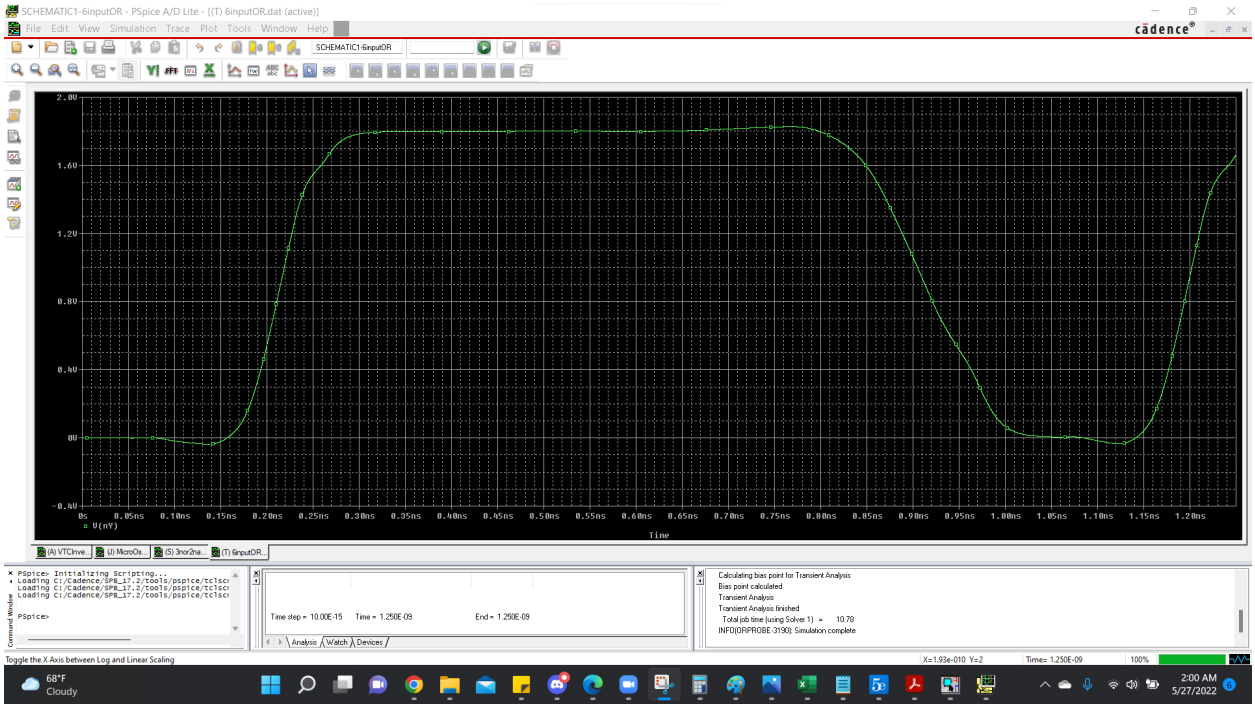


Figure 3.1.7 2 x 3 input NOR, 1 x 2 input NAND - 6 input OR circuit simulation to measure delays.

Parameter	6 input OR	2 x 3 input NOR, 1 x 2 input NAND - 6 input OR
t_r (t_{TLH})	81.15ps	80.28ps
t_f (t_{THL})	137.32ps	140.14ps
t_{PHL}	135.76ps	107.95ps
t_{PLH}	79.01ps	68.76ps
t_p	107.39ps	88.35ps

Table 3.1.1 6 input OR gate implementation measurements

Discussion

When we compare the value we designed for the V_M on the VTC with the values obtained from the simulation we find that they match up to two significant digits. As we did an iterative design process changing the parameters to meet the design requirements, we were able to get the V_M at the $V_{DD}/2$ specification. The power peak is basically at V_M, which we expected as it is the point of transference between the two transistors.

On the ring oscillator, we have the period T that is almost 10 times t_p. This makes sense as we have 5 stages and for each period we need 2 delays, one when the signal goes from low to high and another when the signal goes high to low. Each inverter will take on average t_p to provide output according to an input change and then propagate it to the next inverter on the ring. When we build a ring oscillator using discrete MOS transistors we got different results in terms of scale. This is due to the differences in construction between the discrete and integrated circuit components, which give them different "physical" properties and thus different behavior. For instance, V_{DD} for the integrated circuit version is just 1.8 V whereas the minimum V_{DD} for the discrete component is 3V. It takes more time to charge the innate capacitors to a higher voltage, so this also contributes to the higher results for the actual circuit as compared to the simulated ones. The period T is just 7.5 times t_p. And the measured t_p is around 31 times the time specified on the datasheet. This might be due to the capacitance introduced by the connecting cables, connectors, power source, and measuring equipment.

For the CMOS digital designs, we did and simulated we found that the three gate implementation is somewhat faster than the one gate implementation. When we examine the critical paths that signal A has to go through in both cases, we found that the three gate implementation passes that signal through 5 transistors in series whereas the one gate implementation needed one more transistor to do the job. That extra transistor likely causes the extra delay that the one gate implementation shows.

Conclusion

The difference in parameters for discrete MOS devices and integrated circuit devices make them behave at different scales on voltages and speed. The integrated circuit versions work at lower voltages and have a faster response to signal changes. As we design for integrated circuits, compromises between the size of the devices to match properties between the complementary MOSFETS define the final behavior of the devices. Using these characteristics to resemble as close as possible an ideal inverter and using these in the design of more complex CMOS digital logic circuits allows us to get predictable results out of our designs. Designing CMOS digital gates, we see that sometimes a straight-up implementation just bringing up the fan-in of the circuit might not be the fastest implementation. By using multiple gates to chive the same logical operation, we might get a faster implementation by reducing the number of transistors in series that a signal has to pass through to affect a change in an output signal.