Lab 1 Report: 5-bit R-2R Ladder DAC

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Course: VLSI Design
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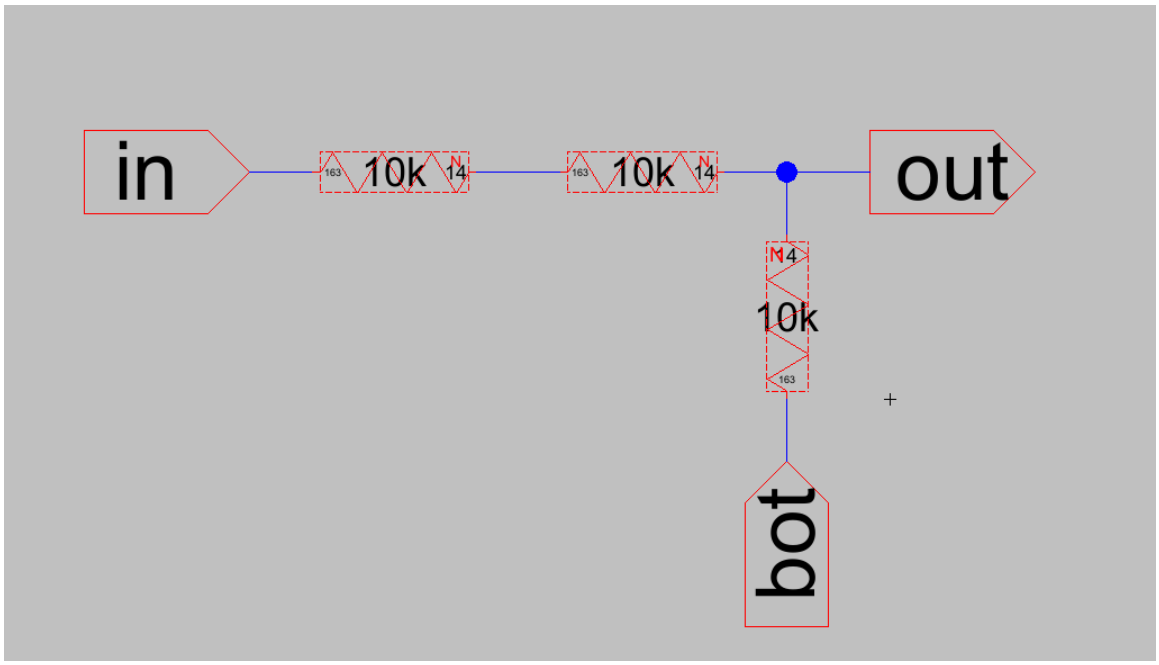
1. Introduction

The goal is to Design a 5-R2R Ladder Dac utilizing 10kΩ resistors in the Electric VLSI design software and preform simulations to confirm the functionality of the design. Then a physical layout can then be implemented using n-well resistors.

2. Schematic and Design

R_Divider Schematic

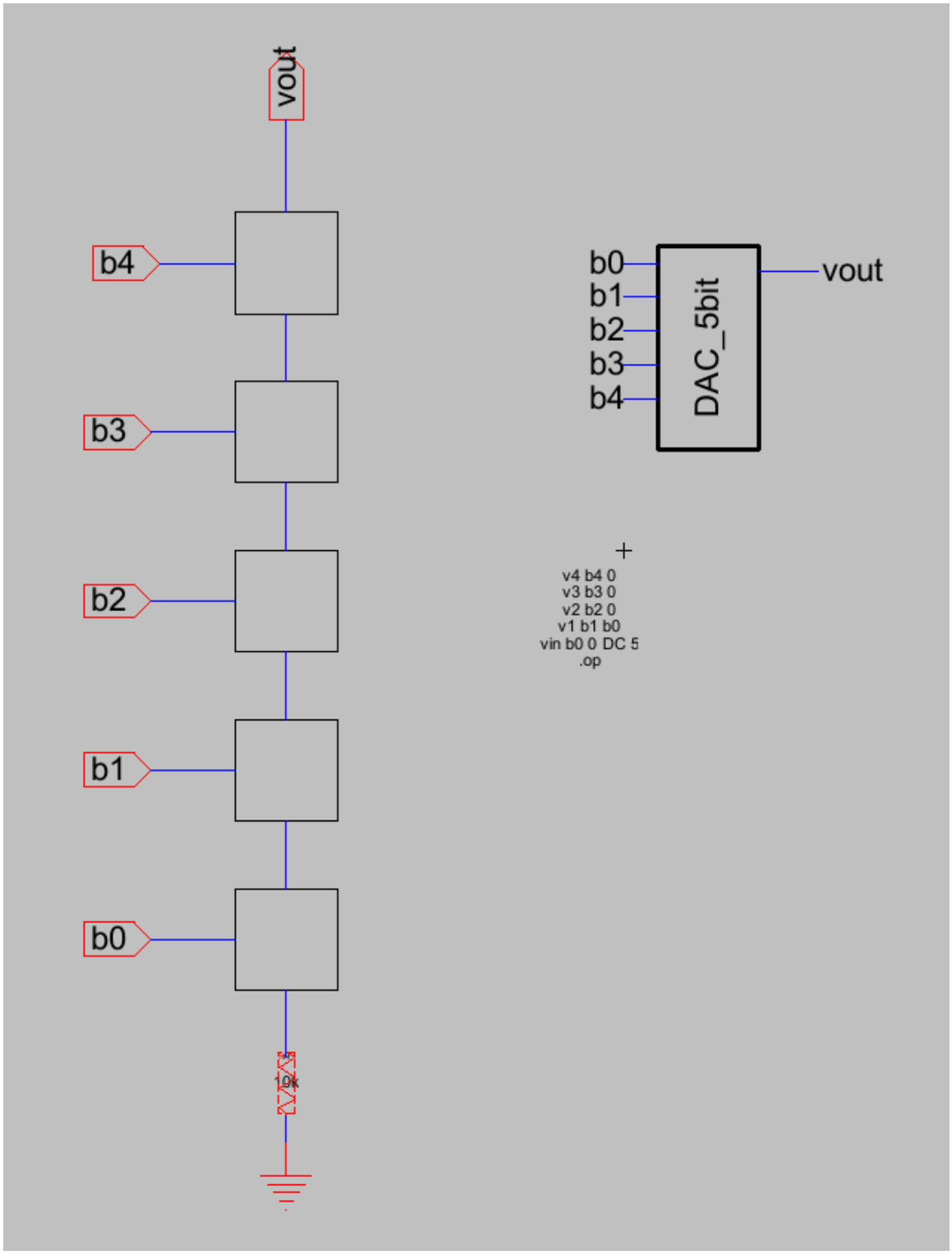


R_Divider Schematic Simulations

```
        --- Operating Point ---

V(vin):         1               voltage
V(vout):        0.333333        voltage
I(vin):         -3.33333e-05    device_current
Ix(xr_divide@1:bot):            -3.33333e-05    subckt_current
Ix(xr_divide@1:in):             3.33333e-05     subckt_current
Ix(xr_divide@1:out):            0               subckt_current
```

5-bit DAC Schematic



Using parallel and series reduction it can be found that the output resistance of the 5-bit DAC is roughly around 10kΩ.

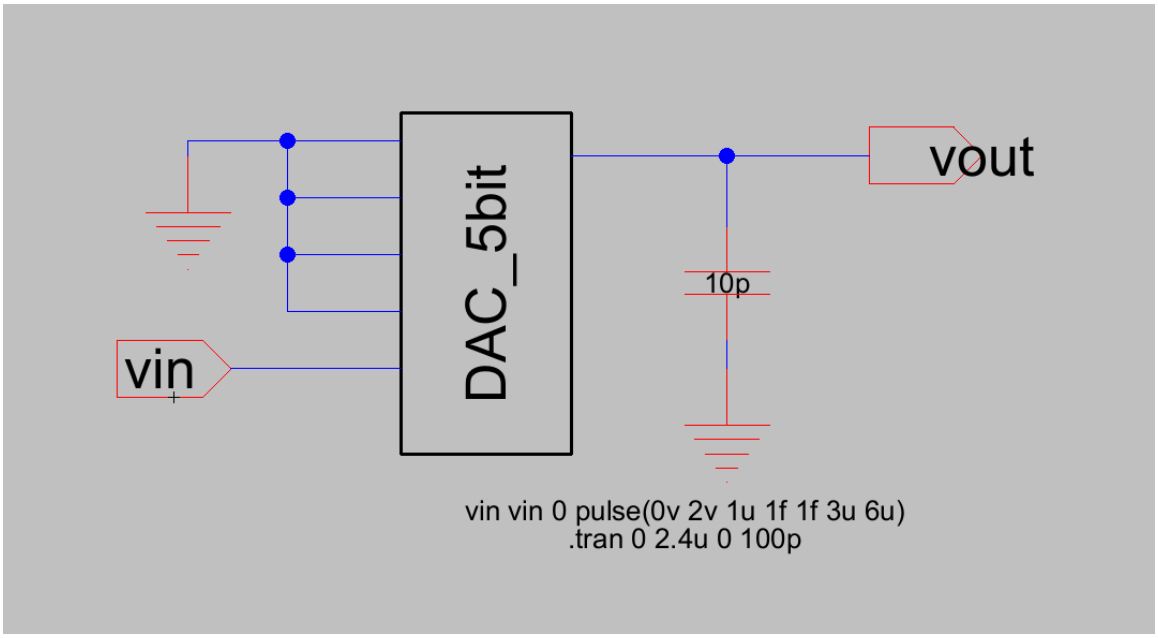
5-bit DAC Schematic Spice simulation

C:\Users\Jameson\Desktop\LAB1_VLSIDESIGN\DAC_5bit.spi

```
       --- Operating Point ---

V(b0):          5              voltage
V(b1):          5              voltage
V(b2):          0              voltage
V(b3):          0              voltage
V(b4):          0              voltage
V(net@0):       2.50977        voltage
V(net@1):       2.51953        voltage
V(net@11):      1.25488        voltage
V(net@2):       1.28906        voltage
V(net@3):       0.703125       voltage
V(vout):        0.46875        voltage
I(Rresnwell@0):                0.000125488    device_current
I(v1):          -0.000124023   device_current
I(v2):          6.44531e-05    device_current
I(v3):          3.51562e-05    device_current
I(v4):          2.34375e-05    device_current
I(vin):         -0.000248535   device_current
Ix(xr_divide@0:bot):           2.34375e-05    subckt_current
Ix(xr_divide@0:in):            -2.34375e-05   subckt_current
Ix(xr_divide@0:out):           0              subckt_current
Ix(xr_divide@1:bot):           5.85937e-05    subckt_current
Ix(xr_divide@1:in):            -3.51562e-05   subckt_current
Ix(xr_divide@1:out):           -2.34375e-05   subckt_current
Ix(xr_divide@2:bot):           0.000123047    subckt_current
Ix(xr_divide@2:in):            -6.44531e-05   subckt_current
Ix(xr_divide@2:out):           -5.85937e-05   subckt_current
Ix(xr_divide@3:bot):           -9.76563e-07   subckt_current
Ix(xr_divide@3:in):            0.000124023    subckt_current
```

Delay Analysis



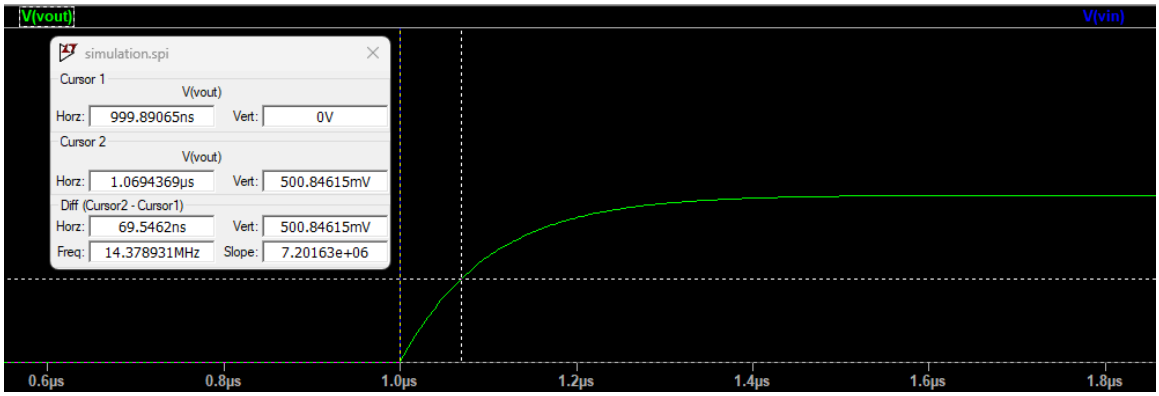
Theoretical Prediction

$$\tau = \mathrm{R_{out}} C_L$$

$$\tau = (10\mathrm{k\Omega})(10\mathrm{pF}) = 100ns$$

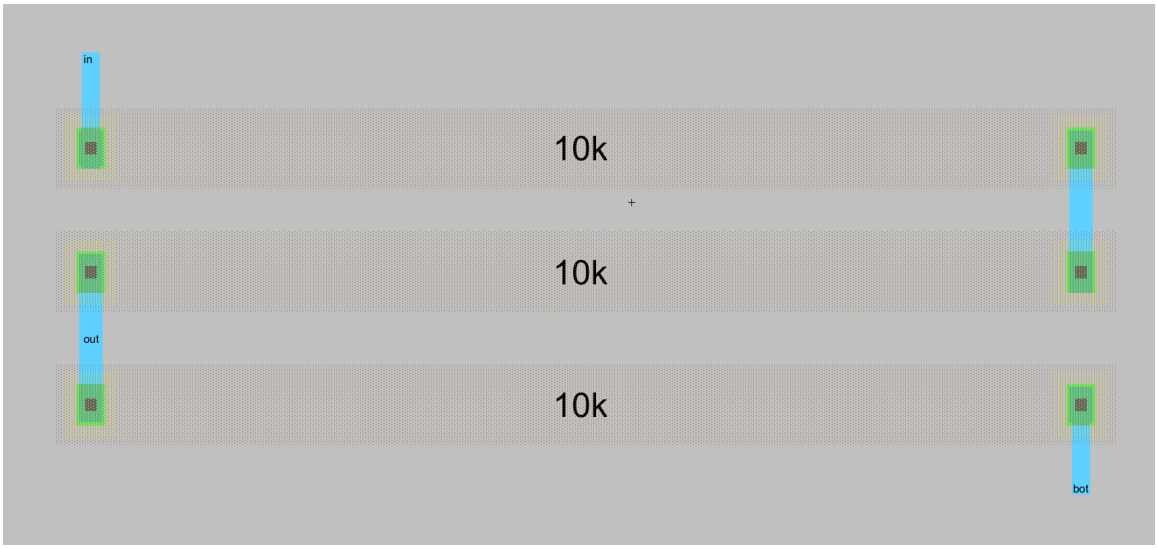
$$\tau 0.7 = (100\mathrm{ns})(0.7) = 70ns$$

Actual Analysis



3. Layout

R_Divider Layout



R_Divider Layout Simulation

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Ix(xr_divide@1:out):             0               subckt_current
```

N-Well Resistor Design

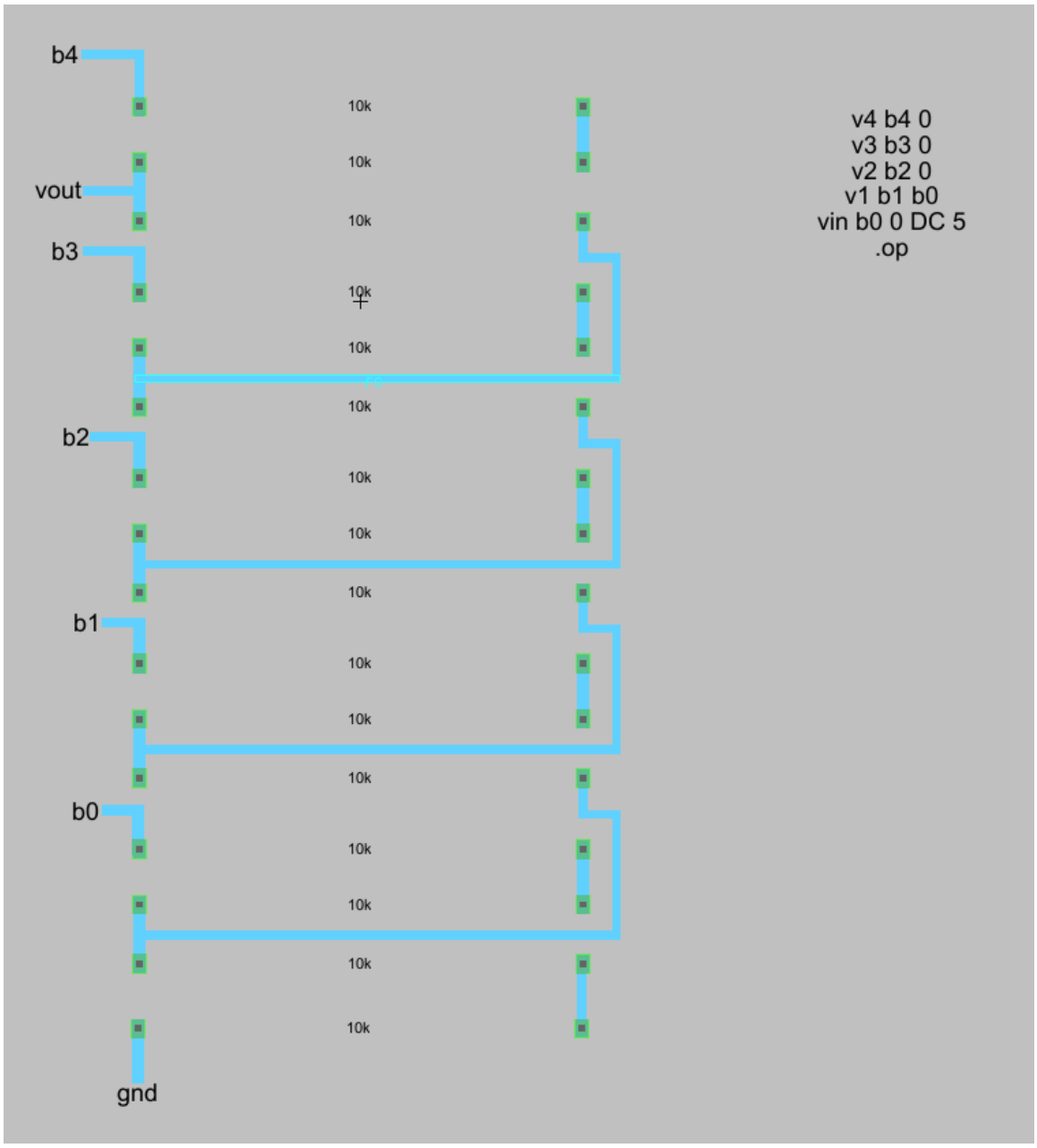
To find the dimensions required for a 10kΩ the equations $R = R_{sq} * \frac{L}{W}$ can be used knowing that $R_{sq} = 855 \frac{\Omega}{sq}$ and using a chosen width of 14 µm to find the length required for a 10kΩ n-well resistor.

$$R = R_{sq} * \frac{L}{W}$$

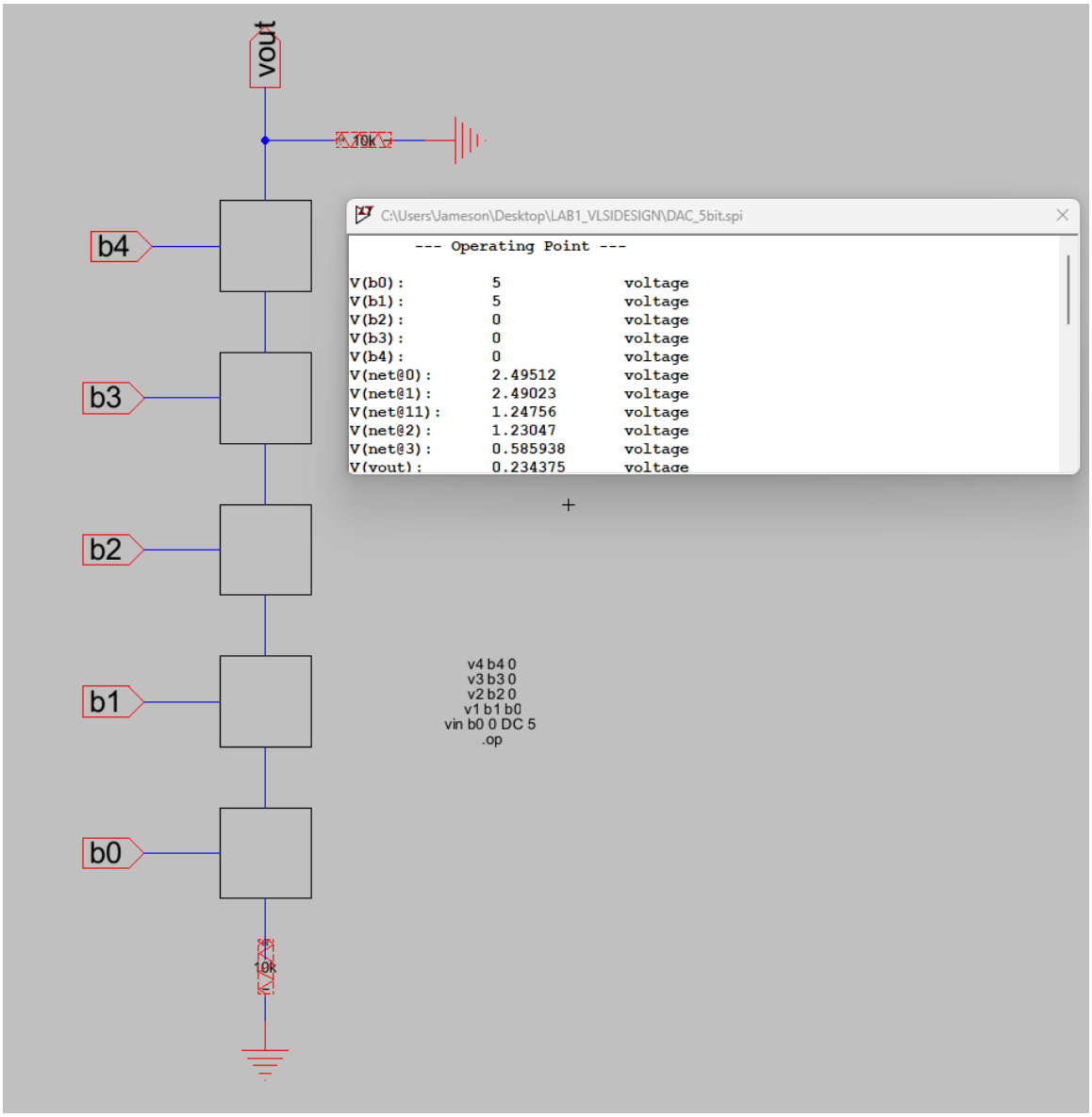
$$10k\Omega = 855 \frac{\Omega}{sq} * \frac{L}{14\mu m}$$

$$\frac{10k\Omega}{855\frac{\Omega}{sq}} * 14\mu m = L$$
$$L \approx 16$$

3.2 DAC Layout



DAC Driving a 10kΩ Load



When driving a 10kΩ load the output voltage is half the original amount. This is caused due to the output resistance of the DAC being 10kΩ causing the 10kΩ load to act like a voltage divider, using the formula of a voltage divider that can be confirmed.

$$V_{out} = V_{in}\left(\frac{R_2}{R_1 + R_2}\right)$$

$$entering\ in\ the\ values\ R_2 = 10k\Omega\ R_1 = 10k\Omega\ Vin$$

DRC & LVS Results

Passed DRC & LVS

References

Electric VLSI