Lab Report Template – Lab 3: Padframe Design with NMOS and ESD Protection

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Objective

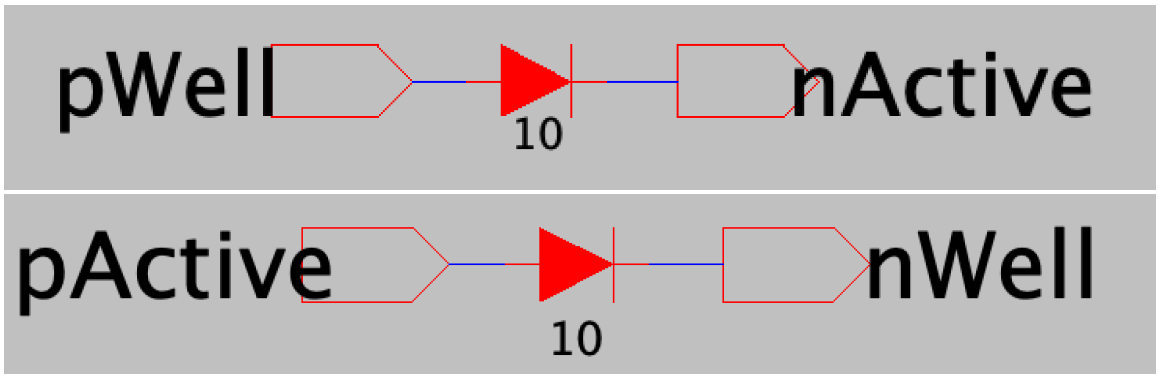
design a die that connects an NMOS transistor to the outside world with ESD protection.

Introduction

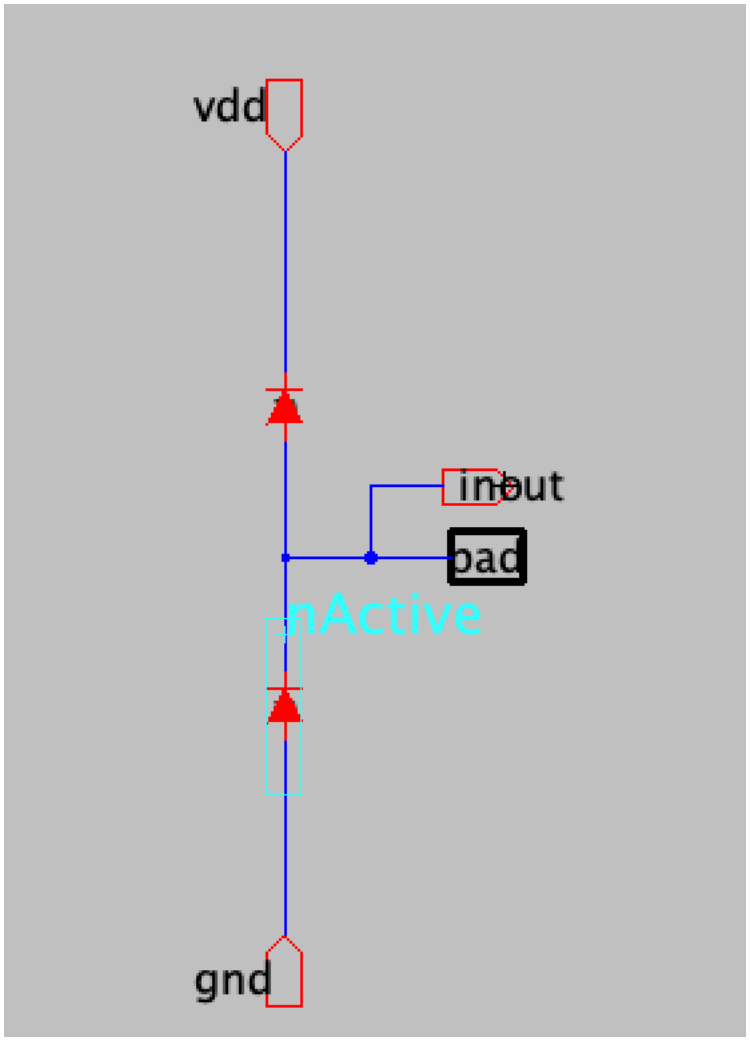
ESD protection is necessary to prevent overvoltage on one of the pads due to static electricity. The pad frame is required to allow the VLSI circuit to be implemented into an IC chip.

Part I – SCHEMATIC

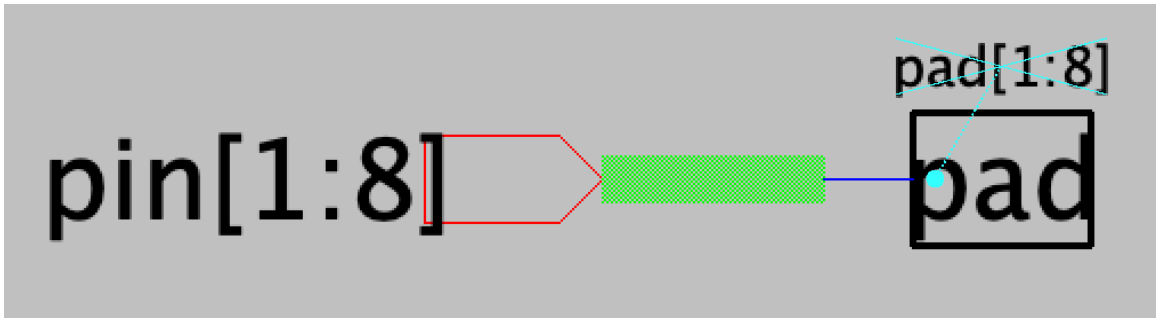
pWell-nActive and pActive-nWell Diodes



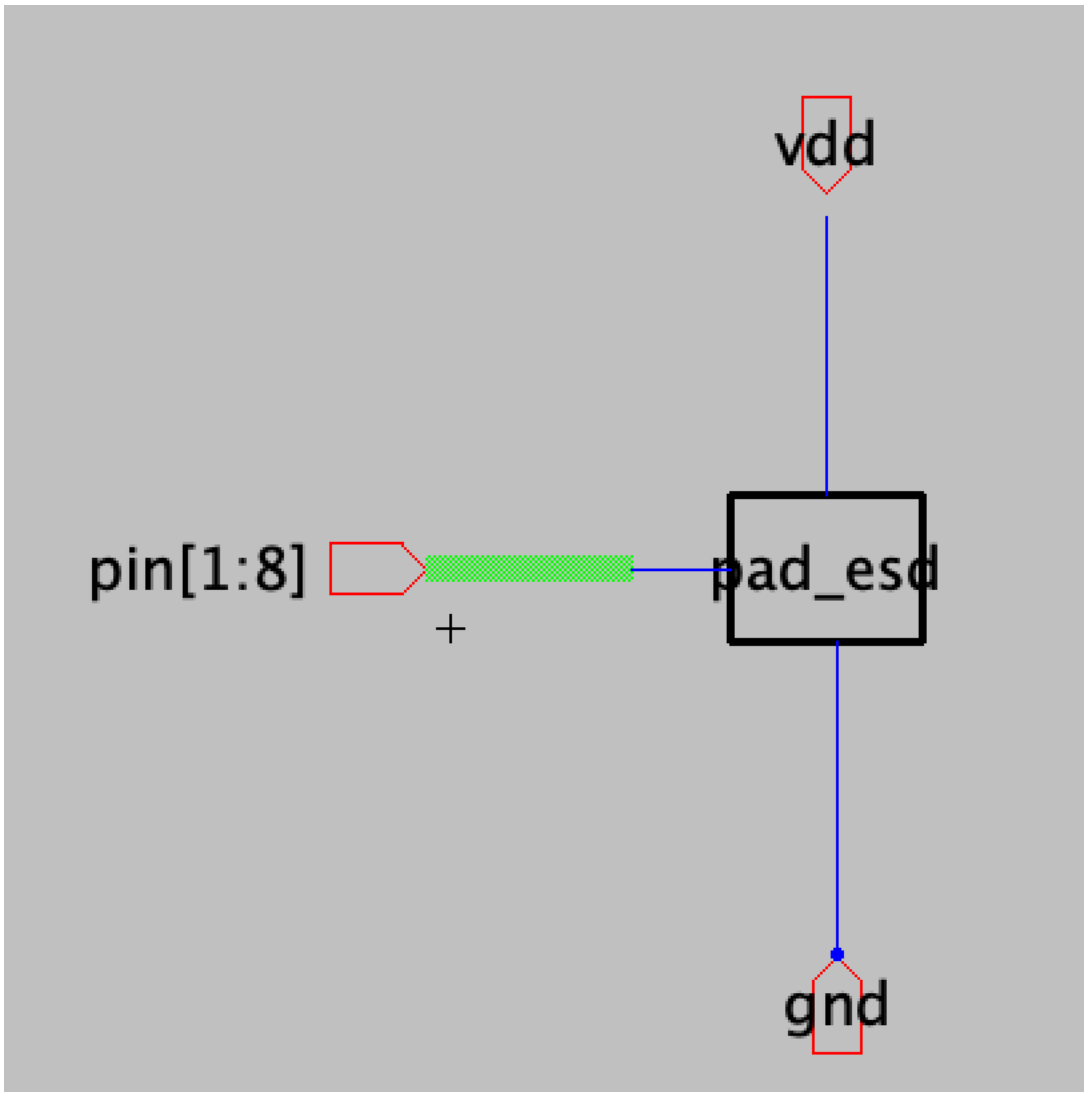
Pad Cell with ESD Protection



Padframe with VDD and GND Bus

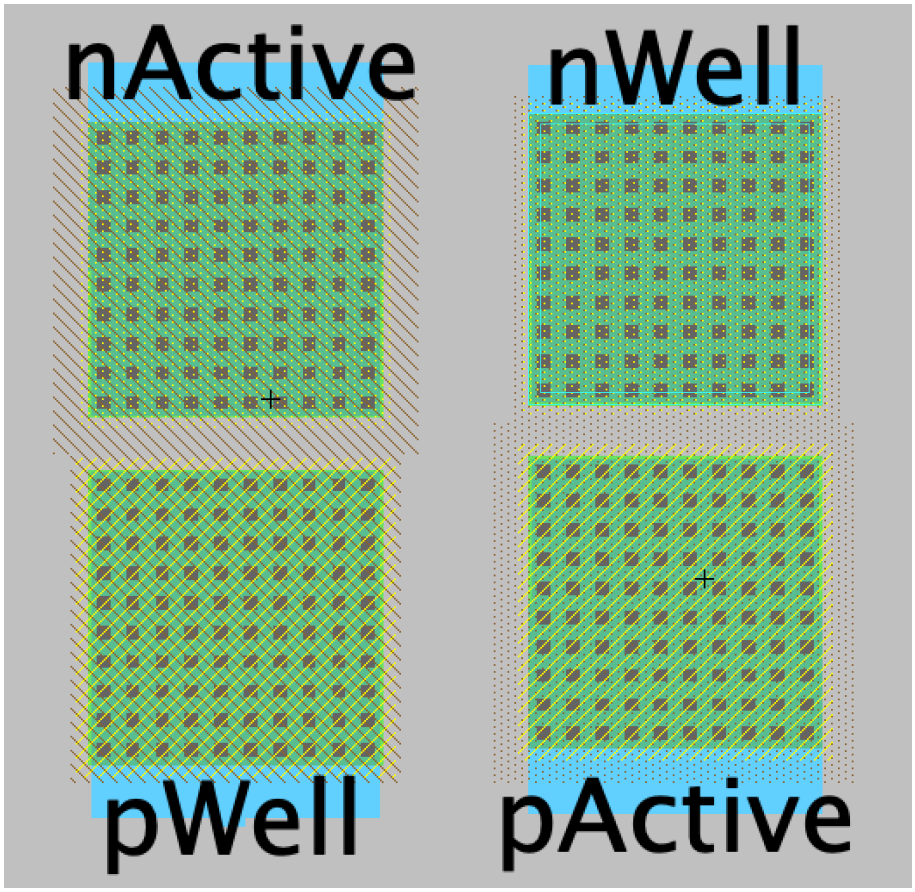


Padframe with NMOS Transistor

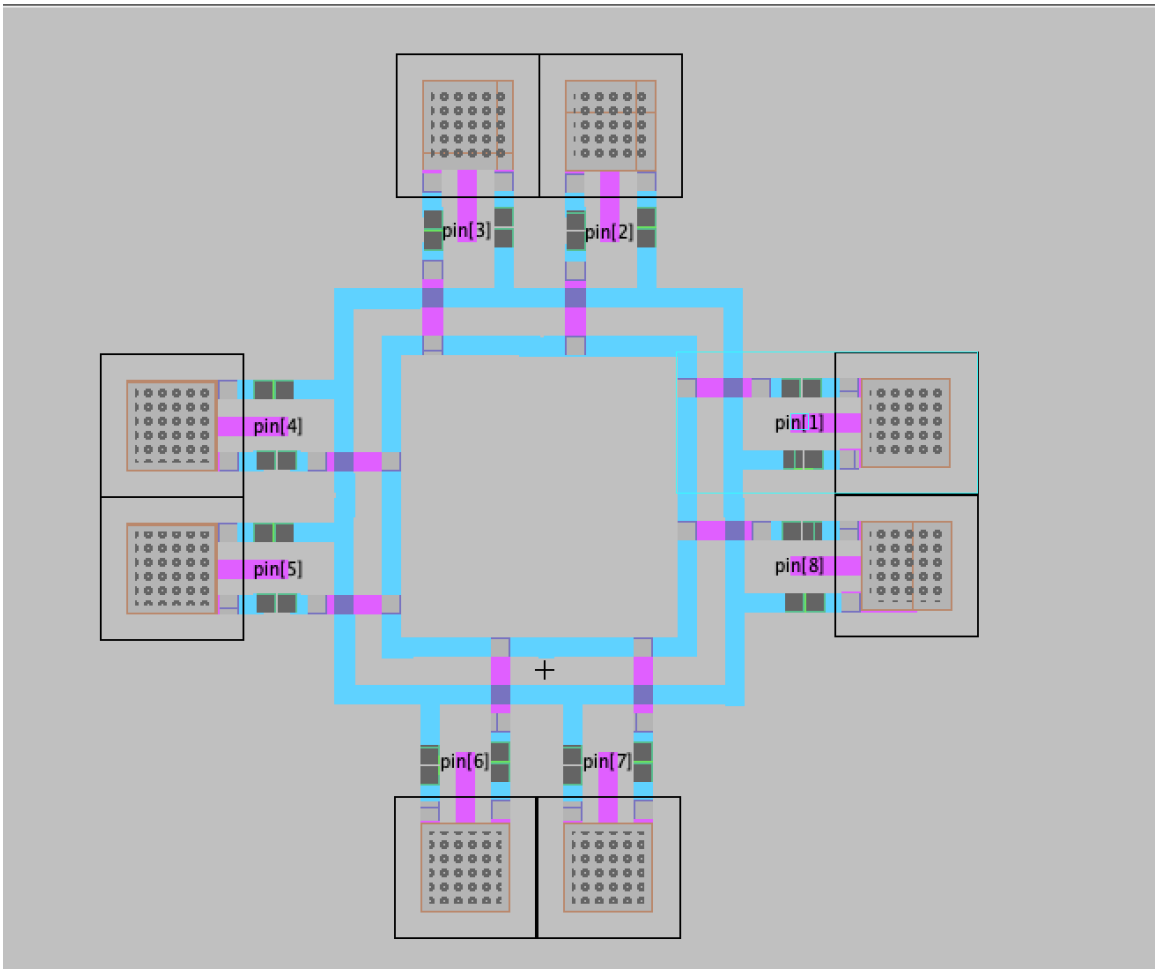


Part II – LAYOUT

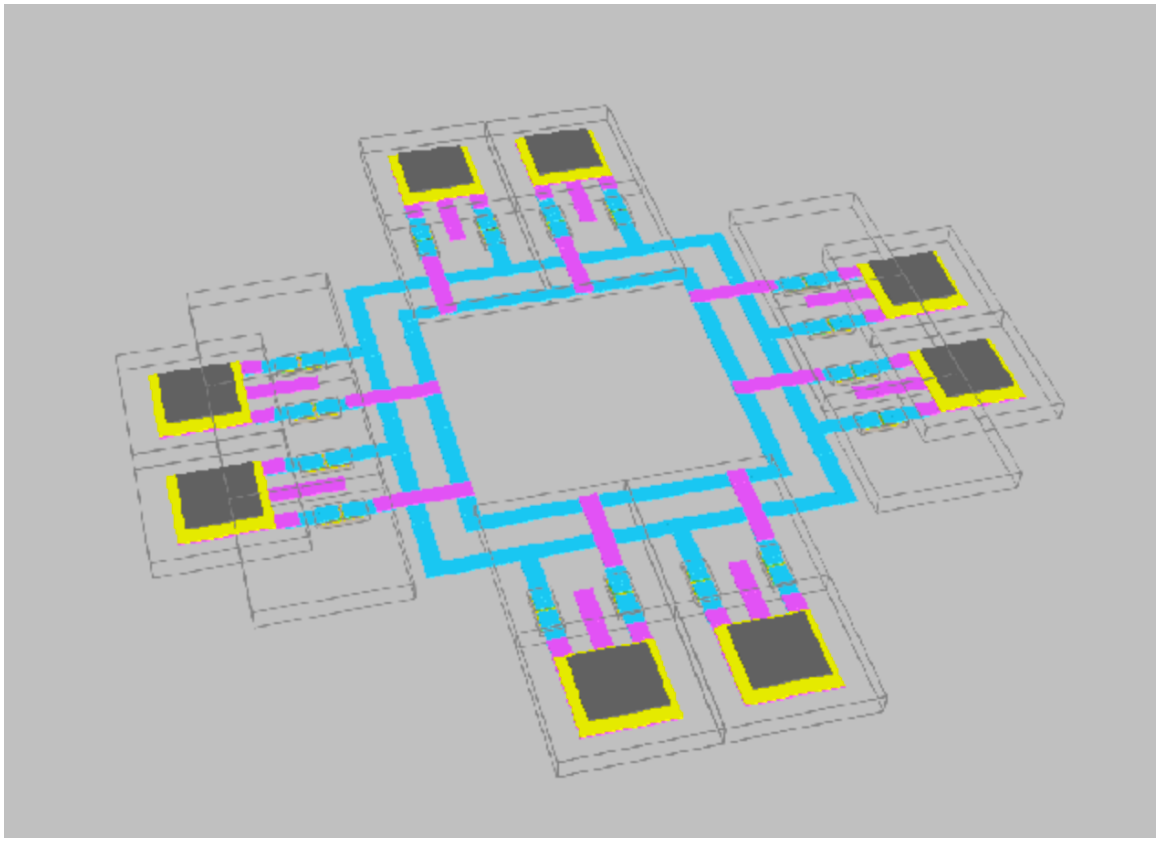
pWell-nActive and pActive-nWell Diodes Layout



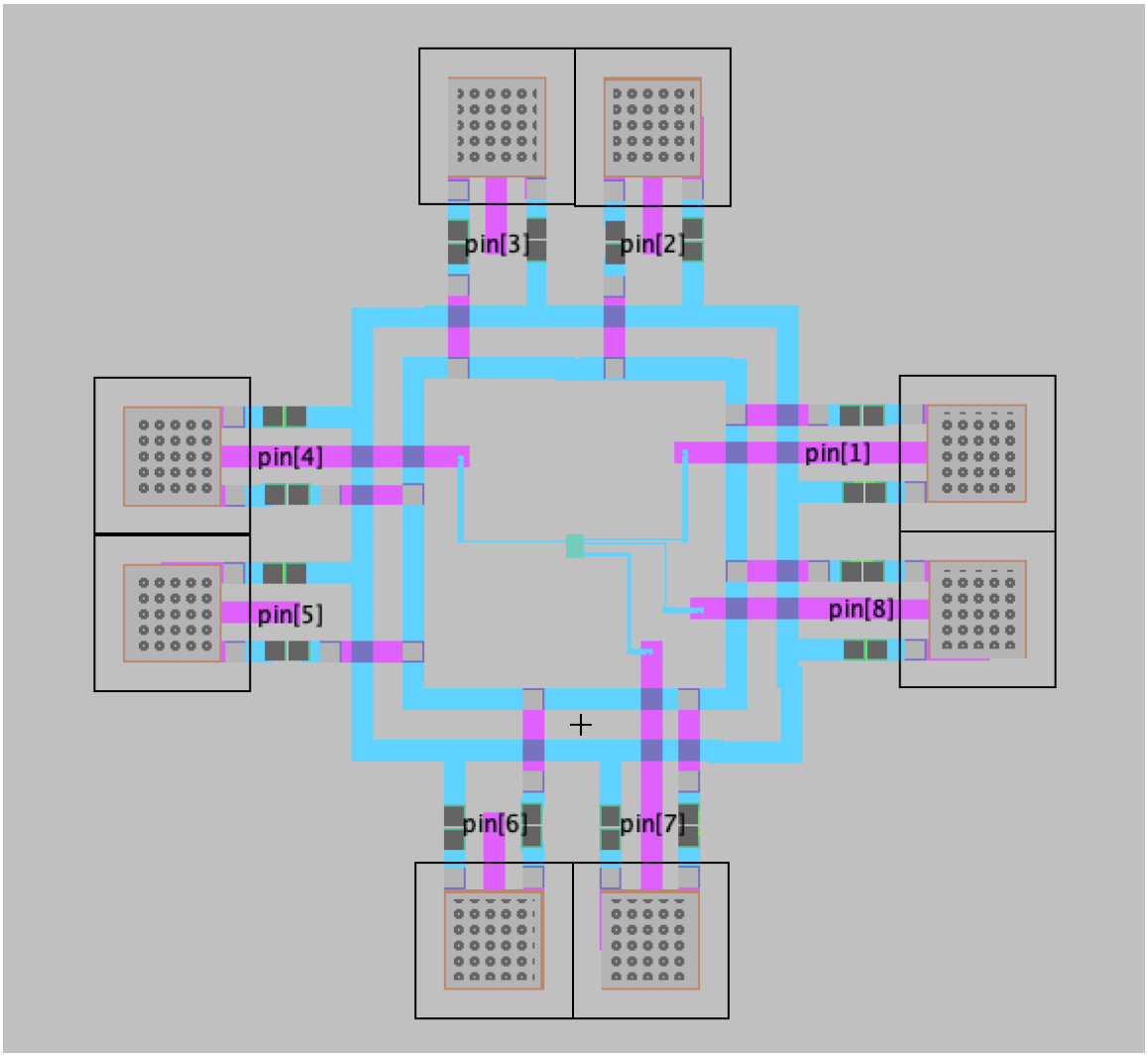
Pad Cell with ESD Protection Layout



Pad Cell with ESD Protection Layout 3D view



Pad frame with NMOS Layout



Pad Frame with NMOS 3D View