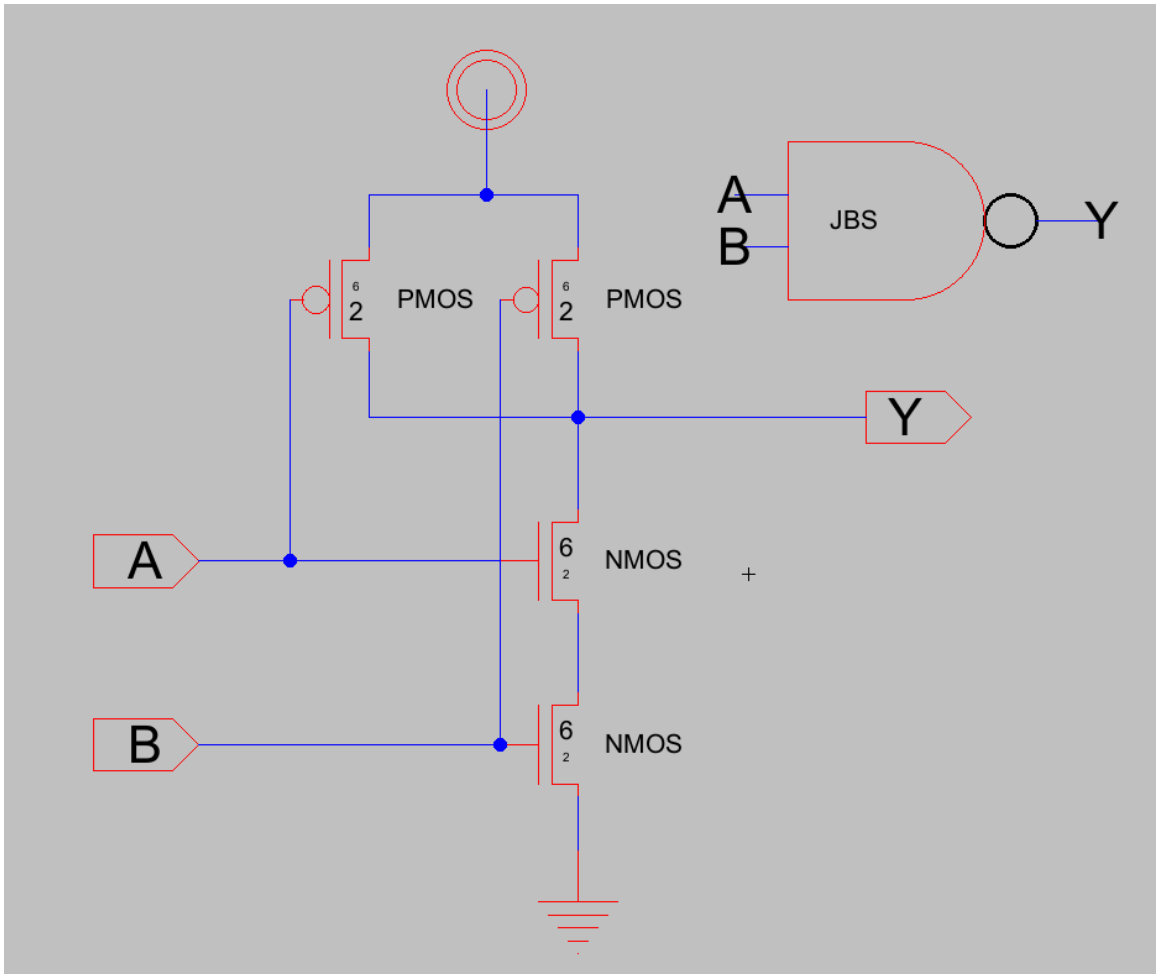
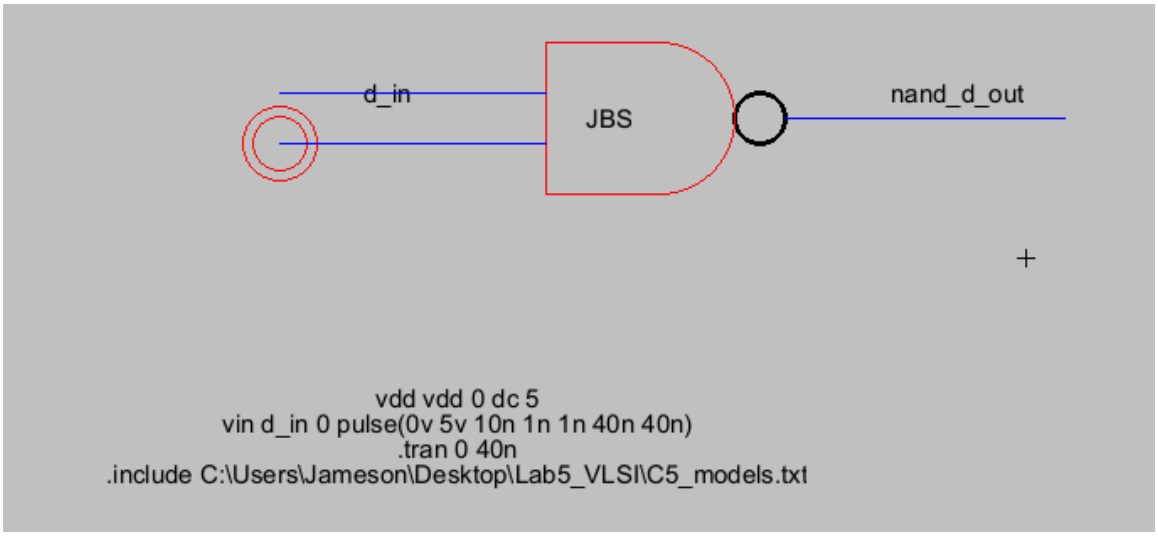
Lab 5

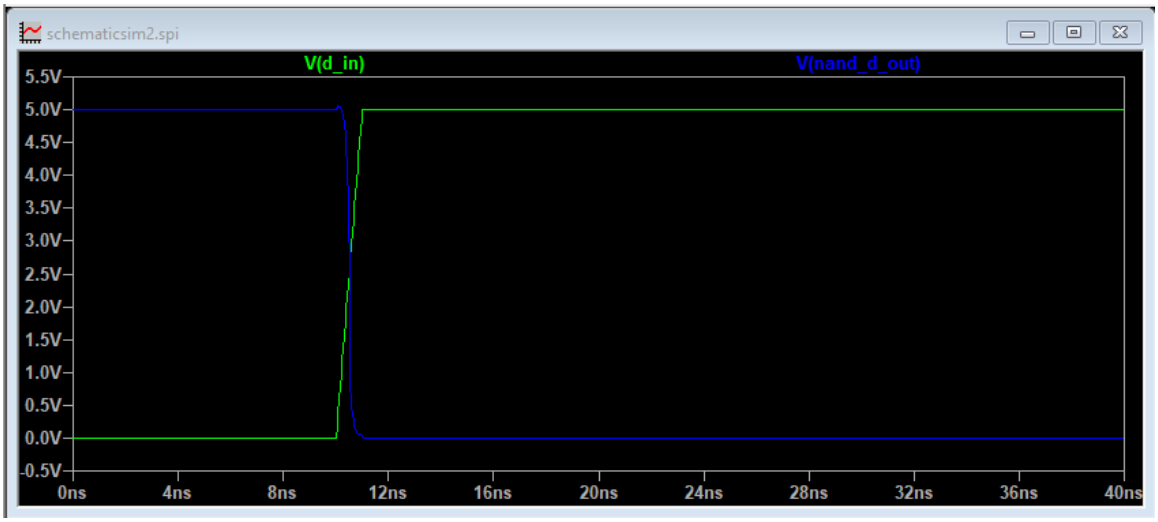
Name: Jameson Stanley Date: October 26, 2025

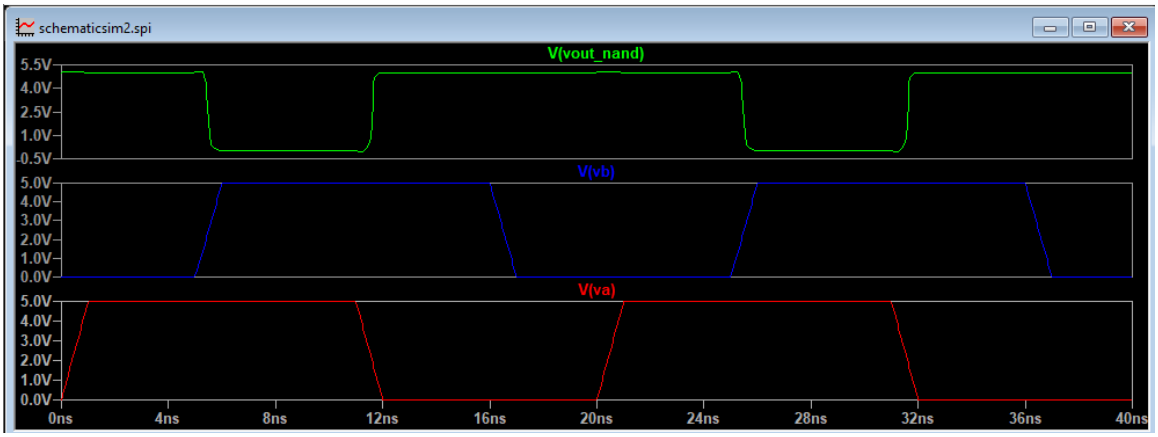
NAND Schematic



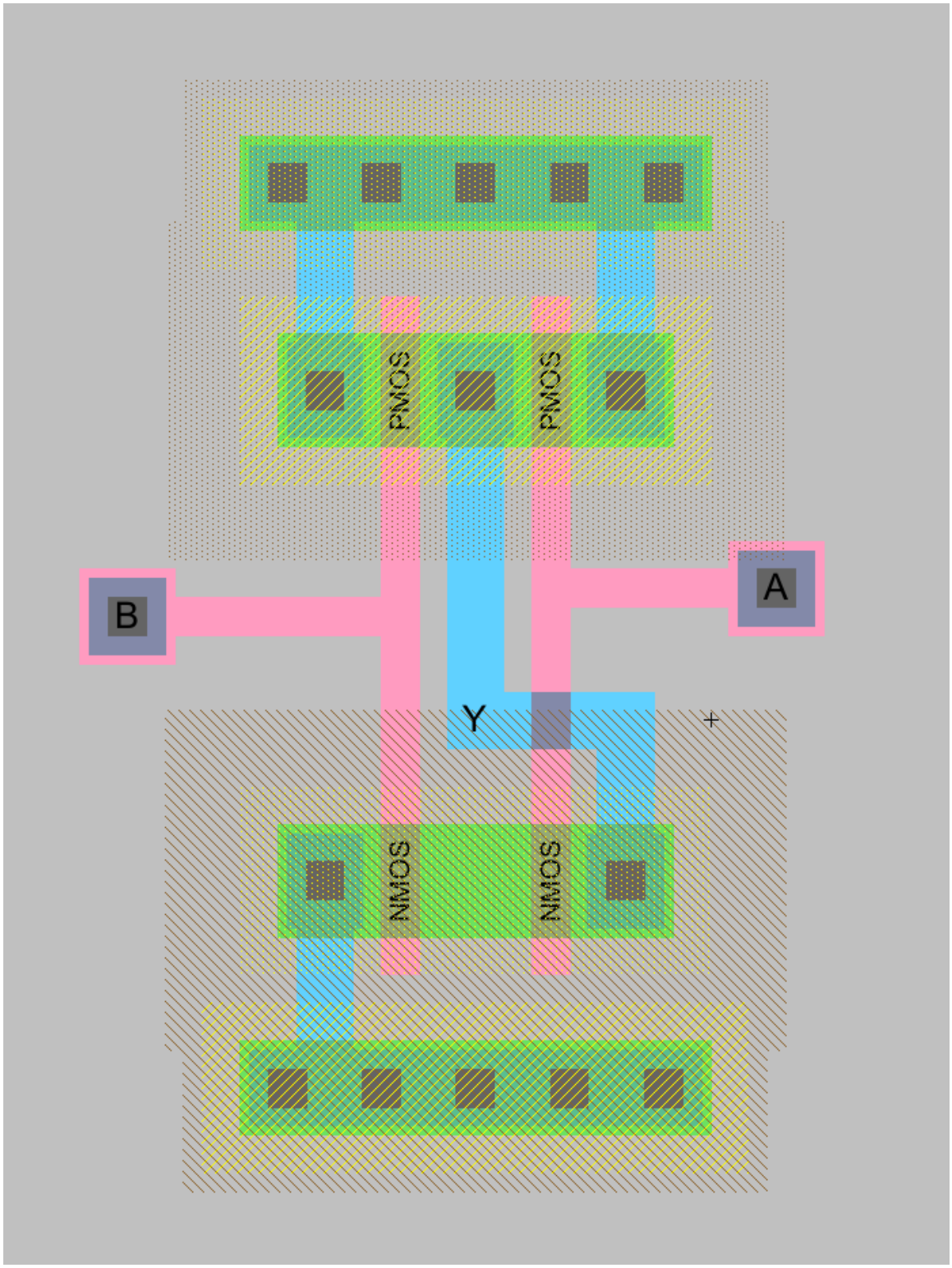
Nand Gate Simulations



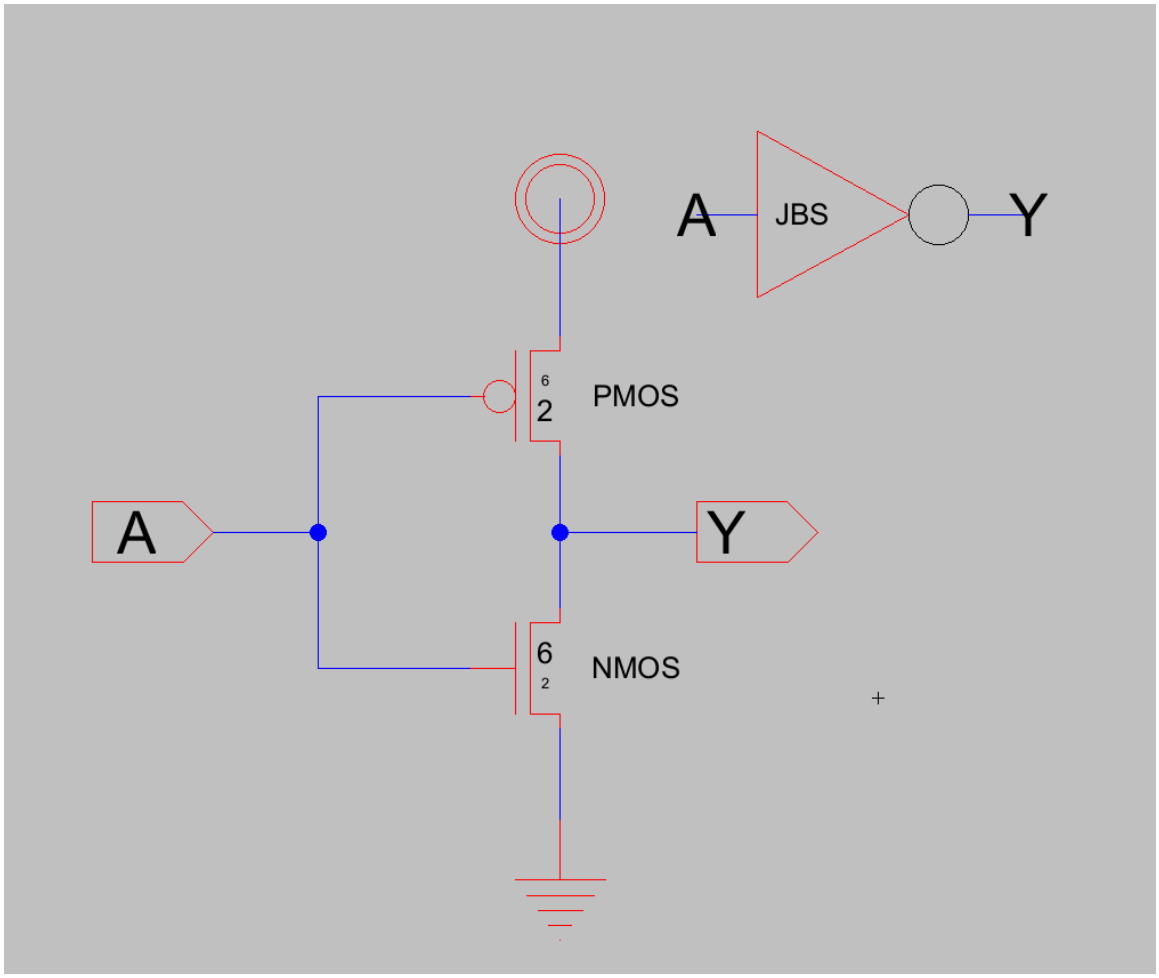




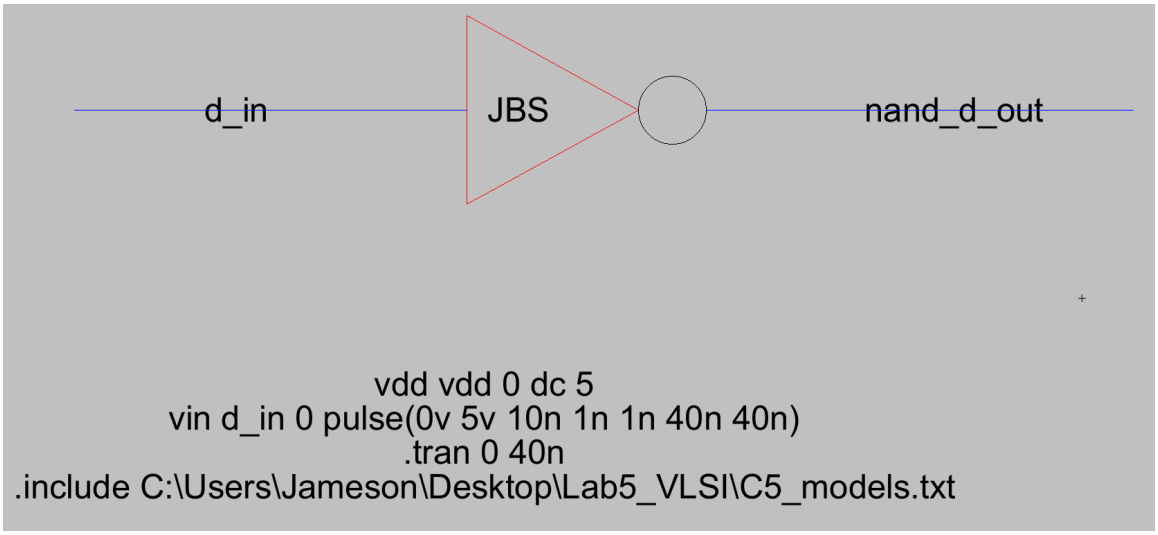
Nand Gate Layout

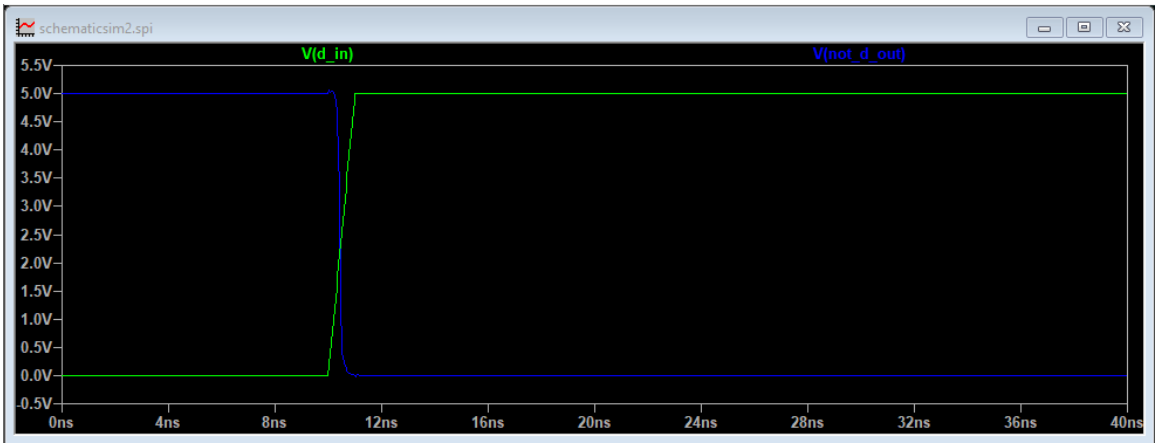


Not Gate Schematic

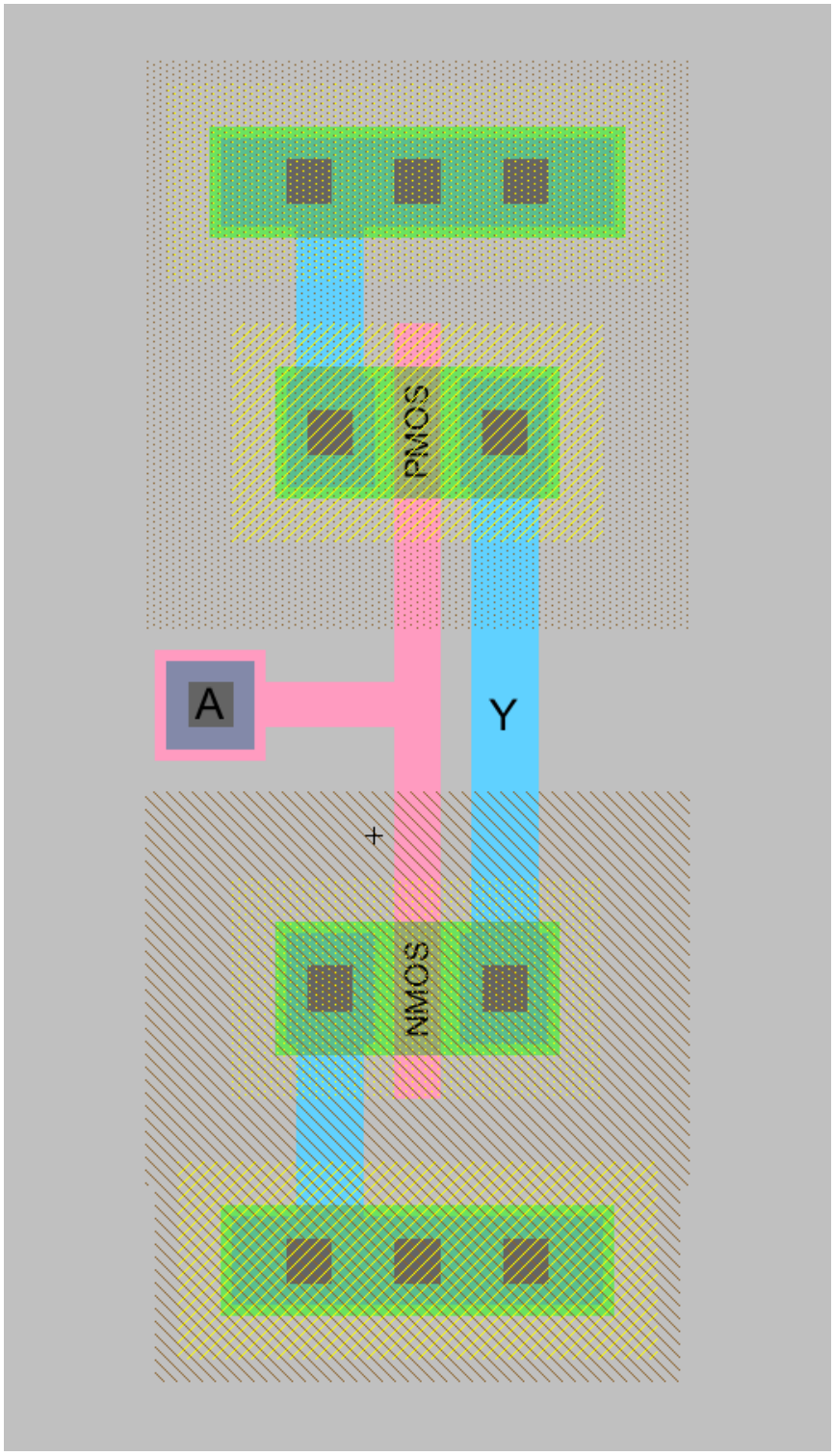


Not Gate Simulations

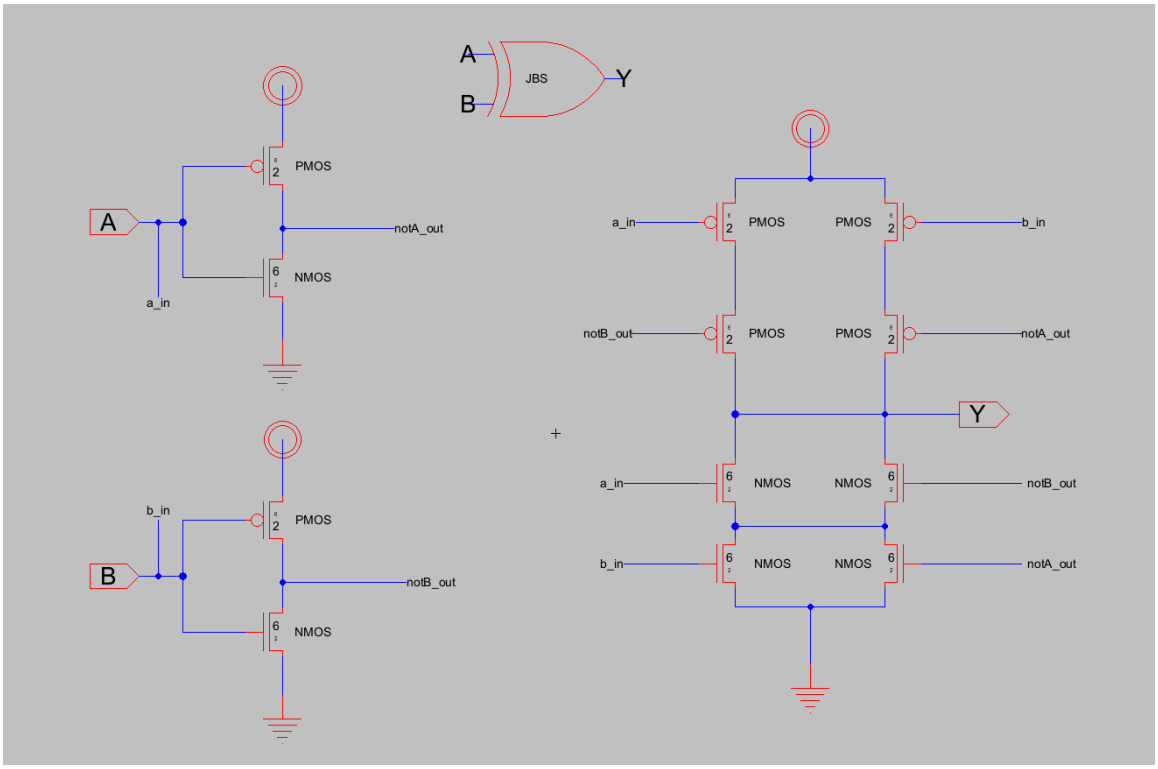




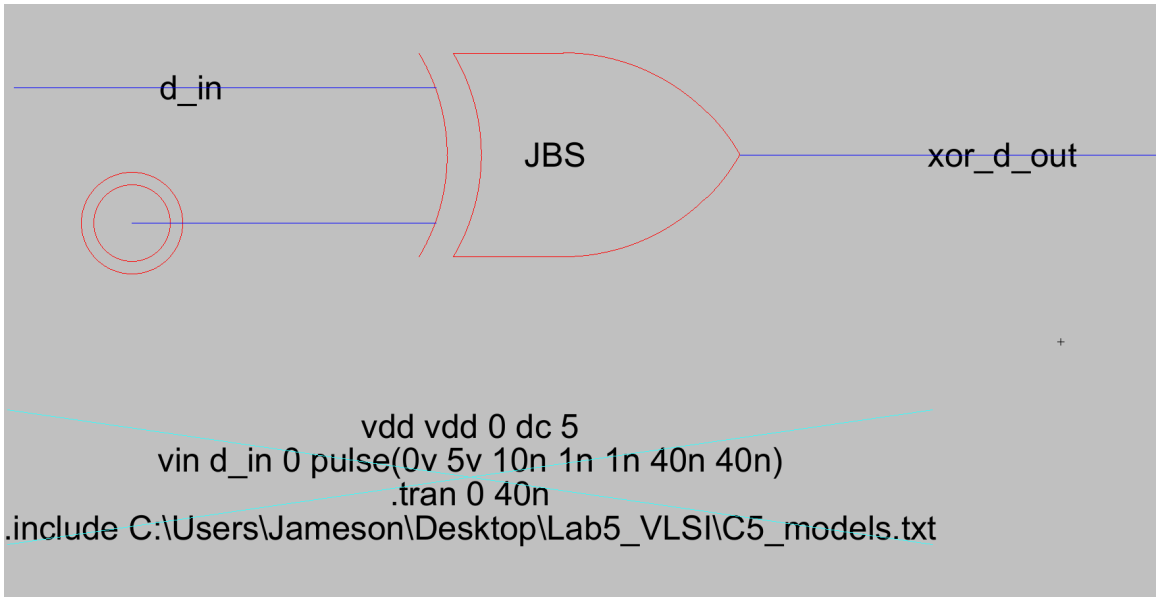
Not Gate Layout

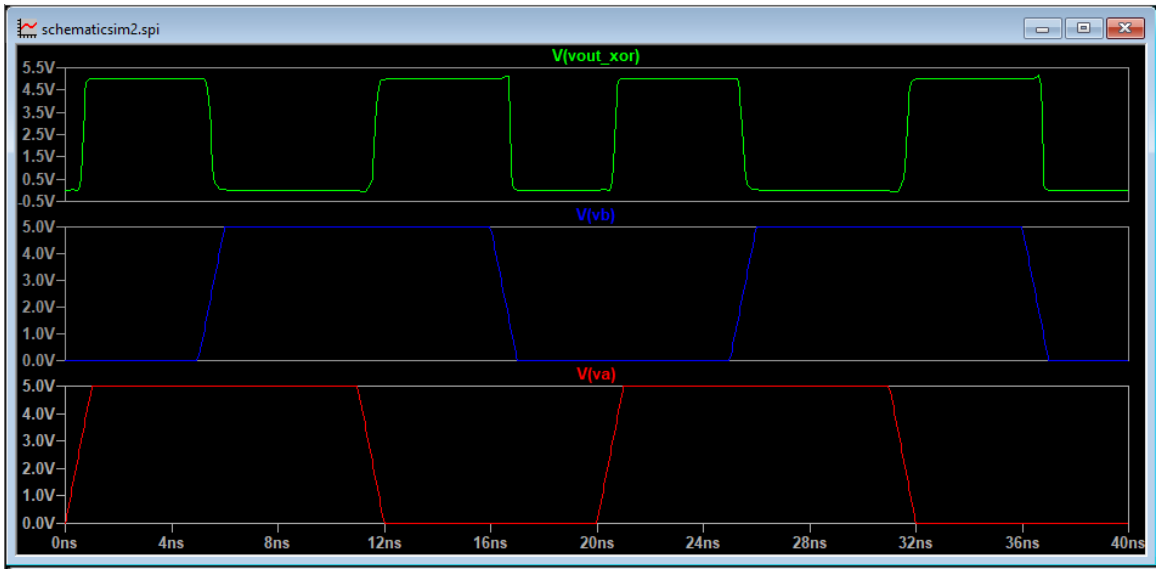


XOR Gate Schematic

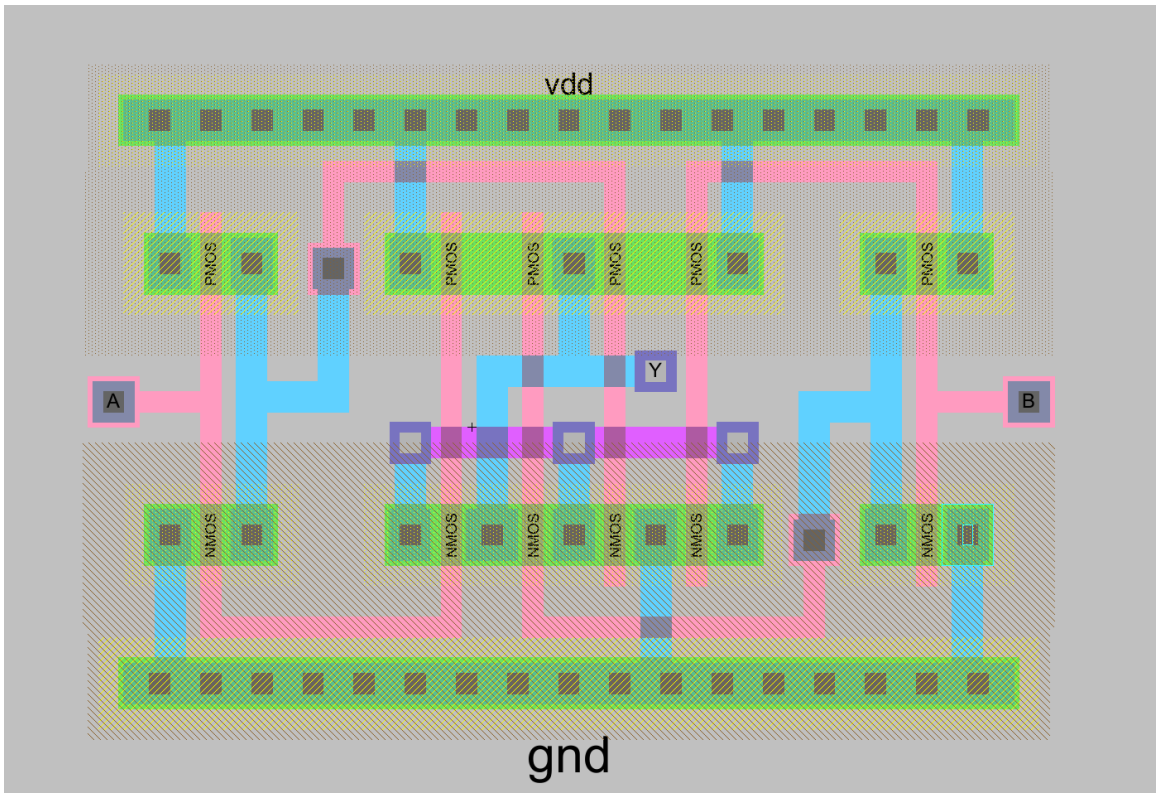


XOR simulations

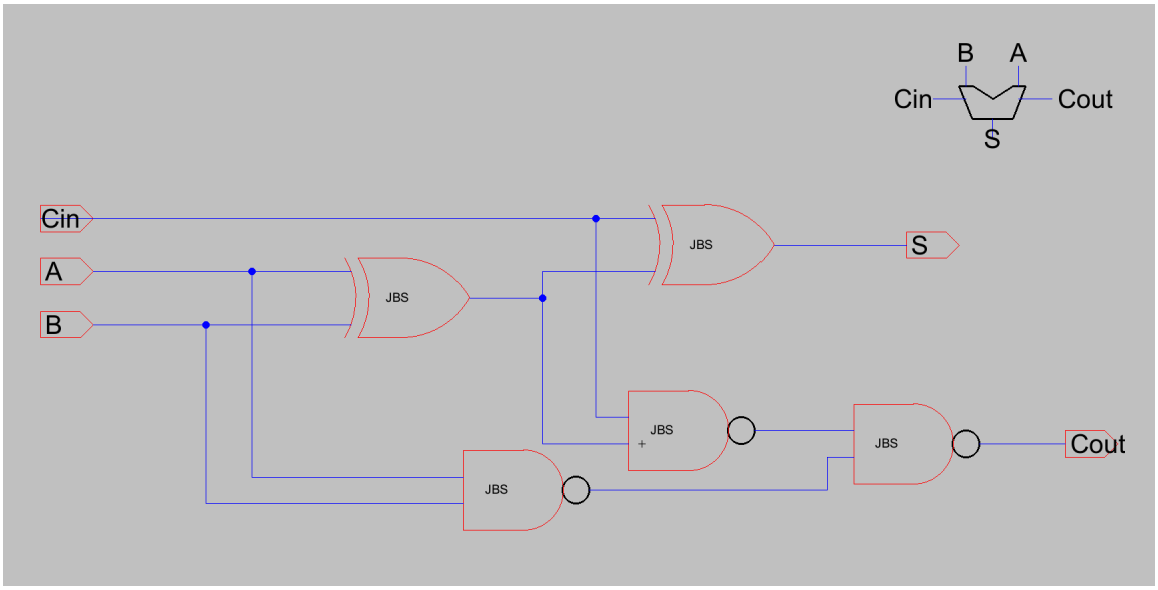




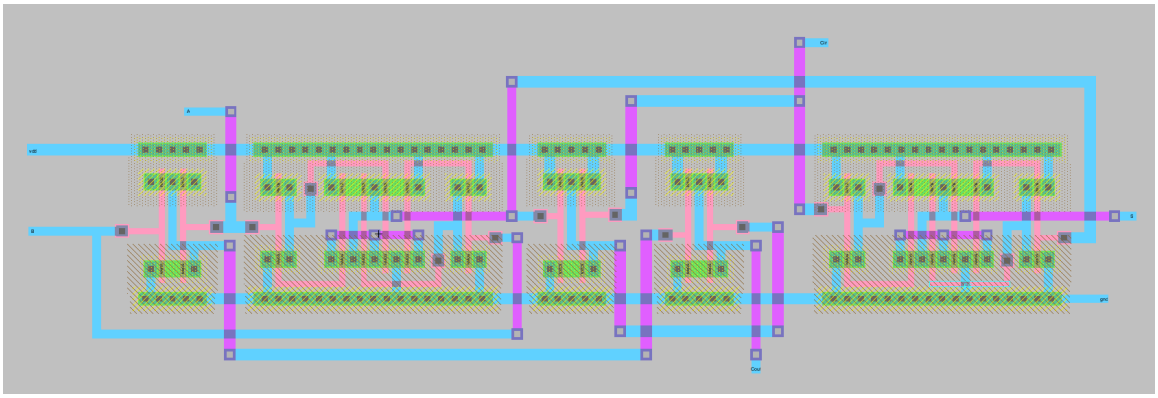
XOR Layout


vdd
PMOS
PMOS
PMOS
PMOS
PMOS
Y
A
B
NMOS
NMOS
NMOS
NMOS
NMOS
NMOS
gnd

Full Adder Schematic

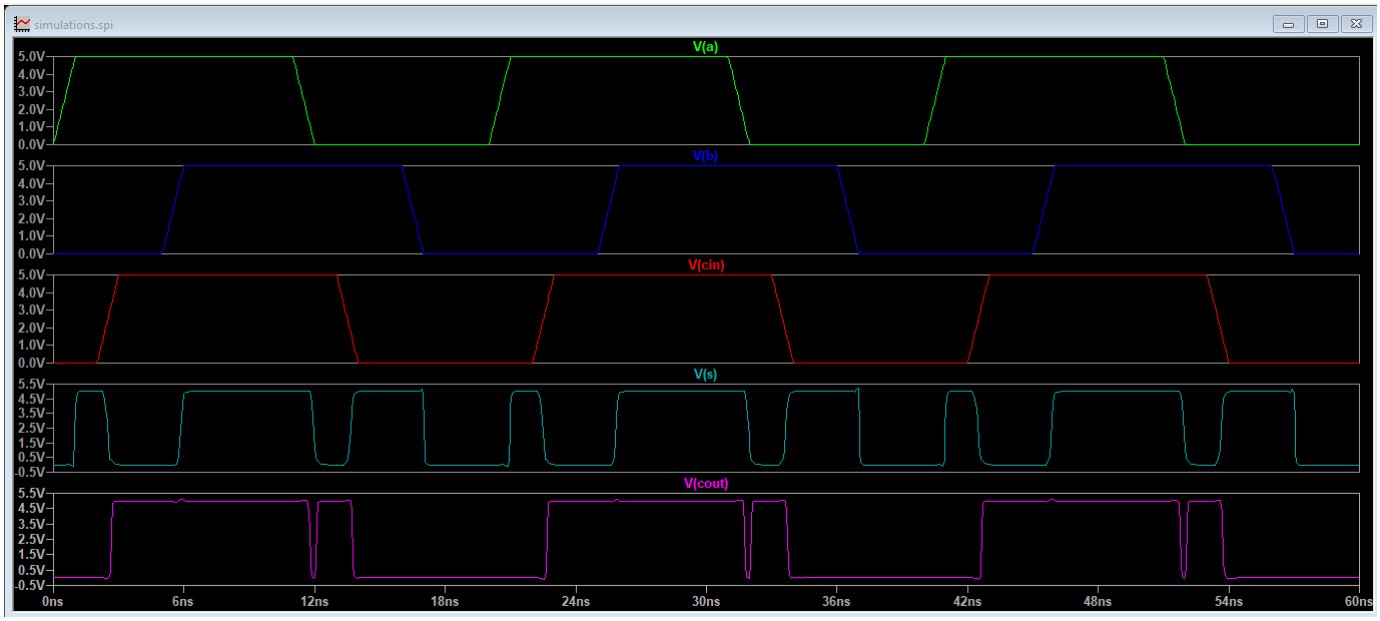


Full Adder Layout



Between the two layouts provided the better option is layout 2. This layout is more compact and has a much better flow to it then layout 1. It also shows how the VDD and Ground rails line up and allow for gates to be lined up together in a compact matter.

Full Adder Simulation



Discussion

The timing of the input pulses can cause race conditions as the transition is not immediate and there is a slight delay in the change of a gate. This can be seen in both the transition delay simulations and the truth table simulations. It can also be seen on the V(Cout) where the V(a) is still changing causing a blip in the C(out)

NRC and DRC Check

All pass NRC and DRC checks