Lab 4: Invertor

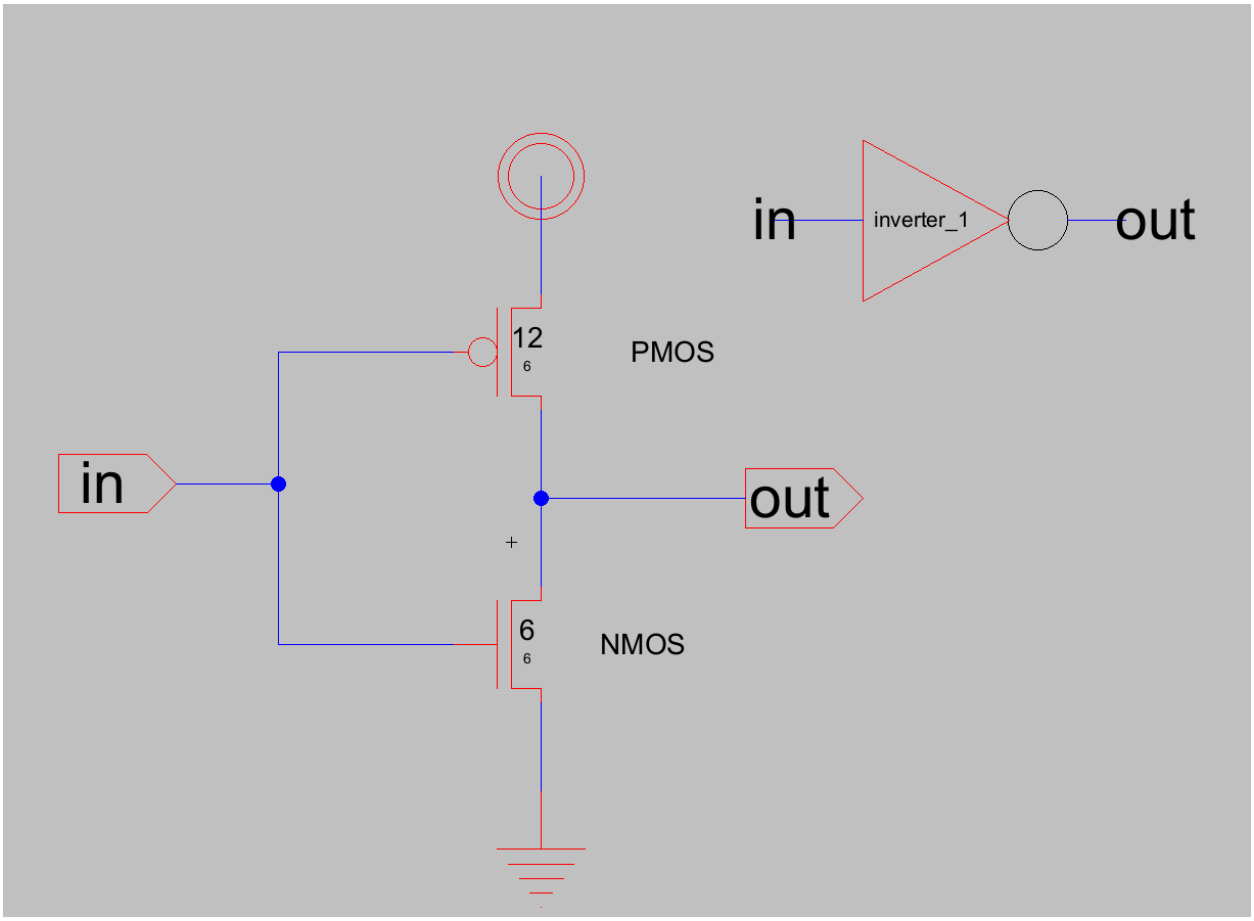
Name: Jameson Stanley Date: October 15, 2025

Objective

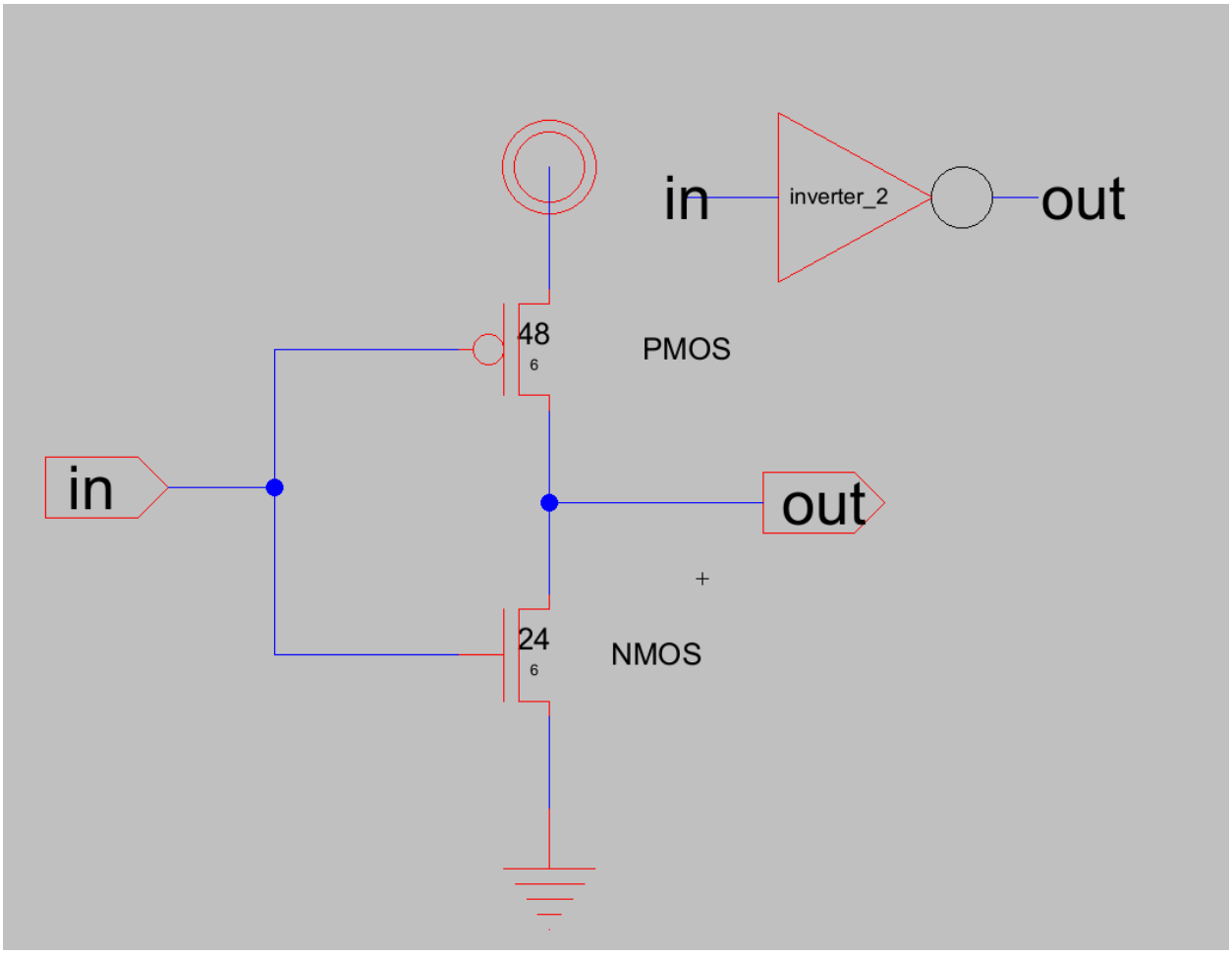
Design 2 inverters with different specifications utilizing NMOS and PMOS transistors. Then using spice simulations, the functionality of the inverter can be confirmed both with and without a load capacitor.

Part I – SCHEMATIC

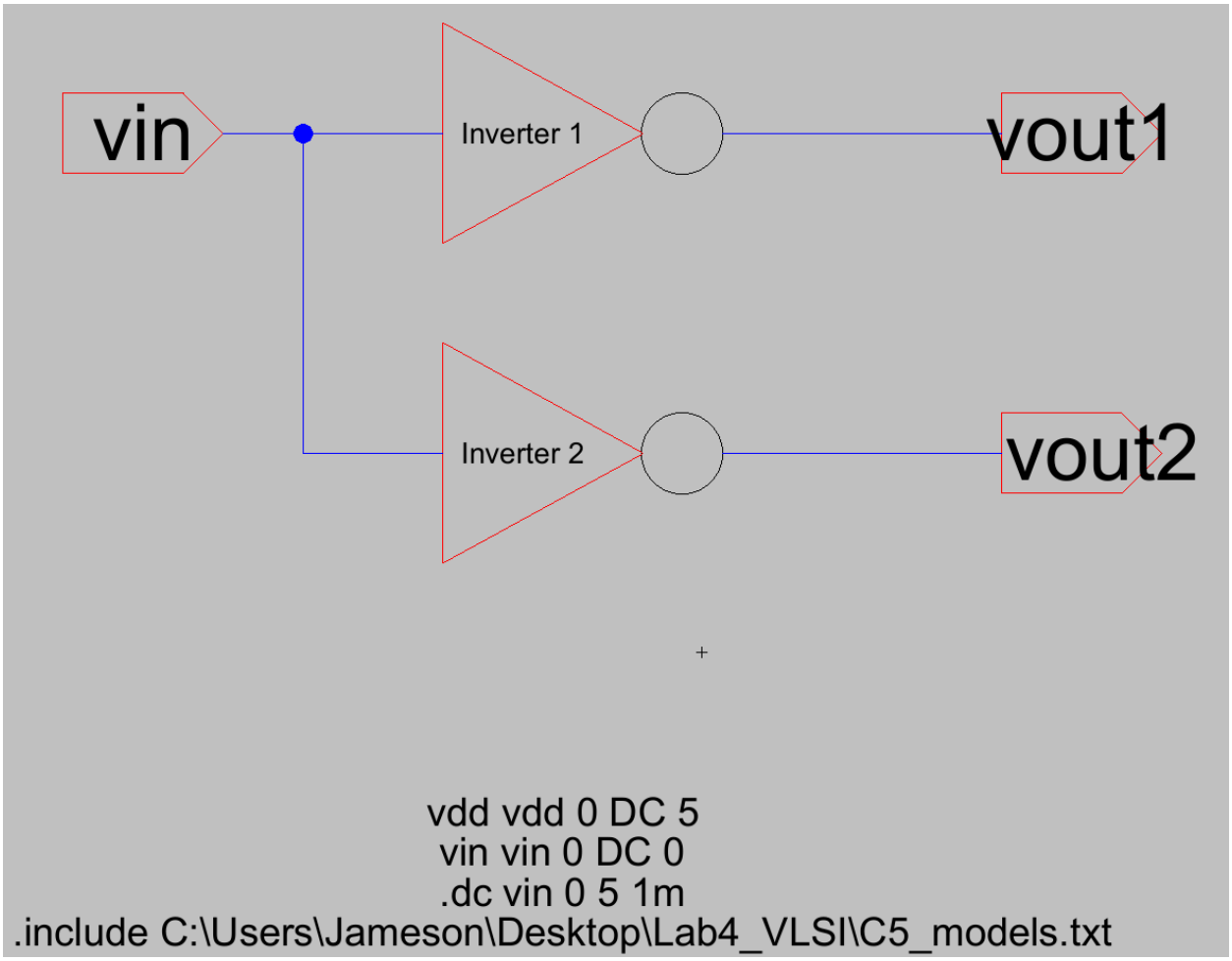
Inverter 1 – 12u/6u (PMOS) / 6u/6u (NMOS)

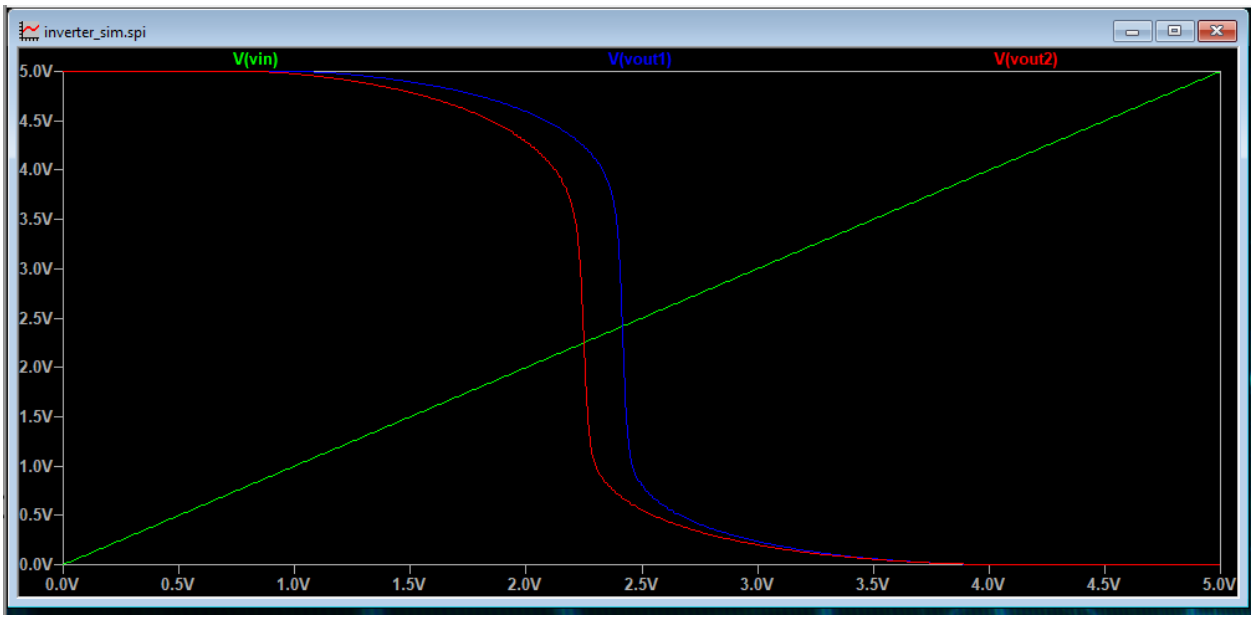


Inverter 2 – 48u/6u (PMOS) / 24u/6u (NMOS)

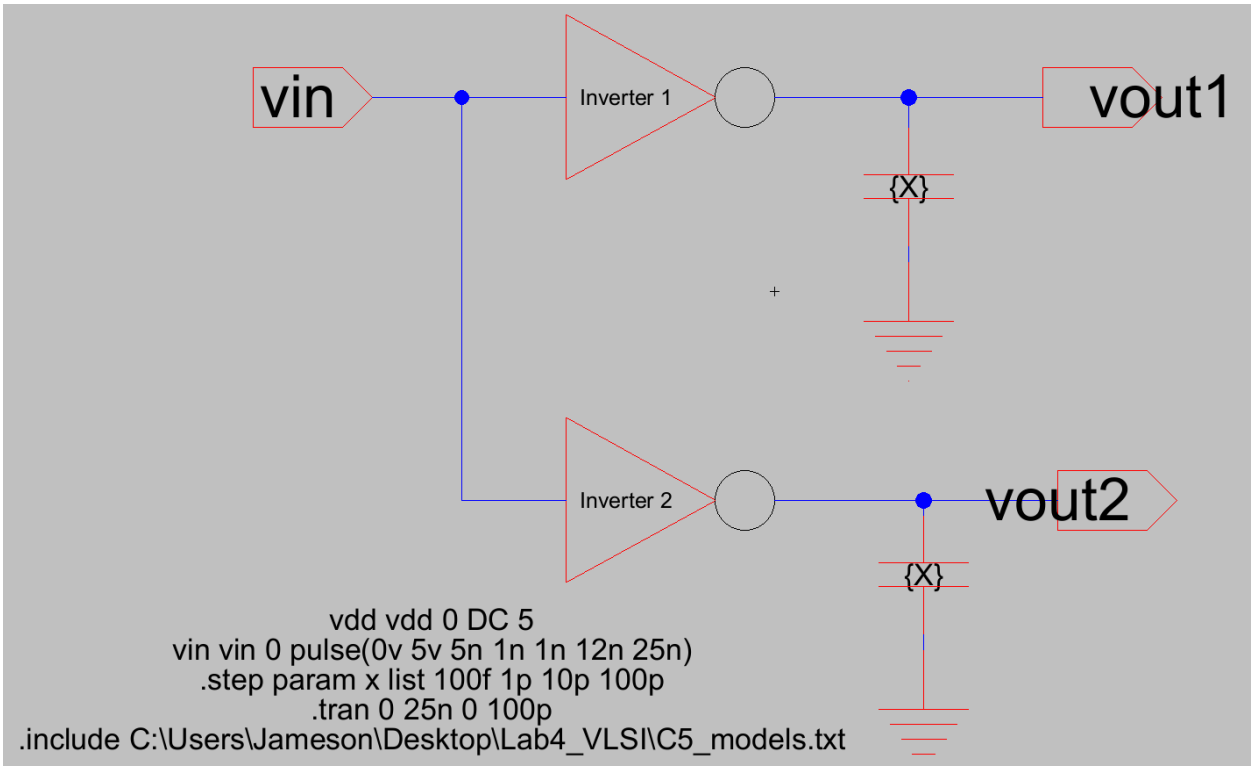


Inverter 1 and 2 Verification schematic with Simulation

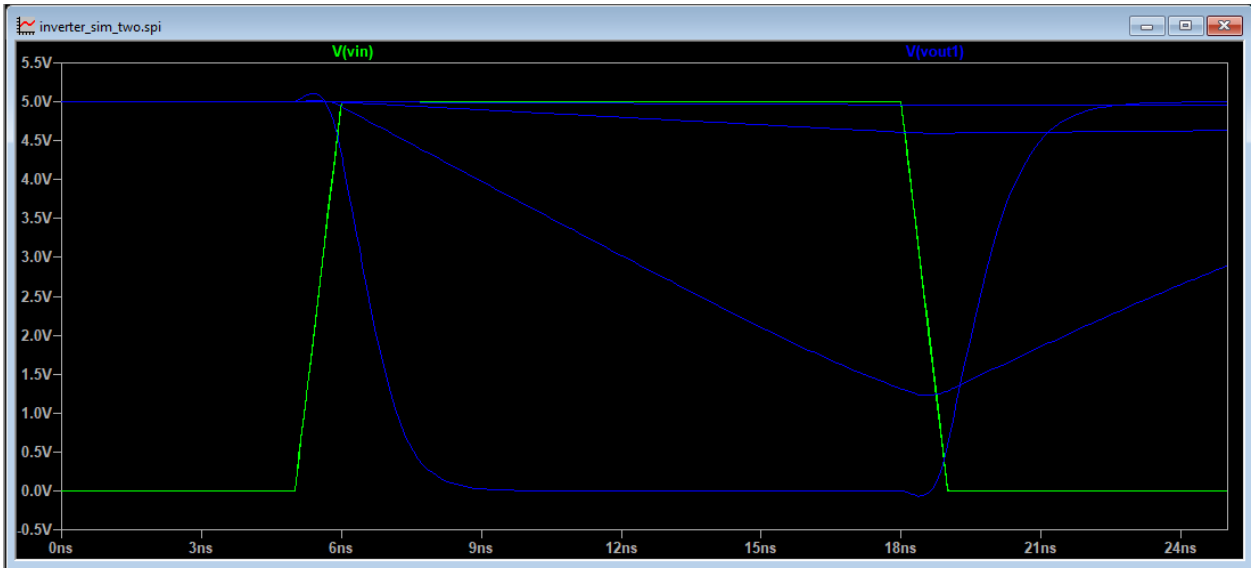




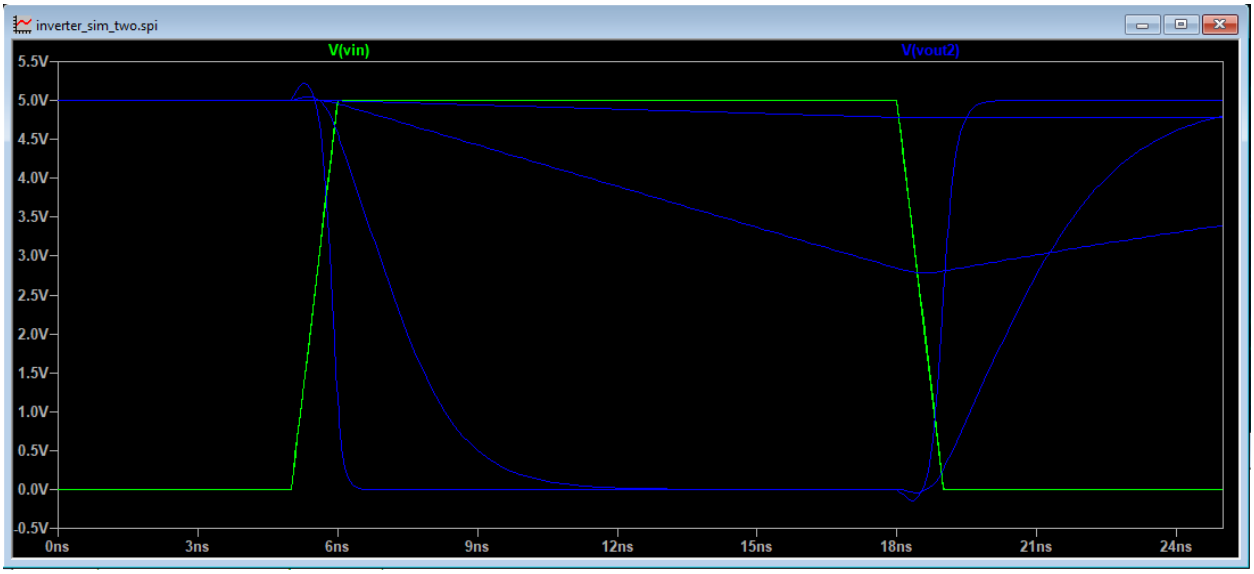
Inverter 1 and 2 with Load Schematic



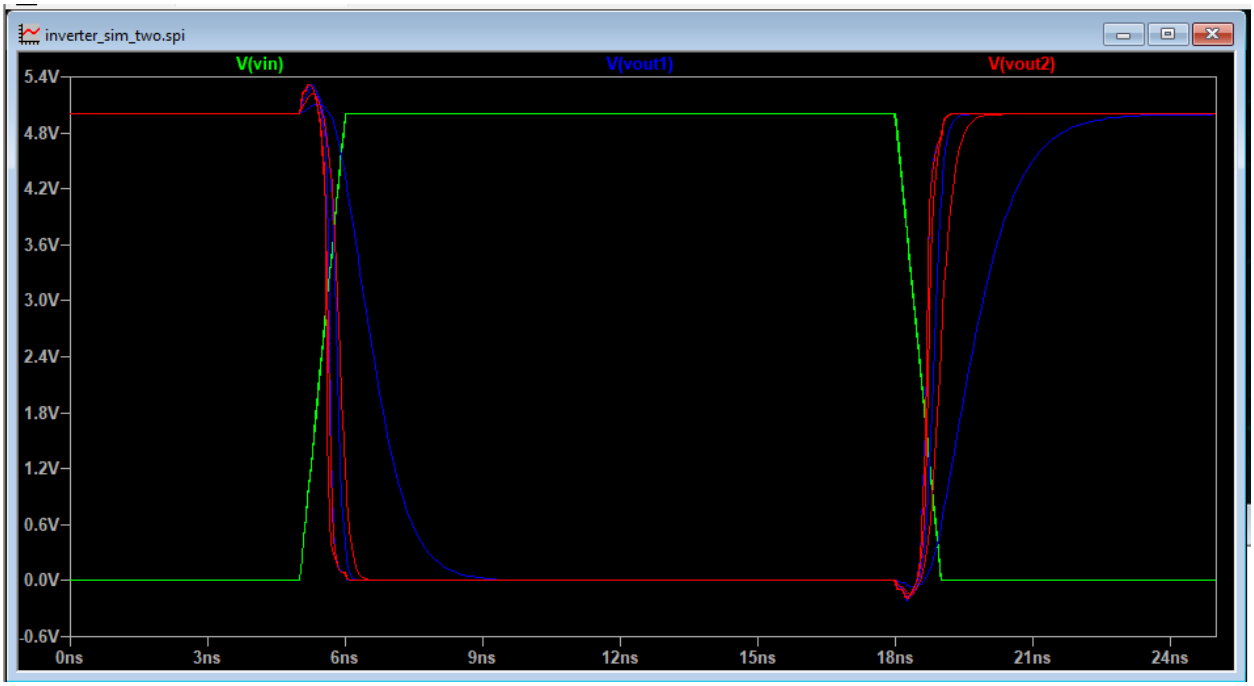
Inverter 1 with load simulation (100f 1p 10p 100p)



Inverter 2 with load simulation(100f 1p 10p 100p)



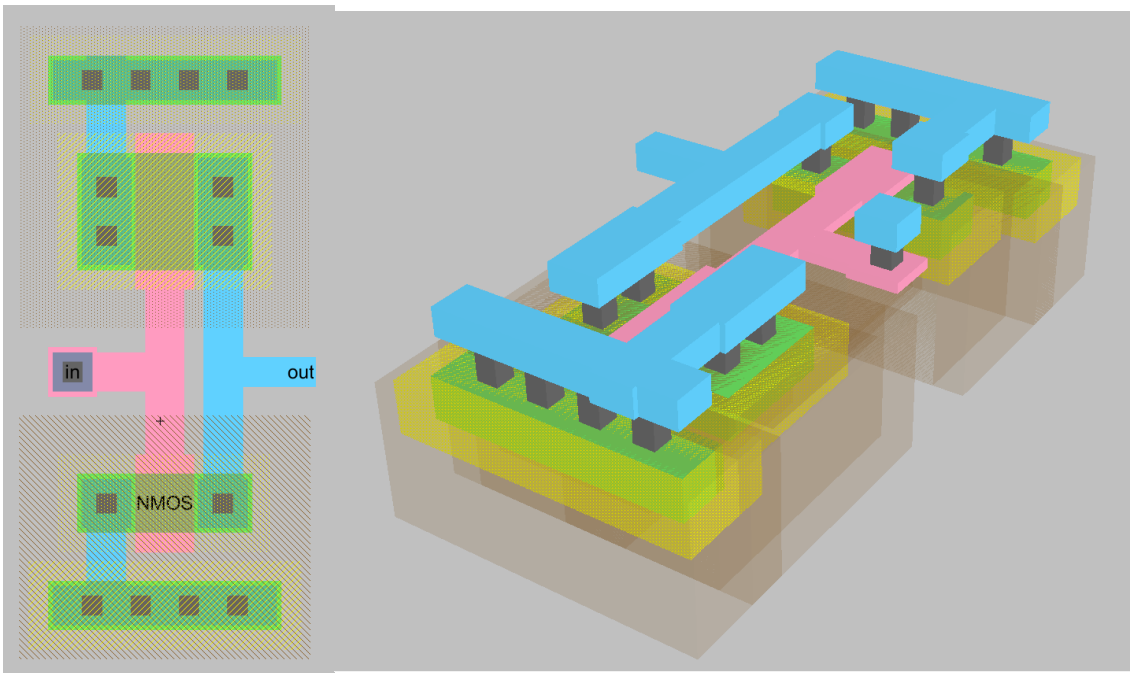
Inverter 1 and 2 with load simulation (1f 10f 100f)



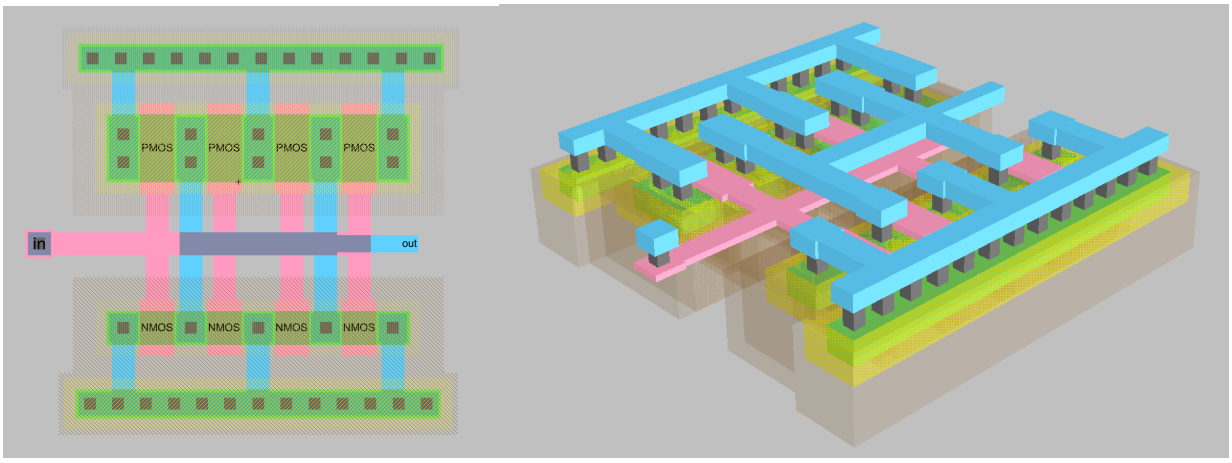
When the load capacitance is increased in the simulation, the propagation delay of both inverters increases. This is expected because the inverter output must charge or discharge the load capacitor through the transistor's resistance. The delay can be approximated by $t_d \approx 0.69RC$, where R is the effective output resistance of the inverter and is the load capacitance. As capacitance increases, the time required for the output to switch also increases, confirming the RC behavior. Additionally, the inverter with larger transistors (Inverter 2) has less delay for the same load because its lower output resistance allows it to drive the capacitor faster.

Part II – LAYOUT

Inverter 1 Layout with 3D View



Inverter 2 Layout with 3D View



Resources used:

VLSI DESIGN
PERPLEXITY