Lab 1 Report: 5-bit R-2R Ladder DAC

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Course: VLSI Design
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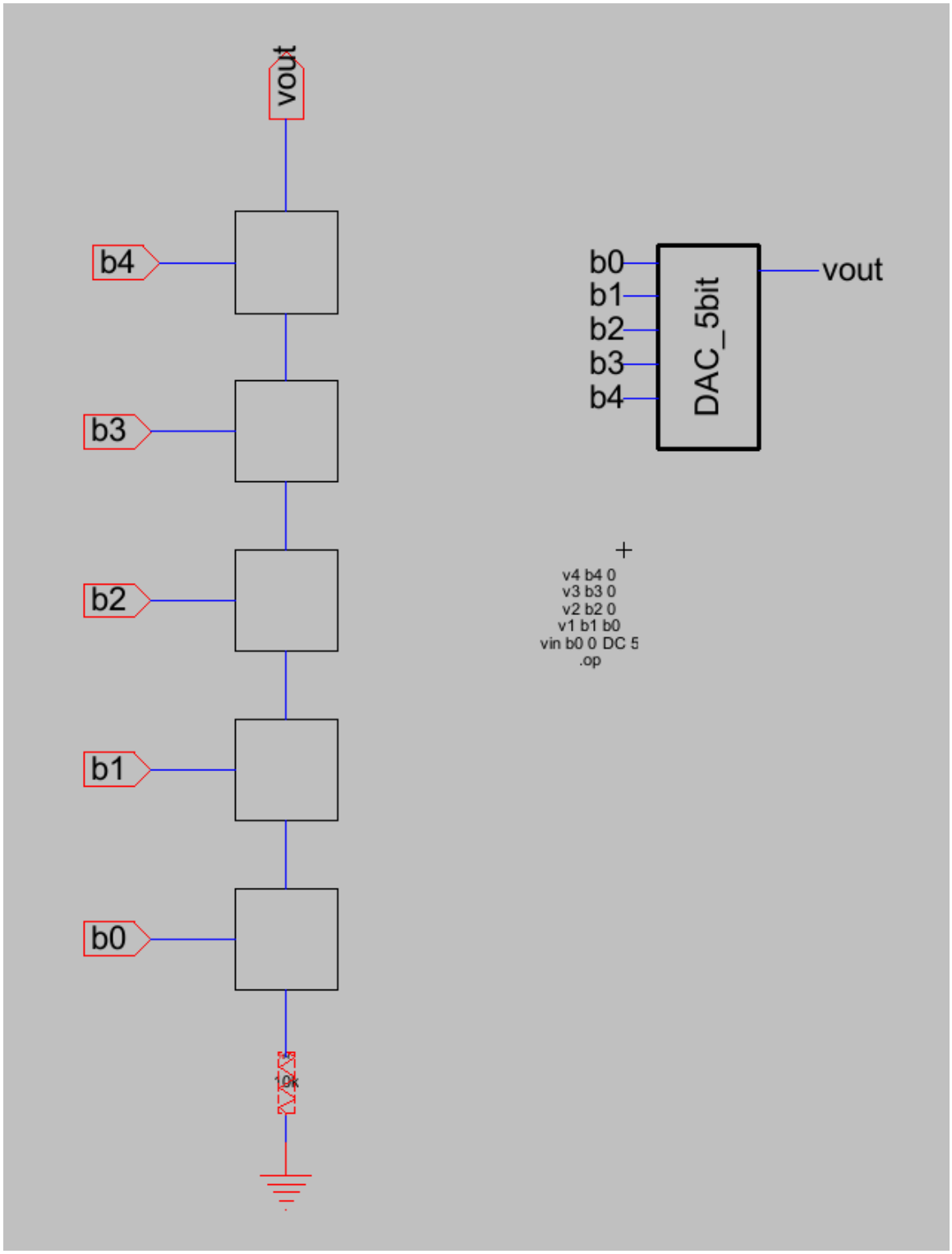
1. Introduction

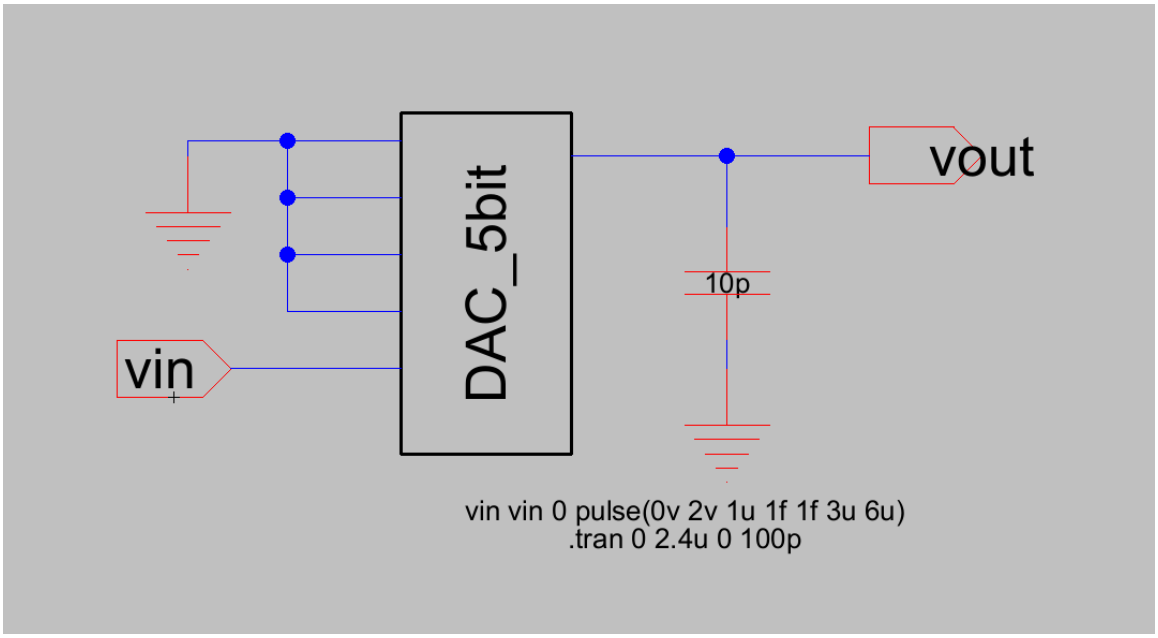
The goal is to Design a 5-R2R Ladder Dac utilizing 10kΩ resistors in the Electric VLSI design software and preform simulations to confirm the functionality of the design. Then a physical layout can then be implemented using n-well resistors.

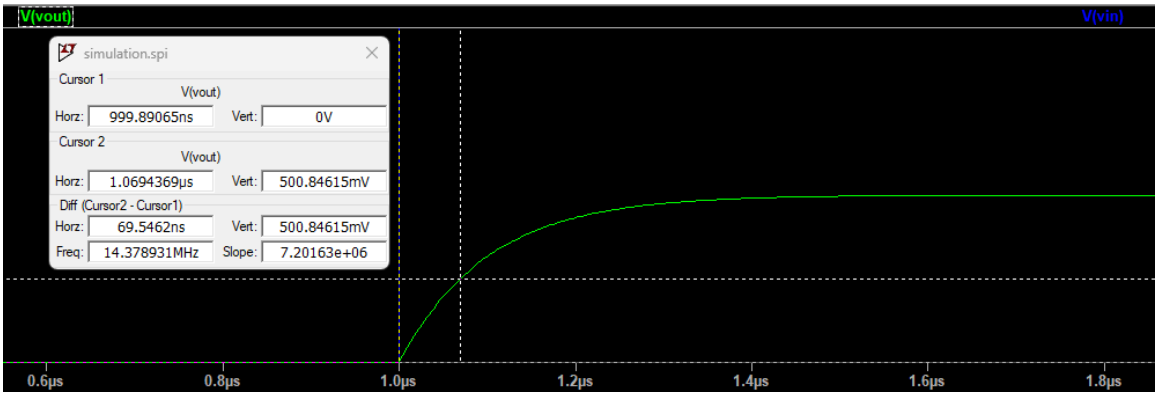
2. Schematic and Design

2.1 5-bit DAC Schematic



2.3 Delay Analysis





3. Layout

3.1 N-Well Resistor Design

To find the dimensions required for a 10kΩ the equations $R = R_{sq} * \frac{L}{W}$ can be used knowing that $R_{sq} = 855 \frac{\Omega}{sq}$ and using a chosen width of 14 µm to find the length required for a 10kΩ n-well resistor.

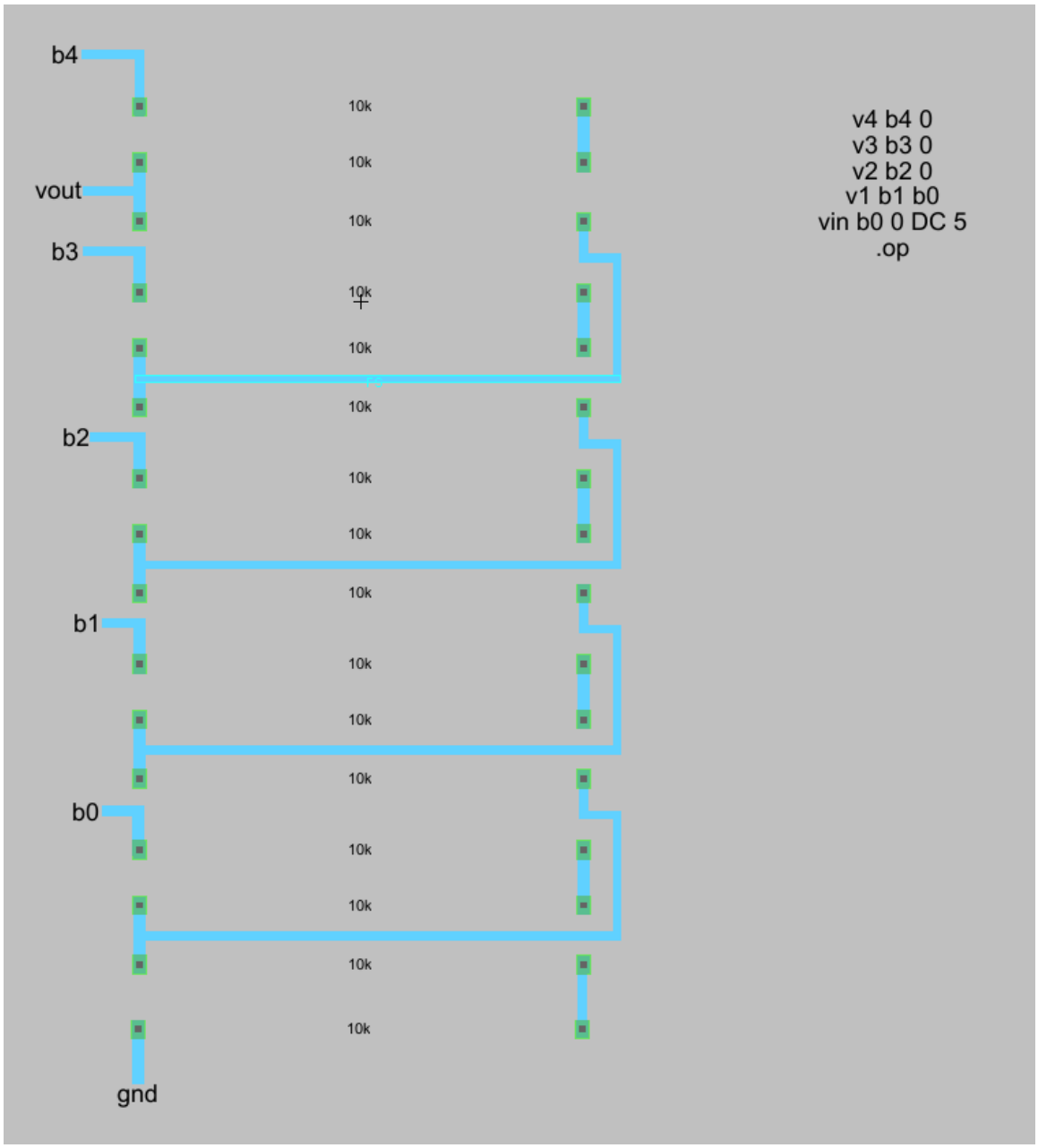
$$R = R_{sq} * \frac{L}{W}$$

$$10k\Omega = 855\frac{\Omega}{sq} * \frac{L}{14\mu m}$$

$$\frac{10k\Omega}{855\frac{\Omega}{sq}} * 14\mu m = L$$

$$L \approx 16$$

3.2 DAC Layout



3.4 DRC & LVS Results

Passed DRC & LVS

6. References

Electric VLSI

List all references used (textbook, lab handouts, PDK documentation, etc.).