YEN-CHENG LIN

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EDUCATION

University of Michigan – Ann Arbor, MI **May. 2026 (Expected)**

M.S. in Electrical and Computer Engineering | Integrated Circuit & VLSI Track

- Coursework: VLSI Design I, Parallel Computer Architecture, Computer Architecture, Advanced Compiler, VLSI for Wireless Comm. and ML

National Central University – Taoyuan, Taiwan **Jun. 2023**

B.S. in Electrical Engineering GPA: 4.0 / 4.3 (3.9 / 4.0 in WES)

- Coursework: VLSI System Design, Digital System Design, Digital Signal Processing, OS, Special Project on VLSI Design

WORK EXPERIENCE

NVIDIA Corp. **May. 2025 – Aug. 2025**

Digital Design Verification Intern | SerDes Digital IP team Santa Clara, CA

- Assisted in the verification of digital designs, golden models, and micro-architecture for SerDes IPs using UVM.
- Developed reusable bus functional models, monitors, and checkers and contributed to defining verification scope and infrastructure.
- participated in writing and implementing test plans to thoroughly verify designs in a dynamic, real-world environment.

Academia Sinica / National Taiwan University **Jun. 2023 – Jul. 2024**

Full- time Research Assistant Taipei, Taiwan

- Participated in ”Angstrom Semiconductor Initiative ” by National Science and Technology Council.
- Used range encoding for similarity search in TCAM and analyzed the training set’s variance to optimize the range; **reduced the average search count from 7.97 to 3.15**.

PROJECT

2-Way Superscalar R10K-styled RISC-V Out-of-Order CPU **Sep. 2024 – Dec. 2024**

Digital Circuit Design | SystemVerilog, Shell Script, RISC-V Assembly, Verdi

- Designed an OoO CPU with tournament branch predictor (w/ PAg & GShare), branch target buffer using Least-recently-used policy, return address stack, instruction prefetching, non-blocking data cache with miss status handling registers, victim cache in data cache, Load-store queue with forwarding.
- Achieved the performance of **minimum 10ns clock period, 2.26 CPI, 44.2 MIPS, 40% better than the class median** and validating with the real world C programs.

A High-Performance Hybrid CPU–GPU Framework for Graph Coloring Problem Acceleration **Jan. 2025 – Present**

Digital Circuit Design & Parallel Computing | SystemVerilog, C++, CUDA, Intel VTune

- Designed a CPU-GPU hybrid framework to accelerate the Graph Coloring Problem (GCP), an NP-complete problem crucial for register allocation in compilers and parallel workload scheduling.
- The CPU manages branching, scheduling, and irregular memory access, while the GPU performs parallel color assignment and conflict resolution.

Asynchronous FIFO Design and Verification **Jun. 2024**

Digital Design & Verification | SystemVerilog, Assertion

- Designed a 8-bit, 16-depth asynchronous FIFO module with SystemVerilog and Solved Clock Domain Crossing (CDC) issue.
- Developed a SystemVerilog verification environment with a transaction generator, driver, monitor, scoreboard and environment.

CNN Accelerator and Hardware Trojan Design on FPGA **Jul. 2022 – Jun. 2023**

Digital Circuit Design | Verilog, Python, C++, Vitis HLS

- Utilized Python TensorFlow to build a LeNet facial recongnition model, which weights be quantized from 32-bit floating point to 8-bit fixed point .
- Designed a parallelized CNN accelerator using Verilog and demonstrated an **11.04x speedup** in inference on Xilinx Zynq 7000 FPGA.
- Inserted a hardware trojan, evading traditional verification and Xilinx’s unused circuit identification.

TECHNICAL SKILL

Programming Languages: Verilog, SystemVerilog, Python, C++, RISC-V Assembly
Technologies/Frameworks: Verdi, PyTorch, TensorFlow, Linux, Xilinx Vivado, Vitis HLS, OOP, SPICE