Middle East Technical University

Electrical & Electronics Engineering Department

EE462 & EE464

Design of a SM-PMSM Variable Frequency Drive with Matlab/Simulink

Project Report

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Introduction

In this project assignment, we will examine a variable frequency drive used for a surface-mounted permanent magnet synchronous machine (SM-PMSM). The analysis will involve implementing field-oriented control (FOC) in MATLAB/Simulink, specifically focusing on maximum torque per ampere (MTPA) control. Additionally, we will investigate the machine's behavior in the field weakening region. Furthermore, the design and analysis of the inverter stage will be carried out.From now on, this paper continues with the pre-design stage, FOC with sinusoidal PWM, FOC with space vector PWM and component selection parts.

Part A: Pre-design Stage

1) $T_{nominal} = \frac{3}{2} * pp * \lambda_{PM} * i_q = 2550\,Nm\ where\ i_q = i_{nominal} = 1700A,\ \lambda_{PM} = 0.5Wb\ and\ pp = 2$

2) $\omega_{mech} = \frac{2\pi}{60} * n_{max} = 235.62\,rad/sec$

$\omega_{e,max} = \omega_{mech} * pp = 2\pi * f_{e,max} \Rightarrow f_{e,max} = 75Hz$

In line with the information we learned in the lesson, we decided to keep the frequency modulation ratio higher than 21 and to make the switching frequency synchronous with the electrical frequency to be 2.7kHz, in order to eliminate the harmonics that may occur during the SPWM formation.In addition, we did not keep the switching frequency very high so that the switching loss does not rise further.

3)

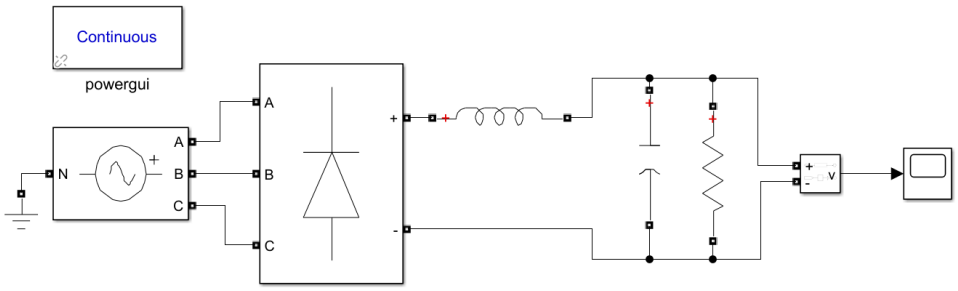


Figure 1. Schematic of rectifier and LC filter design.

1mH inductor and 470mF capacitor are used in the LC filter used to filter the DC link voltage.

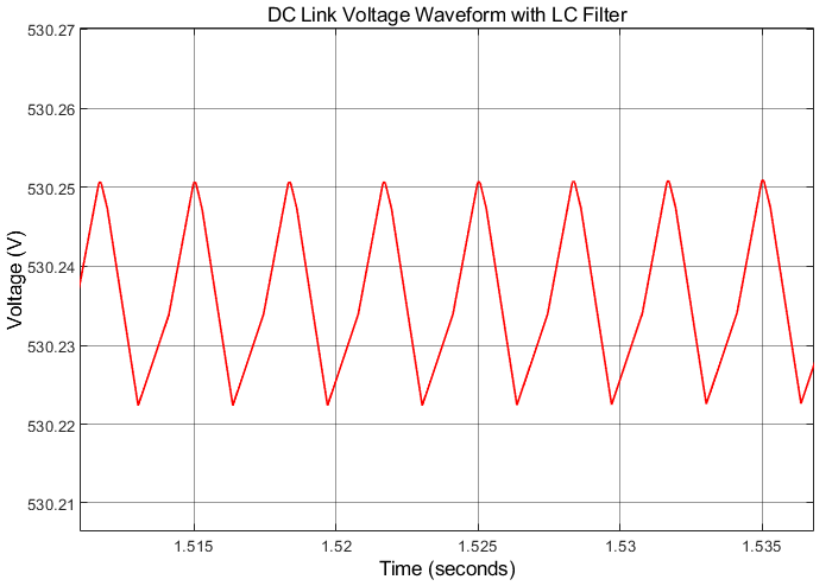
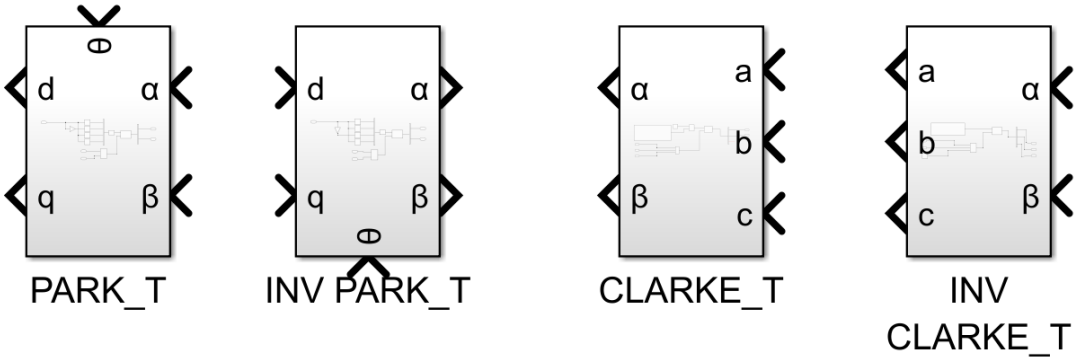


Figure 2. DC link voltage waveform.

As can be seen from the graph, the voltage ripple value formed as a result of filtering is quite small. ($Ripple = \frac{0.03}{530.204} \times 100 = 0.006\%$)

Part B: Sinusoidal PWM

In this part, the model of the motor and the load is implemented in the MATLAB™ Simulink environment. The Park transformation, Clarke transformation and inverse of these two transformations are implemented solely in Simulink, given below.



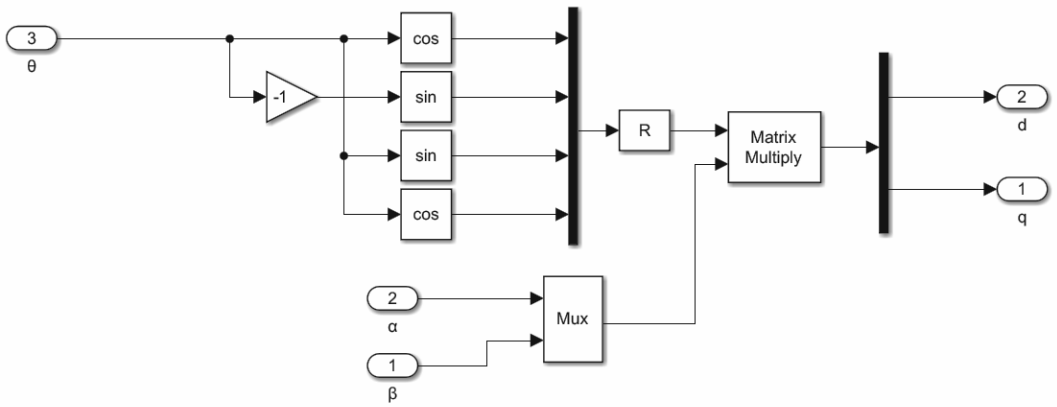


Figure 3. Park Transformation Subsystem.

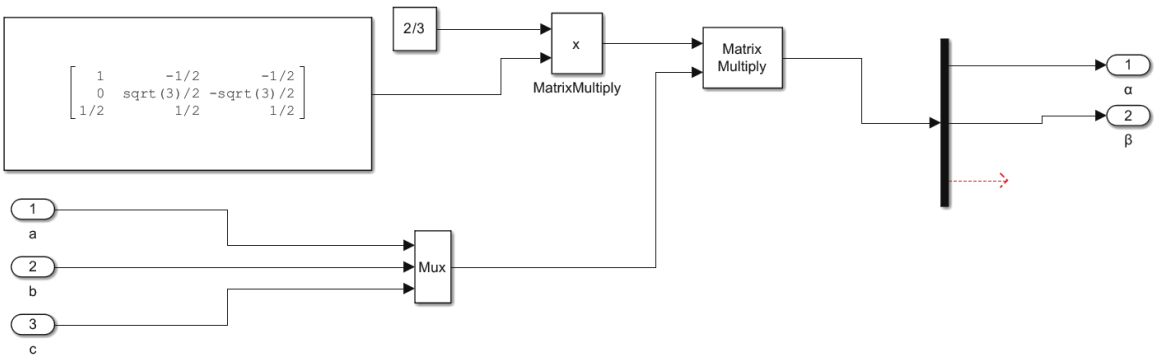


Figure 4. Clarke Transformation Subsystem.

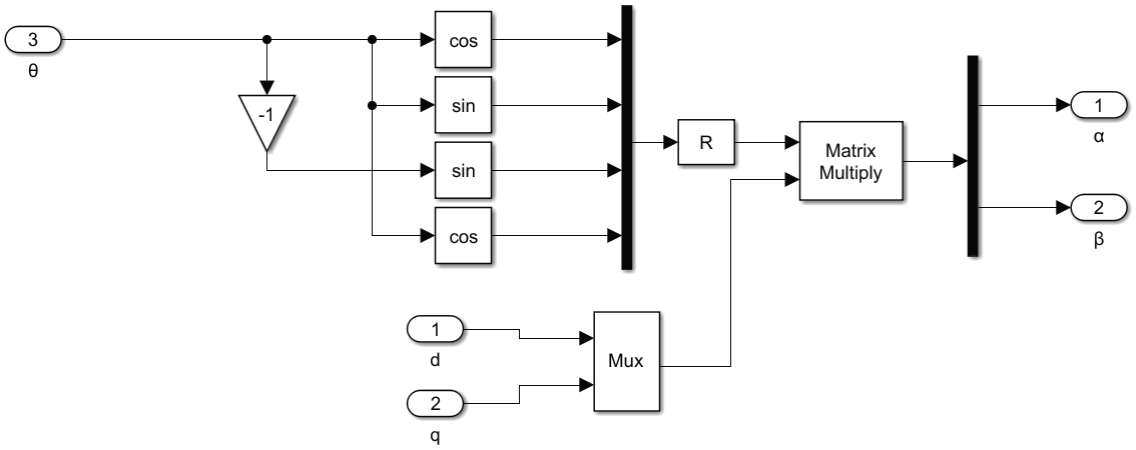


Figure 5. Inverse Park Transformation Subsystem.

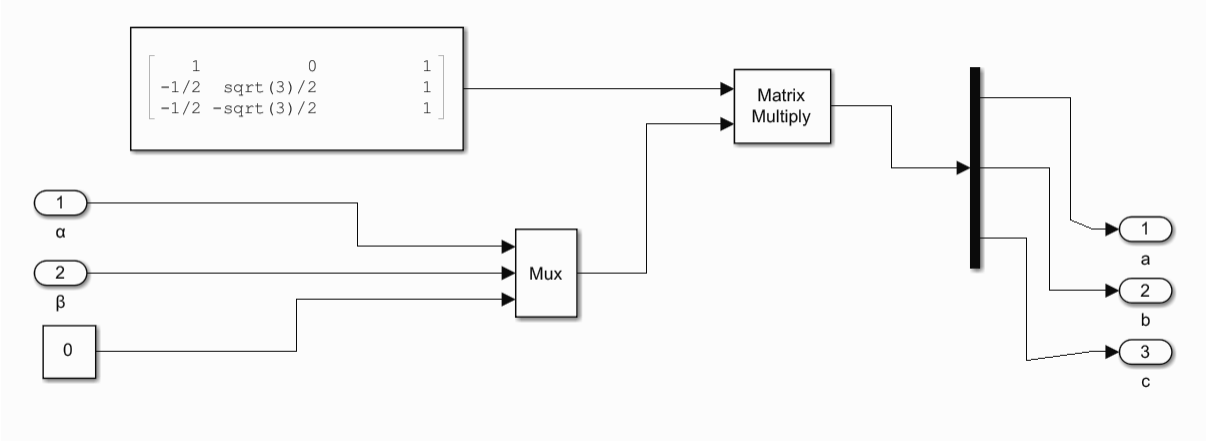


Figure 6. Inverse ClarkeTransformation Subsystem.

PWM generation block is also implemented in Simulink with configuration as shown,

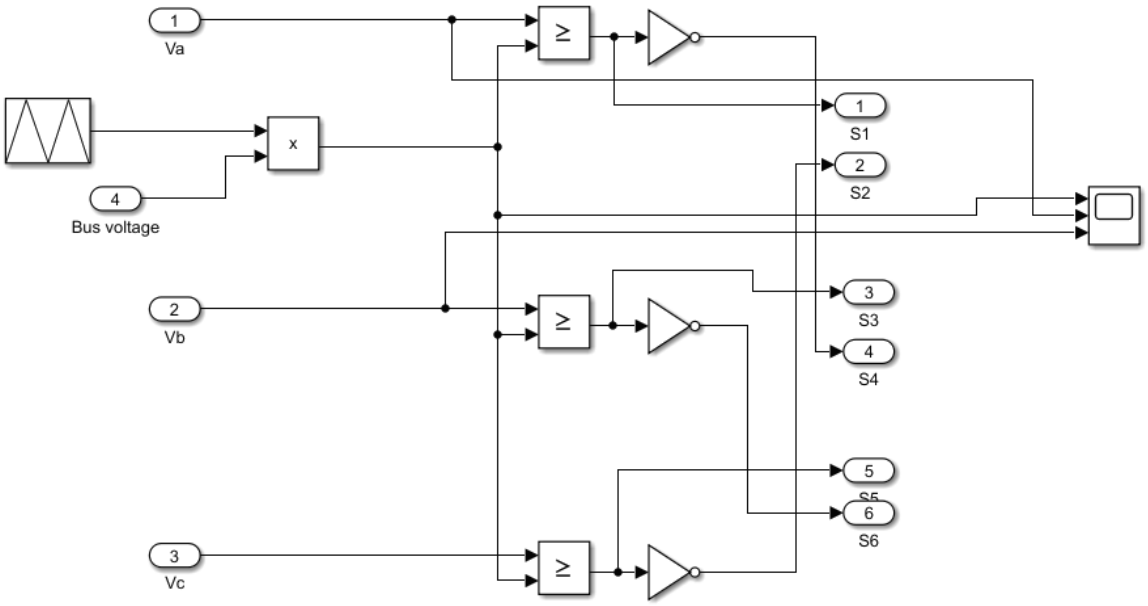
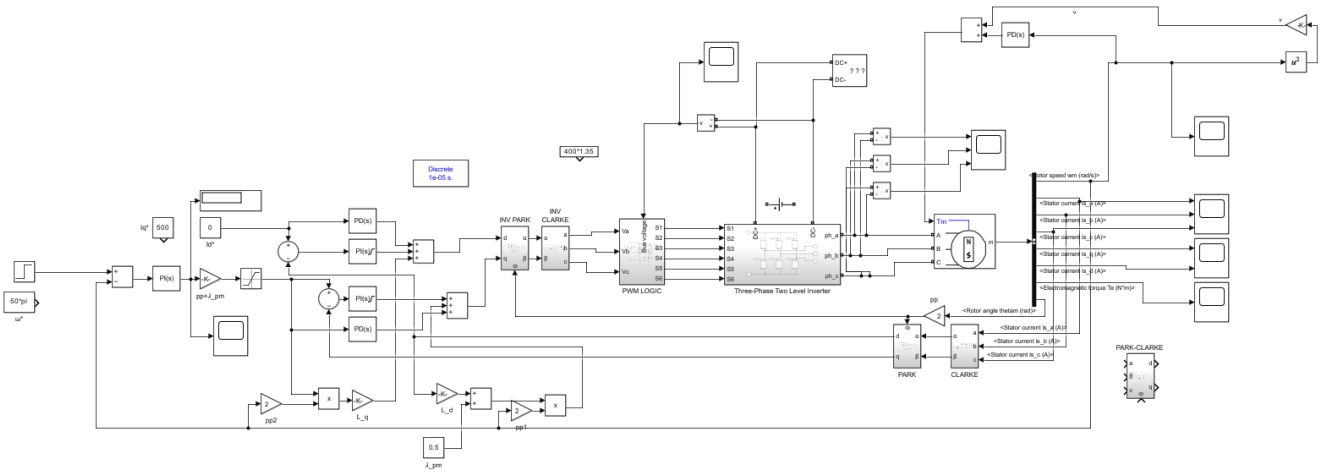
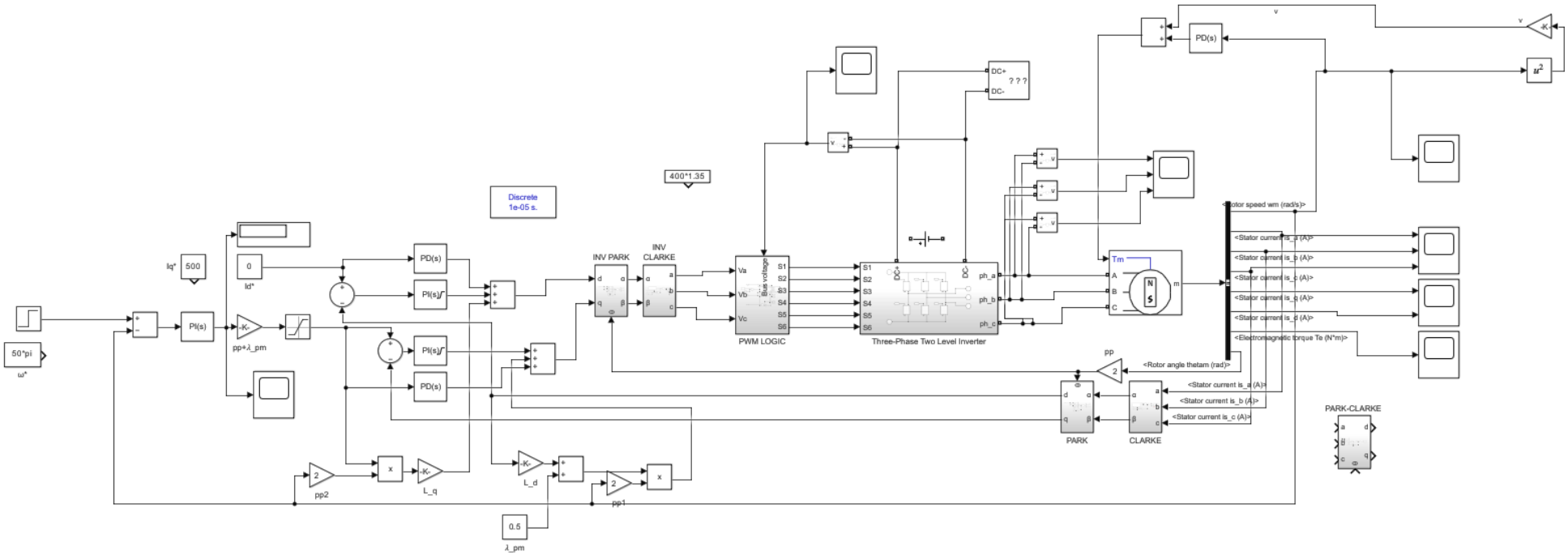


Figure 7. PWM Generation Subsystem.

The whole system is given below configured for the first part, feedforward blocks capturing the inverse machine model are included.




Discrete
1e-05 s.
400*1.35
50*pi
ω*
Iq*
500
Id*
0
PI(s)
-K-
pp+λ_pm
PD(s)
PI(s)
PD(s)
PI(s)
PD(s)
INV PARK
INV
CLARKE
PWM LOGIC
Three-Phase Two Level Inverter
DC+
DC-
? ? ?
Tm
A
B
C
m
N
S
<Rotor speed wm (rad/s)>
<Stator current is_a (A)>
<Stator current is_b (A)>
<Stator current is_c (A)>
<Stator current is_q (A)>
<Stator current is_d (A)>
<Electromagnetic torque Te (N*m)>
pp
2
<Rotor angle thetam (rad)>
<Stator current is_a (A)>
<Stator current is_b (A)>
<Stator current is_c (A)>
PARK
CLARKE
PARK-CLARKE
2
pp2
x
-K-
L_q
-K-
L_d
2
pp1
x
0.5
λ_pm
PD(s)
-K-
u²

1) The first part consists of fan load with a transient speed input from 90% to rated speed which is 157.08 rad/s.

a)

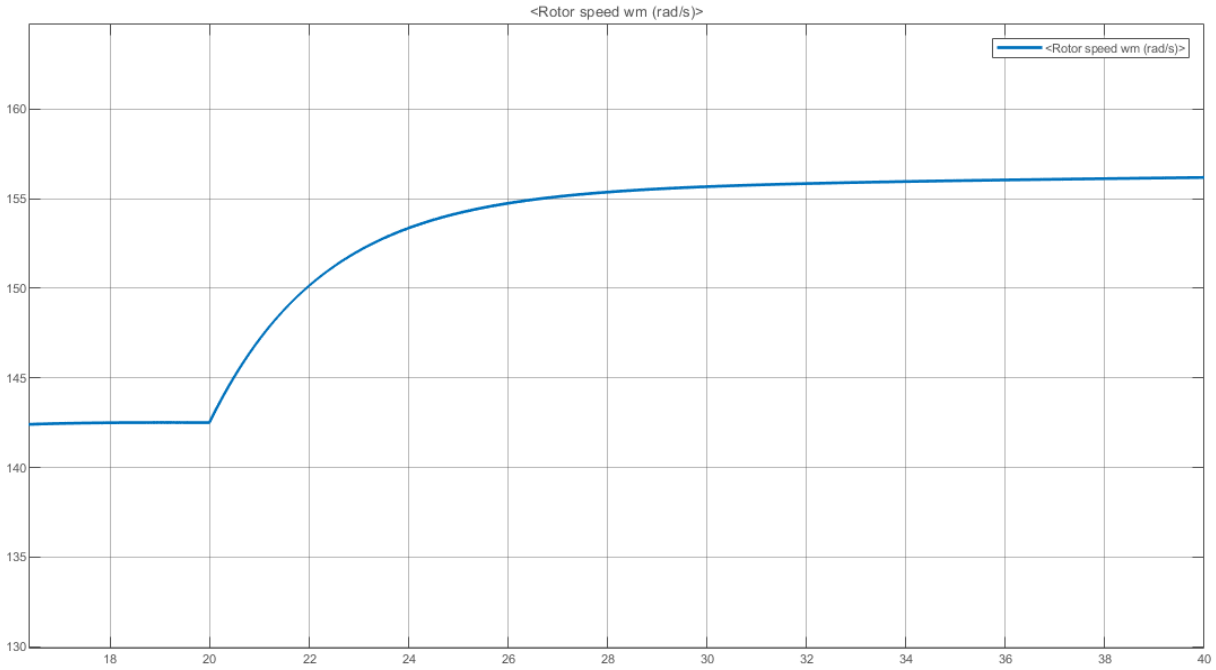


Figure 8. Rotor speed vs time graph of PMSM.

Note that this is a section of the whole time plot in which the rotor is sped up to the 90% of the rated speed, which can be seen below.

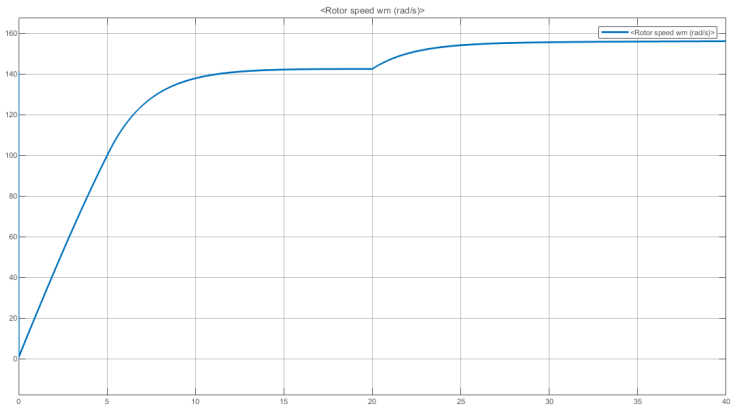


Figure 9. Rotor speed vs time graph of PMSM for the whole simulation time.

b) Transient phase currents for this test are given below.

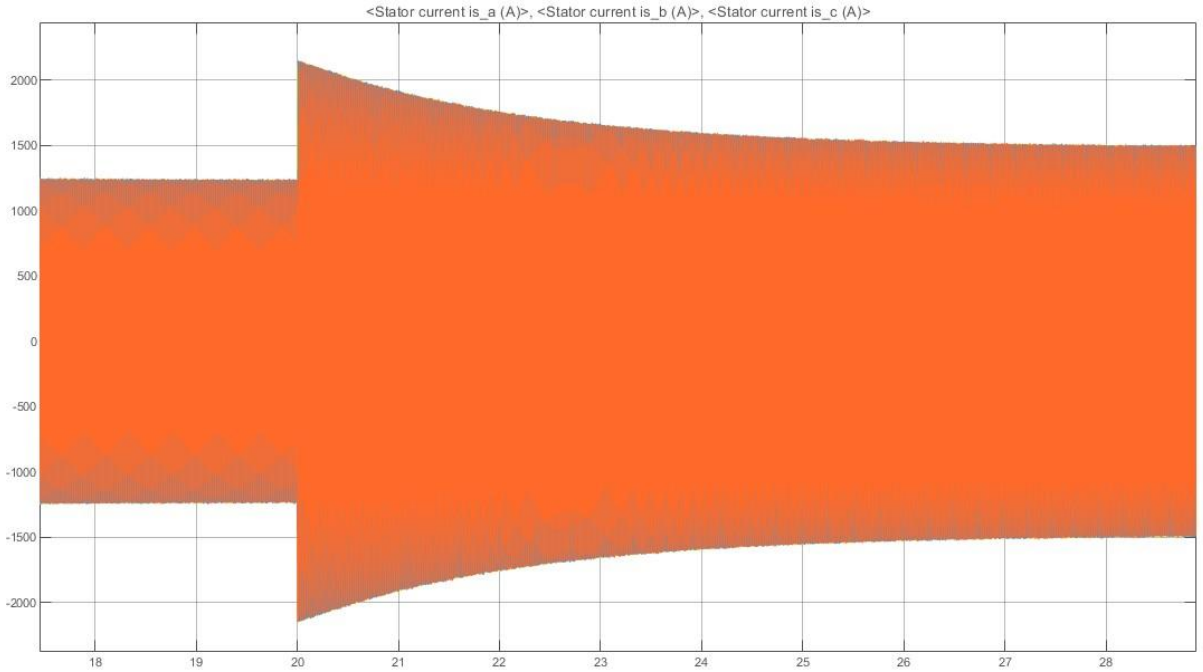


Figure 10. Phase currents vs time graph of PMSM.

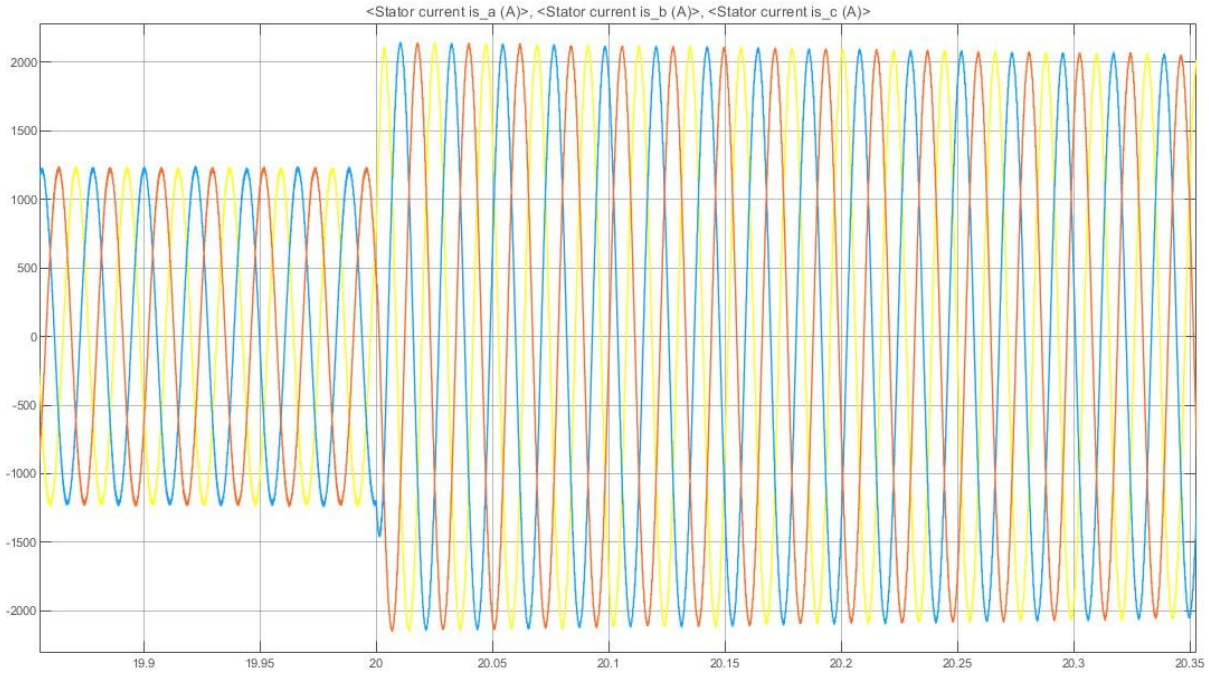


Figure 11. Phase currents vs time graph of PMSM for a small transient step.

Transient phase voltages for this test are given below.

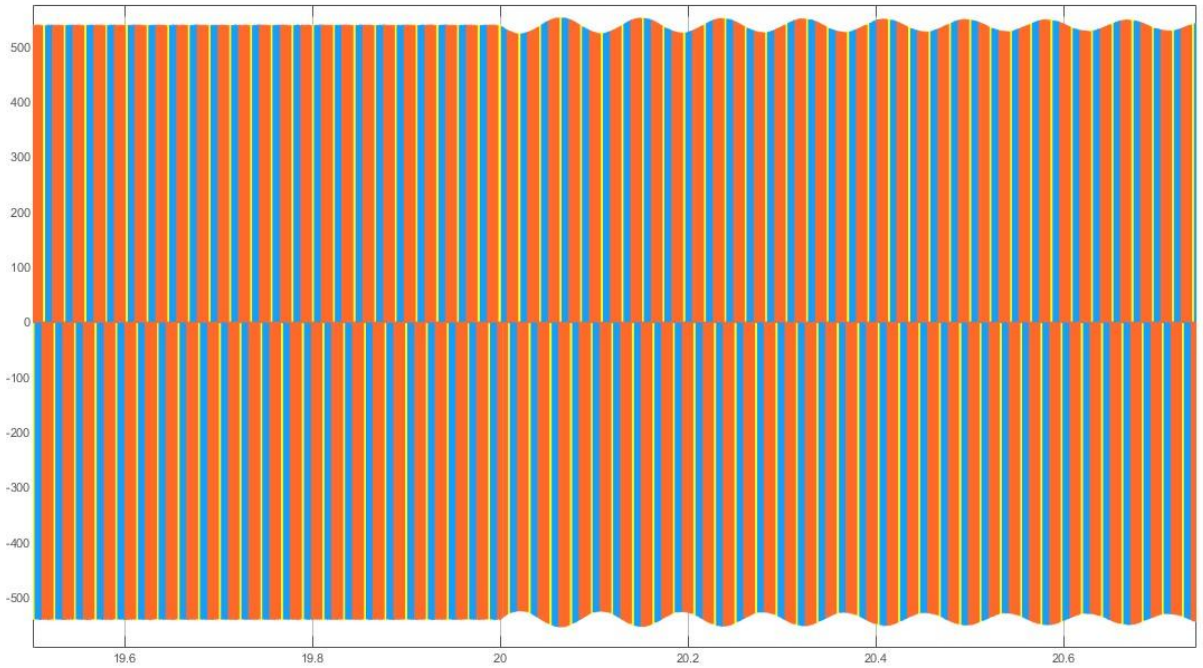


Figure 12. Phase currents vs time graph of PMSM.

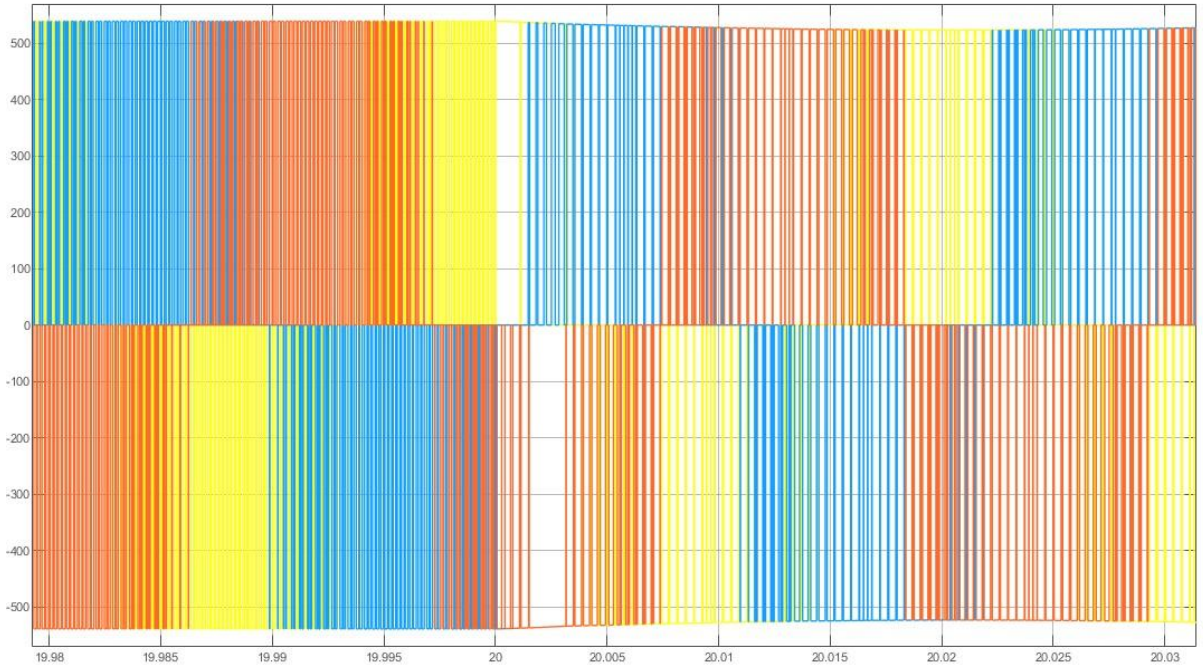


Figure 13. Phase voltages vs time graph of PMSM for a small transient step.

c)

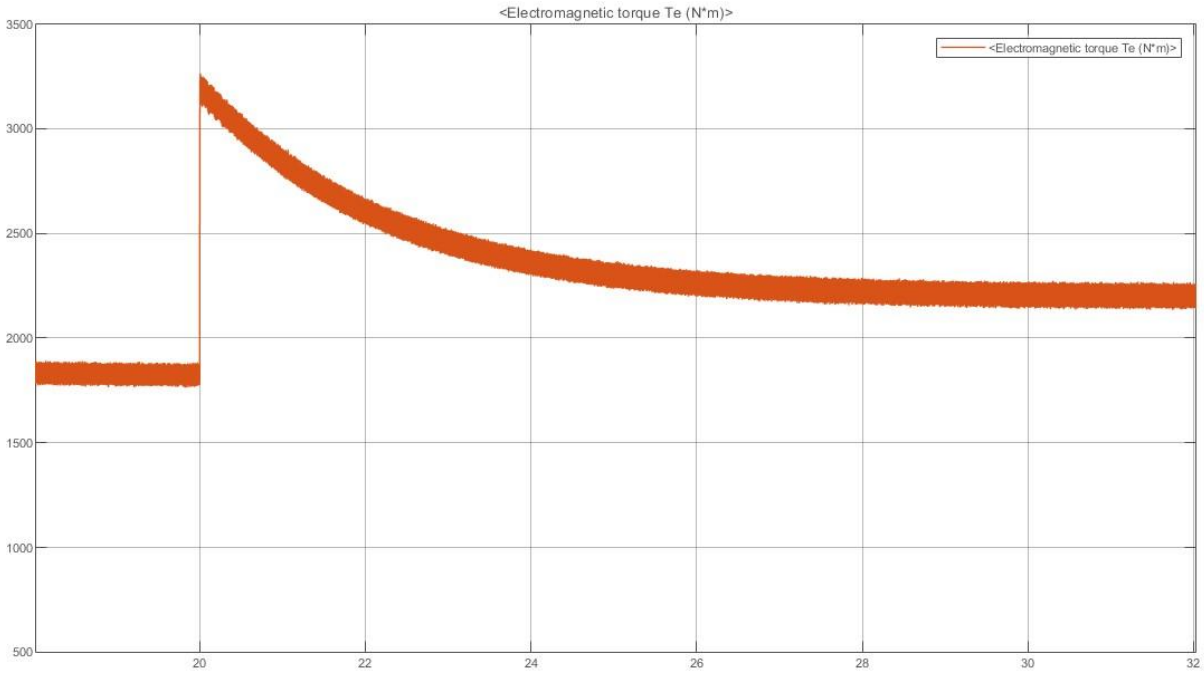


Figure 14.Torque vs time graph of PMSM.

d)

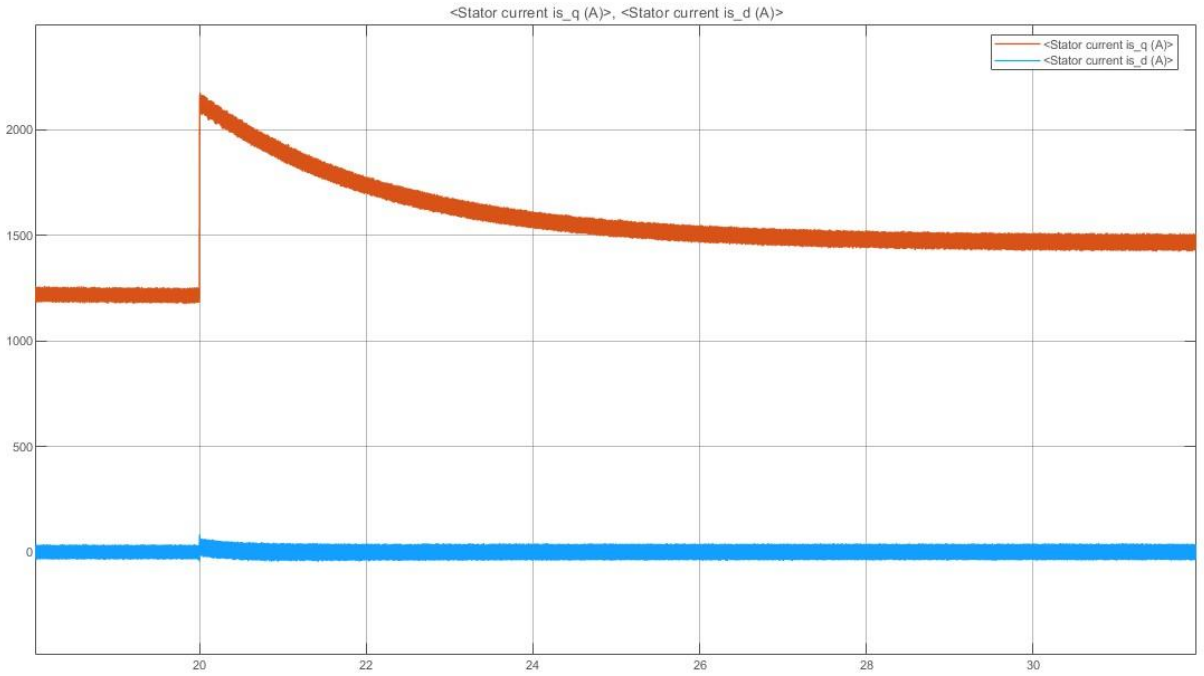


Figure 15. I_d and I_q vs time graph of PMSM.

e) For this condition which is rated load speeding up to the rated speed from 10% less takes around 25 seconds with adequate PI parameters for the speed loop. The current loop is much faster than this hence its effect can not be seen from the plots given in larger time intervals.

2) This test consists of removing the load at an instance and shows the controllers performance. Without any modifications to the PI parameters the response is as given below.

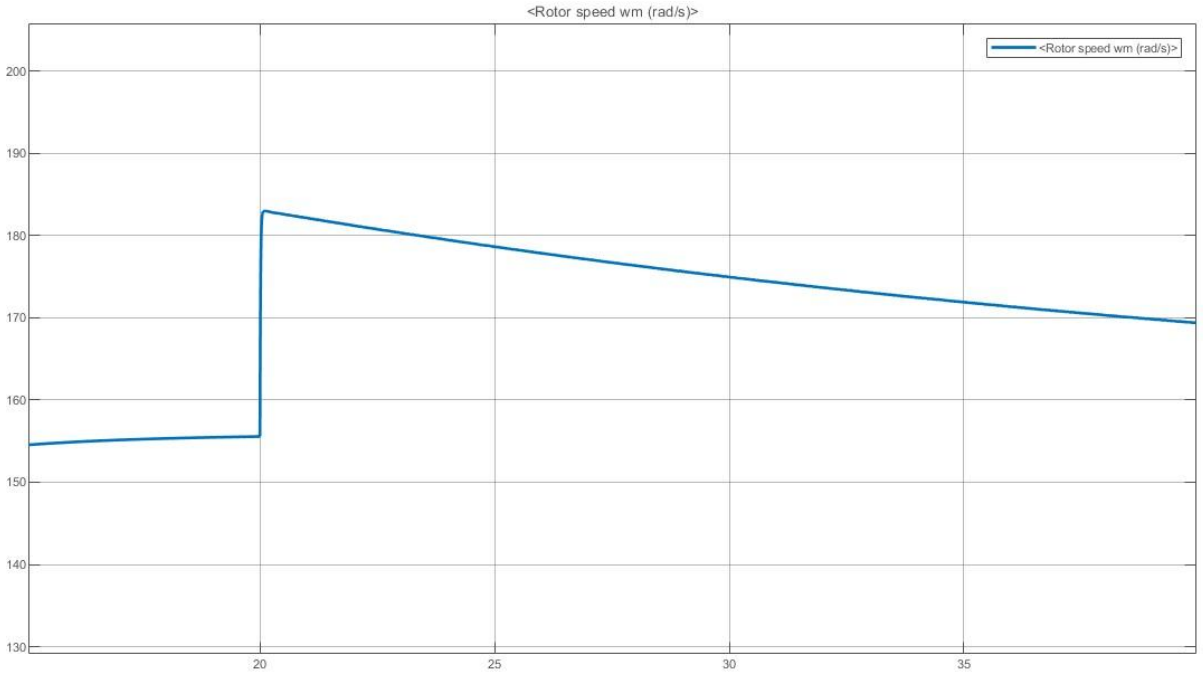


Figure 16. Rotor speed vs time graph of PMSM.

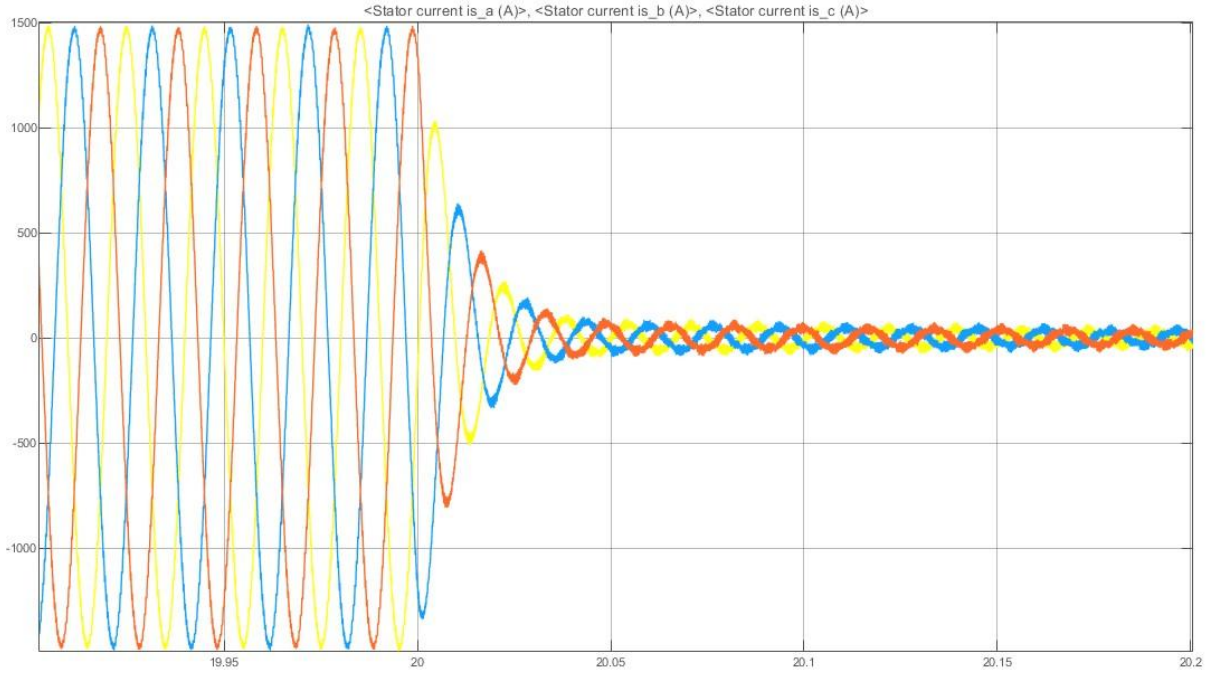


Figure 17. Phase current vs time graph of PMSM.

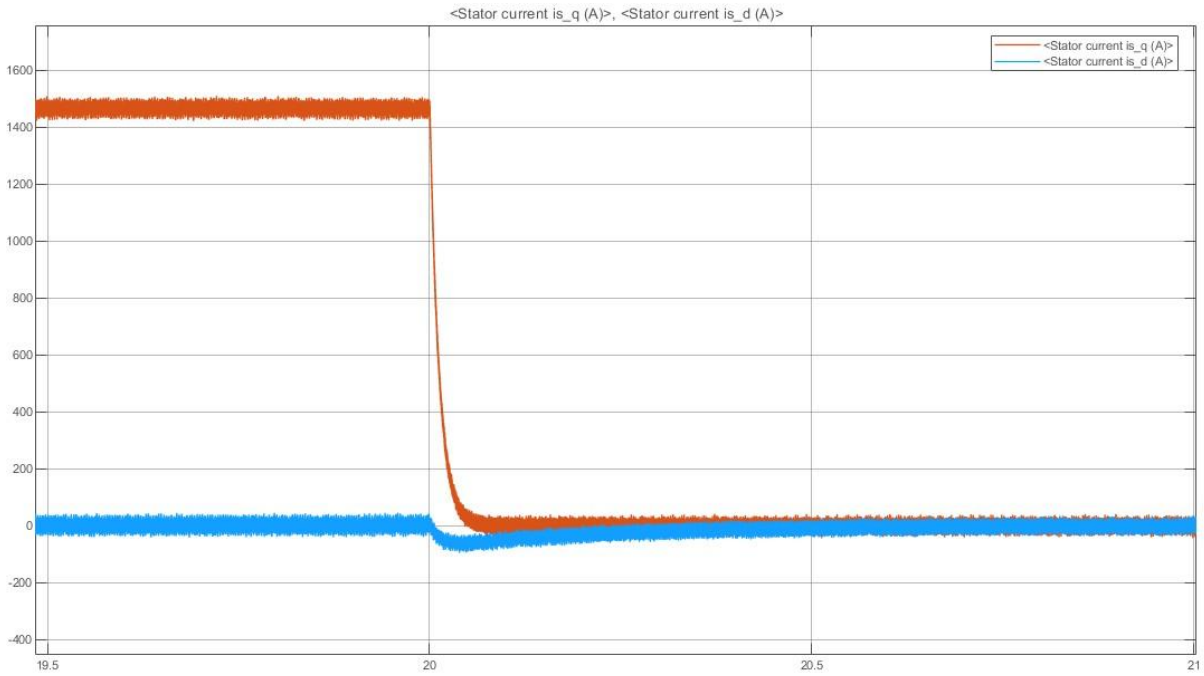


Figure 18. I_d and Iq vs time graph of PMSM.

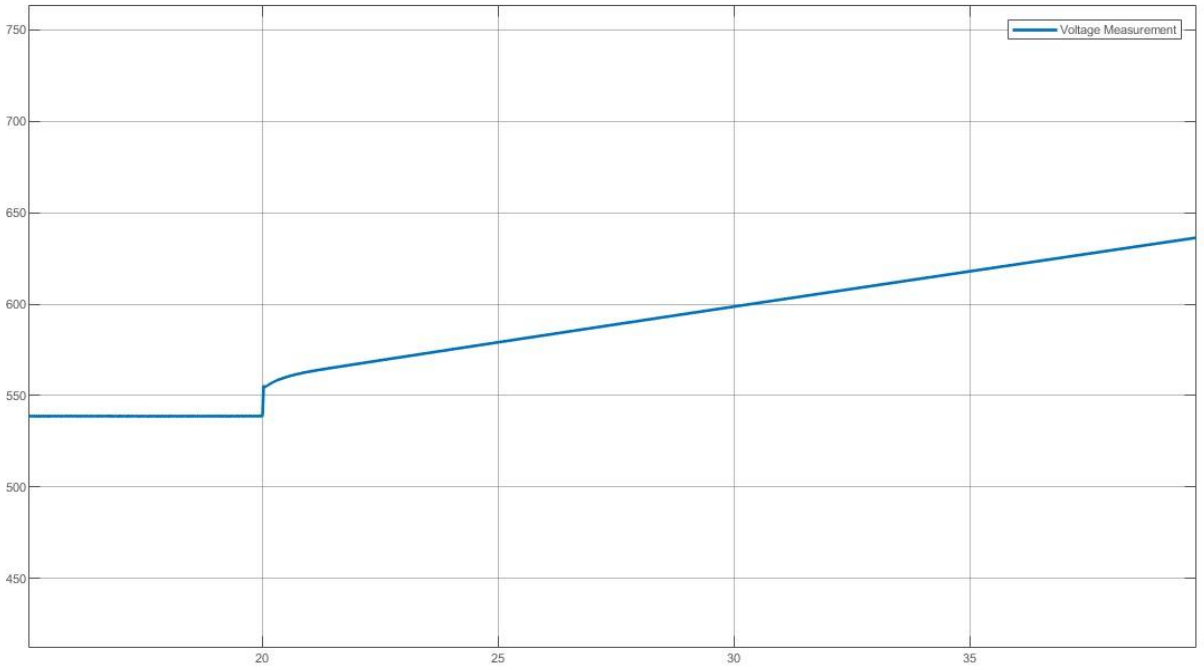


Figure 19. DC bus voltage vs time graph of PMSM.

For a better performance, the PI parameters can be altered at the load removal instance. The figures below show the systems' response with changed parameters adjusted for no load condition.

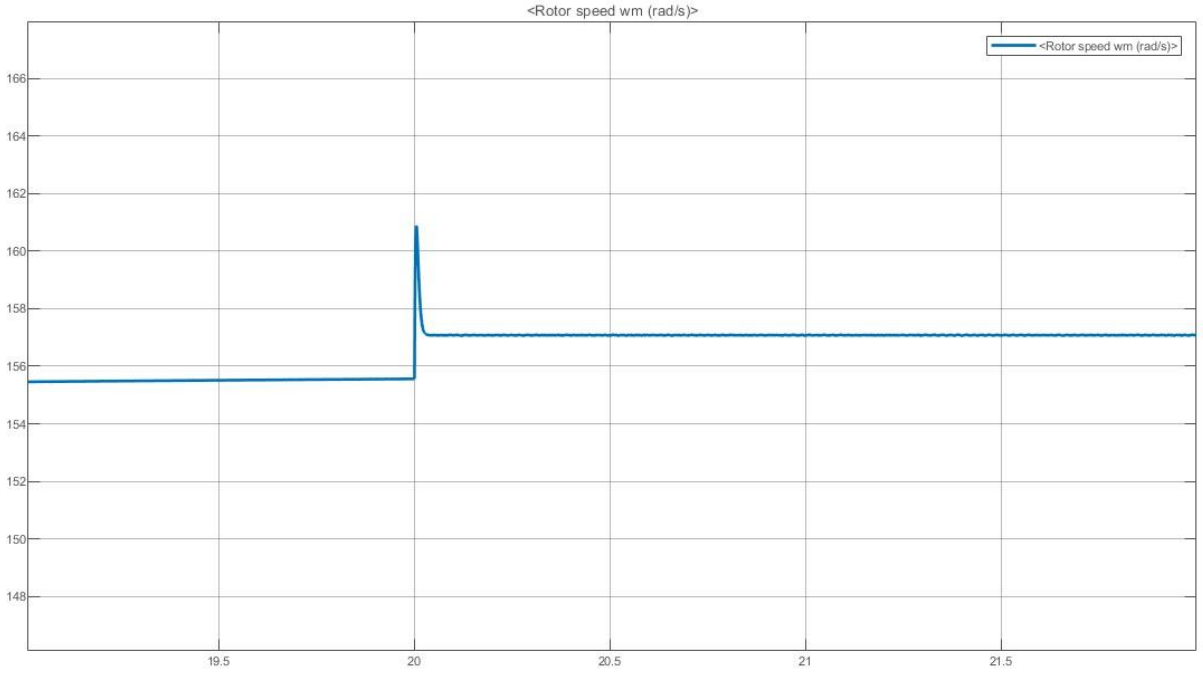


Figure 20. Rotor speed vs time graph of PMSM.

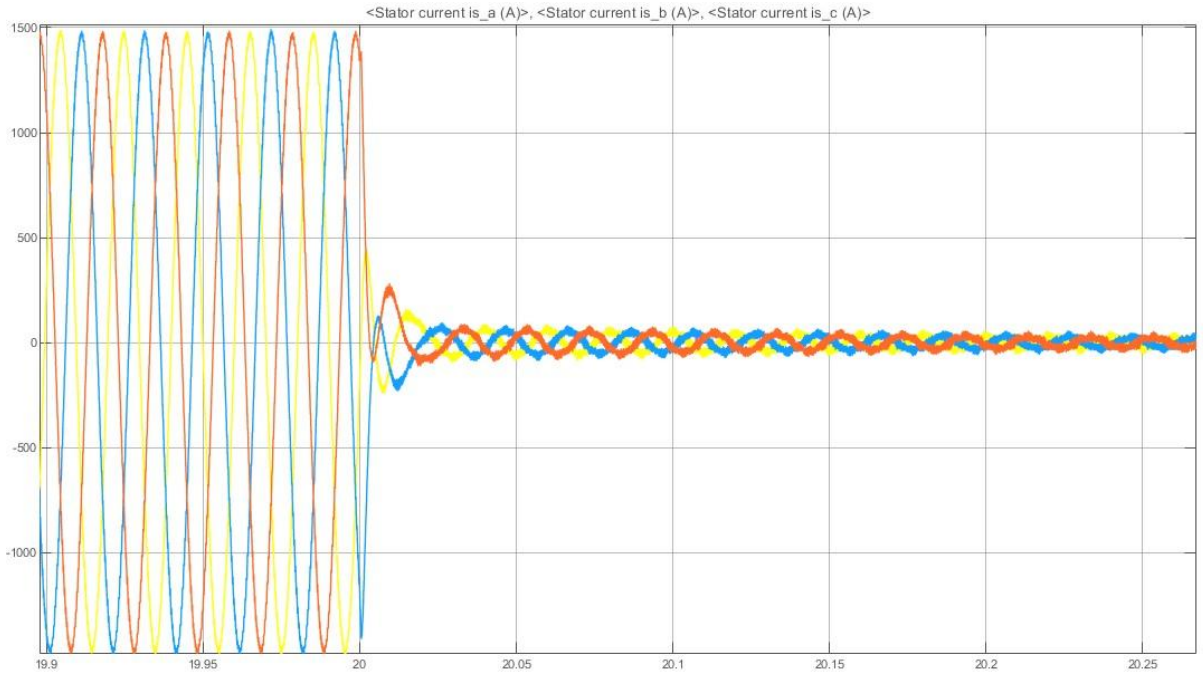


Figure 21. Phase current vs time graph of PMSM.

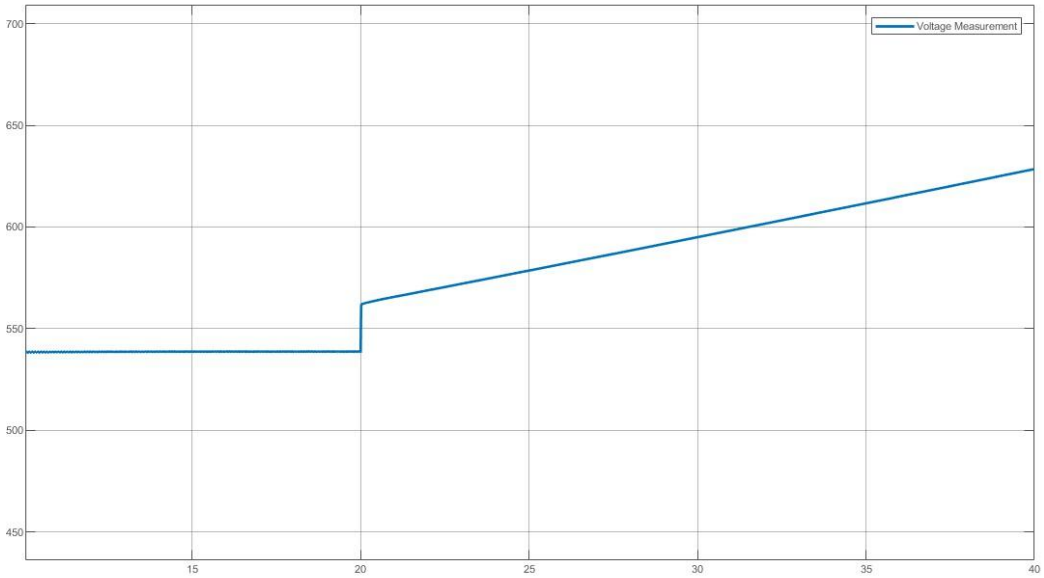


Figure 22. DC bus voltage vs time graph of PMSM.

3) Plugging, speed reversal operation is tested for this part. Its effects on the DC bus voltage is observed.

The diode rectifier passes energy in one way only, it can not be used to transfer power to the grid side. For operations that effectively generate energy the DC bus capacitors will hold the excess. This excess energy increases the voltage over the capacitors and may result in failure. Braking resistors are used to dissipate this excess energy in terms of heat over the resistor and protects the capacitors and rectifier from the high voltages.

a) The speed reversal operation is given below, the response is acceptable.

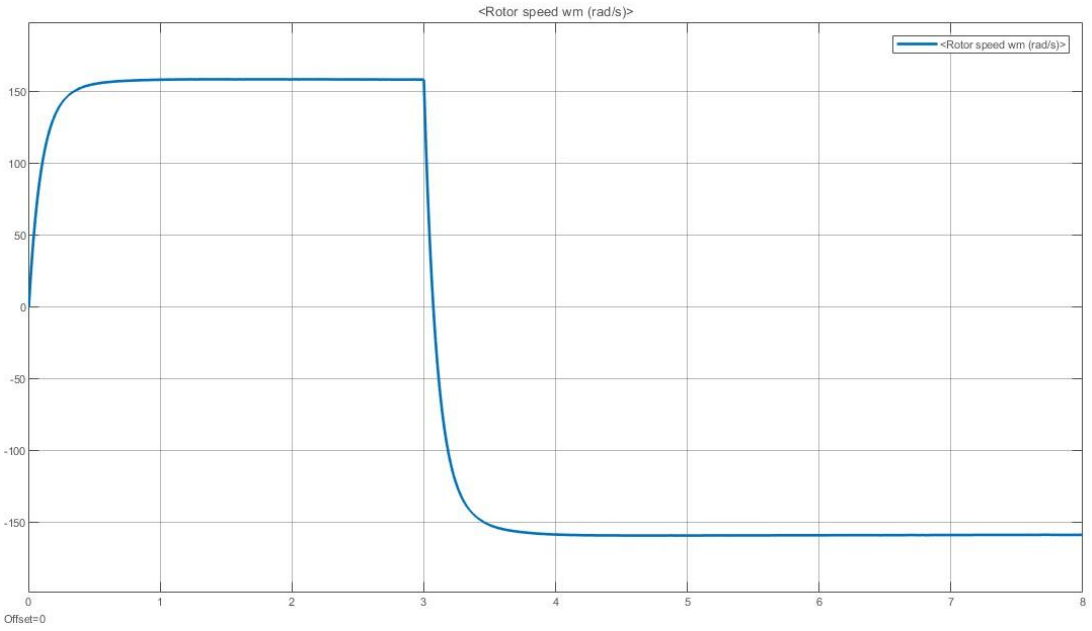


Figure 23. Rotor speed vs time graph for speed reversal.

b) The current waveform shows that in the transient the required torque is quite high. Also the current sequence change can be observed with the current plot below, which means that indeed the speed is reversed.

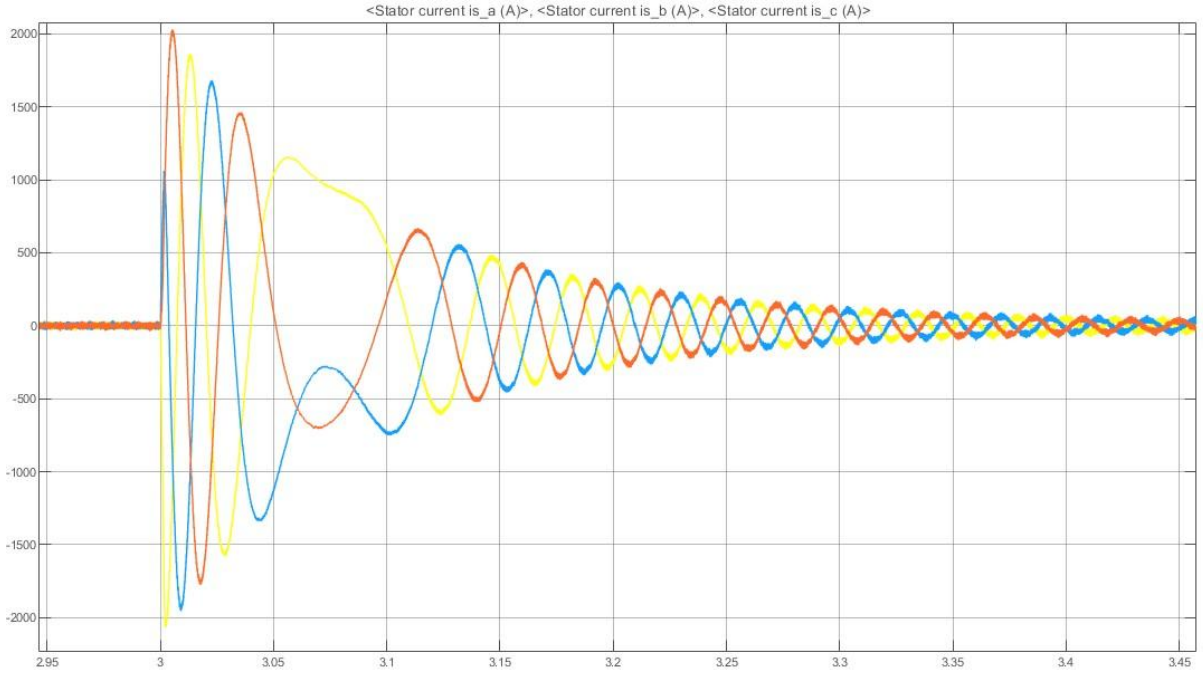


Figure 24. Rotor currents vs time graph for speed reversal.

Large amount of negative torque is applied in order to reduce the speed of the motor to zero, which takes around 75 milliseconds, and again the reverse torque speeds up the motor in the reverse direction. The applied q-axis current is given below.

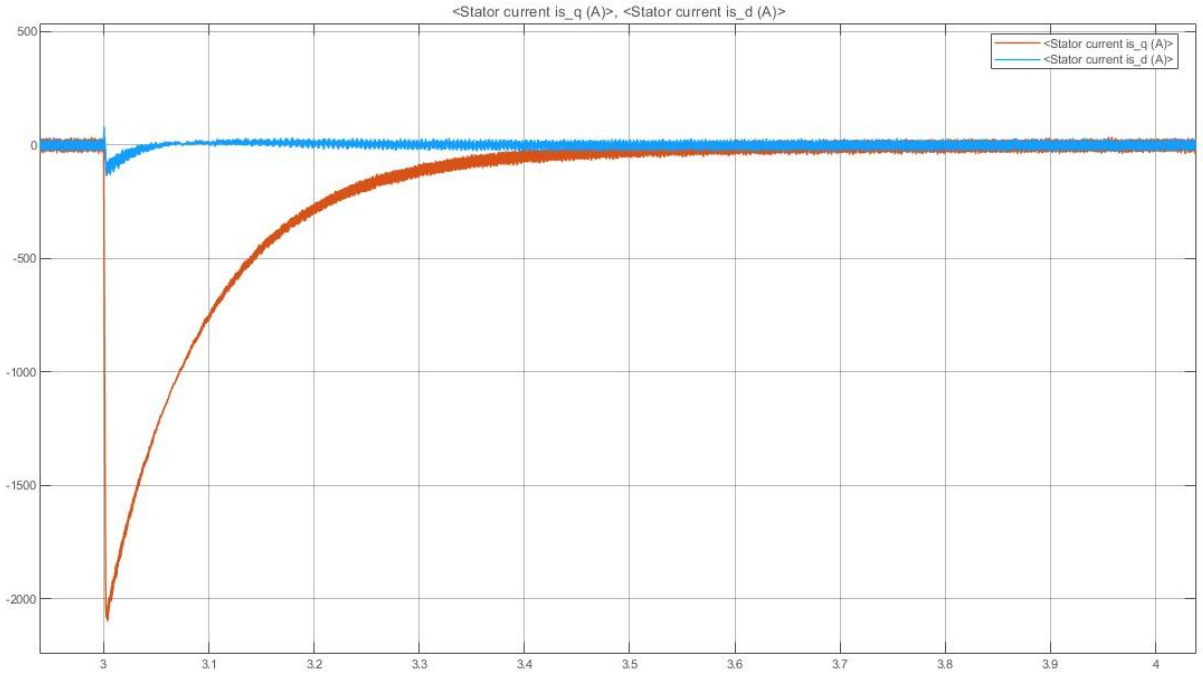


Figure 25. I_q and I_d vs time graph for speed reversal.

Since the back-emf of the motor is reversed the response of the voltage over the motor is reflected to the inverter. The body diodes of the mosfet/IGBT branches effectively help the current to pass through and store over the DC bus capacitors hence the voltage is increased.

The hysteresis voltage controller is implemented in Simulink to keep the voltage at 600V for the fourth quadrant operation. Basically it turns on the load resistor whenever the voltage of the DC bus is higher than a threshold. The selected resistor is 1 Ohms that is plenty enough to effectively reduce the voltage of the capacitor and has a capability of tolerating large amounts of energy to be dissipated for occasions such as regenerative braking or speed reversal.

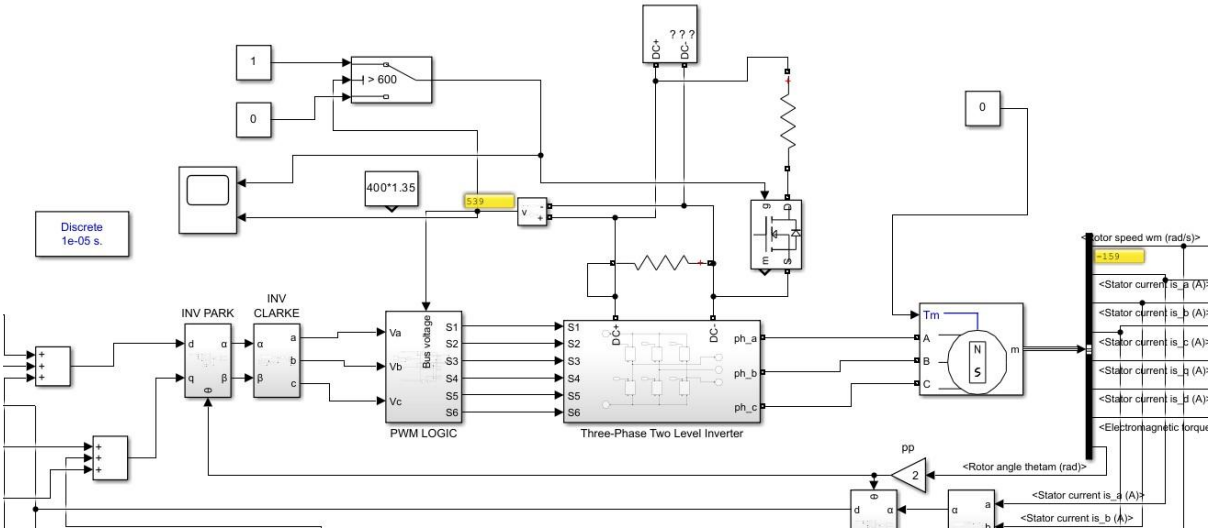


Figure x. System configuration with braking resistor controlled by hysteresis controller.

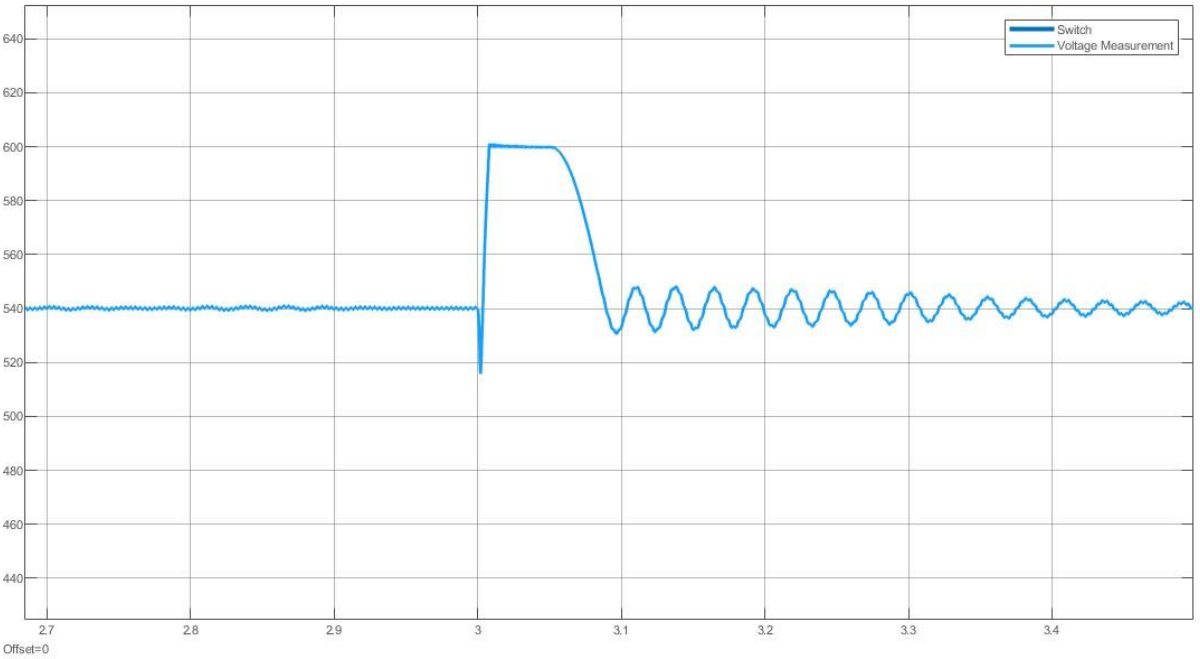


Figure 26. DC bus voltage vs time graph for speed reversal.

4) In this part of the project, the motor is running at half of the rated torque, which was calculated as 2550 Nm, the half is 1275 Nm.

$$\frac{T_{rated}}{2} = 1275 = \frac{3}{2} * pp * \lambda * Iq$$

$$1275 = \frac{3}{2} * 2 * 0.5 * I_q$$

For higher speeds such as 150% voltage is limited hence we should apply field weakening. The modulation technique is selected as SPWM, hence the maximum voltage that can be applied to the phase is half of the DC bus, measured as $\frac{540}{2} = 270\,V$. The required I_d is calculated from the voltage relations and the maximum value.

$$V_d = R_s * I_d - \omega_e * L_q * I_q$$

$$V_q = R_s * I_q + \omega_e * L_d * I_d + \omega_e * \lambda_f$$

$$\sqrt{V_d^{\,2} + V_q^{\,2}} = 270\,V$$

$$\omega_e = 50 * \pi * pp * 1.5 = 471.23\,rad/s$$

$$I_d = -119.24\,A$$

On the MATLAB™ Simulink, the speed reference is set to the rated value and the system is initiated. At a random point the speed reference is set to 150% with I_d reference updated as $-119.2\,A$. The load torque is set to $1275\,A$ and the I_q become $850\,A$.

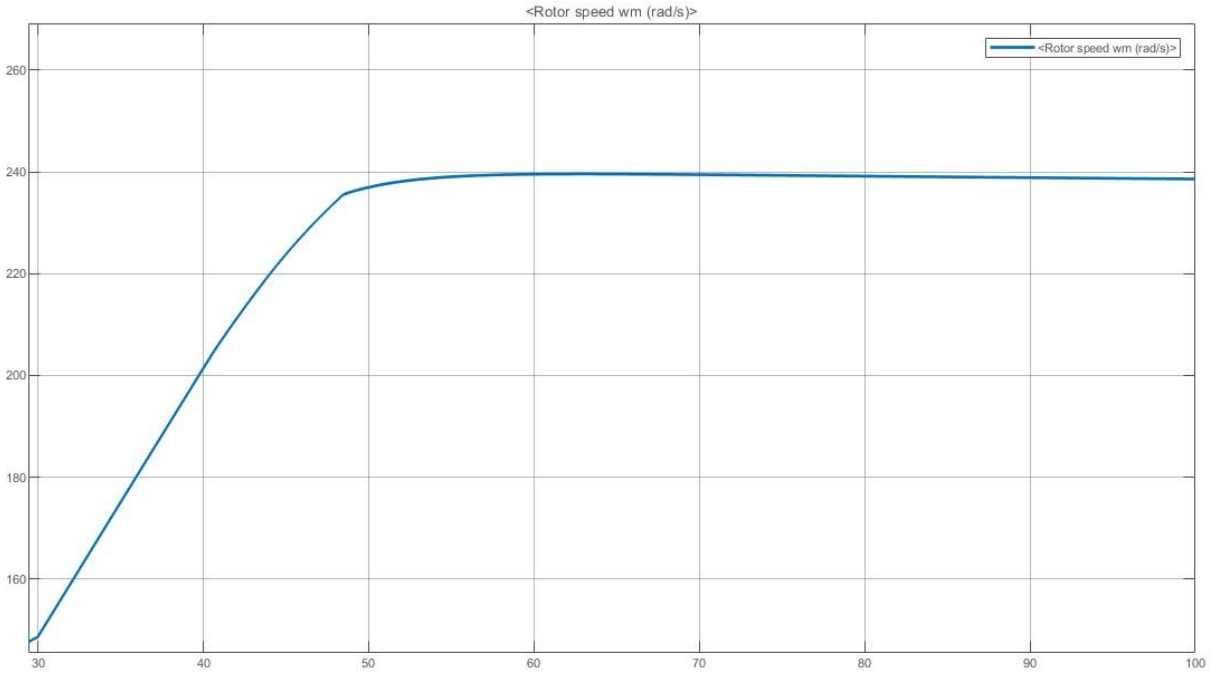


Figure 27. Speed vs time graph for field weakening operation.

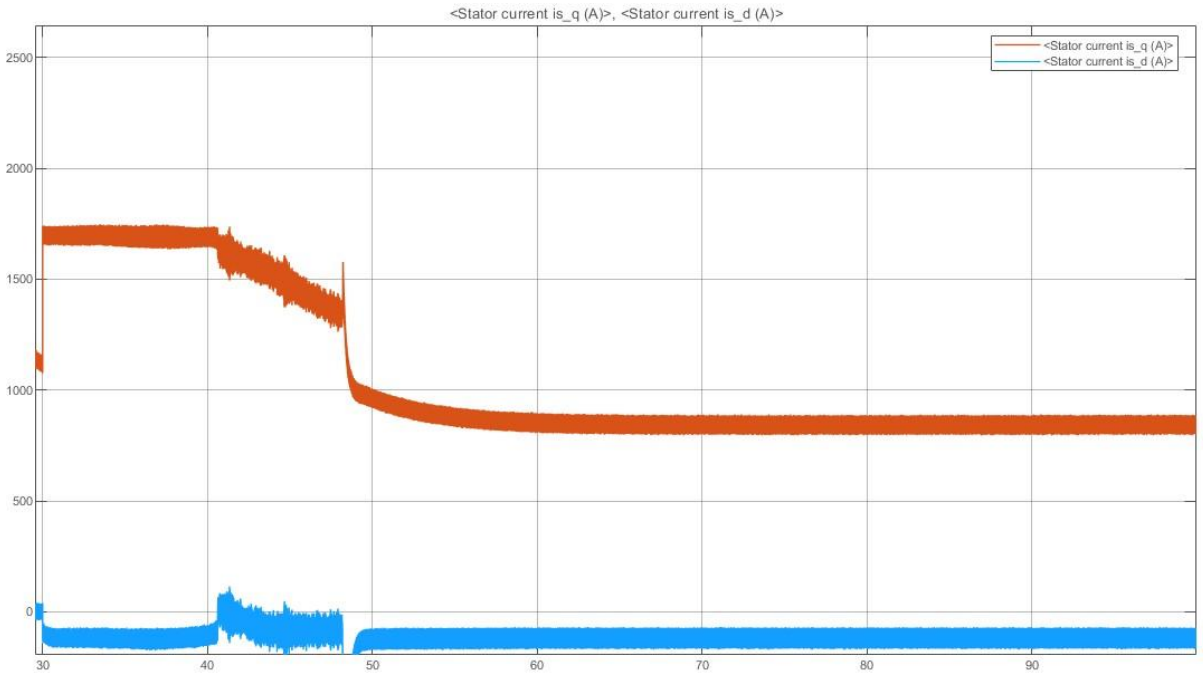


Figure 28. I_d and I_q vs time graph for field weakening operation.

Part C: Space Vector PWM (SV-PWM)

For this part of the project, the model in figure x was used. A ready generator block is used for SVPWM.

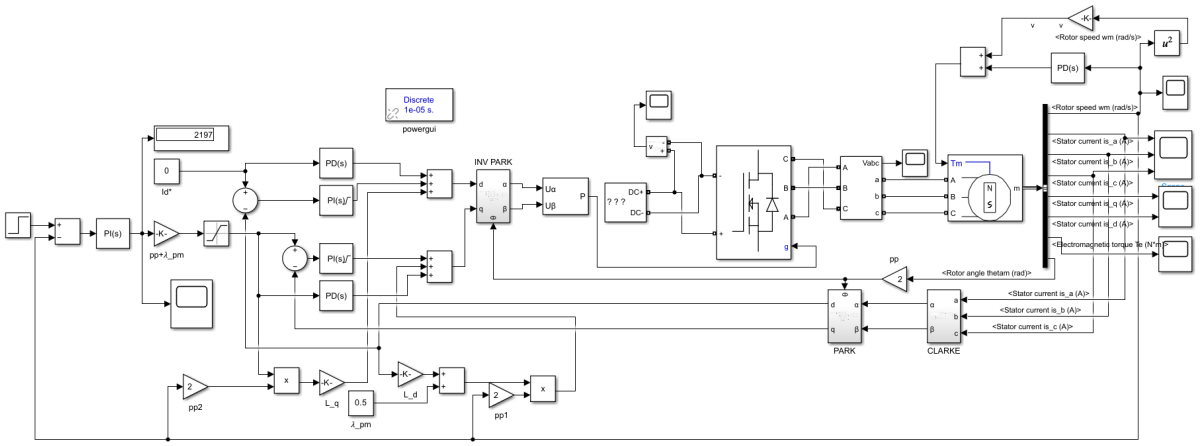


Figure 29. Simulink model of PMSM control by using SVPWM.

1)

a)

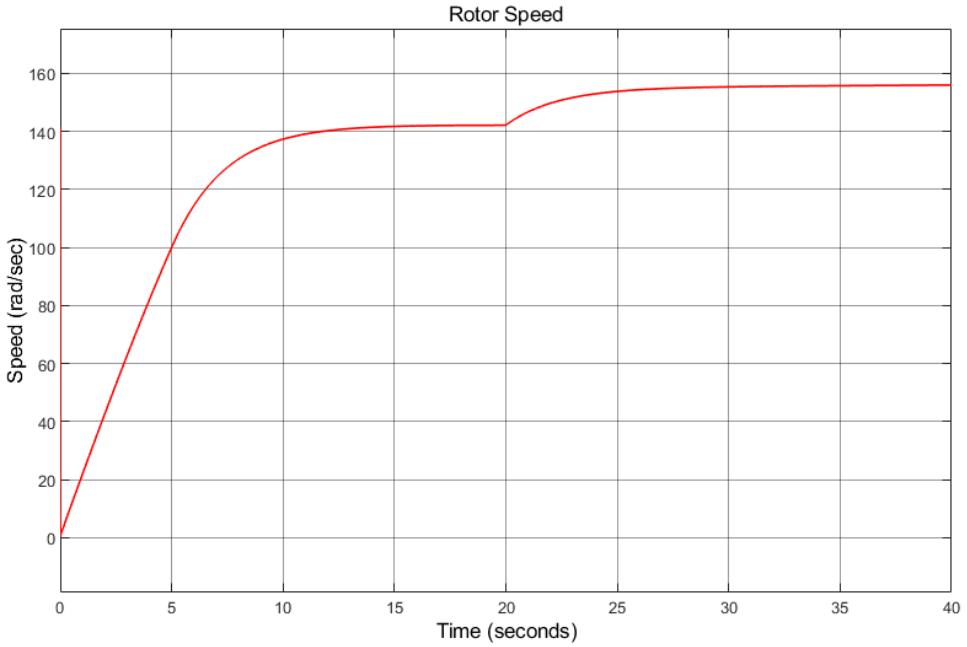


Figure 30. Rotor speed vs time graph of PMSM.

b)

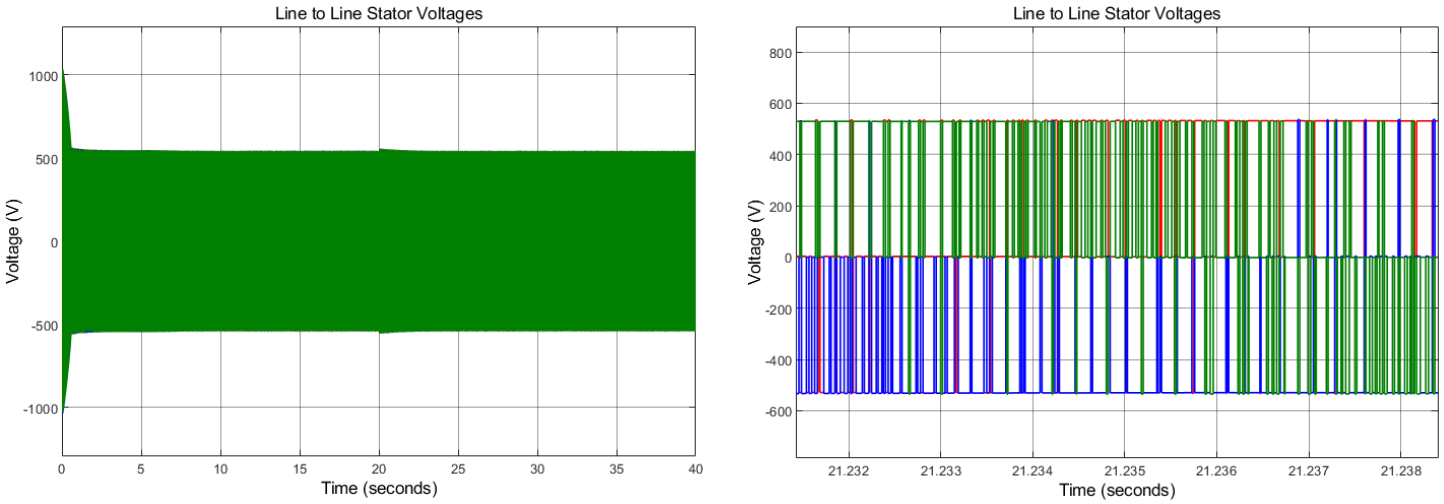


Figure 31. Line to line stator voltage waveforms of PMSM.

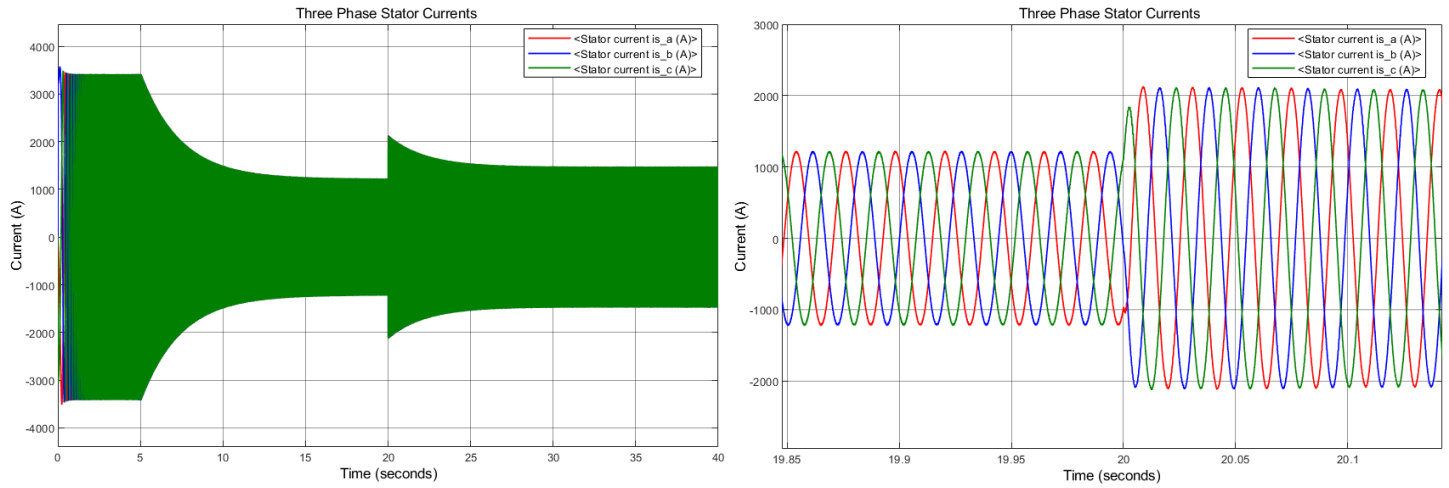


Figure 32. Three phase stator current waveforms of PMSM.

c)

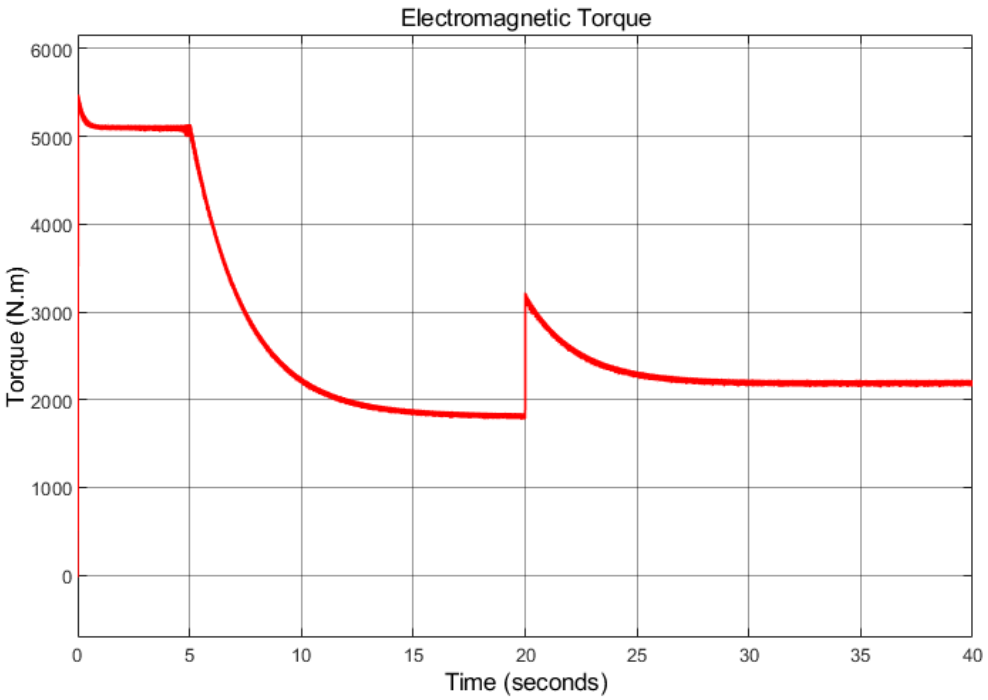


Figure 33. Electromagnetic torque vs time graph of PMSM.

d)

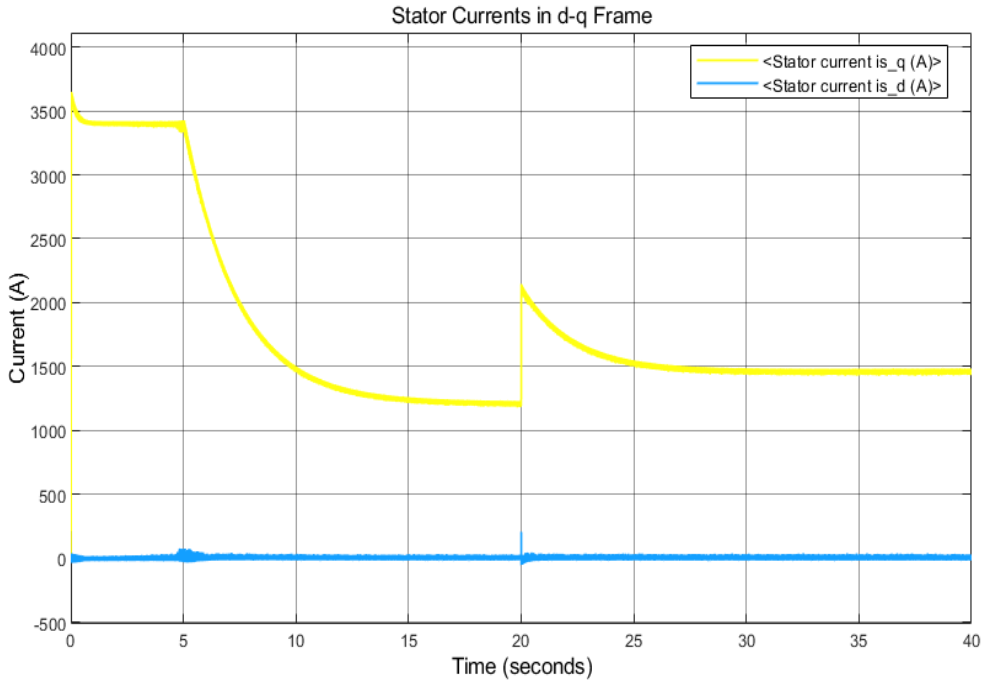


Figure 34. Iq and Id waveforms of PMSM.

2)

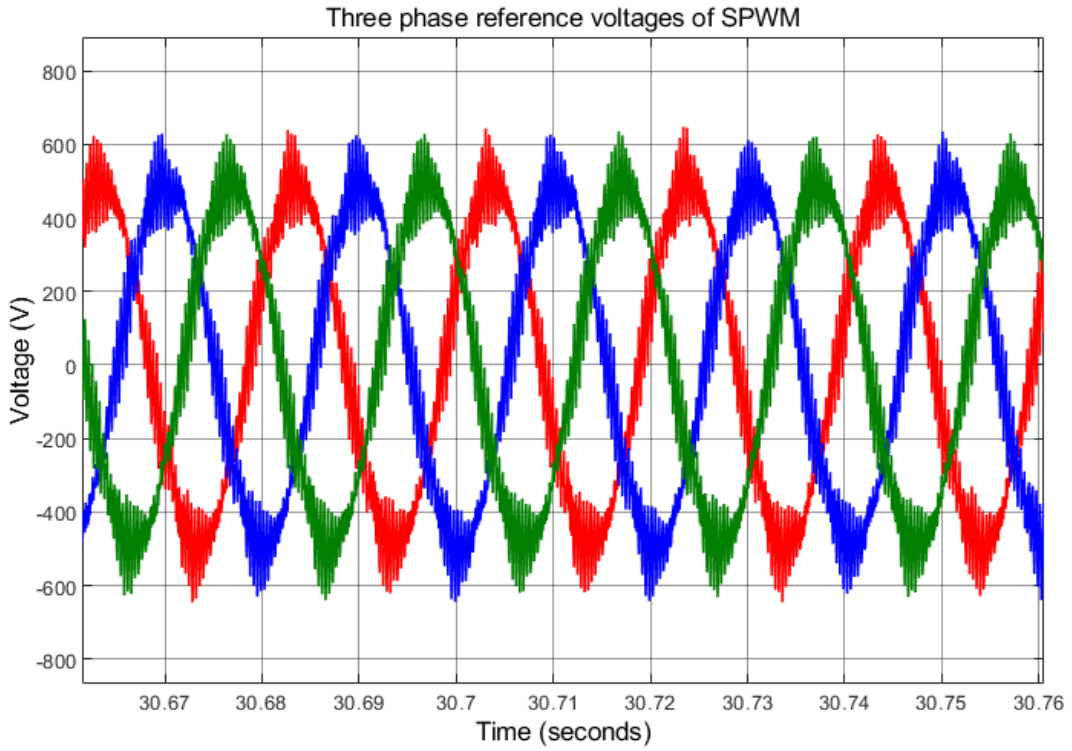


Figure 35. Three phase reference voltage waveforms of SPWM.

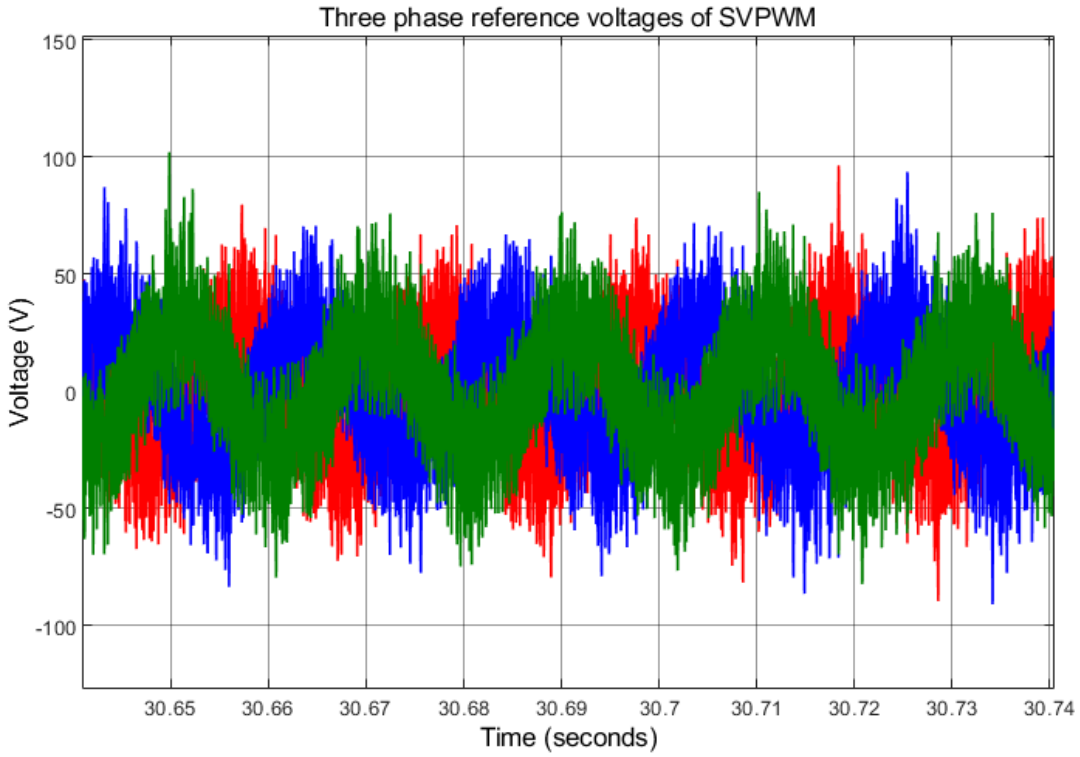


Figure 36. Three phase reference voltage waveforms of SVPWM.

For SPWM reference voltages, each waveform is a pure sine wave with the same frequency and phase.The amplitude of the sine wave is typically fixed at the peak value of the DC bus voltage.
However, the reference voltage waveforms for the three phases in SVPWM can differ in amplitude and phase.The magnitude and timing of these voltage vectors vary for each phase, resulting in different reference voltage waveforms.

3)

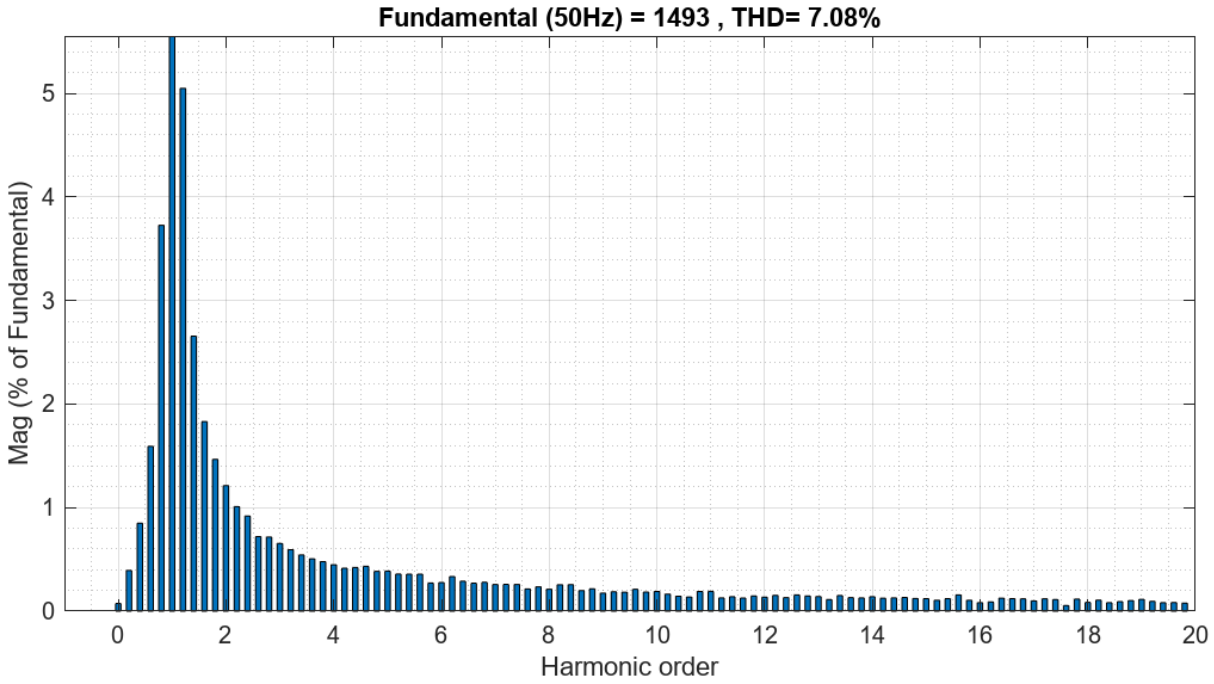


Figure 37. FFT analysis graph of line current with SPWM.

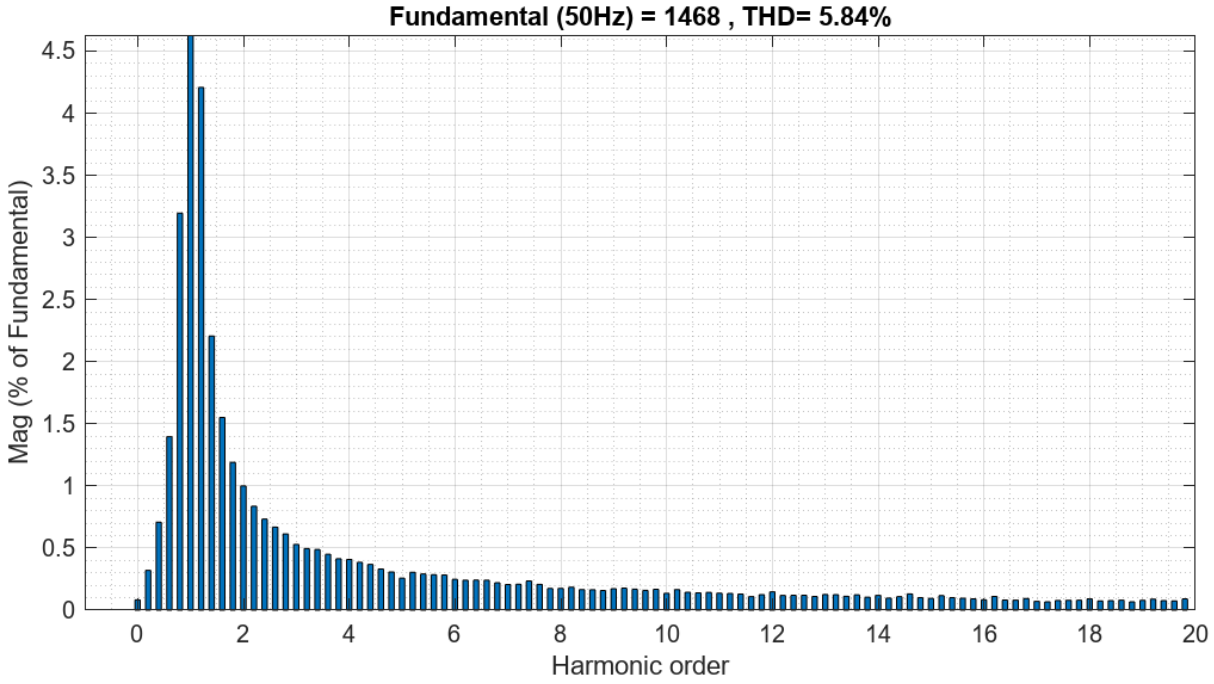


Figure 38. FFT analysis graph of line current with SVPWM.

In the graphs obtained, we observe that the amplitude of lower harmonics is lower for SVPWM. SVPWM has the ability to shape the voltage waveform and distribute harmonics in a more controlled manner. By manipulating the combination of voltage vectors, SVPWM can reduce harmonics and minimize THD. This makes SVPWM a preferred choice in applications where low THD is important, such as motor drives and power quality-sensitive systems.
On the other hand, SPWM, although it generates a pure sine wave voltage, can introduce more harmonics due to its fixed switching pattern. The harmonic content in Sine-PWM depends on the carrier frequency and the modulation index, which affects the THD value.

4)

- In Sine-PWM, the modulation waveform is generated by comparing a high-frequency carrier signal with a sinusoidal reference waveform. The carrier signal switches between two voltage levels (typically positive and negative DC voltages) depending on the comparison result.
- SVPWM synthesizes a three-phase voltage waveform by generating two orthogonal voltage vectors and combining them. These voltage vectors can be in the form of positive or negative half-cycles of the DC bus voltage.
- SVPWM generally has lower THD compared to SPWM and is better suited for applications that require low harmonic distortion.
- SVPWM generates a more optimized voltage waveform that maximizes the utilization of DC bus voltage. It offers higher voltage utilization compared to SPWM and can provide better torque and power output in high-performance applications.
- SPWM operates with a fixed peak voltage, typically at the maximum value of the DC bus voltage. This means that the available voltage range is not fully utilized, resulting in lower system efficiency.
- SVPWM: SVPWM has the advantage of utilizing a larger portion of the DC bus voltage range. It allows the amplitude of the synthesized voltage waveform to vary dynamically within the available voltage range, resulting in improved overall system efficiency.

Considering the requirement for a high-performance drive, SVPWM is generally preferred over SPWM. SVPWM offers better voltage utilization, improved system efficiency, and enhanced control flexibility, which are crucial factors in high-performance applications. It provides the opportunity for advanced control techniques and delivers higher torque and power output, making it an excellent choice for demanding drive systems.

Part D: Component Selection

1-) The maximum current passing through the switch is stated as 1700A. However, the stator of the motor draws around 2100A. Then;

$$I_{rms} = \frac{2100}{\sqrt{2}} \simeq 1485A$$

A regular single IGBT can not handle that current level. Then parallelization will be performed. The maximum voltage level on the switches during off state is;

$$V = 1.35 * 400 = 540V$$

There are few IGBT that can handle these voltage and current ratings. Among them, IXXX300N60B3 is chosen. Parameters of the IGBT are shown as below table 1. Compared to the other options, it has less switching energy loss also it is in the stocks of suppliers. 3 parallel IGBT for each switch will be employed.

Table 1. Properties of selected IGBT

IGBT	V_{CE} (V)	I_{CE} (A)	$V_{CE(On)}$ (V)	E_{On} (mJ)	E_{Off} (mJ)
IXXX300N60B3	600	550	1.6	3.45	2.86

2-) There are two main losses on switching components, conduction and switching losses. While the inverter is working, 3 of the switches are open in different combinations. Two of the switches share the current equally while one of them handles with full current load.

$$P_{Cond} = 1.6 * 1485 + 2 * 1.6 * \frac{1485}{2} = 4752W$$

There are 6 different switch branches and each of them consist of 3 IGBTs.

$$P_{Sw} = 3 * 6 * (3.45 + 2.86) * 10^{-3} * 2.7kHz = 306.6W$$

Total loss on switches;

$$P_{loss} = P_{Cond} + P_{Sw} = 4752 + 306.6 = 5058.6W$$

In order to reduce the losses, among the components suitable for the rated limits, the one with the lower Vce(sat) value to reduce the conduction loss and the one with the lower Eon and Eoff value to reduce the switching losses are preferred. Switches will become hot due to losses. Again, among the alternatives, the one with low thermal resistance can be preferred

so that the switches do not overheat with losses. In addition, heatsinks or cold plates can be used to dissipate the heat of the switches.

3-) As stated before, the switches used in the inverter are used in 3-parallel structure due to the high current level. Therefore, a gate driver capable of driving this parallel structure is needed. In order to meet this priority requirement, it was decided to use TI's TIDA-00917 half-bridge gate driver module. The overview and feature sheet of the product is given below.

Overview

Paralleling IGBTs become necessary for power conversion equipment with higher output power ratings, where a single IGBT cannot provide the required load current. This TI Design implements a reinforced isolated IGBT gate control module to drive parallel IGBTs in half-bridge configuration. Paralleling IGBTs introduces challenges at both the gate driver (insufficient drive strength) as well as at system level in maintaining equal current distribution in both the IGBTs while ensuring faster turnon and turnoff. This reference design uses reinforced isolated IGBT gate driver with integrated features like desaturation detection and soft turnoff to protect the IGBT during fault conditions. An increased gate drive current (15 A) is obtained through external BJT current booster stage without sacrificing the soft turnoff feature. Further, this design demonstrates the mechanism of avoiding gate current loops while operating IGBTs in parallel.

Resources

TIDA-00917	Design Folder
ISO5852S	Product Folder

TI E2E™ Community — ASK Our E2E Experts

Features

- Suited for Low-Voltage Drives up to 480-V_{AC}
- Designed to Drive Parallel IGBT Modules of a 1200-V Rating With Total Gate Charges up to 10 µC Translating to Collector Currents of 500 A
- Sourceand Sink Current Ratings of up to 15 A_{pk} With External BJT Buffer Stage
- Bipolar Gate Drive Voltages
- Split Output for Independent Turnon and Turnoff Control
- IGBT Short-Circuit Protection Using Built-in DESAT and Adjustable Soft Turnoff Time
- Built-in Common-Mode Choke and Emitter Resistance for Limiting Emitter Loop Current
- Generates Fault Output During IGBT Short-Circuit Condition and Gate Driver Undervoltage Scenario
- 8000-V_{pk} V_{IOTM} and 2121-V_{pk} V_{IORM} Reinforced Isolation
- Very High CMTI of 100 kV/µs

Applications

- Variable Speed Drives
- UPS
- Traction Inverter
- Wind and Solar Inverter