MULTIPLE OUTPUT PUSH-PULL CONVERTER WITH POST REGULATED BUCK CONVERTERS

Vivek Ram P
Dept. of E&E
Manipal Institute of Technology
Manipal, India
vivekzak@gmail.com

Namitha Bhat K
Dept. of E&E
Manipal Institute of Technology
Manipal, India
bhat.namitha@gmail.com

Mala R. C.
Dept. of E&E
Manipal Institute of Technology
Manipal, India
mala.rc@manipal.edu

***Abstract*—Switched Mode Power Supplies (SMPS) play a vital role in the field of Power electronic systems. They can be found to be in use in a variety of power processing applications, ranging from lower power applications such as on-chip power management to high power applications such as power systems. In this paper, a multiple output push-pull DC-DC converter is designed and simulated. The power module can supply multiple voltage levels from an input battery. Among the multiple outputs, the Master output or the output with the maximum voltage will be fed back directly using closed loop compensation circuitry. The feedback line will be isolated to maintain a complete galvanic isolation between primary and secondary sides of the circuit. The slave outputs or the lesser voltage outputs will be post regulated using buck converters. The design of the circuit elements for the post regulated buck converters will be done with help of the tool LTpowerCAD. The simulations were done in LTSpice environment. The simulation results show that a stable output is obtained across all the three output ports.**

Keywords— LTSpice, LTpowerCAD, MATLAB, SMPS

I. INTRODUCTION

High speed digital logic circuits which are used nowadays in subsystems of many commercial products demand power supply of different voltage and current levels. The power may have to be driven from a single battery source. Efficiency of such systems must be good enough for the battery to have long life and durability. Unlike LDO's and linear regulators, switched mode converters can do this job more efficiently. The switched mode converter should be of multiple output type to feed all the different output ports. In multiple output converters, only the main or master output can be regulated with good accuracy using direct feedback loop [1]. If tight regulation is expected for the slave outputs as well, then some sort of post regulation technique needs to be used. A previous work has discussed multiple output forward converter which uses linear regulators as post regulation method [6]. This will limit the circuit operation to a few watts as linear regulators are highly inefficient at higher wattages. This paper discusses about the design of a multiple output push-pull DC-DC converter which uses non-isolated closed loop converters as post regulation method which facilitates operation of the circuit at higher wattages efficiently. Usage of push-pull converter facilitates the use of smaller transformer compared to the case when a forward converter is used. Current mode control ensures balanced magnetization and de-magnetization of the transformer core, which will ensure the fruitful operation of the transformer. It also ensures a simple, robust and wide-bandwidth output [2]. First, a theoretical insight is given with regard to the design. Next, the high level architecture and the corresponding low level design choices have been discussed. Last section discusses the important results observed out of the circuit.

II. THEORETICAL DISCUSSION

A. Push-Pull Converter Topology

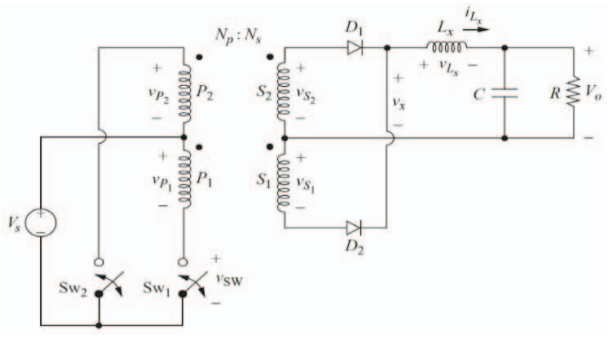

Fig 1. Push-Pull Converter Circuitry

Figure 1 shows the circuit diagram of a DC-DC Push-Pull converter [3]. The primary and secondary windings of the transformer used produces pulses of opposite polarities due to the switching of S_{W1} and S_{W2}. The diodes D1 and D2 on the secondary rectifies the pulsed waveform and yields a waveform V_x at the input of the low-pass L_xC filter. The switching sequence and waveforms for V_{Lx} and i_{Lx} are given in figure 2.

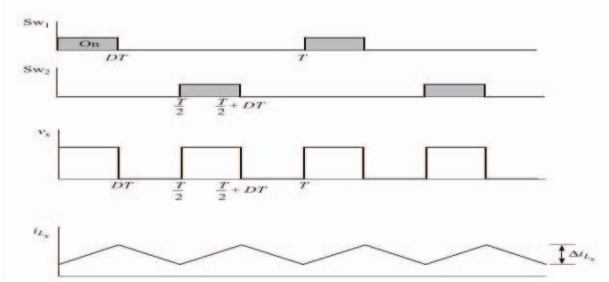

Fig 2. Switching sequence, Vx and i_{Lx} vs time

where, T - Time period D - Duty ratio, Δi_L – Ripple current in inductor

The operation revolves around three cases of switching viz.

1. When S_{W1} is ON and S_{W2} is OFF
2. When S_{W1} is OFF and S_{W2} is ON
3. When both S_{W1} and S_{W2} are OFF

Let us take each case one by one,

When Sw1 is ON and Sw2 is OFF: This will establish positive voltage at the dotted terminal of S1 and S2. This would forward bias the diode D1. On the other hand, the undotted terminal is negative which makes diode D2 to be reverse biased. Diode D1 thus would complete the circuit and Lx starts to get charged. At the same time energy is being transferred on to the capacitor. This will ensure voltage across the output. The path of current would be in the direction S2-D1-Lx-C-S2.

When Sw1 is OFF and Sw2 is ON: This will establish positive voltage at the dotted terminal of S1 and S2. This would forward bias the diode D2. On the other hand, the undotted terminal is negative which makes diode D1 to be reverse biased. Diode D2 thus would complete the circuit and Lx starts to get charged. At the same time energy is being transferred on to the capacitor. This will ensure voltage across the output. The path of current would be in the direction S1-D2-Lx-C-S1.

When both Sw1 and Sw2 are OFF: This will establish zero voltage across S1 and S2. This would force the inductor to discharge current through the capacitor and then split itself and flow partially through D1 and D2. By this way, the inductor current remains continuous as well. The path of current would be in the direction Lx-C-D1&D2-Lx.

Using the principle of inductor volt-second balance, capacitor charge balance and small-ripple approximation, we can derive the output voltage equation, Inductor equation and Capacitor equation. The results are shown below,

$$V_o = 2V_S\left(\frac{N_S}{N_P}\right).D \qquad -(1)$$

$$L_x = \left(\frac{V_S.\left(\frac{N_S}{N_P}\right) - V_o}{\Delta i_{Lx}}\right).DT \qquad -(2)$$

$$C \geq \frac{[1-2D]}{32 \times L \times f_s^2 \times \frac{\Delta V_o}{V_o}} \qquad -(3)$$

Where, Vo - Output voltage
V_S - Input voltage
N_S/N_P - Primary to secondary turns ratio
ΔVo - Ripple in the output voltage
f_S - switching frequency

B. Current Control Method

A current controlled system, in general consists of a sensor gain block, an error amplifier network, an analog comparator block, an S-R latch and a gate driver network. Figure 3 shows the general block diagram representation of the current control system [2]. The sensor gain block takes a part of the output and compares it with a steady reference voltage. The error amplifier network further amplifies the error between these signals to generate a corrective action. So, if there is an increase in the output voltage, the magnitude of the error signal reduces to instruct the converter to diminish its output. On the other hand, if the output voltage decreases, the error voltage will increase to let the converter know that there is a demand for more output voltage. Therefore, the control action comprises of opposing the variation observed on the regulated output. A slope compensation voltage is added with output voltage of the error amplifier. This would provide the necessary corrective action on the instability problems faced by the inductor current during duty ratios of more than 50%.

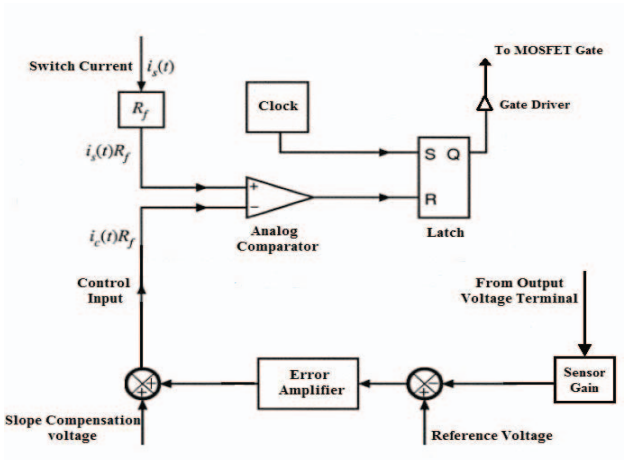

Fig 3. Current control system

The analog comparator compares the control input with the sensed voltage developed across the sense resistor R_f due to the switch current i_S. If the sensed voltage is lesser than the control input, then R terminal of S-R latch becomes low. The clock pulses generated by the clock generator will get replicated on the Q terminal. The gate driver amplifies the clock pulses and feeds the gate terminal of the MOSFET. On the other hand, if the sensed voltage exceeds the control input, then R terminal of S-R latch becomes high forcing the Q terminal to be 0. Hence, no pulses will be fed to the gate of the MOSFET. This would ensure that, if current in the MOSFET exceeds a preset limit, pulses will be skipped which will draw back the current to safe limits. In commercially available controller IC's, excluding the error amplifier network, sensor gain network, current sense resistor and slope compensation resistor, all the other sub networks will be inbuilt. Hence the designer has to design only the excluded networks. Out of these networks, the error amplifier network is of prime importance. The reason is that, output and error signals should never be in phase, because if it does then we would build an oscillator, carrying a sinusoidal signal at a frequency fixed by the 0dB crossover point. Hence, the error amplifier circuit should be designed in such a way that when it gets included in the loop, the total loop gain crosses the 0dB axis at a point where there is sufficient phase difference between the error and the output signal. This would ensure that there is enough phase margin at the 0dB crossover point. Absolute minimum value of phase margin is 45 degrees, but good solid designs aim for a phase margin of around 70 degrees providing sound stability and a fast non-ringing transient response. Choosing the correct error amplifier type

depends on the converter type we choose and the net phase brought about by all the blocks in the closed loop except for the error amplifier block. The most prominent error amplifier types used with power electronic converters are Type 2 and Type 3 error amplifiers. To ensure complete galvanic isolation in the system, isolation should be brought in the feedback stage as well. For this purpose, we should use a precision voltage reference IC with an Optocoupler. With the help of the reference IC, we can implement a type 2 or type 3 error amplifier and with the help of optocoupler, we can bring isolation in the feedback stage. TL431 IC and 4N25 is used for the same respectively. Type 3 error amplifier circuit using TL431 [4] and 4N25 is as shown in figure 4.

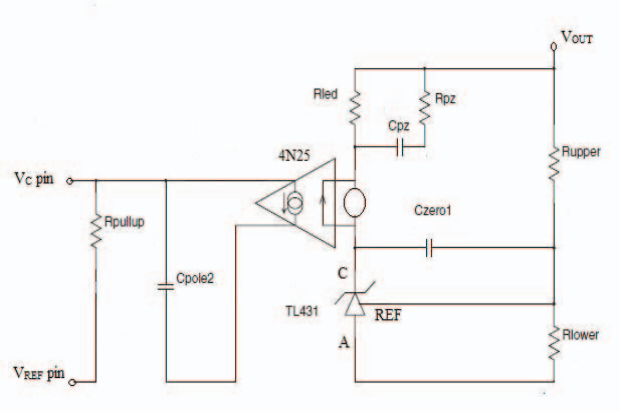

Fig 4. Type 3 Error Amplifier Circuit using TL431 & 4N25

C. *Auxiliary Supply circuitry*

As soon as the power supply is connected to the input battery, the bulk capacitor, Cbulk instantly charges to the peak input voltage. Since the controller IC being used in the circuit is being charge from a low voltage (below 20 V), it cannot be powered directly from the bulk capacitor. Hence an auxiliary supply circuitry is necessary for start-up of the IC. Figure 5 shows one of the prominent circuits being used for this purpose [4].

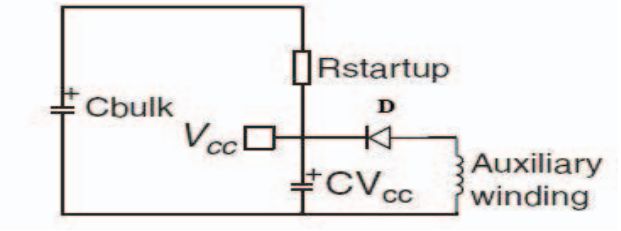

Fig 5. Classical startup circuitry

Initial energy supplied by the Vcc capacitor, is charged through a start-up resistor. At power-on, the Vcc capacitor will be completely discharged. Hence, the power consumed by the IC is zero and does not provide any driving pulses to the MOSFET. As Vcc increases over time, the consumed current remains below a definite limit until the capacitor voltage reach a certain level. This level, often called Vccon or UVLO high (under voltage lockout) depending on the IC manufacturer, fixes the point at which the controller starts to deliver pulses to the power MOSFET. Once the IC starts to deliver pulses, the consumption suddenly increases, and the capacitor will discharge completely. As soon as the discharge happens, the external voltage source or the so-called auxiliary winding takes over and supplies the controller IC. The energy stored in the capacitor must be calculated to feed the controller long enough that the auxiliary circuit takes over in time. If the capacitor fails to maintain Vcc high enough before the auxiliary supply takes over, the voltage across the capacitor drops to a level called UVLO low or VCC (min). This safety level of stored energy ensures that the MOSFET receives pulses of sufficient amplitude and the controller internal logic operates under reliable conditions. Unfortunately, if the auxiliary supply couldn't take over in time and input supply to the controller IC goes to UVLO low level, the controller goes back to its original low current consumption mode. But thanks to the start-up resistor, it makes another restart attempt. Still if no auxiliary voltage comes (may be because of a broken diode or an output short), the controller IC will enter hiccup mode or auto restart mode where it pulses for a few milliseconds waits again until the capacitor refuels and if it fails again, the controller IC will shut off completely.

III. CIRCUIT DESIGN

The high-level architecture of the proposed converter circuit that provides multiple output voltages is shown in figure 6. The input battery supply varies from 100-180 V with a nominal voltage of 150 V. The converter provides multiple output voltages of 12, 24 and 48 V of which the master output is 48 V port. Feedback loop is connected across the 48 V port.

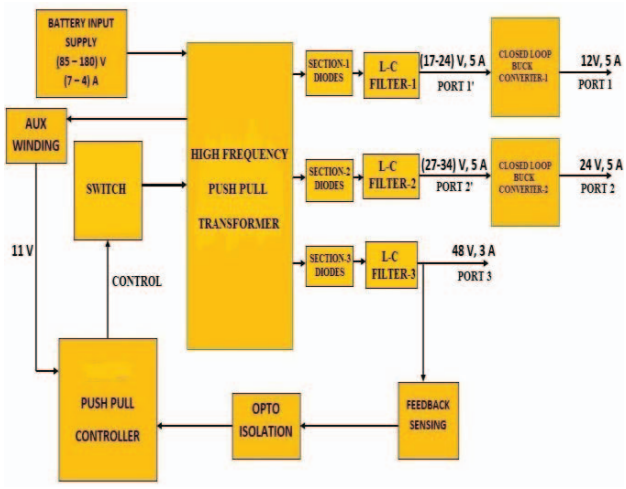

Fig 6. High Level Architecture

The input supply from the battery is given to the H.F push pull transformer and to the push pull controller IC. The push-pull controller IC used is LTC3721-1. Supply from the battery cannot be directly given to the controller IC because the IC input voltage cannot exceed 10 V. For this purpose, an auxiliary winding needs to be used. The auxiliary winding is just like another secondary winding to the transformer. This would step down the battery input voltage and feed the necessary voltage to the IC. The output ports 1' and 2' supply the voltage to the post regulated buck converters. The buck

controller IC used is LT3724. The output specifications are given below in table 1.

Table 1. Output Specifications

Sl.no	V_O'	V_O	I_O	$\Delta V_O'$	ΔV_O
1	20 V	12 V	5A	400mV	200mV
2	30 V	24 V	5A	400mV	200mV
3	-	48 V	3A	-	400mV
4	-	10 V	1A	-	-

The V_O' output is the converter output at the input of the post regulated buck regulators. For the master output 48 V and the auxiliary winding, since there is no need for post regulators, V_O' is not required. Also, for the Auxiliary winding voltage ripple is insignificant, hence ΔV_O value is not required.

A. High Frequency Push-Pull Transformer

The H.F switching transformer is the central unit of the SMPS. It isolates the source and load magnetically transfers energy between them. The switching transformer is designed with required turn's ratio to meet the voltage and current requirements. The size of a power transformer is determined by the area product [5]. A core that has an area product greater than the calculated Ap should be chosen. For a push-pull converter, area product is calculated as:

$$\text{Area product, } A_p = \frac{1.414 . P_{OUT}\left(1+\frac{1}{eff}\right)}{4.Kw.J.Bm.fs}$$

The transformer is designed for a maximum allowable flux density of Bm= 0.1T,
Current density J = 3 A/mm2,
Window utilization factor Kw= 0.4,
Efficiency, eff = 80 %
Now, no of turns in the primary is calculated as follow,

Number of turns in the Primary,

$$N_1 = 2 \times \frac{[V_{inmax} - I_{sw}(R_{on}+R_{sense})]}{4.Bm.Ac.fs} = 32 \text{ turns}$$

Now, turns ration is found using the equation,

$$n = \frac{[V_0 + V_F + (10\%\ V_0)]}{2.D_{max}.(V_{inmin} - I_{sw}(R_{on}+R_{sense}))}$$

Table 2 given below shows the number of turns calculated for the output ports.

Table 2. Turns ratio calculation for output ports

	Port 1'	Port 2'	Port 3	Aux
Output voltage	20	30	48	10
10% Output voltage	2	3	4.8	1
Diode drop	1.5	1.5	1.5	1
Turns ratio	0.2927	0.4297	0.6764	0.125

Secondary-1 number of turns, N_{21} = Turns ratio1*N_1= 10 turns
Secondary-2 number of turns, N_{22} = Turns ratio2*N_1= 14 turns
Secondary-3 number of turns, N_{23} = Turns ratio3*N_1= 22 turns
Auxiliary number of turns, Naux = Turns ratio-aux*N_1
= 2 turns

B. Diode and switch selection

The diode and switches are selected such that it meets the respective voltage stress and current stress. Table 3 shows the final selection of these components.

Table 3. Diode and Switch Selection

	Diodes Chosen	Switch chosen
Input	-	SPA11N60C3
Port 1'	MUR2020R	-
Port 2'	MUR2020R	-
Port 3'	VS-15ETH03-N3	-
Aux Port	1N4148	-

C. L-C Filter selection

Using equation (2) and (3) discussed in section II we can come up with values for the L-C filters for all three output ports. The chosen values for L and C for the various output ports are given below in table 4. The auxiliary port just has a capacitor at the output. The design of it will be discussed in the next section.

Table 4. L-C values for the output ports

	Port 1'	Port 2'	Port 3
Chosen Δi_L	1.5	1.5	1
Turns ratio, n	0.3125	0.4375	0.6875
L	55uH	75uH	170uH
C	100uF	100uF	150uF
ESR, r_C	0.2 Ω	0.2 Ω	0.35 Ω

D. Master Output Regulation

This section will talk about the Master Feedback section which includes the three blocks viz. Feedback sensing, Opto-Isolation and Push-Pull Controller. These three blocks in harmony will provide precise regulation to the 48 V port.

Table 5. Circuit elements for Type 3 Error amplifier

Circuit Elements	Values
R_{pullup}	20kΩ
R_{LED}	3kΩ
R_{PZ}	2.947kΩ
R_{upper}	10kΩ
R_{lower}	0.544kΩ
C_{pz}	3.8nF
C_{zero1}	2.26nF
C_{pole2}	560pF

The feedback sensing is implemented using a resistive divider network and the necessary error amplifier operations are carried out using the Texas Instrument's precision reference IC TL431. Opto-isolation is realized using Vishay's optocoupler

IC 4N25. The necessary current-control action is provided by the Linear Technology's Push pull controller IC LTC3721-1. A prominent small-signal model was developed for realizing transfer functions of DC-DC converters [7] but was rather complex and is not apt for designing controllers. By curbing the shortcomings of the previous model, a dynamic transfer function model with quantitative controller design of a push-pull converter with current-mode control was developed [8]. The bode plot for this transfer function was found with the help of MATLAB. Based on this bode plot, the dB gain and phase lag values were found at the selected cross over frequency of 10kHz. Based on these values, the circuit elements for the type 3 error amplifier as shown in figure 4 were found. Table 5 shows the selected values of these circuit elements. Figure 7 shows the push-pull controller IC used and the various circuit elements around it.

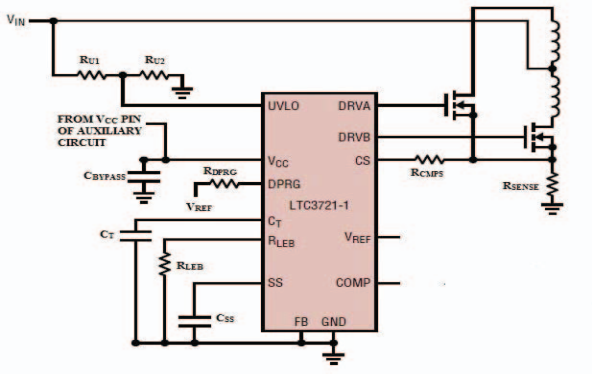

Fig 7. Push-Pull controller IC LTC3721-1

The selection of the MOSFET switches M1 and M2 were discussed in section B under table 2. The other circuit elements around the IC were designed with the help of information obtained directly from the datasheet for a switching frequency of 100kHz.

E. Post regulated Buck converters

Figure 8 shows the buck controller IC used and the various circuit elements around it.

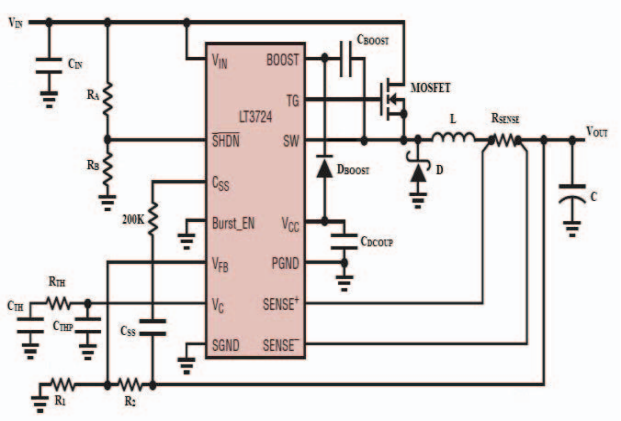

Fig 8. Buck Controller IC LTC3721-1

Some of the most important circuit elements for the IC were found with the help of the tool LTpowerCAD II. Table 6 and Table 7 show the final choice of the design elements around the IC for the closed loop buck converter 1 and 2. The other circuit elements around the IC were found with the help of information obtained directly from the datasheet for a switching frequency of 200 kHz.

Table 6. Circuit elements for closed loop buck converter-1

Circuit Elements	Values or Part No:
MOSFET	Si7852DP
L	47uH
C	280uF,10uF,10uF
D	30BQ060
R_{SENSE}	25mΩ
R_1	4.99kΩ
R_2	43.65kΩ
C_{TH}	1500pF
R_{TH}	4kΩ
C_{THP}	120pF

Table 7. Circuit elements for closed loop buck converter-2

Circuit Elements	Values or Part No:
MOSFET	Si7852DP
L	47uH
C	280uF,10uF,10uF
D	30BQ060
R_{SENSE}	25mΩ
R_1	4.99kΩ
R_2	93.1kΩ
C_{TH}	1500pF
R_{TH}	4kΩ
C_{THP}	120pF

IV. RESULTS

The circuit schematic was created in LTSpice environment. Figure 9 shows the circuit schematic created.

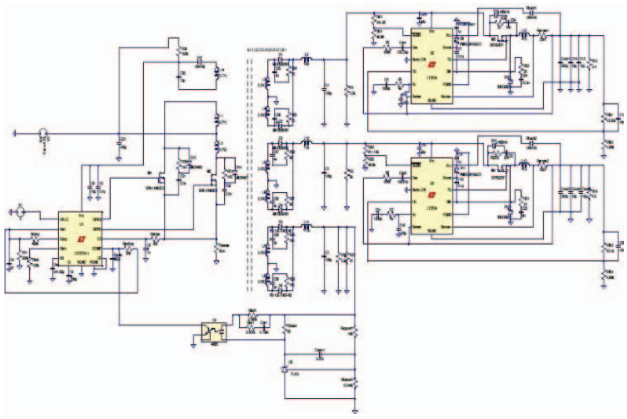

Fig 9. Circuit Schematic

Stable outputs were obtained across all the output ports for an input voltage of 120 V is as shown in figure 10.

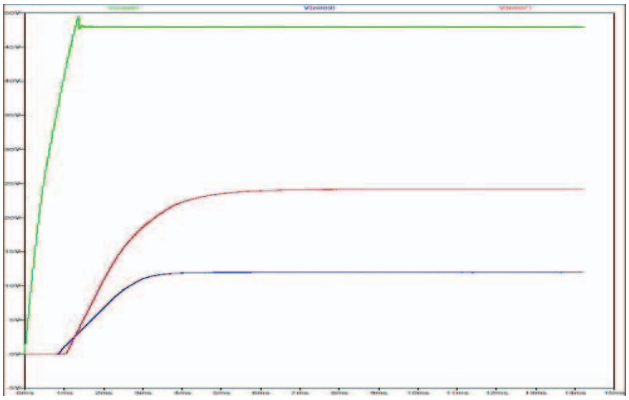

Fig 10. Output voltages of 48 V,24 V & 12 V respectively

To ensure the stability of the outputs, a stability test is carried out where the output current will be intentionally dropped to a value below the full load current. The voltage will initially shoot up a little, but will recover in a few milliseconds. This will ensure that the circuit is stable under varying load conditions. Figure 11 shows the load variations and the corresponding voltage stability for output port 1.

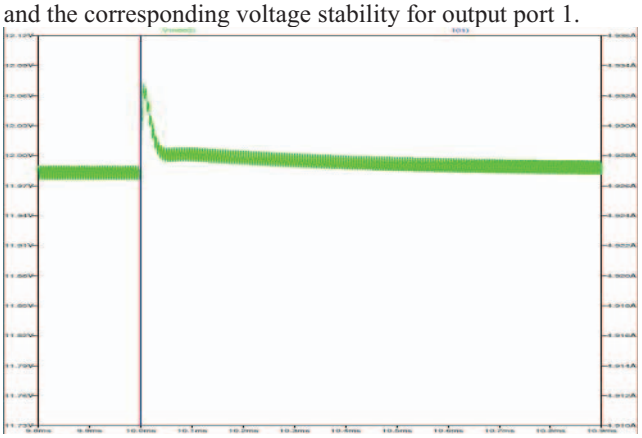

Fig 11. Voltage stability during load variation

Figure 12 shows the load variations and the corresponding voltage stability for output port 2.

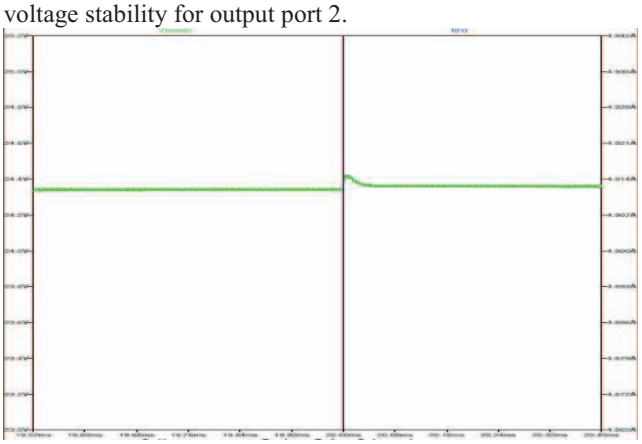

Fig 12. Voltage stability during load variation

Figure 13 shows the load variations and the corresponding voltage stability for output port 3.

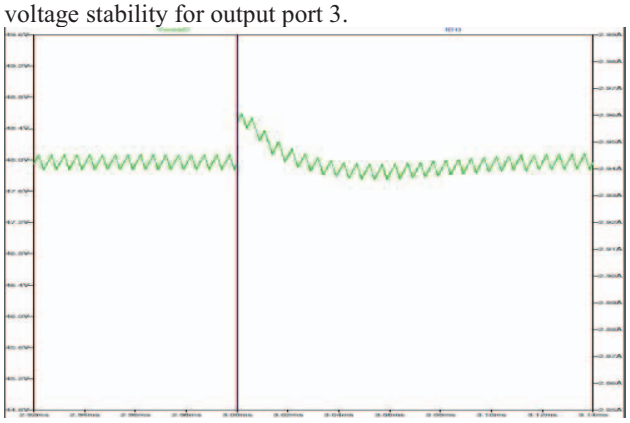

Fig 13. Voltage stability during load variation

The blue line indicates the output current falling from rated value to a lesser value. The green waveform shows the output voltage, which shoots up a little during the load change, but settles down to steady state in few milliseconds.

V. CONCLUSION

A multiple output push-pull DC-DC converter was designed and simulated. The advantages of this topology lie in its simplicity and robustness. The current mode control ensures stability in the operation of the converter. The isolation in the master feedback line ensures a complete galvanic isolation between the source and the load. The slave outputs were also regulated using buck converters. The simulation results show that all the output voltage ports are highly stable in operation and thus making the whole circuitry reliable.

REFERENCES

[1] Abraham I. Pressman, “Switching Power Supply Design”, McGraw Hill

[2] Robert W. Erickson, “Fundamentals of Power Electronics”, Springer International Edition

[3] Daniel W. Hart,” Power Electronics”, McGraw Hill

[4] Christophe P. Basso, “Switch-Mode Power Supplies”, McGraw Hill

[5] L. Umanand, “Power Electronics Essentials & Applications”, Wiley

[6] A multiple output DC-DC converter using two switch forward topology, December 2014, Anjana.S, Revathi.H, Karthik.R, Kavitha Issac, M.A.C, Kothamangalam, Kerala, India

[7] R. D. Middlebrook, "Topics in multiple-loop regulators and currentmode programming," in IEEE Power Electron. Specialists Conf Record, pp. 716--732, 1985.

[8] C. M. Liaw, Member, IEEE, S. 1. Chiang, C. Y. Lai, K. H. Pan, G. C. Leu, and G. S. Hsu, “Modeling and Controller Design of a Current-Mode Controlled Converter”, IEEE Transactions on Industrial Electronics, 1994, Volume: 41, Issue: 2