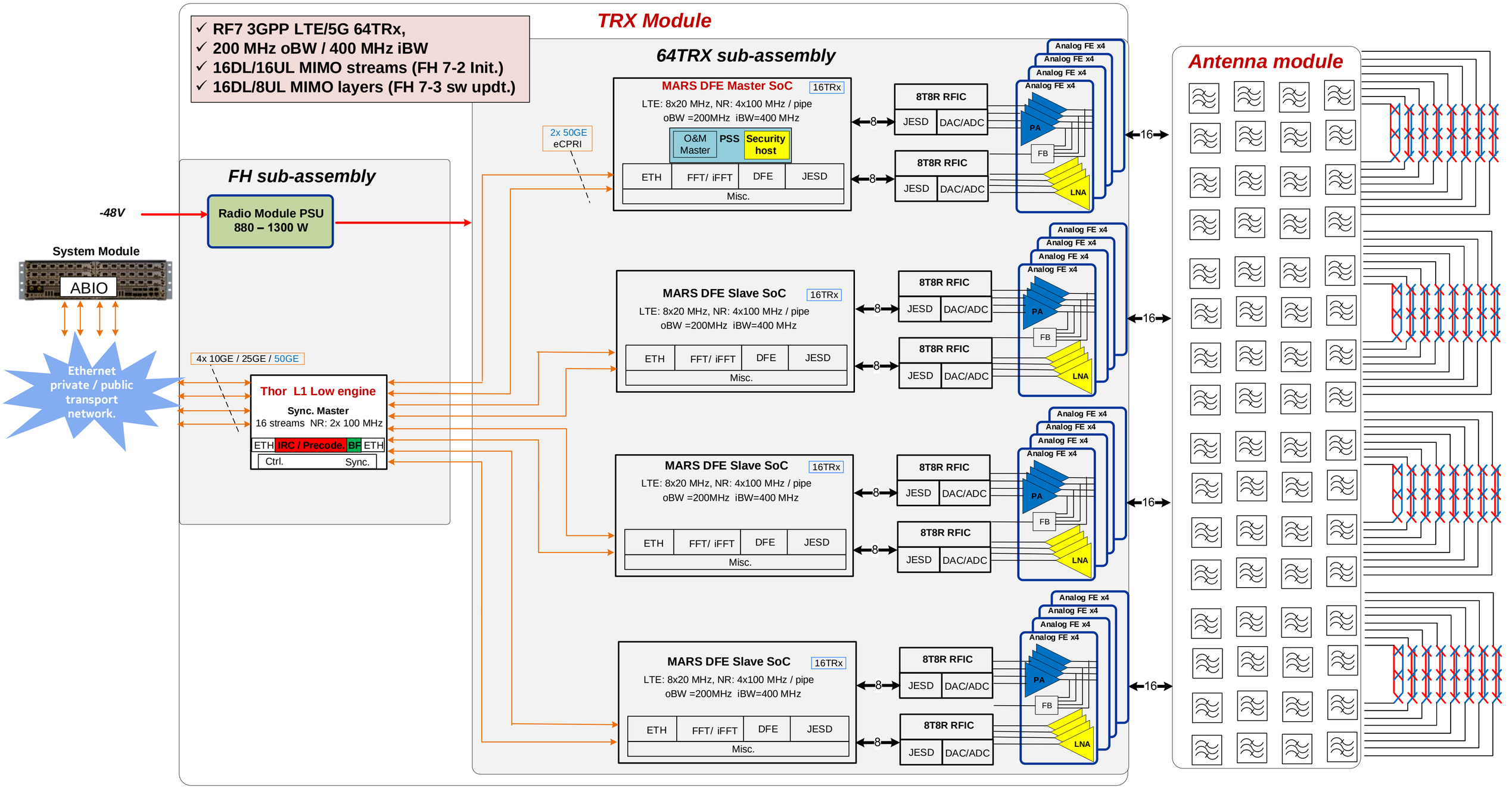
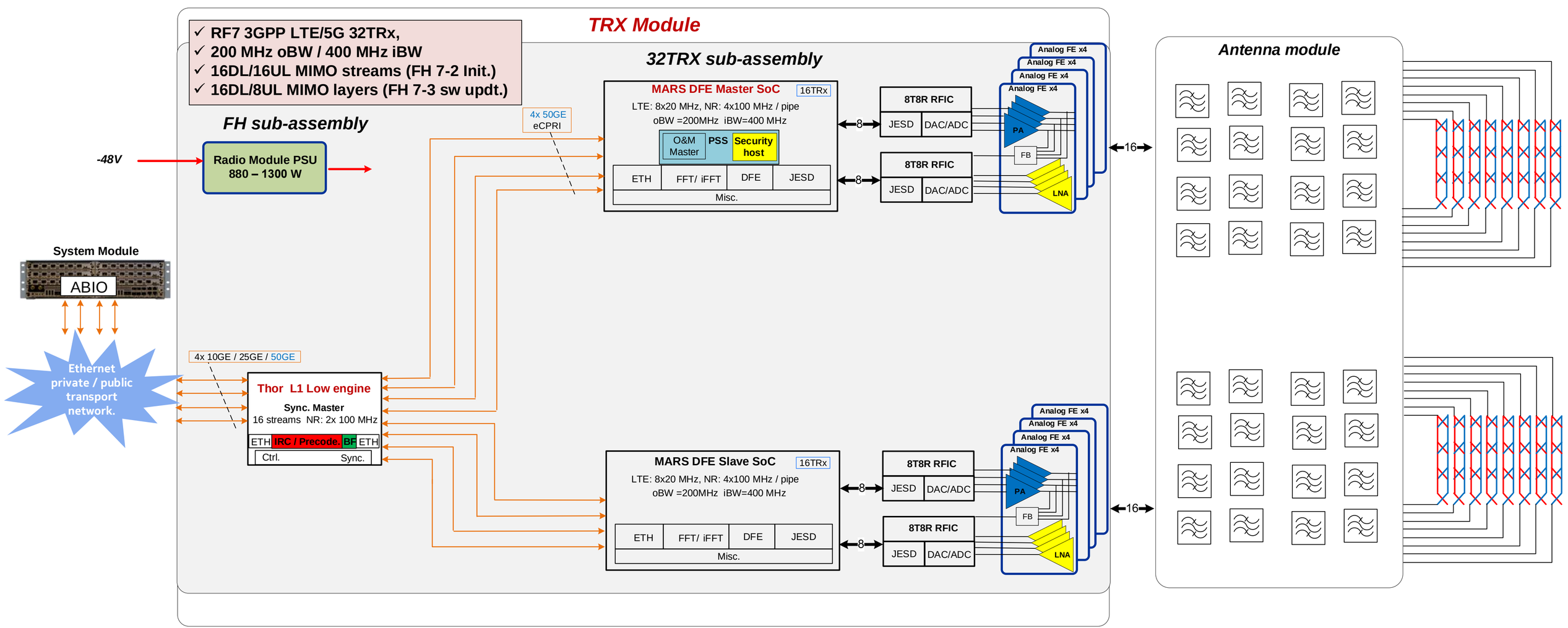

✓ RF7 3GPP LTE/5G 64TRx,
✓ 200 MHz oBW / 400 MHz iBW
✓ 16DL/16UL MIMO streams (FH 7-2 Init.)
✓ 16DL/8UL MIMO layers (FH 7-3 sw updt.)
TRX Module
64TRX sub-assembly
FH sub-assembly
-48V
Radio Module PSU
880 – 1300 W
System Module
ABIO
Ethernet private / public transport network.
4x 10GE / 25GE / 50GE
Thor L1 Low engine
Sync. Master
16 streams NR: 2x 100 MHz
ETH IRC / Precode. BF ETH
Ctrl. Sync.
2x 50GE eCPRI
MARS DFE Master SoC
16TRx
LTE: 8x20 MHz, NR: 4x100 MHz / pipe
oBW =200MHz iBW=400 MHz
O&M Master
PSS
Security host
ETH
FFT/ iFFT
DFE
JESD
Misc.
MARS DFE Slave SoC
8T8R RFIC
JESD
DAC/ADC
8
Analog FE x4
PA
FB
LNA
16
Antenna module


✓ RF7 3GPP LTE/5G 32TRx,
✓ 200 MHz oBW / 400 MHz iBW
✓ 16DL/16UL MIMO streams (FH 7-2 Init.)
✓ 16DL/8UL MIMO layers (FH 7-3 sw updt.)
TRX Module
32TRX sub-assembly
FH sub-assembly
-48V
Radio Module PSU
880 – 1300 W
4x 50GE
eCPRI
MARS DFE Master SoC
16TRx
LTE: 8x20 MHz, NR: 4x100 MHz / pipe
oBW =200MHz iBW=400 MHz
O&M Master
PSS
Security host
ETH
FFT/ iFFT
DFE
JESD
Misc.
8
8T8R RFIC
JESD
DAC/ADC
Analog FE x4
PA
FB
LNA
16
Antenna module
System Module
ABIO
Ethernet private / public transport network.
4x 10GE / 25GE / 50GE
Thor L1 Low engine
Sync. Master
16 streams NR: 2x 100 MHz
ETH
IRC / Precode.
BF
Ctrl.
Sync.
MARS DFE Slave SoC
16TRx
LTE: 8x20 MHz, NR: 4x100 MHz / pipe
oBW =200MHz iBW=400 MHz

RF7 4G/5G 64 mMIMO TRX 200MHz oBW, 400MHz iBW
16DL/8UL MIMO layers (7-3 FH split)
16DL/16UL MIMO streams (7-2 FH split)

FH sub-assembly

Ant. Mon. port

DC power in -48VDC

Radio Module PSU 880 – 1300 W
Surge protection, EMC, Inrush and polarity protection.
Power measurement

Nominal voltage PA supply (voltage level setable at startup)

PA supply with adjustable tapering PA voltage level

Common bus converter +12V

Power Sequencer
Voltage mnitoring
GPIO Control
Watchdog(s)
HW Reset(s)
PWR_EN
V_MON
Resets / GPIOs
POLs /Reg. Group #1
Thor POL supplies
Thor Core supply
...

Unit LED

R&D test connector
PCIe
JTAG

Boot Flash 256MB

DDR5 16GB (16Gbit x16 (12pcs)
DDR5 4GB ECC
4GB
4GB
4GB
ECC

+12V
AISG
RET Ctrl.
EAC 6A/1C
SFP56 10/25/50 GE eCPRI
SFP56 10/25/50 GE eCPRI
SFP56 10/25/50 GE eCPRI
SFP56 10/25/50 GE eCPRI

JTAG | Trace | I2C | QSPI | Mem0 | Mem1 | Mem2 | Mem3

Thor L1 Low Engine
Device_ID-00

UART | GPIO | RST

DSP Cores (L1 Low)
Digital BF DL / UL
BF DL distrip.
Channel Estimation
UL signal combining
Pre-coding

ARM Cores O&M
Local O&M control
PTP -BNC Sync.

4x 25GE or 2x 50GE
8x 50GE
8x 50GE eCPRI

SPI | Sync. IF | 1GE

LMI
Vcc (3.3V)
SGMII
UART
Test clk.
JTAG/ BSCAN

1PPS Sync.
BCN sys. Ref.
1 PPS -ref. Clk.
Sys. Clk.

XO *TCXO*
Init. + PTP freq. tune
LMI test clk. input
Main clock generator (CG1)
PLLs | Frequency synthesizer | Clock Buffer
Device ctrl. & status
Sys. Clk.

XO 100M
Thor ARM cores, System, Mem.,

Misc. Ctrl.
JTAG/BSCAN
UART TX/RX
Unit LED
SEQ. PWR. GOOD
Thor Reset

64TRX sub-assembly

Coaxial cable

32 PAs in columns C3 -C6
32 PAs in columns C1,C2 and C7, C8

RF-lineup supplies
P5V_RX
P1V8_PAM
P5V_PAM
N10V_PAM
P5V_PAM_bias
RF-Lineups 64 PAs

FANs
Factory_cal / Tx_mon
BF_CAL_32_0

POL / Reg. GROUP2
DFE 1 Core supply
DFE 2 Core supply
DFE 1 & 2 POL supplies
...
PWR_EN
V_MON

Power Sequencer
Voltage mnitoring
GPIO Control
HW Reset(s)
Watchdog(s)
Resets / GPIOs

TRX Free-run clocks
XO 125M → *Mars SoCs*
XO 25M → *1GE switch*

DDR4 1GB
TPM v.2.0
Secure Boot FLASH 256MB
eMMC Flash 8GB

Ctrl.
I2C | DDR4 ctrl. | SPI | QSPI | eMMC | I2C
GPIO(s) | QSPI | SGMII | JTAG

Master Mars SoC
Device_ID-0000
LTE: 8x20 MHz, NR:2x100 MHz /pipe
16T16R, oBW=200 MHz, iBW=400 MHz
ARM O&M PSS & DDR & Peripherals
50GE | L1Low | DL | CFR | DPD | RFIF | 16x JESD
FFT / iFFT | UL | TXRXC AIM
SPI | MDIO | SGMII | Ref. Clk
Sync., 1GE, GPIO, Ctrl. Bus, Test

8x Tx *4x Rx* *2x FB* *SPI/ GPIO*
8X JESD | 8X DAC | 2X FADC | 8X ADC
JESD204C
I2C GPIO

RFIC 8TRX
Analog FE x8
PA | FB | FB | LNA | x8

Init
1GE C&M Switch
Fly-over cable

Slave Mars SoC
Device_ID-0001
LTE: 8x20 MHz, NR: 2x100 MHz / pipe
16T16R, oBW=200 MHz, iBW=400 MHz
PSS & DDR & Peripherals
DDR4 1GB
50GE | L1Low | DL | CFR | DPD | RFIF | 16x JESD
FFT / iFFT | UL | TXRXC AIM
Sync., 1GE, GPIO, Ctrl. Bus, Test
JTAG

BCN sys. Ref. + DFE sys. Ref.
PLLs | Synthesizer | Device ctrl. & status | *CG2* | Clock Buffer outputs
Sys. Clk. | Init | *Ctrl.* | *VCXO*

Slave Mars SoC
Device_ID-0010
LTE: 8x20 MHz, NR:2x100 MHz /pipe
16T16R, oBW=200 MHz, iBW=400 MHz
ARM PSS & DDR & Peripherals
DDR4 1GB
50GE | L1Low | DL | CFR | DPD | RFIF | 16x JESD
FFT / iFFT | UL | TXRXC AIM
Sync., 1GE, GPIO, Ctrl. Bus, Test
JTAG

Slave Mars SoC
Device_ID-0011
LTE: 8x20 MHz, NR: 2x100 MHz / pipe
16T16R, oBW=200 MHz, iBW=400 MHz
PSS & DDR & Peripherals
DDR4 1GB
50GE | L1Low | DL | CFR | DPD | RFIF | 16x JESD
FFT / iFFT | UL | TXRXC AIM
Sync., 1GE, GPIO, Ctrl. Bus, Test
JTAG

POL / Reg. GROUP3
DFE 3 Core supply
DFE 4 Core supply
DFE 3 & 4 POL supplies
...
PWR_EN
V_MON
Power Sequencer
Voltage mnitoring
GPIO Control
HW Reset(s)
Watchdog(s)
Resets / GPIOs

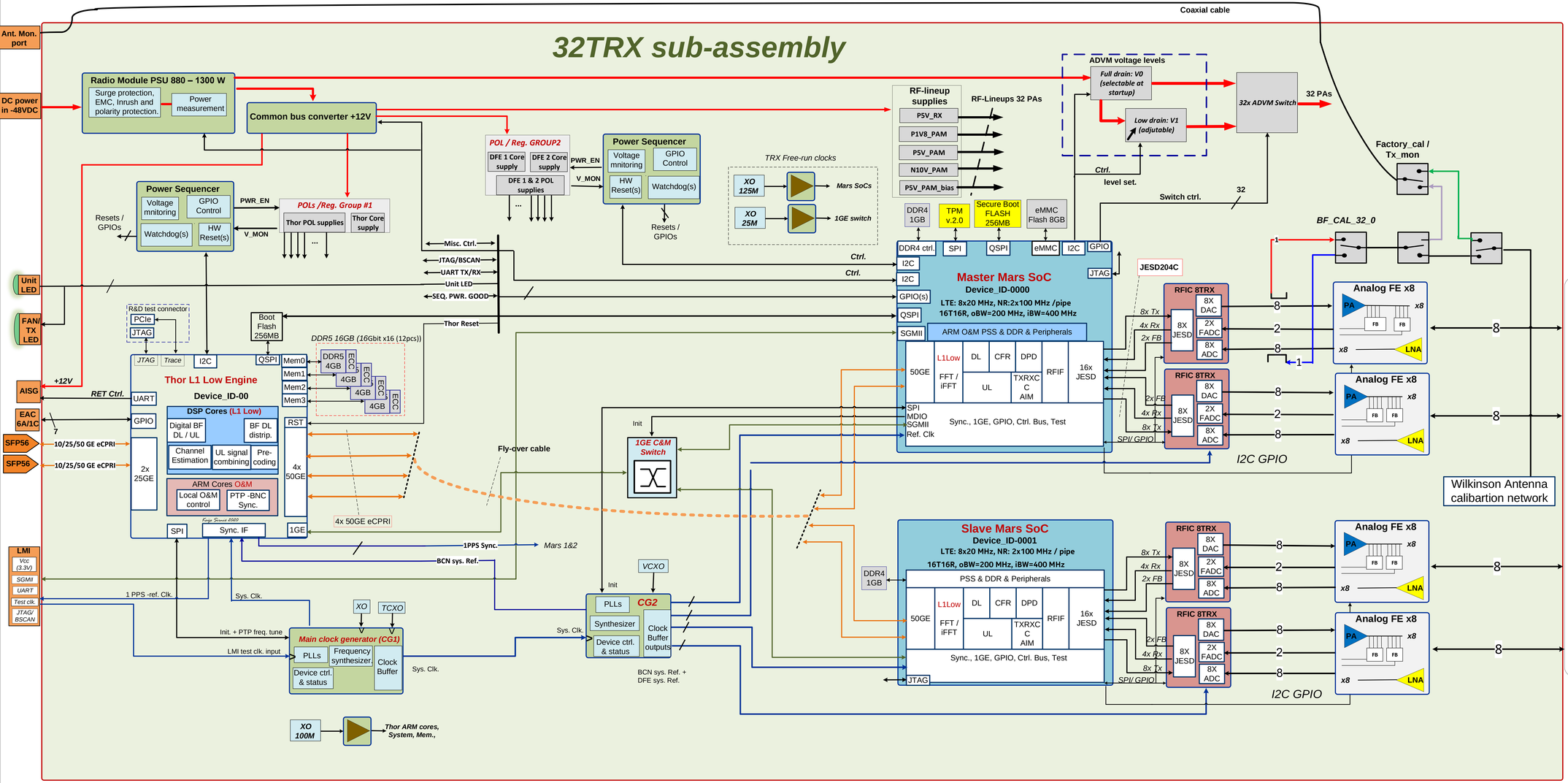
Wilkinson Antenna calibartion network
BF_CAL_32_1

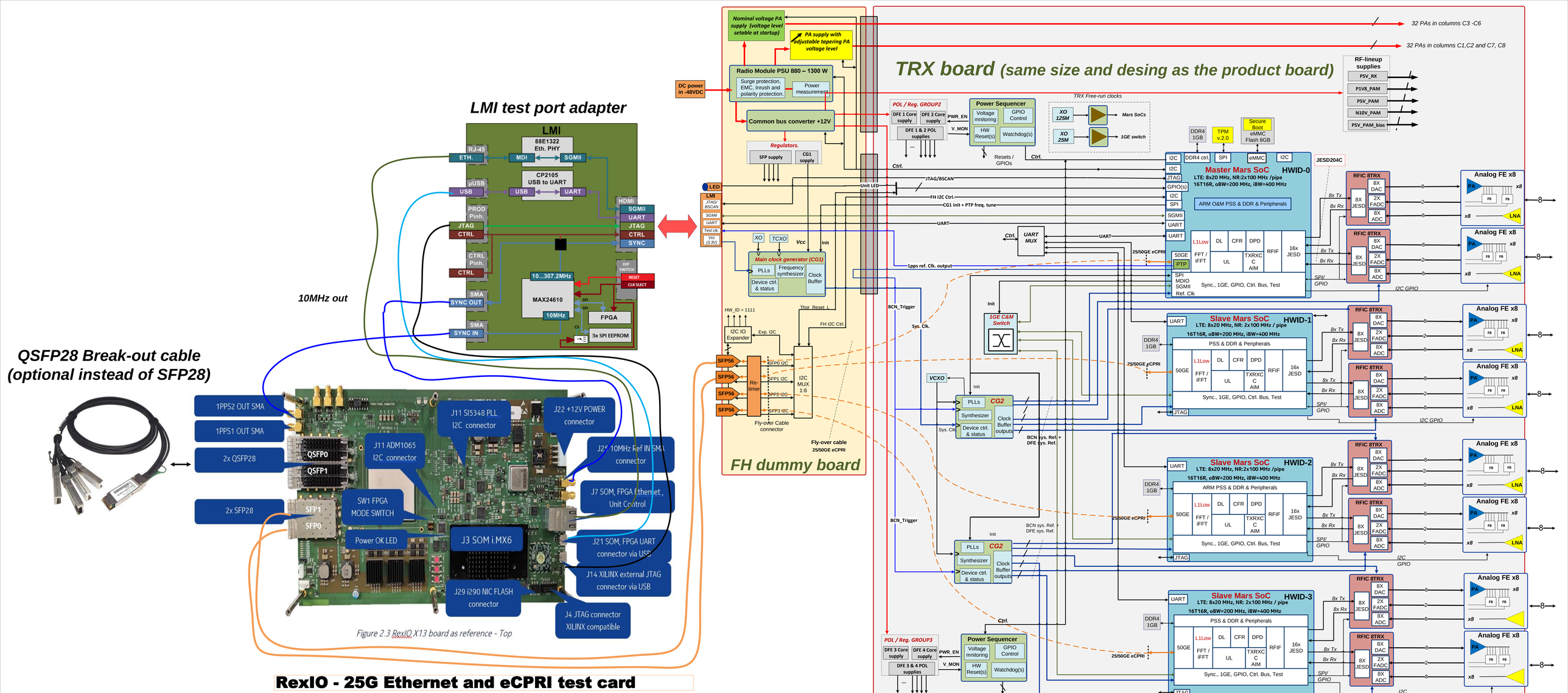
192 AE ; 4 rows x 8 colums x 2 polarizations

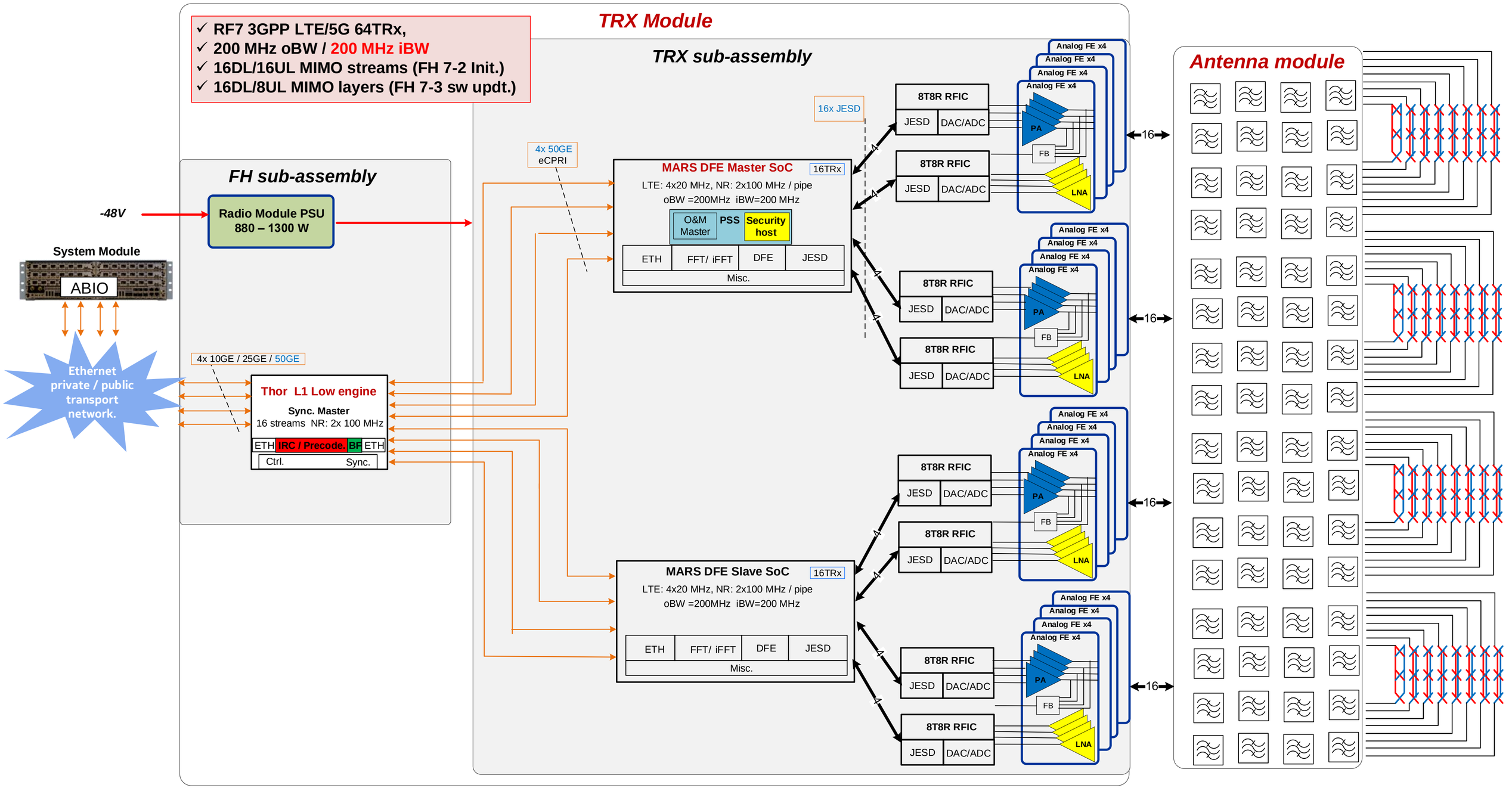
Filtenna

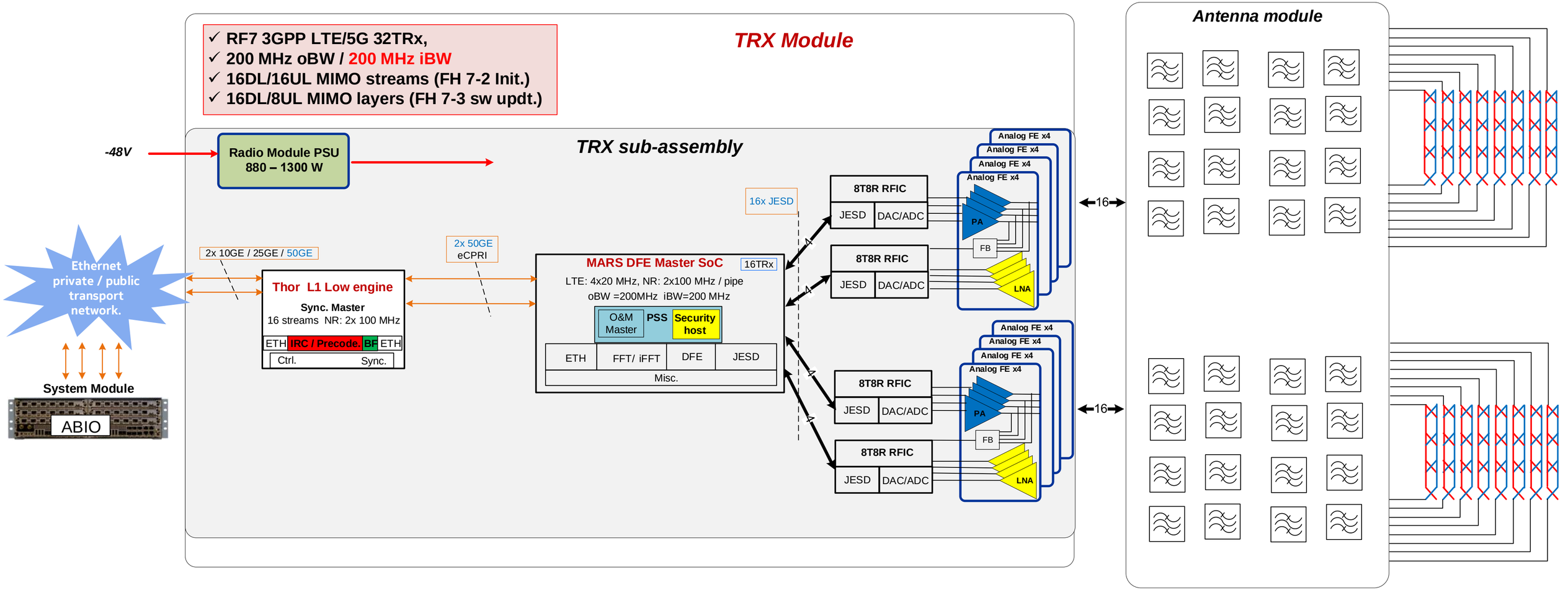
Filter sub-assembly

RF7 4G/5G 32 mMIMO TRX 200MHz oBW, 400MHz iBW
16DL/8UL MIMO layers (7-3 FH split)
16DL/16UL MIMO streams (7-2 FH split)




LMI test port adapter
10MHz out
QSFP28 Break-out cable
(optional instead of SFP28)
LMI
88E1322
Eth. PHY
CP2105
USB to UART
MAX24610
FPGA
3x SPI EEPROM
1PPS2 OUT SMA
1PPS1 OUT SMA
2x QSFP28
2x SFP28
J11 SI5348 PLL
I2C connector
J11 ADM1065
I2C connector
J22 +12V POWER
connector
J25 10MHz Ref IN SMA
connector
J7 SOM, FPGA Ethernet ,
Unit Control
J21 SOM, FPGA UART
connector via USB
J14 XILINX external JTAG
connector via USB
J4 JTAG connector
XILINX compatible
J29 i290 NIC FLASH
connector
SW1 FPGA
MODE SWITCH
Power OK LED
Figure 2.3 RexIO X13 board as reference - Top
RexIO - 25G Ethernet and eCPRI test card
FH dummy board
Nominal voltage PA
supply (voltage level
setable at startup)
PA supply with
adjustable tapering PA
voltage level
Radio Module PSU 880 – 1300 W
Surge protection,
EMC, Inrush and
polarity protection.
Power
measurement
DC power
in -48VDC
Common bus converter +12V
Regulators.
SFP supply
CG1
supply
Main clock generator (CG1)
PLLs
Frequency
synthesizer
Clock
Buffer
Device ctrl.
& status
Fly-over Cable
connector
Fly-over cable
25/50GE eCPRI
TRX board (same size and desing as the product board)
32 PAs in columns C3 -C6
32 PAs in columns C1,C2 and C7, C8
RF-lineup
supplies
Power Sequencer
Voltage
mnitoring
GPIO
Control
HW
Reset(s)
Watchdog(s)
TRX Free-run clocks
Mars SoCs
1GE switch
Master Mars SoC
HWID-0
Slave Mars SoC
HWID-1
Slave Mars SoC
HWID-2
Slave Mars SoC
HWID-3
LTE: 8x20 MHz, NR:2x100 MHz /pipe
16T16R, oBW=200 MHz, iBW=400 MHz
ARM O&M PSS & DDR & Peripherals
PSS & DDR & Peripherals
Sync., 1GE, GPIO, Ctrl. Bus, Test
RFIC 8TRX
Analog FE x8
IGE C&M
Switch
UART
MUX
VCXO
CG2
Secure
Boot
eMMC
Flash 8GB
TPM
v.2.0
DDR4
1GB
JESD204C
25/50GE eCPRI
BCN_Trigger
Sys. Clk.
1pps ref. Clk. output
I2C GPIO
SPI/
GPIO


✓ RF7 3GPP LTE/5G 64TRx,
✓ 200 MHz oBW / 200 MHz iBW
✓ 16DL/16UL MIMO streams (FH 7-2 Init.)
✓ 16DL/8UL MIMO layers (FH 7-3 sw updt.)
TRX Module
TRX sub-assembly
FH sub-assembly
-48V
Radio Module PSU
880 – 1300 W
System Module
ABIO
Ethernet private / public transport network.
4x 10GE / 25GE / 50GE
Thor L1 Low engine
Sync. Master
16 streams NR: 2x 100 MHz
ETH IRC / Precode. BF ETH
Ctrl. Sync.
4x 50GE eCPRI
16x JESD
MARS DFE Master SoC
16TRx
LTE: 4x20 MHz, NR: 2x100 MHz / pipe
oBW =200MHz iBW=200 MHz
O&M Master
PSS
Security host
ETH FFT/ iFFT DFE JESD
Misc.
MARS DFE Slave SoC
16TRx
LTE: 4x20 MHz, NR: 2x100 MHz / pipe
oBW =200MHz iBW=200 MHz
ETH FFT/ iFFT DFE JESD
Misc.
8T8R RFIC
JESD DAC/ADC
Analog FE x4
PA
FB
LNA
16
Antenna module


✓ RF7 3GPP LTE/5G 32TRx,
✓ 200 MHz oBW / 200 MHz iBW
✓ 16DL/16UL MIMO streams (FH 7-2 Init.)
✓ 16DL/8UL MIMO layers (FH 7-3 sw updt.)
TRX Module
TRX sub-assembly
-48V
Radio Module PSU
880 – 1300 W
Ethernet
private / public
transport
network.
System Module
ABIO
2x 10GE / 25GE / 50GE
2x 50GE
eCPRI
Thor L1 Low engine
Sync. Master
16 streams NR: 2x 100 MHz
ETH
IRC / Precode.
BF
ETH
Ctrl.
Sync.
MARS DFE Master SoC
16TRx
LTE: 4x20 MHz, NR: 2x100 MHz / pipe
oBW =200MHz iBW=200 MHz
O&M Master
PSS
Security host
ETH
FFT/ iFFT
DFE
JESD
Misc.
16x JESD
8T8R RFIC
JESD
DAC/ADC
Analog FE x4
PA
FB
LNA
16
Antenna module

RF7 4G/5G 64 mMIMO TRX 200MHz oBW, 200MHz iBW
16DL/8UL MIMO layers (7-3 FH split)
16DL/16UL MIMO streams (7-2 FH split)

FH sub-assembly

Ant. Mon. port
DC power in -48VDC
Radio Module PSU 880 – 1300 W
Surge protection, EMC, Inrush and polarity protection.
Power measurement
Nominal voltage PA supply (voltage level setable at startup)
PA supply with adjustable tapering PA voltage level
Common bus converter +12V
Power Sequencer
Voltage mnitoring
GPIO Control
Watchdog(s)
HW Reset(s)
PWR_EN
V_MON
Resets / GPIOs
POLs /Reg. Group #1
Thor POL supplies
Thor Core supply
Unit LED
FAN/ TX LED
R&D test connector
PCIe
JTAG
Boot Flash 256MB
DDR5 16GB (16Gbit x16 (12pcs)
DDR5 4GB
ECC
+12V
AISG
RET Ctrl.
EAC 6A/1C
SFP56
10/25/50 GE eCPRI
Thor L1 Low Engine
Device_ID-00
JTAG
Trace
I2C
QSPI
UART
GPIO
Mem0
Mem1
Mem2
Mem3
RST
DSP Cores (L1 Low)
Digital BF DL / UL
BF DL distrip.
Channel Estimation
UL signal combining
Pre-coding
ARM Cores O&M
Local O&M control
PTP -BNC Sync.
4x 25GE or 2x 50GE
8x 50GE
8x 50GE eCPRI
SPI
Sync. IF
1GE
1PPS Sync.
BCN sys. Ref.
Misc. Ctrl.
JTAG/BSCAN
UART TX/RX
Unit LED
SEQ. PWR. GOOD
Thor Reset
LMI
Vcc (3.3V)
SGMII
UART
Test clk.
JTAG/ BSCAN
1 PPS -ref. Clk.
Sys. Clk.
Init. + PTP freq. tune
LMI test clk. input
XO
TCXO
Main clock generator (CG1)
PLLs
Frequency synthesizer
Clock Buffer
Device ctrl. & status
XO 100M
Thor ARM cores, System, Mem.,
Mars 1-4
POL / Reg. GROUP2
DFE 1 Core supply
DFE 2 Core supply
DFE 1 & 2 POL supplies
Ctrl.
Power Sequencer
Voltage mnitoring
GPIO Control
HW Reset(s)
Watchdog(s)
PWR_EN
V_MON
Resets / GPIOs
TRX Free-run clocks
XO 125M
XO 25M
Mars SoCs
1GE switch
1GE C&M Switch
Init
Fly-over cable
CG2
PLLs
Synthesizer
Device ctrl. & status
Clock Buffer outputs
Sys. Clk.
Init
Ctrl.
VCXO
BCN sys. Ref. + DFE sys. Ref.
Resets / GPIOs
DDR4 1GB
TPM v.2.0
Secure Boot FLASH 256MB
eMMC Flash 8GB
DDR4 ctrl.
SPI
QSPI
eMMC
I2C
PWM
JTAG
Master Mars SoC
Device_ID-0000
LTE: 8x20 MHz, NR:2x100 MHz /pipe
16T16R, oBW=200 MHz, iBW=400 MHz
GPIO(s)
SGMII
ARM O&M PSS & DDR & Peripherals
50GE
L1Low
FFT / iFFT
DL
CFR
DPD
UL
TXRXC AIM
RFIF
16x JESD
SPI
MDIO
SGMII
Ref. Clk
Sync., 1GE, GPIO, Ctrl. Bus, Test
JTAG
Slave Mars SoC
Device_ID-0010
LTE: 8x20 MHz, NR:2x100 MHz /pipe
16T16R, oBW=200 MHz, iBW=400 MHz
4x Tx
2x Rx
1x FB
I2C GPIO
SPI/ GPIO
JESD204C
RFIC 8TRX
8X DAC
2X FADC
8X ADC
8X JESD
Analog FE x8
PA
FB
LNA
x8
BF_CAL_32_0
BF_CAL_32_1
Factory_cal / Tx_mon
Wilkinson Antenna calibartion network
Coaxial cable
32 PAs in columns C3 -C6
32 PAs in columns C1,C2 and C7, C8
RF-lineup supplies
RF-Lineups 64 PAs
P5V_RX
P1V8_PAM
P5V_PAM
N10V_PAM
P5V_PAM_bias

TRX sub-assembly

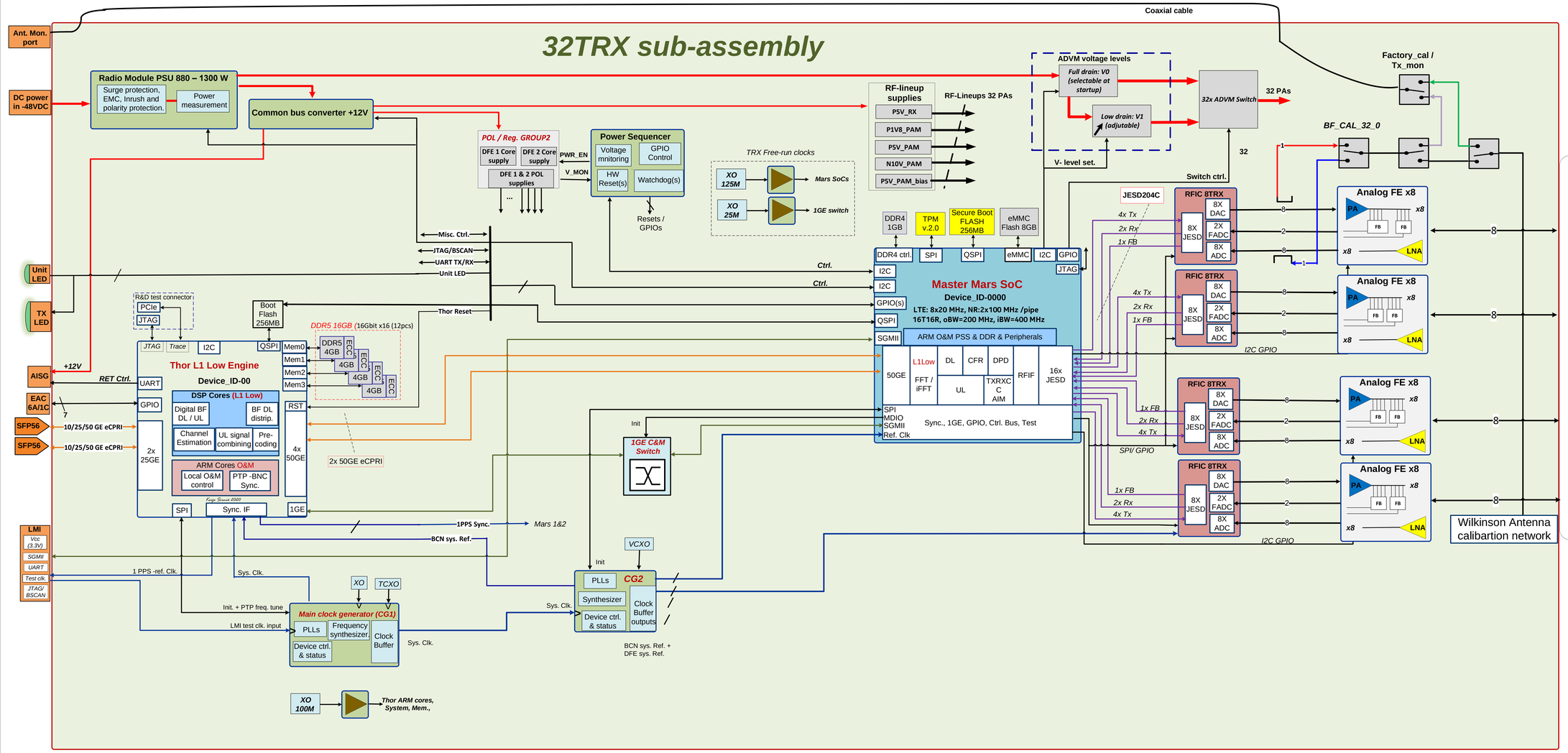
FH sub-assembly

192 AE ; 4 rows x 8 colums x 2 polarizations

Filtenna

Filter sub-assembly

RF7 4G/5G 32 mMIMO TRX 200MHz oBW, 200MHz iBW
16DL/8UL MIMO layers (7-3 FH split)
16DL/16UL MIMO streams (7-2 FH split)



RF7 4G/5G 64 mMIMO TRX 400MHz oBW, 400MHz iBW
16DL/8UL MIMO layers (7-3 FH split)
16DL/16UL MIMO streams (7-2 FH split)

FH sub-assembly

64TRX sub-assembly

Coaxial cable

Ant. Mon. port

DC power in -48VDC

Radio Module PSU 880 – 1300 W
Surge protection, EMC, Inrush and polarity protection.
Power measurement

Nominal voltage PA supply (voltage level setable at startup)

PA supply with adjustable tapering PA voltage level

Common bus converter +12V

32 PAs in columns C3 -C6

32 PAs in columns C1,C2 and C7, C8

RF-lineup supplies
P5V_RX
P1V8_PAM
P5V_PAM
N10V_PAM
P5V_PAM_bias

RF-Lineups 64 PAs

Factory_cal / Tx_mon

BF_CAL_32_0

Power Sequencer
Voltage mnitoring
GPIO Control
Watchdog(s)
HW Reset(s)
PWR_EN
V_MON
POLs /Reg. Group #1
Thor POL supplies
Thor Core supply
Resets / GPIOs

POL / Reg. GROUP2
DFE 1 Core supply
DFE 2 Core supply
DFE 1 & 2 POL supplies

Power Sequencer
Voltage mnitoring
GPIO Control
HW Reset(s)
Watchdog(s)
PWR_EN
V_MON
Resets / GPIOs

TRX Free-run clocks
XO 125M → Mars SoCs
XO 25M → 1GE switch

DDR4 1GB
TPM v.2.0
Secure Boot FLASH 256MB
eMMC Flash 8GB

PWM/RPM Ctrl.

Misc. Ctrl.
JTAG/BSCAN
UART TX/RX
LED ctrl.
SEQ. PWR. GOOD
Thor Reset

Unit LED
FAN/ TX LED
+12V
AISG
RET Ctrl.
EAC 6A/1C
7

R&D test connector
PCIe
JTAG

Boot Flash 256MB

DDR5 16GB (16Gbit x16 (12pcs)
DDR5 4GB ECC

Thor L1 Low Master Engine
Device_ID-00
JTAG Trace I2C QSPI UART GPIO
Mem0 Mem1 Mem2 Mem3 RST
8x 50GE

DSP Cores (L1 Low)
Digital BF DL / UL
BF DL distrip.
Channel Estimation
UL signal combining
Pre-coding

ARM Cores O&M
Local O&M control
PTP -BNC Sync.

50GE 50GE PCIe ctrl.IF Sync IF SPI 1GE
8x 50GE eCPRI

Fly-over cable

Master Mars SoC
Device_ID-0000
LTE: 8x20 MHz, NR:2x100 MHz /pipe
16T16R, oBW=200 MHz, iBW=400 MHz
I2C I2C GPIO(s) QSPI SGMII
ARM O&M PSS & DDR & Peripherals
50GE FFT / iFFT L1Low DL CFR DPD UL TXRXC C AIM RFIF 16x JESD
SPI MDIO SGMII Ref. Clk
Sync., 1GE, GPIO, Ctrl. Bus, Test
DDR4 ctrl. SPI QSPI eMMC I2C PWM JTAG

JESD204C

RFIC 8TRX
8X JESD
8X DAC
2X FADC
8X ADC

8x Tx
4x Rx
2x FB
SPI/ GPIO
I2C GPIO

Analog FE x8
PA x8
FB FB
LNA x8

Slave Mars SoC
Device_ID-0001
LTE: 8x20 MHz, NR: 2x100 MHz / pipe
16T16R, oBW=200 MHz, iBW=400 MHz
PSS & DDR & Peripherals
50GE FFT / iFFT L1Low DL CFR DPD UL TXRXC C AIM RFIF 16x JESD
Sync., 1GE, GPIO, Ctrl. Bus, Test
DDR4 1GB
JTAG

Slave Mars SoC
Device_ID-0010
LTE: 8x20 MHz, NR:2x100 MHz /pipe
16T16R, oBW=200 MHz, iBW=400 MHz
ARM PSS & DDR & Peripherals
50GE FFT / iFFT L1Low DL CFR DPD UL TXRXC C AIM RFIF 16x JESD
Sync., 1GE, GPIO, Ctrl. Bus, Test
DDR4 1GB
JTAG

Slave Mars SoC
Device_ID-0011
LTE: 8x20 MHz, NR: 2x100 MHz / pipe
16T16R, oBW=200 MHz, iBW=400 MHz
PSS & DDR & Peripherals
50GE FFT / iFFT L1Low DL CFR DPD UL TXRXC C AIM RFIF 16x JESD
Sync., 1GE, GPIO, Ctrl. Bus, Test
DDR4 1GB
JTAG

Init
1GE C&M Switch
Mars 1-4

LMI
Vcc (3.3V)
JTAG/ BSCAN
SGMII
UART
Test clk.
SoC & Flash JTAG

1PPS Sync.
BCN sys. Ref.

FH switch
50GE 50GE PCIe ctrl.IF 1GE
4x 25GE
eCPRI routing and switching based on eAxC IDs
Physical layer SyncE clock recovery
50GE 50GE Sync IF

SFP56 10/25/50 GE eCPRI ×4

XO 100M
Thor ARM cores, System, Mem.,

Init. + PTP freq. tune

SyncE recov. clk.

XO TCXO
SPI
Main clock generator (CG1)
Frequency synthesizer
Device ctrl. & status
Clock Buffer
PLLs

LMI test clk. input

Boot Flash 256MB
QSPI

Thor L1 Low Slave Engine
Device_ID-01
50GE 50GE QSPI Sync IF 1GE
8x 50GE eCPRI
8x 25GE
R&D test connector
PCIe JTAG Trace JTAG
DSP Cores (L1 Low)
Digital BF DL / UL
BF DL distrip.
Channel Estimation
UL signal combining
Pre-coding
ARM Cores O&M
Local O&M control
BNC Sync.
Mem3 Mem2 Mem1 Mem0
DDR5 4GB ECC

DDR5 16GB (16Gbit x16 (12pcs)

BCN sys. Ref. + DFE sys. Ref.
PLLs CG2
Synthesizer
Device ctrl. & status
Clock Buffer outputs
Sys. Clk.
Init
Ctrl.
VCXO

POL / Reg. GROUP3
DFE 3 Core supply
DFE 4 Core supply
DFE 3 & 4 POL supplies
PWR_EN
V_MON
Power Sequencer
Voltage mnitoring
GPIO Control
HW Reset(s)
Watchdog(s)
Resets / GPIOs

Wilkinson Antenna calibartion network

BF_CAL_32_1

192 AE ; 4 rows x 8 colums x 2 polarizations

Filtenna

Filter sub-assembly