

Universidad de Costa Rica
Escuela de Ingeniería Eléctrica
IE0624 - Laboratorio de Microcontroladores

Laboratorio 1

Introducción a microcontroladores y manejo de GPIOS

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4 de septiembre de 2022

Introducción

En este documento se presenta el desarrollo de solución al Laboratorio 1 del curso Laboratorio de Microcontroladores correspondiente a una implementación de tombola de bingo que genera números aleatorios y que al sacar 16 números se reinicia. El método de generación de números aleatorios corresponde a un *linear-feedback shift register* que produce una serie de unos y ceros que luego son utilizados para obtener una señal analógica de entre 0 V y 3.2 V que luego se traduce a señales digitales para controlar un par de *displays* de 7 segmentos y desplegar en ellos los números del 0 al 9. Se utiliza un PIC12F675 para contar la cantidad de números aleatorios generados y producir una señal de control para mostrar el número 99 cuando se alcanzan 16 números aleatorios generados.

Todos los recursos asociados la solución desarrollada se encuentran en el siguiente repositorio: https://github.com/yennergonzalez/Laboratorio_Microcontroladores_1.

Nota teórica

Información general del microcontrolador

El PIC12F675 es un microcontrolador sencillo con una arquitectura RISC de 8 bits y cuyo conjunto de instrucciones está conformado por 35 instrucciones (la mayoría ejecutadas en un único ciclo) [2].

Dentro de sus características destacan además:

- Oscilador interno con una frecuencia de 4 MHz.
- Amplio rango de tensiones de operación (2.0 V a 5.5 V)
- Reducido consumo de energía (corriente de *standby* de 1 nA y corriente de operación a 1 MHz de $100 \mu A$)
- ADC con resolución de 10 bits y 4 canales de entrada.
- Memoria de programa de 1024 *words* y memoria de datos de 192 bytes (64 bytes de SRAM y 128 bytes de EEPROM)

Características eléctricas del microcontrolador

Para el diseño del circuito completo es necesario considerar las características eléctricas del microcontrolador a utilizar. Para esto las más importantes a considerar son el consumo de potencia y la corriente suministrada por el microcontrolador, de manera que se pueda garantizar que el microcontrolador pueda soportar las condiciones de operación y no dañarse. A continuación se muestran las características eléctricas del microcontrolador reportadas en la hoja del fabricante [2]:

12.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings†

Ambient temperature under bias.....	-40 to +125°C
Storage temperature	-65°C to +150°C
Voltage on VDD with respect to Vss	-0.3 to +6.5V
Voltage on MCLR with respect to Vss	-0.3 to +13.5V
Voltage on all other pins with respect to Vss	-0.3V to (VDD + 0.3V)
Total power dissipation ⁽¹⁾	800 mW
Maximum current out of Vss pin	300 mA
Maximum current into VDD pin	250 mA
Input clamp current, I _{IK} (V _I < 0 or V _I > V _{DD}).....	± 20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{DD}).....	± 20 mA
Maximum output current sunk by any I/O pin.....	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by all GPIO	125 mA
Maximum current sourced all GPIO.....	125 mA

Figura 1: Características eléctricas del microcontrolador PIC12F675 [2].

Periféricos

Para su interfaz con periféricos el microcontrolador cuenta con 6 pines GPIO (a excepción de GP3 que solo se puede utilizar como entrada, todos los pines se pueden configurar para operar como entradas o como salidas). Para configurar el modo de operación de estos pines se utilizan los registros TRISIO, GPIO, CMCON, ANSEL y CONFIG que se comentarán en la siguiente sección [2].

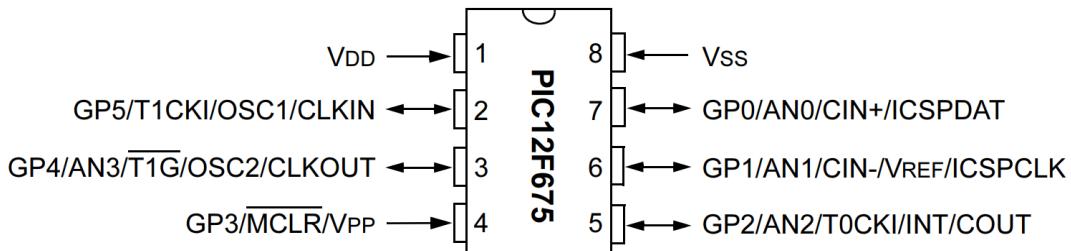


Figura 2: Diagrama de pines del microcontrolador PIC12F675 [2].

Registros

TRISIO

El registro TRISIO es un registro de 8 bits (de los cuales solo los 6 bits menos significativos se pueden configurar) que se utiliza para definir el modo de operación de los pines GPIO, si un bit de TRISIO se coloca en alto, el pin GPIO correspondiente será una entrada y si el bit de TRISIO es bajo, el pin GPIO asociado operará como salida.

REGISTER 3-2: TRISIO — GPIO TRISTATE REGISTER (ADDRESS: 85h)

U-0	U-0	R/W-x	R/W-x	R-1	R/W-x	R/W-x	R/W-x
—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0
bit 7						bit 0	

Figura 3: Diagrama del registro TRISIO [2].

GPIO

El registro GPIO almacena el estado de cada uno de los pines GPIO. Si se escribe a este registro se escribe al *latch* del puerto, modificando el estado correspondiente.

Al igual que con el registro TRISIO, este registro es de 8 bits pero solo 6 de ellos son configurables (uno asociado a cada pin GPIO).

REGISTER 3-1: GPIO — GPIO REGISTER (ADDRESS: 05h)

Figura 4: Diagrama del registro GPIO [2].

CMCON

El registro CMCON se utiliza para configurar al comparador y elegir uno de sus 8 modos de operación. Para este laboratorio el comparador no se utilizó por lo que se colocó en el modo de comparador apagado. (CMCON=111).

REGISTER 6-1: CMCON — COMPARATOR CONTROL REGISTER (ADDRESS: 19h)

U-0	R-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	COUT	—	CINV	CIS	CM2	CM1	CM0
bit 7				bit 0			

Figura 5: Diagrama del registro CMCON [2].

ANSEL

El registro ANSEL se utiliza para configurar cuales puertos del microcontrolador serán utilizados como entradas analógicas ($\text{ANSEL}[i]=1$) o como I/O digital o función especial ($\text{ANSEL}[i]=0$). Para este laboratorio no se utilizó ningún puerto como entrada analógica por lo que a todo el registro ANSEL se le asignó un valor de cero.

REGISTER 7-2: ANSEL — ANALOG SELECT REGISTER (ADDRESS: 9Fh)

U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1
—	ADCS2	ADCS1	ADCS0	ANS3	ANS2	ANS1	ANS0
bit 7				bit 0			

Figura 6: Diagrama del registro ANSEL [2].

CONFIG

El registro **CONFIG** es un registro del microcontrolador que permite seleccionar múltiples configuraciones del dispositivo, entre ellas destacan la selección del oscilador, la habilitación del *Watchdog Timer*, la habilitación del *Power-up Timer*, la selección de función del pin **MCLRE**, entre otras. Para este laboratorio este registro se utilizó para deshabilitar el *Watchdog Timer* para evitar que el microcontrolador pasara al estado de **SLEEP**.

REGISTER 9-1: CONFIG — CONFIGURATION WORD (ADDRESS: 2007h)

R/P-1	R/P-1	U-0	U-0	U-0	R/P-1									
BG1	BG0	—	—	—	CPD	CP	BODEN	MCLRE	PWRTE	WDTE	FOSC2	FOSC1	FOSC0	
bit 13														bit 0

Figura 7: Diagrama del registro CONFIG [2].

Diseño del circuito

En esta sección se describe el diseño del circuito realizado. Inicialmente se realizó una pequeña investigación sobre distintos métodos de generar números aleatorios y se decidió utilizar el método de *linear-feedback shift register* por sus posibles configuraciones para garantizar períodos de repetición de secuencias relativamente extensos. Después de haber definido la configuración del LFSR, el resto del circuito se diseñó de manera que se pudiera controlar el LFSR mediante el PIC12F675.

Generación de números aleatorios - LFSR

Para la generación de números aleatorios se prefirió utilizar un *linear feedback shift register* de 24 etapas utilizando la configuración Fibonacci debido a que la salida de este sería bastante similar a ruido blanco y por ende los resultados obtenidos parecerían verdaderamente aleatorios. De acuerdo a la fuente consultada, para esta configuración la secuencia se repite después de $2^{24} - 1$ ciclos de reloj [3].

A continuación se presenta el esquemático seguido para la implementación del LFSR:

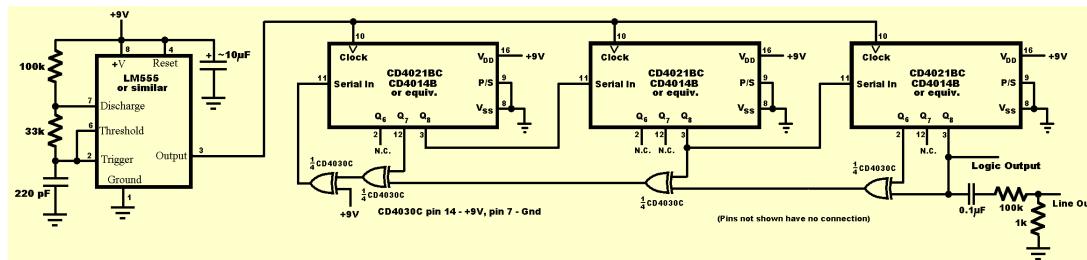


Figura 8: Esquemático de la configuración de LFSR utilizada [3]

Circuito complementario

El conjunto complementario consiste en los demás componentes utilizados para implementar una interfaz entre el LFSR y el microcontrolador. Particularmente se utilizaron flip-flops en cascada a la salida del LFSR para obtener 4 bits aleatorios, luego estos se alimentaron a un conversor digital-analógico para convertirlos en una señal de entre 0 V y 3.2 V y luego esa señal se alimentó a una entrada de un multiplexor analógico (la otra entrada está permanentemente conectada a 3.2 V para

poder implementar el parpadeo del 99 al finalizar el juego) cuya salida finalmente se alimenta a un conversor analógico-digital que finalmente se alimenta a un *display* de 7 segmentos BCD.

Para el microcontrolador se utilizan una entrada y una salida y ambas funcionan como señales de selección de multiplexores, la entrada se utiliza para indicar que se debe generar un número aleatorio y permite la transmisión de la señal de reloj hacia el LFSR (además de ser contada por el microcontrolador para determinar cuantos números han salido). La salida del microcontrolador es normalmente baja y se pone en alto cuando han salido 16 números y por lo tanto hace que los multiplexores que controlan la entrada del *display* seleccionen la entrada de 3.2 V permanente en lugar de la entrada proveniente del LFSR.

Lista de componentes y costos

Cantidad	Componente	Costo unitario
1	Multiplexor digital	\$0.82
2	Multiplexores analógicos	\$1.13
1	PIC12F675	\$1.77
2	Convertidor analógico-digital	\$9.16
2	Convertidor digital-analógico	\$9.09
3	Registros desplazables de 8 etapas	\$0.82
4	Compuertas XOR	\$0.65
1	Interruptor	\$0.35
4	Resistores	\$0.50 (10 unidades)
2	Capacitores	\$0.45
6	Flip-flops tipo D	\$0.83
2	<i>Displays</i> 7 Segmentos	\$1.59

Tabla 1: Tabla de costos de los componentes utilizados [4]

Nota: Para el circuito realizado en SimulIDE se utilizaron algunos de los circuitos integrados genéricos implementados propiamente en SimulIDE por lo que los precios reportados en la tabla anterior corresponden a componentes reales con características similares.

Costo total

De acuerdo con los precios reportados, el costo total de los componentes utilizados sería de \$56.32. Este precio es bastante elevado por lo que es claro que la implementación propuesta no es la mejor en términos económicos. Observando la lista de precios sobresalen los ADCs y DACs como los componentes que elevan tanto el precio por lo que la mejor opción si aún se quisiera implementar esta topología de circuito sería buscar alternativas más económicas de estos componentes.

Conceptos/temas de laboratorio

Generación de números aleatorios

El primer tema del laboratorio consistió en la generación de números aleatorios, como se comentó en secciones anteriores, esta se decidió implementar por *hardware* mediante un *linear feedback shift register*.

Manejo de rebotes de un botón

Otro tema del a considerar en el laboratorio consistió en el manejo de los rebotes resultantes al presionar un botón. Esto se decidió implementar por *hardware* mediante un circuito RC. Este se configura de manera que la constante de tiempo posea un valor aproximado al tiempo esperado de rebote. En este caso se encontró una implementación que asumía 1 milisegundo y se decidió replicar ese mismo diseño.

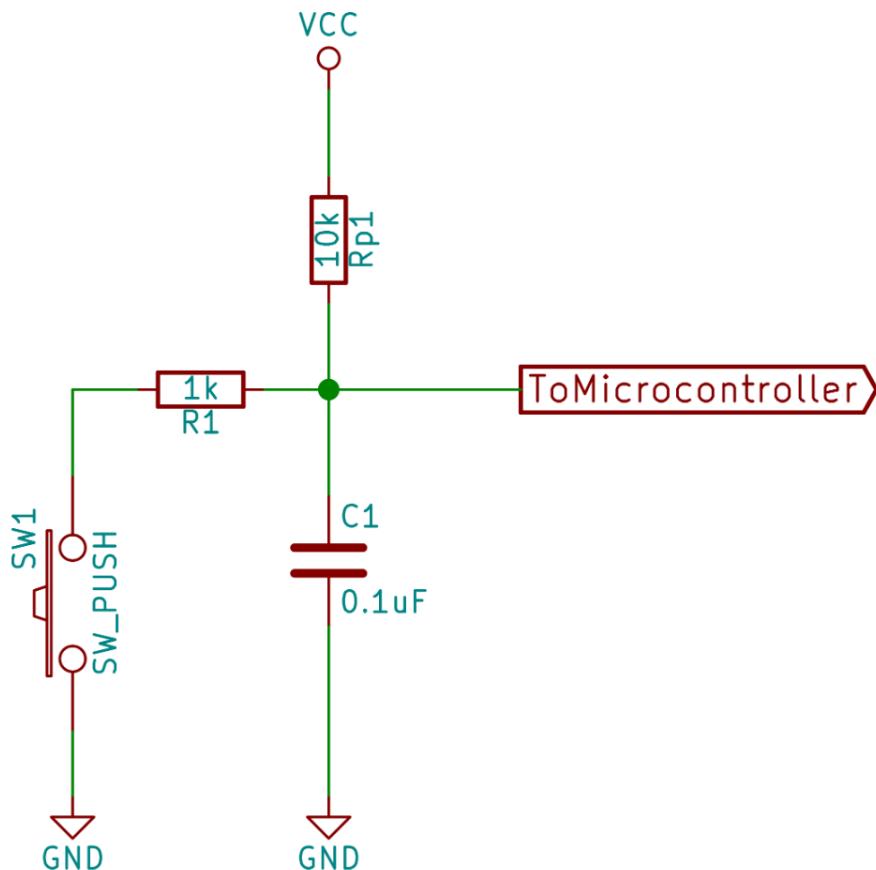


Figura 9: Diagrama esquemático del diseño de circuito RC seguido para solucionar los rebotes del botón [1].

Desarrollo

Análisis del programa

Previo al desarrollo del programa se realizó el siguiente diagrama de flujo del funcionamiento que debería realizar de acuerdo a lo solicitado en el enunciado:

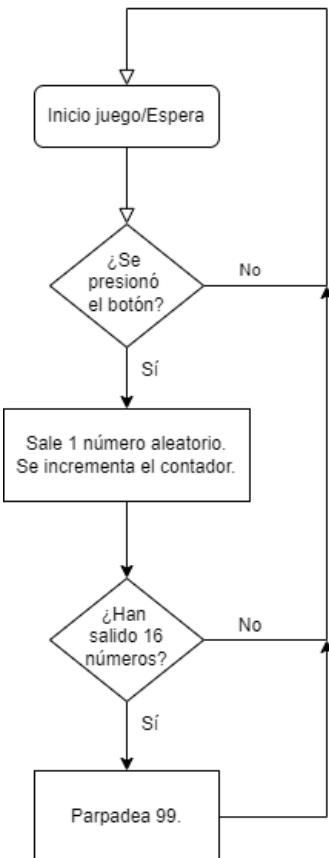


Figura 10: Diagrama de flujo del programa implementado para el laboratorio. Creación propia.

El programa desarrollado es bastante sencillo y consiste de una sección de configuración inicial donde se configura el modo de operación de los pines del microcontrolador y el *main* del programa que se ejecuta en un ciclo infinito.

Configuración

En la sección de configuración se definen valores para los registros TRISIO, ANSEL, CMCON y GPIO. TRISIO se define como 0b00000001 de manera que el pin GPO funcione como entrada (para detectar si el botón es presionado) y los demás como salidas.

Al registro ANSEL se le asigna un valor de cero pues no la única entrada del microcontrolador será digital, no analógica y al registro CMCON se le asigna un valor de 111 pues no se utilizará la función de comparador del microcontrolador.

Adicionalmente en esta sección también se define una variable **count** que se inicializa en cero y que se utilizará para llevar la cuenta de cuántos números han salido en el juego actual de bingo (cantidad de veces que el botón ha sido presionado para generar un número aleatorio).

Función principal - *main*

La función principal consiste de un ciclo *while* infinito que permitirá que el juego de bingo se reinicie tras sacarse 16 números. Dentro del *while* se utiliza un *if-else* para verificar si han salido 16 o más números, de no ser así se revisa si el botón se presionó y luego se dejó de presionar y se genera un número aleatorio y se incrementa el contador una vez. Si el contador alcanza los 16 números se entra en el *else* y se pone el pin GP4 en alto (para hacer parpadear el número 99), luego se pone en bajo y se reinician tanto el contador como el programa.

Análisis del circuito

A continuación se muestra el circuito diseñado para implementar el generador de números de bingo:

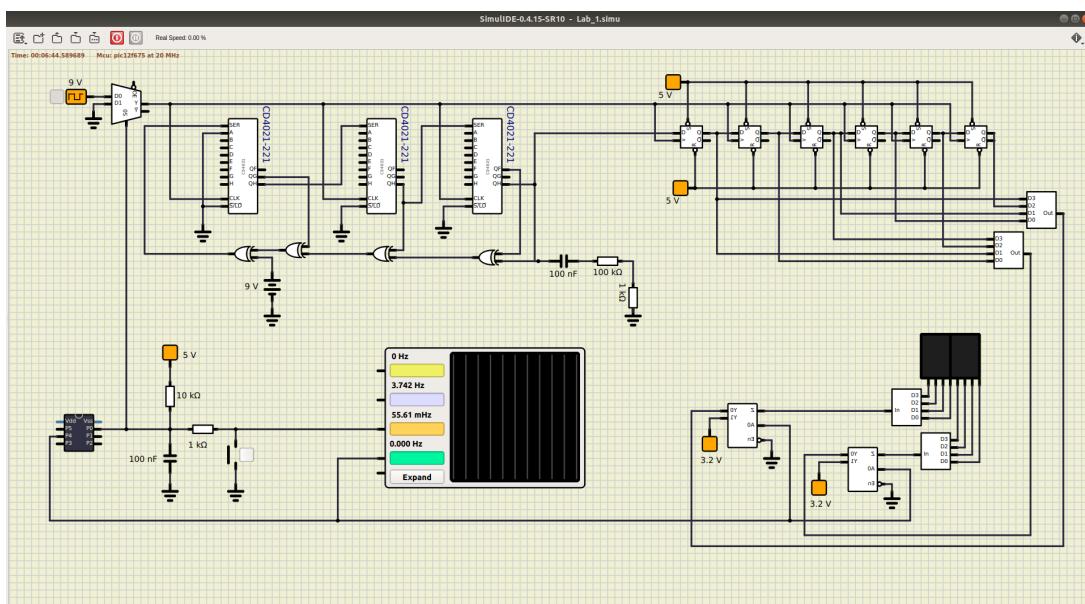


Figura 11: Diagrama esquemático del circuito diseñado.

El circuito está conformado por 4 bloques:

- El *linear feedback shift register* de 24 etapas.
- 6 *Flip-flops* conectados en cascada y cuyas salidas se alimentan a un convertidor digital-analógico.
- El microcontrolador PIC12F675 junto al botón y el circuito RC de *debouncing*.
- El *driver* de los *displays* de 7 segmentos conformado por un multiplexor que selecciona entre la salida del DAC y 3.2 V según el estado del pin GP4 y cuya salida va a un convertidor analógico-digital que finalmente enciende dos *displays* de 7 segmentos BCD.

A continuación se describe la operación del circuito:

Al presionar el botón el multiplexor del LFSR permite que la señal de reloj llegue a los registros desplazables y por ende que estos empiecen a producir una secuencia pseudo-aleatoria de “1”s y “0”s.

Luego esta secuencia se utiliza como entrada a los *flip-flops* de manera que a la salida de cada uno se almacene un uno o un cero, luego se transmiten 4 de estos unos y ceros al convertidor digital-analógico para convertir esa secuencia de 4 bits en una tensión de entre 0 V y 3.2 V que se alimenta a una de las entradas de un multiplexor analógico que la transmite al convertidor analógico-digital para producir una secuencia de 4 bits de 0000 a 1001 (0 a 9 en decimal).

Al presionar el botón el microcontrolador también aumenta un contador interno que al llegar a 16 pone en alto el pin GP4 que se utiliza como selector del multiplexor analógico de manera que cuando el contador es menor a 16 el multiplexor pone en su salida la tensión obtenida del DAC y si el contador es 16 entonces el multiplexor pone en su salida una tensión de 3.2 V que hace que se despliegue el número “9” en cada *display* de 7 segmentos.

Generando un número aleatorio

En la siguiente figura se puede observar en el osciloscopio la forma de onda al generar un número aleatorio tras presionar el botón una vez:

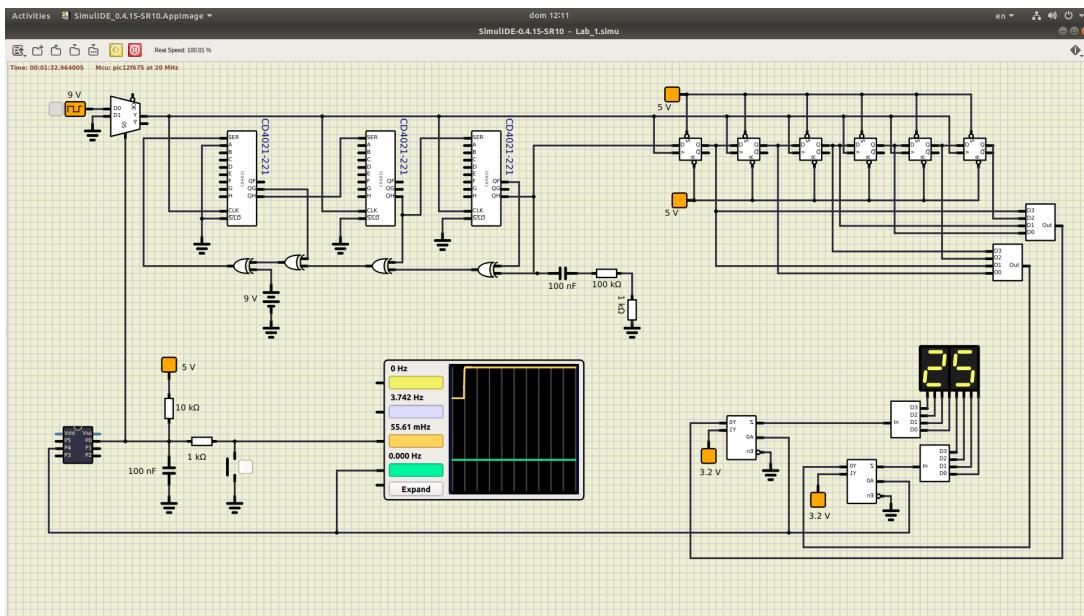


Figura 12: Circuito generando un número aleatorio.

El resultado es el esperado pues al presionar el botón se lleva al pin GP0 de un estado alto a uno bajo (y al dejar de presionar el botón este regresa a un estado alto como se observa en el osciloscopio) y se obtiene un número en los *displays* de siete segmentos. Además, el pin GP4 se mantiene en estado bajo porque no han salido 16 números.

Salida después de generar 16 números aleatorios

En la siguiente figura se muestra la salida producida por el microcontrolador después de haber generado 16 números:

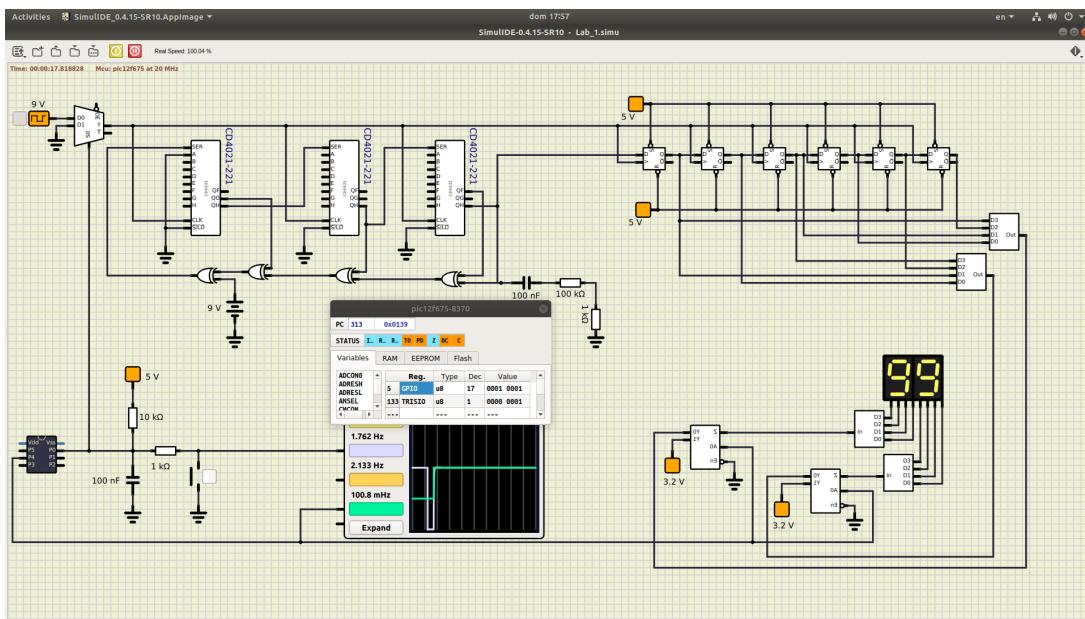


Figura 13: Circuito diseñado mostrando 99 después de haber generado 16 números aleatorios.

En la figura anterior se puede observar que la señal “azul” pasa de un estado alto a uno bajo (presionado del botón) y en el instante en que esta señal regresa a un uno lógico la señal “verde”, correspondiente al pin GP4 del microcontrolador se pone en alto, este es el comportamiento esperado pues en el programa este es el pin que comuta cuando la variable `count` alcanza un valor de 16. Adicionalmente, se puede observar que en los *displays* de 7 segmentos se muestra el número 99, de acuerdo a lo indicado por el enunciado. (Este número se mantiene por un tiempo, manejado por un *delay* en el programa y luego se hace comutar a GP4 nuevamente para reiniciar el juego)

También se puede notar que en el registro TRISIO se tiene el bit 5 en estado alto, lo cual concuerda con lo observado pues este es el bit correspondiente al pin GP4.

Conclusiones y recomendaciones

- Se logró implementar un simulador de tombola de bingo capaz de generar números aleatorios de entre 00 y 99.
- Se utilizó un método de generación de números aleatorios implementado por *hardware* a través de un *linear-feedback shift register*.
- Se utilizó un circuito RC para filtrar los rebotes producidos al presionar un botón.
- Se recomienda revisar posibles funciones de *SLEEP* o bajo consumo habilitadas por defecto en el microcontrolador a utilizar pues esto produjo algunas complicaciones y provocó que el programa no funcionara de la manera esperada.
- Se recomienda preferir soluciones por *software* sobre *hardware* si el costo económico de un proyecto es una prioridad.

Referencias

- [1] Elliot Williams. “Embed With Elliot: Debounce Your Noisy Buttons, Part I.” *Hackaday*, 9 Dec. 2015, <https://hackaday.com/2015/12/09/embed-with-elliot-debounce-your-noisy-buttons-part-i/>.
- [2] *PIC12F629/675 Data Sheet*. Microchip, <https://ww1.microchip.com/downloads/en/devicedoc/41190c.pdf>.
- [3] *White Noise Source - 24 Stage Linear Feedback Shift Register (LFSR)*. Michigan Technological University, <https://pages.mtu.edu/~suits/LFSR.html>. Accessed 4 Sept. 2022.
- [4] *Mouser Electronics*, <https://www.mouser.com>.

Apéndices

En esta sección se presentan las hojas del fabricante de los componentes utilizados. (O en el caso de haber utilizado componentes genéricos de SimulIDE se presentan hojas del fabricante con características similares)



MICROCHIP

PIC12F629/675

Data Sheet

**8-Pin FLASH-Based 8-Bit
CMOS Microcontrollers**

Note the following details of the code protection feature on Microchip devices:

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8-Pin FLASH-Based 8-Bit CMOS Microcontroller

High Performance RISC CPU:

- Only 35 instructions to learn
 - All single cycle instructions except branches
- Operating speed:
 - DC - 20 MHz oscillator/clock input
 - DC - 200 ns instruction cycle
- Interrupt capability
- 8-level deep hardware stack
- Direct, Indirect, and Relative Addressing modes

Special Microcontroller Features:

- Internal and external oscillator options
 - Precision Internal 4 MHz oscillator factory calibrated to $\pm 1\%$
 - External Oscillator support for crystals and resonators
 - 5 μ s wake-up from SLEEP, 3.0V, typical
- Power saving SLEEP mode
- Wide operating voltage range - 2.0V to 5.5V
- Industrial and Extended temperature range
- Low power Power-on Reset (POR)
- Power-up Timer (PWRT) and Oscillator Start-up Timer (OST)
- Brown-out Detect (BOD)
- Watchdog Timer (WDT) with independent oscillator for reliable operation
- Multiplexed MCLR/Input-pin
- Interrupt-on-pin change
- Individual programmable weak pull-ups
- Programmable code protection
- High Endurance FLASH/EEPROM Cell
 - 100,000 write FLASH endurance
 - 1,000,000 write EEPROM endurance
 - FLASH/Data EEPROM Retention: > 40 years

Low Power Features:

- Standby Current:
 - 1 nA @ 2.0V, typical
- Operating Current:
 - 8.5 μ A @ 32 kHz, 2.0V, typical
 - 100 μ A @ 1 MHz, 2.0V, typical
- Watchdog Timer Current
 - 300 nA @ 2.0V, typical
- Timer1 oscillator current:
 - 4 μ A @ 32 kHz, 2.0V, typical

Peripheral Features:

- 6 I/O pins with individual direction control
- High current sink/source for direct LED drive
- Analog comparator module with:
 - One analog comparator
 - Programmable on-chip comparator voltage reference (CVREF) module
 - Programmable input multiplexing from device inputs
 - Comparator output is externally accessible
- Analog-to-Digital Converter module (PIC12F675):
 - 10-bit resolution
 - Programmable 4-channel input
 - Voltage reference input
- Timer0: 8-bit timer/counter with 8-bit programmable prescaler
- Enhanced Timer1:
 - 16-bit timer/counter with prescaler
 - External Gate Input mode
 - Option to use OSC1 and OSC2 in LP mode as Timer1 oscillator, if INTOSC mode selected
- In-Circuit Serial ProgrammingTM (ICSPTM) via two pins

Device	Program Memory	Data Memory		I/O	10-bit A/D (ch)	Comparators	Timers 8/16-bit
	FLASH (words)	SRAM (bytes)	EEPROM (bytes)				
PIC12F629	1024	64	128	6	—	1	1/1
PIC12F675	1024	64	128	6	4	1	1/1

* 8-bit, 8-pin devices protected by Microchip's Low Pin Count Patent: U.S. Patent No. 5,847,450. Additional U.S. and foreign patents and applications may be issued or pending.

PIC12F629/675

Pin Diagrams

8-pin PDIP, SOIC, DFN-S

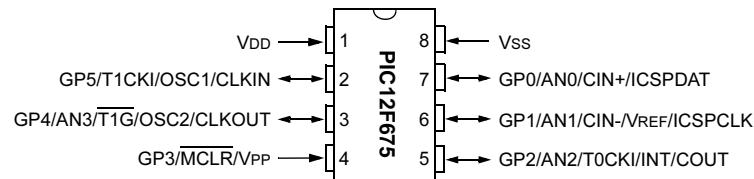
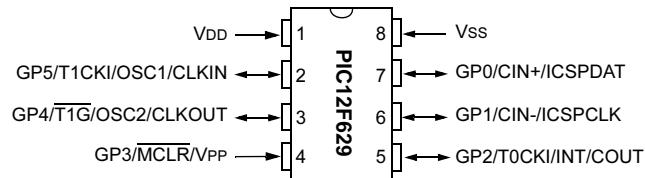


Table of Contents

1.0	Device Overview	5
2.0	Memory Organization.....	7
3.0	GPIO Port	19
4.0	Timer0 Module	27
5.0	Timer1 Module with Gate Control	30
6.0	Comparator Module	35
7.0	Analog-to-Digital Converter (A/D) Module (PIC12F675 only)	41
8.0	Data EEPROM Memory	47
9.0	Special Features of the CPU	51
10.0	Instruction Set Summary	69
11.0	Development Support	77
12.0	Electrical Specifications	83
13.0	DC and AC Characteristics Graphs and Tables	105
14.0	Packaging Information	115
Appendix A:	Data Sheet Revision History	121
Appendix B:	Device Differences	121
Appendix C:	Device Migrations	122
Appendix D:	Migrating from other PICmicro® Devices	122
Index	123	
On-Line Support	127	
Systems Information and Upgrade Hot Line	127	
Reader Response	128	
Product Identification System	129	

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PIC12F629/675

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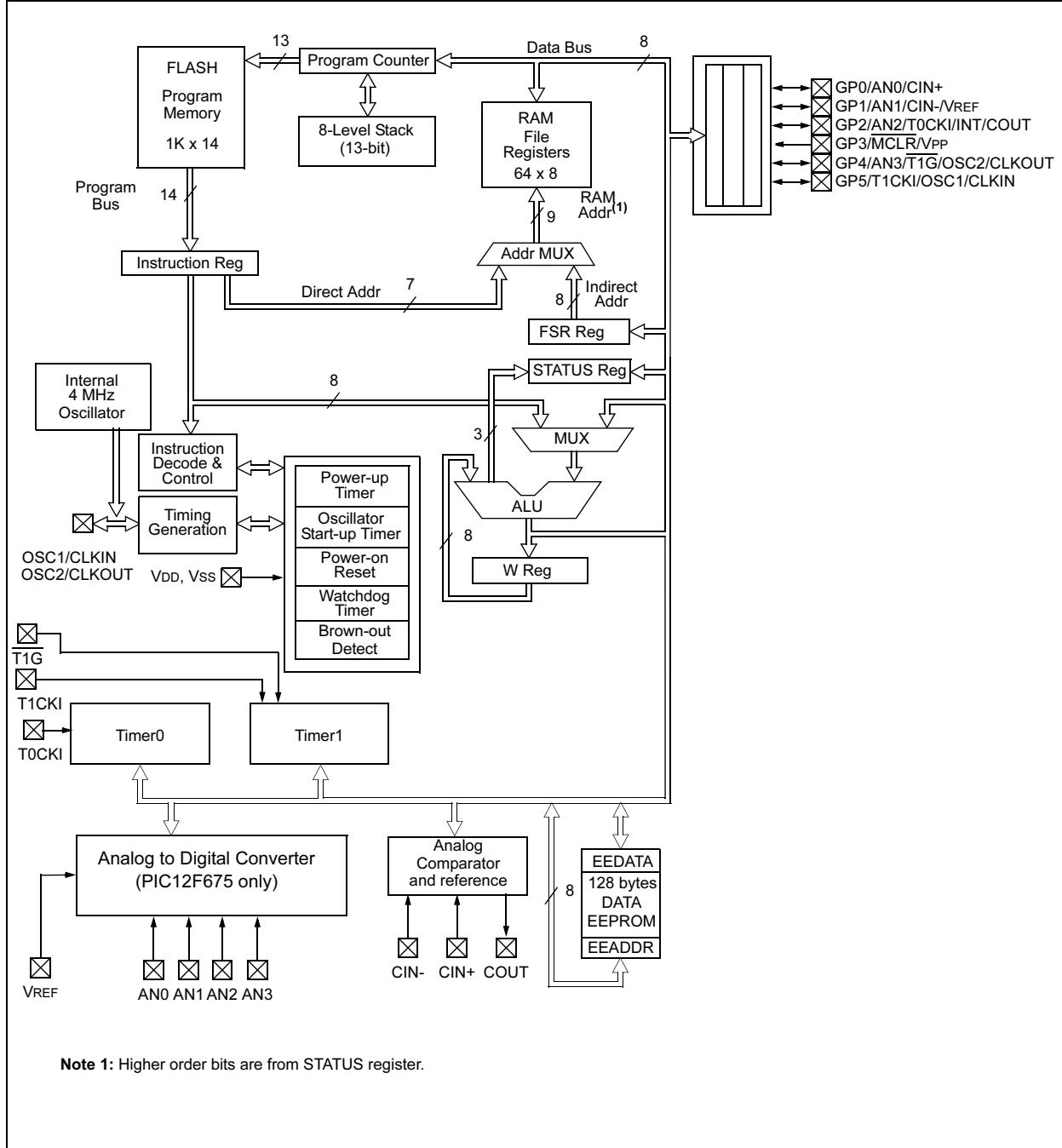
1.0 DEVICE OVERVIEW

This document contains device specific information for the PIC12F629/675. Additional information may be found in the PICmicro™ Mid-Range Reference Manual (DS33023), which may be obtained from your local Microchip Sales Representative or downloaded from the Microchip web site. The Reference Manual should be considered a complementary document to this Data

Sheet, and is highly recommended reading for a better understanding of the device architecture and operation of the peripheral modules.

The PIC12F629 and PIC12F675 devices are covered by this Data Sheet. They are identical, except the PIC12F675 has a 10-bit A/D converter. They come in 8-pin PDIP, SOIC, and MLF-S packages. Figure 1-1 shows a block diagram of the PIC12F629/675 devices. Table 1-1 shows the Pinout Description.

FIGURE 1-1: PIC12F629/675 BLOCK DIAGRAM



PIC12F629/675

TABLE 1-1: PIC12F629/675 PINOUT DESCRIPTION

Name	Function	Input Type	Output Type	Description
GP0/AN0/CIN+/ICSPDAT	GP0	TTL	CMOS	Bi-directional I/O w/ programmable pull-up and interrupt-on-change
	AN0	AN		A/D Channel 0 input
	CIN+	AN		Comparator input
	ICSPDAT	TTL	CMOS	Serial programming I/O
GP1/AN1/CIN-/VREF/ICSPCLK	GP1	TTL	CMOS	Bi-directional I/O w/ programmable pull-up and interrupt-on-change
	AN1	AN		A/D Channel 1 input
	CIN-	AN		Comparator input
	VREF	AN		External voltage reference
	ICSPCLK	ST		Serial programming clock
GP2/AN2/T0CKI/INT/COUT	GP2	ST	CMOS	Bi-directional I/O w/ programmable pull-up and interrupt-on-change
	AN2	AN		A/D Channel 2 input
	T0CKI	ST		TMR0 clock input
	INT	ST		External interrupt
	COUT		CMOS	Comparator output
GP3/MCLR/VPP	GP3	TTL		Input port w/ interrupt-on-change
	MCLR	ST		Master Clear
	VPP	HV		Programming voltage
GP4/AN3/T1G/OSC2/CLKOUT	GP4	TTL	CMOS	Bi-directional I/O w/ programmable pull-up and interrupt-on-change
	AN3	AN		A/D Channel 3 input
	T1G	ST		TMR1 gate
	OSC2		XTAL	Crystal/resonator
	CLKOUT		CMOS	Fosc/4 output
GP5/T1CKI/OSC1/CLKIN	GP5	TTL	CMOS	Bi-directional I/O w/ programmable pull-up and interrupt-on-change
	T1CKI	ST		TMR1 clock
	OSC1	XTAL		Crystal/resonator
	CLKIN	ST		External clock input/RC oscillator connection
Vss	Vss	Power		Ground reference
Vdd	Vdd	Power		Positive supply

Legend: Shade = PIC12F675 only

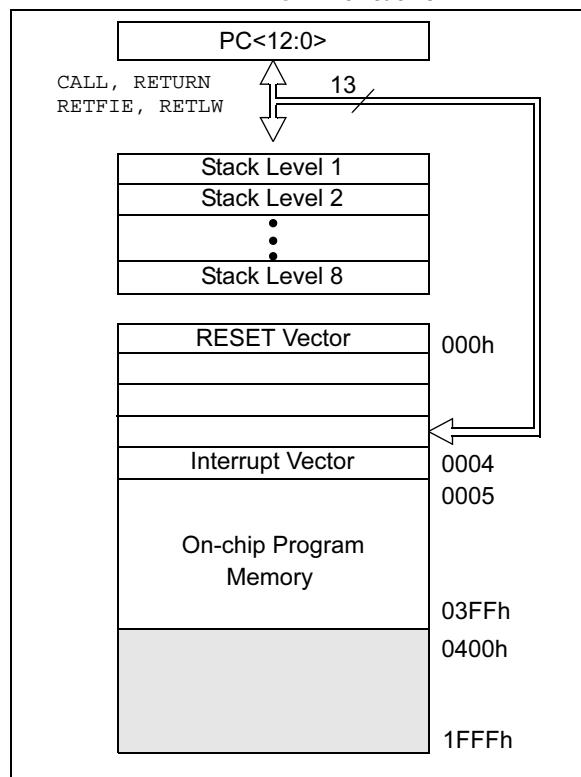
TTL = TTL input buffer, ST = Schmitt Trigger input buffer

2.0 MEMORY ORGANIZATION

2.1 Program Memory Organization

The PIC12F629/675 devices have a 13-bit program counter capable of addressing an 8K x 14 program memory space. Only the first 1K x 14 (0000h - 03FFh) for the PIC12F629/675 devices is physically implemented. Accessing a location above these boundaries will cause a wrap around within the first 1K x 14 space. The RESET vector is at 0000h and the interrupt vector is at 0004h (see Figure 2-1).

FIGURE 2-1: PROGRAM MEMORY MAP AND STACK FOR THE PIC12F629/675



2.2 Data Memory Organization

The data memory (see Figure 2-2) is partitioned into two banks, which contain the General Purpose registers and the Special Function registers. The Special Function registers are located in the first 32 locations of each bank. Register locations 20h-5Fh are General Purpose registers, implemented as static RAM and are mapped across both banks. All other RAM is unimplemented and returns '0' when read. RP0 (STATUS<5>) is the bank select bit.

- RP0 = 0 Bank 0 is selected
- RP0 = 1 Bank 1 is selected

Note: The IRP and RP1 bits STATUS<7:6> are reserved and should always be maintained as '0's.

2.2.1 GENERAL PURPOSE REGISTER FILE

The register file is organized as 64 x 8 in the PIC12F629/675 devices. Each register is accessed, either directly or indirectly, through the File Select Register FSR (see Section 2.4).

PIC12F629/675

2.2.2 SPECIAL FUNCTION REGISTERS

The Special Function registers are registers used by the CPU and peripheral functions for controlling the desired operation of the device (see Table 2-1). These registers are static RAM.

The special registers can be classified into two sets: core and peripheral. The Special Function registers associated with the "core" are described in this section. Those related to the operation of the peripheral features are described in the section of that peripheral feature.

FIGURE 2-2: DATA MEMORY MAP OF THE PIC12F629/675

File Address	File Address
Indirect addr. ⁽¹⁾	Indirect addr. ⁽¹⁾
00h	80h
TMR0	OPTION_REG
01h	81h
PCL	PCL
02h	82h
STATUS	STATUS
03h	83h
FSR	FSR
04h	84h
GPIO	TRISIO
05h	85h
06h	86h
07h	87h
08h	88h
09h	89h
PCLATH	PCLATH
0Ah	8Ah
INTCON	INTCON
0Bh	8Bh
PIR1	PIE1
0Ch	8Ch
0Dh	8Dh
TMR1L	PCON
0Eh	8Eh
TMR1H	OSCCAL
0Fh	8Fh
T1CON	90h
10h	91h
11h	92h
12h	93h
13h	94h
14h	95h
15h	WPU
16h	IOC
17h	96h
18h	97h
CMCON	98h
19h	VRCON
1Ah	99h
ADRESH ⁽²⁾	EEDATA
1Bh	9Ah
ADCON0 ⁽²⁾	EEADR
1Ch	9Bh
1Dh	EECON1
ADRESL ⁽²⁾	9Ch
1Eh	EECON2 ⁽¹⁾
ANSEL ⁽²⁾	9Dh
1Fh	9Eh
20h	9Fh
General Purpose Registers 64 Bytes	A0h
5Fh	DFh
60h	E0h
7Fh	FFh

Bank 0 Bank 1

 Unimplemented data memory locations, read as '0'.

1: Not a physical register.

2: PIC12F675 only.

TABLE 2-1: SPECIAL FUNCTION REGISTERS SUMMARY

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD	Page
Bank 0											
00h	INDF ⁽¹⁾	Addressing this Location uses Contents of FSR to Address Data Memory								0000 0000	18,59
01h	TMR0	Timer0 Module's Register								xxxxx xxxx	27
02h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	17
03h	STATUS	IRP ⁽²⁾	RP1 ⁽²⁾	RP0	TO	PD	Z	DC	C	0001 1xxxx	11
04h	FSR	Indirect Data Memory Address Pointer								xxxxx xxxx	18
05h	GPIO	—	—	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0	--xxx xxxx	19
06h	—	Unimplemented								—	—
07h	—	Unimplemented								—	—
08h	—	Unimplemented								—	—
09h	—	Unimplemented								—	—
0Ah	PCLATH	—	—	—	Write Buffer for Upper 5 bits of Program Counter				---0 0000	17	
0Bh	INTCON	GIE	PEIE	TOIE	INTE	GPIE	TOIF	INTF	GPIF	0000 0000	13
0Ch	PIR1	EEIF	ADIF	—	—	CMIF	—	—	TMR1IF	00-- 0--0	15
0Dh	—	Unimplemented								—	—
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit Timer1								xxxxx xxxx	30
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit Timer1								xxxxx xxxx	30
10h	T1CON	—	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	—	TMR1CS	TMR1ON	-000 0000	32
11h	—	Unimplemented								—	—
12h	—	Unimplemented								—	—
13h	—	Unimplemented								—	—
14h	—	Unimplemented								—	—
15h	—	Unimplemented								—	—
16h	—	Unimplemented								—	—
17h	—	Unimplemented								—	—
18h	—	Unimplemented								—	—
19h	CMCON	—	COUT	—	CINV	CIS	CM2	CM1	CM0	-0-0 0000	35
1Ah	—	Unimplemented								—	—
1Bh	—	Unimplemented								—	—
1Ch	—	Unimplemented								—	—
1Dh	—	Unimplemented								—	—
1Eh	ADRESH ⁽³⁾	Most Significant 8 bits of the Left Shifted A/D Result or 2 bits of the Right Shifted Result								xxxxx xxxx	42
1Fh	ADCON0 ⁽³⁾	ADFM	VCFG	—	—	CHS1	CHS0	GO/DONE	ADON	00-- 0000	43,59

Legend: — = unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition,
shaded = unimplemented

Note 1: This is not a physical register.

2: These bits are reserved and should always be maintained as '0'.

3: PIC12F675 only.

PIC12F629/675

TABLE 2-1: SPECIAL FUNCTION REGISTERS SUMMARY (CONTINUED)

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD	Page
Bank 1											
80h	INDF ⁽¹⁾	Addressing this Location uses Contents of FSR to Address Data Memory								0000 0000	18,59
81h	OPTION_REG	GPPU	INTEGD	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	12,28
82h	PCL	Program Counter's (PC) Least Significant Byte								0000 0000	17
83h	STATUS	IRP ⁽²⁾	RP1 ⁽²⁾	RP0	TO	PD	Z	DC	C	0001 1xxx	11
84h	FSR	Indirect Data Memory Address Pointer								xxxx xxxx	18
85h	TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	--11 1111	19
86h	—	Unimplemented								—	—
87h	—	Unimplemented								—	—
88h	—	Unimplemented								—	—
89h	—	Unimplemented								—	—
8Ah	PCLATH	—	—	—	Write Buffer for Upper 5 bits of Program Counter					---0 0000	17
8Bh	INTCON	GIE	PEIE	TOIE	INTE	GPIE	TOIF	INTF	GPIF	0000 0000	13
8Ch	PIE1	EEIE	ADIE	—	—	CMIE	—	—	TMR1IE	00-- 0--0	14
8Dh	—	Unimplemented								—	—
8Eh	PCON	—	—	—	—	—	—	POR	BOD	---- --0x	16
8Fh	—	Unimplemented								—	—
90h	OSCCAL	CAL5	CAL4	CAL3	CAL2	CAL1	CAL0	—	—	1000 00--	16
91h	—	Unimplemented								—	—
92h	—	Unimplemented								—	—
93h	—	Unimplemented								—	—
94h	—	Unimplemented								—	—
95h	WPU	—	—	WPU5	WPU4	—	WPU2	WPU1	WPU0	--11 -111	20
96h	IOC	—	—	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0	--00 0000	21
97h	—	Unimplemented								—	—
98h	—	Unimplemented								—	—
99h	VRCON	VREN	—	VRR	—	VR3	VR2	VR1	VR0	0-0- 0000	40
9Ah	EEDATA	Data EEPROM Data Register								0000 0000	47
9Bh	EEADR	—	Data EEPROM Address Register								-000 0000
9Ch	EECON1	—	—	—	—	WRERR	WREN	WR	RD	---- x000	48
9Dh	EECON2 ⁽¹⁾	EEPROM Control Register 2								---- ----	48
9Eh	ADRESL ⁽³⁾	Least Significant 2 bits of the Left Shifted A/D Result of 8 bits or the Right Shifted Result								xxxx xxxx	42
9Fh	ANSEL ⁽³⁾	—	ADCS2	ADCS1	ADCS0	ANS3	ANS2	ANS1	ANS0	-000 1111	44,59

Legend: — = unimplemented locations read as '0', u = unchanged, x = unknown, q = value depends on condition,
shaded = unimplemented

Note 1: This is not a physical register.

2: These bits are reserved and should always be maintained as '0'.

3: PIC12F675 only.

2.2.2.1 STATUS Register

The STATUS register, shown in Register 2-1, contains:

- the arithmetic status of the ALU
- the RESET status
- the bank select bits for data memory (SRAM)

The STATUS register can be the destination for any instruction, like any other register. If the STATUS register is the destination for an instruction that affects the Z, DC or C bits, then the write to these three bits is disabled. These bits are set or cleared according to the device logic. Furthermore, the $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are not writable. Therefore, the result of an instruction with the STATUS register as destination may be different than intended.

For example, CLRF STATUS will clear the upper three bits and set the Z bit. This leaves the STATUS register as 000_u uuu (where u = unchanged).

It is recommended, therefore, that only BCF, BSF, SWAPF and MOVWF instructions are used to alter the STATUS register, because these instructions do not affect any STATUS bits. For other instructions not affecting any STATUS bits, see the "Instruction Set Summary".

Note 1: Bits IRP and RP1 (STATUS<7:6>) are not used by the PIC12F629/675 and should be maintained as clear. Use of these bits is not recommended, since this may affect upward compatibility with future products.

2: The C and DC bits operate as a Borrow and Digit Borrow out bit, respectively, in subtraction. See the SUBLW and SUBWF instructions for examples.

REGISTER 2-1: STATUS — STATUS REGISTER (ADDRESS: 03h OR 83h)

Reserved	Reserved	R/W-0	R-1	R-1	R/W-x	R/W-x	R/W-x
		IRP	RP1	RP0	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z
bit 7							bit 0

bit 7	IRP: This bit is reserved and should be maintained as '0'
bit 6	RP1: This bit is reserved and should be maintained as '0'
bit 5	RP0: Register Bank Select bit (used for direct addressing) 0 = Bank 0 (00h - 7Fh) 1 = Bank 1 (80h - FFh)
bit 4	TO: Time-out bit 1 = After power-up, CLRWD instruction, or SLEEP instruction 0 = A WDT time-out occurred
bit 3	PD: Power-down bit 1 = After power-up or by the CLRWD instruction 0 = By execution of the SLEEP instruction
bit 2	Z: Zero bit 1 = The result of an arithmetic or logic operation is zero 0 = The result of an arithmetic or logic operation is not zero
bit 1	DC: Digit carry/borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions) For borrow, the polarity is reversed. 1 = A carry-out from the 4th low order bit of the result occurred 0 = No carry-out from the 4th low order bit of the result
bit 0	C: Carry/borrow bit (ADDWF, ADDLW, SUBLW, SUBWF instructions) 1 = A carry-out from the Most Significant bit of the result occurred 0 = No carry-out from the Most Significant bit of the result occurred

Note: For borrow the polarity is reversed. A subtraction is executed by adding the two's complement of the second operand. For rotate (RRF, RLF) instructions, this bit is loaded with either the high or low order bit of the source register

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

PIC12F629/675

2.2.2.2 OPTION Register

The OPTION register is a readable and writable register, which contains various control bits to configure:

Note: To achieve a 1:1 prescaler assignment for TMR0, assign the prescaler to the WDT by setting PSA bit to '1' (OPTION<3>). See Section 4.4.

- TMR0/WDT prescaler
 - External GP2/INT interrupt
 - TMR0
 - Weak pull-ups on GPIO

REGISTER 2-2: OPTION_REG — OPTION REGISTER (ADDRESS: 81h)

bit 7	GPPU: GPIO Pull-up Enable bit 1 = GPIO pull-ups are disabled 0 = GPIO pull-ups are enabled by individual port latch values
bit 6	INTEDG: Interrupt Edge Select bit 1 = Interrupt on rising edge of GP2/INT pin 0 = Interrupt on falling edge of GP2/INT pin
bit 5	T0CS: TMR0 Clock Source Select bit 1 = Transition on GP2/T0CKI pin 0 = Internal instruction cycle clock (CLKOUT)
bit 4	T0SE: TMR0 Source Edge Select bit 1 = Increment on high-to-low transition on GP2/T0CKI pin 0 = Increment on low-to-high transition on GP2/T0CKI pin
bit 3	PSA: Prescaler Assignment bit 1 = Prescaler is assigned to the WDT 0 = Prescaler is assigned to the TIMER0 module
bit 2-0	PS2:PS0: Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

Legend:

R ≡ Readable bit

W ≡ Writable bit

$\text{U} \equiv \text{Unimplemented bit, read as '0'}$

- n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

$x \equiv$ Bit is unknown

2.2.2.3 INTCON Register

The INTCON register is a readable and writable register, which contains the various enable and flag bits for TMR0 register overflow, GPIO port change and external GP2/INT pin interrupts.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-3: INTCON — INTERRUPT CONTROL REGISTER (ADDRESS: 0Bh OR 8Bh)

| R/W-0 |
|-------|-------|-------|-------|-------|-------|-------|-------|
| GIE | PEIE | TOIE | INTE | GPIE | T0IF | INTF | GPIF |
| bit 7 | | | | | | | bit 0 |

bit 7	GIE: Global Interrupt Enable bit 1 = Enables all unmasked interrupts 0 = Disables all interrupts
bit 6	PEIE: Peripheral Interrupt Enable bit 1 = Enables all unmasked peripheral interrupts 0 = Disables all peripheral interrupts
bit 5	TOIE: TMR0 Overflow Interrupt Enable bit 1 = Enables the TMR0 interrupt 0 = Disables the TMR0 interrupt
bit 4	INTE: GP2/INT External Interrupt Enable bit 1 = Enables the GP2/INT external interrupt 0 = Disables the GP2/INT external interrupt
bit 3	GPIE: Port Change Interrupt Enable bit ⁽¹⁾ 1 = Enables the GPIO port change interrupt 0 = Disables the GPIO port change interrupt
bit 2	T0IF: TMR0 Overflow Interrupt Flag bit ⁽²⁾ 1 = TMR0 register has overflowed (must be cleared in software) 0 = TMR0 register did not overflow
bit 1	INTF: GP2/INT External Interrupt Flag bit 1 = The GP2/INT external interrupt occurred (must be cleared in software) 0 = The GP2/INT external interrupt did not occur
bit 0	GPIF: Port Change Interrupt Flag bit 1 = When at least one of the GP5:GP0 pins changed state (must be cleared in software) 0 = None of the GP5:GP0 pins have changed state

Note 1: IOC register must also be enabled to enable an interrupt-on-change.

2: T0IF bit is set when TIMER0 rolls over. TIMER0 is unchanged on RESET and should be initialized before clearing T0IF bit.

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

PIC12F629/675

2.2.2.4 PIE1 Register

The PIE1 register contains the interrupt enable bits, as shown in Register 2-4.

Note: Bit PEIE (INTCON<6>) must be set to enable any peripheral interrupt.

REGISTER 2-4: PIE1 — PERIPHERAL INTERRUPT ENABLE REGISTER 1 (ADDRESS: 8Ch)

R/W-0	R/W-0	U-0	U-0	R/W-0	U-0	U-0	R/W-0
EEIE	ADIE	—	—	CMIE	—	—	TMR1IE

bit 7

bit 0

bit 7 **EEIE:** EE Write Complete Interrupt Enable bit

1 = Enables the EE write complete interrupt

0 = Disables the EE write complete interrupt

bit 6 **ADIE:** A/D Converter Interrupt Enable bit (PIC12F675 only)

1 = Enables the A/D converter interrupt

0 = Disables the A/D converter interrupt

bit 5-4 **Unimplemented:** Read as '0'

bit 3 **CMIE:** Comparator Interrupt Enable bit

1 = Enables the comparator interrupt

0 = Disables the comparator interrupt

bit 2-1 **Unimplemented:** Read as '0'

bit 0 **TMR1IE:** TMR1 Overflow Interrupt Enable bit

1 = Enables the TMR1 overflow interrupt

0 = Disables the TMR1 overflow interrupt

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

- n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

2.2.2.5 PIR1 Register

The PIR1 register contains the interrupt flag bits, as shown in Register 2-5.

Note: Interrupt flag bits are set when an interrupt condition occurs, regardless of the state of its corresponding enable bit or the global enable bit, GIE (INTCON<7>). User software should ensure the appropriate interrupt flag bits are clear prior to enabling an interrupt.

REGISTER 2-5: PIR1 — PERIPHERAL INTERRUPT REGISTER 1 (ADDRESS: 0Ch)

R/W-0	R/W-0	U-0	U-0	R/W-0	U-0	U-0	R/W-0
EEIF	ADIF	—	—	CMIF	—	—	TMR1IF

bit 7

bit 0

- bit 7 **EEIF:** EEPROM Write Operation Interrupt Flag bit
1 = The write operation completed (must be cleared in software)
0 = The write operation has not completed or has not been started
- bit 6 **ADIF:** A/D Converter Interrupt Flag bit (PIC12F675 only)
1 = The A/D conversion is complete (must be cleared in software)
0 = The A/D conversion is not complete
- bit 5-4 **Unimplemented:** Read as '0'
- bit 3 **CMIF:** Comparator Interrupt Flag bit
1 = Comparator input has changed (must be cleared in software)
0 = Comparator input has not changed
- bit 2-1 **Unimplemented:** Read as '0'
- bit 0 **TMR1IF:** TMR1 Overflow Interrupt Flag bit
1 = TMR1 register overflowed (must be cleared in software)
0 = TMR1 register did not overflow

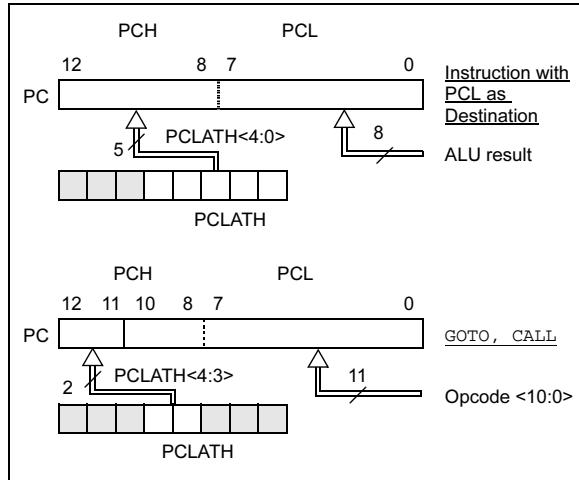
Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

2.3 PCL and PCLATH

The program counter (PC) is 13-bits wide. The low byte comes from the PCL register, which is a readable and writable register. The high byte ($PC<12:8>$) is not directly readable or writable and comes from PCLATH. On any RESET, the PC is cleared. Figure 2-3 shows the two situations for the loading of the PC. The upper example in Figure 2-3 shows how the PC is loaded on a write to PCL ($PCLATH<4:0> \rightarrow PCH$). The lower example in Figure 2-3 shows how the PC is loaded during a CALL or GOTO instruction ($PCLATH<4:3> \rightarrow PCH$).

FIGURE 2-3: LOADING OF PC IN DIFFERENT SITUATIONS



2.3.1 COMPUTED GOTO

A computed GOTO is accomplished by adding an offset to the program counter (ADDWF PCL). When performing a table read using a computed GOTO method, care should be exercised if the table location crosses a PCL memory boundary (each 256-byte block). Refer to the Application Note "Implementing a Table Read" (AN556).

2.3.2 STACK

The PIC12F629/675 family has an 8-level deep \times 13-bit wide hardware stack (see Figure 2-1). The stack space is not part of either program or data space and the stack pointer is not readable or writable. The PC is PUSHed onto the stack when a CALL instruction is executed, or an interrupt causes a branch. The stack is POPped in the event of a RETURN, RETLW or a RETFIE instruction execution. PCLATH is not affected by a PUSH or POP operation.

The stack operates as a circular buffer. This means that after the stack has been PUSHed eight times, the ninth push overwrites the value that was stored from the first push. The tenth push overwrites the second push (and so on).

- Note 1:** There are no STATUS bits to indicate stack overflow or stack underflow conditions.
- 2:** There are no instructions/mnemonics called PUSH or POP. These are actions that occur from the execution of the CALL, RETURN, RETLW and RETFIE instructions, or the vectoring to an interrupt address.

PIC12F629/675

2.4 Indirect Addressing, INDF and FSR Registers

The INDF register is not a physical register. Addressing the INDF register will cause indirect addressing.

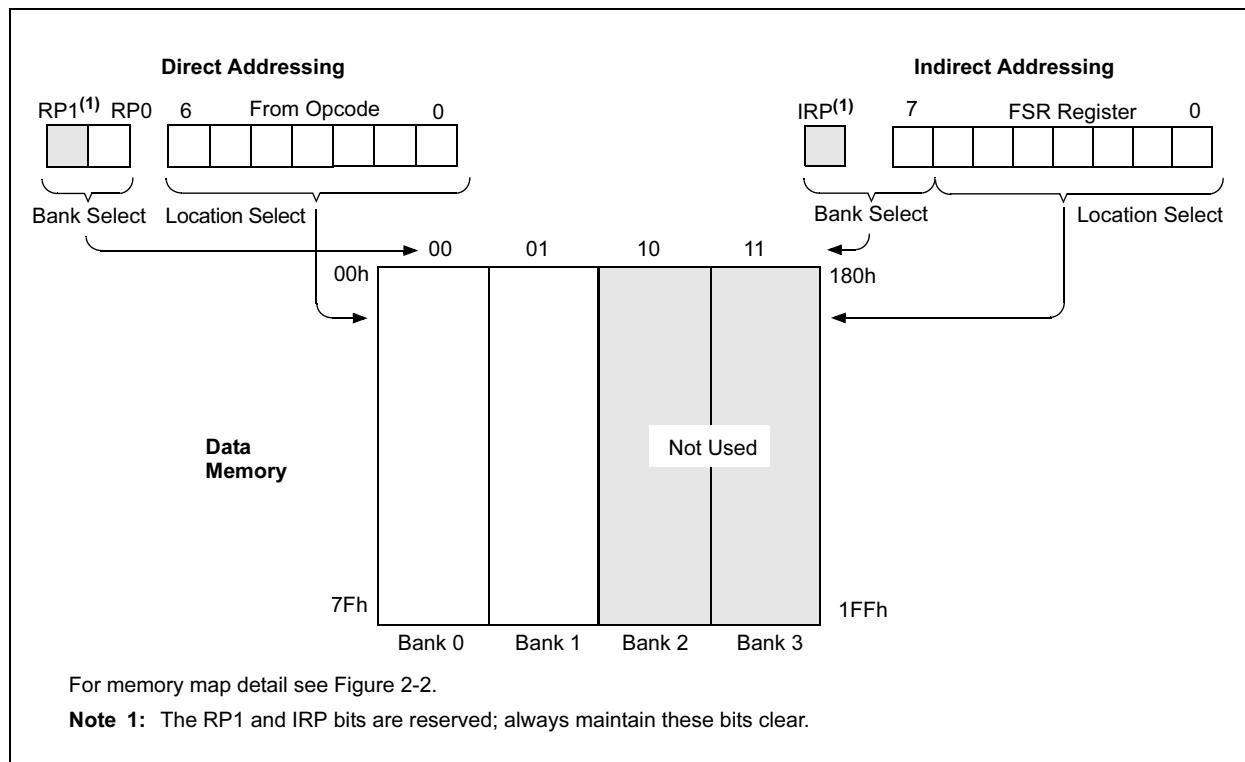
Indirect addressing is possible by using the INDF register. Any instruction using the INDF register actually accesses data pointed to by the File Select register (FSR). Reading INDF itself indirectly will produce 00h. Writing to the INDF register indirectly results in a no operation (although STATUS bits may be affected). An effective 9-bit address is obtained by concatenating the 8-bit FSR register and the IRP bit (STATUS<7>), as shown in Figure 2-4.

A simple program to clear RAM location 20h-2Fh using indirect addressing is shown in Example 2-1.

EXAMPLE 2-1: INDIRECT ADDRESSING

```
        movlw 0x20 ;initialize pointer
        movwf FSR   ;to RAM
NEXT    clrf INDF ;clear INDF register
        incf FSR   ;inc pointer
        btfss FSR, 4 ;all done?
        goto NEXT  ;no clear next
CONTINUE           ;yes continue
```

FIGURE 2-4: DIRECT/INDIRECT ADDRESSING PIC12F629/675



3.0 GPIO PORT

There are as many as six general purpose I/O pins available. Depending on which peripherals are enabled, some or all of the pins may not be available as general purpose I/O. In general, when a peripheral is enabled, the associated pin may not be used as a general purpose I/O pin.

Note: Additional information on I/O ports may be found in the PICmicro™ Mid-Range Reference Manual, (DS33023)

3.1 GPIO and the TRISIO Registers

GPIO is an 8-bit wide, bi-directional port. The corresponding data direction register is TRISIO. Setting a TRISIO bit (= 1) will make the corresponding GPIO pin an input (i.e., put the corresponding output driver in a Hi-impedance mode). Clearing a TRISIO bit (= 0) will make the corresponding GPIO pin an output (i.e., put the contents of the output latch on the selected pin). The exception is GP3, which is input only and its TRISIO bit will always read as '1'. Example 3-1 shows how to initialize GPIO.

Reading the GPIO register reads the status of the pins, whereas writing to it will write to the port latch. All write operations are read-modify-write operations. Therefore, a write to a port implies that the port pins are read, this value is modified, and then written to the port data latch. GP3 reads '0' when MCLREN = 1.

The TRISIO register controls the direction of the GP pins, even when they are being used as analog inputs. The user must ensure the bits in the TRISIO

register are maintained set when using them as analog inputs. I/O pins configured as analog inputs always read '0'.

Note: The ANSEL (9Fh) and CMCON (19h) registers (9Fh) must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'. The ANSEL register is defined for the PIC12F675.

EXAMPLE 3-1: INITIALIZING GPIO

```

bcf    STATUS,RP0      ;Bank 0
clrf   GPIO           ;Init GPIO
movlw  07h            ;Set GP<2:0> to
movwf  CMCON          ;digital IO
bsf    STATUS,RP0      ;Bank 1
clrf   ANSEL          ;Digital I/O
movlw  0Ch             ;Set GP<3:2> as inputs
movwf  TRISIO          ;and set GP<5:4,1:0>
                      ;as outputs

```

3.2 Additional Pin Functions

Every GPIO pin on the PIC12F629/675 has an interrupt-on-change option and every GPIO pin, except GP3, has a weak pull-up option. The next two sections describe these functions.

3.2.1 WEAK PULL-UP

Each of the GPIO pins, except GP3, has an individually configurable weak internal pull-up. Control bits WPUX enable or disable each pull-up. Refer to Register 3-3. Each weak pull-up is automatically turned off when the port pin is configured as an output. The pull-ups are disabled on a Power-on Reset by the GPPU bit (OPTION<7>).

REGISTER 3-1: GPIO — GPIO REGISTER (ADDRESS: 05h)

U-0	U-0	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x	R/W-x
—	—	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0

bit 7

bit 0

- bit 7-6: **Unimplemented:** Read as '0'
- bit 5-0: **GPIO<5:0>:** General Purpose I/O pin.
1 = Port pin is >VIH
0 = Port pin is <VIL

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared
		x = Bit is unknown

PIC12F629/675

REGISTER 3-2: TRISIO — GPIO TRISTATE REGISTER (ADDRESS: 85h)

bit 7-6:	Unimplemented: Read as '0'
bit 5-0:	TRISIO<5:0>: General Purpose I/O Tri-State Control bit 1 = GPIO pin configured as an input (tri-stated) 0 = GPIO pin configured as an output.
	Note: TRISIO<3> always reads 1.

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

REGISTER 3-3: WPU — WEAK PULL-UP REGISTER (ADDRESS: 95h)

bit 7-6	Unimplemented: Read as '0'
bit 5-4	WPU<5:4>: Weak Pull-up Register bit 1 = Pull-up enabled 0 = Pull-up disabled
bit 3	Unimplemented: Read as '0'
bit 2-0	WPU<2:0>: Weak Pull-up Register bit 1 = Pull-up enabled 0 = Pull-up disabled

Note 1: Global GPPU must be enabled for individual pull-ups to be enabled.
2: The weak pull-up device is automatically disabled if the pin is in Output mode (TRISIO = 0).

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

3.2.2 INTERRUPT-ON-CHANGE

Each of the GPIO pins is individually configurable as an interrupt-on-change pin. Control bits IOC enable or disable the interrupt function for each pin. Refer to Register 3-4. The interrupt-on-change is disabled on a Power-on Reset.

For enabled interrupt-on-change pins, the values are compared with the old value latched on the last read of GPIO. The 'mismatch' outputs of the last read are OR'd together to set, the GP Port Change Interrupt flag bit (GPIF) in the INTCON register.

This interrupt can wake the device from SLEEP. The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

- Any read or write of GPIO. This will end the mismatch condition.
- Clear the flag bit GPIF.

A mismatch condition will continue to set flag bit GPIF. Reading GPIO will end the mismatch condition and allow flag bit GPIF to be cleared.

Note: If a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the GPIF interrupt flag may not get set.

REGISTER 3-4: IOC — INTERRUPT-ON-CHANGE GPIO REGISTER (ADDRESS: 96h)

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0

bit 7

bit 0

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **IOC<5:0>:** Interrupt-on-Change GPIO Control bit

1 = Interrupt-on-change enabled

0 = Interrupt-on-change disabled

Note 1: Global interrupt enable (GIE) must be enabled for individual interrupts to be recognized.

Legend:

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

- n = Value at POR

'1' = Bit is set

'0' = Bit is cleared

x = Bit is unknown

PIC12F629/675

3.3 Pin Descriptions and Diagrams

Each GPIO pin is multiplexed with other functions. The pins and their combined functions are briefly described here. For specific information about individual functions such as the comparator or the A/D, refer to the appropriate section in this Data Sheet.

3.3.1 GP0/AN0/CIN+

Figure 3-1 shows the diagram for this pin. The GP0 pin is configurable to function as one of the following:

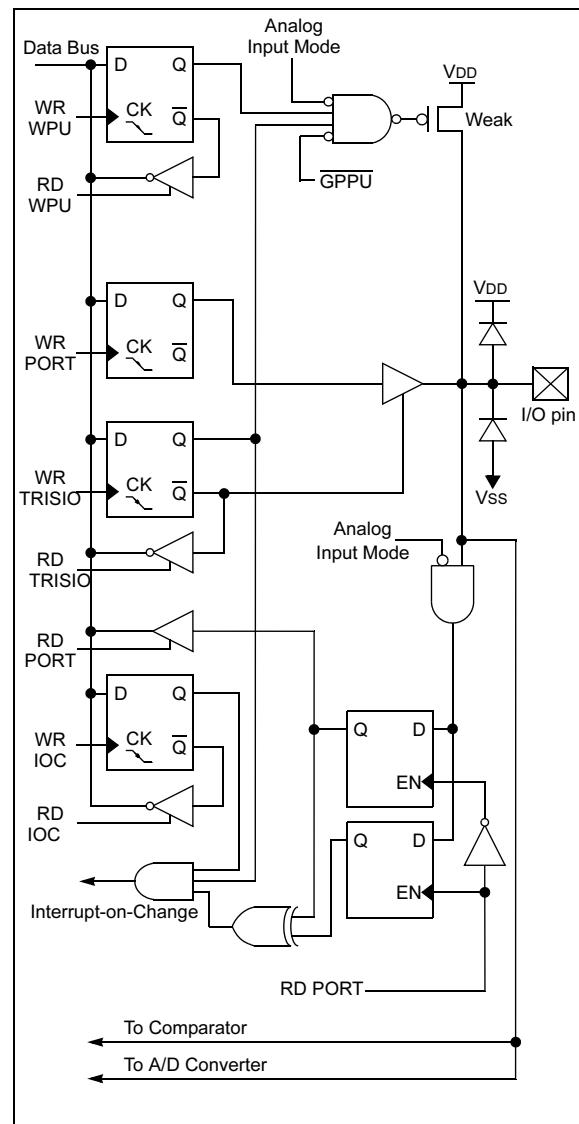
- a general purpose I/O
 - an analog input for the A/D (PIC12F675 only)
 - an analog input to the comparator

3.3.2 GP1/AN1/CIN-/VREF

Figure 3-1 shows the diagram for this pin. The GP1 pin is configurable to function as one of the following:

- as a general purpose I/O
 - an analog input for the A/D (PIC12F675 only)
 - an analog input to the comparator
 - a voltage reference input for the A/D (PIC12F675 only)

FIGURE 3-1: BLOCK DIAGRAM OF GP0 AND GP1 PINS

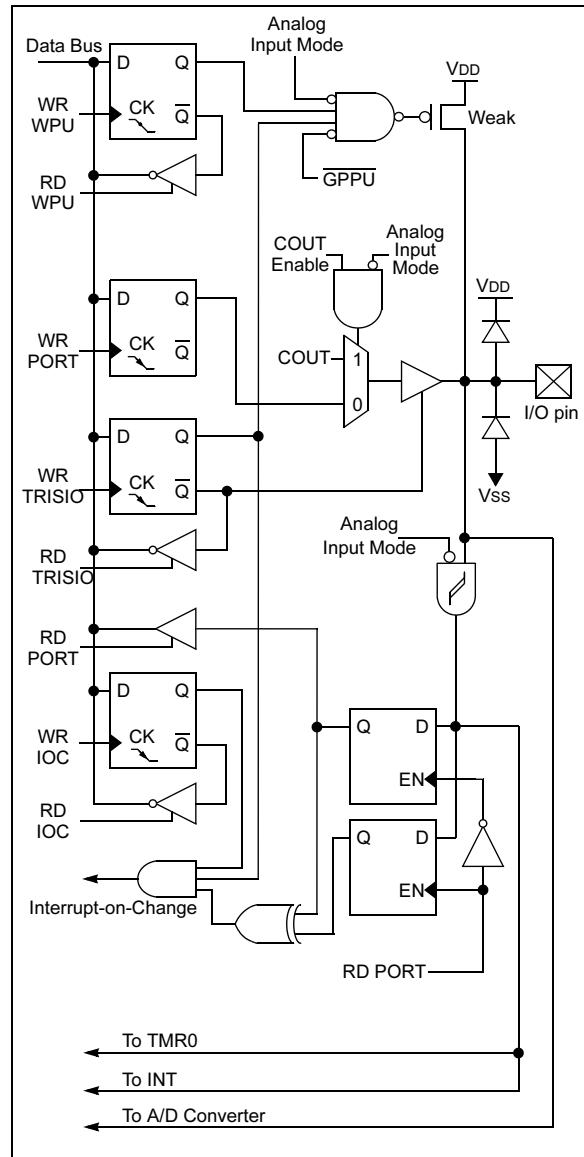


3.3.3 GP2/AN2/T0CKI/INT/COUT

Figure 3-2 shows the diagram for this pin. The GP2 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the A/D (PIC12F675 only)
- the clock input for TMR0
- an external edge triggered interrupt
- a digital output from the comparator

FIGURE 3-2: BLOCK DIAGRAM OF GP2

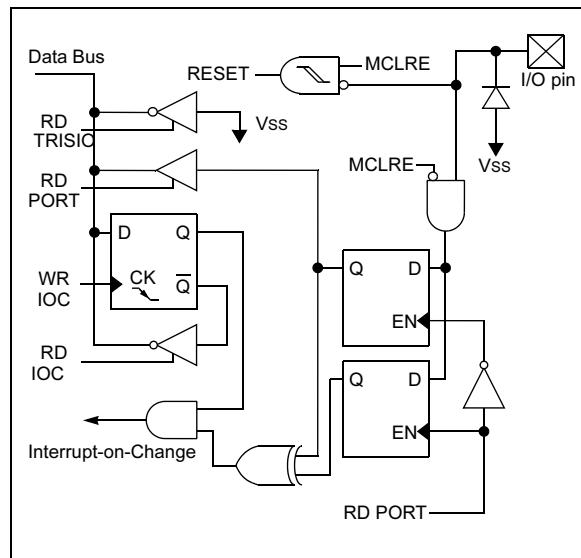


3.3.4 GP3/MCLR/VPP

Figure 3-3 shows the diagram for this pin. The GP3 pin is configurable to function as one of the following:

- a general purpose input
- as Master Clear Reset

FIGURE 3-3: BLOCK DIAGRAM OF GP3



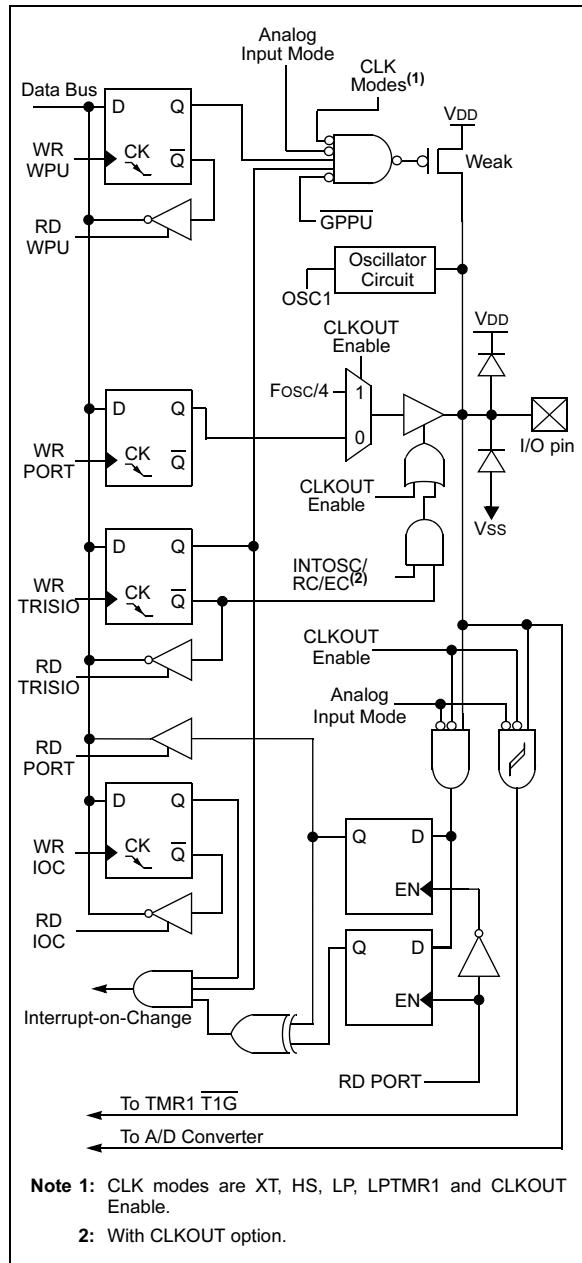
PIC12F629/675

3.3.5 GP4/AN3/T1G/OSC2/CLKOUT

Figure 3-4 shows the diagram for this pin. The GP4 pin is configurable to function as one of the following:

- a general purpose I/O
- an analog input for the A/D (PIC12F675 only)
- a TMR1 gate input
- a crystal/resonator connection
- a clock output

FIGURE 3-4: BLOCK DIAGRAM OF GP4



3.3.6 GP5/T1CKI/OSC1/CLKIN

Figure 3-5 shows the diagram for this pin. The GP5 pin is configurable to function as one of the following:

- a general purpose I/O
- a TMR1 clock input
- a crystal/resonator connection
- a clock input

FIGURE 3-5: BLOCK DIAGRAM OF GP5

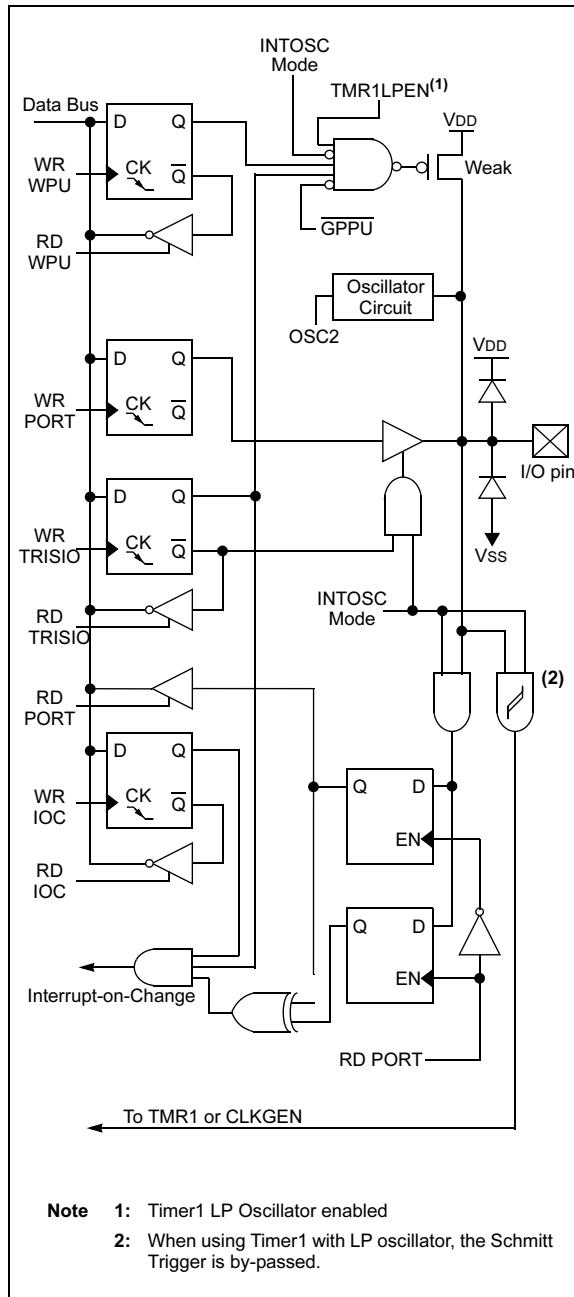


TABLE 3-1: SUMMARY OF REGISTERS ASSOCIATED WITH GPIO

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOD	Value on all other RESETS
05h	GPIO	—	—	GP5	GP4	GP3	GP2	GP1	GP0	---xx xxxx	--uu uuuu
0Bh/8Bh	INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	0000 000u
19h	CMCON	—	COUT	—	CINV	CIS	CM2	CM1	CM0	-0-0 0000	-0-0 0000
81h	OPTION_REG	GPPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
85h	TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	--11 1111	--11 1111
95h	WPU	—	—	WPU5	WPU4	—	WPU2	WPU1	WPU0	--11 -111	--11 -111
96h	IOC	—	—	IOC5	IOC4	IOC3	IOC2	IOC1	IOC0	--00 0000	--00 0000
9Fh	ANSEL	—	ADCS2	ADCS1	ADCS0	ANS3	ANS2	ANS1	ANS0	-000 1111	-000 1111

Legend: x = unknown, u = unchanged, - = unimplemented locations read as '0'. Shaded cells are not used by GPIO.

PIC12F629/675

NOTES:

4.0 TIMER0 MODULE

The Timer0 module timer/counter has the following features:

- 8-bit timer/counter
- Readable and writable
- 8-bit software programmable prescaler
- Internal or external clock select
- Interrupt on overflow from FFh to 00h
- Edge select for external clock

Figure 4-1 is a block diagram of the Timer0 module and the prescaler shared with the WDT.

Note: Additional information on the Timer0 module is available in the PICmicro™ Mid-Range Reference Manual, (DS33023).

4.1 Timer0 Operation

Timer mode is selected by clearing the T0CS bit (OPTION_REG<5>). In Timer mode, the Timer0 module will increment every instruction cycle (without prescaler). If TMR0 is written, the increment is inhibited for the following two instruction cycles. The user can work around this by writing an adjusted value to the TMR0 register.

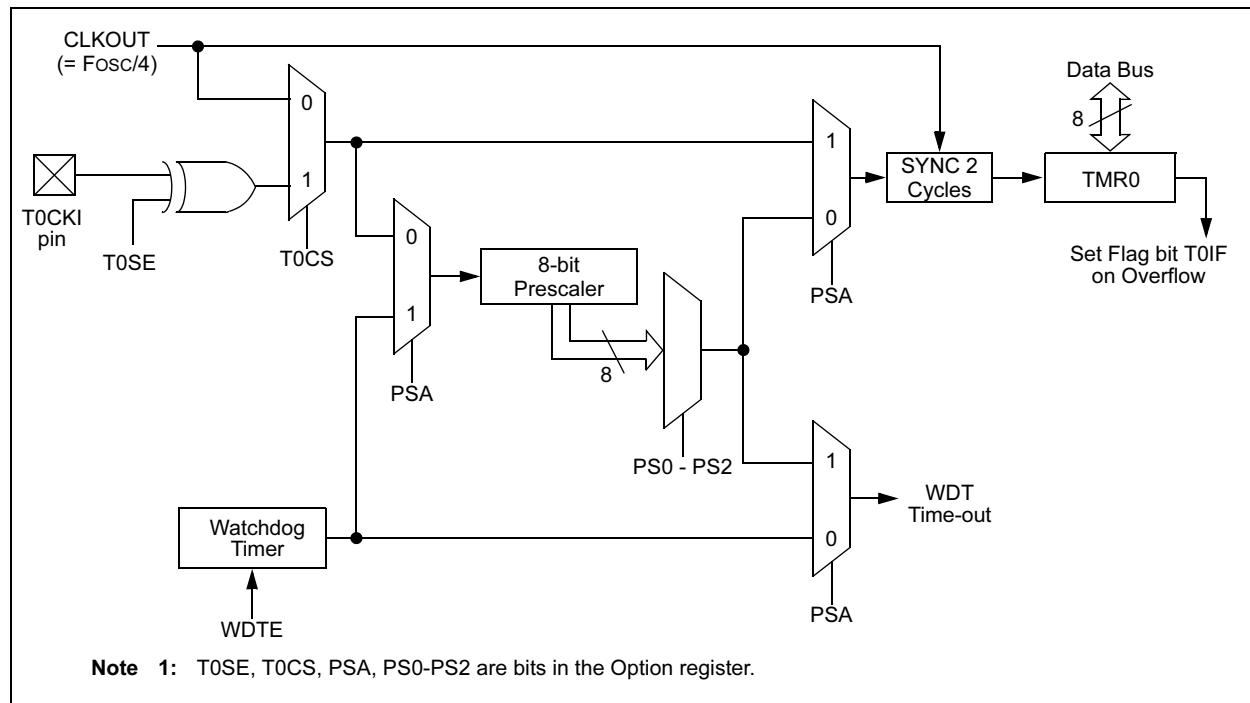
Counter mode is selected by setting the T0CS bit (OPTION_REG<5>). In this mode, the Timer0 module will increment either on every rising or falling edge of pin GP2/T0CKI. The incrementing edge is determined by the source edge (T0SE) control bit (OPTION_REG<4>). Clearing the T0SE bit selects the rising edge.

Note: Counter mode has specific external clock requirements. Additional information on these requirements is available in the PICmicro™ Mid-Range Reference Manual, (DS33023).

4.2 Timer0 Interrupt

A Timer0 interrupt is generated when the TMR0 register timer/counter overflows from FFh to 00h. This overflow sets the T0IF bit. The interrupt can be masked by clearing the T0IE bit (INTCON<5>). The T0IF bit (INTCON<2>) must be cleared in software by the Timer0 module Interrupt Service Routine before re-enabling this interrupt. The Timer0 interrupt cannot wake the processor from SLEEP since the timer is shut-off during SLEEP.

FIGURE 4-1: BLOCK DIAGRAM OF THE TIMER0/WDT PRESCALER



PIC12F629/675

4.3 Using Timer0 with an External Clock

When no prescaler is used, the external clock input is the same as the prescaler output. The synchronization of T0CKI, with the internal phase clocks, is accomplished by sampling the prescaler output on the Q2 and Q4 cycles of the internal phase clocks. Therefore, it is necessary for T0CKI to be high for at least 2Tosc (and

a small RC delay of 20 ns) and low for at least 2Tosc (and a small RC delay of 20 ns). Refer to the electrical specification of the desired device.

Note: The ANSEL (9Fh) and CMCON (19h) registers must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'. The ANSEL register is defined for the PIC12F675.

REGISTER 4-1: OPTION_REG — OPTION REGISTER (ADDRESS: 81h)

bit 7	GPPU: GPIO Pull-up Enable bit 1 = GPIO pull-ups are disabled 0 = GPIO pull-ups are enabled by individual port latch values
bit 6	INTEDG: Interrupt Edge Select bit 1 = Interrupt on rising edge of GP2/INT pin 0 = Interrupt on falling edge of GP2/INT pin
bit 5	T0CS: TMR0 Clock Source Select bit 1 = Transition on GP2/T0CKI pin 0 = Internal instruction cycle clock (CLKOUT)
bit 4	T0SE: TMR0 Source Edge Select bit 1 = Increment on high-to-low transition on GP2/T0CKI pin 0 = Increment on low-to-high transition on GP2/T0CKI pin
bit 3	PSA: Prescaler Assignment bit 1 = Prescaler is assigned to the WDT 0 = Prescaler is assigned to the TIMER0 module
bit 2-0	PS2:PS0: Prescaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

Legend:

R = Readable bit

- n = Value at POR

W = Writable bit

U = Unimplemented bit, read as '0'

'1' = Bit is set

'0' = Bit is cleared x = Bit is unknown

4.4 Prescaler

An 8-bit counter is available as a prescaler for the Timer0 module, or as a postscaler for the Watchdog Timer. For simplicity, this counter will be referred to as "prescaler" throughout this Data Sheet. The prescaler assignment is controlled in software by the control bit PSA (OPTION_REG<3>). Clearing the PSA bit will assign the prescaler to Timer0. Prescale values are selectable via the PS2:PS0 bits (OPTION_REG<2:0>).

The prescaler is not readable or writable. When assigned to the Timer0 module, all instructions writing to the TMR0 register (e.g., CLRF 1, MOVWF 1, BSF 1, etc...) will clear the prescaler. When assigned to WDT, a CLRWDT instruction will clear the prescaler along with the Watchdog Timer.

4.4.1 SWITCHING PRESCALER ASSIGNMENT

The prescaler assignment is fully under software control (i.e., it can be changed "on the fly" during program execution). To avoid an unintended device RESET, the following instruction sequence (Example 4-1) must be executed when changing the prescaler assignment from Timer0 to WDT.

EXAMPLE 4-1: CHANGING PRESCALER (TIMER0→WDT)

```

bcf STATUS, RP0 ;Bank 0
clrwdt          ;Clear WDT
clrf  TMR0      ;Clear TMR0 and
                 ; prescaler
bsf  STATUS, RP0 ;Bank 1

movlw b'00101111' ;Required if desired
movwf OPTION_REG ; PS2:PS0 is
clrwdt          ; 000 or 001
                 ;
movlw b'00101xxx' ;Set postscaler to
movwf OPTION_REG ; desired WDT rate
bcf  STATUS, RP0 ;Bank 0

```

To change prescaler from the WDT to the TMR0 module, use the sequence shown in Example 4-2. This precaution must be taken even if the WDT is disabled.

EXAMPLE 4-2: CHANGING PRESCALER (WDT→TIMER0)

```

clrwdt          ;Clear WDT and
                 ; postscaler
bsf  STATUS, RP0 ;Bank 1

movlw b'xxxx0xxx' ;Select TMR0,
                 ; prescale, and
                 ; clock source
movwf OPTION_REG ;
bcf  STATUS, RP0 ;Bank 0

```

TABLE 4-1: REGISTERS ASSOCIATED WITH TIMER0

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD	Value on all other RESETS
01h	TMR0	Timer0 Module Register							xxxx xxxx	uuuu uuuu	
0Bh/8Bh	INTCON	GIE	PEIE	TOIE	INTE	GPIE	TOIF	INTF	GPIF	0000 0000	0000 000u
81h	OPTION_REG	GPPU	INTEDG	TOCS	TOSE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
85h	TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	--11 1111	--11 1111

Legend: — = Unimplemented locations, read as '0', u = unchanged, x = unknown.

Shaded cells are not used by the Timer0 module.

PIC12F629/675

5.0 TIMER1 MODULE WITH GATE CONTROL

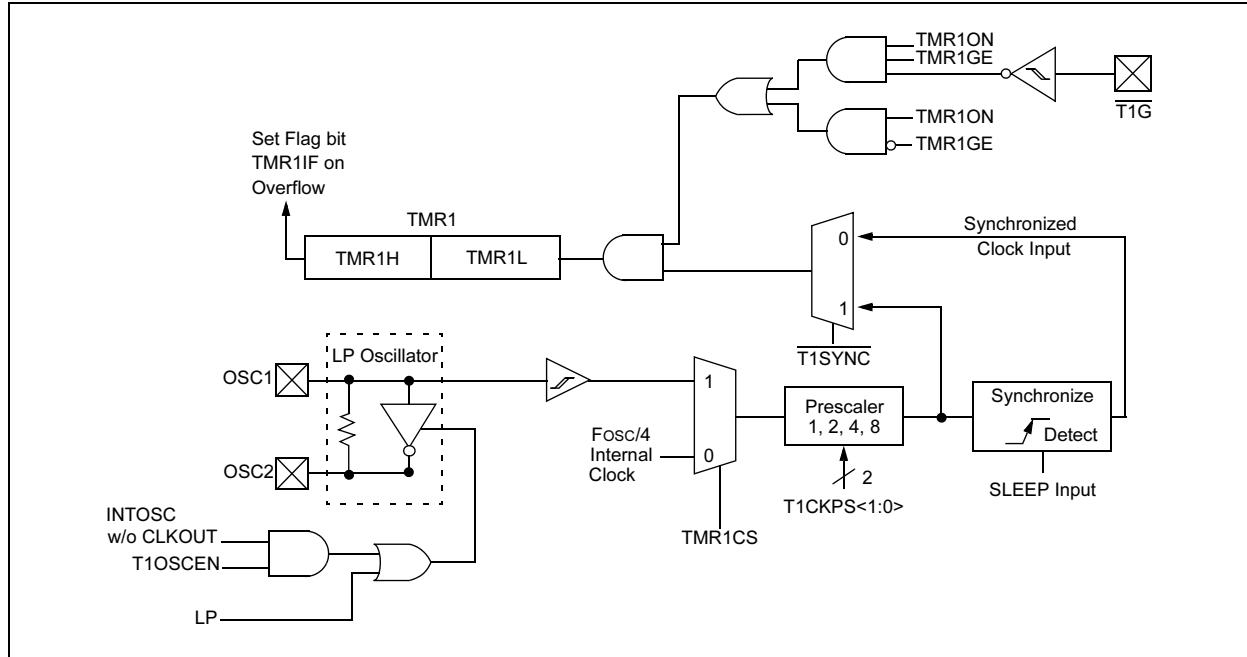
The PIC12F629/675 devices have a 16-bit timer. Figure 5-1 shows the basic block diagram of the Timer1 module. Timer1 has the following features:

- 16-bit timer/counter (TMR1H:TMR1L)
- Readable and writable
- Internal or external clock selection
- Synchronous or asynchronous operation
- Interrupt on overflow from FFFFh to 0000h
- Wake-up upon overflow (Asynchronous mode)
- Optional external enable input ($\overline{T1G}$)
- Optional LP oscillator

The Timer1 Control register (T1CON), shown in Register 5-1, is used to enable/disable Timer1 and select the various features of the Timer1 module.

Note: Additional information on timer modules is available in the PICmicro™ Mid-Range Reference Manual, (DS33023).

FIGURE 5-1: TIMER1 BLOCK DIAGRAM



5.1 Timer1 Modes of Operation

Timer1 can operate in one of three modes:

- 16-bit timer with prescaler
- 16-bit synchronous counter
- 16-bit asynchronous counter

In Timer mode, Timer1 is incremented on every instruction cycle. In Counter mode, Timer1 is incremented on the rising edge of the external clock input T1CKI. In addition, the Counter mode clock can be synchronized to the microcontroller system clock or run asynchronously.

In Counter and Timer modules, the counter/timer clock can be gated by the T1G input.

If an external clock oscillator is needed (and the microcontroller is using the INTOSC w/o CLKOUT), Timer1 can use the LP oscillator as a clock source.

Note: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge.

5.2 Timer1 Interrupt

The Timer1 register pair (TMR1H:TMR1L) increments to FFFFh and rolls over to 0000h. When Timer1 rolls over, the Timer1 interrupt flag bit (PIR1<0>) is set. To enable the interrupt on rollover, you must set these bits:

- Timer1 interrupt Enable bit (PIE1<0>)
- PEIE bit (INTCON<6>)
- GIE bit (INTCON<7>).

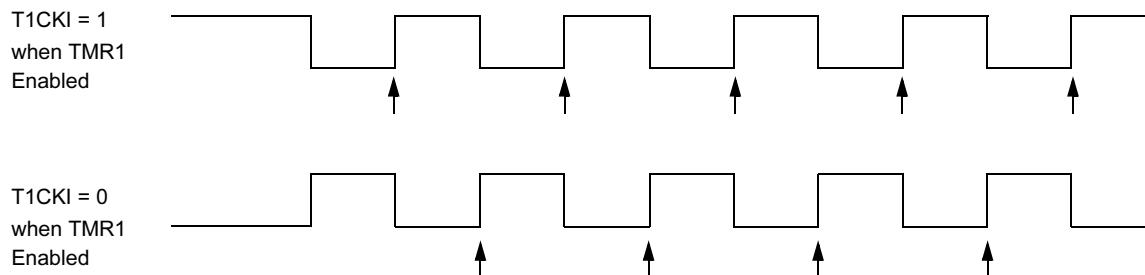
The interrupt is cleared by clearing the TMR1IF in the Interrupt Service Routine.

Note: The TMR1H:TTMR1L register pair and the TMR1IF bit should be cleared before enabling interrupts.

5.3 Timer1 Prescaler

Timer1 has four prescaler options allowing 1, 2, 4, or 8 divisions of the clock input. The T1CKPS bits (T1CON<5:4>) control the prescale counter. The prescale counter is not directly readable or writable; however, the prescaler counter is cleared upon a write to TMR1H or TMR1L.

FIGURE 5-2: TIMER1 INCREMENTING EDGE



Note 1: Arrows indicate counter increments.

Note 2: In Counter mode, a falling edge must be registered by the counter prior to the first incrementing rising edge of the clock.

PIC12F629/675

REGISTER 5-1: T1CON — TIMER1 CONTROL REGISTER (ADDRESS: 10h)

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	<u>T1SYNC</u>	TMR1CS	TMR1ON	bit 0

- | | |
|---------|---|
| bit 7 | Unimplemented: Read as '0' |
| bit 6 | TMR1GE: Timer1 Gate Enable bit
<u>If TMR1ON = 0:</u>
This bit is ignored
<u>If TMR1ON = 1:</u>
1 = Timer1 is on if T1G pin is low
0 = Timer1 is on |
| bit 5-4 | T1CKPS1:T1CKPS0: Timer1 Input Clock Prescale Select bits
11 = 1:8 Prescale Value
10 = 1:4 Prescale Value
01 = 1:2 Prescale Value
00 = 1:1 Prescale Value |
| bit 3 | T1OSCEN: LP Oscillator Enable Control bit
<u>If INTOSC without CLKOUT oscillator is active:</u>
1 = LP oscillator is enabled for Timer1 clock
0 = LP oscillator is off
<u>Else:</u>
This bit is ignored |
| bit 2 | T1SYNC: Timer1 External Clock Input Synchronization Control bit
<u>TMR1CS = 1:</u>
1 = Do not synchronize external clock input
0 = Synchronize external clock input
<u>TMR1CS = 0:</u>
This bit is ignored. Timer1 uses the internal clock. |
| bit 1 | TMR1CS: Timer1 Clock Source Select bit
1 = External clock from T1OSO/T1CKI pin (on the rising edge)
0 = Internal clock (Fosc/4) |
| bit 0 | TMR1ON: Timer1 On bit
1 = Enables Timer1
0 = Stops Timer1 |

Legend:

R = Readable bit

- n = Value at PQR

W = Writable bit

U = Unimplemented bit, read as '0'

'1' = Bit is set

'0' = Bit is cleared x = Bit is unknown

5.4 Timer1 Operation in Asynchronous Counter Mode

If control bit T1SYNC (T1CON<2>) is set, the external clock input is not synchronized. The timer continues to increment asynchronous to the internal phase clocks. The timer will continue to run during SLEEP and can generate an interrupt on overflow, which will wake-up the processor. However, special precautions in software are needed to read/write the timer (Section 5.4.1).

Note: The ANSEL (9Fh) and CMCON (19h) registers must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'. The ANSEL register is defined for the PIC12F675.

5.4.1 READING AND WRITING TIMER1 IN ASYNCHRONOUS COUNTER MODE

Reading TMR1H or TMR1L, while the timer is running from an external asynchronous clock, will ensure a valid read (taken care of in hardware). However, the user should keep in mind that reading the 16-bit timer in two 8-bit values itself, poses certain problems, since the timer may overflow between the reads.

For writes, it is recommended that the user simply stop the timer and write the desired values. A write contention may occur by writing to the timer registers, while the register is incrementing. This may produce an unpredictable value in the timer register.

Reading the 16-bit value requires some care. Examples 12-2 and 12-3 in the PICmicro™ Mid-Range MCU Family Reference Manual (DS33023) show how to read and write Timer1 when it is running in Asynchronous mode.

5.5 Timer1 Oscillator

A crystal oscillator circuit is built-in between pins OSC1 (input) and OSC2 (amplifier output). It is enabled by setting control bit T1OSCEN (T1CON<3>). The oscillator is a low power oscillator rated up to 37 kHz. It will continue to run during SLEEP. It is primarily intended for a 32 kHz crystal. Table 9-2 shows the capacitor selection for the Timer1 oscillator.

The Timer1 oscillator is shared with the system LP oscillator. Thus, Timer1 can use this mode only when the system clock is derived from the internal oscillator. As with the system LP oscillator, the user must provide a software time delay to ensure proper oscillator start-up

While enabled, TRISIO4 and TRISIO5 are set. GP4 and GP5 read '0' and TRISIO4 and TRISIO5 are read '1'.

Note: The oscillator requires a start-up and stabilization time before use. Thus, T1OSCEN should be set and a suitable delay observed prior to enabling Timer1.

5.6 Timer1 Operation During SLEEP

Timer1 can only operate during SLEEP when setup in Asynchronous Counter mode. In this mode, an external crystal or clock source can be used to increment the counter. To setup the timer to wake the device:

- Timer1 must be on (T1CON<0>)
- TMR1IE bit (PIE1<0>) must be set
- PEIE bit (INTCON<6>) must be set

The device will wake-up on an overflow. If the GIE bit (INTCON<7>) is set, the device will wake-up and jump to the Interrupt Service Routine on an overflow.

TABLE 5-1: REGISTERS ASSOCIATED WITH TIMER1 AS A TIMER/COUNTER

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD	Value on all other RESETS
0Bh/8Bh	INTCON	GIE	PEIE	T0IE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	0000 000 <u></u>
0Ch	PIR1	EEIF	ADIF	—	—	CMIF	—	—	TMR1IF	00-- 0--0	00-- 0--0
0Eh	TMR1L	Holding Register for the Least Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
0Fh	TMR1H	Holding Register for the Most Significant Byte of the 16-bit TMR1 Register								xxxx xxxx	uuuu uuuu
10h	T1CON	—	TMR1GE	T1CKPS1	T1CKPS0	T1OSCEN	T1SYNC	TMR1CS	TMR1ON	-000 0000	-uuu uuuu
8Ch	PIE1	EEIE	ADIE	—	—	CMIE	—	—	TMR1IE	00-- 0--0	00-- 0--0

Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the Timer1 module.

PIC12F629/675

NOTES:

6.0 COMPARATOR MODULE

The PIC12F629/675 devices have one analog comparator. The inputs to the comparator are multiplexed with the GP0 and GP1 pins. There is an on-chip Comparator Voltage Reference that can also

be applied to an input of the comparator. In addition, GP2 can be configured as the comparator output. The Comparator Control Register (CMCON), shown in Register 6-1, contains the bits to control the comparator.

REGISTER 6-1: CMCON — COMPARATOR CONTROL REGISTER (ADDRESS: 19h)

- | | |
|---------|--|
| bit 7 | Unimplemented: Read as '0' |
| bit 6 | COUT: Comparator Output bit
<u>When CINV = 0:</u>
1 = $V_{IN+} > V_{IN-}$
0 = $V_{IN+} < V_{IN-}$
<u>When CINV = 1:</u>
1 = $V_{IN+} < V_{IN-}$
0 = $V_{IN+} > V_{IN-}$ |
| bit 5 | Unimplemented: Read as '0' |
| bit 4 | CINV: Comparator Output Inversion bit
1 = Output inverted
0 = Output not inverted |
| bit 3 | CIS: Comparator Input Switch bit
<u>When CM2:CM0 = 110 or 101:</u>
1 = V_{IN-} connects to C_{IN+}
0 = V_{IN-} connects to C_{IN-} |
| bit 2-0 | CM2:CM0: Comparator Mode bits
Figure 6-2 shows the Comparator modes and CM2:CM0 bit settings |

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

PIC12F629/675

6.1 Comparator Operation

A single comparator is shown in Figure 6-1, along with the relationship between the analog input levels and the digital output. When the analog input at V_{IN+} is less than the analog input V_{IN-} , the output of the comparator is a digital low level. When the analog input at V_{IN+} is greater than the analog input V_{IN-} , the output of the comparator is a digital high level. The shaded areas of the output of the comparator in Figure 6-1 represent the uncertainty due to input offsets and response time.

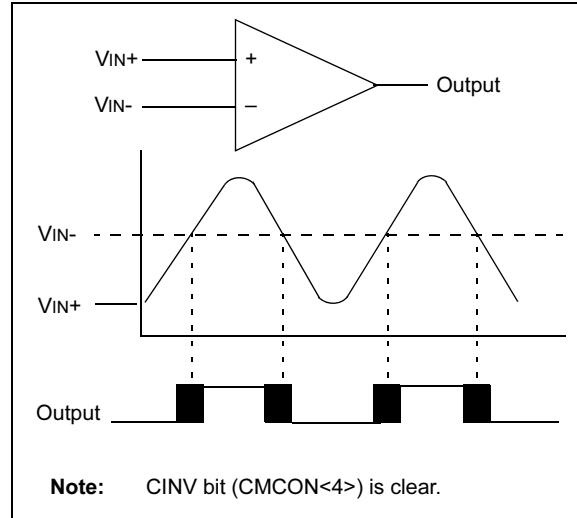
Note: To use $CIN+$ and $CIN-$ pins as analog inputs, the appropriate bits must be programmed in the CMCON (19h) register.

The polarity of the comparator output can be inverted by setting the $CINV$ bit (CMCON<4>). Clearing $CINV$ results in a non-inverted output. A complete table showing the output state versus input conditions and the polarity bit is shown in Table 6-1.

TABLE 6-1: OUTPUT STATE VS. INPUT CONDITIONS

Input Conditions	$CINV$	$COUT$
$V_{IN-} > V_{IN+}$	0	0
$V_{IN-} < V_{IN+}$	0	1
$V_{IN-} > V_{IN+}$	1	1
$V_{IN-} < V_{IN+}$	1	0

FIGURE 6-1: SINGLE COMPARATOR



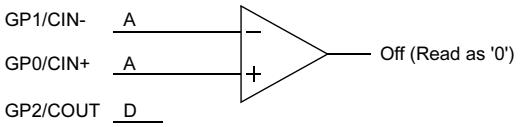
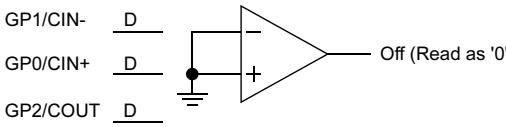
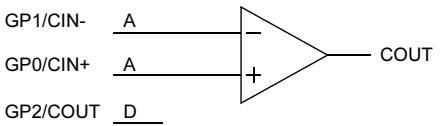
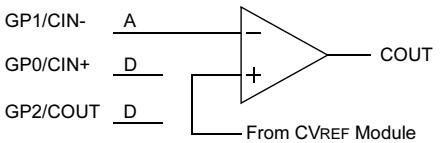
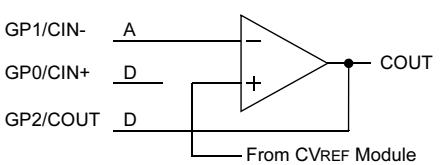
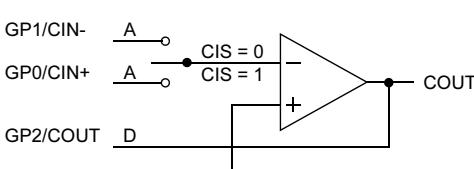
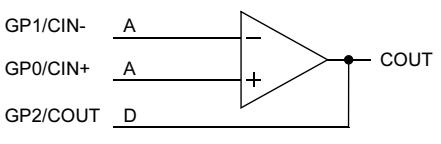
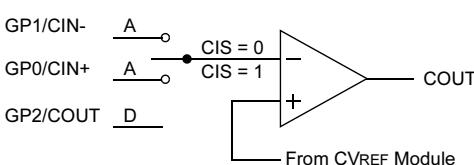
6.2 Comparator Configuration

There are eight modes of operation for the comparator. The CMCON register, shown in Register 6-1, is used to select the mode. Figure 6-2 shows the eight possible modes. The TRISIO register controls the data direction of the comparator pins for each mode. If the

Comparator mode is changed, the comparator output level may not be valid for a specified period of time. Refer to the specifications in Section 12.0.

Note: Comparator interrupts should be disabled during a Comparator mode change. Otherwise, a false interrupt may occur.

FIGURE 6-2: COMPARATOR I/O OPERATING MODES

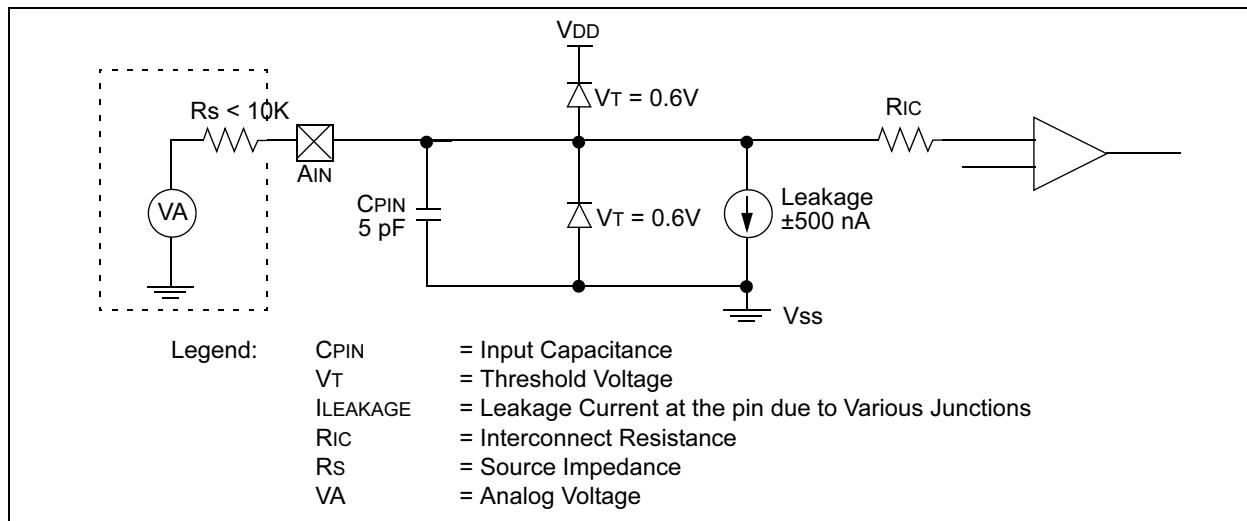
<p>Comparator Reset (POR Default Value - low power) CM2:CM0 = 000</p> 	<p>Comparator Off (Lowest power) CM2:CM0 = 111</p> 
<p>Comparator without Output CM2:CM0 = 010</p> 	<p>Comparator w/o Output and with Internal Reference CM2:CM0 = 100</p> 
<p>Comparator with Output and Internal Reference CM2:CM0 = 011</p> 	<p>Multiplexed Input with Internal Reference and Output CM2:CM0 = 101</p> 
<p>Comparator with Output CM2:CM0 = 001</p> 	<p>Multiplexed Input with Internal Reference CM2:CM0 = 110</p> 
<p>A = Analog Input, ports always reads '0' D = Digital Input CIS = Comparator Input Switch (CMCON<3>)</p>	

6.3 Analog Input Connection Considerations

A simplified circuit for an analog input is shown in Figure 6-3. Since the analog pins are connected to a digital output, they have reverse biased diodes to VDD and Vss. The analog input, therefore, must be between Vss and VDD. If the input voltage deviates from this

range by more than 0.6V in either direction, one of the diodes is forward biased and a latchup may occur. A maximum source impedance of $10\text{ k}\Omega$ is recommended for the analog sources. Any external component connected to an analog input pin, such as a capacitor or a Zener diode, should have very little leakage current.

FIGURE 6-3: ANALOG INPUT MODE



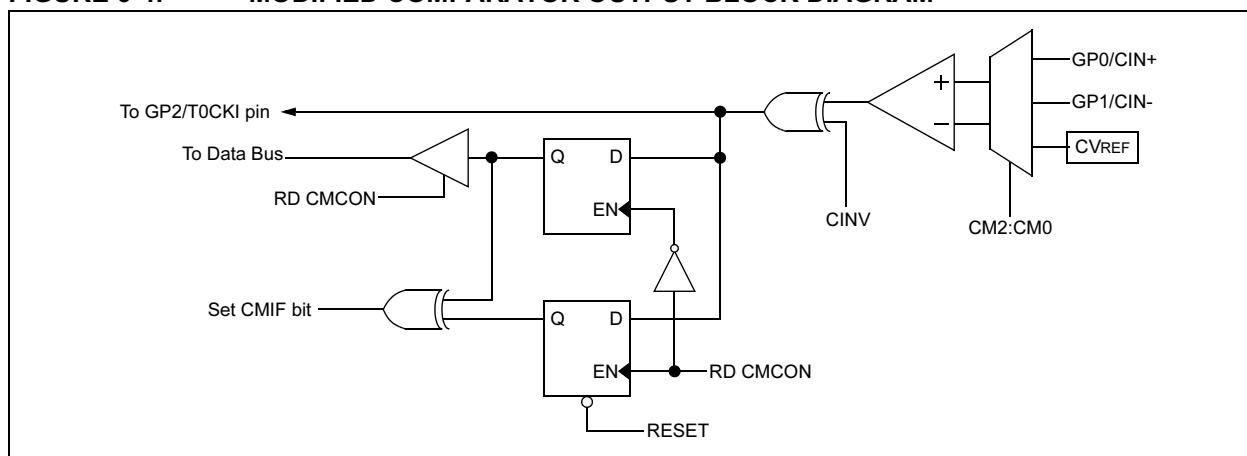
6.4 Comparator Output

The comparator output, COUT, is read through the CMCON register. This bit is read only. The comparator output may also be directly output to the GP2 pin in three of the eight possible modes, as shown in Figure 6-2. When in one of these modes, the output on GP2 is asynchronous to the internal clock. Figure 6-4 shows the comparator output block diagram.

The TRISIO<2> bit functions as an output enable/disable for the GP2 pin while the comparator is in an Output mode.

- Note 1:** When reading the GPIO register, all pins configured as analog inputs will read as a '0'. Pins configured as digital inputs will convert an analog input according to the TTL input specification.
- 2:** Analog levels on any pin that is defined as a digital input, may cause the input buffer to consume more current than is specified.

FIGURE 6-4: MODIFIED COMPARATOR OUTPUT BLOCK DIAGRAM



6.5 Comparator Reference

The comparator module also allows the selection of an internally generated voltage reference for one of the comparator inputs. The internal reference signal is used for four of the eight Comparator modes. The VRCON register, Register 6-2, controls the voltage reference module shown in Figure 6-5.

6.5.1 CONFIGURING THE VOLTAGE REFERENCE

The voltage reference can output 32 distinct voltage levels, 16 in a high range and 16 in a low range.

The following equations determine the output voltages:

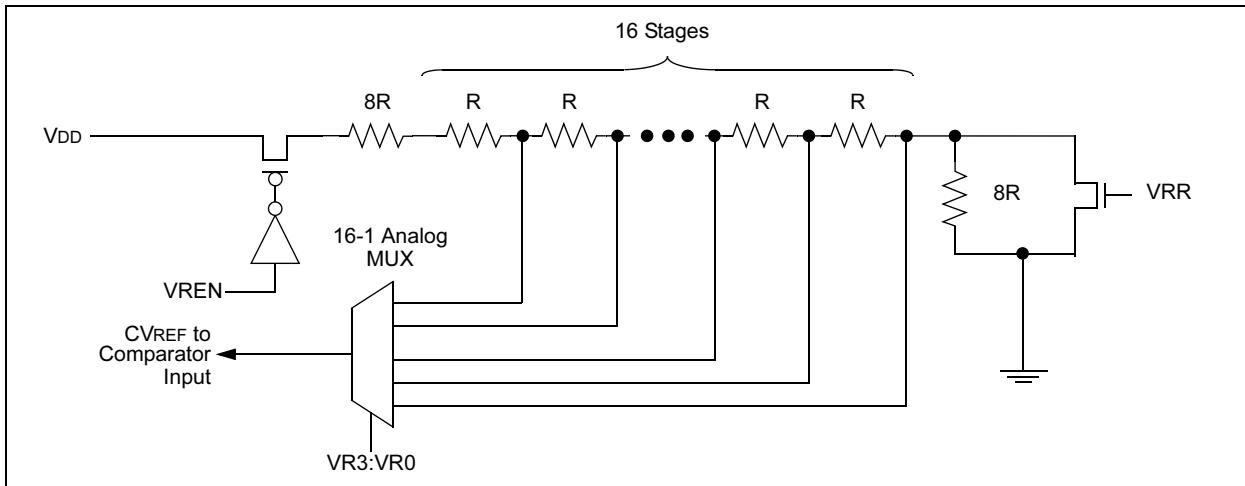
$$VRR = 1 \text{ (low range): } CVREF = (VR3:VR0 / 24) \times VDD$$

$$VRR = 0 \text{ (high range): } CVREF = (VDD / 4) + (VR3:VR0 \times VDD / 32)$$

6.5.2 VOLTAGE REFERENCE ACCURACY/ERROR

The full range of Vss to VDD cannot be realized due to the construction of the module. The transistors on the top and bottom of the resistor ladder network (Figure 6-5) keep CVREF from approaching Vss or VDD. The Voltage Reference is VDD derived and therefore, the CVREF output changes with fluctuations in VDD. The tested absolute accuracy of the Comparator Voltage Reference can be found in Section 12.0.

FIGURE 6-5: COMPARATOR VOLTAGE REFERENCE BLOCK DIAGRAM



6.6 Comparator Response Time

Response time is the minimum time, after selecting a new reference voltage or input source, before the comparator output is ensured to have a valid level. If the internal reference is changed, the maximum delay of the internal voltage reference must be considered when using the comparator outputs. Otherwise, the maximum delay of the comparators should be used (Table 12-7).

6.7 Operation During SLEEP

Both the comparator and voltage reference, if enabled before entering SLEEP mode, remain active during SLEEP. This results in higher SLEEP currents than shown in the power-down specifications. The additional current consumed by the comparator and the voltage reference is shown separately in the specifications. To minimize power consumption while in SLEEP mode, turn off the comparator, CM2:CM0 = 111, and voltage reference, VRCON<7> = 0.

While the comparator is enabled during SLEEP, an interrupt will wake-up the device. If the device wakes up from SLEEP, the contents of the CMCON and VRCON registers are not affected.

6.8 Effects of a RESET

A device RESET forces the CMCON and VRCON registers to their RESET states. This forces the comparator module to be in the Comparator Reset mode, CM2:CM0 = 000 and the voltage reference to its off state. Thus, all potential inputs are analog inputs with the comparator and voltage reference disabled to consume the smallest current possible.

PIC12F629/675

REGISTER 6-2: VRCON — VOLTAGE REFERENCE CONTROL REGISTER (ADDRESS: 99h)

bit 7 **VREN:** CVREF Enable bit
1 = CVREF circuit powered on
0 = CVREF circuit powered down, no IDD draw

bit 6 **Unimplemented:** Read as '0'

bit 5 **VRR:** CVREF Range Selection bit

1 = Low range

0 = High range

bit 4 Unimplemented

bit 4 Unimplemented. Read as 0

bit 3-0 VR3:VR0: CVREF value selection $0 \leq VR[3:0] \leq 15$
When $VRB = 1$: $CVREF = (VR3:VR0 / 24) + VREF$

Legend:

R = Readable bit

- n ≡ Value at POR

W = Writable bit

'1' = Bit is set

U = Unimplemented bit, read as '0'

'0' ≡ Bit is cleared x ≡ Bit is unknown

6.9 Comparator Interrupts

The comparator interrupt flag is set whenever there is a change in the output value of the comparator. Software will need to maintain information about the status of the output bits, as read from CMCON<6>, to determine the actual change that has occurred. The CMIF bit, PIR1<3>, is the comparator interrupt flag. This bit must be reset in software by clearing it to '0'. Since it is also possible to write a '1' to this register, a simulated interrupt may be initiated.

The CMIE bit (PIE1<3>) and the PEIE bit (INTCON<6>) must be set to enable the interrupt. In addition, the GIE bit must also be set. If any of these bits are cleared, the interrupt is not enabled, though the CMIF bit will still be set if an interrupt condition occurs.

The user, in the Interrupt Service Routine, can clear the interrupt in the following manner:

- a) Any read or write of CMCON. This will end the mismatch condition.
 - b) Clear flag bit CMIF.

A mismatch condition will continue to set flag bit CMIF. Reading CMCON will end the mismatch condition, and allow flag bit CMIF to be cleared.

Note: If a change in the CMCON register (COUT) should occur when a read operation is being executed (start of the Q2 cycle), then the CMIF (PIR1<3>) interrupt flag may not get set.

TABLE 6-2: REGISTERS ASSOCIATED WITH COMPARATOR MODULE

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD	Value on all other RESETS
0Bh/8Bh	INTCON	GIE	PEIE	TOIE	INTE	GPIE	TOIF	INTF	GPIF	0000 0000	0000 0000u
0Ch	PIR1	EEIF	ADIF	—	—	CMIF	—	—	TMR1IF	00-- 0--0	00-- 0--0
19h	CMCON	—	COUT	—	CINV	CIS	CM2	CM1	CM0	-0-0 0000	-0-0 0000
8Ch	PIE1	EEIE	ADIE	—	—	CMIE	—	—	TMR1IE	00-- 0--0	00-- 0--0
85h	TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	--11 1111	--11 1111
99h	VRCON	VREN	—	VRR	—	VR3	VR2	VR1	VR0	0-0- 0000	0-0- 0000

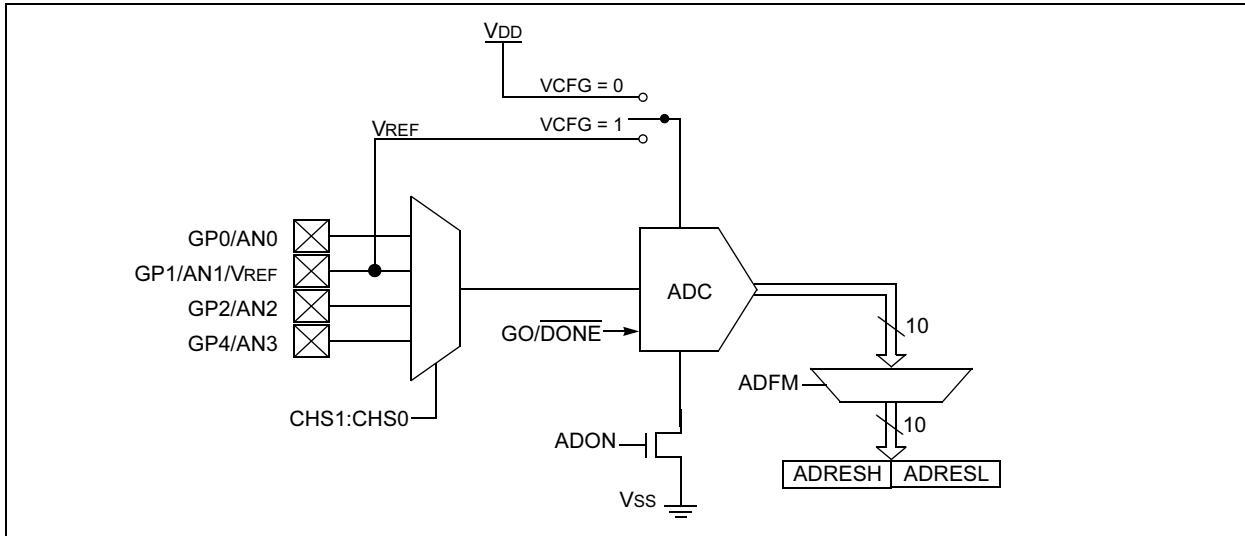
Legend: x = unknown, u = unchanged, - = unimplemented, read as '0'. Shaded cells are not used by the comparator module.

7.0 ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE (PIC12F675 ONLY)

The analog-to-digital converter (A/D) allows conversion of an analog input signal to a 10-bit binary representation of that signal. The PIC12F675 has four analog inputs, multiplexed into one sample and hold circuit.

The output of the sample and hold is connected to the input of the converter. The converter generates a binary result via successive approximation and stores the result in a 10-bit register. The voltage reference used in the conversion is software selectable to either VDD or a voltage applied by the VREF pin. Figure 7-1 shows the block diagram of the A/D on the PIC12F675.

FIGURE 7-1: A/D BLOCK DIAGRAM



7.1 A/D Configuration and Operation

There are two registers available to control the functionality of the A/D module:

1. ADCON0 (Register 7-1)
2. ANSEL (Register 7-2)

7.1.1 ANALOG PORT PINS

The ANS3:ANS0 bits (ANSEL<3:0>) and the TRISIO bits control the operation of the A/D port pins. Set the corresponding TRISIO bits to set the pin output driver to its high impedance state. Likewise, set the corresponding ANS bit to disable the digital input buffer.

Note: Analog voltages on any pin that is defined as a digital input may cause the input buffer to conduct excess current.

7.1.2 CHANNEL SELECTION

There are four analog channels on the PIC12F675, AN0 through AN3. The CHS1:CHS0 bits (ADCON0<3:2>) control which channel is connected to the sample and hold circuit.

7.1.3 VOLTAGE REFERENCE

There are two options for the voltage reference to the A/D converter: either VDD is used, or an analog voltage applied to VREF is used. The VCFG bit (ADCON0<6>)

controls the voltage reference selection. If VCFG is set, then the voltage on the VREF pin is the reference; otherwise, VDD is the reference.

7.1.4 CONVERSION CLOCK

The A/D conversion cycle requires 11 TAD. The source of the conversion clock is software selectable via the ADCS bits (ANSEL<6:4>). There are seven possible clock options:

- Fosc/2
- Fosc/4
- Fosc/8
- Fosc/16
- Fosc/32
- Fosc/64
- FRC (dedicated internal RC oscillator)

For correct conversion, the A/D conversion clock (1/TAD) must be selected to ensure a minimum TAD of 1.6 μ s. Table 7-1 shows a few TAD calculations for selected frequencies.

PIC12F629/675

TABLE 7-1: TAD vs. DEVICE OPERATING FREQUENCIES

A/D Clock Source (TAD)		Device Frequency			
Operation	ADCS2:ADCS0	20 MHz	5 MHz	4 MHz	1.25 MHz
2 Tosc	000	100 ns ⁽²⁾	400 ns ⁽²⁾	500 ns ⁽²⁾	1.6 µs
4 Tosc	100	200 ns ⁽²⁾	800 ns ⁽²⁾	1.0 µs ⁽²⁾	3.2 µs
8 Tosc	001	400 ns ⁽²⁾	1.6 µs	2.0 µs	6.4 µs
16 Tosc	101	800 ns ⁽²⁾	3.2 µs	4.0 µs	12.8 µs ⁽³⁾
32 Tosc	010	1.6 µs	6.4 µs	8.0 µs ⁽³⁾	25.6 µs ⁽³⁾
64 Tosc	110	3.2 µs	12.8 µs ⁽³⁾	16.0 µs ⁽³⁾	51.2 µs ⁽³⁾
A/D RC	x11	2 - 6 µs ^(1,4)			

Legend: Shaded cells are outside of recommended range.

Note 1: The A/D RC source has a typical TAD time of 4 µs for VDD > 3.0V.

2: These values violate the minimum required TAD time.

3: For faster conversion times, the selection of another clock source is recommended.

4: When the device frequency is greater than 1 MHz, the A/D RC clock source is only recommended if the conversion will be performed during SLEEP.

7.1.5 STARTING A CONVERSION

The A/D conversion is initiated by setting the GO/DONE bit (ADCON0<1>). When the conversion is complete, the A/D module:

- Clears the GO/DONE bit
- Sets the ADIF flag (PIR1<6>)
- Generates an interrupt (if enabled).

If the conversion must be aborted, the GO/DONE bit can be cleared in software. The ADRESH:ADRESL registers will not be updated with the partially complete A/D conversion sample. Instead, the ADRESH:ADRESL registers will retain the value of the

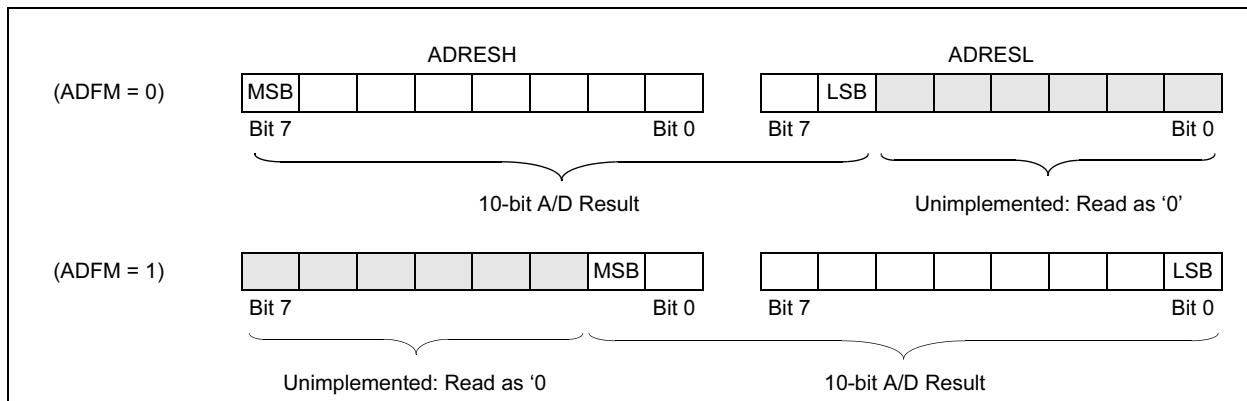
previous conversion. After an aborted conversion, a 2 TAD delay is required before another acquisition can be initiated. Following the delay, an input acquisition is automatically started on the selected channel.

Note: The GO/DONE bit should not be set in the same instruction that turns on the A/D.

7.1.6 CONVERSION OUTPUT

The A/D conversion can be supplied in two formats: left or right shifted. The ADFM bit (ADCON0<7>) controls the output format. Figure 7-2 shows the output formats.

FIGURE 7-2: 10-BIT A/D RESULT FORMAT



REGISTER 7-1: ADCON0 — A/D CONTROL REGISTER (ADDRESS: 1Fh)

R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
ADFM	VCFG	—	—	CHS1	CHS0	GO/DONE	ADON
bit 7				bit 0			

- | | |
|---------|---|
| bit 7 | ADFM: A/D Result Formed Select bit
1 = Right justified
0 = Left justified |
| bit 6 | VCFG: Voltage Reference bit
1 = VREF pin
0 = VDD |
| bit 5-4 | Unimplemented: Read as zero |
| bit 3-2 | CHS1:CHS0: Analog Channel Select bits
00 = Channel 00 (AN0)
01 = Channel 01 (AN1)
10 = Channel 02 (AN2)
11 = Channel 03 (AN3) |
| bit 1 | GO/DONE: A/D Conversion Status bit
1 = A/D conversion cycle in progress. Setting this bit starts an A/D conversion cycle.
This bit is automatically cleared by hardware when the A/D conversion has completed.
0 = A/D conversion completed/not in progress |
| bit 0 | ADON: A/D Conversion STATUS bit
1 = A/D converter module is operating
0 = A/D converter is shut-off and consumes no operating current |

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

PIC12F629/675

REGISTER 7-2: ANSEL — ANALOG SELECT REGISTER (ADDRESS: 9Fh)

U-0	R/W-0	R/W-0	R/W-0	R/W-1	R/W-1	R/W-1	R/W-1
—	ADCS2	ADCS1	ADCS0	ANS3	ANS2	ANS1	ANS0

bit 7 **Unimplemented:** Read as ‘0’.

bit 6-4 **ADCS<2:0>**: A/D Conversion Clock Select bits

$$000 = F_{osc}/2$$

$$001 = F_{osc}/8$$

$$010 = \text{Fosc}/32$$

x11 = FRC (clock derived from a dedicated internal oscillator = 500 kHz max)

$$100 = F_{osc}/4$$

$$101 = \text{Fosc}/10$$

$$110 = F_{osc}/64$$

ANS3:ANS0: A

bit 3-0 **ANSIANSI**: Analog Select bits
(Between analog or digital function)

1 ≡ Analog input: pin is assigned as analog input⁽¹⁾

\perp = Analog input, pin is assigned as analog input
 \ominus = Digital I/O; pin is assigned to port or special function

\cup = Digital I/O, pin is assigned to port or special function
Note: A, B, C, D are used to denote individual pins on the chip.

Note 1: Setting a pin to an analog input automatically disables the digital input circuitry, weak pull-ups, and interrupt-on-change. The corresponding TRISIO bit must be set to Input mode in order to allow external control of the voltage on the pin.

Legend:		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

7.2 A/D Acquisition Requirements

For the A/D converter to meet its specified accuracy, the charge holding capacitor (CHOLD) must be allowed to fully charge to the input channel voltage level. The analog input model is shown in Figure 7-3. The source impedance (R_s) and the internal sampling switch (R_{ss}) impedance directly affect the time required to charge the capacitor CHOLD. The sampling switch (R_{ss}) impedance varies over the device voltage (V_{DD}), see Figure 7-3. **The maximum recommended impedance for analog sources is 10 k Ω .** As the impedance is decreased, the acquisition time may be decreased.

After the analog input channel is selected (changed), this acquisition must be done before the conversion can be started.

To calculate the minimum acquisition time, Equation 7-1 may be used. This equation assumes that 1/2 LSB error is used (1024 steps for the A/D). The 1/2 LSB error is the maximum error allowed for the A/D to meet its specified resolution.

To calculate the minimum acquisition time, T_{ACQ} , see the PICmicro™ Mid-Range Reference Manual (DS33023).

EQUATION 7-1: ACQUISITION TIME

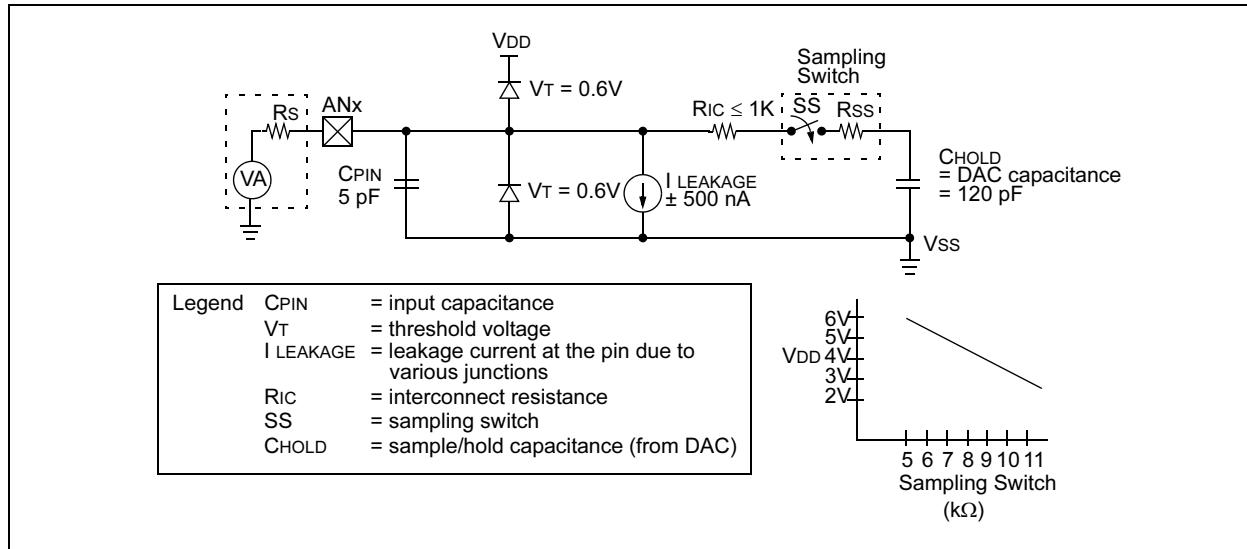
$T_{ACQ} = \text{Amplifier Settling Time} +$ $\text{Hold Capacitor Charging Time} +$ $\text{Temperature Coefficient}$	
	$= T_{AMP} + T_C + T_{COFF}$ $= 2\mu\text{s} + T_C + [(Temperature - 25^\circ\text{C})(0.05\mu\text{s}/^\circ\text{C})]$ $T_C = CHOLD (R_{IC} + R_{SS} + R_s) \ln(1/2047)$ $= -120\text{pF} (1\text{k}\Omega + 7\text{k}\Omega + 10\text{k}\Omega) \ln(0.0004885)$ $= 16.47\mu\text{s}$ $T_{ACQ} = 2\mu\text{s} + 16.47\mu\text{s} + [(50^\circ\text{C} - 25^\circ\text{C})(0.05\mu\text{s}/^\circ\text{C})]$ $= 19.72\mu\text{s}$

Note 1: The reference voltage (V_{REF}) has no effect on the equation, since it cancels itself out.

2: The charge holding capacitor (CHOLD) is not discharged after each conversion.

3: The maximum recommended impedance for analog sources is 10 k Ω . This is required to meet the pin leakage specification.

FIGURE 7-3: ANALOG INPUT MODEL



PIC12F629/675

7.3 A/D Operation During SLEEP

The A/D converter module can operate during SLEEP. This requires the A/D clock source to be set to the internal RC oscillator. When the RC clock source is selected, the A/D waits one instruction before starting the conversion. This allows the SLEEP instruction to be executed, thus eliminating much of the switching noise from the conversion. When the conversion is complete, the GO/DONE bit is cleared, and the result is loaded into the ADRESH:ADRESL registers. If the A/D interrupt is enabled, the device awakens from SLEEP. If the A/D interrupt is not enabled, the A/D module is turned off, although the ADON bit remains set.

When the A/D clock source is something other than RC, a SLEEP instruction causes the present conversion to be aborted, and the A/D module is turned off. The ADON bit remains set.

7.4 Effects of RESET

A device RESET forces all registers to their RESET state. Thus the A/D module is turned off and any pending conversion is aborted. The ADRESH:ADRESL registers are unchanged.

TABLE 7-2: SUMMARY OF A/D REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on: POR, BOD	Value on all other RESETS
05h	GPIO	—	—	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1	GPIO0	--xx xxxx	--uu uuuu
0Bh, 8Bh	INTCON	GIE	PEIE	TOIE	INTE	GPIE	T0IF	INTF	GPIF	0000 0000	0000 000u
0Ch	PIR1	EEIF	ADIF	—	—	CMIF	—	—	TMR1IF	00-- 0--0	00-- 0--0
1Eh	ADRESH	Most Significant 8 bits of the Left Shifted A/D result or 2 bits of the Right Shifted Result								xxxx xxxx	uuuu uuuu
1Fh	ADCON0	ADFM	VCFG	—	—	CHS1	CHS0	GO	ADON	00-- 0000	00-- 0000
85h	TRISIO	—	—	TRISIO5	TRISIO4	TRISIO3	TRISIO2	TRISIO1	TRISIO0	--11 1111	--11 1111
8Ch	PIE1	EEIE	ADIE	—	—	CMIE	—	—	TMR1IE	00-- 0--0	00-- 0--0
9Eh	ADRESL	Least Significant 2 bits of the Left Shifted A/D Result or 8 bits of the Right Shifted Result								xxxx xxxx	uuuu uuuu
9Fh	ANSEL	—	ADCS2	ADCS1	ADCS0	ANS3	ANS2	ANS1	ANS0	-000 1111	-000 1111

Legend: x = unknown, u = unchanged, - = unimplemented read as '0'. Shaded cells are not used for A/D converter module.

8.0 DATA EEPROM MEMORY

The EEPROM data memory is readable and writable during normal operation (full VDD range). This memory is not directly mapped in the register file space. Instead, it is indirectly addressed through the Special Function Registers. There are four SFRs used to read and write this memory:

- EECON1
- EECON2 (not a physically implemented register)
- EEDATA
- EEADR

EEDATA holds the 8-bit data for read/write, and EEADR holds the address of the EEPROM location being accessed. PIC12F629/675 devices have 128 bytes of data EEPROM with an address range from 0h to 7Fh.

The EEPROM data memory allows byte read and write. A byte write automatically erases the location and writes the new data (erase before write). The EEPROM data memory is rated for high erase/write cycles. The write time is controlled by an on-chip timer. The write time will vary with voltage and temperature as well as from chip to chip. Please refer to AC Specifications for exact limits.

When the data memory is code protected, the CPU may continue to read and write the data EEPROM memory. The device programmer can no longer access this memory.

Additional information on the Data EEPROM is available in the PICmicro™ Mid-Range Reference Manual, (DS33023).

REGISTER 8-1: EEDAT — EEPROM DATA REGISTER (ADDRESS: 9Ah)

R/W-0	R/W-0							
EEDAT7	EEDAT6	EEDAT5	EEDAT4	EEDAT3	EEDAT2	EEDAT1	EEDAT0	
bit 7								bit 0

bit 7-0 **EEDATn:** Byte value to write to or read from Data EEPROM

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

REGISTER 8-2: EEADR — EEPROM ADDRESS REGISTER (ADDRESS: 9Bh)

U-0	R/W-0	R/W-0						
—	EEADR6	EEADR5	EEADR4	EEADR3	EEADR2	EEADR1	EEADR0	
bit 7								bit 0

bit 7 **Unimplemented:** Should be set to '0'

bit 6-0 **EEADR:** Specifies one of 128 locations for EEPROM Read/Write Operation

Legend:

R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'
- n = Value at POR	'1' = Bit is set	'0' = Bit is cleared x = Bit is unknown

PIC12F629/675

8.1 EEAR

The EEADR register can address up to a maximum of 128 bytes of data EEPROM. Only seven of the eight bits in the register (EEADR<6:0>) are required. The MSb (bit 7) is ignored.

The upper bit should always be '0' to remain upward compatible with devices that have more data EEPROM memory.

8.2 EECON1 AND EECON2 REGISTERS

EECON1 is the control register with four low order bits physically implemented. The upper four bits are non-implemented and read as '0's.

Control bits RD and WR initiate read and write, respectively. These bits cannot be cleared, only set, in software. They are cleared in hardware at completion.

of the read or write operation. The inability to clear the WR bit in software prevents the accidental, premature termination of a write operation.

The WREN bit, when set, will allow a write operation. On power-up, the WREN bit is clear. The WRERR bit is set when a write operation is interrupted by a MCLR Reset, or a WDT Time-out Reset during normal operation. In these situations, following RESET, the user can check the WRERR bit, clear it, and rewrite the location. The data and address will be cleared, therefore, the EEDATA and EEADR registers will need to be re-initialized.

Interrupt flag bit EEIF in the PIR1 register is set when write is complete. This bit must be cleared in software.

EECON2 is not a physical register. Reading EECON2 will read all '0's. The EECON2 register is used exclusively in the Data EEPROM write sequence.

REGISTER 8-3: EECON1 — EEPROM CONTROL REGISTER (ADDRESS: 9Ch)

U-0	U-0	U-0	U-0	R/W-x	R/W-0	R/S-0	R/S-0
—	—	—	—	WRERR	WREN	WR	RD
bit 7				bit 0			

bit 7-4	Unimplemented: Read as '0'
bit 3	WRERR: EEPROM Error Flag bit 1 = A write operation is prematurely terminated (any <u>MCLR</u> Reset, any WDT Reset during normal operation or BOD detect) 0 = The write operation completed
bit 2	WREN: EEPROM Write Enable bit 1 = Allows write cycles 0 = Inhibits write to the data EEPROM
bit 1	WR: Write Control bit 1 = Initiates a write cycle (The bit is cleared by hardware once write is complete. The WR bit can only be set, not cleared, in software.) 0 = Write cycle to the data EEPROM is complete
bit 0	RD: Read Control bit 1 = Initiates an EEPROM read (Read takes one cycle. RD is cleared in hardware. The RD bit can only be set, not cleared, in software.) 0 = Does not initiate an EEPROM read

Legend:

S = Bit can only be set

R ≡ Readable bit

- p = Value at POF

W ≡ Writable bit

$\text{U} \equiv \text{Unimplemented bit, read as '0'}$

'0' = Bit is cleared x = Bit is unknown

8.3 READING THE EEPROM DATA MEMORY

To read a data memory location, the user must write the address to the EEADR register and then set control bit RD (EECON1<0>), as shown in Example 8-1. The data is available, in the very next cycle, in the EEDATA register. Therefore, it can be read in the next instruction. EEDATA holds this value until another read, or until it is written to by the user (during a write operation).

EXAMPLE 8-1: DATA EEPROM READ

```
bsf STATUS,RP0 ;Bank 1
movlw CONFIG_ADDR ;
movwf EEADR ;Address to read
bsf EECON1,RD ;EE Read
movf EEDATA,W ;Move data to W
```

8.4 WRITING TO THE EEPROM DATA MEMORY

To write an EEPROM data location, the user must first write the address to the EEADR register and the data to the EEDATA register. Then the user must follow a specific sequence to initiate the write for each byte, as shown in Example 8-2.

EXAMPLE 8-2: DATA EEPROM WRITE

```
bsf STATUS,RP0 ;Bank 1
bsf EECON1,WREN ;Enable write
bcf INTCON,GIE ;Disable INTs
movlw 55h ;Unlock write
movwf EECON2 ;
movlw AAh ;
movwf EECON2 ;
bsf EECON1,WR ;Start the write
bsf INTCON,GIE ;Enable INTs
```

The write will not initiate if the above sequence is not exactly followed (write 55h to EECON2, write AAh to EECON2, then set WR bit) for each byte. We strongly recommend that interrupts be disabled during this code segment. A cycle count is executed during the required sequence. Any number that is not equal to the required cycles to execute the required sequence will prevent the data from being written into the EEPROM.

Additionally, the WREN bit in EECON1 must be set to enable write. This mechanism prevents accidental writes to data EEPROM due to errant (unexpected) code execution (i.e., lost programs). The user should keep the WREN bit clear at all times, except when updating EEPROM. The WREN bit is not cleared by hardware.

Required Sequence

After a write sequence has been initiated, clearing the WREN bit will not affect this write cycle. The WR bit will be inhibited from being set unless the WREN bit is set.

At the completion of the write cycle, the WR bit is cleared in hardware and the EE Write Complete Interrupt Flag bit (EEIF) is set. The user can either enable this interrupt or poll this bit. The EEIF bit (PIR<7>) register must be cleared by software.

8.5 WRITE VERIFY

Depending on the application, good programming practice may dictate that the value written to the Data EEPROM should be verified (see Example 8-3) to the desired value to be written.

EXAMPLE 8-3: WRITE VERIFY

```
bcf STATUS,RP0 ;Bank 0
:
bsf STATUS,RP0 ;Any code
movf EEDATA,W ;Bank 1 READ
;EEDATA not changed
;from previous write
bsf EECON1,RD ;YES, Read the
;value written
xorwf EEDATA,W
btfsr STATUS,Z ;Is data the same
goto WRITE_ERR ;No, handle error
:
;Yes, continue
```

8.5.1 USING THE DATA EEPROM

The Data EEPROM is a high-endurance, byte addressable array that has been optimized for the storage of frequently changing information (e.g., program variables or other data that are updated often). Frequently changing values will typically be updated more often than specifications D120 or D120A. If this is not the case, an array refresh must be performed. For this reason, variables that change infrequently (such as constants, IDs, calibration, etc.) should be stored in FLASH program memory.

8.6 PROTECTION AGAINST SPURIOUS WRITE

There are conditions when the device may not want to write to the data EEPROM memory. To protect against spurious EEPROM writes, various mechanisms have been built in. On power-up, WREN is cleared. Also, the Power-up Timer (72 ms duration) prevents EEPROM write.

The write initiate sequence and the WREN bit together help prevent an accidental write during:

- brown-out
- power glitch
- software malfunction

PIC12F629/675

8.7 DATA EEPROM OPERATION DURING CODE PROTECT

Data memory can be code protected by programming the CPD bit to '0'.

When the data memory is code protected, the CPU is able to read and write data to the Data EEPROM. It is recommended to code protect the program memory when code protecting data memory. This prevents anyone from programming zeroes over the existing code (which will execute as NOPs) to reach an added routine, programmed in unused program memory, which outputs the contents of data memory. Programming unused locations to '0' will also help prevent data memory code protection from becoming breached.

TABLE 8-1: REGISTERS/BITS ASSOCIATED WITH DATA EEPROM

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD	Value on all other RESETS
0Ch	PIR1	EEIF	ADIF	—	—	CMIF	—	—	TMR1IF	00-- 0--0	00-- 0--0
9Ah	EEDATA	EEPROM Data Register								0000 0000	0000 0000
9Bh	EEADR	—	EEPROM Address Register								-000 0000
9Ch	EECON1	—	—	—	—	WRERR	WREN	WR	RD	---- x000	---- q000
9Dh	EECON2 ⁽¹⁾	EEPROM Control Register 2								-----	-----

Legend: x = unknown, u = unchanged, - = unimplemented read as '0', q = value depends upon condition.

Shaded cells are not used by Data EEPROM module.

Note 1: EECON2 is not a physical register.

9.0 SPECIAL FEATURES OF THE CPU

Certain special circuits that deal with the needs of real time applications are what sets a microcontroller apart from other processors. The PIC12F629/675 family has a host of such features intended to:

- maximize system reliability
- minimize cost through elimination of external components
- provide power saving operating modes and offer code protection.

These features are:

- Oscillator selection
- RESET
 - Power-on Reset (POR)
 - Power-up Timer (PWRT)
 - Oscillator Start-up Timer (OST)
 - Brown-out Detect (BOD)
- Interrupts
- Watchdog Timer (WDT)
- SLEEP
- Code protection
- ID Locations
- In-Circuit Serial Programming

The PIC12F629/675 has a Watchdog Timer that is controlled by configuration bits. It runs off its own RC oscillator for added reliability. There are two timers that offer necessary delays on power-up. One is the Oscillator Start-up Timer (OST), intended to keep the chip in RESET until the crystal oscillator is stable. The other is the Power-up Timer (PWRT), which provides a fixed delay of 72 ms (nominal) on power-up only, designed to keep the part in RESET while the power supply stabilizes. There is also circuitry to reset the device if a brown-out occurs, which can provide at least a 72 ms RESET. With these three functions on-chip, most applications need no external RESET circuitry.

The SLEEP mode is designed to offer a very low current Power-down mode. The user can wake-up from SLEEP through:

- External RESET
- Watchdog Timer wake-up
- An interrupt

Several oscillator options are also made available to allow the part to fit the application. The INTOSC option saves system cost while the LP crystal option saves power. A set of configuration bits are used to select various options (see Register 9-1).

PIC12F629/675

9.1 Configuration Bits

The configuration bits can be programmed (read as '0'), or left unprogrammed (read as '1') to select various device configurations, as shown in Register 9-1. These bits are mapped in program memory location 2007h.

Note: Address 2007h is beyond the user program memory space. It belongs to the special configuration memory space (2000h - 3FFFh), which can be accessed only during programming. See PIC12F629/675 Programming Specification for more information.

REGISTER 9-1: CONFIG — CONFIGURATION WORD (ADDRESS: 2007h)

R/P-1	R/P-1	U-0	U-0	U-0	R/P-1								
BG1	BG0	—	—	—	CPD	CP	BODEN	MCLRE	PWRTE	WDTE	F0SC2	F0SC1	F0SC0

bit 13

bit 0

bit 13-12 **BG1:BG0:** Bandgap Calibration bits for BOD and POR voltage⁽¹⁾

- 00 = Lowest bandgap voltage
- 11 = Highest bandgap voltage

bit 11-9 **Unimplemented:** Read as '0'

bit 8 **CPD:** Data Code Protection bit⁽²⁾

- 1 = Data memory code protection is disabled
- 0 = Data memory code protection is enabled

bit 7 **CP:** Code Protection bit⁽³⁾

- 1 = Program Memory code protection is disabled
- 0 = Program Memory code protection is enabled

bit 6 **BODEN:** Brown-out Detect Enable bit⁽⁴⁾

- 1 = BOD enabled
- 0 = BOD disabled

bit 5 **MCLRE:** GP3/MCLR pin function select⁽⁵⁾

- 1 = GP3/MCLR pin function is MCLR
- 0 = GP3/MCLR pin function is digital I/O, MCLR internally tied to VDD

bit 4 **PWRTE:** Power-up Timer Enable bit

- 1 = PWRT disabled
- 0 = PWRT enabled

bit 3 **WDTE:** Watchdog Timer Enable bit

- 1 = WDT enabled
- 0 = WDT disabled

bit 2-0 **FOSC2:FOSC0:** Oscillator Selection bits

- 111 = RC oscillator: CLKOUT function on GP4/OSC2/CLKOUT pin, RC on GP5/OSC1/CLKIN
- 110 = RC oscillator: I/O function on GP4/OSC2/CLKOUT pin, RC on GP5/OSC1/CLKIN
- 101 = INTOSC oscillator: CLKOUT function on GP4/OSC2/CLKOUT pin, I/O function on GP5/OSC1/CLKIN
- 100 = INTOSC oscillator: I/O function on GP4/OSC2/CLKOUT pin, I/O function on GP5/OSC1/CLKIN
- 011 = EC: I/O function on GP4/OSC2/CLKOUT pin, CLKIN on GP5/OSC1/CLKIN
- 010 = HS oscillator: High speed crystal/resonator on GP4/OSC2/CLKOUT and GP5/OSC1/CLKIN
- 001 = XT oscillator: Crystal/resonator on GP4/OSC2/CLKOUT and GP5/OSC1/CLKIN
- 000 = LP oscillator: Low power crystal on GP4/OSC2/CLKOUT and GP5/OSC1/CLKIN

Note 1: The Bandgap Calibration bits are factory programmed and must be read and saved prior to erasing the device as specified in the PIC12F629/675 Programming Specification. These bits are reflected in an export of the configuration word. Microchip Development Tools maintain all calibration bits to factory settings.

2: The entire data EEPROM will be erased when the code protection is turned off.

3: The entire program memory will be erased, including OSCCAL value, when the code protection is turned off.

4: Enabling Brown-out Detect does not automatically enable Power-up Timer.

5: When MCLR is asserted in INTOSC or RC mode, the internal clock oscillator is disabled.

Legend:

P = Programmed using ICSP

R = Readable bit

W = Writable bit

U = Unimplemented bit, read as '0'

-n = Value at POR

1 = bit is set

0 = bit is cleared

x = bit is unknown

9.2 Oscillator Configurations

9.2.1 OSCILLATOR TYPES

The PIC12F629/675 can be operated in eight different oscillator option modes. The user can program three configuration bits (FOSC2 through FOSC0) to select one of these eight modes:

- LP Low Power Crystal
- XT Crystal/Resonator
- HS High Speed Crystal/Resonator
- RC External Resistor/Capacitor (2 modes)
- INTOSC Internal Oscillator (2 modes)
- EC External Clock In

Note: Additional information on oscillator configurations is available in the PICmicro™ Mid-Range Reference Manual, (DS33023).

9.2.2 CRYSTAL OSCILLATOR / CERAMIC RESONATORS

In XT, LP or HS modes a crystal or ceramic resonator is connected to the OSC1 and OSC2 pins to establish oscillation (see Figure 9-1). The PIC12F629/675 oscillator design requires the use of a parallel cut crystal. Use of a series cut crystal may yield a frequency outside of the crystal manufacturers specifications. When in XT, LP or HS modes, the device can have an external clock source to drive the OSC1 pin (see Figure 9-2).

FIGURE 9-1: CRYSTAL OPERATION (OR CERAMIC RESONATOR) HS, XT OR LP OSC CONFIGURATION

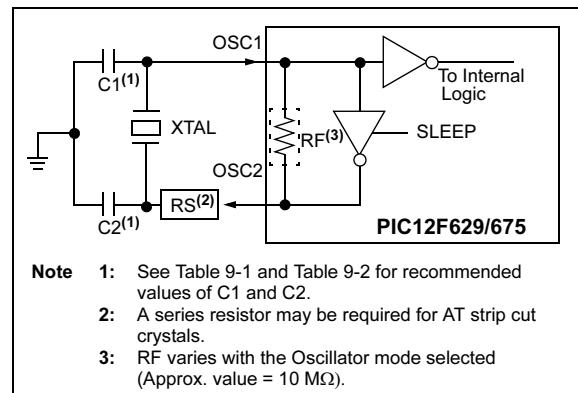


FIGURE 9-2: EXTERNAL CLOCK INPUT OPERATION (HS, XT, EC, OR LP OSC CONFIGURATION)

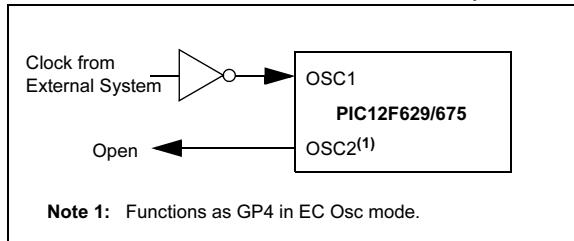


TABLE 9-1: CAPACITOR SELECTION FOR CERAMIC RESONATORS

Ranges Characterized:			
Mode	Freq	OSC1(C1)	OSC2(C2)
XT	455 kHz	68 - 100 pF	68 - 100 pF
	2.0 MHz	15 - 68 pF	15 - 68 pF
	4.0 MHz	15 - 68 pF	15 - 68 pF
HS	8.0 MHz	10 - 68 pF	10 - 68 pF
	16.0 MHz	10 - 22 pF	10 - 22 pF

Note 1: Higher capacitance increases the stability of the oscillator but also increases the start-up time. These values are for design guidance only. Since each resonator has its own characteristics, the user should consult the resonator manufacturer for appropriate values of external components.

TABLE 9-2: CAPACITOR SELECTION FOR CRYSTAL OSCILLATOR

Mode	Freq	OSC1(C1)	OSC2(C2)
LP	32 kHz	68 - 100 pF	68 - 100 pF
XT	100 kHz	68 - 150 pF	150 - 200 pF
	2 MHz	15 - 30 pF	15 - 30 pF
	4 MHz	15 - 30 pF	15 - 30 pF
HS	8 MHz	15 - 30 pF	15 - 30 pF
	10 MHz	15 - 30 pF	15 - 30 pF
	20 MHz	15 - 30 pF	15 - 30 pF

Note 1: Higher capacitance increases the stability of the oscillator but also increases the start-up time. These values are for design guidance only. Rs may be required in HS mode as well as XT mode to avoid overdriving crystals with low drive level specification. Since each crystal has its own characteristics, the user should consult the crystal manufacturer for appropriate values of external components.

PIC12F629/675

9.2.3 EXTERNAL CLOCK IN

For applications where a clock is already available elsewhere, users may directly drive the PIC12F629/675 provided that this external clock source meets the AC/DC timing requirements listed in Section 12.0. Figure 9-2 shows how an external clock circuit should be configured.

9.2.4 RC OSCILLATOR

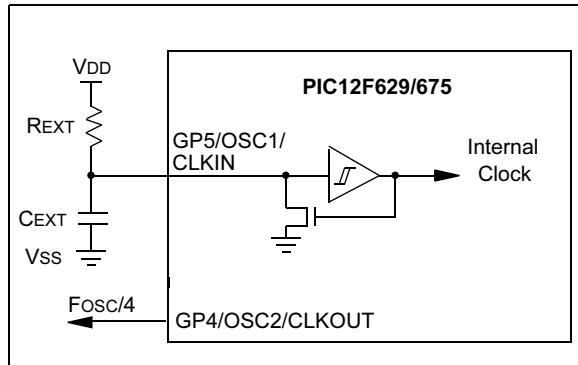
For applications where precise timing is not a requirement, the RC oscillator option is available. The operation and functionality of the RC oscillator is dependent upon a number of variables. The RC oscillator frequency is a function of:

- Supply voltage
- Resistor (R_{EXT}) and capacitor (C_{EXT}) values
- Operating temperature.

The oscillator frequency will vary from unit to unit due to normal process parameter variation. The difference in lead frame capacitance between package types will also affect the oscillation frequency, especially for low C_{EXT} values. The user also needs to account for the tolerance of the external R and C components. Figure 9-3 shows how the R/C combination is connected.

Two options are available for this Oscillator mode which allow GP4 to be used as a general purpose I/O or to output Fosc/4.

FIGURE 9-3: RC OSCILLATOR MODE



9.2.5 INTERNAL 4 MHz OSCILLATOR

When calibrated, the internal oscillator provides a fixed 4 MHz (nominal) system clock. See Electrical Specifications, Section 12.0, for information on variation over voltage and temperature.

Two options are available for this Oscillator mode which allow GP4 to be used as a general purpose I/O or to output Fosc/4.

9.2.5.1 Calibrating the Internal Oscillator

A calibration instruction is programmed into the last location of program memory. This instruction is a RETLW XX, where the literal is the calibration value. The literal is placed in the OSCCAL register to set the calibration of the internal oscillator. Example 9-1 demonstrates how to calibrate the internal oscillator. For best operation, decouple (with capacitance) VDD and Vss as close to the device as possible.

Note: Erasing the device will also erase the pre-programmed internal calibration value for the internal oscillator. The calibration value must be saved prior to erasing part as specified in the PIC12F629/675 Programming specification. Microchip Development Tools maintain all calibration bits to factory settings.

EXAMPLE 9-1: CALIBRATING THE INTERNAL OSCILLATOR

```
bsf    STATUS, RP0      ;Bank 1
call   3FFh              ;Get the cal value
movwf  OSCCAL            ;Calibrate
bcf    STATUS, RP0      ;Bank 0
```

9.2.6 CLKOUT

The PIC12F629/675 devices can be configured to provide a clock out signal in the INTOSC and RC oscillator modes. When configured, the oscillator frequency divided by four (Fosc/4) is output on the GP4/OSC2/CLKOUT pin. Fosc/4 can be used for test purposes or to synchronize other logic.

9.3 RESET

The PIC12F629/675 differentiates between various kinds of RESET:

- Power-on Reset (POR)
- WDT Reset during normal operation
- WDT Reset during SLEEP
- MCLR Reset during normal operation
- MCLR Reset during SLEEP
- Brown-out Detect (BOD)

Some registers are not affected in any RESET condition; their status is unknown on POR and unchanged in any other RESET. Most other registers are reset to a “RESET state” on:

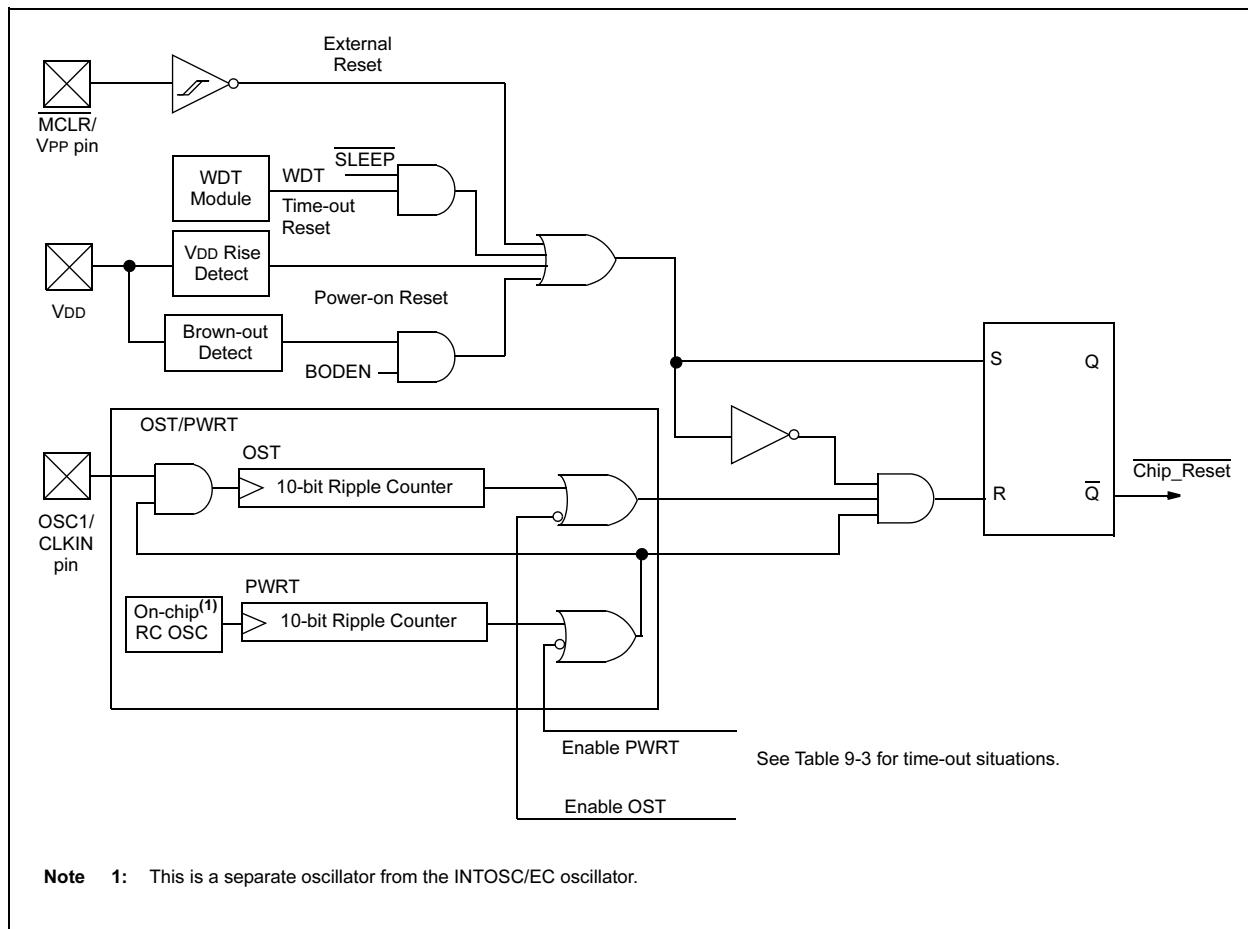
- Power-on Reset
- MCLR Reset
- WDT Reset
- WDT Reset during SLEEP
- Brown-out Detect (BOD) Reset

They are not affected by a WDT wake-up, since this is viewed as the resumption of normal operation. $\overline{\text{TO}}$ and $\overline{\text{PD}}$ bits are set or cleared differently in different RESET situations as indicated in Table 9-4. These bits are used in software to determine the nature of the RESET. See Table 9-7 for a full description of RESET states of all registers.

A simplified block diagram of the On-Chip Reset Circuit is shown in Figure 9-4.

The MCLR Reset path has a noise filter to detect and ignore small pulses. See Table 12-4 in Electrical Specifications Section for pulse width specification.

FIGURE 9-4: SIMPLIFIED BLOCK DIAGRAM OF ON-CHIP RESET CIRCUIT



Note 1: This is a separate oscillator from the INTOSC/EC oscillator.

PIC12F629/675

9.3.1 MCLR

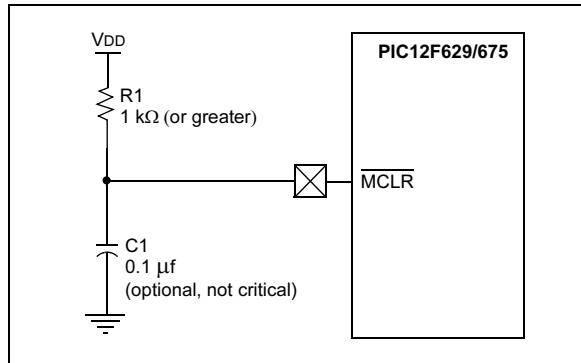
PIC12F629/675 devices have a noise filter in the MCLR Reset path. The filter will detect and ignore small pulses.

It should be noted that a WDT Reset does not drive MCLR pin low.

The behavior of the ESD protection on the MCLR pin has been altered from previous devices of this family. Voltages applied to the pin that exceed its specification can result in both MCLR Resets and excessive current beyond the device specification during the ESD event. For this reason, Microchip recommends that the MCLR pin no longer be tied directly to VDD. The use of an RC network, as shown in Figure 9-5, is suggested.

An internal MCLR option is enabled by setting the MCLRE bit in the configuration word. When enabled, MCLR is internally tied to VDD. No internal pull-up option is available for the MCLR pin.

FIGURE 9-5: RECOMMENDED MCLR CIRCUIT



9.3.2 POWER-ON RESET (POR)

The on-chip POR circuit holds the chip in RESET until VDD has reached a high enough level for proper operation. To take advantage of the POR, simply tie the MCLR pin through a resistor to VDD. This will eliminate external RC components usually needed to create Power-on Reset. A maximum rise time for VDD is required. See Electrical Specifications for details (see Section 12.0). If the BOD is enabled, the maximum rise time specification does not apply. The BOD circuitry will keep the device in RESET until VDD reaches VBOD (see Section 9.3.5).

Note: The POR circuit does not produce an internal RESET when VDD declines.

When the device starts normal operation (exits the RESET condition), device operating parameters (i.e., voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, the device must be held in RESET until the operating conditions are met.

For additional information, refer to Application Note AN607 "Power-up Trouble Shooting".

9.3.3 POWER-UP TIMER (PWRT)

The Power-up Timer provides a fixed 72 ms (nominal) time-out on power-up only, from POR or Brown-out Detect. The Power-up Timer operates on an internal RC oscillator. The chip is kept in RESET as long as PWRT is active. The PWRT delay allows the VDD to rise to an acceptable level. A configuration bit, PWRTE can disable (if set) or enable (if cleared or programmed) the Power-up Timer. The Power-up Timer should always be enabled when Brown-out Detect is enabled.

The Power-up Time delay will vary from chip to chip and due to:

- VDD variation
- Temperature variation
- Process variation.

See DC parameters for details (Section 12.0).

9.3.4 OSCILLATOR START-UP TIMER (OST)

The Oscillator Start-up Timer (OST) provides a 1024 oscillator cycle (from OSC1 input) delay after the PWRT delay is over. This ensures that the crystal oscillator or resonator has started and stabilized.

The OST time-out is invoked only for XT, LP and HS modes and only on Power-on Reset or wake-up from SLEEP.

9.3.5 BROWN-OUT DETECT (BOD)

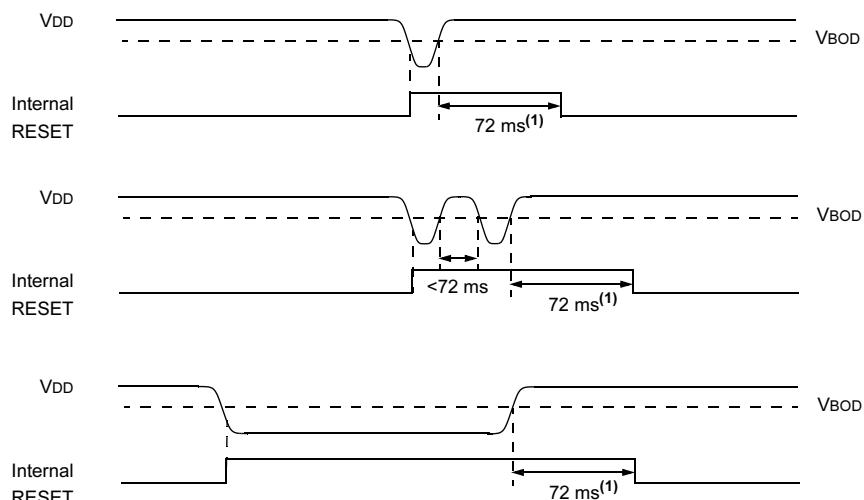
The PIC12F629/675 members have on-chip Brown-out Detect circuitry. A configuration bit, BODEN, can disable (if clear/programmed) or enable (if set) the Brown-out Detect circuitry. If VDD falls below VBOD for greater than parameter (TBOD) in Table 12-4 (see Section 12.0), the Brown-out situation will reset the device. This will occur regardless of VDD slew-rate. A RESET is not guaranteed to occur if VDD falls below VBOD for less than parameter (TBOD).

On any RESET (Power-on, Brown-out, Watchdog, etc.), the chip will remain in RESET until VDD rises above BVDD (see Figure 9-6). The Power-up Timer will now be invoked, if enabled, and will keep the chip in RESET an additional 72 ms.

Note: A Brown-out Detect does not enable the Power-up Timer if the PWRTE bit in the configuration word is set.

If VDD drops below BVDD while the Power-up Timer is running, the chip will go back into a Brown-out Detect and the Power-up Timer will be re-initialized. Once VDD rises above BVDD, the Power-up Timer will execute a 72 ms RESET.

FIGURE 9-6: BROWN-OUT SITUATIONS



Note 1: 72 ms delay only if PWRTE bit is programmed to '0'.

9.3.6 TIME-OUT SEQUENCE

On power-up, the time-out sequence is as follows: first, PWRT time-out is invoked after POR has expired. Then, OST is activated. The total time-out will vary based on oscillator configuration and PWRTE bit status. For example, in EC mode with PWRTE bit erased (PWRT disabled), there will be no time-out at all. Figure 9-7, Figure 9-8 and Figure 9-9 depict time-out sequences.

Since the time-outs occur from the POR pulse, if MCLR is kept low long enough, the time-outs will expire. Then bringing MCLR high will begin execution immediately (see Figure 9-8). This is useful for testing purposes or to synchronize more than one PIC12F629/675 device operating in parallel.

Table 9-6 shows the RESET conditions for some special registers, while Table 9-7 shows the RESET conditions for all the registers.

9.3.7 POWER CONTROL (PCON) STATUS REGISTER

The power CONTROL/STATUS register, PCON (address 8Eh) has two bits.

Bit0 is BOD (Brown-out). BOD is unknown on Power-on Reset. It must then be set by the user and checked on subsequent RESETS to see if BOD = 0, indicating that a brown-out has occurred. The BOD STATUS bit is a don't care and is not necessarily predictable if the brown-out circuit is disabled (by setting BODEN bit = 0 in the Configuration word).

Bit1 is POR (Power-on Reset). It is a '0' on Power-on Reset and unaffected otherwise. The user must write a '1' to this bit following a Power-on Reset. On a subsequent RESET, if POR is '0', it will indicate that a Power-on Reset must have occurred (i.e., VDD may have gone too low).

PIC12F629/675

TABLE 9-3: TIME-OUT IN VARIOUS SITUATIONS

Oscillator Configuration	Power-up		Brown-out Detect		Wake-up from SLEEP
	$\overline{\text{PWRTE}} = 0$	$\overline{\text{PWRTE}} = 1$	$\overline{\text{PWRTE}} = 0$	$\overline{\text{PWRTE}} = 1$	
XT, HS, LP	TPWRT + 1024•TOSC	1024•TOSC	TPWRT + 1024•TOSC	1024•TOSC	1024•TOSC
RC, EC, INTOSC	TPWRT	—	TPWRT	—	—

TABLE 9-4: STATUS/PCON BITS AND THEIR SIGNIFICANCE

$\overline{\text{POR}}$	$\overline{\text{BOD}}$	$\overline{\text{TO}}$	$\overline{\text{PD}}$	
0	u	1	1	Power-on Reset
1	0	1	1	Brown-out Detect
u	u	0	u	WDT Reset
u	u	0	0	WDT Wake-up
u	u	u	u	MCLR Reset during normal operation
u	u	1	0	MCLR Reset during SLEEP

Legend: u = unchanged, x = unknown

TABLE 9-5: SUMMARY OF REGISTERS ASSOCIATED WITH BROWN-OUT

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD	Value on all other RESETS ⁽¹⁾
03h	STATUS	IRP	RP1	RPO	$\overline{\text{TO}}$	$\overline{\text{PD}}$	Z	DC	C	0001 1xxx	000q quuu
8Eh	PCON	—	—	—	—	—	—	POR	BOD	---- --0x	---- --uq

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: Other (non Power-up) Resets include MCLR Reset, Brown-out Detect and Watchdog Timer Reset during normal operation.

TABLE 9-6: INITIALIZATION CONDITION FOR SPECIAL REGISTERS

Condition	Program Counter	STATUS Register	PCON Register
Power-on Reset	000h	0001 1xxx	---- --0x
MCLR Reset during normal operation	000h	000u uuuu	---- --uu
MCLR Reset during SLEEP	000h	0001 0uuu	---- --uu
WDT Reset	000h	0000 uuuu	---- --uu
WDT Wake-up	PC + 1	uuu0 0uuu	---- --uu
Brown-out Detect	000h	0001 1uuu	---- --10
Interrupt Wake-up from SLEEP	PC + 1 ⁽¹⁾	uuu1 0uuu	---- --uu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0'.

Note 1: When the wake-up is due to an interrupt and global enable bit GIE is set, the PC is loaded with the interrupt vector (0004h) after execution of PC+1.

TABLE 9-7: INITIALIZATION CONDITION FOR REGISTERS

Register	Address	Power-on Reset	• <u>MCLR Reset during normal operation</u> • <u>MCLR Reset during SLEEP</u> • <u>WDT Reset</u> • <u>Brown-out Detect⁽¹⁾</u>	• Wake-up from SLEEP through interrupt • Wake-up from SLEEP through WDT time-out
W	—	xxxx xxxx	uuuu uuuu	uuuu uuuu
INDF	00h/80h	—	—	—
TMR0	01h	xxxx xxxx	uuuu uuuu	uuuu uuuu
PCL	02h/82h	0000 0000	0000 0000	PC + 1 ⁽³⁾
STATUS	03h/83h	0001 1xxx	000q quuu ⁽⁴⁾	uuuq quuu ⁽⁴⁾
FSR	04h/84h	xxxx xxxx	uuuu uuuu	uuuu uuuu
GPIO	05h	--xx xxxx	--uu uuuu	--uu uuuu
PCLATH	0Ah/8Ah	--0 0000	--0 0000	--u uuuu
INTCON	0Bh/8Bh	0000 0000	0000 000u	uuuu uqqq ⁽²⁾
PIR1	0Ch	00-- 0--0	00-- 0--0	qq-- q--q ^(2,5)
T1CON	10h	-000 0000	-uuu uuuu	-uuu uuuu
CMCON	19h	-0-0 0000	-0-0 0000	-u-u uuuu
ADRESH	1Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
ADCON0	1Fh	00-- 0000	00-- 0000	uu-- uuuu
OPTION_REG	81h	1111 1111	1111 1111	uuuu uuuu
TRISIO	85h	--11 1111	--11 1111	--uu uuuu
PIE1	8Ch	00-- 0--0	00-- 0--0	uu-- u--u
PCON	8Eh	---- --0x	---- --uu ^(1,6)	---- --uu
OSCCAL	90h	1000 00--	1000 00--	uuuu uu--
WPU	95h	--11 -111	--11 -111	uuuu uuuu
IOC	96h	--00 0000	--00 0000	--uu uuuu
VRCON	99h	0-0- 0000	0-0- 0000	u-u- uuuu
EEDATA	9Ah	0000 0000	0000 0000	uuuu uuuu
EEADR	9Bh	-000 0000	-000 0000	-uuu uuuu
EECON1	9Ch	---- x000	---- q000	---- uuuu
EECON2	9Dh	---- ----	---- ----	---- ----
ADRESL	9Eh	xxxx xxxx	uuuu uuuu	uuuu uuuu
ANSEL	9Fh	-000 1111	-000 1111	-uuu uuuu

Legend: u = unchanged, x = unknown, - = unimplemented bit, reads as '0', q = value depends on condition.

Note 1: If VDD goes too low, Power-on Reset will be activated and registers will be affected differently.

- 2: One or more bits in INTCON and/or PIR1 will be affected (to cause wake-up).
- 3: When the wake-up is due to an interrupt and the GIE bit is set, the PC is loaded with the interrupt vector (0004h).
- 4: See Table 9-6 for RESET value for specific condition.
- 5: If wake-up was due to data EEPROM write completing, Bit 7 = 1; A/D conversion completing, Bit 6 = 1; Comparator input changing, bit 3 = 1; or Timer1 rolling over, bit 0 = 1. All other interrupts generating a wake-up will cause these bits to = u.
- 6: If RESET was due to brown-out, then bit 0 = 0. All other RESETS will cause bit 0 = u.

PIC12F629/675

FIGURE 9-7: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO V_{DD}): CASE 1

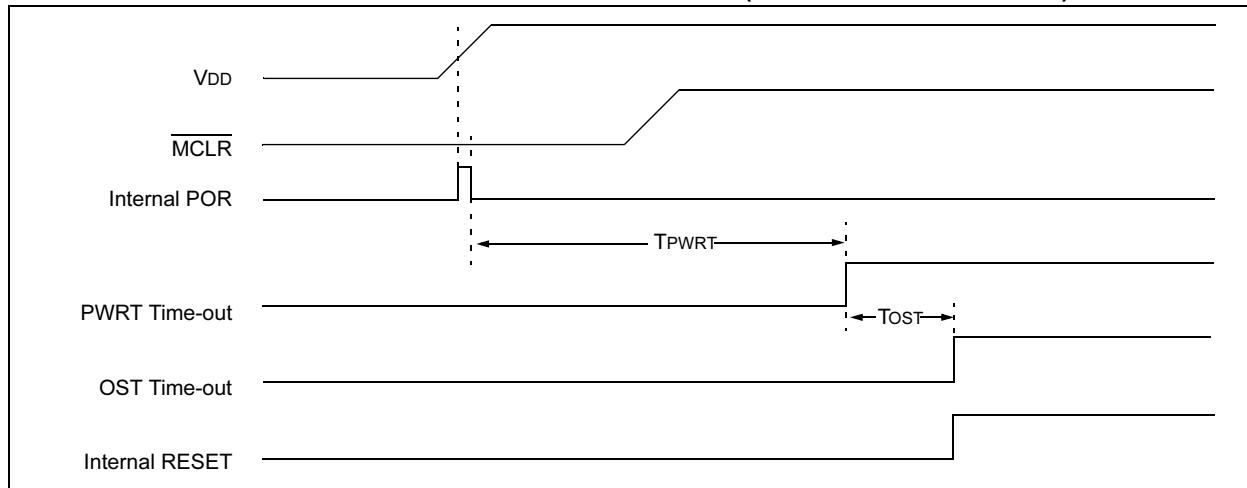


FIGURE 9-8: TIME-OUT SEQUENCE ON POWER-UP (MCLR NOT TIED TO V_{DD}): CASE 2

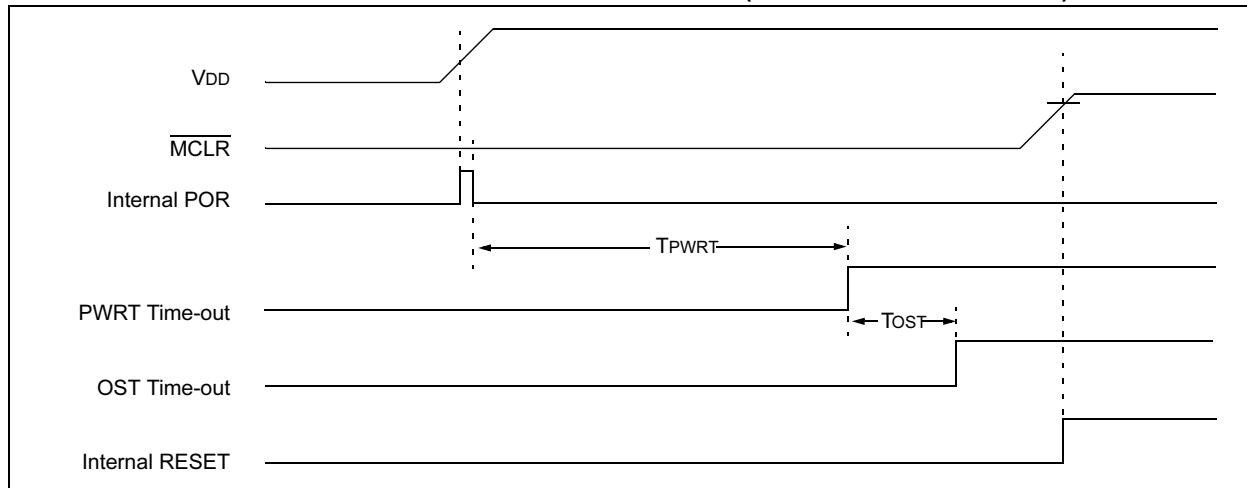
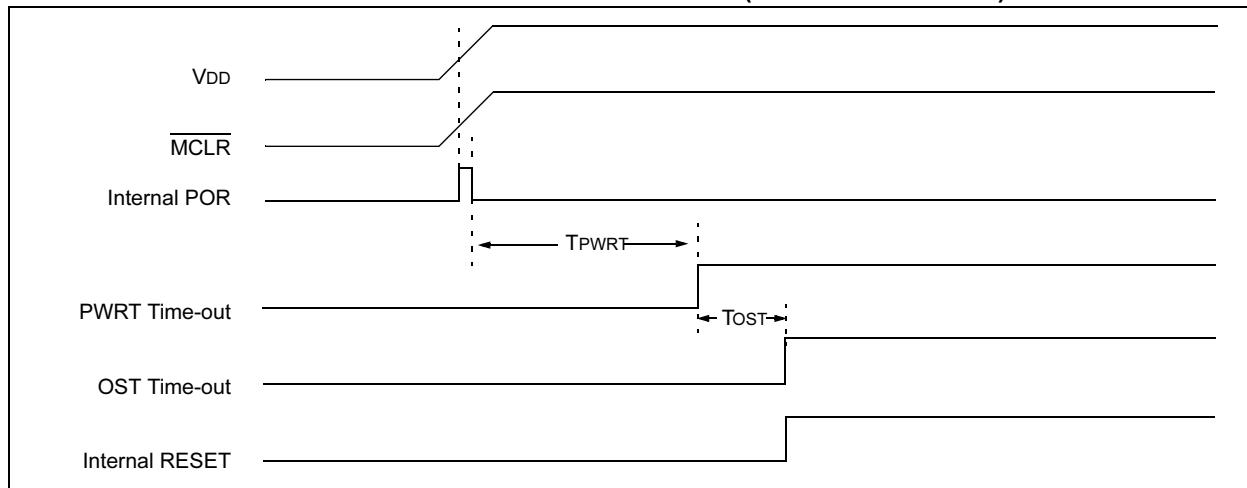


FIGURE 9-9: TIME-OUT SEQUENCE ON POWER-UP (MCLR TIED TO V_{DD})



9.4 Interrupts

The PIC12F629/675 has 7 sources of interrupt:

- External Interrupt GP2/INT
- TMR0 Overflow Interrupt
- GPIO Change Interrupts
- Comparator Interrupt
- A/D Interrupt (PIC12F675 only)
- TMR1 Overflow Interrupt
- EEPROM Data Write Interrupt

The Interrupt Control register (INTCON) and Peripheral Interrupt register (PIR) record individual interrupt requests in flag bits. The INTCON register also has individual and global interrupt enable bits.

A global interrupt enable bit, GIE (INTCON<7>) enables (if set) all unmasked interrupts, or disables (if cleared) all interrupts. Individual interrupts can be disabled through their corresponding enable bits in INTCON register and PIE register. GIE is cleared on RESET.

The return from interrupt instruction, RETFIE, exits interrupt routine, as well as sets the GIE bit, which re-enables unmasked interrupts.

The following interrupt flags are contained in the INTCON register:

- INT pin interrupt
- GP port change interrupt
- TMR0 overflow interrupt

The peripheral interrupt flags are contained in the special register PIR1. The corresponding interrupt enable bit is contained in Special Register PIE1.

The following interrupt flags are contained in the PIR register:

- EEPROM data write interrupt
- A/D interrupt
- Comparator interrupt
- Timer1 overflow interrupt

When an interrupt is serviced:

- The GIE is cleared to disable any further interrupt
- The return address is pushed onto the stack
- The PC is loaded with 0004h

Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid GP2/INT recursive interrupts.

For external interrupt events, such as the INT pin, or GP port change interrupt, the interrupt latency will be three or four instruction cycles. The exact latency depends upon when the interrupt event occurs (see Figure 9-11). The latency is the same for one or two-cycle instructions. Once in the Interrupt Service Routine, the source(s) of the interrupt can be determined by polling the interrupt flag bits. The

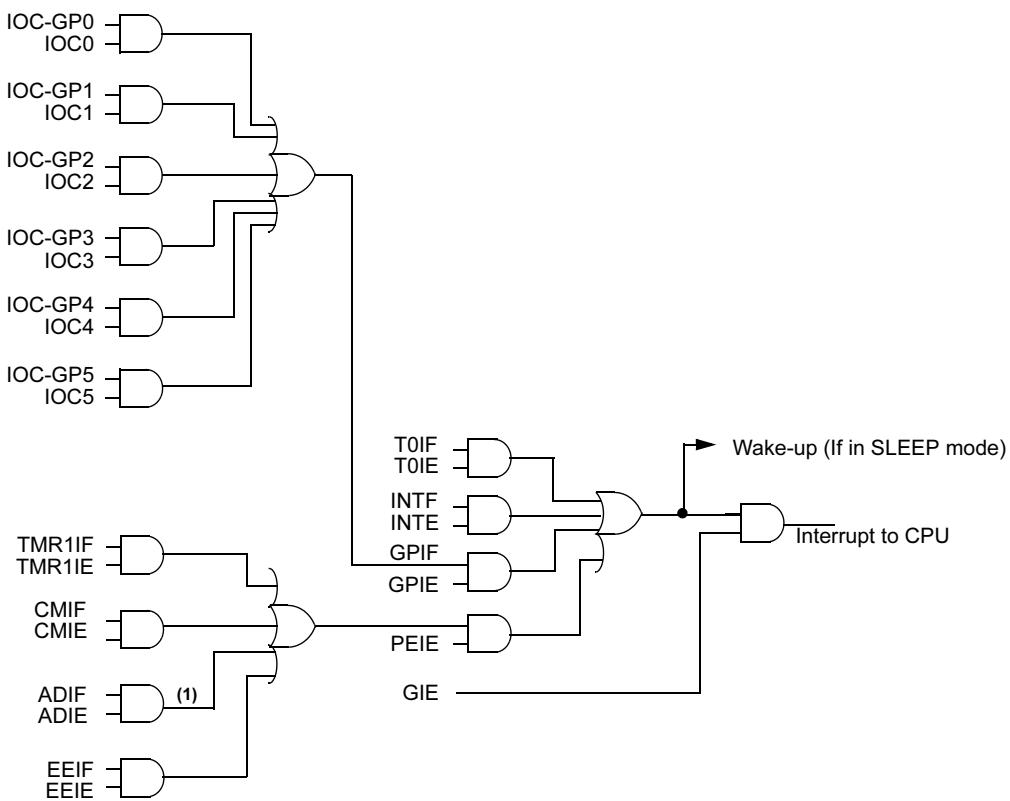
interrupt flag bit(s) must be cleared in software before re-enabling interrupts to avoid multiple interrupt requests.

Note 1: Individual interrupt flag bits are set, regardless of the status of their corresponding mask bit or the GIE bit.

2: When an instruction that clears the GIE bit is executed, any interrupts that were pending for execution in the next cycle are ignored. The interrupts which were ignored are still pending to be serviced when the GIE bit is set again.

PIC12F629/675

FIGURE 9-10: INTERRUPT LOGIC



Note 1: PIC12F675 only.

9.4.1 GP2/INT INTERRUPT

External interrupt on GP2/INT pin is edge-triggered; either rising if INTEDG bit (OPTION<6>) is set, or falling, if INTEDG bit is clear. When a valid edge appears on the GP2/INT pin, the INTF bit (INTCON<1>) is set. This interrupt can be disabled by clearing the INTE control bit (INTCON<4>). The INTF bit must be cleared in software in the Interrupt Service Routine before re-enabling this interrupt. The GP2/INT interrupt can wake-up the processor from SLEEP if the INTE bit was set prior to going into SLEEP. The status of the GIE bit decides whether or not the processor branches to the interrupt vector following wake-up. See Section 9.7 for details on SLEEP and Figure 9-13 for timing of wake-up from SLEEP through GP2/INT interrupt.

Note: The ANSEL (9Fh) and CMCON (19h) registers must be initialized to configure an analog channel as a digital input. Pins configured as analog inputs will read '0'. The ANSEL register is defined for the PIC12F675.

9.4.2 TMR0 INTERRUPT

An overflow (FFh → 00h) in the TMR0 register will set the T0IF (INTCON<2>) bit. The interrupt can be enabled/disabled by setting/clearing T0IE (INTCON<5>) bit. For operation of the Timer0 module, see Section 4.0.

9.4.3 GPIO INTERRUPT

An input change on GPIO change sets the GPIF (INTCON<0>) bit. The interrupt can be enabled/disabled by setting/clearing the GPIE (INTCON<3>) bit. Plus individual pins can be configured through the IOC register.

Note: If a change on the I/O pin should occur when the read operation is being executed (start of the Q2 cycle), then the GPIF interrupt flag may not get set.

9.4.4 COMPARATOR INTERRUPT

See Section 6.9 for description of comparator interrupt.

9.4.5 A/D CONVERTER INTERRUPT

After a conversion is complete, the ADIF flag (PIR<6>) is set. The interrupt can be enabled/disabled by setting or clearing ADIE (PIE<6>).

See Section 7.0 for operation of the A/D converter interrupt.

FIGURE 9-11: INT PIN INTERRUPT TIMING

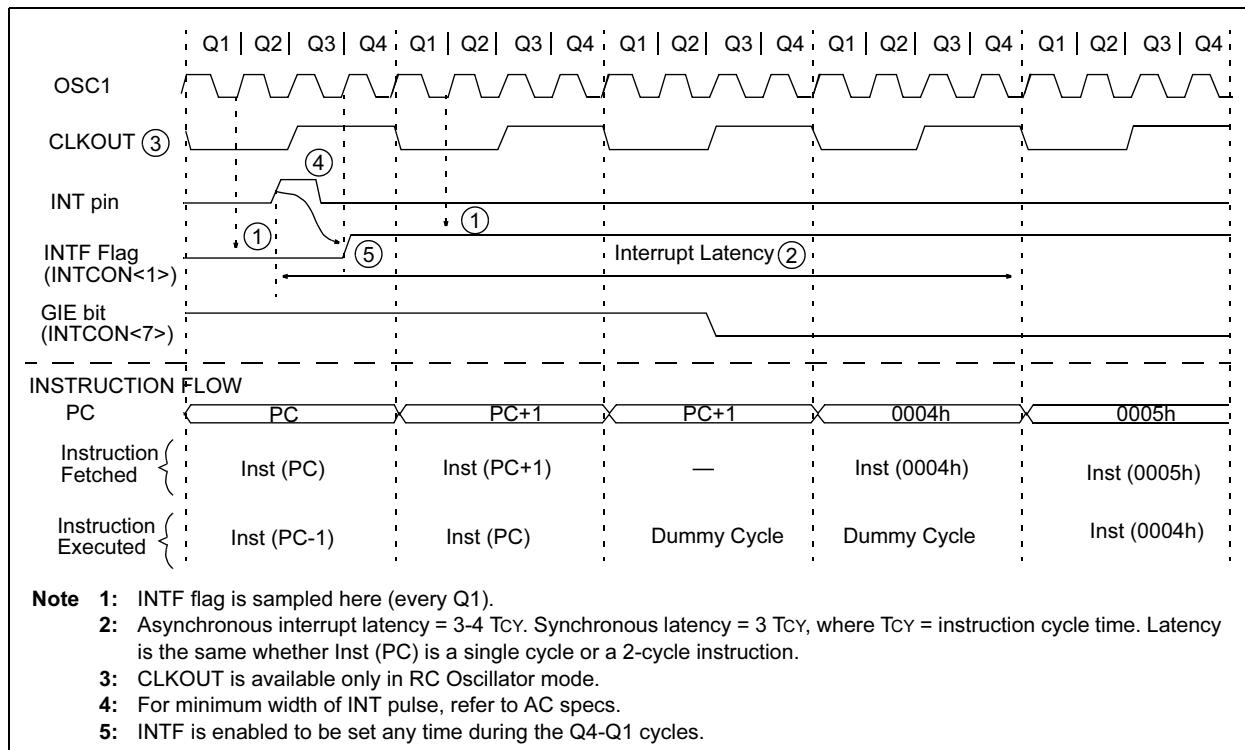


TABLE 9-8: SUMMARY OF INTERRUPT REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD	Value on all other RESETS
0Bh, 8Bh	INTCON	GIE	PEIE	TOIE	INTE	GPIE	TOIF	INTF	GPIF	0000 0000	0000 000u
0Ch	PIR1	EEIF	ADIF	—	—	CMIF	—	—	TMR1IF	00-- 0--0	00-- 0--0
8Ch	PIE1	EEIE	ADIE	—	—	CMIE	—	—	TMR1IE	00-- 0--0	00-- 0--0

Legend: x = unknown, u = unchanged, - = unimplemented read as '0', q = value depends upon condition.

Shaded cells are not used by the Interrupt module.

9.5 Context Saving During Interrupts

During an interrupt, only the return PC value is saved on the stack. Typically, users may wish to save key registers during an interrupt, e.g., W register and STATUS register. This must be implemented in software.

Example 9-2 stores and restores the STATUS and W registers. The user register, W_TEMP, must be defined in both banks and must be defined at the same offset from the bank base address (i.e., W_TEMP is defined at 0x20 in Bank 0 and it must also be defined at 0xA0 in Bank 1). The user register, STATUS_TEMP, must be defined in Bank 0. The Example 9-2:

- Stores the W register
- Stores the STATUS register in Bank 0
- Executes the ISR code
- Restores the STATUS (and bank select bit register)
- Restores the W register

EXAMPLE 9-2: SAVING THE STATUS AND W REGISTERS IN RAM

```

MOVWF W_TEMP      ;copy W to temp register,
                   ;could be in either bank
SWAPF STATUS,W    ;swap status to be saved into W
BCF   STATUS,RPO  ;change to bank 0 regardless of
                  ;current bank
MOVWF STATUS_TEMP ;save status to bank 0 register
:
:(ISR)
:
SWAPP STATUS_TEMP,W;swap STATUS_TEMP register into
                   ;W, sets bank to original state
MOVWF STATUS        ;move W into STATUS register
SWAPP W_TEMP,F     ;swap W_TEMP
SWAPP W_TEMP,W     ;swap W_TEMP into W

```

9.6 Watchdog Timer (WDT)

The Watchdog Timer is a free running, on-chip RC oscillator, which requires no external components. This RC oscillator is separate from the external RC oscillator of the CLKIN pin and INTOSC. That means that the WDT will run, even if the clock on the OSC1 and OSC2 pins of the device has been stopped (for example, by execution of a SLEEP instruction). During normal operation, a WDT time-out generates a device RESET. If the device is in SLEEP mode, a WDT time-out causes the device to wake-up and continue with normal operation. The WDT can be permanently disabled by programming the configuration bit WDTE as clear (Section 9.1).

9.6.1 WDT PERIOD

The WDT has a nominal time-out period of 18 ms, (with no prescaler). The time-out periods vary with temperature, VDD and process variations from part to part (see DC specs). If longer time-out periods are desired, a prescaler with a division ratio of up to 1:128 can be assigned to the WDT under software control by writing to the OPTION register. Thus, time-out periods up to 2.3 seconds can be realized.

The CLRWD and SLEEP instructions clear the WDT and the prescaler, if assigned to the WDT, and prevent it from timing out and generating a device RESET.

The TO bit in the STATUS register will be cleared upon a Watchdog Timer time-out.

9.6.2 WDT PROGRAMMING CONSIDERATIONS

It should also be taken in account that under worst case conditions (i.e., VDD = Min., Temperature = Max., Max. WDT prescaler) it may take several seconds before a WDT time-out occurs.

FIGURE 9-12: WATCHDOG TIMER BLOCK DIAGRAM

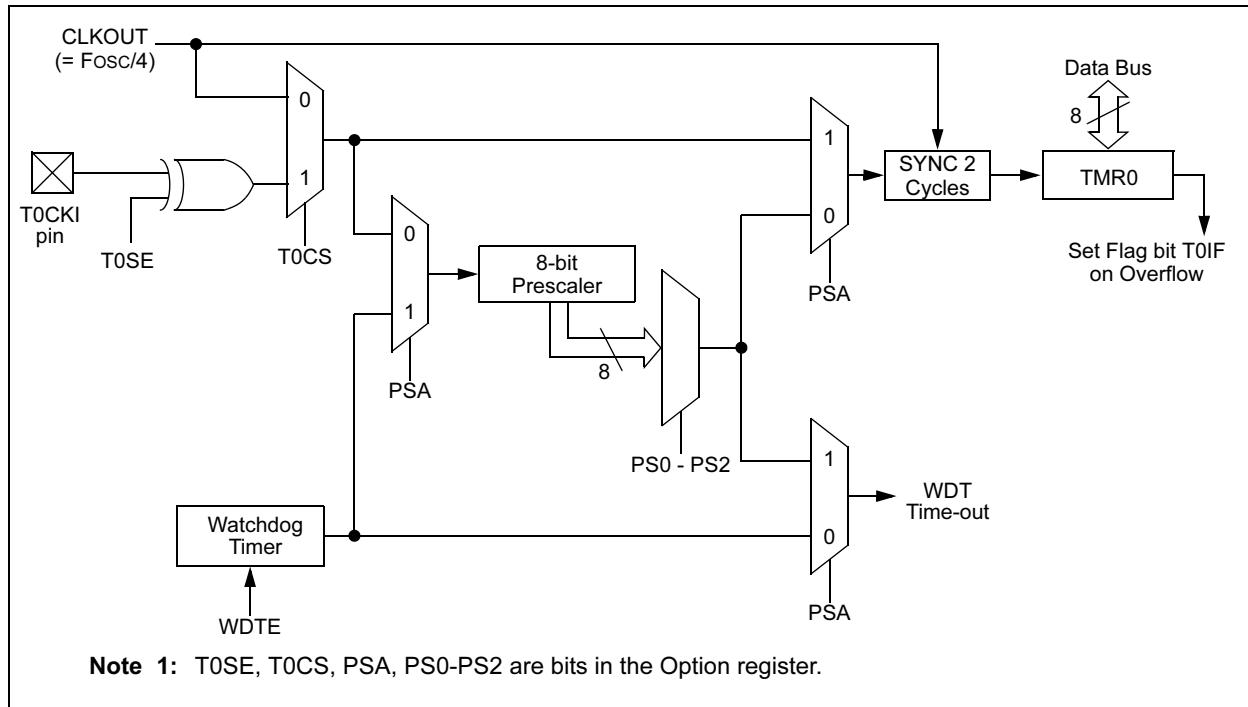


TABLE 9-9: SUMMARY OF WATCHDOG TIMER REGISTERS

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Value on POR, BOD	Value on all other RESETS
81h	OPTION_REG	GPPU	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0	1111 1111	1111 1111
2007h	Config. bits	CP	BODEN	MCLRE	PWRTE	WDTE	F0SC2	F0SC1	F0SC0	uuuu uuuu	uuuu uuuu

Legend: u = Unchanged, shaded cells are not used by the Watchdog Timer.

9.7 Power-Down Mode (SLEEP)

The Power-down mode is entered by executing a SLEEP instruction.

If the Watchdog Timer is enabled:

- WDT will be cleared but keeps running
- PD bit in the STATUS register is cleared
- TO bit is set
- Oscillator driver is turned off
- I/O ports maintain the status they had before SLEEP was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode, all I/O pins should be either at VDD, or VSS, with no external circuitry drawing current from the I/O pin and the comparators and CVREF should be disabled. I/O pins that are hi-impedance inputs should be pulled high or low externally to avoid switching currents caused by floating inputs. The T0CKI input should also be at VDD or Vss for lowest current consumption. The contribution from on-chip pull-ups on GPIO should be considered.

The MCLR pin must be at a logic high level (VIHMC).

Note: It should be noted that a RESET generated by a WDT time-out does not drive MCLR pin low.

The first event will cause a device RESET. The two latter events are considered a continuation of program execution. The TO and PD bits in the STATUS register can be used to determine the cause of device RESET. The PD bit, which is set on power-up, is cleared when SLEEP is invoked. TO bit is cleared if WDT Wake-up occurred.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction, then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have an NOP after the SLEEP instruction.

Note: If the global interrupts are disabled (GIE is cleared), but any interrupt source has both its interrupt enable bit and the corresponding interrupt flag bits set, the device will immediately wake-up from SLEEP. The SLEEP instruction is completely executed.

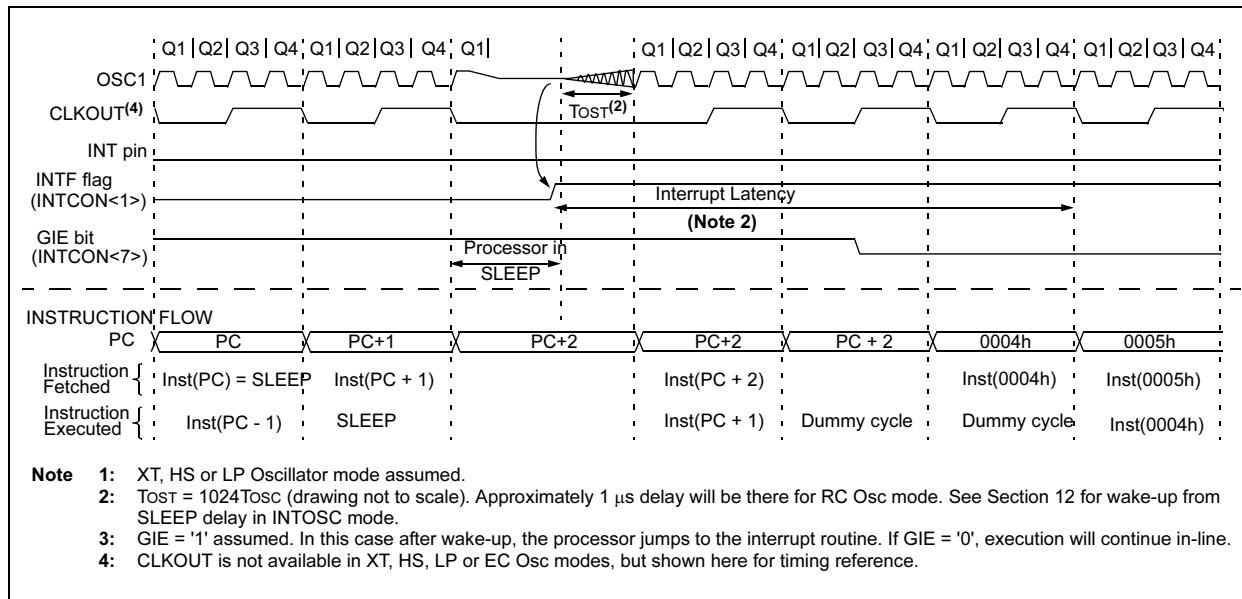
The WDT is cleared when the device wakes up from SLEEP, regardless of the source of wake-up.

9.7.1 WAKE-UP FROM SLEEP

The device can wake-up from SLEEP through one of the following events:

1. External RESET input on MCLR pin
2. Watchdog Timer Wake-up (if WDT was enabled)
3. Interrupt from GP2/INT pin, GPIO change, or a peripheral interrupt.

FIGURE 9-13: WAKE-UP FROM SLEEP THROUGH INTERRUPT



9.8 Code Protection

If the code protection bit(s) have not been programmed, the on-chip program memory can be read out for verification purposes.

Note: The entire data EEPROM and FLASH program memory will be erased when the code protection is turned off. The INTOSC calibration data is also erased. See PIC12F629/675 Programming Specification for more information.

9.9 ID Locations

Four memory locations (2000h-2003h) are designated as ID locations where the user can store checksum or other code identification numbers. These locations are not accessible during normal execution but are readable and writable during Program/Verify. Only the Least Significant 7 bits of the ID locations are used.

9.10 In-Circuit Serial Programming

The PIC12F629/675 microcontrollers can be serially programmed while in the end application circuit. This is simply done with two lines for clock and data, and three other lines for:

- power
- ground
- programming voltage

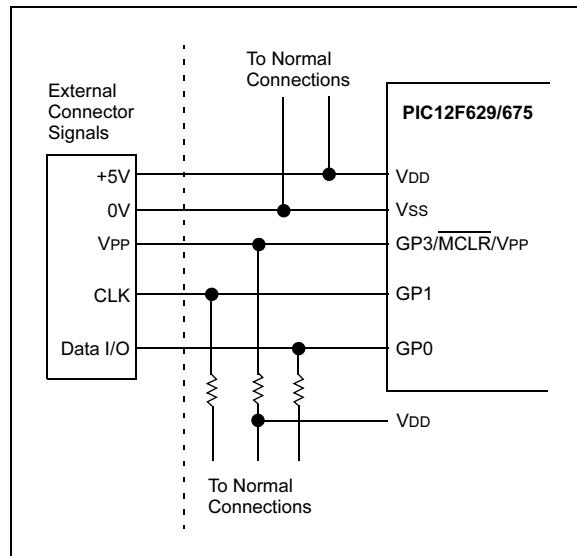
This allows customers to manufacture boards with unprogrammed devices, and then program the microcontroller just before shipping the product. This also allows the most recent firmware or a custom firmware to be programmed.

The device is placed into a Program/Verify mode by holding the GP0 and GP1 pins low, while raising the MCLR (VPP) pin from VIL to VIHH (see Programming Specification). GP0 becomes the programming data and GP1 becomes the programming clock. Both GP0 and GP1 are Schmitt Trigger inputs in this mode.

After RESET, to place the device into Programming/Verify mode, the program counter (PC) is at location 00h. A 6-bit command is then supplied to the device. Depending on the command, 14-bits of program data are then supplied to or from the device, depending on whether the command was a load or a read. For complete details of serial programming, please refer to the Programming Specifications.

A typical In-Circuit Serial Programming connection is shown in Figure 9-14.

FIGURE 9-14: TYPICAL IN-CIRCUIT SERIAL PROGRAMMING CONNECTION



9.11 In-Circuit Debugger

Since in-circuit debugging requires the loss of clock, data and MCLR pins, MPLAB® ICD 2 development with an 8-pin device is not practical. A special 14-pin PIC12F675-ICD device is used with MPLAB ICD 2 to provide separate clock, data and MCLR pins and frees all normally available pins to the user.

This special ICD device is mounted on the top of the header and its signals are routed to the MPLAB ICD 2 connector. On the bottom of the header is an 8-pin socket that plugs into the user's target via the 8-pin stand-off connector.

When the ICD pin on the PIC12F675-ICD device is held low, the In-Circuit Debugger functionality is enabled. This function allows simple debugging functions when used with MPLAB ICD 2. When the microcontroller has this feature enabled, some of the resources are not available for general use. Table 9-10 shows which features are consumed by the background debugger:

TABLE 9-10: DEBUGGER RESOURCES

I/O pins	ICDCLK, ICDDATA
Stack	1 level
Program Memory	Address 0h must be NOP 300h - 3FEh

For more information, see 8-Pin MPLAB ICD 2 Header Information Sheet (DS51292) available on Microchip's website (www.microchip.com).

PIC12F629/675

NOTES:

10.0 INSTRUCTION SET SUMMARY

The PIC12F629/675 instruction set is highly orthogonal and is comprised of three basic categories:

- **Byte-oriented** operations
- **Bit-oriented** operations
- **Literal and control** operations

Each PIC12F629/675 instruction is a 14-bit word divided into an **opcode**, which specifies the instruction type, and one or more **operands**, which further specify the operation of the instruction. The formats for each of the categories is presented in Figure 10-1, while the various opcode fields are summarized in Table 10-1.

Table 10-2 lists the instructions recognized by the MPASM™ assembler. A complete description of each instruction is also available in the PICmicro™ Mid-Range Reference Manual (DS33023).

For **byte-oriented** instructions, ‘f’ represents a file register designator and ‘d’ represents a destination designator. The file register designator specifies which file register is to be used by the instruction.

The destination designator specifies where the result of the operation is to be placed. If ‘d’ is zero, the result is placed in the W register. If ‘d’ is one, the result is placed in the file register specified in the instruction.

For **bit-oriented** instructions, ‘b’ represents a bit field designator, which selects the bit affected by the operation, while ‘f’ represents the address of the file in which the bit is located.

For **literal and control** operations, ‘k’ represents an 8-bit or 11-bit constant, or literal value.

One instruction cycle consists of four oscillator periods; for an oscillator frequency of 4 MHz, this gives a normal instruction execution time of 1 μ s. All instructions are executed within a single instruction cycle, unless a conditional test is true, or the program counter is changed as a result of an instruction. When this occurs, the execution takes two instruction cycles, with the second cycle executed as a NOP.

Note: To maintain upward compatibility with future products, do not use the OPTION and TRISIO instructions.

All instruction examples use the format ‘0xhh’ to represent a hexadecimal number, where ‘h’ signifies a hexadecimal digit.

10.1 READ-MODIFY-WRITE OPERATIONS

Any instruction that specifies a file register as part of the instruction performs a Read-Modify-Write (R-M-W) operation. The register is read, the data is modified, and the result is stored according to either the instruction, or the destination designator ‘d’. A read operation is performed on a register even if the instruction writes to that register.

For example, a CLRF GPIO instruction will read GPIO, clear all the data bits, then write the result back to GPIO. This example would have the unintended result that the condition that sets the GPIF flag would be cleared.

TABLE 10-1: OPCODE FIELD DESCRIPTIONS

Field	Description
f	Register file address (0x00 to 0x7F)
w	Working register (accumulator)
b	Bit address within an 8-bit file register
k	Literal field, constant data or label
x	Don't care location (= 0 or 1). The assembler will generate code with x = 0. It is the recommended form of use for compatibility with all Microchip software tools.
d	Destination select; d = 0: store result in W, d = 1: store result in file register f. Default is d = 1.
PC	Program Counter
TO	Time-out bit
PD	Power-down bit

FIGURE 10-1: GENERAL FORMAT FOR INSTRUCTIONS

Byte-oriented file register operations

13	8	7	6	0
OPCODE	d		f (FILE #)	

d = 0 for destination W
d = 1 for destination f
f = 7-bit file register address

Bit-oriented file register operations

13	10	9	7	6	0
OPCODE	b (BIT #)		f (FILE #)		

b = 3-bit bit address
f = 7-bit file register address

Literal and control operations

General

13	8	7	0
OPCODE		k (literal)	

k = 8-bit immediate value

CALL and GOTO instructions only

13	11	10	0
OPCODE		k (literal)	

k = 11-bit immediate value

PIC12F629/675

TABLE 10-2: PIC12F629/675 INSTRUCTION SET

Mnemonic, Operands	Description	Cycles	14-Bit Opcode		Status Affected	Notes
			MSb	Lsb		
BYTE-ORIENTED FILE REGISTER OPERATIONS						
ADDWF	f, d	Add W and f	1	00 0111 dfff ffff	C,DC,Z	1,2
ANDWF	f, d	AND W with f	1	00 0101 dfff ffff	Z	1,2
CLRF	f	Clear f	1	00 0001 lfff ffff	Z	2
CLRW	-	Clear W	1	00 0001 0xxx xxxx	Z	
COMF	f, d	Complement f	1	00 1001 dfff ffff	Z	1,2
DECFSZ	f, d	Decrement f, Skip if 0	1(2)	00 1011 dfff ffff		1,2,3
INCF	f, d	Increment f	1	00 1010 dfff ffff	Z	1,2
INCFSZ	f, d	Increment f, Skip if 0	1(2)	00 1111 dfff ffff		1,2,3
IOWF	f, d	Inclusive OR W with f	1	00 0100 dfff ffff	Z	1,2
MOVF	f, d	Move f	1	00 1000 dfff ffff	Z	1,2
MOVWF	f	Move W to f	1	00 0000 1fff ffff		
NOP	-	No Operation	1	00 0000 0xx0 0000		
RLF	f, d	Rotate Left f through Carry	1	00 1101 dfff ffff	C	1,2
RRF	f, d	Rotate Right f through Carry	1	00 1100 dfff ffff	C	1,2
SUBWF	f, d	Subtract W from f	1	00 0010 dfff ffff	C,DC,Z	1,2
SWAPF	f, d	Swap nibbles in f	1	00 1110 dfff ffff		1,2
XORWF	f, d	Exclusive OR W with f	1	00 0110 dfff ffff	Z	1,2
BIT-ORIENTED FILE REGISTER OPERATIONS						
BCF	f, b	Bit Clear f	1	01 00bb bfff ffff		1,2
BSF	f, b	Bit Set f	1	01 01bb bfff ffff		1,2
BTFSZ	f, b	Bit Test f, Skip if Clear	1(2)	01 10bb bfff ffff		3
BTFSZ	f, b	Bit Test f, Skip if Set	1(2)	01 11bb bfff ffff		3
LITERAL AND CONTROL OPERATIONS						
ADDLW	k	Add literal and W	1	11 111x kkkk kkkk	C,DC,Z	
ANDLW	k	AND literal with W	1	11 1001 kkkk kkkk	Z	
CALL	k	Call subroutine	2	10 0kkk kkkk kkkk		
CLRWD	-	Clear Watchdog Timer	1	00 0000 0110 0100	<u>TO</u> , <u>PD</u>	
GOTO	k	Go to address	2	10 1kkk kkkk kkkk		
IORLW	k	Inclusive OR literal with W	1	11 1000 kkkk kkkk	Z	
MOVLW	k	Move literal to W	1	11 00xx kkkk kkkk		
RETFIE	-	Return from interrupt	2	00 0000 0000 1001		
RETLW	k	Return with literal in W	2	11 01xx kkkk kkkk		
RETURN	-	Return from Subroutine	2	00 0000 0000 1000		
SLEEP	-	Go into Standby mode	1	00 0000 0110 0011	<u>TO</u> , <u>PD</u>	
SUBLW	k	Subtract W from literal	1	11 110x kkkk kkkk	C,DC,Z	
XORLW	k	Exclusive OR literal with W	1	11 1010 kkkk kkkk	Z	

- Note 1:** When an I/O register is modified as a function of itself (e.g., MOVF GPIO, 1), the value used will be that value present on the pins themselves. For example, if the data latch is '1' for a pin configured as input and is driven low by an external device, the data will be written back with a '0'.
- 2:** If this instruction is executed on the TMR0 register (and, where applicable, d = 1), the prescaler will be cleared if assigned to the Timer0 module.
- 3:** If Program Counter (PC) is modified, or a conditional test is true, the instruction requires two cycles. The second cycle is executed as a NOP.

Note: Additional information on the mid-range instruction set is available in the PICmicro™ Mid-Range MCU Family Reference Manual (DS33023).

10.2 Instruction Descriptions

ADDLW Add Literal and W

Syntax:	[label] ADDLW k
Operands:	$0 \leq k \leq 255$
Operation:	$(W) + k \rightarrow (W)$
Status Affected:	C, DC, Z
Description:	The contents of the W register are added to the eight-bit literal 'k' and the result is placed in the W register.

BCF Bit Clear f

Syntax:	[label] BCF f,b
Operands:	$0 \leq f \leq 127$ $0 \leq b \leq 7$
Operation:	$0 \rightarrow (f)$
Status Affected:	None
Description:	Bit 'b' in register 'f' is cleared.

ADDWF Add W and f

Syntax:	[label] ADDWF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(W) + (f) \rightarrow (\text{destination})$
Status Affected:	C, DC, Z
Description:	Add the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

BSF Bit Set f

Syntax:	[label] BSF f,b
Operands:	$0 \leq f \leq 127$ $0 \leq b \leq 7$
Operation:	$1 \rightarrow (f)$
Status Affected:	None
Description:	Bit 'b' in register 'f' is set.

ANDLW AND Literal with W

Syntax:	[label] ANDLW k
Operands:	$0 \leq k \leq 255$
Operation:	$(W) .AND. (k) \rightarrow (W)$
Status Affected:	Z
Description:	The contents of W register are AND'ed with the eight-bit literal 'k'. The result is placed in the W register.

BTFSS Bit Test f, Skip if Set

Syntax:	[label] BTFSS f,b
Operands:	$0 \leq f \leq 127$ $0 \leq b < 7$
Operation:	skip if $(f) = 1$
Status Affected:	None
Description:	If bit 'b' in register 'f' is '0', the next instruction is executed. If bit 'b' is '1', then the next instruction is discarded and a NOP is executed instead, making this a 2TCY instruction.

ANDWF AND W with f

Syntax:	[label] ANDWF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(W) .AND. (f) \rightarrow (\text{destination})$
Status Affected:	Z
Description:	AND the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

BTFSC Bit Test, Skip if Clear

Syntax:	[label] BTFSC f,b
Operands:	$0 \leq f \leq 127$ $0 \leq b \leq 7$
Operation:	skip if $(f) = 0$
Status Affected:	None
Description:	If bit 'b' in register 'f' is '1', the next instruction is executed. If bit 'b', in register 'f', is '0', the next instruction is discarded, and a NOP is executed instead, making this a 2TCY instruction.

PIC12F629/675

CALL	Call Subroutine	CLRWDT	Clear Watchdog Timer
Syntax:	[<i>label</i>] CALL k	Syntax:	[<i>label</i>] CLRWDT
Operands:	0 ≤ k ≤ 2047	Operands:	None
Operation:	(PC)+ 1 → TOS, k → PC<10:0>, (PCLATH<4:3>) → PC<12:11>	Operation:	00h → WDT 0 → <u>WDT prescaler</u> , 1 → <u>TO</u> 1 → <u>PD</u>
Status Affected:	None	Status Affected:	<u>TO</u> , <u>PD</u>
Description:	Call Subroutine. First, return address (PC+1) is pushed onto the stack. The eleven-bit immediate address is loaded into PC bits <10:0>. The upper bits of the PC are loaded from PCLATH. CALL is a two-cycle instruction.	Description:	CLRWDT instruction resets the Watchdog Timer. It also resets the prescaler of the WDT. STATUS bits <u>TO</u> and <u>PD</u> are set.
CLRF	Clear f	COMF	Complement f
Syntax:	[<i>label</i>] CLRF f	Syntax:	[<i>label</i>] COMF f,d
Operands:	0 ≤ f ≤ 127	Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	00h → (f) 1 → Z	Operation:	(f̄) → (destination)
Status Affected:	Z	Status Affected:	Z
Description:	The contents of register 'f' are cleared and the Z bit is set.	Description:	The contents of register 'f' are complemented. If 'd' is 0, the result is stored in W. If 'd' is 1, the result is stored back in register 'f'.
CLRW	Clear W	DEC F	Decrement f
Syntax:	[<i>label</i>] CLRW	Syntax:	[<i>label</i>] DEC F,d
Operands:	None	Operands:	0 ≤ f ≤ 127 d ∈ [0,1]
Operation:	00h → (W) 1 → Z	Operation:	(f) - 1 → (destination)
Status Affected:	Z	Status Affected:	Z
Description:	W register is cleared. Zero bit (Z) is set.	Description:	Decrement register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

DECFSZ	Decrement f, Skip if 0
Syntax:	[<i>label</i>] DECFSZ f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(f) - 1 \rightarrow (\text{destination})$, skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are decremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'. If the result is 1, the next instruction is executed. If the result is 0, then a NOP is executed instead, making it a 2TCY instruction.

INCFSZ	Increment f, Skip if 0
Syntax:	[<i>label</i>] INCFSZ f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(f) + 1 \rightarrow (\text{destination})$, skip if result = 0
Status Affected:	None
Description:	The contents of register 'f' are incremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'. If the result is 1, the next instruction is executed. If the result is 0, a NOP is executed instead, making it a 2TCY instruction.

GOTO	Unconditional Branch
Syntax:	[<i>label</i>] GOTO k
Operands:	$0 \leq k \leq 2047$
Operation:	$k \rightarrow \text{PC} <10:0>$ $\text{PCLATH} <4:3> \rightarrow \text{PC} <12:11>$
Status Affected:	None
Description:	GOTO is an unconditional branch. The eleven-bit immediate value is loaded into PC bits <10:0>. The upper bits of PC are loaded from PCLATH<4:3>. GOTO is a two-cycle instruction.

IORLW	Inclusive OR Literal with W
Syntax:	[<i>label</i>] IORLW k
Operands:	$0 \leq k \leq 255$
Operation:	$(W) .\text{OR. } k \rightarrow (W)$
Status Affected:	Z
Description:	The contents of the W register are OR'ed with the eight-bit literal 'k'. The result is placed in the W register.

INCF	Increment f
Syntax:	[<i>label</i>] INCF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(f) + 1 \rightarrow (\text{destination})$
Status Affected:	Z
Description:	The contents of register 'f' are incremented. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.

IORWF	Inclusive OR W with f
Syntax:	[<i>label</i>] IORWF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(W) .\text{OR. } (f) \rightarrow (\text{destination})$
Status Affected:	Z
Description:	Inclusive OR the W register with register 'f'. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'.

PIC12F629/675

MOVF	Move f
Syntax:	[<i>label</i>] MOVF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(f) \rightarrow (\text{destination})$
Status Affected:	Z
Description:	The contents of register f are moved to a destination dependant upon the status of d. If d = 0, destination is W register. If d = 1, the destination is file register f itself. d = 1 is useful to test a file register, since status flag Z is affected.

MOVLW	Move Literal to W
Syntax:	[<i>label</i>] MOVLW k
Operands:	$0 \leq k \leq 255$
Operation:	$k \rightarrow (W)$
Status Affected:	None
Description:	The eight-bit literal 'k' is loaded into W register. The don't cares will assemble as 0's.

MOVWF	Move W to f
Syntax:	[<i>label</i>] MOVWF f
Operands:	$0 \leq f \leq 127$
Operation:	$(W) \rightarrow (f)$
Status Affected:	None
Description:	Move data from W register to register 'f'.

NOP	No Operation
Syntax:	[<i>label</i>] NOP
Operands:	None
Operation:	No operation
Status Affected:	None
Description:	No operation.

RETFIE	Return from Interrupt
Syntax:	[<i>label</i>] RETFIE
Operands:	None
Operation:	TOS \rightarrow PC, 1 \rightarrow GIE
Status Affected:	None

RETLW	Return with Literal in W
Syntax:	[<i>label</i>] RETLW k
Operands:	$0 \leq k \leq 255$
Operation:	$k \rightarrow (W);$ TOS \rightarrow PC
Status Affected:	None
Description:	The W register is loaded with the eight-bit literal 'k'. The program counter is loaded from the top of the stack (the return address). This is a two-cycle instruction.

RLF	Rotate Left f through Carry
Syntax:	[<i>label</i>] RLF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	See description below
Status Affected:	C
Description:	The contents of register 'f' are rotated one bit to the left through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is stored back in register 'f'. 

SLEEP	
Syntax:	[<i>label</i>] SLEEP
Operands:	None
Operation:	$00h \rightarrow \text{WDT}$, $0 \rightarrow \text{WDT prescaler}$, $1 \rightarrow \overline{\text{TO}}$, $0 \rightarrow \text{PD}$
Status Affected:	$\overline{\text{TO}}, \overline{\text{PD}}$
Description:	The power-down STATUS bit, PD is cleared. Time-out STATUS bit, TO is set. Watchdog Timer and its prescaler are cleared. The processor is put into SLEEP mode with the oscillator stopped.

RETURN	Return from Subroutine
Syntax:	[<i>label</i>] RETURN
Operands:	None
Operation:	TOS \rightarrow PC
Status Affected:	None
Description:	Return from subroutine. The stack is POPped and the top of the stack (TOS) is loaded into the program counter. This is a two-cycle instruction.

SUBLW	Subtract W from Literal
Syntax:	[<i>label</i>] SUBLW k
Operands:	$0 \leq k \leq 255$
Operation:	$k - (W) \rightarrow (W)$
Status Affected:	C, DC, Z
Description:	The W register is subtracted (2's complement method) from the eight-bit literal 'k'. The result is placed in the W register.

RRF	Rotate Right f through Carry
Syntax:	[<i>label</i>] RRF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	See description below
Status Affected:	C
Description:	The contents of register 'f' are rotated one bit to the right through the Carry Flag. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed back in register 'f'. 

SUBWF	Subtract W from f
Syntax:	[<i>label</i>] SUBWF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(f) - (W) \rightarrow (\text{destination})$
Status Affected:	C, DC, Z
Description:	Subtract (2's complement method) W register from register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.

PIC12F629/675

SWAPF	Swap Nibbles in f	XORWF	Exclusive OR W with f
Syntax:	[label] SWAPF f,d	Syntax:	[label] XORWF f,d
Operands:	$0 \leq f \leq 127$ $d \in [0,1]$	Operands:	$0 \leq f \leq 127$ $d \in [0,1]$
Operation:	$(f<3:0>) \rightarrow (\text{destination}<7:4>),$ $(f<7:4>) \rightarrow (\text{destination}<3:0>)$	Operation:	$(W) .XOR. (f) \rightarrow (\text{destination})$
Status Affected:	None	Status Affected:	Z
Description:	The upper and lower nibbles of register 'f' are exchanged. If 'd' is 0, the result is placed in the W register. If 'd' is 1, the result is placed in register 'f'.	Description:	Exclusive OR the contents of the W register with register 'f'. If 'd' is 0, the result is stored in the W register. If 'd' is 1, the result is stored back in register 'f'.
XORLW	Exclusive OR Literal with W		
Syntax:	[label] XORLW k		
Operands:	$0 \leq k \leq 255$		
Operation:	$(W) .XOR. k \rightarrow (W)$		
Status Affected:	Z		
Description:	The contents of the W register are XOR'ed with the eight-bit literal 'k'. The result is placed in the W register.		

11.0 DEVELOPMENT SUPPORT

The PICmicro® microcontrollers are supported with a full range of hardware and software development tools:

- Integrated Development Environment
 - MPLAB® IDE Software
- Assemblers/Compilers/Linkers
 - MPASM™ Assembler
 - MPLAB C17 and MPLAB C18 C Compilers
 - MPLINK™ Object Linker/
MPLIB™ Object Librarian
 - MPLAB C30 C Compiler
 - MPLAB ASM30 Assembler/Linker/Library
- Simulators
 - MPLAB SIM Software Simulator
 - MPLAB dsPIC30 Software Simulator
- Emulators
 - MPLAB ICE 2000 In-Circuit Emulator
 - MPLAB ICE 4000 In-Circuit Emulator
- In-Circuit Debugger
 - MPLAB ICD 2
- Device Programmers
 - PRO MATE® II Universal Device Programmer
 - PICSTART® Plus Development Programmer
- Low Cost Demonstration Boards
 - PICDEM™ 1 Demonstration Board
 - PICDEM.net™ Demonstration Board
 - PICDEM 2 Plus Demonstration Board
 - PICDEM 3 Demonstration Board
 - PICDEM 17 Demonstration Board
 - PICDEM 18R Demonstration Board
 - PICDEM LIN Demonstration Board
 - PICDEM USB Demonstration Board
- Evaluation Kits
 - KEELOQ®
 - PICDEM MSC
 - microID®
 - CAN
 - PowerSmart®
 - Analog

11.1 MPLAB Integrated Development Environment Software

The MPLAB IDE software brings an ease of software development previously unseen in the 8/16-bit microcontroller market. The MPLAB IDE is a Windows® based application that contains:

- An interface to debugging tools
 - simulator
 - programmer (sold separately)
 - emulator (sold separately)
 - in-circuit debugger (sold separately)
- A full-featured editor with color coded context
- A multiple project manager
- Customizable data windows with direct edit of contents
- High level source code debugging
- Mouse over variable inspection
- Extensive on-line help

The MPLAB IDE allows you to:

- Edit your source files (either assembly or C)
- One touch assemble (or compile) and download to PICmicro emulator and simulator tools (automatically updates all project information)
- Debug using:
 - source files (assembly or C)
 - absolute listing file (mixed assembly and C)
 - machine code

MPLAB IDE supports multiple debugging tools in a single development paradigm, from the cost effective simulators, through low cost in-circuit debuggers, to full-featured emulators. This eliminates the learning curve when upgrading to tools with increasing flexibility and power.

11.2 MPASM Assembler

The MPASM assembler is a full-featured, universal macro assembler for all PICmicro MCUs.

The MPASM assembler generates relocatable object files for the MPLINK object linker, Intel® standard HEX files, MAP files to detail memory usage and symbol reference, absolute LST files that contains source lines and generated machine code and COFF files for debugging.

The MPASM assembler features include:

- Integration into MPLAB IDE projects
- User defined macros to streamline assembly code
- Conditional assembly for multi-purpose source files
- Directives that allow complete control over the assembly process

11.3 MPLAB C17 and MPLAB C18 C Compilers

The MPLAB C17 and MPLAB C18 Code Development Systems are complete ANSI C compilers for Microchip's PIC17CXXX and PIC18CXXX family of microcontrollers. These compilers provide powerful integration capabilities, superior code optimization and ease of use not found with other compilers.

For easy source level debugging, the compilers provide symbol information that is optimized to the MPLAB IDE debugger.

11.4 MPLINK Object Linker/ MPLIB Object Librarian

The MPLINK object linker combines relocatable objects created by the MPASM assembler and the MPLAB C17 and MPLAB C18 C compilers. It can link relocatable objects from pre-compiled libraries, using directives from a linker script.

The MPLIB object librarian manages the creation and modification of library files of pre-compiled code. When a routine from a library is called from a source file, only the modules that contain that routine will be linked in with the application. This allows large libraries to be used efficiently in many different applications.

The object linker/library features include:

- Efficient linking of single libraries instead of many smaller files
- Enhanced code maintainability by grouping related modules together
- Flexible creation of libraries with easy module listing, replacement, deletion and extraction

11.5 MPLAB C30 C Compiler

The MPLAB C30 C compiler is a full-featured, ANSI compliant, optimizing compiler that translates standard ANSI C programs into dsPIC30F assembly language source. The compiler also supports many command-line options and language extensions to take full advantage of the dsPIC30F device hardware capabilities, and afford fine control of the compiler code generator.

MPLAB C30 is distributed with a complete ANSI C standard library. All library functions have been validated and conform to the ANSI C library standard. The library includes functions for string manipulation, dynamic memory allocation, data conversion, time-keeping, and math functions (trigonometric, exponential and hyperbolic). The compiler provides symbolic information for high level source debugging with the MPLAB IDE.

11.6 MPLAB ASM30 Assembler, Linker, and Librarian

MPLAB ASM30 assembler produces relocatable machine code from symbolic assembly language for dsPIC30F devices. MPLAB C30 compiler uses the assembler to produce its object file. The assembler generates relocatable object files that can then be archived or linked with other relocatable object files and archives to create an executable file. Notable features of the assembler include:

- Support for the entire dsPIC30F instruction set
- Support for fixed-point and floating-point data
- Command line interface
- Rich directive set
- Flexible macro language
- MPLAB IDE compatibility

11.7 MPLAB SIM Software Simulator

The MPLAB SIM software simulator allows code development in a PC hosted environment by simulating the PICmicro series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user defined key press, to any pin. The execution can be performed in Single-Step, Execute Until Break, or Trace mode.

The MPLAB SIM simulator fully supports symbolic debugging using the MPLAB C17 and MPLAB C18 C Compilers, as well as the MPASM assembler. The software simulator offers the flexibility to develop and debug code outside of the laboratory environment, making it an excellent, economical software development tool.

11.8 MPLAB SIM30 Software Simulator

The MPLAB SIM30 software simulator allows code development in a PC hosted environment by simulating the dsPIC30F series microcontrollers on an instruction level. On any given instruction, the data areas can be examined or modified and stimuli can be applied from a file, or user defined key press, to any of the pins.

The MPLAB SIM30 simulator fully supports symbolic debugging using the MPLAB C30 C Compiler and MPLAB ASM30 assembler. The simulator runs in either a Command Line mode for automated tasks, or from MPLAB IDE. This high speed simulator is designed to debug, analyze and optimize time intensive DSP routines.

11.9 MPLAB ICE 2000 High Performance Universal In-Circuit Emulator

The MPLAB ICE 2000 universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for PICmicro microcontrollers. Software control of the MPLAB ICE 2000 in-circuit emulator is advanced by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICE 2000 is a full-featured emulator system with enhanced trace, trigger and data monitoring features. Interchangeable processor modules allow the system to be easily reconfigured for emulation of different processors. The universal architecture of the MPLAB ICE in-circuit emulator allows expansion to support new PICmicro microcontrollers.

The MPLAB ICE 2000 in-circuit emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft® Windows 32-bit operating system were chosen to best make these features available in a simple, unified application.

11.10 MPLAB ICE 4000 High Performance Universal In-Circuit Emulator

The MPLAB ICE 4000 universal in-circuit emulator is intended to provide the product development engineer with a complete microcontroller design tool set for high-end PICmicro microcontrollers. Software control of the MPLAB ICE in-circuit emulator is provided by the MPLAB Integrated Development Environment, which allows editing, building, downloading and source debugging from a single environment.

The MPLAB ICD 4000 is a premium emulator system, providing the features of MPLAB ICE 2000, but with increased emulation memory and high speed performance for dsPIC30F and PIC18XXXX devices. Its advanced emulator features include complex triggering and timing, up to 2 Mb of emulation memory, and the ability to view variables in real-time.

The MPLAB ICE 4000 in-circuit emulator system has been designed as a real-time emulation system with advanced features that are typically found on more expensive development tools. The PC platform and Microsoft Windows 32-bit operating system were chosen to best make these features available in a simple, unified application.

11.11 MPLAB ICD 2 In-Circuit Debugger

Microchip's In-Circuit Debugger, MPLAB ICD 2, is a powerful, low cost, run-time development tool, connecting to the host PC via an RS-232 or high speed USB interface. This tool is based on the FLASH PICmicro MCUs and can be used to develop for these and other PICmicro microcontrollers. The MPLAB ICD 2 utilizes the in-circuit debugging capability built into the FLASH devices. This feature, along with Microchip's In-Circuit Serial Programming™ (ICSP™) protocol, offers cost effective in-circuit FLASH debugging from the graphical user interface of the MPLAB Integrated Development Environment. This enables a designer to develop and debug source code by setting breakpoints, single-stepping and watching variables, CPU status and peripheral registers. Running at full speed enables testing hardware and applications in real-time. MPLAB ICD 2 also serves as a development programmer for selected PICmicro devices.

11.12 PRO MATE II Universal Device Programmer

The PRO MATE II is a universal, CE compliant device programmer with programmable voltage verification at VDDMIN and VDDMAX for maximum reliability. It features an LCD display for instructions and error messages and a modular detachable socket assembly to support various package types. In Stand-alone mode, the PRO MATE II device programmer can read, verify, and program PICmicro devices without a PC connection. It can also set code protection in this mode.

11.13 PICSTART Plus Development Programmer

The PICSTART Plus development programmer is an easy-to-use, low cost, prototype programmer. It connects to the PC via a COM (RS-232) port. MPLAB Integrated Development Environment software makes using the programmer simple and efficient. The PICSTART Plus development programmer supports most PICmicro devices up to 40 pins. Larger pin count devices, such as the PIC16C92X and PIC17C76X, may be supported with an adapter socket. The PICSTART Plus development programmer is CE compliant.

PIC12F629/675

11.14 PICDEM 1 PICmicro Demonstration Board

The PICDEM 1 demonstration board demonstrates the capabilities of the PIC16C5X (PIC16C54 to PIC16C58A), PIC16C61, PIC16C62X, PIC16C71, PIC16C8X, PIC17C42, PIC17C43 and PIC17C44. All necessary hardware and software is included to run basic demo programs. The sample microcontrollers provided with the PICDEM 1 demonstration board can be programmed with a PRO MATE II device programmer, or a PICSTART Plus development programmer. The PICDEM 1 demonstration board can be connected to the MPLAB ICE in-circuit emulator for testing. A prototype area extends the circuitry for additional application components. Features include an RS-232 interface, a potentiometer for simulated analog input, push button switches and eight LEDs.

11.15 PICDEM.net Internet/Ethernet Demonstration Board

The PICDEM.net demonstration board is an Internet/Ethernet demonstration board using the PIC18F452 microcontroller and TCP/IP firmware. The board supports any 40-pin DIP device that conforms to the standard pinout used by the PIC16F877 or PIC18C452. This kit features a user friendly TCP/IP stack, web server with HTML, a 24L256 Serial EEPROM for Xmodem download to web pages into Serial EEPROM, ICSP/MPLAB ICD 2 interface connector, an Ethernet interface, RS-232 interface, and a 16 x 2 LCD display. Also included is the book and CD-ROM "TCP/IP Lean, Web Servers for Embedded Systems," by Jeremy Bentham

11.16 PICDEM 2 Plus Demonstration Board

The PICDEM 2 Plus demonstration board supports many 18-, 28-, and 40-pin microcontrollers, including PIC16F87X and PIC18FX2 devices. All the necessary hardware and software is included to run the demonstration programs. The sample microcontrollers provided with the PICDEM 2 demonstration board can be programmed with a PRO MATE II device programmer, PICSTART Plus development programmer, or MPLAB ICD 2 with a Universal Programmer Adapter. The MPLAB ICD 2 and MPLAB ICE in-circuit emulators may also be used with the PICDEM 2 demonstration board to test firmware. A prototype area extends the circuitry for additional application components. Some of the features include an RS-232 interface, a 2 x 16 LCD display, a piezo speaker, an on-board temperature sensor, four LEDs, and sample PIC18F452 and PIC16F877 FLASH microcontrollers.

11.17 PICDEM 3 PIC16C92X Demonstration Board

The PICDEM 3 demonstration board supports the PIC16C923 and PIC16C924 in the PLCC package. All the necessary hardware and software is included to run the demonstration programs.

11.18 PICDEM 17 Demonstration Board

The PICDEM 17 demonstration board is an evaluation board that demonstrates the capabilities of several Microchip microcontrollers, including PIC17C752, PIC17C756A, PIC17C762 and PIC17C766. A programmed sample is included. The PRO MATE II device programmer, or the PICSTART Plus development programmer, can be used to reprogram the device for user tailored application development. The PICDEM 17 demonstration board supports program download and execution from external on-board FLASH memory. A generous prototype area is available for user hardware expansion.

11.19 PICDEM 18R PIC18C601/801 Demonstration Board

The PICDEM 18R demonstration board serves to assist development of the PIC18C601/801 family of Microchip microcontrollers. It provides hardware implementation of both 8-bit Multiplexed/De-multiplexed and 16-bit Memory modes. The board includes 2 Mb external FLASH memory and 128 Kb SRAM memory, as well as serial EEPROM, allowing access to the wide range of memory types supported by the PIC18C601/801.

11.20 PICDEM LIN PIC16C43X Demonstration Board

The powerful LIN hardware and software kit includes a series of boards and three PICmicro microcontrollers. The small footprint PIC16C432 and PIC16C433 are used as slaves in the LIN communication and feature on-board LIN transceivers. A PIC16F874 FLASH microcontroller serves as the master. All three microcontrollers are programmed with firmware to provide LIN bus communication.

11.21 PICkit™ 1 FLASH Starter Kit

A complete "development system in a box", the PICkit FLASH Starter Kit includes a convenient multi-section board for programming, evaluation, and development of 8/14-pin FLASH PIC® microcontrollers. Powered via USB, the board operates under a simple Windows GUI. The PICkit 1 Starter Kit includes the user's guide (on CD ROM), PICkit 1 tutorial software and code for various applications. Also included are MPLAB® IDE (Integrated Development Environment) software, software and hardware "Tips 'n Tricks for 8-pin FLASH PIC® Microcontrollers" Handbook and a USB Interface Cable. Supports all current 8/14-pin FLASH PIC microcontrollers, as well as many future planned devices.

11.22 PICDEM USB PIC16C7X5 Demonstration Board

The PICDEM USB Demonstration Board shows off the capabilities of the PIC16C745 and PIC16C765 USB microcontrollers. This board provides the basis for future USB products.

11.23 Evaluation and Programming Tools

In addition to the PICDEM series of circuits, Microchip has a line of evaluation kits and demonstration software for these products.

- KEELOQ evaluation and programming tools for Microchip's HCS Secure Data Products
- CAN developers kit for automotive network applications
- Analog design boards and filter design software
- PowerSmart battery charging evaluation/calibration kits
- IrDA® development kit
- microID development and rfLab™ development software
- SEEVAL® designer kit for memory evaluation and endurance calculations
- PICDEM MSC demo boards for Switching mode power supply, high power IR driver, delta sigma ADC, and flow rate sensor

Check the Microchip web page and the latest Product Line Card for the complete list of demonstration and evaluation kits.

PIC12F629/675

NOTES:

12.0 ELECTRICAL SPECIFICATIONS

Absolute Maximum Ratings†

Ambient temperature under bias.....	-40 to +125°C
Storage temperature	-65°C to +150°C
Voltage on VDD with respect to Vss	-0.3 to +6.5V
Voltage on MCLR with respect to Vss	-0.3 to +13.5V
Voltage on all other pins with respect to VSS	-0.3V to (VDD + 0.3V)
Total power dissipation ⁽¹⁾	800 mW
Maximum current out of Vss pin	300 mA
Maximum current into VDD pin	250 mA
Input clamp current, I _{IK} (V _I < 0 or V _I > VDD).....	± 20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > VDD).....	± 20 mA
Maximum output current sunk by any I/O pin.....	25 mA
Maximum output current sourced by any I/O pin	25 mA
Maximum current sunk by all GPIO	125 mA
Maximum current sourced all GPIO	125 mA

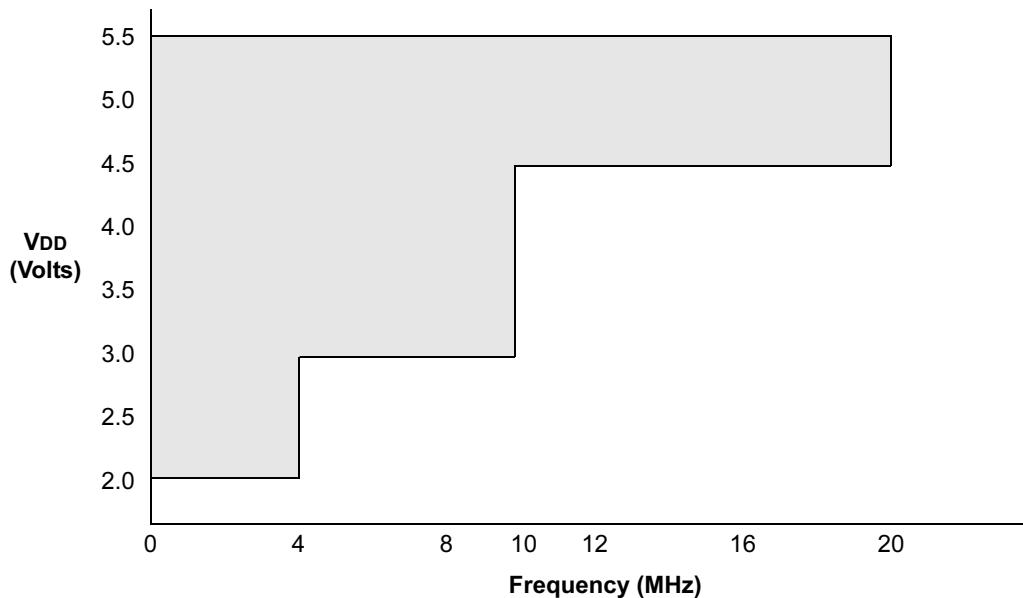
Note 1: Power dissipation is calculated as follows: P_{DIS} = V_{DD} x {I_{DD} - \sum I_{OH}} + \sum {(V_{DD}-V_{OH}) x I_{OH}} + \sum (V_{OL} x I_{OL}).

† NOTICE: Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operation listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Note: Voltage spikes below V_{SS} at the MCLR pin, inducing currents greater than 80 mA, may cause latchup. Thus, a series resistor of 50-100 Ω should be used when applying a "low" level to the MCLR pin, rather than pulling this pin directly to V_{SS}.

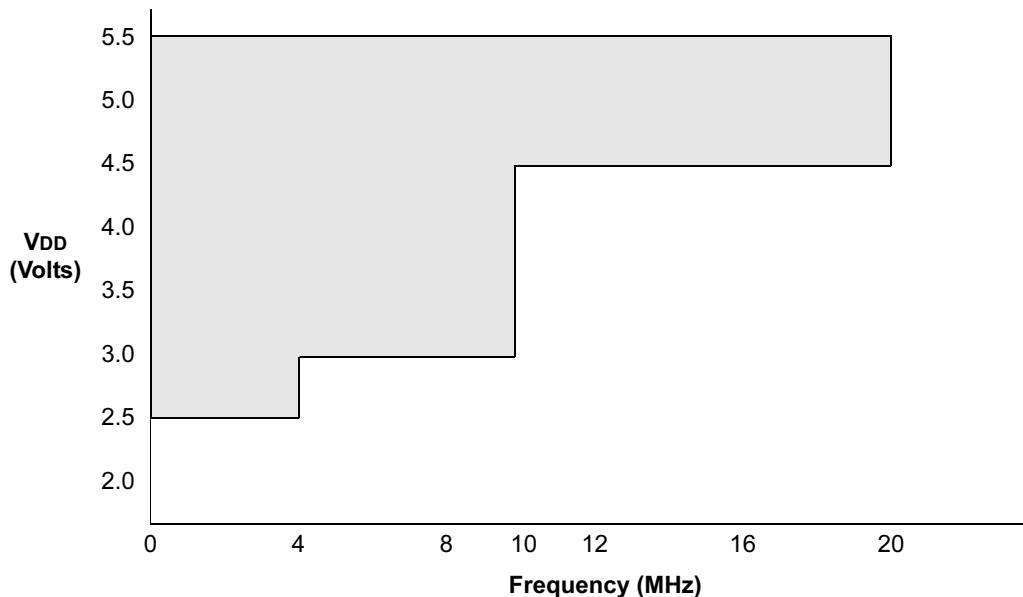
PIC12F629/675

**FIGURE 12-1: PIC12F629/675 WITH A/D DISABLED VOLTAGE-FREQUENCY GRAPH,
 $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$**



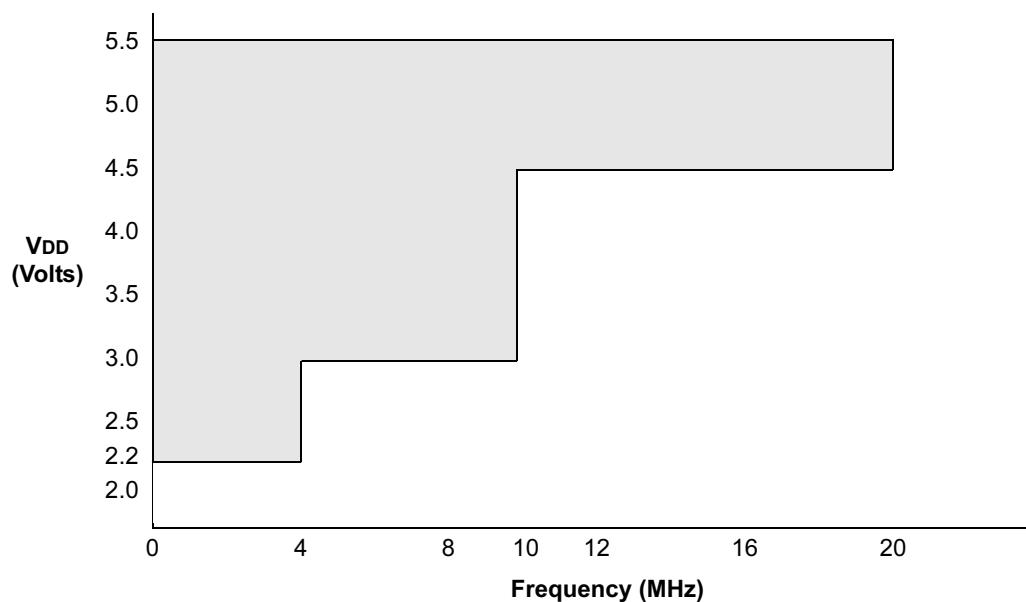
Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

**FIGURE 12-2: PIC12F675 WITH A/D ENABLED VOLTAGE-FREQUENCY GRAPH,
 $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$**



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

**FIGURE 12-3: PIC12F675 WITH A/D ENABLED VOLTAGE-FREQUENCY GRAPH,
 $0^{\circ}\text{C} \leq T_{\text{A}} \leq +125^{\circ}\text{C}$**



Note 1: The shaded region indicates the permissible combinations of voltage and frequency.

PIC12F629/675

12.1 DC Characteristics: PIC12F629/675-I (Industrial), PIC12F629/675-E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D001 D001A D001B D001C D001D	VDD	Supply Voltage	2.0	—	5.5	V	Fosc < = 4 MHz: PIC12F629/675 with A/D off
			2.2	—	5.5	V	PIC12F675 with A/D on, 0°C to +125°C
			2.5	—	5.5	V	PIC12F675 with A/D on, -40°C to +125°C
			3.0	—	5.5	V	4 MHz < Fosc < = 10 MHz
			4.5	—	5.5	V	
D002	VDR	RAM Data Retention Voltage⁽¹⁾	1.5*	—	—	V	Device in SLEEP mode
D003	VPOR	VDD Start Voltage to ensure internal Power-on Reset signal	—	Vss	—	V	See section on Power-on Reset for details
D004	SVDD	VDD Rise Rate to ensure internal Power-on Reset signal	0.05*	—	—	V/ms	See section on Power-on Reset for details
D005	VBOD		—	2.1	—	V	

* These parameters are characterized but not tested.

† Data in "Typ" column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: This is the limit to which VDD can be lowered in SLEEP mode without losing RAM data.

12.2 DC Characteristics: PIC12F629/675-I (Industrial)

		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +85^{\circ}\text{C}$ for industrial					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions	
						VDD	Note
D010	Supply Current (IDD)	—	9	16	μA	2.0	Fosc = 32 kHz LP Oscillator Mode
		—	18	28	μA	3.0	
		—	35	54	μA	5.0	
D011		—	110	150	μA	2.0	Fosc = 1 MHz XT Oscillator Mode
		—	190	280	μA	3.0	
		—	330	450	μA	5.0	
D012		—	220	280	μA	2.0	Fosc = 4 MHz XT Oscillator Mode
		—	370	650	μA	3.0	
		—	0.6	1.4	mA	5.0	
D013		—	70	110	μA	2.0	Fosc = 1 MHz EC Oscillator Mode
		—	140	250	μA	3.0	
		—	260	390	μA	5.0	
D014		—	180	250	μA	2.0	Fosc = 4 MHz EC Oscillator Mode
		—	320	470	μA	3.0	
		—	580	850	μA	5.0	
D015		—	340	450	μA	2.0	Fosc = 4 MHz INTOSC Mode
		—	500	700	μA	3.0	
		—	0.8	1.1	mA	5.0	
D016		—	180	250	μA	2.0	Fosc = 4 MHz EXTRC Mode
		—	320	450	μA	3.0	
		—	580	800	μA	5.0	
D017		—	2.1	2.95	mA	4.5	Fosc = 20 MHz HS Oscillator Mode
		—	2.4	3.0	mA	5.0	

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in Active Operation mode are: OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD; MCLR = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

PIC12F629/675

12.3 DC Characteristics: PIC12F629/675-I (Industrial)

		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +85^{\circ}\text{C}$ for industrial					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions	
						V _{DD}	Note
D020	Power-down Base Current (IPD)	—	0.99	700	nA	2.0	WDT, BOD, Comparators, VREF, and T1OSC disabled
		—	1.2	770	nA	3.0	
		—	2.9	995	nA	5.0	
D021		—	0.3	1.5	μA	2.0	WDT Current ⁽¹⁾
		—	1.8	3.5	μA	3.0	
		—	8.4	17	μA	5.0	
D022		—	58	70	μA	3.0	BOD Current ⁽¹⁾
		—	109	130	μA	5.0	
D023		—	3.3	6.5	μA	2.0	Comparator Current ⁽¹⁾
		—	6.1	8.5	μA	3.0	
		—	11.5	16	μA	5.0	
D024		—	58	70	μA	2.0	CVREF Current ⁽¹⁾
		—	85	100	μA	3.0	
		—	138	160	μA	5.0	
D025		—	4.0	6.5	μA	2.0	T1 Osc Current ⁽¹⁾
		—	4.6	7.0	μA	3.0	
		—	6.0	10.5	μA	5.0	
D026		—	1.2	775	nA	3.0	A/D Current ⁽¹⁾
		—	0.0022	1.0	μA	5.0	

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1:** The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.
- 2:** The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to V_{DD}.

12.4 DC Characteristics: PIC12F629/675-E (Extended)

		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$ for extended					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions	
						VDD	Note
D010E	Supply Current (IDD)	—	9	16	μA	2.0	Fosc = 32 kHz LP Oscillator Mode
		—	18	28	μA	3.0	
		—	35	54	μA	5.0	
D011E		—	110	150	μA	2.0	Fosc = 1 MHz XT Oscillator Mode
		—	190	280	μA	3.0	
		—	330	450	μA	5.0	
D012E		—	220	280	μA	2.0	Fosc = 4 MHz XT Oscillator Mode
		—	370	650	μA	3.0	
		—	0.6	1.4	mA	5.0	
D013E		—	70	110	μA	2.0	Fosc = 1 MHz EC Oscillator Mode
		—	140	250	μA	3.0	
		—	260	390	μA	5.0	
D014E		—	180	250	μA	2.0	Fosc = 4 MHz EC Oscillator Mode
		—	320	470	μA	3.0	
		—	580	850	μA	5.0	
D015E		—	340	450	μA	2.0	Fosc = 4 MHz INTOSC Mode
		—	500	780	μA	3.0	
		—	0.8	1.1	mA	5.0	
D016E		—	180	250	μA	2.0	Fosc = 4 MHz EXTRC Mode
		—	320	450	μA	3.0	
		—	580	800	μA	5.0	
D017E		—	2.1	2.95	mA	4.5	Fosc = 20 MHz HS Oscillator Mode
		—	2.4	3.0	mA	5.0	

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: The test conditions for all IDD measurements in Active Operation mode are: OSC1 = external square wave, from rail to rail; all I/O pins tri-stated, pulled to VDD; MCLR = VDD; WDT disabled.

2: The supply current is mainly a function of the operating voltage and frequency. Other factors such as I/O pin loading and switching rate, oscillator type, internal code execution pattern, and temperature also have an impact on the current consumption.

PIC12F629/675

12.5 DC Characteristics: PIC12F629/675-E (Extended)

		Standard Operating Conditions (unless otherwise stated) Operating temperature $-40^{\circ}\text{C} \leq \text{TA} \leq +125^{\circ}\text{C}$ for extended					
Param No.	Device Characteristics	Min	Typ†	Max	Units	Conditions	
						V _{DD}	Note
D020E	Power-down Base Current (IPD)	—	0.00099	3.5	μA	2.0	WDT, BOD, Comparators, V _{REF} , and T1OSC disabled
		—	0.0012	4.0	μA	3.0	
		—	0.0029	8.0	μA	5.0	
D021E		—	0.3	6.0	μA	2.0	WDT Current ⁽¹⁾
		—	1.8	9.0	μA	3.0	
		—	8.4	20	μA	5.0	
D022E		—	58	70	μA	3.0	BOD Current ⁽¹⁾
		—	109	130	μA	5.0	
D023E		—	3.3	10	μA	2.0	Comparator Current ⁽¹⁾
		—	6.1	13	μA	3.0	
		—	11.5	24	μA	5.0	
D024E		—	58	70	μA	2.0	CVREF Current ⁽¹⁾
		—	85	100	μA	3.0	
		—	138	165	μA	5.0	
D025E		—	4.0	10	μA	2.0	T1 Osc Current ⁽¹⁾
		—	4.6	12	μA	3.0	
		—	6.0	20	μA	5.0	
D026E		—	0.0012	6.0	μA	3.0	A/D Current ⁽¹⁾
		—	0.0022	8.5	μA	5.0	

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1:** The peripheral current is the sum of the base IDD or IPD and the additional current consumed when this peripheral is enabled. The peripheral Δ current can be determined by subtracting the base IDD or IPD current from this limit. Max values should be used when calculating total current consumption.
- 2:** The power-down current in SLEEP mode does not depend on the oscillator type. Power-down current is measured with the part in SLEEP mode, with all I/O pins in hi-impedance state and tied to V_{DD}.

12.6 DC Characteristics: PIC12F629/675-I (Industrial), PIC12F629/675-E (Extended)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D030 D030A D031 D032 D033 D033A	VIL	Input Low Voltage I/O ports with TTL buffer	Vss	—	0.8	V	4.5V ≤ VDD ≤ 5.5V
		with Schmitt Trigger buffer	Vss	—	0.15 VDD	V	Otherwise
		MCLR, OSC1 (RC mode)	Vss	—	0.2 VDD	V	Entire range
		OSC1 (XT and LP modes)	Vss	—	0.2 VDD	V	
		OSC1 (HS mode)	Vss	—	0.3	V	(Note 1)
			Vss	—	0.3 VDD	V	(Note 1)
D040 D040A D041 D042 D043 D043A D043B	VIH	Input High Voltage I/O ports with TTL buffer	2.0 (0.25 VDD+0.8)	—	VDD	V	4.5V ≤ VDD ≤ 5.5V
		with Schmitt Trigger buffer	0.8 VDD	—	VDD	V	otherwise
		MCLR	0.8 VDD	—	VDD	V	entire range
		OSC1 (XT and LP modes)	1.6	—	VDD	V	
		OSC1 (HS mode)	0.7 VDD	—	VDD	V	(Note 1)
		OSC1 (RC mode)	0.9 VDD	—	VDD	V	(Note 1)
D070	IPUR	GPIO Weak Pull-up Current	50*	250	400*	μA	VDD = 5.0V, VPIN = Vss
D060 D060A D060B D061 D063	IIL	Input Leakage Current⁽³⁾ I/O ports	—	± 0.1	± 1	μA	VSS ≤ VPIN ≤ VDD, Pin at hi-impedance
		Analog inputs	—	± 0.1	± 1	μA	VSS ≤ VPIN ≤ VDD
		VREF	—	± 0.1	± 1	μA	VSS ≤ VPIN ≤ VDD
		MCLR ⁽²⁾	—	± 0.1	± 5	μA	VSS ≤ VPIN ≤ VDD
		OSC1	—	± 0.1	± 5	μA	VSS ≤ VPIN ≤ VDD, XT, HS and LP osc configuration
D080 D083	VOL	Output Low Voltage I/O ports OSC2/CLKOUT (RC mode)	—	—	0.6	V	IOL = 8.5 mA, VDD = 4.5V (Ind.)
			—	—	0.6	V	IOL = 1.6 mA, VDD = 4.5V (Ind.)
							IOL = 1.2 mA, VDD = 4.5V (Ext.)
D090 D092	VOH	Output High Voltage I/O ports OSC2/CLKOUT (RC mode)	VDD - 0.7	—	—	V	IOH = -3.0 mA, VDD = 4.5V (Ind.)
			VDD - 0.7	—	—	V	IOH = -1.3 mA, VDD = 4.5V (Ind.)
							IOH = -1.0 mA, VDD = 4.5V (Ext.)

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

- Note 1:** In RC oscillator configuration, the OSC1/CLKIN pin is a Schmitt Trigger input. It is not recommended to use an external clock in RC mode.
- 2:** The leakage current on the MCLR pin is strongly dependent on the applied voltage level. The specified levels represent normal operating conditions. Higher leakage current may be measured at different input voltages.
- 3:** Negative current is defined as current sourced by the pin.

PIC12F629/675

12.7 DC Characteristics: PIC12F629/675-I (Industrial), PIC12F629/675-E (Extended) (Cont.)

DC CHARACTERISTICS			Standard Operating Conditions (unless otherwise stated)				
			Operating temperature -40°C ≤ TA ≤ +85°C for industrial -40°C ≤ TA ≤ +125°C for extended				
Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
D100	Cosc2	Capacitive Loading Specs on Output Pins OSC2 pin	—	—	15*	pF	In XT, HS and LP modes when external clock is used to drive OSC1
D101	CIO	All I/O pins	—	—	50*	pF	
D120	ED	Data EEPROM Memory Byte Endurance	100K	1M	—	E/W	-40°C ≤ TA ≤ +85°C
D120A	ED	Byte Endurance	10K	100K	—	E/W	+85°C ≤ TA ≤ +125°C
D121	VDRW	VDD for Read/Write	VMIN	—	5.5	V	Using EECON to read/write VMIN = Minimum operating voltage
D122	TDEW	Erase/Write cycle time	—	5	6	ms	
D123	TRETD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated
D124	TREF	Number of Total Erase/Write Cycles before Refresh ⁽¹⁾	1M	10M	—	E/W	-40°C ≤ TA ≤ +85°C
D130	EP	Program FLASH Memory Cell Endurance	10K	100K	—	E/W	-40°C ≤ TA ≤ +85°C
D130A	ED	Cell Endurance	1K	10K	—	E/W	+85°C ≤ TA ≤ +125°C
D131	VPR	VDD for Read	VMIN	—	5.5	V	VMIN = Minimum operating voltage
D132	VPEW	VDD for Erase/Write	4.5	—	5.5	V	
D133	TPEW	Erase/Write cycle time	—	2	2.5	ms	
D134	TRETD	Characteristic Retention	40	—	—	Year	Provided no other specifications are violated

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: See Section 8.5.1 for additional information.

12.8 TIMING PARAMETER SYMOLOGY

The timing parameter symbols have been created with one of the following formats:

1. TppS2ppS

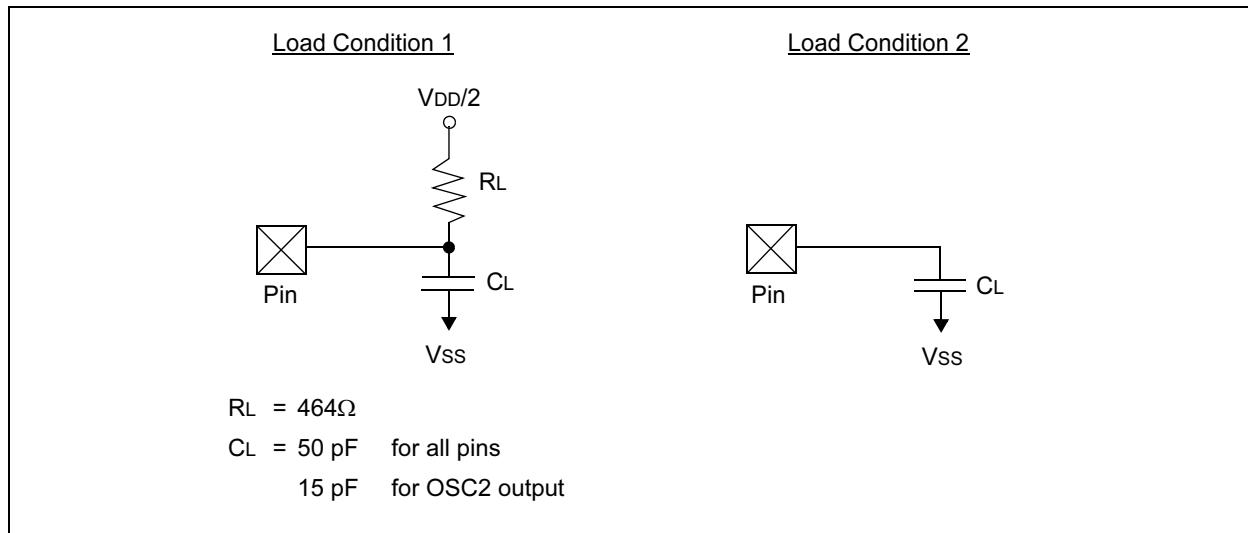
2. TppS

T	F	Frequency	T	Time
Lowercase letters (pp) and their meanings:				
pp				
cc	CCP1		osc	OSC1
ck	CLKOUT		rd	\overline{RD}
cs	\overline{CS}		rw	\overline{RD} or \overline{WR}
di	SDI		sc	SCK
do	SDO		ss	\overline{SS}
dt	Data in		t0	T0CKI
io	I/O port		t1	T1CKI
mc	MCLR		wr	\overline{WR}

Uppercase letters and their meanings:

S	F	P	R
	Fall	Period	
H	High	Rise	
I	Invalid (Hi-impedance)	Valid	
L	Low	Z	Hi-impedance

FIGURE 12-4: LOAD CONDITIONS



PIC12F629/675

12.9 AC CHARACTERISTICS: PIC12F629/675 (INDUSTRIAL, EXTENDED)

FIGURE 12-5: EXTERNAL CLOCK TIMING

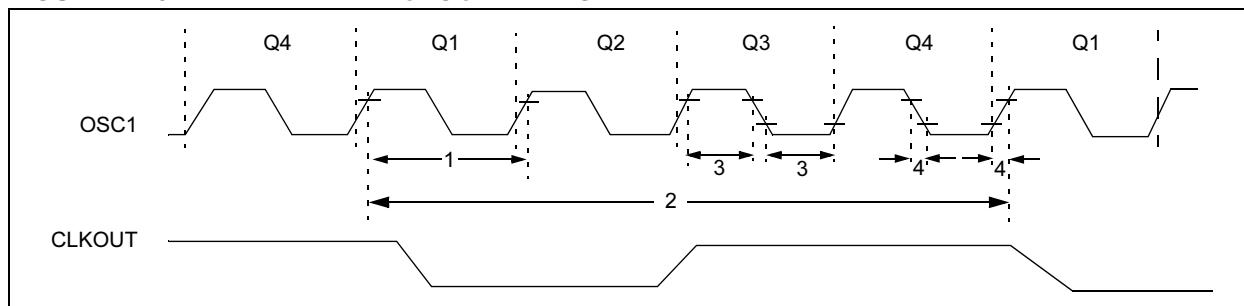


TABLE 12-1: EXTERNAL CLOCK TIMING REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
	Fosc	External CLKIN Frequency ⁽¹⁾	DC	—	37	kHz	LP Osc mode
			DC	—	4	MHz	XT mode
			DC	—	20	MHz	HS mode
			DC	—	20	MHz	EC mode
	Oscillator Frequency ⁽¹⁾	5	—	37	kHz	LP Osc mode	
		—	4	—	MHz	INTOSC mode	
		DC	—	4	MHz	RC Osc mode	
		0.1	—	4	MHz	XT Osc mode	
		1	—	20	MHz	HS Osc mode	
1	Tosc	External CLKIN Period ⁽¹⁾	27	—	∞	μs	LP Osc mode
			50	—	∞	ns	HS Osc mode
			50	—	∞	ns	EC Osc mode
			250	—	∞	ns	XT Osc mode
	Oscillator Period ⁽¹⁾	27	—	200	μs	LP Osc mode	
		—	250	—	ns	INTOSC mode	
		250	—	—	ns	RC Osc mode	
		250	—	10,000	ns	XT Osc mode	
		50	—	1,000	ns	HS Osc mode	
2	Tcy	Instruction Cycle Time ⁽¹⁾	200	Tcy	DC	ns	Tcy = 4/Fosc
3	TosL, Tosh	External CLKIN (OSC1) High	2*	—	—	μs	LP oscillator, Tosc L/H duty cycle
		External CLKIN Low	20*	—	—	ns	HS oscillator, Tosc L/H duty cycle
			100 *	—	—	ns	XT oscillator, Tosc L/H duty cycle
4	TosR, TosF	External CLKIN Rise	—	—	50*	ns	LP oscillator
		External CLKIN Fall	—	—	25*	ns	XT oscillator
			—	—	15*	ns	HS oscillator

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: Instruction cycle period (Tcy) equals four times the input oscillator time-base period. All specified values are based on characterization data for that particular oscillator type under standard operating conditions with the device executing code. Exceeding these specified limits may result in an unstable oscillator operation and/or higher than expected current consumption. All devices are tested to operate at 'min' values with an external clock applied to OSC1 pin. When an external clock input is used, the 'max' cycle time limit is 'DC' (no clock) for all devices.

TABLE 12-2: PRECISION INTERNAL OSCILLATOR PARAMETERS

Param No.	Sym	Characteristic	Freq Tolerance	Min	Typ†	Max	Units	Conditions
F10	Fosc	Internal Calibrated INTOSC Frequency	±1	3.96	4.00	4.04	MHz	VDD = 3.5V, 25°C
			±2	3.92	4.00	4.08	MHz	2.5V ≤ VDD ≤ 5.5V
			±5	3.80	4.00	4.20	MHz	0°C ≤ TA ≤ +85°C 2.0V ≤ VDD ≤ 5.5V -40°C ≤ TA ≤ +85°C (IND) -40°C ≤ TA ≤ +125°C (EXT)
F14	Tiosc _{ST}	Oscillator Wake-up from SLEEP start-up time*	—	—	6	8	μs	VDD = 2.0V, -40°C to +85°C
			—	—	4	6	μs	VDD = 3.0V, -40°C to +85°C
			—	—	3	5	μs	VDD = 5.0V, -40°C to +85°C

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

PIC12F629/675

FIGURE 12-6: CLKOUT AND I/O TIMING

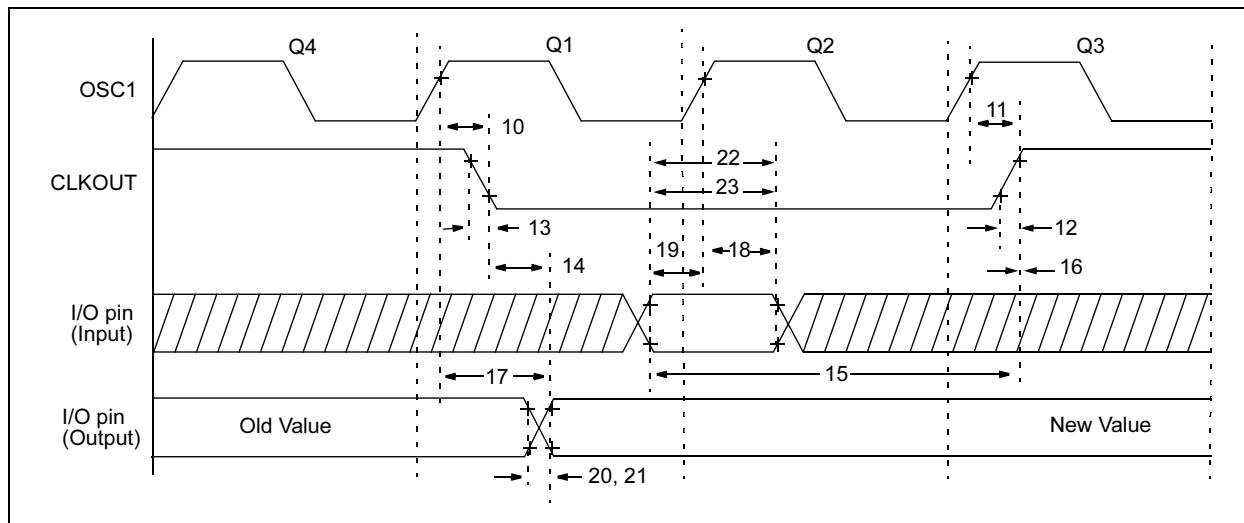


TABLE 12-3: CLKOUT AND I/O TIMING REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
10	T _{oscH2ckL}	OSC1 \uparrow to CLK-OUT \downarrow	—	75	200	ns	(Note 1)
11	T _{oscH2ckH}	OSC1 \uparrow to CLK-OUT \uparrow	—	75	200	ns	(Note 1)
12	T _{cR}	CLKOUT rise time	—	35	100	ns	(Note 1)
13	T _{cF}	CLKOUT fall time	—	35	100	ns	(Note 1)
14	T _{ckL2ioV}	CLKOUT \downarrow to Port out valid	—	—	20	ns	(Note 1)
15	T _{ioV2ckH}	Port in valid before CLKOUT \uparrow	T _{osc} + 200 ns	—	—	ns	(Note 1)
16	T _{ckH2iol}	Port in hold after CLKOUT \uparrow	0	—	—	ns	(Note 1)
17	T _{oscH2ioV}	OSC1 \uparrow (Q1 cycle) to Port out valid	—	50	150 *	ns	
			—	—	300	ns	
18	T _{oscH2iol}	OSC1 \uparrow (Q2 cycle) to Port input invalid (I/O in hold time)	100	—	—	ns	
19	T _{ioV2osH}	Port input valid to OSC1 \uparrow (I/O in setup time)	0	—	—	ns	
20	T _{ioR}	Port output rise time	—	10	40	ns	
21	T _{ioF}	Port output fall time	—	10	40	ns	
22	T _{inp}	INT pin high or low time	25	—	—	ns	
23	T _{rbp}	GPIO change INT high or low time	T _{CY}	—	—	ns	

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated.

Note 1: Measurements are taken in RC mode where CLKOUT output is 4xT_{osc}.

FIGURE 12-7: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER AND POWER-UP TIMER TIMING

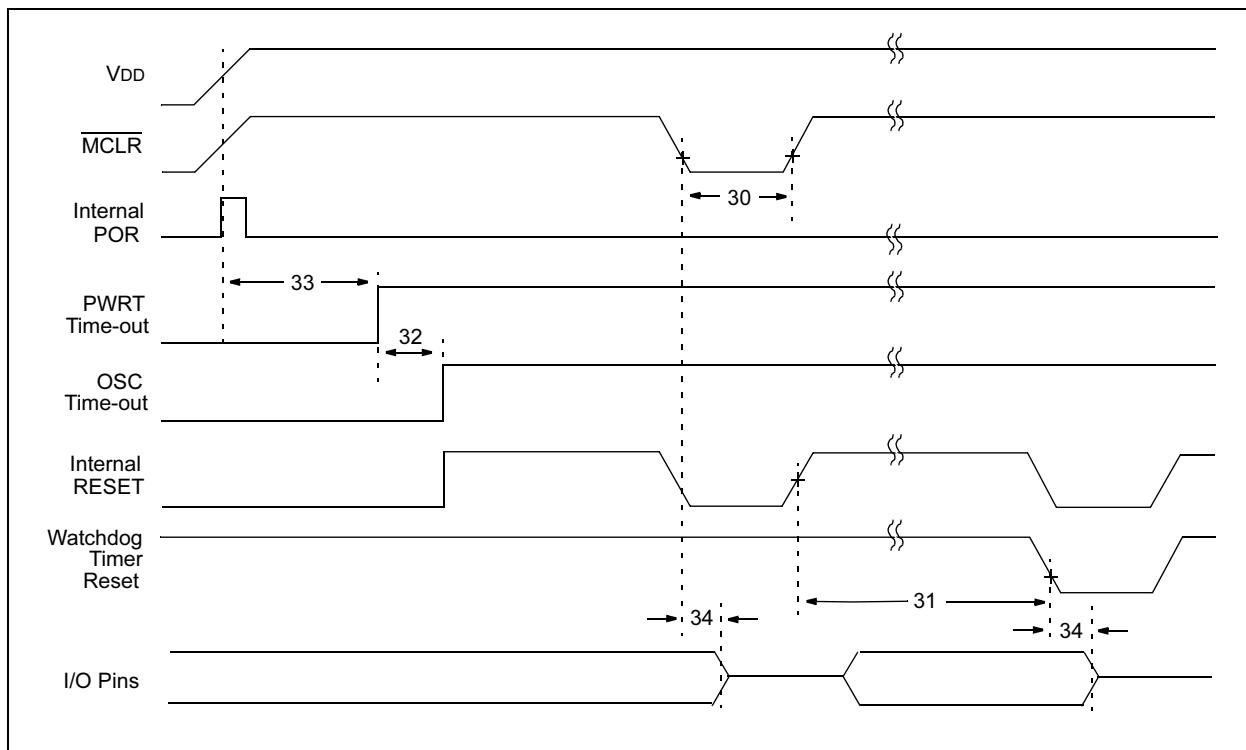
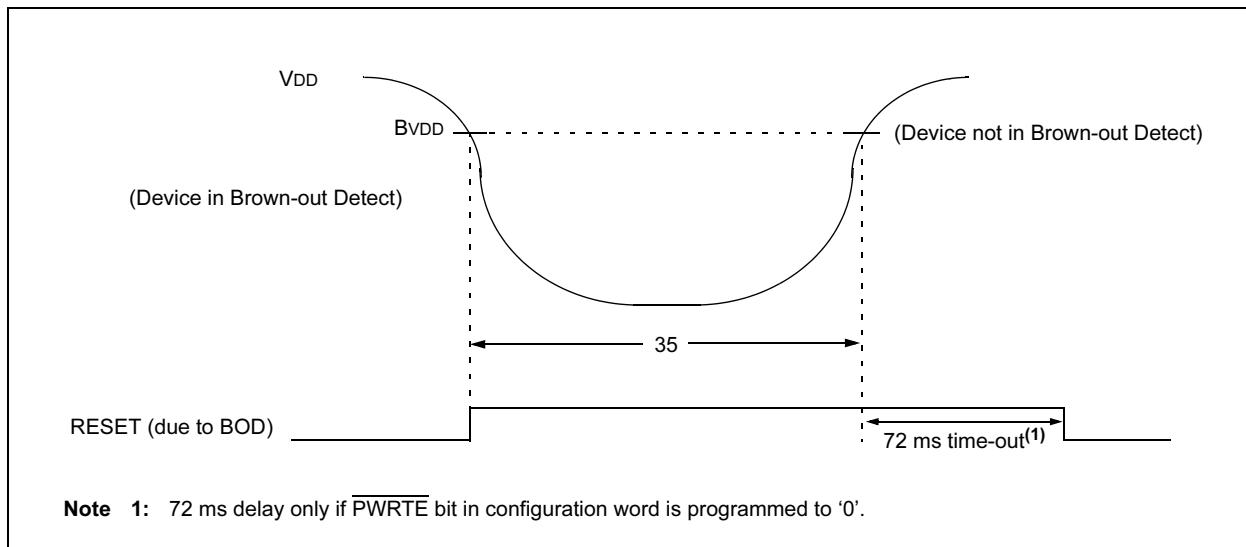


FIGURE 12-8: BROWN-OUT DETECT TIMING AND CHARACTERISTICS



PIC12F629/675

TABLE 12-4: RESET, WATCHDOG TIMER, OSCILLATOR START-UP TIMER, POWER-UP TIMER, AND BROWN-OUT DETECT REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
30	TMCL	MCLR Pulse Width (low)	2 TBD	— TBD	— TBD	μs ms	VDD = 5V, -40°C to +85°C Extended temperature
31	TWDT	Watchdog Timer Time-out Period (No Prescaler)	10 10	17 17	25 30	ms ms	VDD = 5V, -40°C to +85°C Extended temperature
32	TOST	Oscillation Start-up Timer Period	—	1024Tosc	—	—	Tosc = OSC1 period
33*	TPWRT	Power-up Timer Period	28* TBD	72 TBD	132* TBD	ms ms	VDD = 5V, -40°C to +85°C Extended Temperature
34	TIOZ	I/O Hi-impedance from MCLR Low or Watchdog Timer Reset	—	—	2.0	μs	
	BVDD	Brown-out Detect Voltage	2.025	—	2.175	V	
		Brown-out Hysteresis	TBD	—	—	—	
35	TBOD	Brown-out Detect Pulse Width	100*	—	—	μs	VDD ≤ BVDD (D005)

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

FIGURE 12-9: TIMER0 AND TIMER1 EXTERNAL CLOCK TIMINGS

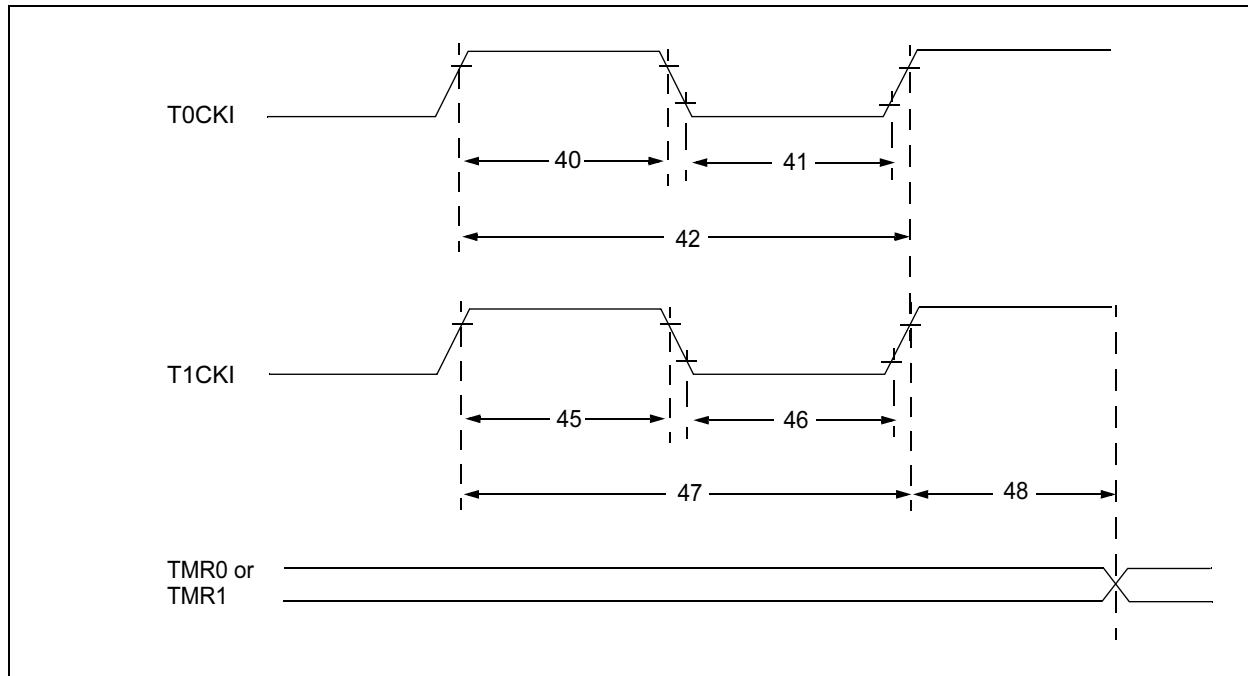


TABLE 12-5: TIMER0 AND TIMER1 EXTERNAL CLOCK REQUIREMENTS

Param No.	Sym	Characteristic		Min	Typ†	Max	Units	Conditions
40*	Tt0H	T0CKI High Pulse Width	No Prescaler	0.5 T _{CY} + 20	—	—	ns	
			With Prescaler	10	—	—	ns	
41*	Tt0L	T0CKI Low Pulse Width	No Prescaler	0.5 T _{CY} + 20	—	—	ns	
			With Prescaler	10	—	—	ns	
42*	Tt0P	T0CKI Period		Greater of: 20 or <u>T_{CY} + 40</u> N	—	—	ns	N = prescale value (2, 4, ..., 256)
45*	Tt1H	T1CKI High Time	Synchronous, No Prescaler	0.5 T _{CY} + 20	—	—	ns	
			Synchronous, with Prescaler	15	—	—	ns	
			Asynchronous	30	—	—	ns	
46*	Tt1L	T1CKI Low Time	Synchronous, No Prescaler	0.5 T _{CY} + 20	—	—	ns	
			Synchronous, with Prescaler	15	—	—	ns	
			Asynchronous	30	—	—	ns	
47*	Tt1P	T1CKI Input Period	Synchronous	Greater of: 30 or <u>T_{CY} + 40</u> N	—	—	ns	N = prescale value (1, 2, 4, 8)
			Asynchronous	60	—	—	ns	
Ft1		Timer1 oscillator input frequency range (oscillator enabled by setting bit T1OSCEN)	DC	—	200*	kHz		
48	TCKEZtmr1	Delay from external clock edge to timer increment	2 T _{Osc} *	—	7 T _{Osc} *	—		

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

PIC12F629/675

TABLE 12-6: COMPARATOR SPECIFICATIONS

Comparator Specifications		Standard Operating Conditions -40°C to +125°C (unless otherwise stated)				
Sym	Characteristics	Min	Typ	Max	Units	Comments
Vos	Input Offset Voltage	—	± 5.0	± 10	mV	
VCM	Input Common Mode Voltage	0	—	VDD - 1.5	V	
CMRR	Common Mode Rejection Ratio	+55*	—	—	db	
TRT	Response Time ⁽¹⁾	—	150	400*	ns	
TMC2coV	Comparator Mode Change to Output Valid	—	—	10*	μs	

* These parameters are characterized but not tested.

Note 1: Response time measured with one comparator input at (VDD - 1.5)/2 while the other input transitions from Vss to VDD - 1.5V.

TABLE 12-7: COMPARATOR VOLTAGE REFERENCE SPECIFICATIONS

Voltage Reference Specifications		Standard Operating Conditions -40°C to +125°C (unless otherwise stated)				
Sym	Characteristics	Min	Typ	Max	Units	Comments
	Resolution	—	VDD/24*	—	Lsb	Low Range (VRR = 1)
		—	VDD/32	—	Lsb	High Range (VRR = 0)
	Absolute Accuracy	—	—	± 1/2	Lsb	Low Range (VRR = 1)
		—	—	± 1/2*	Lsb	High Range (VRR = 0)
	Unit Resistor Value (R)	—	2k*	—	Ω	
	Settling Time ⁽¹⁾	—	—	10*	μs	

* These parameters are characterized but not tested.

Note 1: Settling time measured while VRR = 1 and VR<3:0> transitions from 0000 to 1111.

TABLE 12-8: PIC12F675 A/D CONVERTER CHARACTERISTICS:

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
A01	NR	Resolution	—	—	10 bits	bit	
A02	EABS	Total Absolute Error*	—	—	± 1	LSb	VREF = 5.0V
A03	EIL	Integral Error	—	—	± 1	LSb	VREF = 5.0V
A04	EDL	Differential Error	—	—	± 1	LSb	No missing codes to 10 bits VREF = 5.0V
A05	EFS	Full Scale Range	2.2*	—	5.5*	V	
A06	EOFF	Offset Error	—	—	± 1	LSb	VREF = 5.0V
A07	EGN	Gain Error	—	—	± 1	LSb	VREF = 5.0V
A10	—	Monotonicity	—	guaranteed ⁽³⁾	—	—	$V_{SS} \leq V_{AIN} \leq V_{REF+}$
A20 A20A	VREF	Reference Voltage	2.0 2.5	—	— $V_{DD} + 0.3$	V	Absolute minimum to ensure 10-bit accuracy
A21	VREF	Reference V High (VDD or VREF)	Vss	—	VDD	V	
A25	VAIN	Analog Input Voltage	Vss	—	VREF	V	
A30	ZAIN	Recommended Impedance of Analog Voltage Source	—	—	10	kΩ	
A50	IREF	VREF Input Current ⁽²⁾	10 —	— —	1000 10	μA μA	During VAIN acquisition. Based on differential of VHOLD to VAIN. During A/D conversion cycle.

* These parameters are characterized but not tested.

† Data in 'Typ' column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: When A/D is off, it will not consume any current other than leakage current. The power-down current spec includes any such leakage from the A/D module.

2: VREF current is from External VREF or VDD pin, whichever is selected as reference input.

3: The A/D conversion result never decreases with an increase in the input voltage and has no missing codes.

PIC12F629/675

FIGURE 12-10: PIC12F675 A/D CONVERSION TIMING (NORMAL MODE)

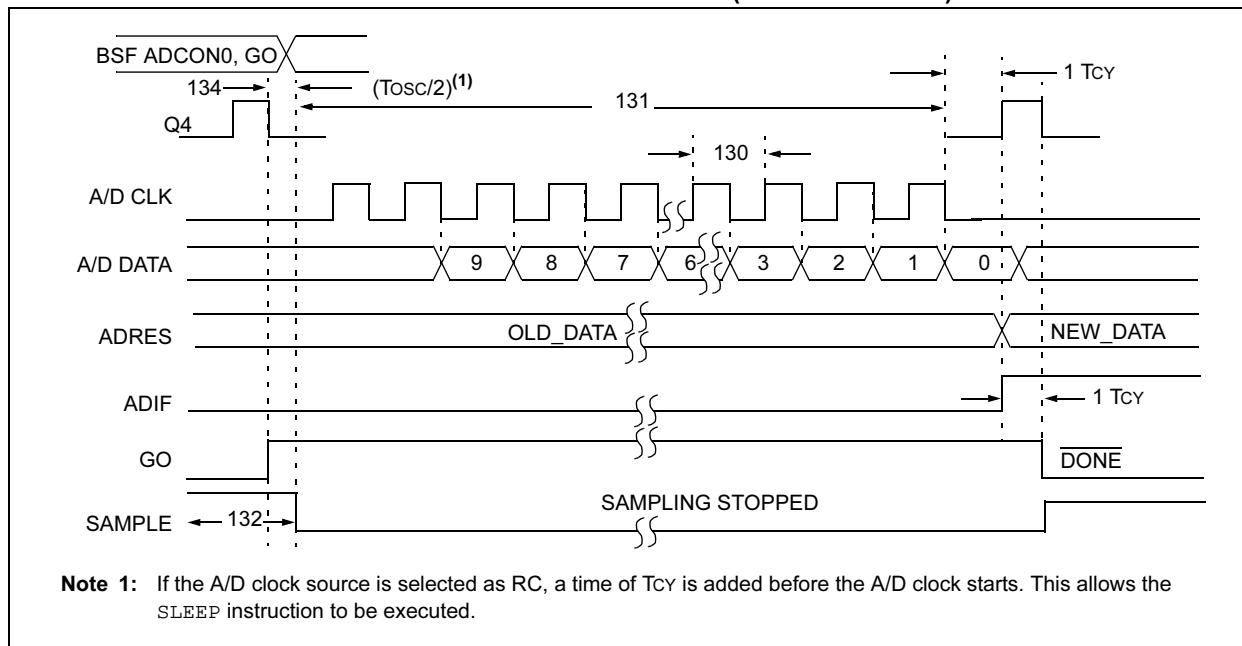


TABLE 12-9: PIC12F675 A/D CONVERSION REQUIREMENTS

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
130	TAD	A/D Clock Period	1.6 3.0*	— —	— —	μs	TOSC based, $V_{REF} \geq 3.0V$
130	TAD	A/D Internal RC Oscillator Period	3.0* 2.0*	6.0 4.0	9.0* 6.0*	μs	TOSC based, V_{REF} full range ADCS<1:0> = 11 (RC mode) At $V_{DD} = 2.5V$ At $V_{DD} = 5.0V$
131	TCNV	Conversion Time (not including Acquisition Time) ⁽¹⁾	—	11	—	TAD	Set GO bit to new data in A/D result register
132	TACQ	Acquisition Time	(Note 2) 5*	11.5 —	— —	μs	The minimum time is the amplifier settling time. This may be used if the “new” input voltage has not changed by more than 1 Lsb (i.e., 4.1 mV @ 4.096V) from the last sampled voltage (as stored on CHOLD).
134	TGO	Q4 to A/D Clock Start	—	Tosc/2	—	—	If the A/D clock source is selected as RC, a time of T_{CY} is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

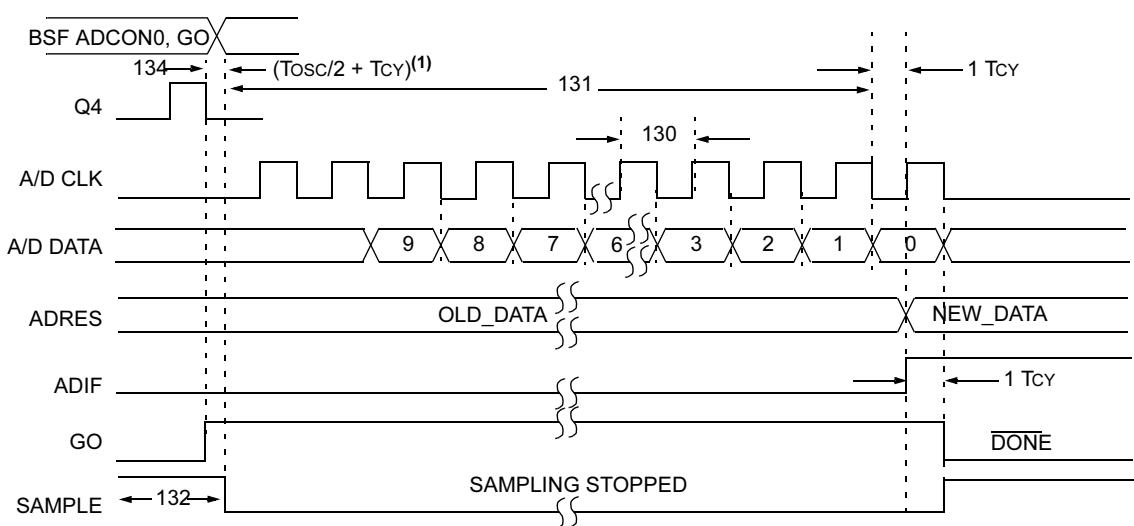
* These parameters are characterized but not tested.

† Data in ‘Typ’ column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRES register may be read on the following T_{CY} cycle.

2: See Section 7.1 for minimum conditions.

FIGURE 12-11: PIC12F675 A/D CONVERSION TIMING (SLEEP MODE)



Note 1: If the A/D clock source is selected as RC, a time of T_{CY} is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

TABLE 12-10: PIC12F675 A/D CONVERSION REQUIREMENTS (SLEEP MODE)

Param No.	Sym	Characteristic	Min	Typ†	Max	Units	Conditions
130	TAD	A/D Clock Period	1.6 3.0*	— —	— —	μs	$V_{REF} \geq 3.0V$
130	TAD	A/D Internal RC Oscillator Period	3.0* 2.0*	6.0 4.0	9.0* 6.0*	μs	V_{REF} full range $ADCS<1:0> = 11$ (RC mode) At $V_{DD} = 2.5V$ At $V_{DD} = 5.0V$
131	TCNV	Conversion Time (not including Acquisition Time) ⁽¹⁾	—	11	—	TAD	
132	TACQ	Acquisition Time	(Note 2) 5*	11.5	—	μs	The minimum time is the amplifier settling time. This may be used if the “new” input voltage has not changed by more than 1 Lsb (i.e., 4.1 mV @ 4.096V) from the last sampled voltage (as stored on CHOLD).
134	TGO	Q4 to A/D Clock Start	—	$T_{osc}/2 + T_{CY}$	—	—	If the A/D clock source is selected as RC, a time of T_{CY} is added before the A/D clock starts. This allows the SLEEP instruction to be executed.

* These parameters are characterized but not tested.

† Data in ‘Typ’ column is at 5.0V, 25°C unless otherwise stated. These parameters are for design guidance only and are not tested.

Note 1: ADRES register may be read on the following T_{CY} cycle.

2: See Section 7.1 for minimum conditions.

PIC12F629/675

NOTES:

13.0 DC AND AC CHARACTERISTICS GRAPHS AND TABLES

The graphs and tables provided in this section are for **design guidance** and are **not tested**.

In some graphs or tables, the data presented are **outside specified operating range** (i.e., outside specified V_{DD} range). This is for **information only** and devices are ensured to operate properly only within the specified range.

The data presented in this section is a **statistical summary** of data collected on units from different lots over a period of time and matrix samples. 'Typical' represents the mean of the distribution at 25°C. 'Max' or 'min' represents (mean + 3σ) or (mean - 3σ) respectively, where σ is standard deviation, over the whole temperature range.

FIGURE 13-1: TYPICAL IPD vs. V_{DD} OVER TEMP (-40°C TO +25°C)

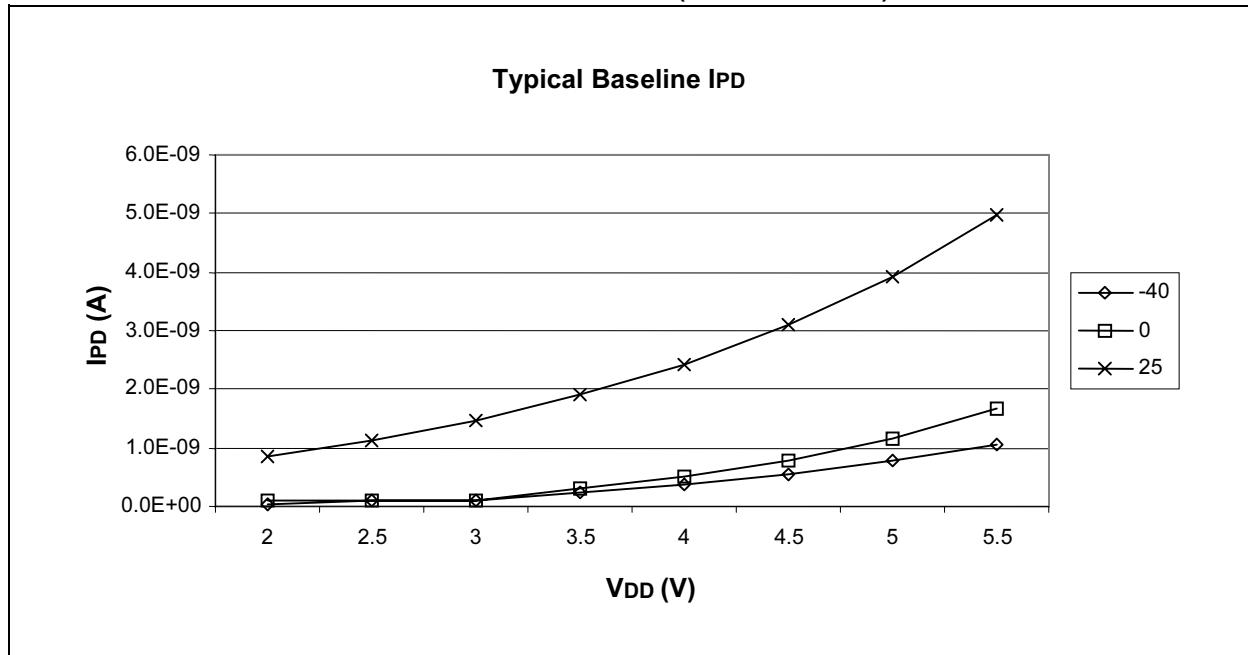
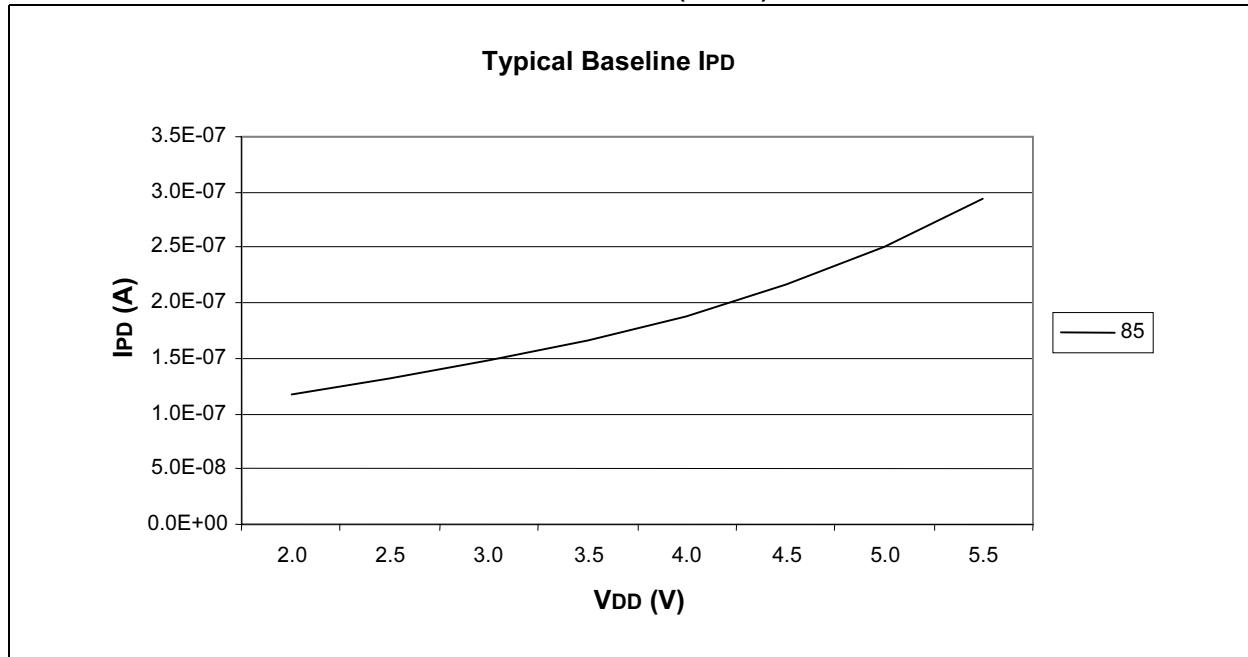


FIGURE 13-2: TYPICAL IPD vs. V_{DD} OVER TEMP (+85°C)



PIC12F629/675

FIGURE 13-3: TYPICAL IPD VS. VDD OVER TEMP (+125°C)

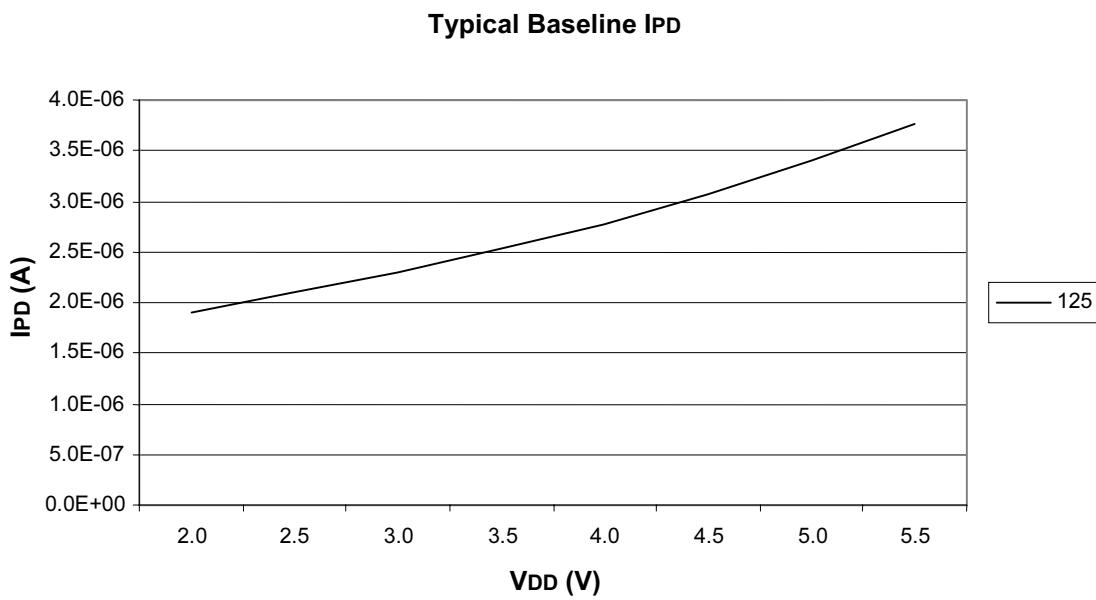


FIGURE 13-4: MAXIMUM IPD VS. VDD OVER TEMP (-40°C TO +25°C)

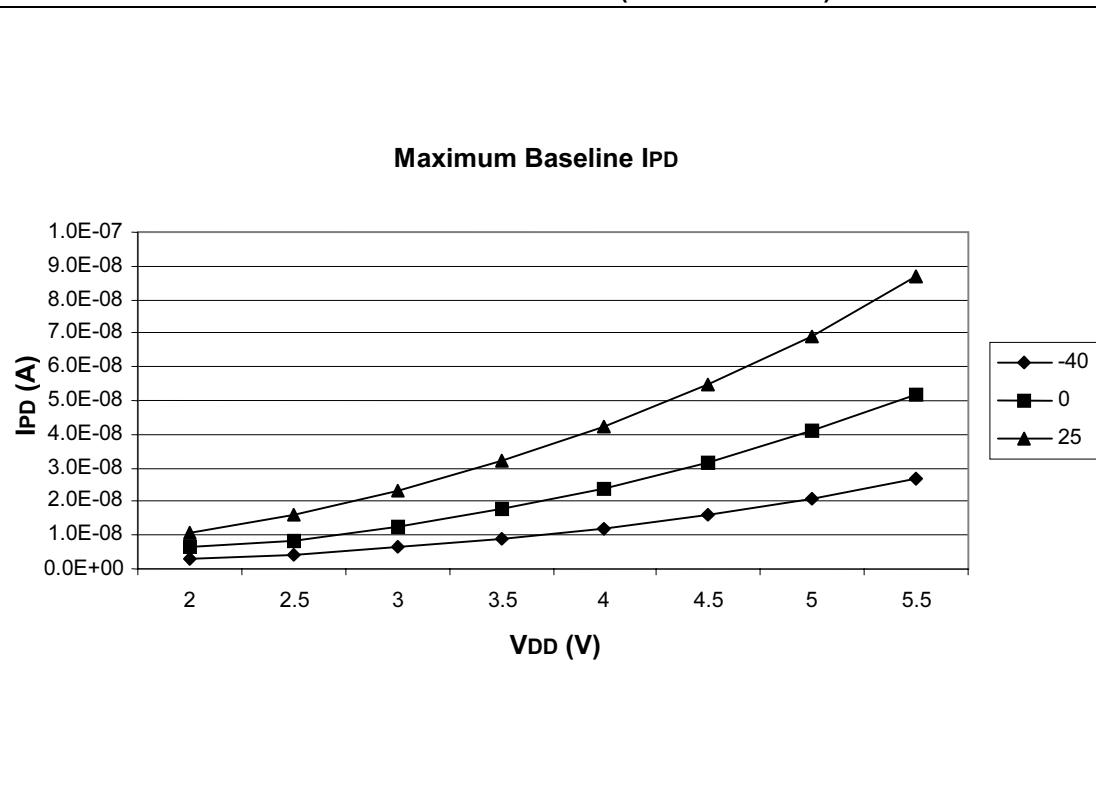


FIGURE 13-5: MAXIMUM IPD vs. V_{DD} OVER TEMP (+85°C)

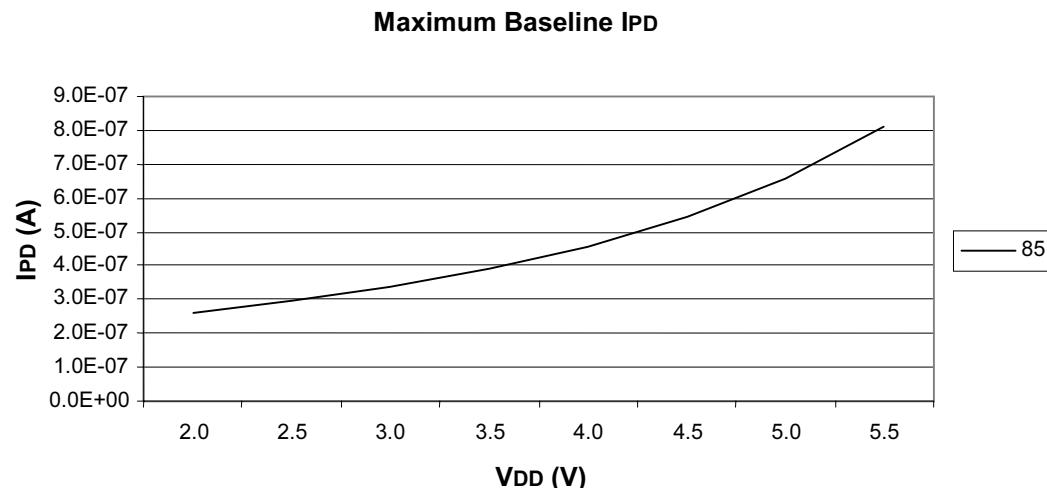
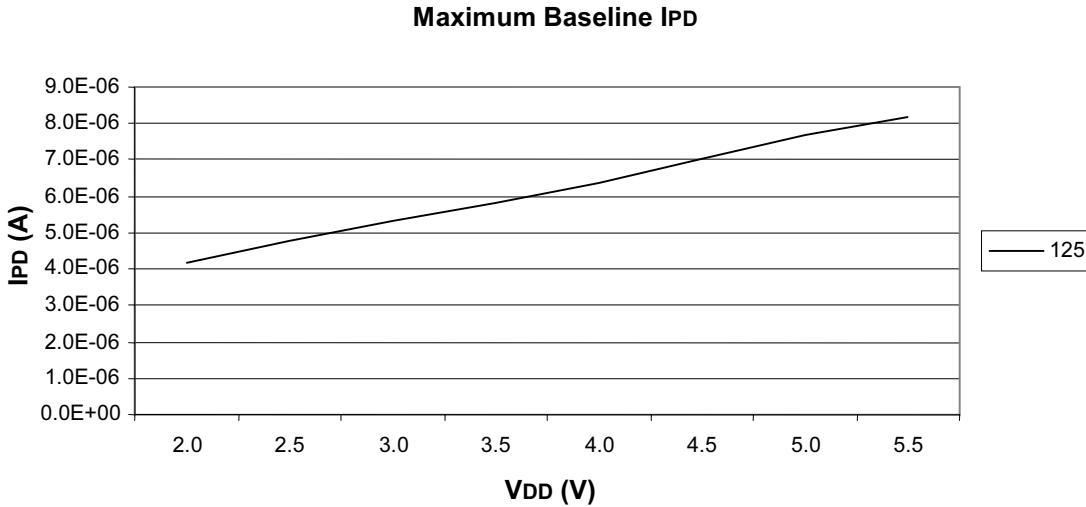


FIGURE 13-6: MAXIMUM IPD vs. V_{DD} OVER TEMP (+125°C)



PIC12F629/675

FIGURE 13-7: TYPICAL IPD WITH BOD ENABLED vs. V_{DD} OVER TEMP (-40°C TO +125°C)

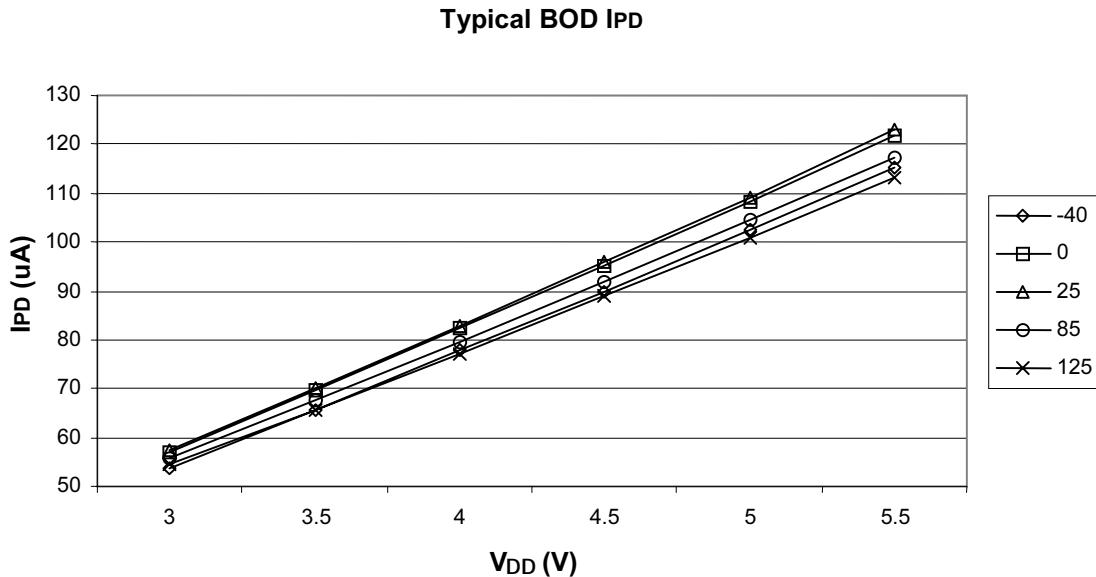


FIGURE 13-8: TYPICAL IPD WITH CMP ENABLED vs. V_{DD} OVER TEMP (-40°C TO +125°C)

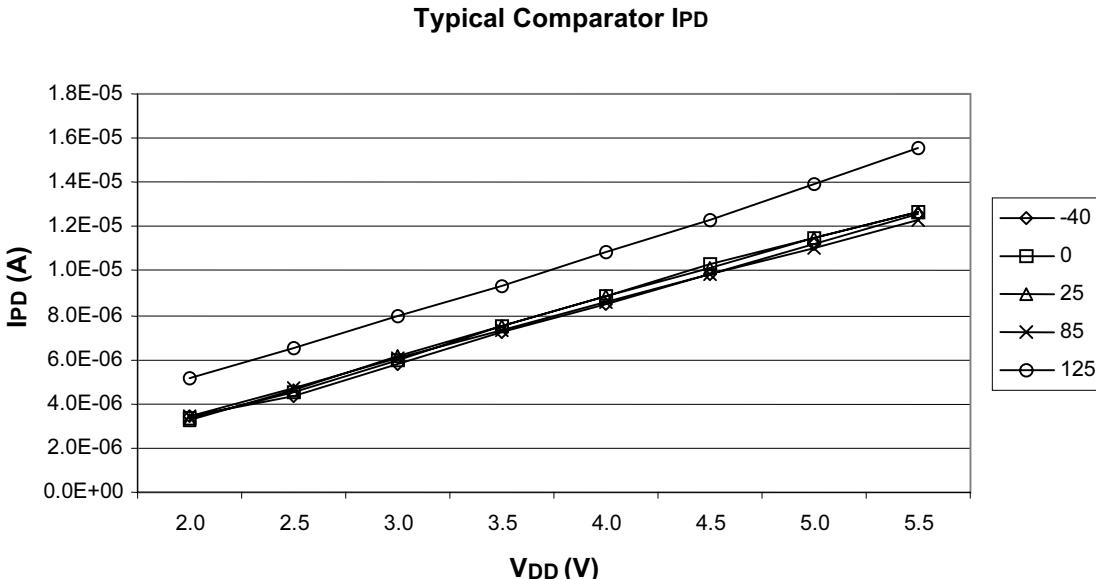


FIGURE 13-9: TYPICAL IPD WITH A/D ENABLED vs. V_{DD} OVER TEMP (-40°C TO +25°C)

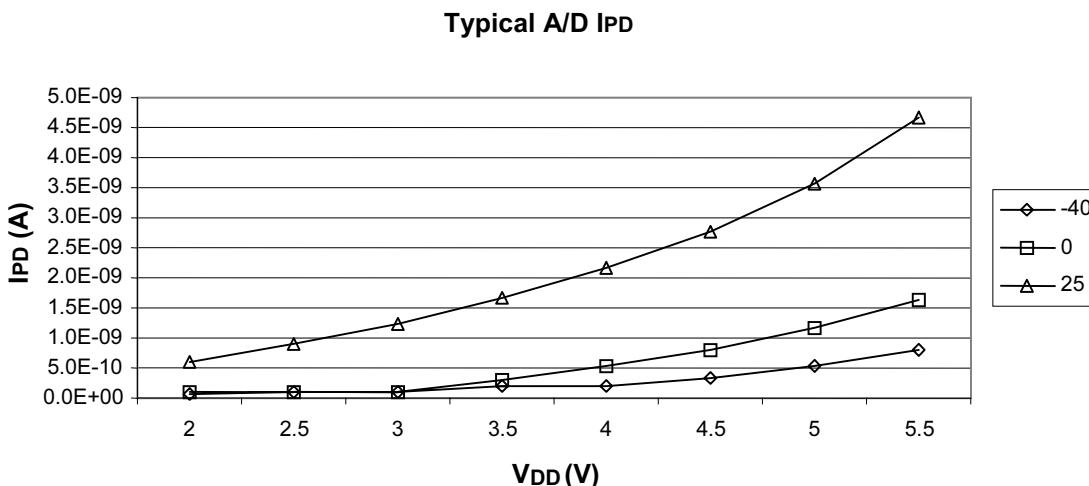
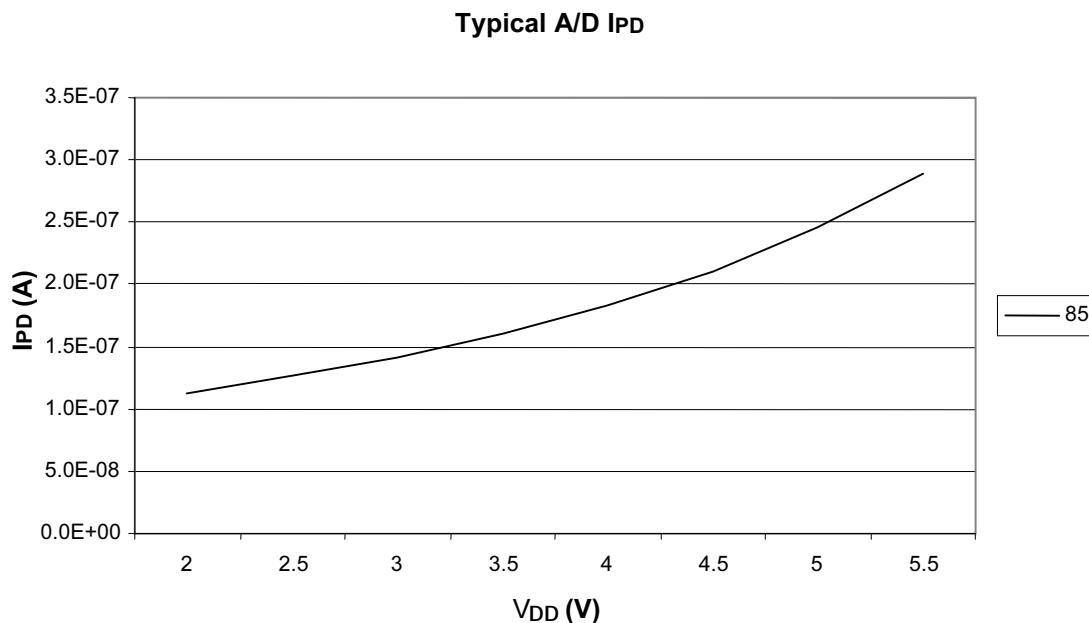


FIGURE 13-10: TYPICAL IPD WITH A/D ENABLED vs. V_{DD} OVER TEMP (+85°C)



PIC12F629/675

FIGURE 13-11: TYPICAL IPD WITH A/D ENABLED vs. V_{DD} OVER TEMP (+125°C)

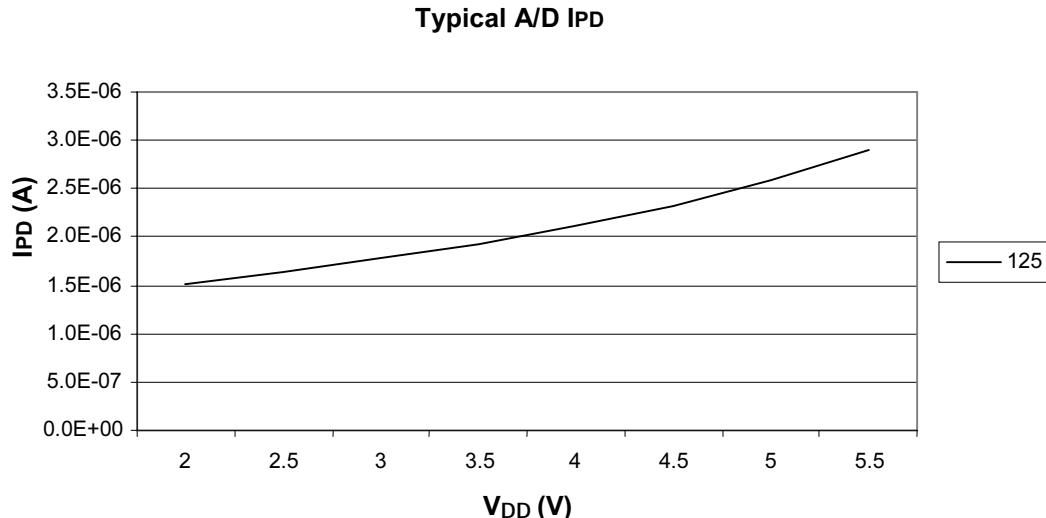


FIGURE 13-12: TYPICAL IPD WITH T1 OSC ENABLED vs. V_{DD} OVER TEMP (-40°C TO +125°C), 32 KHZ, C₁ AND C₂=50 pF

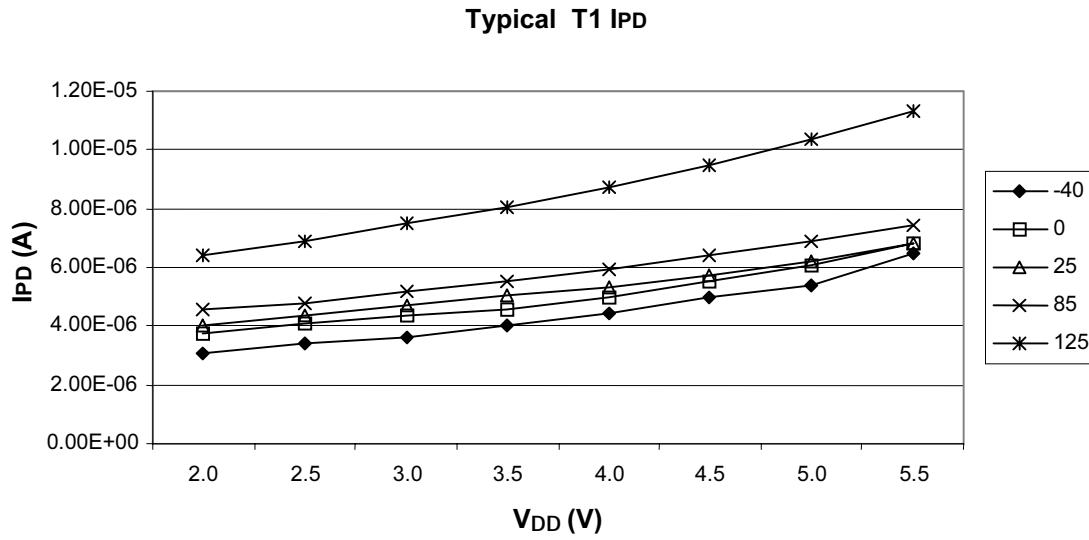


FIGURE 13-13: TYPICAL IPD WITH CVREF ENABLED vs. VDD OVER TEMP (-40°C TO +125°C)

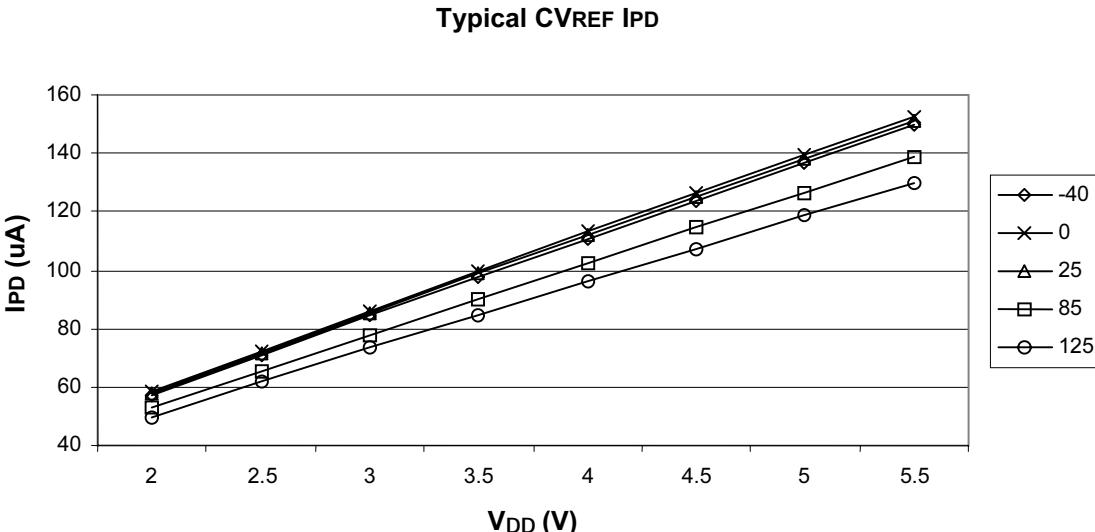
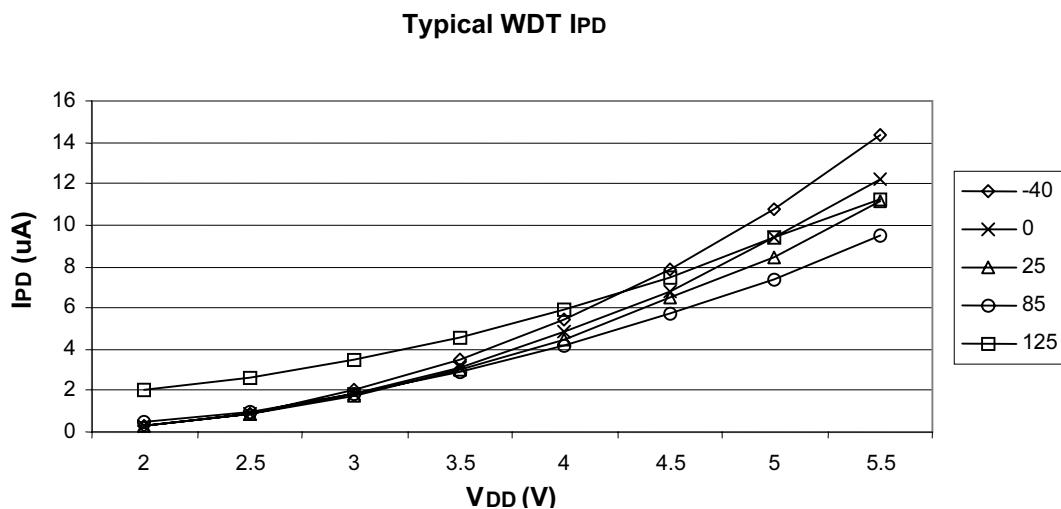


FIGURE 13-14: TYPICAL IPD WITH WDT ENABLED vs. VDD OVER TEMP (-40°C TO +125°C)



PIC12F629/675

FIGURE 13-15: MAXIMUM AND MINIMUM INTOSC FREQ vs. TEMPERATURE WITH $0.1\mu\text{F}$ AND $0.01\mu\text{F}$ DECOUPLING ($\text{VDD} = 3.5\text{V}$)

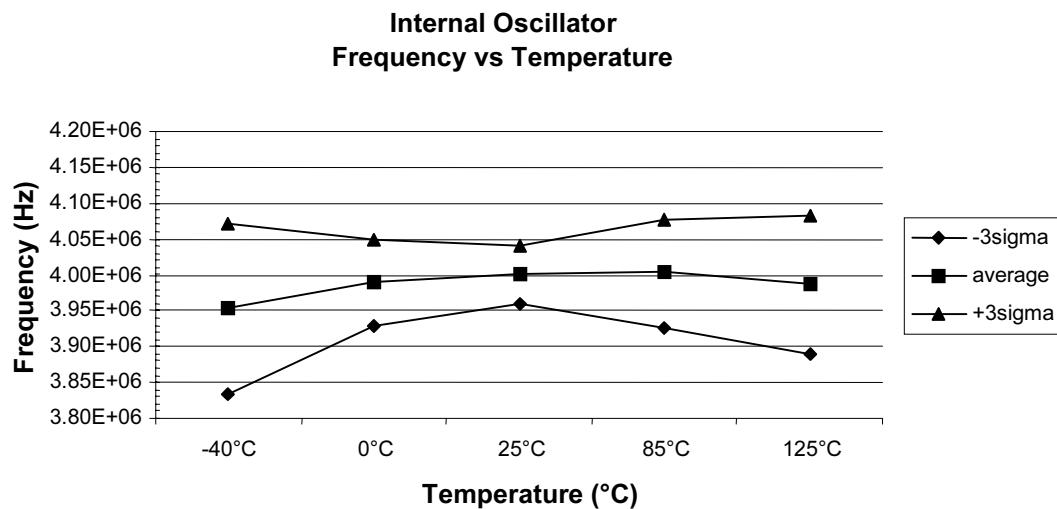


FIGURE 13-16: MAXIMUM AND MINIMUM INTOSC FREQ vs. VDD WITH $0.1\mu\text{F}$ AND $0.01\mu\text{F}$ DECOUPLING (+25°C)

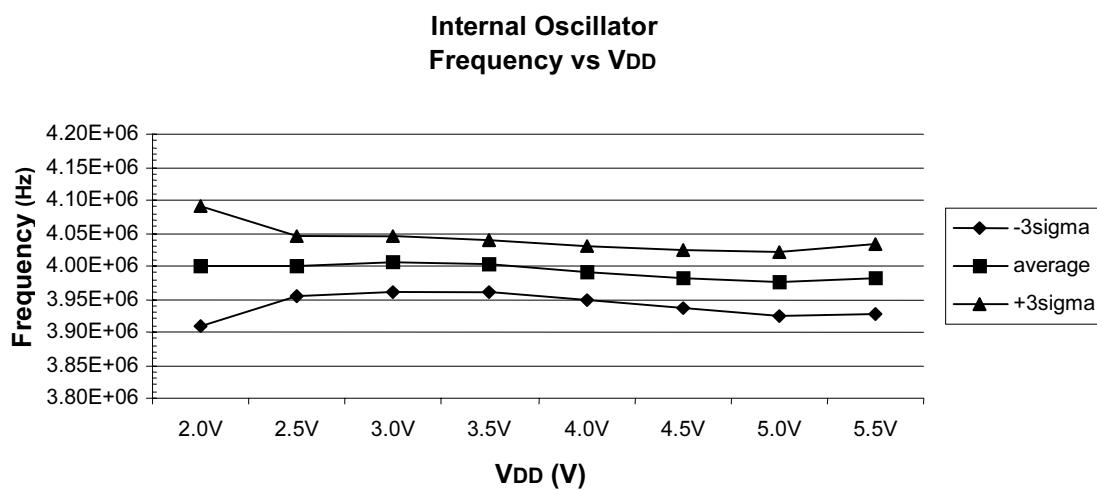
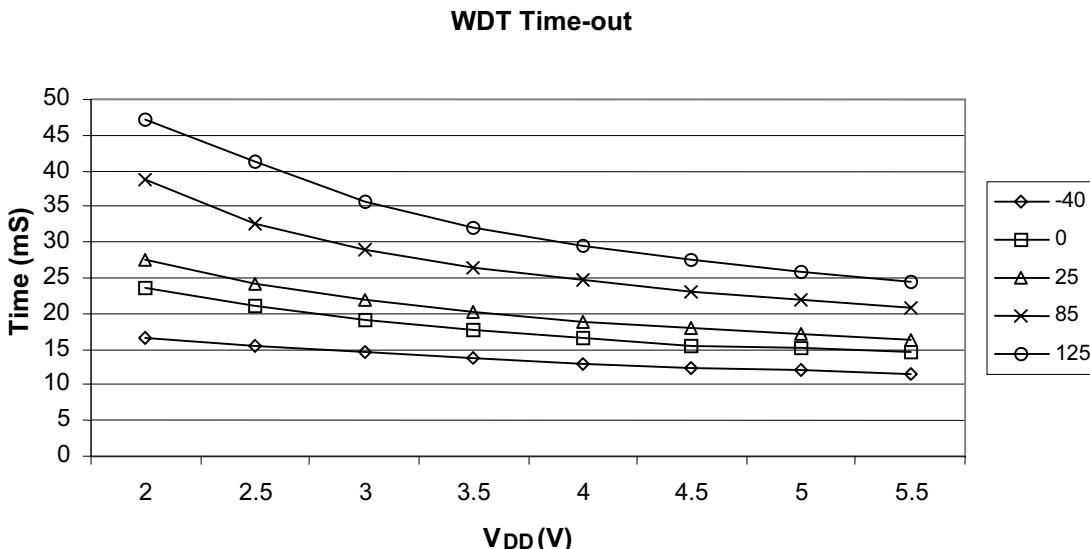


FIGURE 13-17: TYPICAL WDT PERIOD vs. V_{DD} (-40°C TO +125°C)



PIC12F629/675

NOTES:

14.0 PACKAGING INFORMATION

14.1 Package Marking Information

8-Lead PDIP (Skinny DIP)

XXXXXXX
XXXXXNNN
○  YYWW

Example

12F629-I
/017
○  0215

8-Lead SOIC

XXXXXXX
XXXXYYWW
○  NNN

Example

12F629-E
/0215
○  017

8-Lead DFN-S

XXXXXXX
XXXXXXX
XXYYWW
○  NNN

Example

12F629
-E/021
0215
○  017

Legend:

XX...X	Customer specific information*
Y	Year code (last digit of calendar year)
YY	Year code (last 2 digits of calendar year)
WW	Week code (week of January 1 is week '01')
NNN	Alphanumeric traceability code

Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line thus limiting the number of available characters for customer specific information.

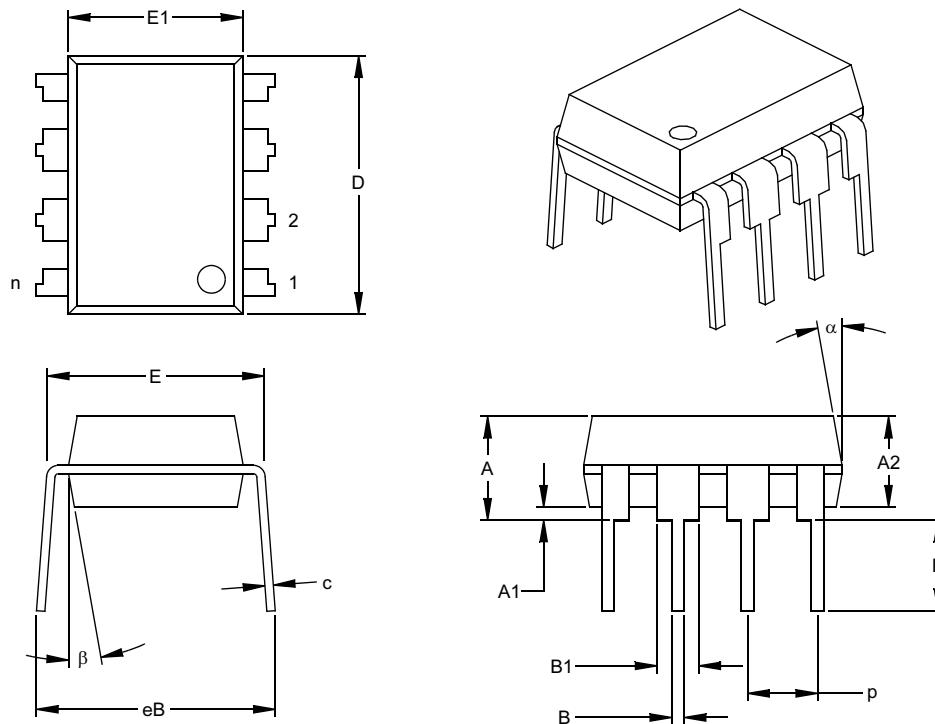
- * Standard PICmicro device marking consists of Microchip part number, year code, week code, and traceability code. For PICmicro device marking beyond this, certain price adders apply. Please check with your Microchip Sales Office. For QTP devices, any special marking adders are included in QTP price.

PIC12F629/675

14.2 Package Details

The following sections give the technical details of the packages.

8-Lead Plastic Dual In-line (P) – 300 mil (PDIP)



Units		INCHES*			MILLIMETERS		
Dimension	Limits	MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n			.8			.8
Pitch	p			.100			2.54
Top to Seating Plane	A	.140	.155	.170	3.56	3.94	4.32
Molded Package Thickness	A2	.115	.130	.145	2.92	3.30	3.68
Base to Seating Plane	A1	.015			0.38		
Shoulder to Shoulder Width	E	.300	.313	.325	7.62	7.94	8.26
Molded Package Width	E1	.240	.250	.260	6.10	6.35	6.60
Overall Length	D	.360	.373	.385	9.14	9.46	9.78
Tip to Seating Plane	L	.125	.130	.135	3.18	3.30	3.43
Lead Thickness	c	.008	.012	.015	0.20	0.29	0.38
Upper Lead Width	B1	.045	.058	.070	1.14	1.46	1.78
Lower Lead Width	B	.014	.018	.022	0.36	0.46	0.56
Overall Row Spacing	§ eB	.310	.370	.430	7.87	9.40	10.92
Mold Draft Angle Top	α	5	10	15	5	10	15
Mold Draft Angle Bottom	β	5	10	15	5	10	15

* Controlling Parameter

§ Significant Characteristic

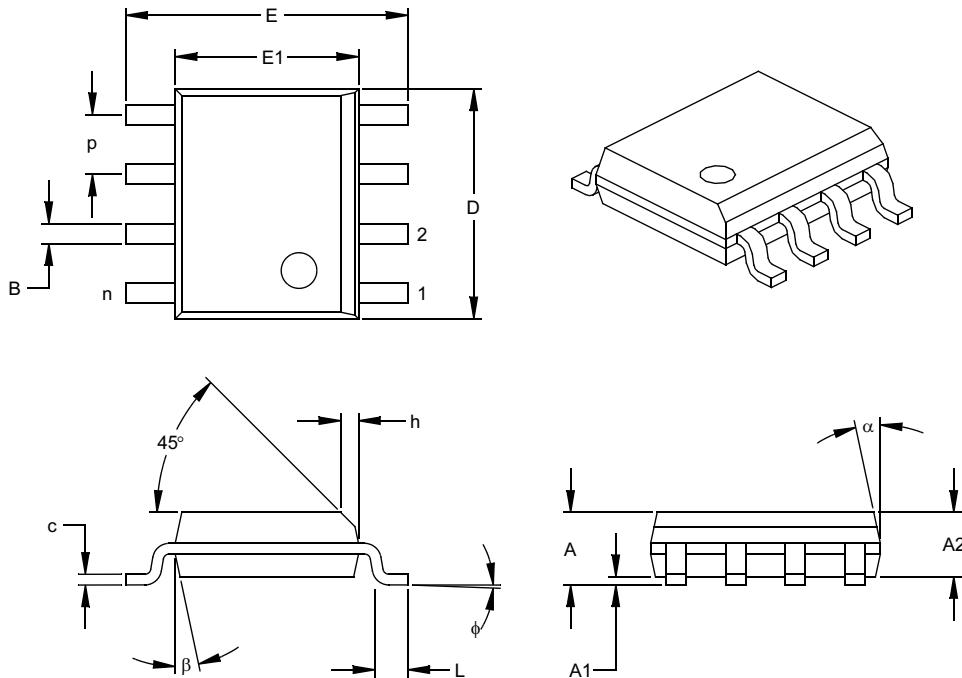
Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-001

Drawing No. C04-018

8-Lead Plastic Small Outline (SN) – Narrow, 150 mil (SOIC)



Dimension Limits		INCHES*			MILLIMETERS		
		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p		.050			1.27	
Overall Height	A	.053	.061	.069	1.35	1.55	1.75
Molded Package Thickness	A2	.052	.056	.061	1.32	1.42	1.55
Standoff §	A1	.004	.007	.010	0.10	0.18	0.25
Overall Width	E	.228	.237	.244	5.79	6.02	6.20
Molded Package Width	E1	.146	.154	.157	3.71	3.91	3.99
Overall Length	D	.189	.193	.197	4.80	4.90	5.00
Chamfer Distance	h	.010	.015	.020	0.25	0.38	0.51
Foot Length	L	.019	.025	.030	0.48	0.62	0.76
Foot Angle	ϕ	0	4	8	0	4	8
Lead Thickness	c	.008	.009	.010	0.20	0.23	0.25
Lead Width	B	.013	.017	.020	0.33	0.42	0.51
Mold Draft Angle Top	α	0	12	15	0	12	15
Mold Draft Angle Bottom	β	0	12	15	0	12	15

* Controlling Parameter

§ Significant Characteristic

Notes:

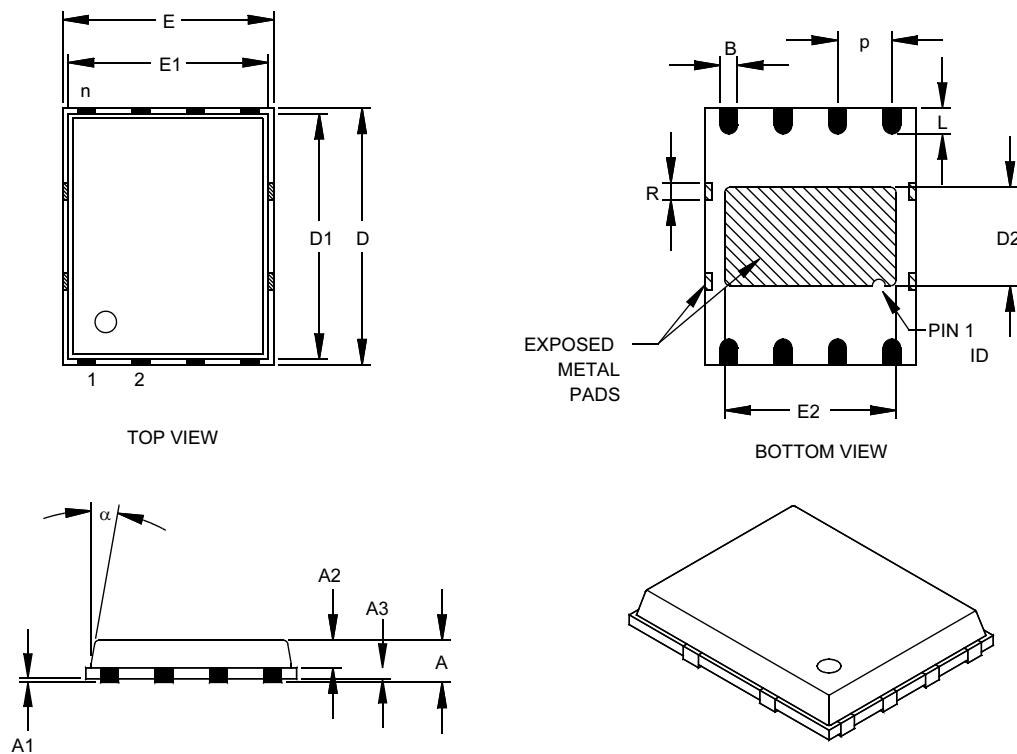
Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.

JEDEC Equivalent: MS-012

Drawing No. C04-057

PIC12F629/675

8-Lead Plastic Dual Flat No Lead Package (MF) 6x5 mm Body (DFN-S)



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		8			8	
Pitch	p	.050	BSC		1.27	BSC	
Overall Height	A	.033	.039		0.85	1.00	
Molded Package Thickness	A2	.026	.031		0.65	0.80	
Standoff	A1	.000	.0004	.002	0.00	0.01	0.05
Base Thickness	A3	.008 REF.			0.20 REF.		
Overall Length	E	.194 BSC			4.92 BSC		
Molded Package Length	E1	.184 BSC			4.67 BSC		
Exposed Pad Length	E2	.152	.158	.163	3.85	4.00	4.15
Overall Width	D	.236 BSC			5.99 BSC		
Molded Package Width	D1	.226 BSC			5.74 BSC		
Exposed Pad Width	D2	.085	.091	.097	2.16	2.31	2.46
Lead Width	B	.014	.016	.019	0.35	0.40	0.47
Lead Length	L	.020	.024	.030	0.50	0.60	0.75
Tie Bar Width	R		.014			.356	
Mold Draft Angle Top	α			12°			12°

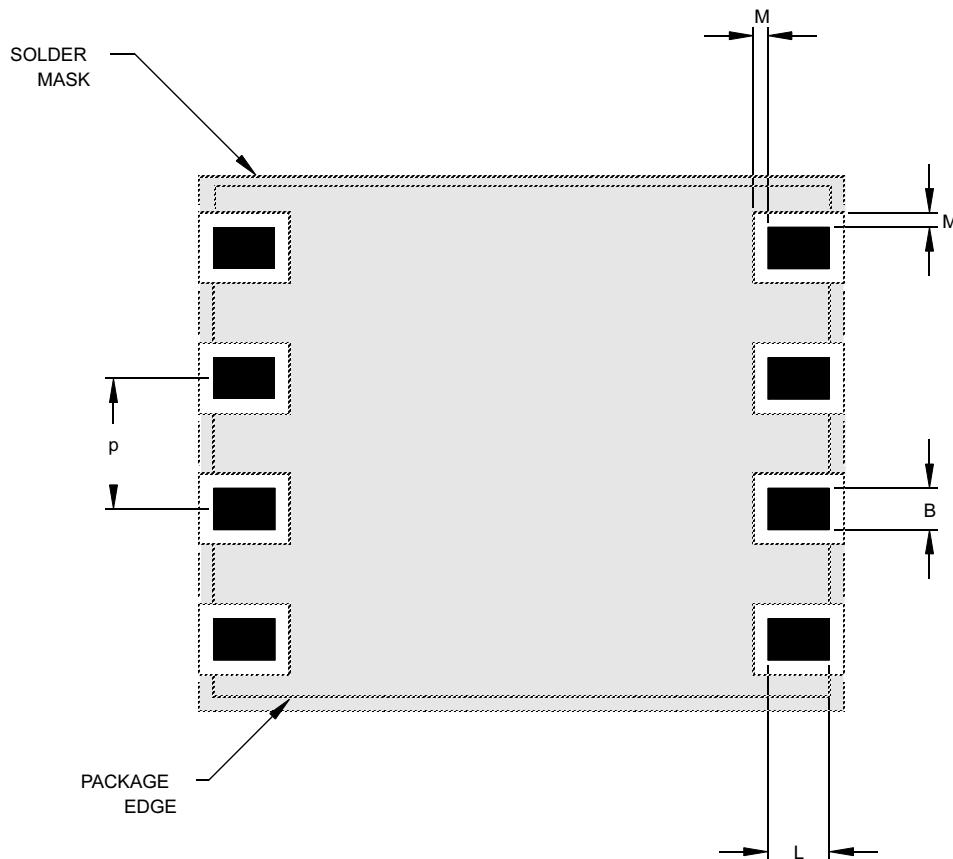
*Controlling Parameter

Notes:

Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed .010" (0.254mm) per side.
JEDEC equivalent: pending

Drawing No. C04-113

**8-Lead Plastic Dual Flat No Lead Package (MF) 6x5 mm Body (DFN-S)
Land Pattern and Solder Mask**



Units		INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Pitch	p		.050	BSC		1.27	BSC
Pad Width	B	.014	.016	.019	.035	.040	.047
Pad Length	L	.020	.024	.030	.050	.060	.075
Pad to Solder Mask	M	.005		.006	.013		.015

*Controlling Parameter

Drawing No. C04-2113

PIC12F629/675

NOTES:

APPENDIX A: DATA SHEET REVISION HISTORY

Revision A

This is a new data sheet.

Revision B

Added characterization graphs.

Updated specifications.

Added notes to indicate Microchip programmers maintain all calibration bits to factory settings and the PIC12F675 ANSEL register must be initialized to configure pins as digital I/O.

Updated MLF-S package name to DFN-S.

APPENDIX B: DEVICE DIFFERENCES

The differences between the PIC12F629/675 devices listed in this data sheet are shown in Table B-1.

TABLE B-1: DEVICE DIFFERENCES

Feature	PIC12F629	PIC12F675
A/D	No	Yes

PIC12F629/675

APPENDIX C: DEVICE MIGRATIONS

This section is intended to describe the functional and electrical specification differences when migrating between functionally similar devices (such as from a PIC16C74A to a PIC16C74B).

Not Applicable

APPENDIX D: MIGRATING FROM OTHER PICmicro® DEVICES

This discusses some of the issues in migrating from other PICmicro devices to the PIC12F6XX family of devices.

D.1 PIC12C67X to PIC12F6XX

TABLE 1: FEATURE COMPARISON

Feature	PIC12C67X	PIC12F6XX
Max Operating Speed	10 MHz	20 MHz
Max Program Memory	2048 bytes	1024 bytes
A/D Resolution	8-bit	10-bit
Data EEPROM	16 bytes	64 bytes
Oscillator Modes	5	8
Brown-out Detect	N	Y
Internal Pull-ups	GP0/1/3	GP0/1/2/4/5
Interrupt-on-change	GP0/1/3	GP0/1/2/3/4/5
Comparator	N	Y

Note: This device has been designed to perform to the parameters of its data sheet. It has been tested to an electrical specification designed to determine its conformance with these parameters. Due to process differences in the manufacture of this device, this device may have different performance characteristics than its earlier version. These differences may cause this device to perform differently in your application than the earlier version of this device.

INDEX

A

A/D	41
Acquisition Requirements	45
Block Diagram.....	41
Calculating Acquisition Time.....	45
Configuration and Operation.....	41
Effects of a RESET.....	46
Internal Sampling Switch (Rss) Impedance	45
Operation During SLEEP	46
PIC12F675 Converter Characteristics	101
Source Impedance.....	45
Summary of Registers	46
Absolute Maximum Ratings	83
AC Characteristics	
Industrial and Extended	94
Additional Pin Functions	19
Interrupt-on-Change.....	21
Weak Pull-up.....	19
Analog Input Connection Considerations.....	38
Analog-to-Digital Converter. See A/D	
Assembler	
MPASM Assembler.....	77
B	
Block Diagram	
TMR0/WDT Prescaler.....	27
Block Diagrams	
Analog Input Mode.....	38
Analog Input Model.....	45
Comparator Output	38
Comparator Voltage Reference	39
GP0 and GP1 Pins.....	22
GP2.....	23
GP3.....	23
GP4.....	24
GP5.....	24
On-Chip Reset Circuit.....	55
RC Oscillator Mode.....	54
Timer1	30
Watchdog Timer.....	65
Brown-out	
Associated Registers	58
Brown-out Detect (BOD)	57
Brown-out Detect Timing and Characteristics.....	97
C	
C Compilers	
MPLAB C17	78
MPLAB C18	78
MPLAB C30	78
Calibrated Internal RC Frequencies.....	95
CLKOUT	54
Code Examples	
Changing Prescaler	29
Data EEPROM Read	49
Data EEPROM Write	49
Initializing GPIO	19
Saving STATUS and W Registers in RAM	64
Write Verify	49
Code Protection	67
Comparator	35
Associated Registers	40
Configuration.....	37
Effects of a RESET	39
I/O Operating Modes.....	37
Interrupts.....	40

Operation.....	36
Operation During SLEEP	39
Output.....	38
Reference	39
Response Time	39
Comparator Specifications.....	100
Comparator Voltage Reference Specifications.....	100
Configuration Bits	52
Configuring the Voltage Reference.....	39
Crystal Operation.....	53

D

Data EEPROM Memory	
Associated Registers/Bits	50
Code Protection.....	50
EEADR Register	47
EECON1 Register	47
EECON2 Register	47
EEDATA Register.....	47
Data Memory Organization.....	7
DC Characteristics	
Extended and Industrial.....	91
Industrial	86
Demonstration Boards	
PICDEM 1.....	80
PICDEM 17.....	80
PICDEM 18R PIC18C601/801	81
PICDEM 2 Plus.....	80
PICDEM 3 PIC16C92X.....	80
PICDEM LIN PIC16C43X	81
PICDEM USB PIC16C7X5	81
PICDEM.net Internet/Ethernet.....	80
Development Support	77
Device Differences.....	121
Device Migrations	122
Device Overview.....	5

E

EEPROM Data Memory	
Reading	49
Spurious Write	49
Write Verify	49
Writing	49
Electrical Specifications	83
Errata	3
Evaluation and Programming Tools.....	81

F

Firmware Instructions	69
-----------------------------	----

G

General Purpose Register File	7
GPIO	
Associated Registers	25
GPIO Port	19
GPIO, TRISIO Registers.....	19

I

ID Locations	67
In-Circuit Debugger	67
In-Circuit Serial Programming	67
Indirect Addressing, INDF and FSR Registers	18
Instruction Format	69
Instruction Set	69
ADDLW	71
ADDWF	71
ANDLW	71
ANDWF	71
BCF	71

PIC12F629/675

BSF	71
BTFSC	71
BTFSS	71
CALL	72
CLRF	72
CLRW	72
CLRWD	72
COMF	72
DECFSZ	72
GOTO	73
INCF	73
INCFSZ	73
IORLW	73
IORWF	73
MOVF	74
MOVWF	74
NOP	74
RETFIE	74
RETLW	74
RETURN	75
RLF	75
RRF	75
SLEEP	75
SUBLW	75
SUBWF	75
SWAPF	76
XORLW	76
XORWF	76
Summary Table	70
Internal 4 MHz Oscillator	54
Internal Sampling Switch (Rss) Impedance	45
Interrupts	61
A/D Converter	63
Comparator	63
Context Saving	64
GP2/INT	63
GPIO	63
Summary of Registers	64
TMR0	63
M	
MCLR	56
Memory Organization	
Data EEPROM Memory	47
Migrating from other PICmicro Devices	122
MPLAB ASM30 Assembler, Linker, Librarian	78
MPLAB ICD 2 In-Circuit Debugger	79
MPLAB ICE 2000 High Performance Universal In-Circuit Emulator	79
MPLAB ICE 4000 High Performance Universal In-Circuit Emulator	79
MPLAB Integrated Development Environment Software	77
MPLINK Object Linker/MPLIB Object Librarian	78
O	
OPCODE Field Descriptions	69
Oscillator Configurations	53
Oscillator Start-up Timer (OST)	56
P	
Packaging	115
Details	116
Marking	115
PCL and PCLATH	17
Computed GOTO	17
Stack	17
PICkit 1 FLASH Starter Kit	81
PICSTART Plus Development Programmer	79
Pin Descriptions and Diagrams	22
Pinout Descriptions	
PIC12F629	6
PIC12F675	6
Power Control/Status Register (PCON)	57
Power-Down Mode (SLEEP)	66
Power-on Reset (POR)	56
Power-up Timer (PWRT)	56
Prescaler	29
Switching Prescaler Assignment	29
PRO MATE II Universal Device Programmer	79
Program Memory Organization	7
Programming, Device Instructions	69
R	
RC Oscillator	54
READ-MODIFY-WRITE OPERATIONS	69
Registers	
ADCON0 (A/D Control)	43
ANSEL (Analog Select)	44
CMCON (Comparator Control)	35
CONFIG (Configuration Word)	52
EEADR (EEPROM Address)	47
EECON1 (EEPROM Control)	48
EEDAT (EEPROM Data)	47
INTCON (Interrupt Control)	13
IOC (Interrupt-on-Change GPIO)	21
Maps	
PIC12F629	8
PIC12F675	8
OPTION_REG (Option)	12, 28
OSCCAL (Oscillator Calibration)	16
PCON (Power Control)	16
PIE1 (Peripheral Interrupt Enable 1)	14
PIR1 (Peripheral Interrupt 1)	15
STATUS	11
T1CON (Timer1 Control)	32
VRCON (Voltage Reference Control)	40
WPU (Weak Pull-up)	20
RESET	55
Revision History	121
S	
Software Simulator (MPLAB SIM)	78
Software Simulator (MPLAB SIM30)	78
Special Features of the CPU	51
Special Function Registers	8
Special Functions Registers Summary	9
T	
Time-out Sequence	57
Timer0	27
Associated Registers	29
External Clock	28
Interrupt	27
Operation	27
T0CKI	28
Timer1	
Associated Registers	33
Asynchronous Counter Mode	33
Reading and Writing	33
Interrupt	31
Modes of Operations	31
Operation During SLEEP	33
Oscillator	33

Prescaler.....	31
Timer1 Module with Gate Control	30
Timing Diagrams	
CLKOUT and I/O.....	96
External Clock.....	94
INT Pin Interrupt.....	63
PIC12F675 A/D Conversion (Normal Mode).....	102
PIC12F675 A/D Conversion Timing (SLEEP Mode).....	103
RESET, Watchdog Timer, Oscillator Start-up	
Timer and Power-up Timer	97
Time-out Sequence on Power-up (<u>MCLR</u> not Tied to VDD)	
Case 1	60
Case 2	60
Time-out Sequence on Power-up (MCLR Tied to VDD).....	60
Timer0 and Timer1 External Clock	99
Timer1 Incrementing Edge.....	31
Timing Parameter Symbology.....	93
V	
Voltage Reference Accuracy/Error	39
W	
Watchdog Timer	
Summary of Registers	65
Watchdog Timer (WDT).....	64
WWW, On-Line Support	3

PIC12F629/675

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To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	X	/XX	XXX	
Device	Temperature Range	Package	Pattern	
Device		PIC12F6XX: Standard VDD range PIC12F6XXT: (Tape and Reel)		
Temperature Range	I = -40°C to +85°C E = -40°C to +125°C			
Package		P = PDIP SN = SOIC (Gull wing, 150 mil body) MF = MLF-S		
Pattern		3-Digit Pattern Code for QTP (blank otherwise)		

Examples:

- PIC12F629 – E/P 301 = Extended Temp., PDIP package, 20 MHz, QTP pattern #301
- PIC12F675 – I/SO = Industrial Temp., SOIC package, 20 MHz

* JW Devices are UV erasable and can be programmed to any device configuration. JW Devices meet the electrical requirement of each oscillator type.

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02/12/03

High-Speed CMOS Logic 16-Channel Analog Multiplexer/Demultiplexer

Features

- Wide Analog Input Voltage Range
- Low “ON” Resistance
 - $V_{CC} = 4.5V$ 70Ω (Typ)
 - $V_{CC} = 6V$ 60Ω (Typ)
- Fast Switching and Propagation Speeds
- “Break-Before-Make” Switching 6ns (Typ) at 4.5V
- Available in Both Narrow and Wide-Body Plastic Packages
- Fanout (Over Temperature Range)
 - Standard Outputs 10 LSTTL Loads
 - Bus Driver Outputs 15 LSTTL Loads
- Wide Operating Temperature Range -55°C to 125°C
- Balanced Propagation Delay and Transition Times
- Significant Power Reduction Compared to LSTTL Logic ICs
- HC Types
 - 2V to 6V Operation
 - High Noise Immunity: $N_{IL} = 30\%$, $N_{IH} = 30\%$ of V_{CC} at $V_{CC} = 5V$
- HCT Types
 - 4.5V to 5.5V Operation
 - Direct LSTTL Input Logic Compatibility, $V_{IL} = 0.8V$ (Max), $V_{IH} = 2V$ (Min)
 - CMOS Input Compatibility, $I_I \leq 1\mu A$ at V_{OL}, V_{OH}

Description

The CD74HC4067 and CD74HCT4067 devices are digitally controlled analog switches that utilize silicon-gate CMOS technology to achieve operating speeds similar to LSTTL, with the low power consumption of standard CMOS integrated circuits.

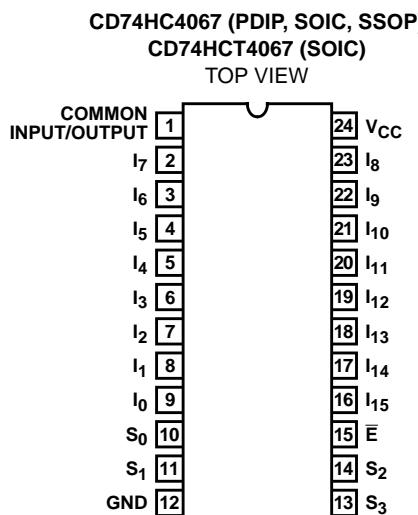
These analog multiplexers/demultiplexers control analog voltages that may vary across the voltage supply range. They are bidirectional switches thus allowing any analog input to be used as an output and vice-versa. The switches have low “on” resistance and low “off” leakages. In addition, these devices have an enable control which when high will disable all switches to their “off” state.

Ordering Information

PART NUMBER	TEMP. RANGE (°C)	PACKAGE
CD74HC4067E	-55 to 125	24 Ld PDIP
CD74HC4067M	-55 to 125	24 Ld SOIC
CD74HC4067M96	-55 to 125	24 Ld SOIC
CD74HC4067SM96	-55 to 125	24 Ld SSOP
CD74HCT4067M	-55 to 125	24 Ld SOIC

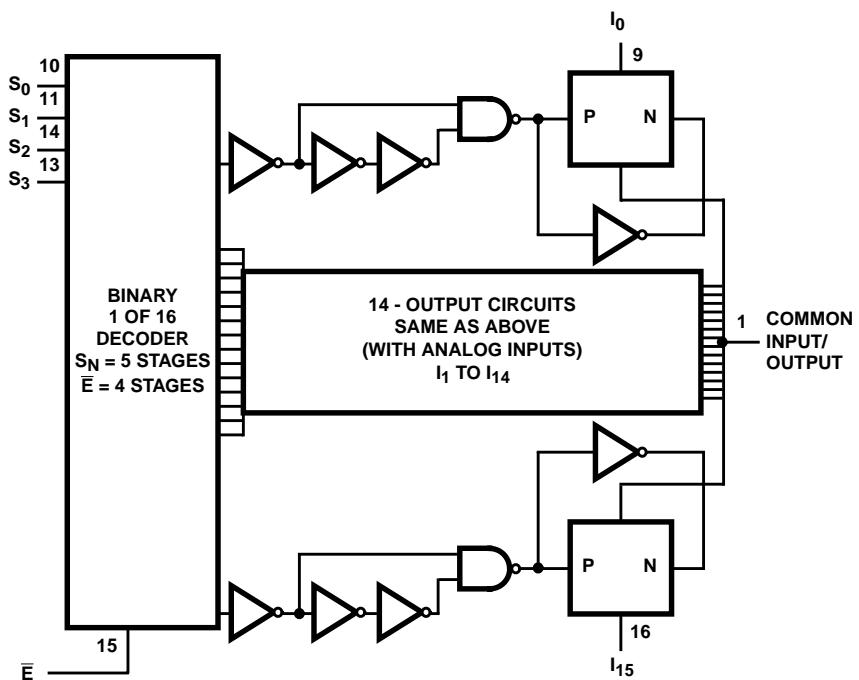
NOTE: When ordering, use the entire part number. The suffix 96 denotes tape and reel.

Pinout



CD74HC4067, CD74HCT4067

Functional Diagram



TRUTH TABLE

S0	S1	S2	S3	\bar{E}	SELECTED CHANNEL
X	X	X	X	1	None
0	0	0	0	0	0
1	0	0	0	0	1
0	1	0	0	0	2
1	1	0	0	0	3
0	0	1	0	0	4
1	0	1	0	0	5
0	1	1	0	0	6
1	1	1	0	0	7
0	0	0	1	0	8
1	0	0	1	0	9
0	1	0	1	0	10
1	1	0	1	0	11
0	0	1	1	0	12
1	0	1	1	0	13
0	1	1	1	0	14
1	1	1	1	0	15

H= High Level

L= Low Level

X= Don't Care

Absolute Maximum Ratings

DC Supply Voltage, V _{CC}	
(Voltages Referenced to Ground)	-0.5V to 7V
DC Input Diode Current, I _{IK}	
For V _I < -0.5V or V _I > V _{CC} + 0.5V	±20mA
DC Drain Current, I _O	
For -0.5V < V _O < V _{CC} + 0.5V	±25mA
DC Output Diode Current, I _{OK}	
For V _O < -0.5V or V _O > V _{CC} + 0.5V	±20mA
DC Output Source or Sink Current per Output Pin, I _O	
For V _O > -0.5V or V _O < V _{CC} + 0.5V	±25mA
DC V _{CC} or Ground Current, I _{CC}	±50mA

Thermal Information

Thermal Resistance (Typical)	θ _{JA} (°C/W)
E (PDIP) Package, Note 1	67
M (SOIC) Package, Note 2	46
SM (SSOP) Package, Note 2	63
Maximum Junction Temperature (Plastic Package)	150°C
Maximum Storage Temperature Range	-65°C to 150°C

Operating Conditions

Temperature Range, T _A	-55°C to 125°C
Supply Voltage Range, V _{CC}	
HC Types	2V to 6V	
HCT Types	4.5V to 5.5V	
DC Input or Output Voltage, V _I , V _O	0V to V _{CC}
Input Rise and Fall Time	
2V	1000ns (Max)	
4.5V	500ns (Max)	
6V	400ns (Max)	

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. The package thermal impedance is calculated in accordance with JESD 51-3.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

DC Electrical Specifications

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	V _{IS} (V)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES												
High Level Input Voltage	V _{IH}	-	-	2	1.5	-	-	1.5	-	1.5	-	V
				4.5	3.15	-	-	3.15	-	3.15	-	V
				6	4.2	-	-	4.2	-	4.2	-	V
Low Level Input Voltage	V _{IL}	-	-	2	-	-	0.5	-	0.5	-	0.5	V
				4.5	-	-	1.35	-	1.35	-	1.35	V
				6	-	-	1.8	-	1.8	-	1.8	V
Maximum "ON" Resistance I _O = 1mA	R _{ON}	V _{CC} or GND	V _{CC} or GND	4.5	-	70	160	-	200	-	240	Ω
				6	-	60	140	-	175	-	210	Ω
		V _{CC} to GND	V _{CC} to GND	4.5	-	90	180	-	225	-	270	Ω
				6	-	80	160	-	200	-	240	Ω
Maximum "ON" Resistance Between Any Two Switches	ΔR _{ON}	-	-	4.5	-	10	-	-	-	-	-	Ω
				6	-	8.5	-	-	-	-	-	Ω
Switch "Off" Leakage Current 16 Channels	I _{IZ}	Ē = V _{CC}	V _{CC} or GND	6	-	-	±0.8	-	±8	-	±8	µA
Logic Input Leakage Current	I _I	V _{CC} or GND	-	6	-	-	±0.1	-	±1	-	±1	µA

CD74HC4067, CD74HCT4067

DC Electrical Specifications (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS		V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
		V _I (V)	V _{IS} (V)		MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Quiescent Device Current I _O = 0mA	I _{CC}	V _{CC} or GND	-	6	-	-	8	-	80	-	160	µA
HCT TYPES												
High Level Input Voltage	V _{IH}	-	-	4.5	2	-	-	2	-	2	-	V
Low Level Input Voltage	V _{IL}	-	-	4.5	-	-	0.8	-	0.8	-	0.8	V
Maximum "ON" Resistance I _O = 1mA	R _{ON}	V _{CC} or GND	V _{CC} or GND	4.5	-	70	160	-	200	-	240	Ω
		V _{CC} to GND	V _{CC} to GND	4.5	-	90	180	-	225	-	270	Ω
Maximum "ON" Resistance Between Any Two Switches	ΔR _{ON}	-	-	4.5	-	10	-	-	-	-	-	Ω
Switch "Off" Leakage Current 16 Channels	I _{IZ}	Ē = V _{CC}	V _{CC} or GND	6	-	-	±0.8	-	±8	-	±8	µA
Logic Input Leakage Current	I _I	V _{CC} or GND (Note 3)	-	6	-	-	±0.1	-	±1	-	±1	µA
Quiescent Device Current	I _{CC}	V _{CC} or GND	-	6	-	-	8	-	80	-	160	µA
Additional Quiescent Device Current Per Input Pin: 1 Unit Load	ΔI _{CC} (Note 4)	V _{CC} -2.1	-	-	-	100	360	-	450	-	490	µA

NOTES:

3. Any voltage between V_{CC} and GND.
4. For dual-supply systems theoretical worst case (V_I = 2.4V, V_{CC} = 5.5V) specification is 1.8mA.

HCT Input Loading Table

INPUT	UNIT LOAD
S ₀ - S ₃	0.5
Ē	0.3

NOTE: Unit Load is ΔI_{CC} limit specified in DC Electrical Specifications table, e.g., 360µA max at 25°C.

Switching Specifications Input t_r, t_f = 6ns

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
Propagation Delay Time Switch In to Out	t _{PLH} , t _{PHL}	C _L = 50pF	2	-	-	75	-	95	-	110	ns
			4.5	-	-	15	-	19	-	22	ns
			6	-	-	13	-	16	-	19	ns
			C _L = 15pF	5	-	6	-	-	-	-	ns

CD74HC4067, CD74HCT4067

Switching Specifications Input $t_r, t_f = 6\text{ns}$ (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	V _{CC} (V)	25°C			-40°C TO 85°C		-55°C TO 125°C		UNITS
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
Switch Turn On E to Out	t _{PZH} , t _{PZL}	C _L = 50pF	2	-	-	275	-	345	-	415	ns
			4.5	-	-	55	-	69	-	83	ns
			6	-	-	47	-	59	-	71	ns
		C _L = 15pF	5	-	23	-	-	-	-	-	ns
Switch Turn On Sn to Out	t _{PZH} , t _{PZL}	C _L = 50pF	2	-	-	300	-	375	-	450	ns
			4.5	-	-	60	-	75	-	90	ns
			6	-	-	51	-	64	-	76	ns
		C _L = 15pF	5	-	25	-	-	-	-	-	ns
Switch Turn Off E to Out	t _{PHZ} , t _{PLZ}	C _L = 50pF	2	-	-	275	-	345	-	415	ns
			4.5	-	-	55	-	69	-	83	ns
			6	-	-	47	-	59	-	71	ns
		C _L = 15pF	5	-	23	-	-	-	-	-	ns
Switch Turn Off Sn to Out	t _{PHZ} , t _{PLZ}	C _L = 50pF	2	-	-	290	-	365	-	435	ns
			4.5	-	-	58	-	73	-	87	ns
			6	-	-	49	-	62	-	74	ns
		C _L = 50pF	5	-	21	-	-	-	-	-	ns
Input (Control) Capacitance	C _I	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 5, 6)	C _{PD}	-	5	-	93	-	-	-	-	-	pF
HCT TYPES											
Propagation Delay Time Switch In to Out	t _{PLH} , t _{PHL}	C _L = 50pF	4.5	-	-	15	-	19	-	22	ns
		C _L = 15pF	5	-	6	-	-	-	-	-	ns
Switch Turn On E to Out	t _{PZH} , t _{PZL}	C _L = 50pF	4.5	-	-	60	-	75	-	90	ns
		C _L = 15pF	5	-	25	-	-	-	-	-	ns
Switch Turn On Sn to Out	t _{PZH} , t _{PZL}	C _L = 50pF	4.5	-	-	60	-	75	-	90	ns
		C _L = 15pF	5	-	25	-	-	-	-	-	ns
Switch Turn Off E to Out	t _{PHZ} , t _{PLZ}	C _L = 50pF	4.5	-	-	55	-	69	-	83	ns
		C _L = 15pF	5	-	23	-	-	-	-	-	ns
Switch Turn Off Sn to Out	t _{PHZ} , t _{PLZ}	C _L = 50pF	4.5	-	-	58	-	73	-	87	ns
		C _L = 15pF	5	-	21	-	-	-	-	-	ns
Input (Control) Capacitance	C _I	-	-	-	-	10	-	10	-	10	pF
Power Dissipation Capacitance (Notes 5, 6)	C _{PD}	-	5	-	96	-	-	-	-	-	pF

NOTES:

5. C_{PD} is used to determine the dynamic power consumption, per package.
6. P_D = C_{PD} V_{CC}² f_i + Σ (C_L + C_S) V_{CC}² f_o where f_i = input frequency, f_o = output frequency, C_L = output load capacitance, C_S = switch capacitance, V_{CC} = supply voltage.

Analog Channel Specifications $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	V_{CC} (V)	HC/HCT	UNITS
Switch Frequency Response Bandwidth at -3dB (Figure 2)	Figure 4, Notes 7, 8	4.5	89	MHz
Sine Wave Distortion	Figure 5	4.5	0.051	%
Feedthrough Noise \bar{E} to Switch	Figure 6, Notes 8, 9	4.5	TBE	mV
Feedthrough Noise S to Switch			TBE	mV
Switch "OFF" Signal Feedthrough (Figure 3)	Figure 7	4.5	-75	dB
Switch Input Capacitance, C_S		-	5	pF
Common Capacitance, C_{COM}		-	50	pF

NOTES:

7. Adjust input level for 0dBm at output, $f = 1\text{MHz}$.
8. V_{IS} is centered at $V_{CC}/2$.
9. Adjust input for 0dBm at V_{IS} .

Typical Performance Curves

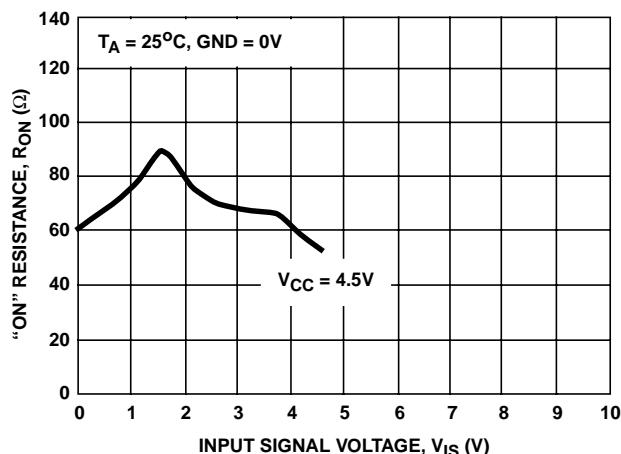


FIGURE 1. TYPICAL "ON" RESISTANCE vs INPUT SIGNAL VOLTAGE

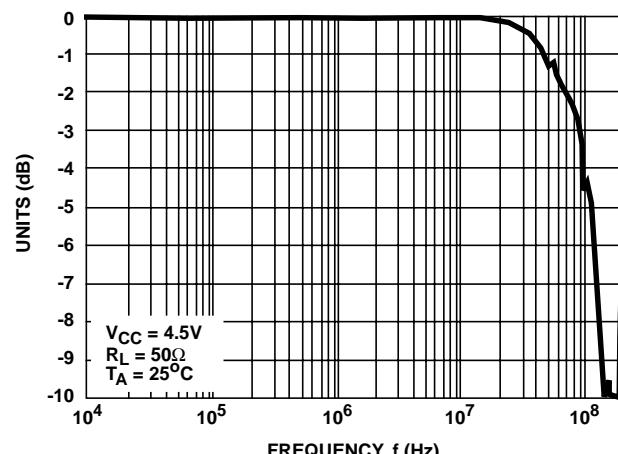


FIGURE 2. TYPICAL SWITCH FREQUENCY RESPONSE

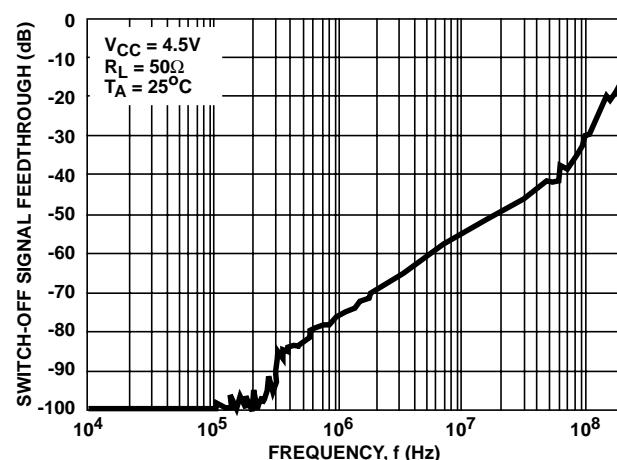


FIGURE 3. TYPICAL SWITCH-OFF SIGNAL FEEDTHROUGH vs FREQUENCY

Analog Test Circuits

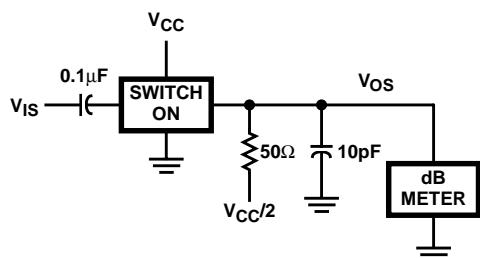


FIGURE 4. FREQUENCY RESPONSE TEST CIRCUIT

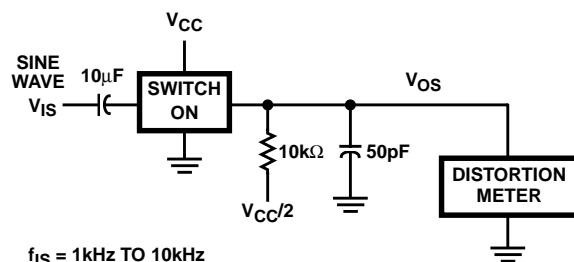


FIGURE 5. SINE WAVE DISTORTION TEST CIRCUIT

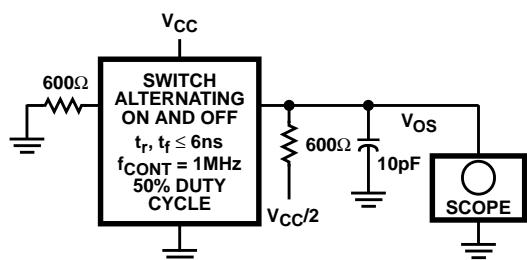


FIGURE 6. CONTROL-TO-SWITCH FEEDTHROUGH NOISE TEST CIRCUIT

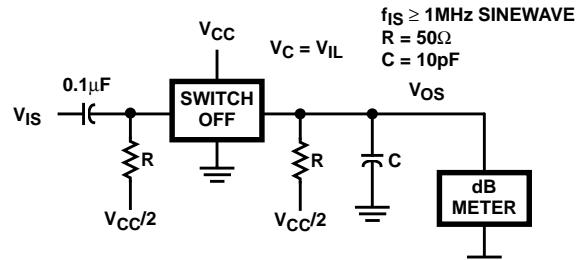


FIGURE 7. SWITCH OFF SIGNAL FEEDTHROUGH TEST CIRCUIT

Test Circuits and Waveforms

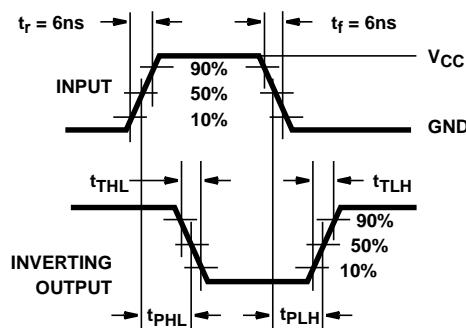


FIGURE 8. HC TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

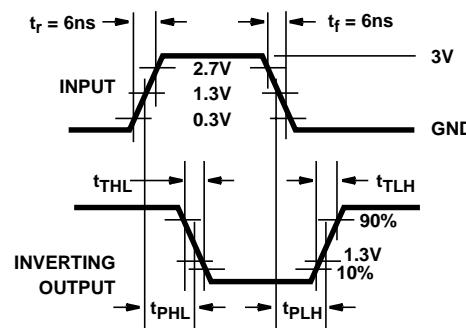


FIGURE 9. HCT TRANSITION TIMES AND PROPAGATION DELAY TIMES, COMBINATION LOGIC

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD74HC4067M	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4067M	Samples
CD74HC4067M96	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-55 to 125	HC4067M	Samples
CD74HC4067M96E4	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4067M	Samples
CD74HC4067M96G4	ACTIVE	SOIC	DW	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4067M	Samples
CD74HC4067MG4	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4067M	Samples
CD74HC4067SM96	ACTIVE	SSOP	DB	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HP4067	Samples
CD74HC4067SM96E4	ACTIVE	SSOP	DB	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HP4067	Samples
CD74HC4067SM96G4	ACTIVE	SSOP	DB	24	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HP4067	Samples
CD74HCT4067M	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4067M	Samples
CD74HCT4067ME4	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4067M	Samples
CD74HCT4067MG4	ACTIVE	SOIC	DW	24	25	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4067M	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.**OBSOLETE:** TI has discontinued the production of the device.(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.



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PACKAGE OPTION ADDENDUM

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(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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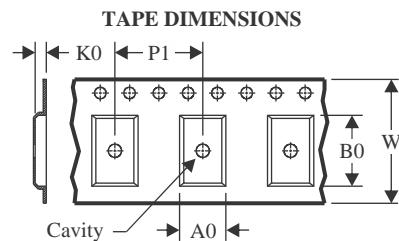
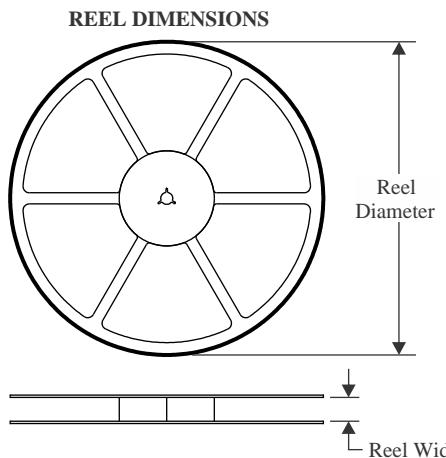
OTHER QUALIFIED VERSIONS OF CD74HCT4067 :

- Automotive : [CD74HCT4067-Q1](#)

NOTE: Qualified Version Definitions:

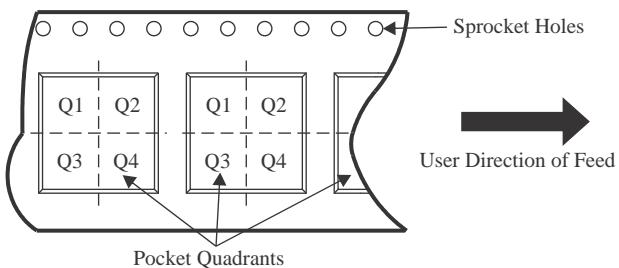
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



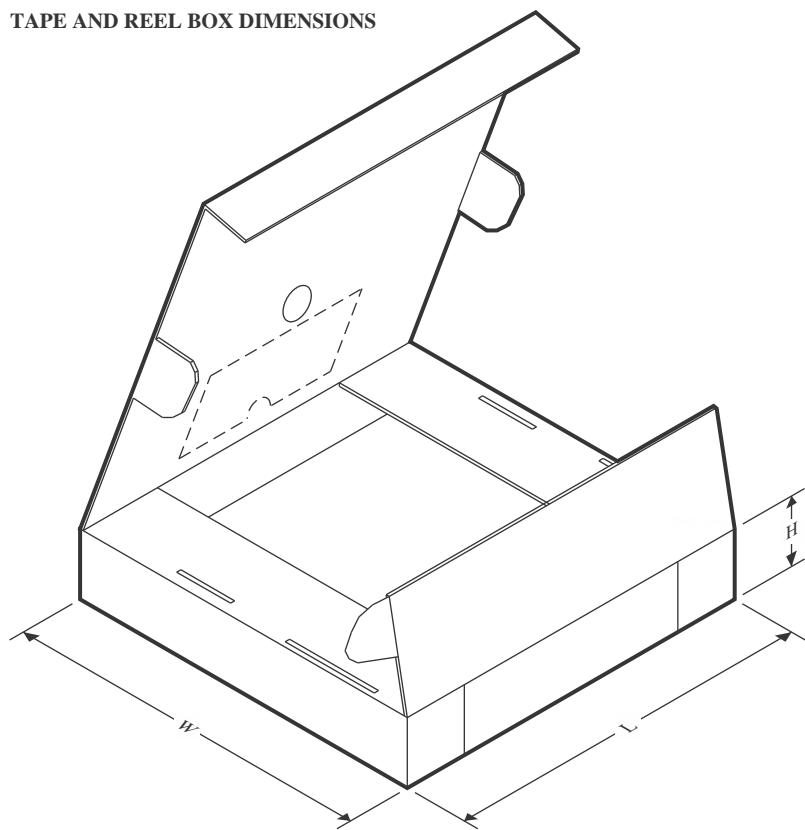
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



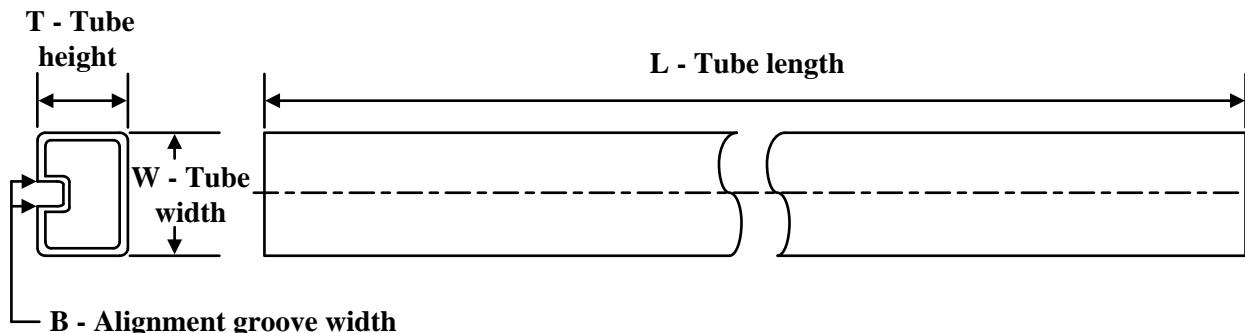
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4067M96	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
CD74HC4067M96	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
CD74HC4067M96G4	SOIC	DW	24	2000	330.0	24.4	10.75	15.7	2.7	12.0	24.0	Q1
CD74HC4067SM96	SSOP	DB	24	2000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4067M96	SOIC	DW	24	2000	364.0	361.0	36.0
CD74HC4067M96	SOIC	DW	24	2000	350.0	350.0	43.0
CD74HC4067M96G4	SOIC	DW	24	2000	350.0	350.0	43.0
CD74HC4067SM96	SSOP	DB	24	2000	356.0	356.0	35.0

TUBE


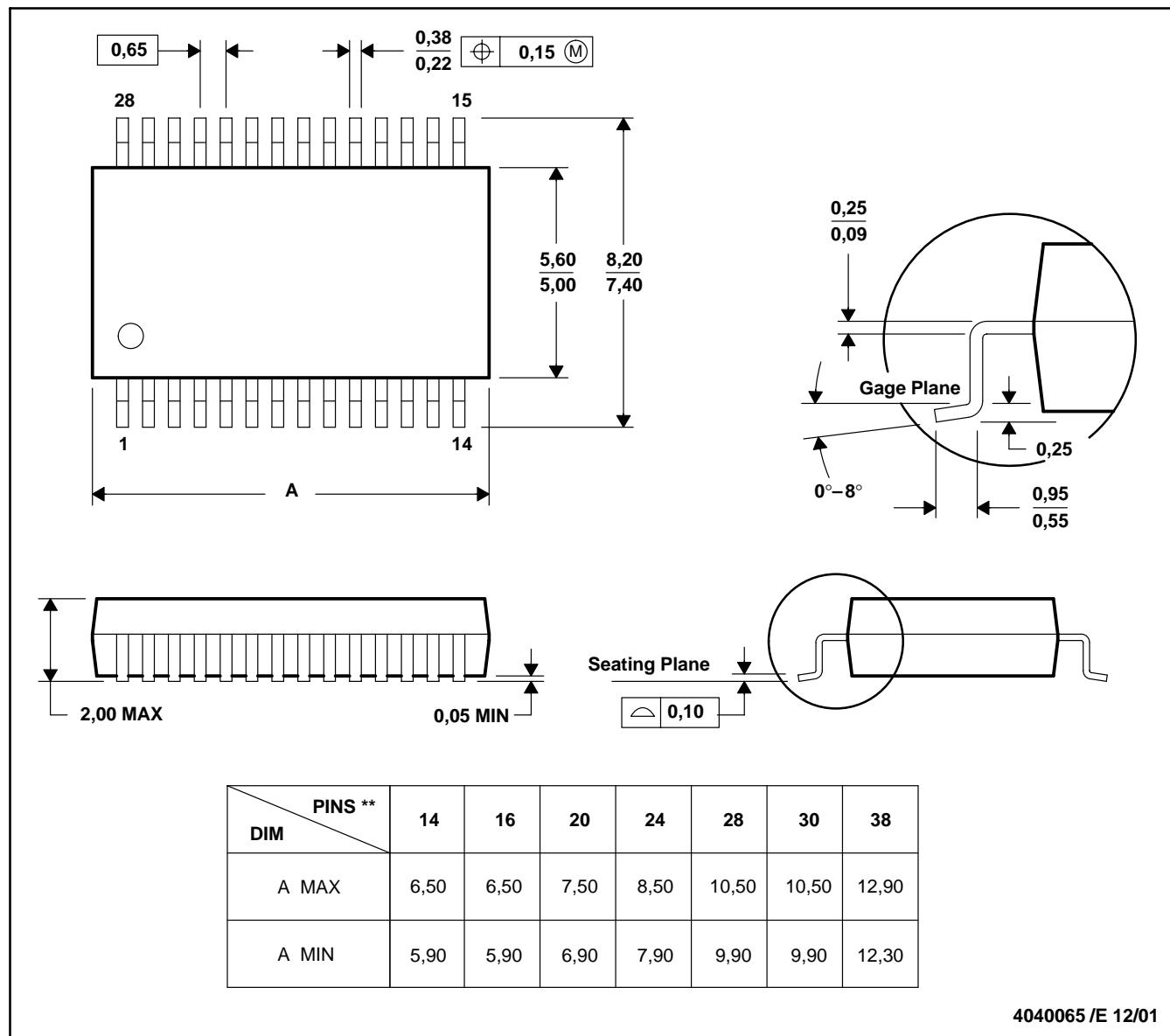
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μ m)	B (mm)
CD74HC4067M	DW	SOIC	24	25	506.98	12.7	4826	6.6
CD74HC4067MG4	DW	SOIC	24	25	506.98	12.7	4826	6.6
CD74HCT4067M	DW	SOIC	24	25	506.98	12.7	4826	6.6
CD74HCT4067ME4	DW	SOIC	24	25	506.98	12.7	4826	6.6
CD74HCT4067MG4	DW	SOIC	24	25	506.98	12.7	4826	6.6

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN

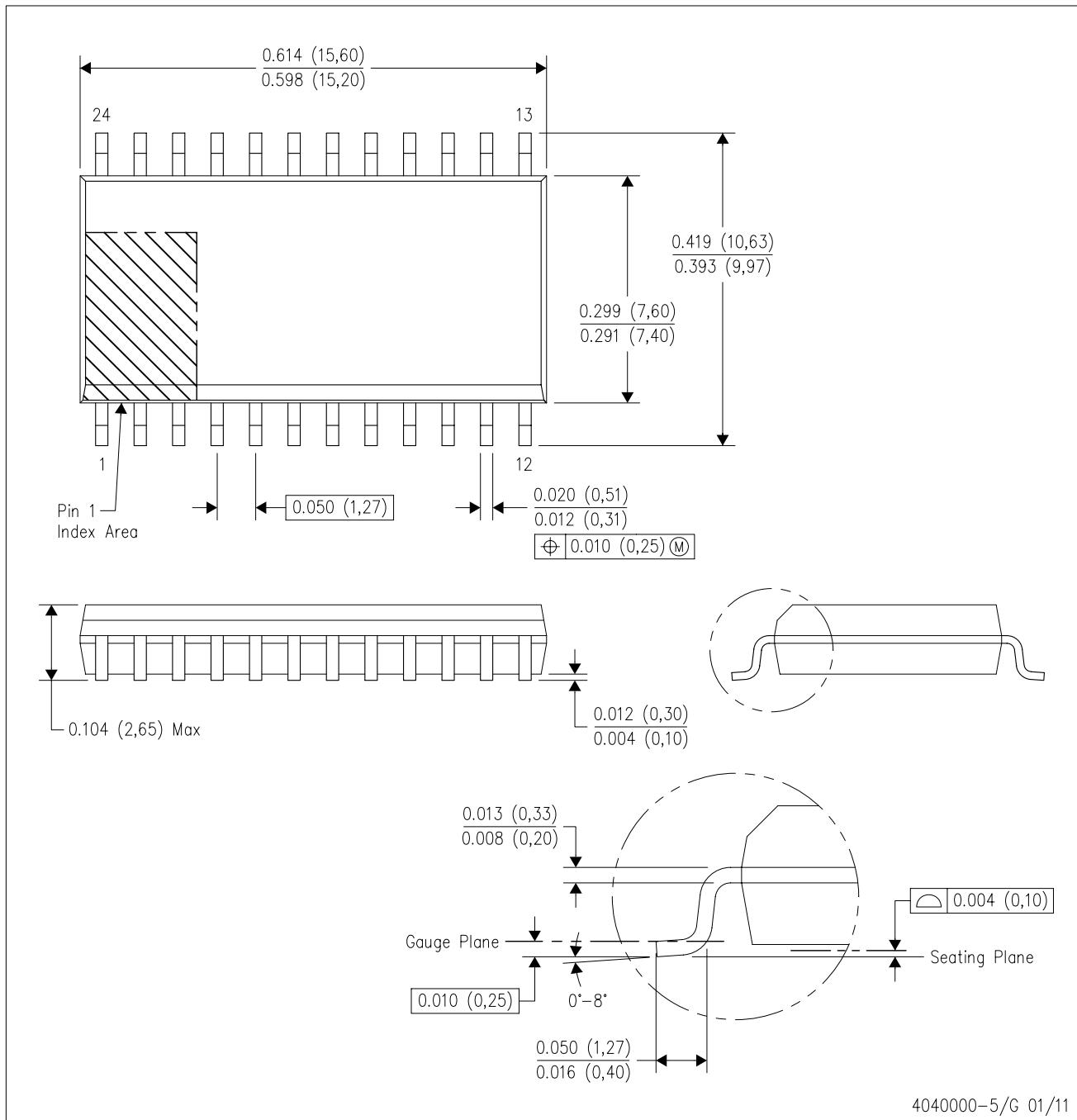


- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - D. Falls within JEDEC MO-150

MECHANICAL DATA

DW (R-PDSO-G24)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
 - D. Falls within JEDEC MS-013 variation AD.

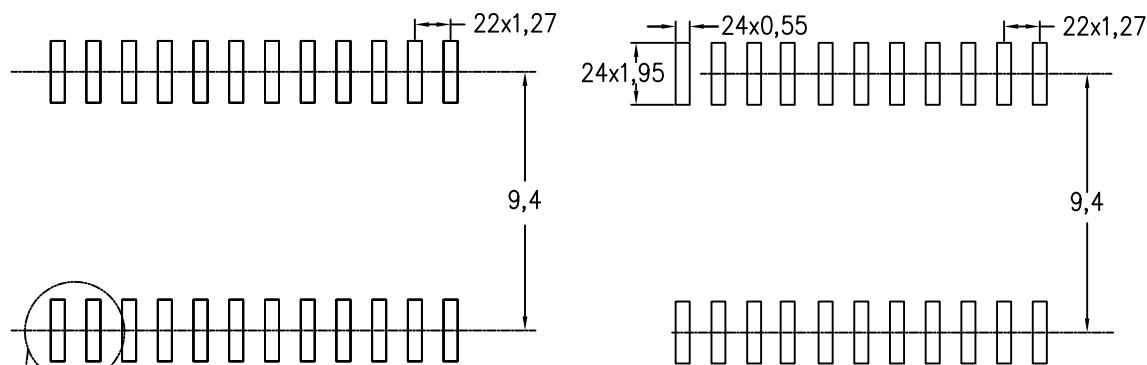
LAND PATTERN DATA

DW (R-PDSO-G24)

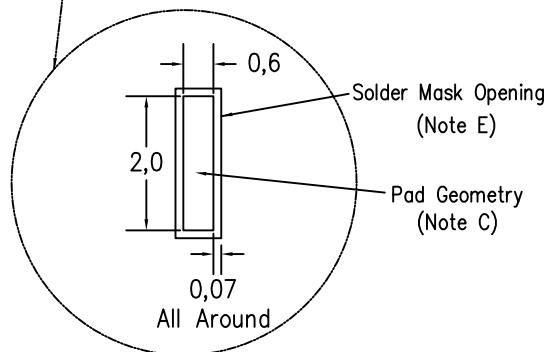
PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)

Stencil Openings
(Note D)



Non Solder Mask Define Pad



4209202-5/F 08/13

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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CMOS 8-STAGE STATIC SHIFT REGISTER

Check for Samples: [CD4021B-Q1](#)

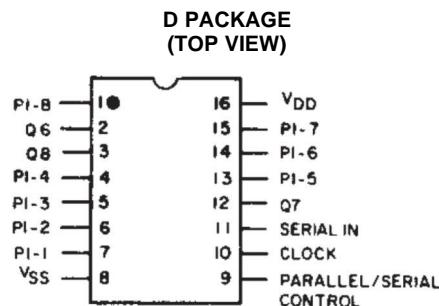
FEATURES

- Qualified for Automotive Applications
- Medium-Speed Operation: 12-MHz (Typ) Clock Rate at $V_{DD} - V_{SS} = 10$ V
- Fully Static Operation
- Eight Master-Slave Flip-Flops Plus Output Buffering and Control Gating
- 100% Tested for Quiescent Current at 20 V
- Maximum Input Current of 1 μ A at 18 V Over Full Package-Temperature Range: 100 nA at 18 V and 25°C
- Noise Margin (Full Package-Temperature Range):
 - 1 V at $V_{DD} = 5$ V
 - 2 V at $V_{DD} = 10$ V
 - 2.5 V at $V_{DD} = 15$ V
- Standardized Symmetrical Output Characteristics
- 5-V, 10-V, and 15-V Parametric Ratings

- Meets All Requirements of JEDEC Tentative Standard No. 13B, "Standard Specifications for Description of 'B' Series CMOS Devices"
- Latch-Up Performance Meets 50 mA per JESD 78, Class I

APPLICATIONS

- Parallel Input/Serial Output Data Queuing
- Parallel-to-Serial Data Conversion
- General-Purpose Register



DESCRIPTION

CD4021B series types are 8-stage parallel- or serial-input/serial output registers having common CLOCK and PARALLEL/SERIAL CONTROL inputs, a single SERIAL data input, and individual parallel "JAM" inputs to each register stage. Each register stage is a D-type, master-slave flip-flop. In addition to an output from stage 8, "Q" outputs are also available from stages 6 and 7. Parallel as well as serial entry is made into the register synchronously with the positive clock line transition in the CD4014B. In the CD4021B serial entry is synchronous with the clock but parallel entry is asynchronous. In both types, entry is controlled by the PARALLEL/SERIAL CONTROL input. When the PARALLEL/SERIAL CONTROL input is low, data is serially shifted into the 8-stage register synchronously with the positive transition of the clock line. When the PARALLEL/SERIAL CONTROL input is high, data is jammed into the 8-stage register via the parallel input lines and synchronous with the positive transition of the clock line. In the CD4021B, the CLOCK input of the internal stage is "forced" when asynchronous parallel entry is made. Register expansion using multiple packages is permitted.

The CD4021B series types are supplied in 16-lead hermetic dual-in-line ceramic packages (D and F suffixes), 16-lead dual-in-line plastic packages (E suffix), and in chip form (H suffix).

ORDERING INFORMATION⁽¹⁾

T _A	PACKAGE ⁽²⁾	ORDERABLE PART NUMBER	TOP-SIDE MARKING
-40°C to 125°C	SOIC – D	Reel of 2500	CD4010BQDRQ1

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.

(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.



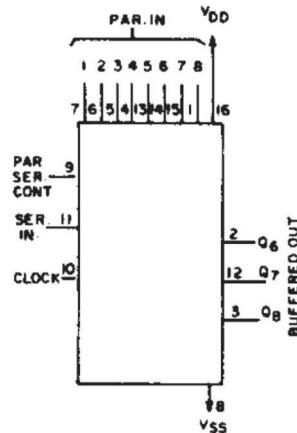
Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.



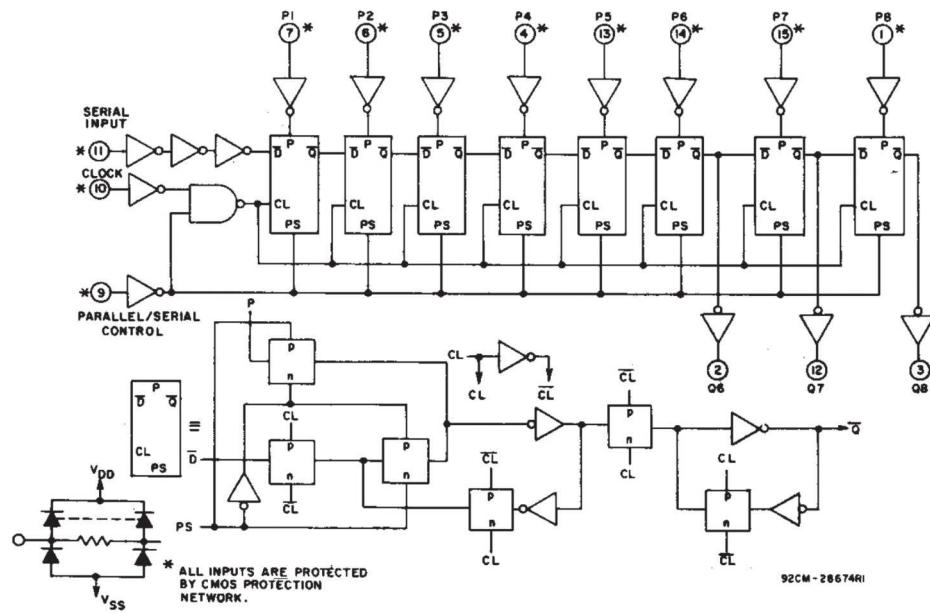
This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

Functional Diagram



Logic Diagram



TRUTH TABLE – CD4021B

CL	Serial Input	Parallel/Serial Control	PI-1	PI-n	Q1 (Internal)	Qn
X	X	1	0	0	0	0
X	X	1	0	1	0	1
X	X	1	1	0	1	0
X	X	1	1	1	1	1
/	0	0	X	X	0	Qn1
/	1	0	X	X	1	Qn1
\	X	0	X	X	Q1	Qn

X = DON'T CARE CASE

ABSOLUTE MAXIMUM RATINGS⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		VALUE	UNIT
V _{DD}	DC supply voltage range (voltage referenced to V _{SS} terminal)	–0.5 to +20	V
	Input voltage range, all inputs	–0.5 to V _{DD} +0.5	V
	DC input current, any one input	±10	mA
P _D	T _A = –40°C to +100°C	500	mW
	T _A = +100°C to +125°C	Derate Linearity at 12mW/°C to 20 mW	
P _D	Device dissipation per output transistor	100	mW
T _A	Operating temperature range	–40 to +125	°C
T _{stg}	Storage temperature range	–65 to +150	°C
ESD	Human-body model (HBM)	2000	V
	Machine model (MM)	200	
	Charged-Device Model (CDM)	1000	
Latch-up performance per JESD 78, Class I		50	mA

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) Tested in accordance with AEC-Q100.

RECOMMENDED OPERATING CONDITIONS

At $T_A = 25^\circ\text{C}$, unless otherwise specified. For maximum reliability, nominal operating conditions should be selected so that operation is always within the following ranges.

		V_{DD}	MIN	MAX	UNIT
	Supply voltage range (T_A = full package-temperature range)		3	18	V
t_W	Clock pulse width	5	180		ns
		10	80		
		15	50		
f_{CL}	Clock frequency	5		3	MHz
		10		6	
		15		8.5	
t_{rCL}, t_{fCL}	Clock rise and fall time	5		15	μs
		10		15	
		15		15	
t_s	Set-up time	Serial input (referred to CL)	5	120	ns
			10	80	
			15	60	
	Parallel inputs CD4014B (referred to CL)	Parallel inputs CD4014B (referred to CL)	5	80	ns
			10	50	
			15	40	
	Parallel inputs CD4021B (referred to P/S)	Parallel inputs CD4021B (referred to P/S)	5	50	ns
			10	30	
			15	20	
	Parallel/Serial Control CD4014B (referred to CL)	Parallel/Serial Control CD4014B (referred to CL)	5	180	ns
			10	80	
			15	60	
t_W	Parallel/serial pulse width		5	160	ns
			10	80	
			15	50	
t_{REM}	Parallel/serial removal time		5	280	ns
			10	140	
			15	100	

STATIC ELECTRICAL CHARACTERISTICS

PARAMETER		TEST CONDITIONS			LIMITS AT INDICATED TEMPERATURES (°C)					UNIT			
		V _D (V)	V _{IN} (V)	V _{DD} (V)	-40	+85	+125	+25					
I _{DD} Max	Quiescent device current		0.5	5	10	300	300	0.04			μA		
			0.10	10	20	600	600	0.04					
			0.15	15	100	3000	3000	0.04					
			0.20	20	0.61	0.42	0.36	0.08					
I _{OL} Min	Output low (sink) current	0.4	0.5	5	1.5	1.1	0.9	0.51	1		mA		
		0.5	0.10	10	4	2.8	2.4	1.3	2.6				
		1.5	0.15	15	-0.61	-0.42	-0.36	3.4	6.8				
I _{OH} Min	Output high (source) current	4.6	0.5	5	-1.8	-1.3	-1.15	-0.51	-1		mA		
		2.5	0.5	5	-1.5	-1.1	-0.9	-1.6	-3.2				
		9.5	0.10	10	-4	-2.8	-2.4	-1.3	-2.6				
		13.5	0.15	15	-4.2			-3.4	-6.8				
V _{OL} Max	Output voltage: low level		0.5	5	0.05			0	0.05		V		
			0.10	10	0.05			0	0.05				
			0.15	15	0.05			0	0.05				
V _{OH} Min	Output voltage: high level		0.5	5	4.95			4.95	5		V		
			0.10	10	9.95			9.95	10				
			0.15	15	14.95			14.95	15				
V _{IL} Max	Input low voltage	0.5, 4.5		5	1.5				1.5		V		
		1, 9		10	3				3				
		1.5, 13.5		15	4				4				
V _{IH} Min	Input high voltage	0.5, 4.5		5	3.5			3.5			V		
		1, 9		10	7			7					
		1.5, 13.5		15	11			11					
I _{IN} Max	Input current		0, 18	18	±0.1	±1	±1		±10 ⁻⁵	±0.1	μA		

DYNAMIC ELECTRICAL CHARACTERISTICS

T_A = 25°C, Input t_r/t_f = 20 ns, C_L = 50 pF, R_L 200 kΩ

PARAMETER	TEST CONDITIONS	V _{DD}	MIN	TYP	MAX	UNIT
t _{PLH} , t _{PHL} Propagation delay time		5	160	320		ns
		10	80	160		
		15	30	120		
t _{THL} , t _{TLH} Transition time		5	100	200		ns
		10	50	100		
		15	40	80		
f _{CL} Maximum clock input ⁽¹⁾		5	3	6		MHz
		10	6	12		
		15	8.5	17		
t _W Minimum clock pulse width ⁽¹⁾		5	90	180		ns
		10	40	80		
		15	25	50		
t _{rCL} , t _{fCL} Clock rise and fall time ⁽²⁾⁽¹⁾		5		15		μs
		10		15		
		15		15		
t _s Minimum setup time ⁽¹⁾	Serial input (referred to CL)	5	60	120		ns
		10	40	80		
		15	30	60		
	Parallel inputs (referred to CL)	5	40	80		
		10	25	50		
		15	20	40		
	Parallel inputs (referred to P/S)	5	25	50		
		10	15	30		
		15	10	20		
	Serial in, Parallel in, Parallel/Serial Control	5	90	180		
		10	40	80		
		15	30	60		
t _H Minimum hold time ⁽¹⁾		5		0		ns
		10		0		
		15		0		
t _{WH} Minimum P/S pulse width ⁽¹⁾		5	80	160		ns
		10	40	80		
		15	25	50		
t _{REM} Minimum P/S removal time ⁽¹⁾		5	140	280		ns
		10	70	140		
		15	50	100		
C _I Average input capacitance ⁽¹⁾			5	7.5	pF	

(1) Not production tested

(2) If more than one unit is cascaded, t_{rCL} should be made less than or equal to the sum of the transition time and the fixed propagation delay of the output of the driving stage for the estimated capacitive load.

Typical Characteristics

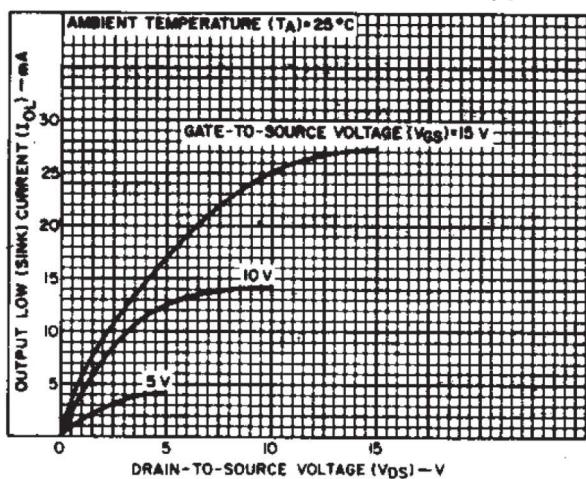


Figure 1. Typical Output Low (Sink) Current Characteristics

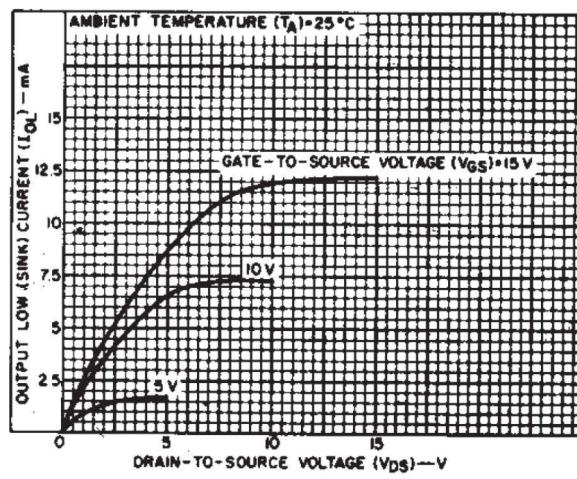


Figure 2. Minimum Output Low (Sink) Current Characteristics

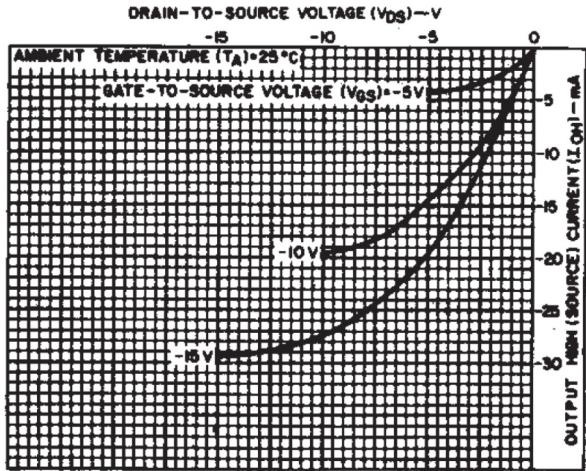


Figure 3. Typical Output High (Source) Current Characteristics

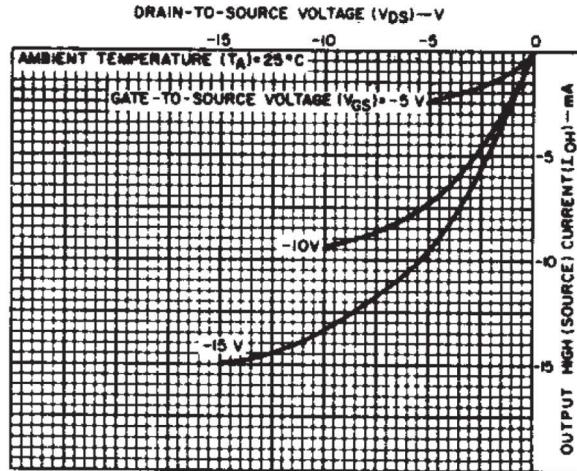


Figure 4. Minimum Output High (Source) Current Characteristics

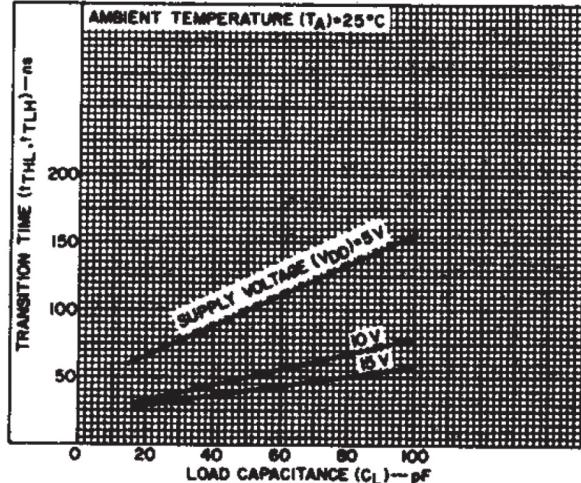


Figure 5. Typical Transition Time as a Function of Load Capacitance

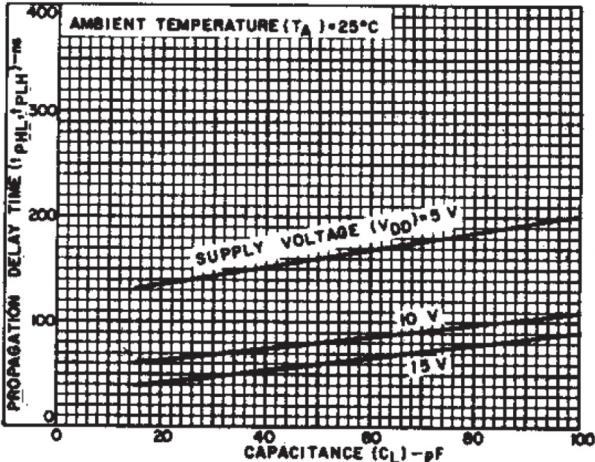


Figure 6. Typical Propagation Delay Times as a Function of Load Capacitance

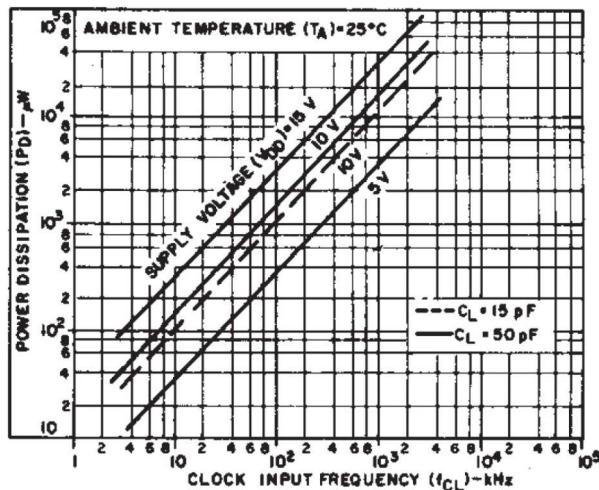
Typical Characteristics (continued)

Figure 7. Typical Dynamic Power Dissipation as a Function of Clock Input Frequency

PARAMETER MEASUREMENT INFORMATION

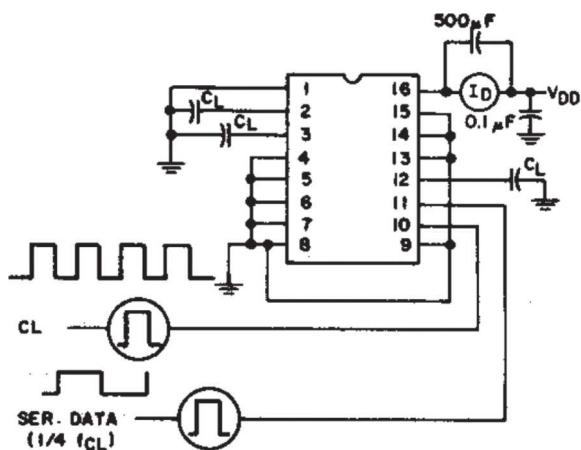


Figure 8. Dynamic Power Dissipation Test Circuit

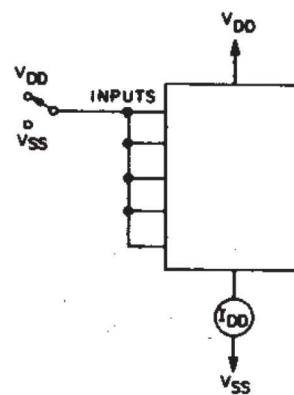


Figure 9. Quiescent Device Current Test Circuit

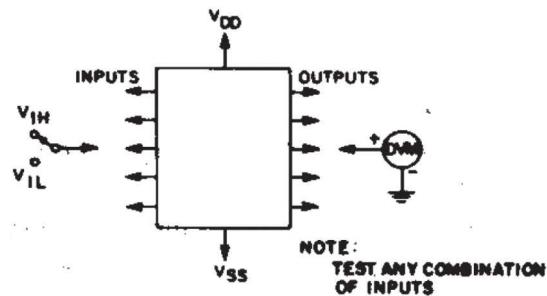


Figure 10. Input Voltage Test Circuit

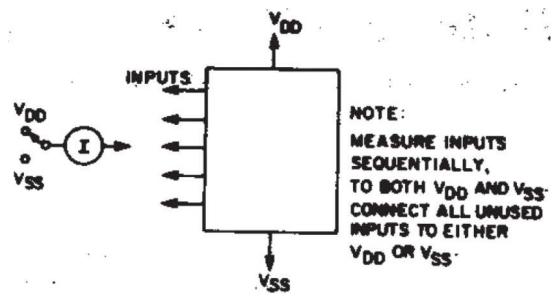
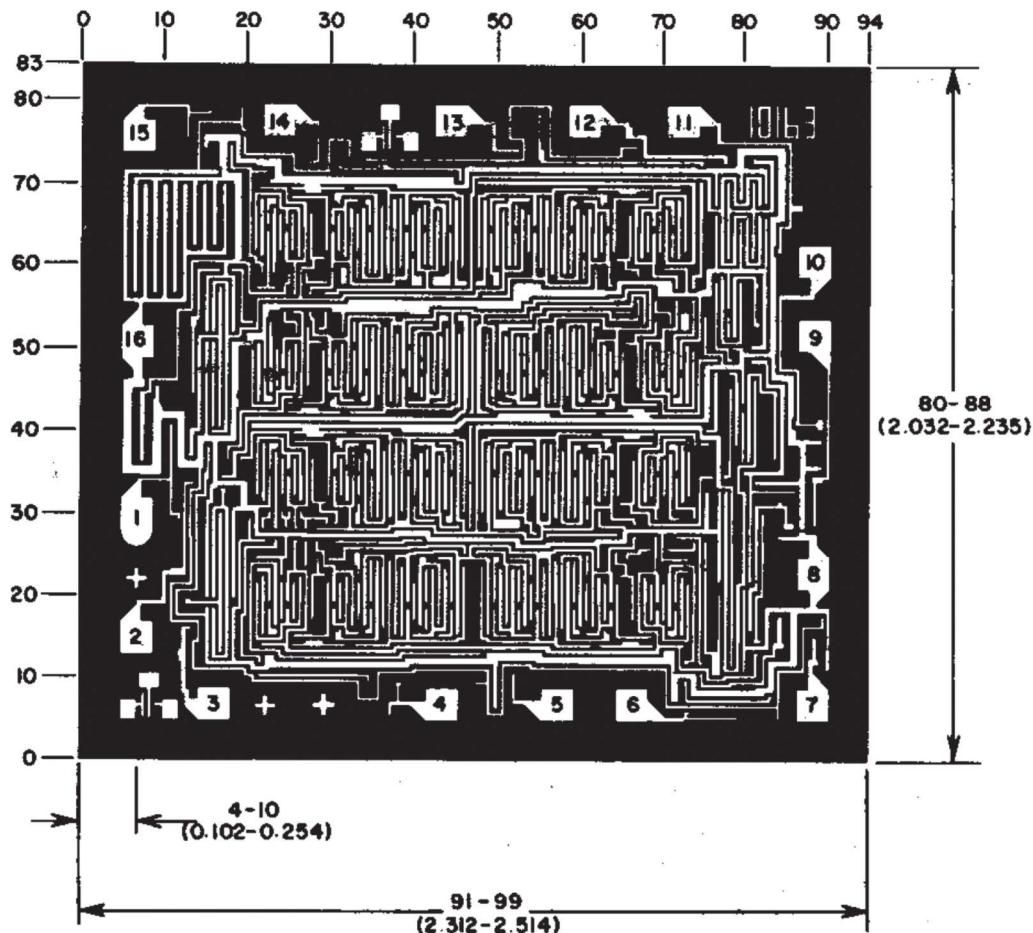


Figure 11. Input Current Test Circuit



Note: Dimensions in parentheses are in millimeters and are derived from the basic inch dimensions as indicated. Grid graduation are in mils (10^{-3} inch).

Figure 12. Dimensions and Pad Layout



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PACKAGE OPTION ADDENDUM

10-Dec-2020

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CD4021BQDRQ1	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CD4021BQ	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE OPTION ADDENDUM

10-Dec-2020

- Catalog: [CD4021B](#)

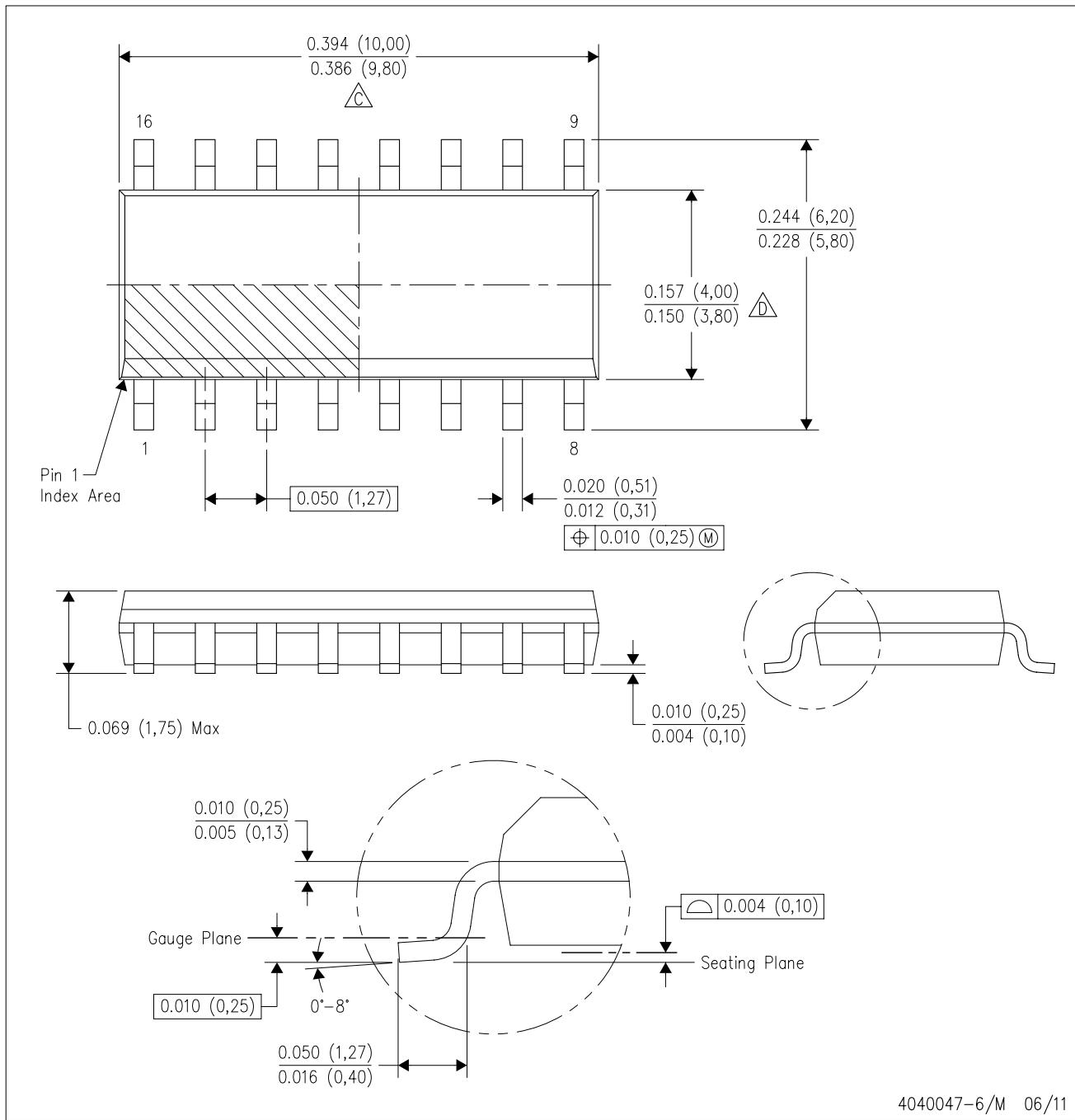
- Military: [CD4021B-MIL](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

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SN74HCS86 Quadruple 2-Input XOR Gates with Schmitt-Trigger Inputs

1 Features

- Wide operating voltage range: 2 V to 6 V
- Schmitt-trigger inputs allow for slow or noisy input signals
- Low power consumption
 - Typical I_{CC} of 100 nA
 - Typical input leakage current of ± 100 nA
- ± 7.8 -mA output drive at 6 V
- Extended ambient temperature range: -40°C to $+125^{\circ}\text{C}$, T_A

2 Applications

- Detect phase differences in input signals
- Create a selectable inverter / buffer

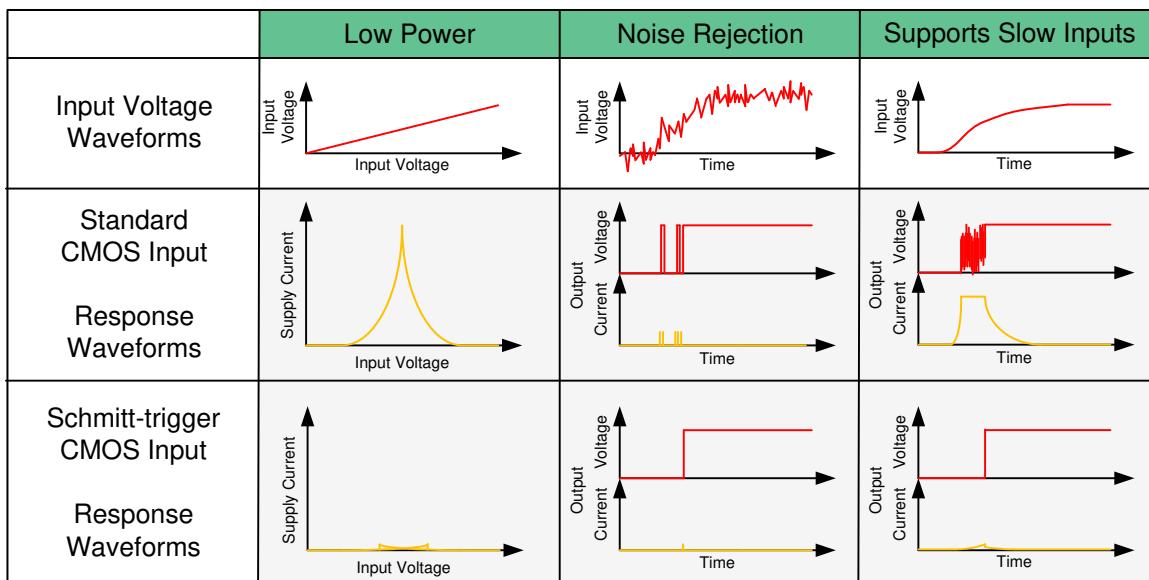
3 Description

This device contains four independent 2-input XOR Gates with Schmitt-trigger inputs. Each gate performs the Boolean function $Y = A \oplus B$ in positive logic.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
SN74HCS86PW	TSSOP (14)	5.00 mm \times 4.40 mm
SN74HCS86D	SOIC (14)	8.70 mm \times 3.90 mm
SN74HCS86BQA	WQFN (14)	3.00 mm \times 2.50 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Benefits of Schmitt-trigger inputs



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Table of Contents

1 Features.....	1	8.3 Feature Description.....	8
2 Applications.....	1	8.4 Device Functional Modes.....	9
3 Description.....	1	9 Application and Implementation.....	10
4 Revision History.....	2	9.1 Application Information.....	10
5 Pin Configuration and Functions.....	3	9.2 Typical Application.....	10
Pin Functions.....	3	10 Power Supply Recommendations.....	13
6 Specifications.....	4	11 Layout.....	13
6.1 Absolute Maximum Ratings	4	11.1 Layout Guidelines.....	13
6.2 ESD Ratings	4	11.2 Layout Example.....	13
6.3 Recommended Operating Conditions	4	12 Device and Documentation Support.....	14
6.4 Thermal Information	5	12.1 Documentation Support.....	14
6.5 Electrical Characteristics	5	12.2 Receiving Notification of Documentation Updates..	14
6.6 Switching Characteristics	6	12.3 Support Resources.....	14
6.7 Typical Characteristics.....	6	12.4 Trademarks.....	14
7 Parameter Measurement Information.....	7	12.5 Electrostatic Discharge Caution.....	14
8 Detailed Description.....	8	12.6 Glossary.....	14
8.1 Overview.....	8	13 Mechanical, Packaging, and Orderable	
8.2 Functional Block Diagram.....	8	Information.....	15

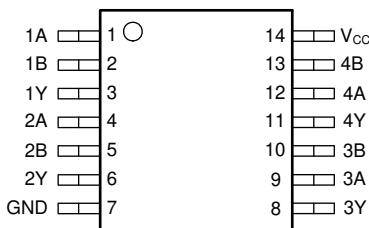
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

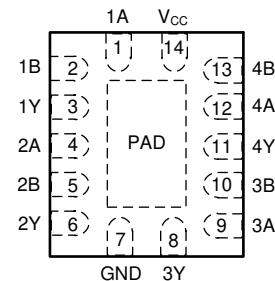
Changes from Revision A (May 2020) to Revision B (January 2021)	Page
• Updated the numbering format for tables, figures, and cross-references throughout the document.....	1
• Added BQA package information to the <i>Device Information</i> table.....	1
• Added BQA package information to <i>Pin Configuration and Functions</i>	3
• Added BQA package information to <i>Thermal Information</i> table.....	5

Changes from Revision * (January 2020) to Revision A (May 2020)	Page
• Added D package to <i>Device Information</i> table.....	1
• Added D package information to <i>Pin Configuration and Functions</i>	3
• Added D package column to <i>Thermal Information</i> table.....	5

5 Pin Configuration and Functions



**Figure 5-1. D or PW Package
14-Pin SOIC or TSSOP
Top View**



**Figure 5-2. BQA Package
14-Pin WQFN
Top View**

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
1A	1	Input	Channel 1, Input A
1B	2	Input	Channel 1, Input B
1Y	3	Output	Channel 1, Output Y
2A	4	Input	Channel 2, Input A
2B	5	Input	Channel 2, Input B
2Y	6	Output	Channel 2, Output Y
GND	7	—	Ground
3Y	8	Output	Channel 3, Output Y
3A	9	Input	Channel 3, Input A
3B	10	Input	Channel 3, Input B
4Y	11	Output	Channel 4, Output Y
4A	12	Input	Channel 4, Input A
4B	13	Input	Channel 4, Input B
V _{CC}	14	—	Positive Supply
Thermal Pad ⁽¹⁾		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply

1. BQA Package only.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		-0.5	7	V
I _{IK}	Input clamp current ⁽²⁾	V _I < -0.5 V or V _I > V _{CC} + 0.5 V		±20	mA
I _{OK}	Output clamp current ⁽²⁾	V _I < -0.5 V or V _I > V _{CC} + 0.5 V		±20	mA
I _O	Continuous output current	V _O = 0 to V _{CC}		±35	mA
	Continuous current through V _{CC} or GND			±70	mA
T _J	Junction temperature ⁽³⁾			150	°C
T _{stg}	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) Guaranteed by design.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ⁽¹⁾ HBM ESD Classification Level 2	±4000	V
		Charged device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	±1500	

(1) AEC Q100-002 indicate that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	2	5	6	V
V _I	Input voltage	0		V _{CC}	V
V _O	Output voltage	0		V _{CC}	V
Δt/Δv	Input transition rise and fall rate			Unlimited	ns/V
T _A	Ambient temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74HCS86			UNIT
		PW (TSSOP)	D (SOIC)	BQA (WQFN)	
		14 PINS	14 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	151.7	133.6	109.7	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	79.4	89.0	111.0	°C/W
R _{θJB}	Junction-to-board thermal resistance	94.7	89.5	77.9	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	25.2	45.5	20.2	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	94.1	89.1	77.8	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	56.6	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

6.5 Electrical Characteristics

over operating free-air temperature range; typical ratings measured at T_A = 25°C (unless otherwise noted).

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
V _{T+}	Positive switching threshold		2 V	0.7	1.5	V
			4.5 V	1.7	3.15	
			6 V	2.1	4.2	
V _{T-}	Negative switching threshold		2 V	0.3	1.0	V
			4.5 V	0.9	2.2	
			6 V	1.2	3.0	
ΔV _T	Hysteresis (V _{T+} - V _{T-})		2 V	0.2	1.0	V
			4.5 V	0.4	1.4	
			6 V	0.6	1.6	
V _{OH}	High-level output voltage	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	2 V to 6 V	V _{CC} – 0.1 V _{CC} – 0.002	V
			I _{OH} = -6 mA	4.5 V	4.0 4.3	
			I _{OH} = -7.8 mA	6 V	5.4 5.75	
V _{OL}	Low-level output voltage	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	2 V to 6 V	0.002 0.1	V
			I _{OL} = 6 mA	4.5 V	0.18 0.30	
			I _{OL} = 7.8 mA	6 V	0.22 0.33	
I _I	Input leakage current	V _I = V _{CC} or 0	6 V		±100 ±1000	nA
I _{CC}	Supply current	V _I = V _{CC} or 0, I _O = 0	6 V		0.1 2	μA
C _i	Input capacitance		2 V to 6 V		5	pF
C _{pd}	Power dissipation capacitance per gate	No load	2 V to 6 V		10	pF

6.6 Switching Characteristics

$C_L = 50 \text{ pF}$; over operating free-air temperature range; typical ratings measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted). See [Parameter Measurement Information](#).

PARAMETER		FROM (INPUT)	TO (OUTPUT)	V_{CC}	MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay	A or B	Y	2 V		15	36	ns
				4.5 V		7	13	
				6 V		6	12	
t_t	Transition-time		Y	2 V		9	16	ns
				4.5 V		5	9	
				6 V		4	8	

6.7 Typical Characteristics

$T_A = 25^\circ\text{C}$

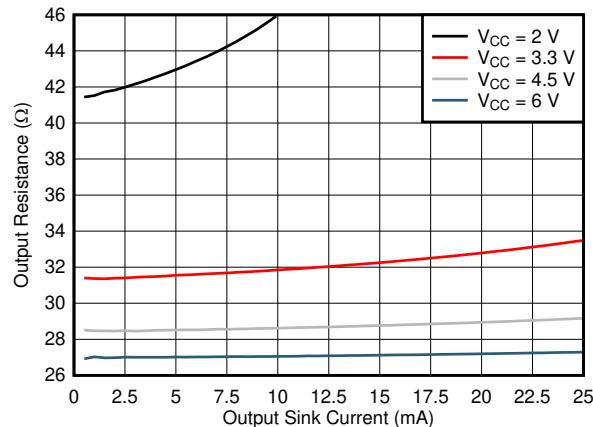


Figure 6-1. Output driver resistance in LOW state.

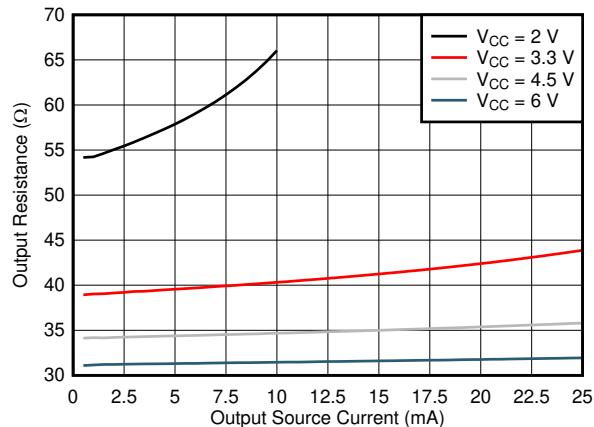


Figure 6-2. Output driver resistance in HIGH state.

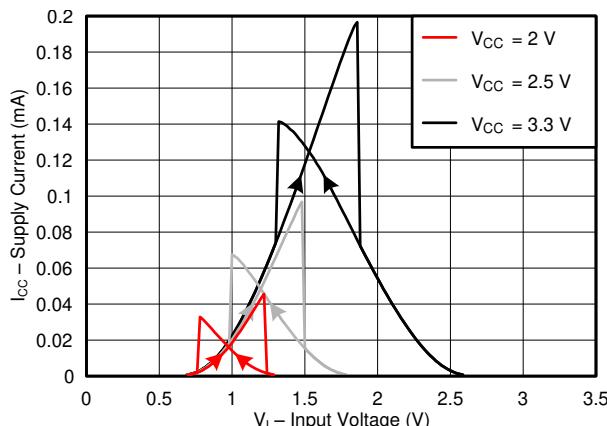


Figure 6-3. Supply current across input voltage, 2-, 2.5-, and 3.3-V supply

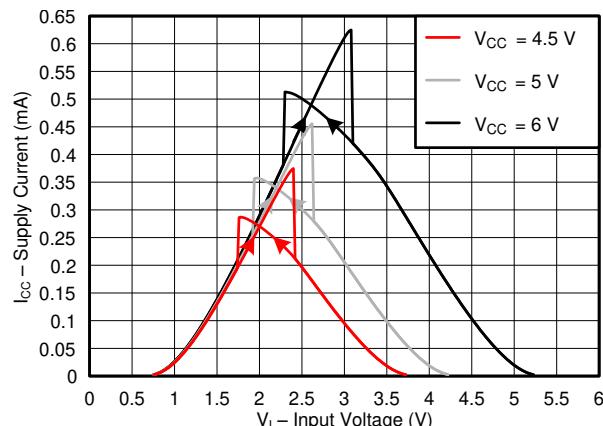


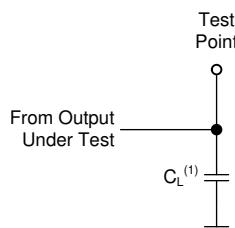
Figure 6-4. Supply current across input voltage, 4.5-, 5-, and 6-V supply

7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_t < 2.5$ ns.

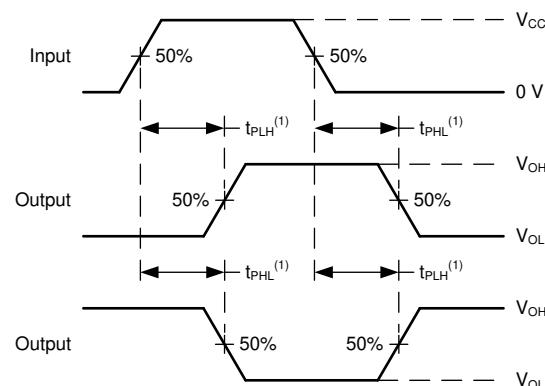
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



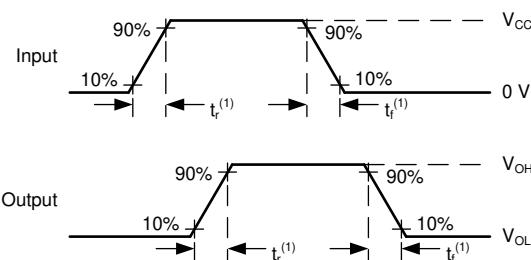
(1) C_L includes probe and test-fixture capacitance.

Figure 7-1. Load Circuit for Push-Pull Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

Figure 7-2. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t .

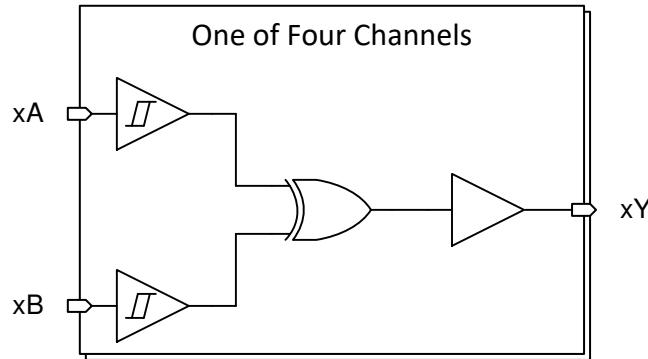
Figure 7-3. Voltage Waveforms, Input and Output Transition Times

8 Detailed Description

8.1 Overview

This device contains four independent 2-input XOR Gates with Schmitt-trigger inputs. Each gate performs the Boolean function $Y = A \oplus B$ in positive logic.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term "balanced" indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

8.3.2 CMOS Schmitt-Trigger Inputs

This device includes inputs with the Schmitt-trigger architecture. These inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics* table from the input to ground. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* table, and the maximum input leakage current, given in the *Electrical Characteristics* table, using Ohm's law ($R = V / I$).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the inputs with slow transitioning signals will increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see [Understanding Schmitt Triggers](#).

8.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in [Electrical Placement of Clamping Diodes for Each Input and Output](#).

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

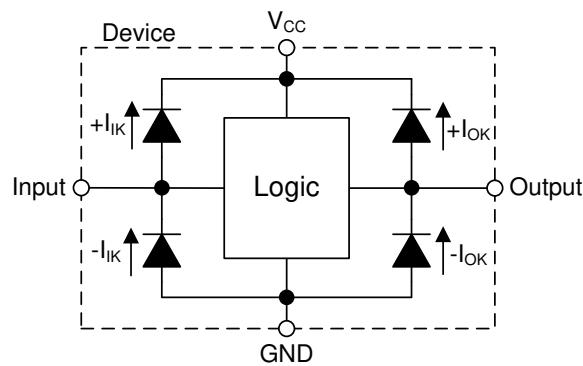


Figure 8-1. Electrical Placement of Clamping Diodes for Each Input and Output

8.4 Device Functional Modes

[Function Table](#) lists the functional modes of the SN74HCS86.

Table 8-1. Function Table

INPUTS ⁽¹⁾		OUTPUT Y
A	B	
L	L	L
L	H	H
H	L	H
H	H	L

(1) H = High Voltage Level, L = Low Voltage Level

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

In this application, a 2-input XOR gate is used as a phase difference detector as shown in [Typical application block diagram](#). The remaining three gates can be used for other applications in the system, or the inputs can be grounded and the channels left unused.

The SN74HCS86 is used to identify phase difference between a reference clock and another input clock. Whenever the clock states are different, the XOR output will pulse HIGH until the clocks return to the same state. The output is fed into a low-pass filter to obtain a DC representation of the phase difference.

Typically, clock signals have fast transition rates, but additional filtering can be added to the clock signals which can lead to slower transitions rates. This makes the SN74HCS86 ideal for the application because it has Schmitt-trigger inputs that do not have input transition rate requirements.

9.2 Typical Application

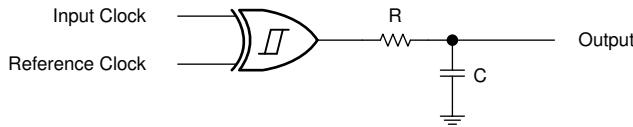


Figure 9-1. Typical application block diagram

9.2.1 Design Requirements

9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics*.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HCS86 plus the maximum static supply current, I_{CC} , listed in *Electrical Characteristics* and any transient current required for switching. The logic device can only source as much current as is provided by the positive supply source. Be sure not to exceed the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74HCS86 plus the maximum supply current, I_{CC} , listed in *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current as can be sunk into its ground connection. Be sure not to exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74HCS86 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed 50 pF.

The SN74HCS86 can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL} . When outputting in the high state, the output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and Cpd Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

9.2.1.2 Input Considerations

Input signals must cross $V_{t-(min)}$ to be considered a logic LOW, and $V_{t+(max)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74HCS86, as specified in the *Electrical Characteristics*, and the desired input transition rate. A 10-k Ω resistor value is often used due to these factors.

The SN74HCS86 has no input signal transition rate requirements because it has Schmitt-trigger inputs.

Another benefit to having Schmitt-trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_{T(min)}$ in the *Electrical Characteristics*. This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than V_{CC} or ground is plotted in the *Typical Characteristics*.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to *Feature Description* section for additional information regarding the outputs for this device.

9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74HCS86 to the receiving device(s).
3. Ensure the resistive load at the output is larger than $(V_{CC} / I_{O(max)}) \Omega$. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.

4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#).

9.2.3 Application Curves

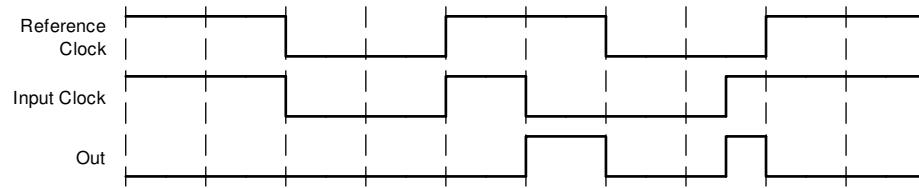


Figure 9-2. Application timing diagram

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in given example layout image.

11 Layout

11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

11.2 Layout Example

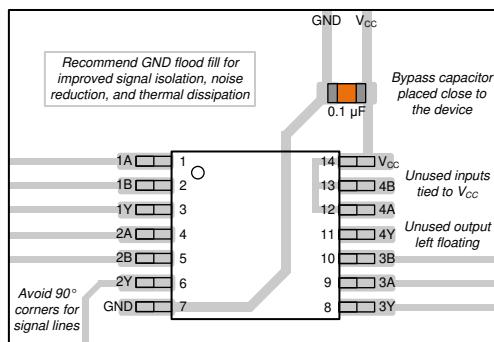


Figure 11-1. Example layout for the SN74HCS86

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *HCMOS Design Considerations* application report (SCLA007)
- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application report (SDYA009)
- Texas Instruments, *Designing With Logic* application report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

12.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

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12.5 Electrostatic Discharge Caution

 This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



www.ti.com

PACKAGE OPTION ADDENDUM

3-Feb-2021

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HCS86BQAR	ACTIVE	WQFN	BQA	14	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	HCS86	Samples
SN74HCS86DR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	HCS86	Samples
SN74HCS86PWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	HCS86	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.



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PACKAGE OPTION ADDENDUM

3-Feb-2021

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

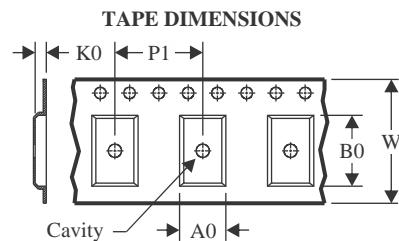
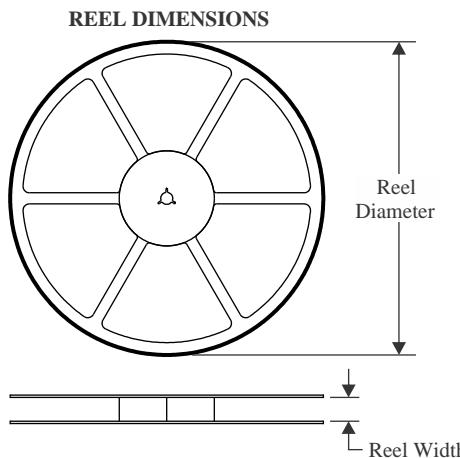
OTHER QUALIFIED VERSIONS OF SN74HCS86 :

- Automotive: [SN74HCS86-Q1](#)

NOTE: Qualified Version Definitions:

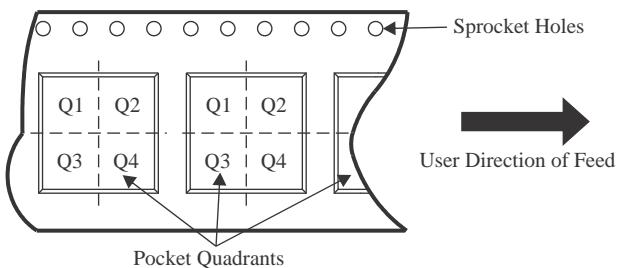
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



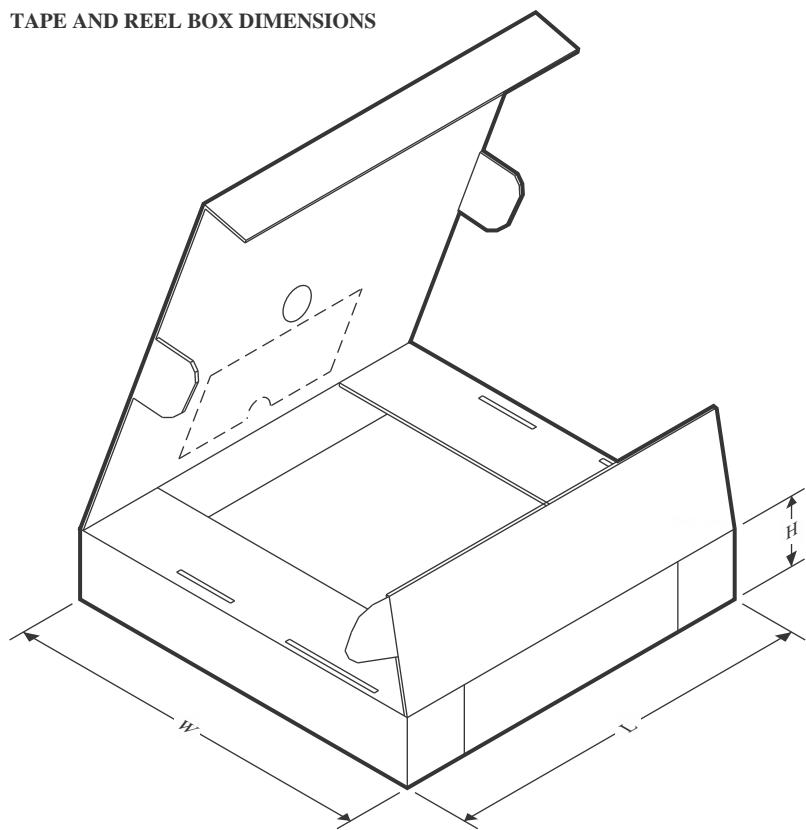
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCS86BQAR	WQFN	BQA	14	3000	180.0	12.4	2.8	3.3	1.1	4.0	12.0	Q1
SN74HCS86DR	SOIC	D	14	2500	330.0	16.4	6.6	9.3	2.1	8.0	16.0	Q1
SN74HCS86DR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74HCS86PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCS86PWR	TSSOP	PW	14	2000	330.0	12.4	6.85	5.45	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCS86BQAR	WQFN	BQA	14	3000	210.0	185.0	35.0
SN74HCS86DR	SOIC	D	14	2500	366.0	364.0	50.0
SN74HCS86DR	SOIC	D	14	2500	356.0	356.0	35.0
SN74HCS86PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74HCS86PWR	TSSOP	PW	14	2000	366.0	364.0	50.0

GENERIC PACKAGE VIEW

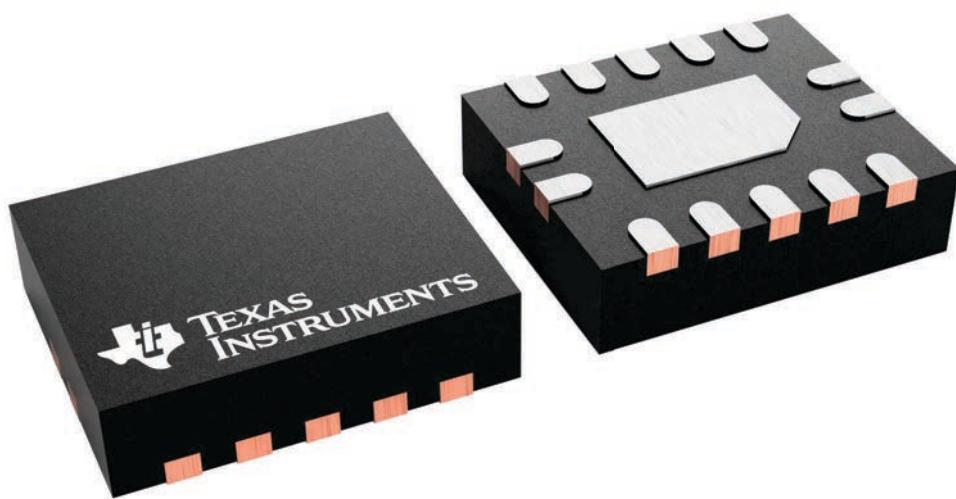
BQA 14

WQFN - 0.8 mm max height

2.5 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



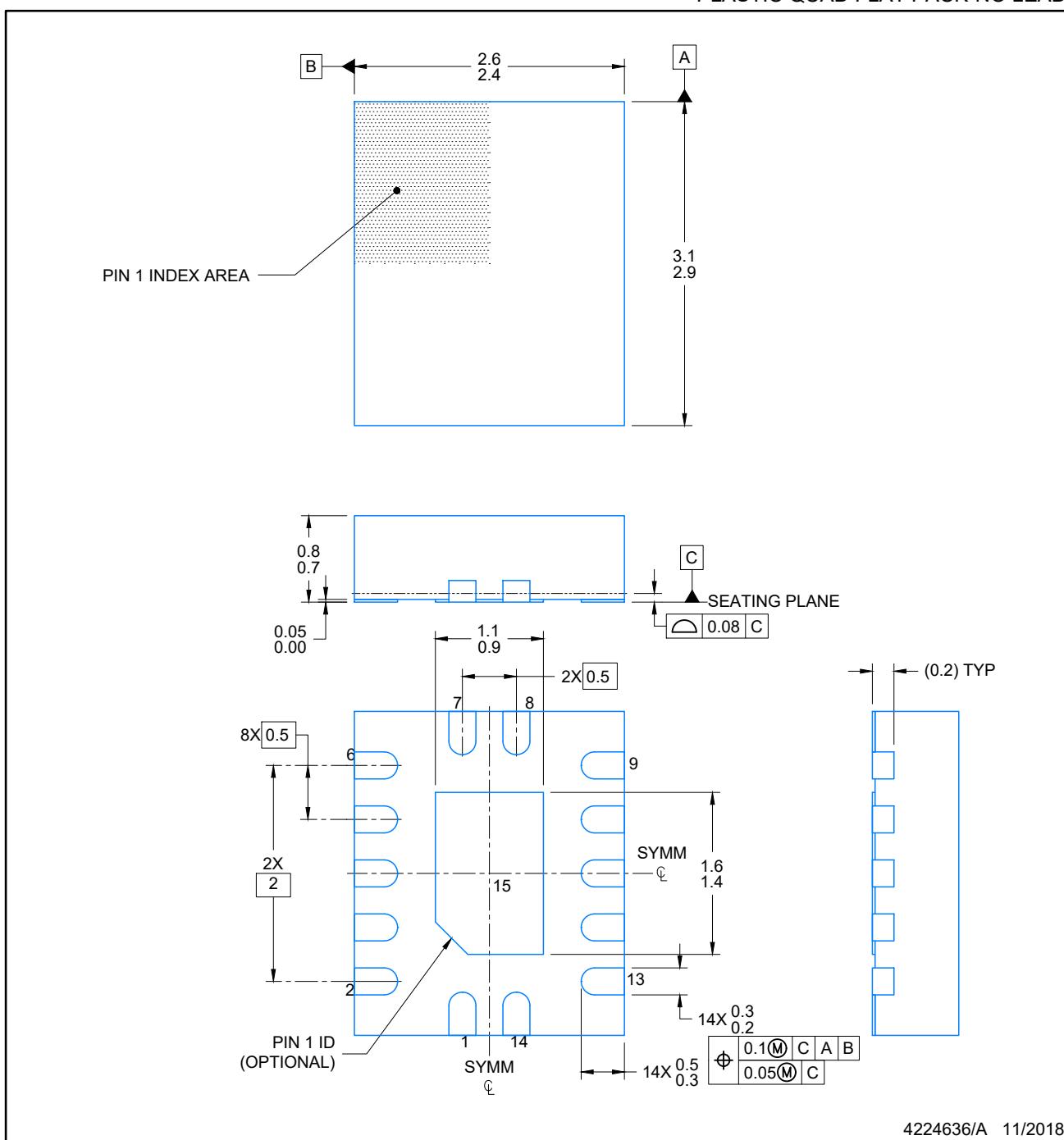
4227145/A

PACKAGE OUTLINE

WQFN - 0.8 mm max height

BQA0014A

PLASTIC QUAD FLAT PACK-NO LEAD



4224636/A 11/2018

NOTES:

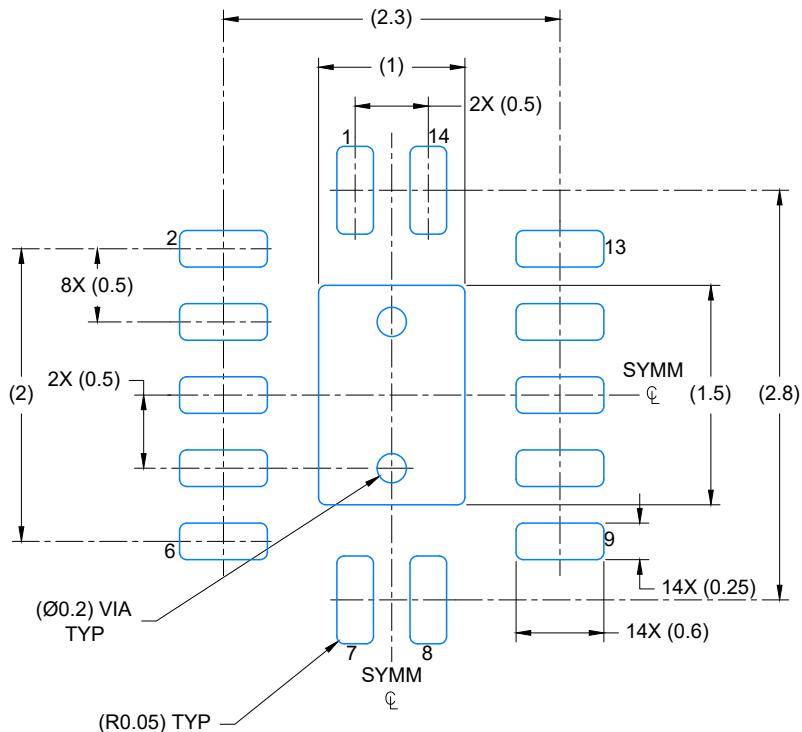
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

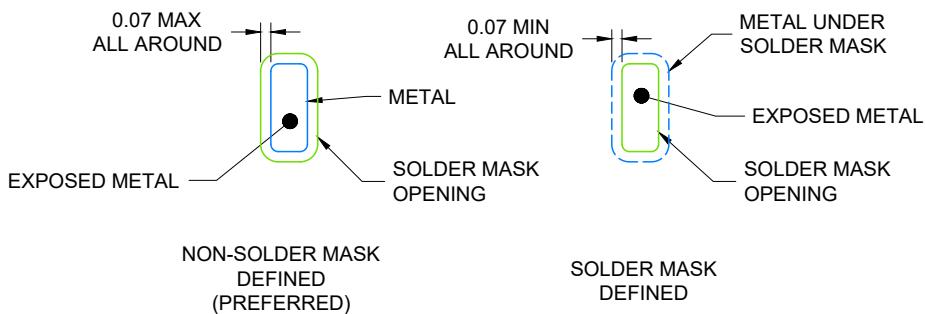
BQA0014A

WQFN - 0.8 mm max height

PLASTIC QUAD FLAT PACK-NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X



4224636/A 11/2018

NOTES: (continued)

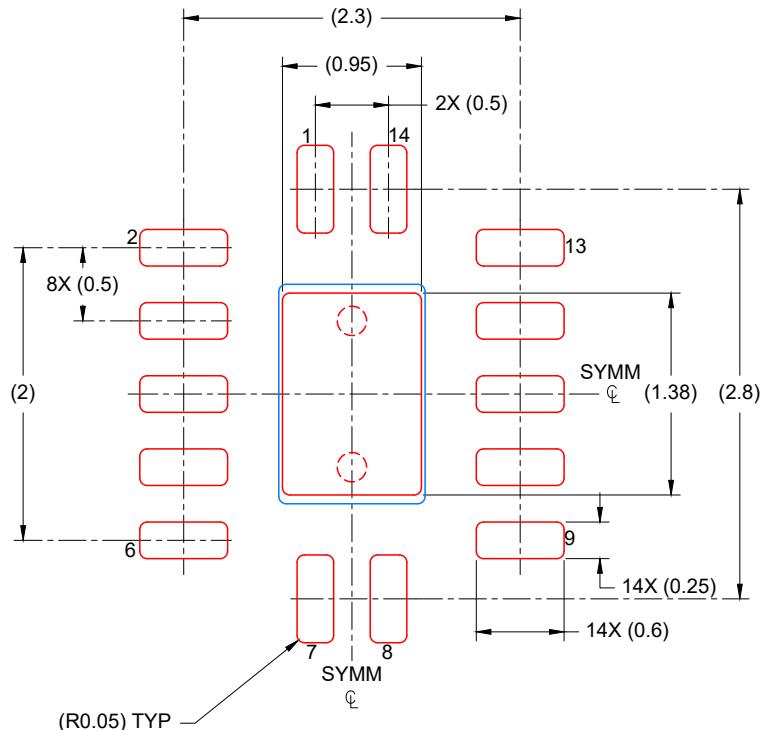
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

WQFN - 0.8 mm max height

BQA0014A

PLASTIC QUAD FLAT PACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
88% PRINTED COVERAGE BY AREA
SCALE: 20X

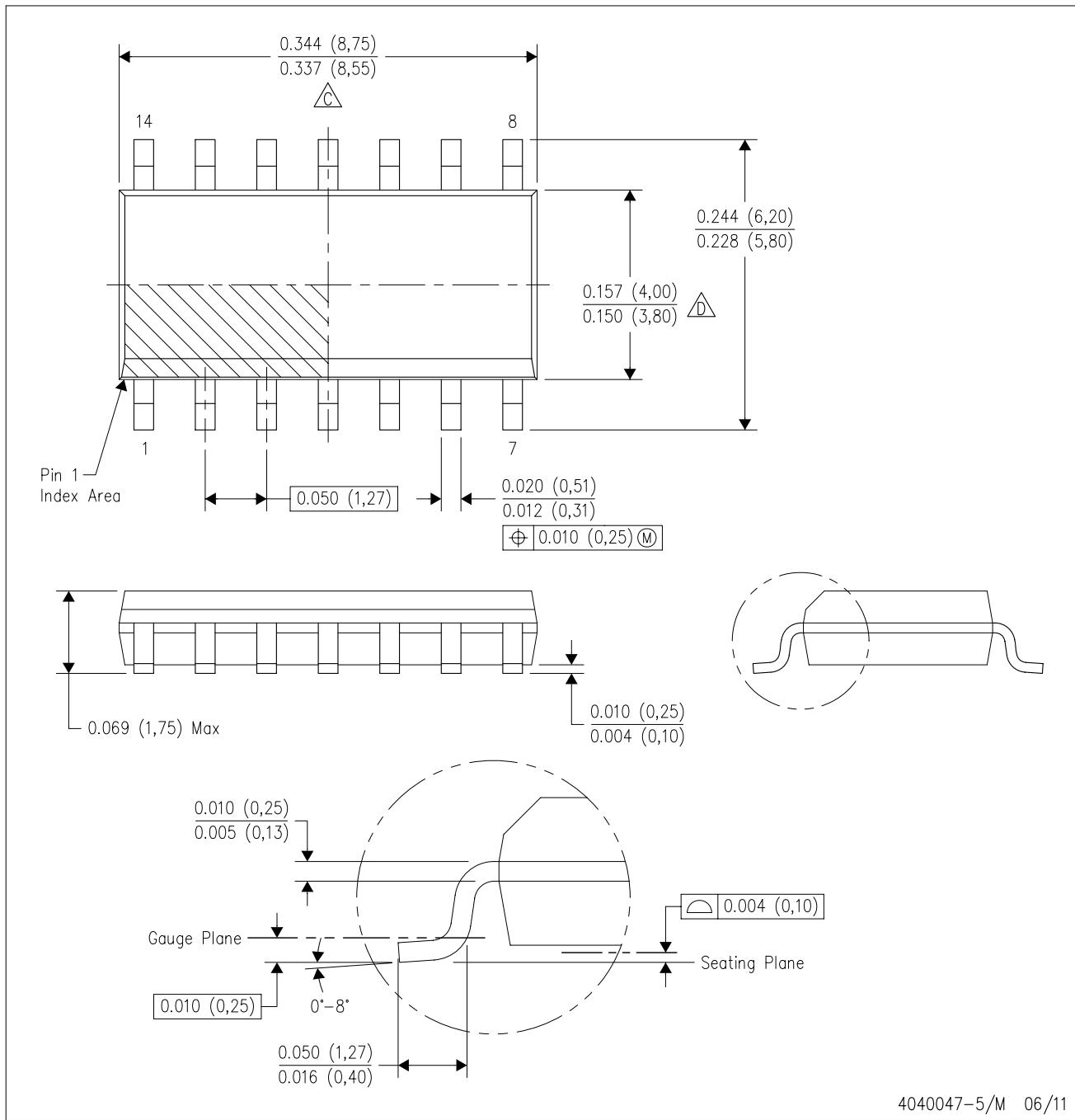
4224636/A 11/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

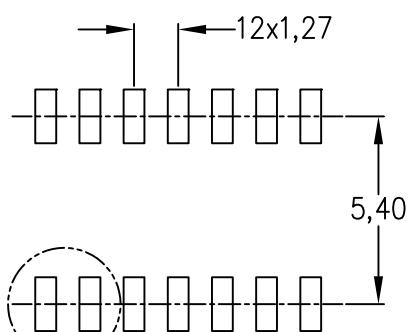
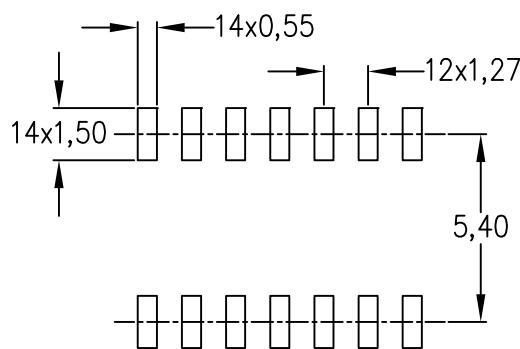
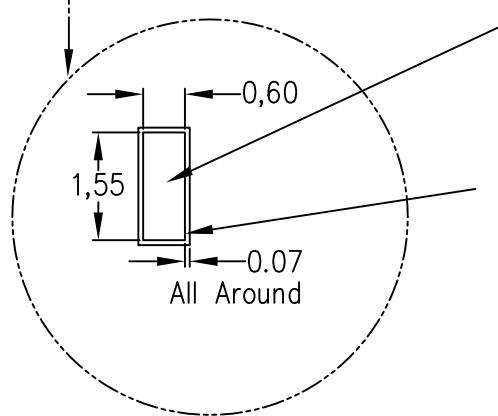
B. This drawing is subject to change without notice.

C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE

Example Board Layout
(Note C)Stencil Openings
(Note D)Example
Non Soldermask Defined PadExample
Pad Geometry
(See Note C)Example
Solder Mask Opening
(See Note E)

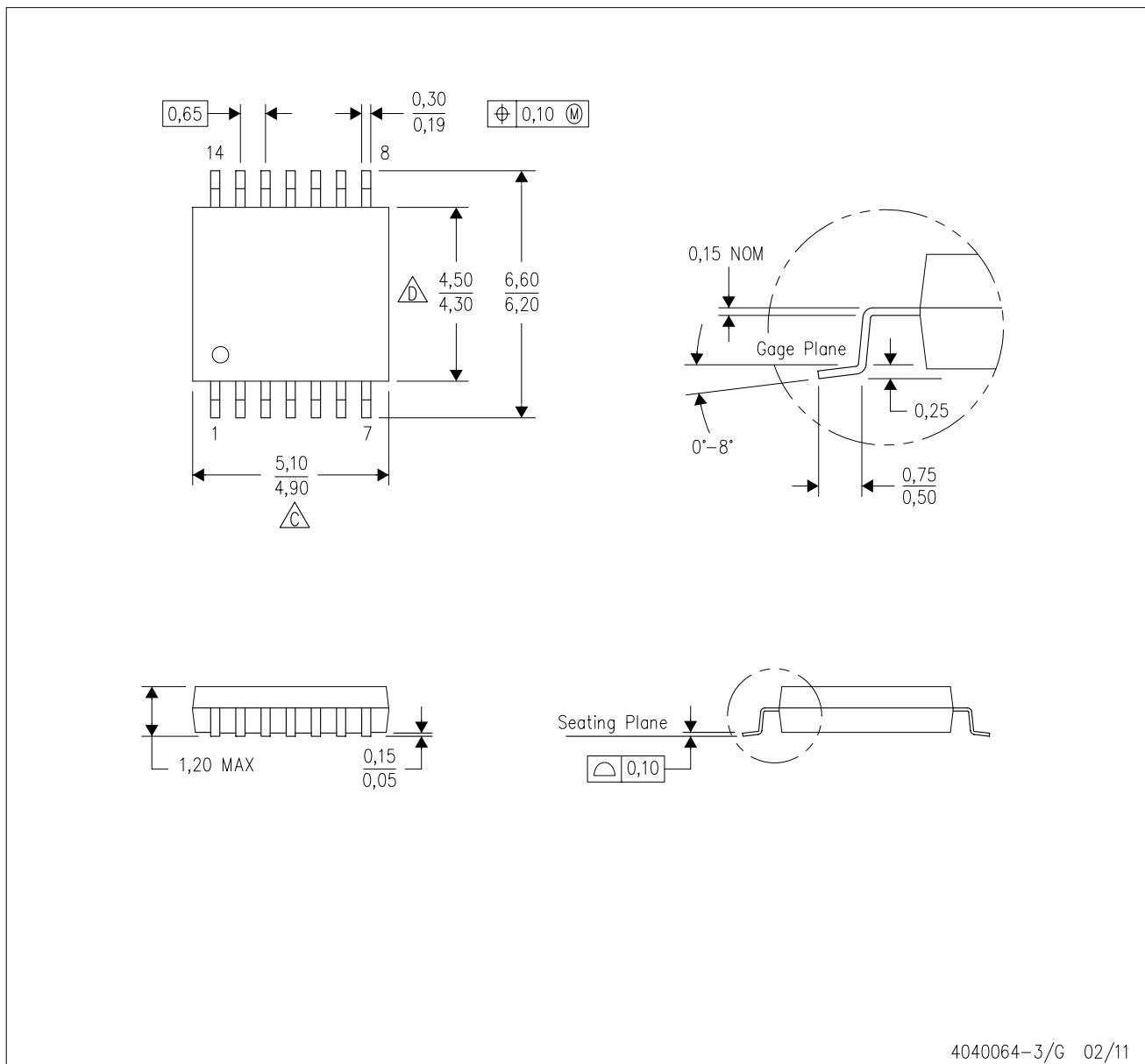
4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

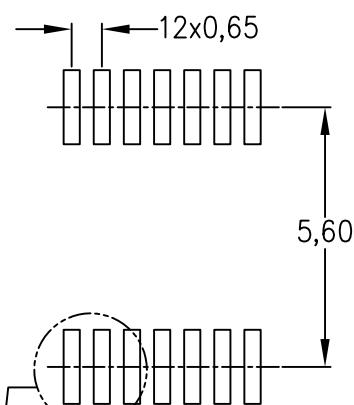
E. Falls within JEDEC MO-153

LAND PATTERN DATA

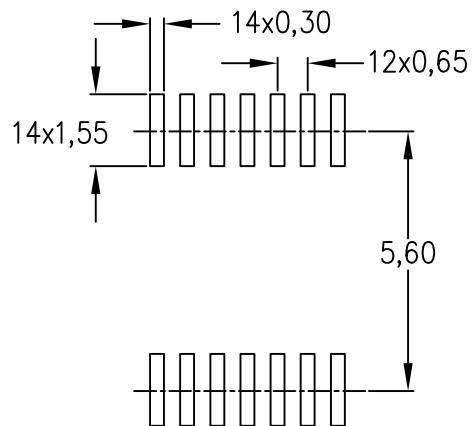
PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

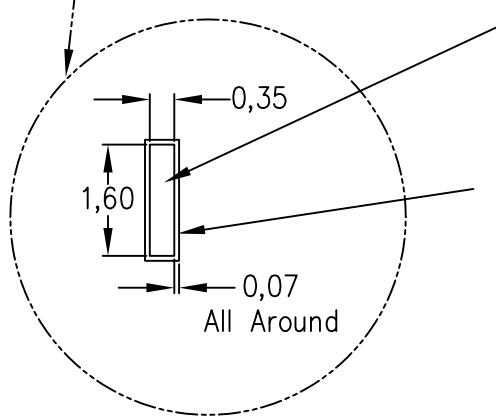
Example Board Layout
(Note C)



Stencil Openings
(Note D)



Example
Non Soldermask Defined Pad



Example
Pad Geometry
(See Note C)

Example
Solder Mask Opening
(See Note E)

4211284-2/G 08/15

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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SN74HCS157 Quadruple 2-to-1 Multiplexer with Schmitt-Trigger Inputs

1 Features

- Wide operating voltage range: 2 V to 6 V
- Schmitt-trigger inputs allow for slow or noisy input signals
- Low power consumption
 - Typical I_{CC} of 100 nA
 - Typical input leakage current of ± 100 nA
- ± 7.8 -mA output drive at 6 V
- Extended ambient temperature range: -40°C to $+125^{\circ}\text{C}$, T_A

2 Applications

- Data selection
- Multiplexing

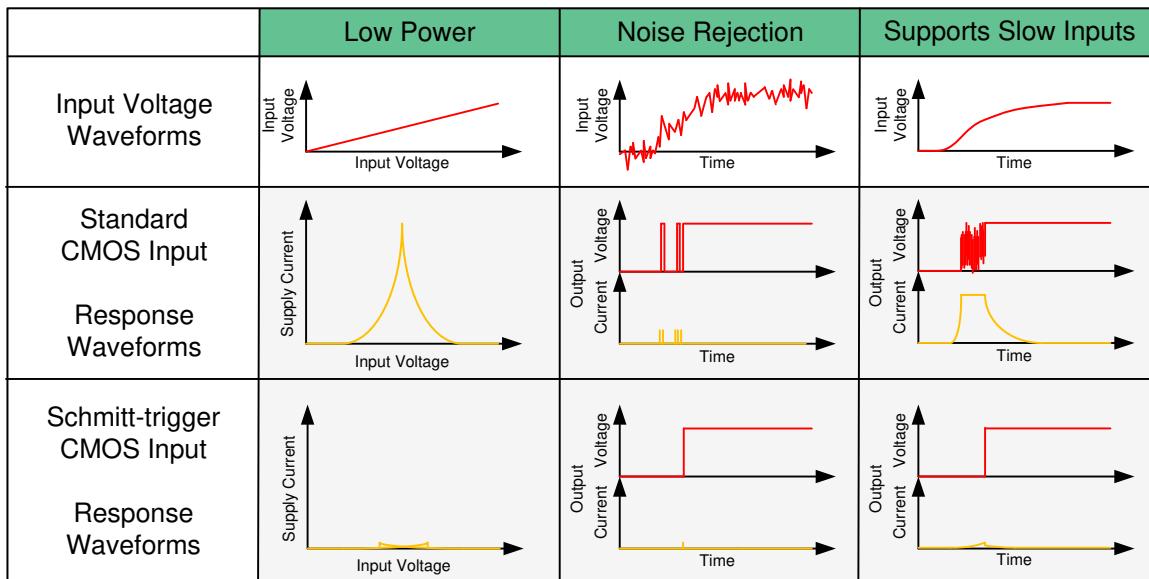
3 Description

The SN74HCS157 contains four data selectors/multiplexers to select one of two data sources. All channels are controlled by the same address select (\bar{A}/B) input, and strobe (\bar{G}) input. A high level at the strobe terminal forces all outputs low.

Device Information

PART NUMBER	PACKAGE ⁽¹⁾	BODY SIZE (NOM)
SN74HCS157PW	TSSOP (16)	5.00 mm × 4.40 mm
SN74HCS157D	SOIC (16)	9.90 mm × 3.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.



Benefits of Schmitt-trigger inputs



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

Table of Contents

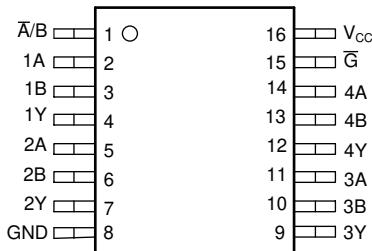
1 Features	1	8.3 Feature Description.....	9
2 Applications	1	8.4 Device Functional Modes.....	10
3 Description	1	9 Application and Implementation	11
4 Revision History	2	9.1 Application Information.....	11
5 Pin Configuration and Functions	3	9.2 Typical Application.....	11
6 Specifications	4	10 Power Supply Recommendations	14
6.1 Absolute Maximum Ratings	4	11 Layout.....	14
6.2 ESD Ratings	4	11.1 Layout Guidelines.....	14
6.3 Recommended Operating Conditions	4	11.2 Layout Example.....	14
6.4 Thermal Information	4	12 Device and Documentation Support	15
6.5 Electrical Characteristics	5	12.1 Documentation Support.....	15
6.6 Switching Characteristics	5	12.2 Receiving Notification of Documentation Updates..	15
6.7 Operating Characteristics	6	12.3 Support Resources.....	15
6.8 Typical Characteristics.....	7	12.4 Trademarks.....	15
7 Parameter Measurement Information	8	12.5 Electrostatic Discharge Caution.....	15
8 Detailed Description	9	12.6 Glossary.....	15
8.1 Reference.....	9	13 Mechanical, Packaging, and Orderable Information	16
8.2 Functional Block Diagram.....	9		

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

DATE	REVISION	NOTES
September 2020	*	Initial Release

5 Pin Configuration and Functions



D or PW Package 16-Pin SOIC or TSSOP Top View

Pin Functions

PIN		I/O ⁽¹⁾	DESCRIPTION
SOIC or TSSOP NO.	NAME		
1	Ā/B	I	Address select
2	1A	I	Channel 1, data input A
3	1B	I	Channel 1, data input B
4	1Y	I	Channel 1, data output
5	2A	O	Channel 2, data input A
6	2B	O	Channel 2, data input B
7	2Y	I	Channel 2, data output
8	GND	—	Ground
9	3Y	I	Channel 3, data output
10	3B	I	Channel 3, data input B
11	3A	I	Channel 3, data input A
12	4Y	I	Channel 4, data output
13	4B	I	Channel 4, data input B
14	4A	I	Channel 4, data input A
15	G	I	Output strobe, active low
16	V _{cc}	—	Positive supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		-0.5	7	V
I _{IK}	Input clamp current ⁽²⁾	V _I < -0.5 V or V _I > V _{CC} + 0.5 V		±20	mA
I _{OK}	Output clamp current ⁽²⁾	V _I < -0.5 V or V _I > V _{CC} + 0.5 V		±20	mA
I _O	Continuous output current	V _O = 0 to V _{CC}		±35	mA
	Continuous current through V _{CC} or GND			±70	mA
T _J	Junction temperature ⁽³⁾			150	°C
T _{stg}	Storage temperature		-65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

(3) Guaranteed by design.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±4000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1500

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V _{CC}	Supply voltage	2	5	6	V
V _I	Input voltage	0		V _{CC}	V
V _O	Output voltage	0		V _{CC}	V
T _A	Ambient temperature	-40		125	°C

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74HCS157		UNIT
		PW (TSSOP)	D (SOIC)	
		16 PINS	16 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	141.2	122.2	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	78.8	80.9	°C/W
R _{θJB}	Junction-to-board thermal resistance	85.8	80.6	°C/W
Ψ _{JT}	Junction-to-top characterization parameter	27.7	40.4	°C/W
Ψ _{JB}	Junction-to-board characterization parameter	85.5	80.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics application report](#).

6.5 Electrical Characteristics

over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted).

PARAMETER		TEST CONDITIONS		V _{CC}	MIN	TYP	MAX	UNIT
V _{T+}	Positive switching threshold			2 V	0.7		1.5	V
				4.5 V	1.7		3.15	
				6 V	2.1		4.2	
V _{T-}	Negative switching threshold			2 V	0.3		1.0	V
				4.5 V	0.9		2.2	
				6 V	1.2		3.0	
ΔV_T	Hysteresis ($V_{T+} - V_{T-}$) ⁽¹⁾			2 V	0.2		1.0	V
				4.5 V	0.4		1.4	
				6 V	0.6		1.6	
V _{OH}	High-level output voltage	V _I = V _{IH} or V _{IL}	I _{OH} = -20 μA	2 V to 6 V	V _{CC} - 0.1	V _{CC} - 0.002		V
			I _{OH} = -6 mA	4.5 V	4.0	4.3		
			I _{OH} = -7.8 mA	6 V	5.4	5.75		
V _{OL}	Low-level output voltage	V _I = V _{IH} or V _{IL}	I _{OL} = 20 μA	2 V to 6 V		0.002	0.1	V
			I _{OL} = 6 mA	4.5 V		0.18	0.30	
			I _{OL} = 7.8 mA	6 V		0.22	0.33	
I _I	Input leakage current	V _I = V _{CC} or 0		6 V		± 100	± 1000	nA
I _{CC}	Supply current	V _I = V _{CC} or 0, I _O = 0		6 V		0.1	2	μA
C _i	Input capacitance			2 V to 6 V			5	pF

(1) Guaranteed by design.

6.6 Switching Characteristics

C_L = 50 pF; over operating free-air temperature range (unless otherwise noted). See [Parameter Measurement Information](#).

PARAMETER		FROM	TO	V _{CC}	Operating free-air temperature (T _A)			UNIT	
					25°C		-40°C to 125°C		
					MIN	TYP	MAX		
f _{max}	Max switching frequency			2 V	6		5	MHz	
				4.5 V	31		25		
				6 V	36		29		
t _{pd}	Propagation delay	A or B	Y	2 V	21	32		ns	
				4.5 V	8	12			
				6 V	7	11			
		A/B	Y	2 V	21	32		ns	
				4.5 V	8	12			
				6 V	7	11			
		G̅	Y	2 V	22	33		ns	
				4.5 V	9	14			
				6 V	8	12			
t _t	Transition-time	Any output		2 V		13		ns	
				4.5 V		6			
				6 V		5			

6.7 Operating Characteristics

over operating free-air temperature range; typical values measured at $T_A = 25^\circ\text{C}$ (unless otherwise noted).

PARAMETER	TEST CONDITIONS	V _{CC}	MIN	TYP	MAX	UNIT
C _{pd}	Power dissipation capacitance per gate	No load	2 V to 6 V	40		pF

6.8 Typical Characteristics

$T_A = 25^\circ\text{C}$

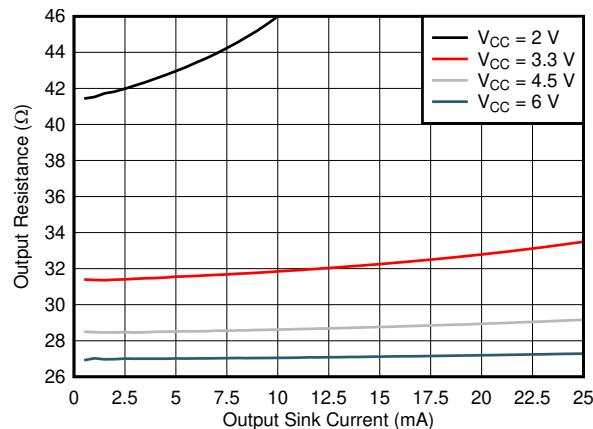


Figure 6-1. Output driver resistance in LOW state.

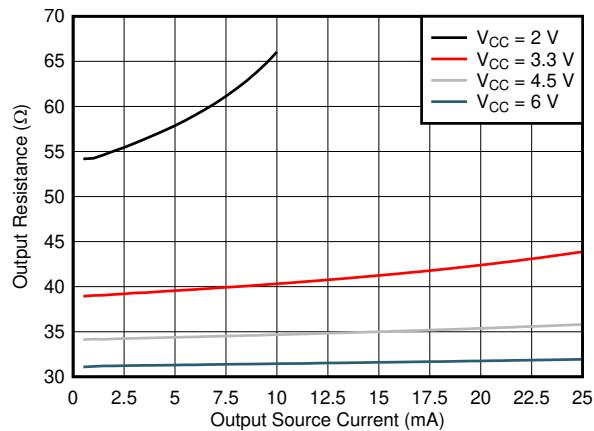


Figure 6-2. Output driver resistance in HIGH state.

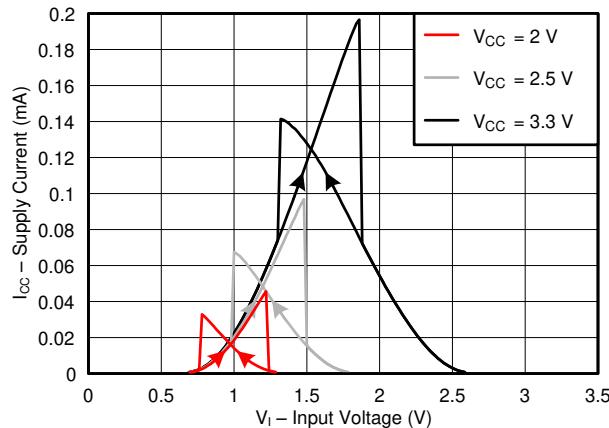


Figure 6-3. Supply current across input voltage, 2-, 2.5-, and 3.3-V supply

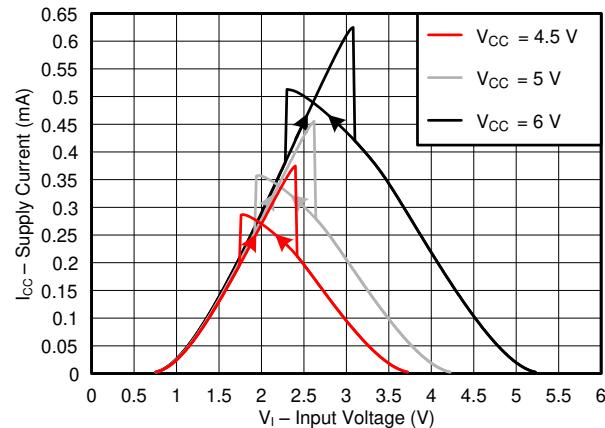


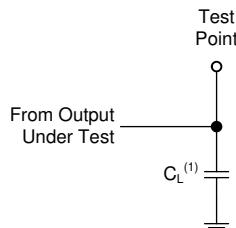
Figure 6-4. Supply current across input voltage, 4.5-, 5-, and 6-V supply

7 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR \leq 1 MHz, $Z_O = 50 \Omega$, $t_t < 2.5$ ns.

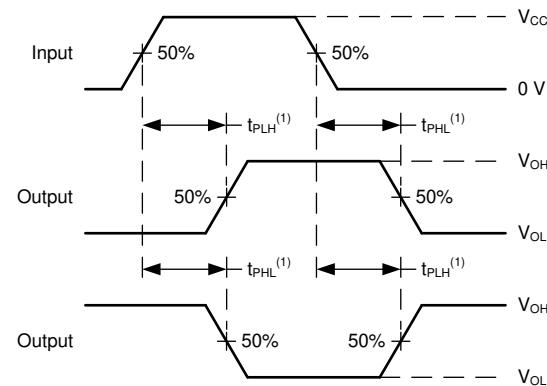
For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



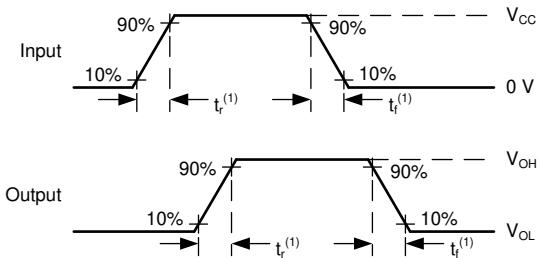
(1) C_L includes probe and test-fixture capacitance.

Figure 7-1. Load Circuit for Push-Pull Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

Figure 7-2. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t .

Figure 7-3. Voltage Waveforms, Input and Output Transition Times

8 Detailed Description

8.1 Reference

The SN74HCS157 is a high speed silicon gate CMOS multiplexer well suited to multiplexing and data routing applications. It contains four 2:1 multiplexers.

The SN74HCS157 operates asynchronously, with each Y output being equal to the input selected by the address input (\bar{A}/B). All four channels are controlled by the same address input.

The strobe (\bar{G}) input forces all Y outputs low, regardless of the state of other inputs.

All inputs include Schmitt-triggers allowing for slow input transitions and providing additional noise margin.

8.2 Functional Block Diagram

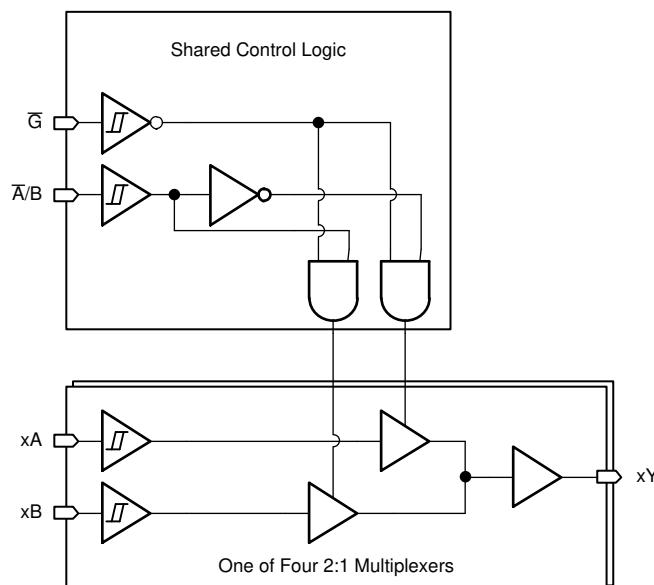


Figure 8-1. Logic Diagram (Positive Logic) for SN74HCS157

8.3 Feature Description

8.3.1 Balanced CMOS Push-Pull Outputs

This device includes balanced CMOS push-pull outputs. The term "balanced" indicates that the device can sink and source similar currents. The drive capability of this device may create fast edges into light loads so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to overcurrent. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

Unused push-pull CMOS outputs should be left disconnected.

8.3.2 CMOS Schmitt-Trigger Inputs

This device includes inputs with the Schmitt-trigger architecture. These inputs are high impedance and are typically modeled as a resistor in parallel with the input capacitance given in the *Electrical Characteristics* table from the input to ground. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings* table, and the maximum input leakage current, given in the *Electrical Characteristics* table, using Ohm's law ($R = V / I$).

The Schmitt-trigger input architecture provides hysteresis as defined by ΔV_T in the *Electrical Characteristics* table, which makes this device extremely tolerant to slow or noisy inputs. While the inputs can be driven much slower than standard CMOS inputs, it is still recommended to properly terminate unused inputs. Driving the

inputs with slow transitioning signals will increase dynamic current consumption of the device. For additional information regarding Schmitt-trigger inputs, please see [Understanding Schmitt Triggers](#).

8.3.3 Clamp Diode Structure

The inputs and outputs to this device have both positive and negative clamping diodes as depicted in [Electrical Placement of Clamping Diodes for Each Input and Output](#).

CAUTION

Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

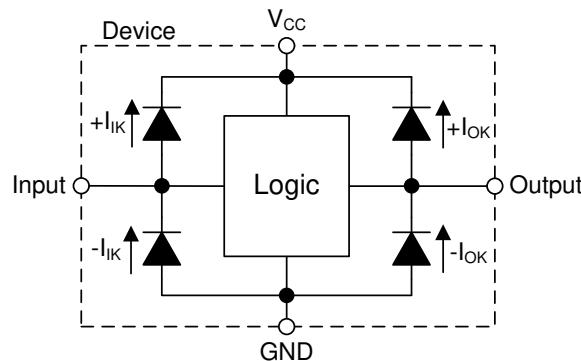


Figure 8-2. Electrical Placement of Clamping Diodes for Each Input and Output

8.4 Device Functional Modes

[Function Table](#) lists the functional modes of the SN74HCS157.

Table 8-1. Function Table

\bar{G}	INPUTS ⁽¹⁾			OUTPUT
	SELECT \bar{A}/B	DATA		
		A	B	Y
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

(1) H = High Voltage Level, L = Low Voltage Level, X = Don't Care

9 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74HCS157 is a quadruple 2-to-1 data selector/multiplexer. This application shows an example of using the device with all required connections to switch a 4-bit data bus between two source devices.

9.2 Typical Application

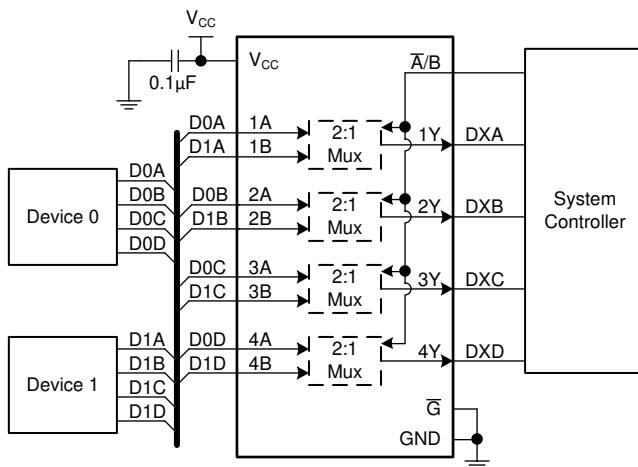


Figure 9-1. Typical application block diagram

9.2.1 Design Requirements

9.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the device's electrical characteristics as described in the *Electrical Characteristics*.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74HCS157 plus the maximum static supply current, I_{CC}, listed in *Electrical Characteristics* and any transient current required for switching. The logic device can only source as much current as is provided by the positive supply source. Be sure not to exceed the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74HCS157 plus the maximum supply current, I_{CC}, listed in *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current as can be sunk into its ground connection. Be sure not to exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74HCS157 can drive a load with a total capacitance less than or equal to 50 pF while still meeting all of the datasheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed 50 pF.

The SN74HCS157 can drive a load with total resistance described by R_L ≥ V_O / I_O, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the high state, the

output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in [CMOS Power Consumption and Cpd Calculation](#).

Thermal increase can be calculated using the information provided in [Thermal Characteristics of Standard Linear and Logic \(SLL\) Packages and Devices](#).

CAUTION

The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

9.2.1.2 Input Considerations

Input signals must cross $V_{t-(min)}$ to be considered a logic LOW, and $V_{t+(max)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. These can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input is to be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The resistor size is limited by drive current of the controller, leakage current into the SN74HCS157, as specified in the *Electrical Characteristics*, and the desired input transition rate. A 10-k Ω resistor value is often used due to these factors.

The SN74HCS157 has no input signal transition rate requirements because it has Schmitt-trigger inputs.

Another benefit to having Schmitt-trigger inputs is the ability to reject noise. Noise with a large enough amplitude can still cause issues. To know how much noise is too much, please refer to the $\Delta V_{T(min)}$ in the *Electrical Characteristics*. This hysteresis value will provide the peak-to-peak limit.

Unlike what happens with standard CMOS inputs, Schmitt-trigger inputs can be held at any valid value without causing huge increases in power consumption. The typical additional current caused by holding an input at a value other than V_{CC} or ground is plotted in the *Typical Characteristics*.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

9.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to *Feature Description* section for additional information regarding the outputs for this device.

9.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in the *Layout* section.
2. Ensure the capacitive load at the output is ≤ 50 pF. This is not a hard limit, however it will ensure optimal performance. This can be accomplished by providing short, appropriately sized traces from the SN74HCS157 to the receiving device(s).

3. Ensure the resistive load at the output is larger than $(V_{CC} / I_{O(max)}) \Omega$. This will ensure that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in megaohms; much larger than the minimum calculated above.
4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, [CMOS Power Consumption and Cpd Calculation](#).

9.2.3 Application Curve

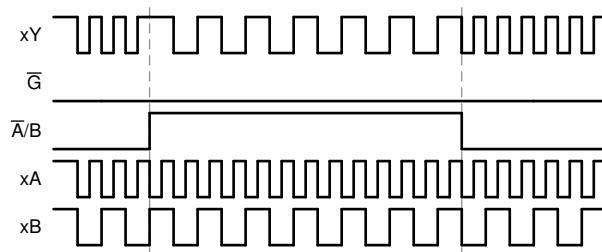


Figure 9-2. Application timing diagram

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μF and 1- μF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in given example layout image.

11 Layout

11.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

11.2 Layout Example

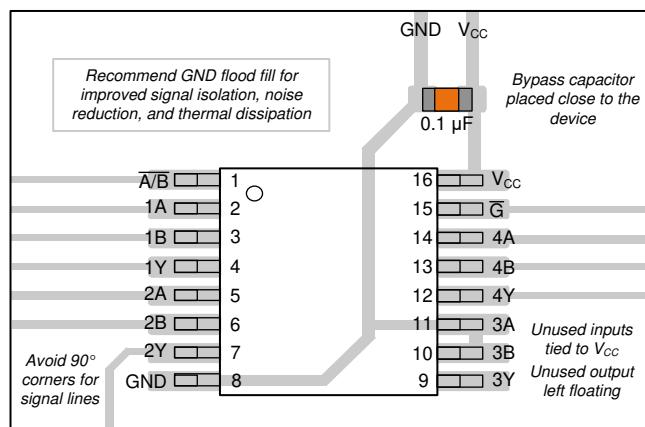


Figure 11-1. Example layout for the SN74HCS157.

12 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *HCMOS Design Considerations* application report (SCLA007)
- Texas Instruments, *CMOS Power Consumption and C_{pd} Calculation* application report (SDYA009)
- Texas Instruments, *Designing With Logic* application report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.3 Support Resources

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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12.4 Trademarks

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12.5 Electrostatic Discharge Caution

 This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



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PACKAGE OPTION ADDENDUM

6-Jan-2021

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74HCS157DR	ACTIVE	SOIC	D	16	2500	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	HCS157	Samples
SN74HCS157PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	HCS157	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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PACKAGE OPTION ADDENDUM

6-Jan-2021

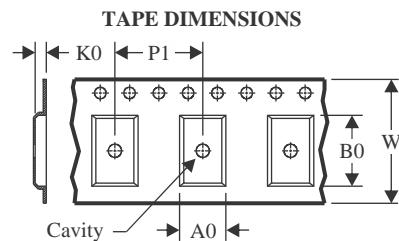
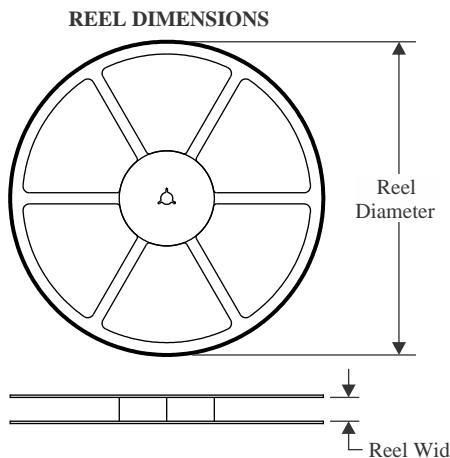
OTHER QUALIFIED VERSIONS OF SN74HCS157 :

- Automotive: [SN74HCS157-Q1](#)

NOTE: Qualified Version Definitions:

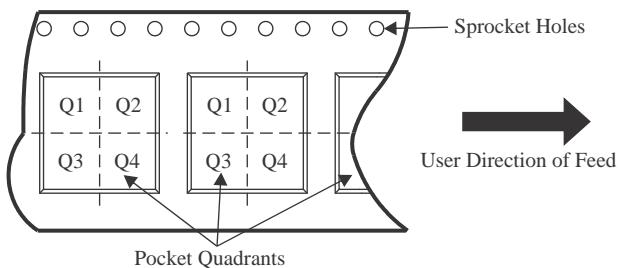
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION



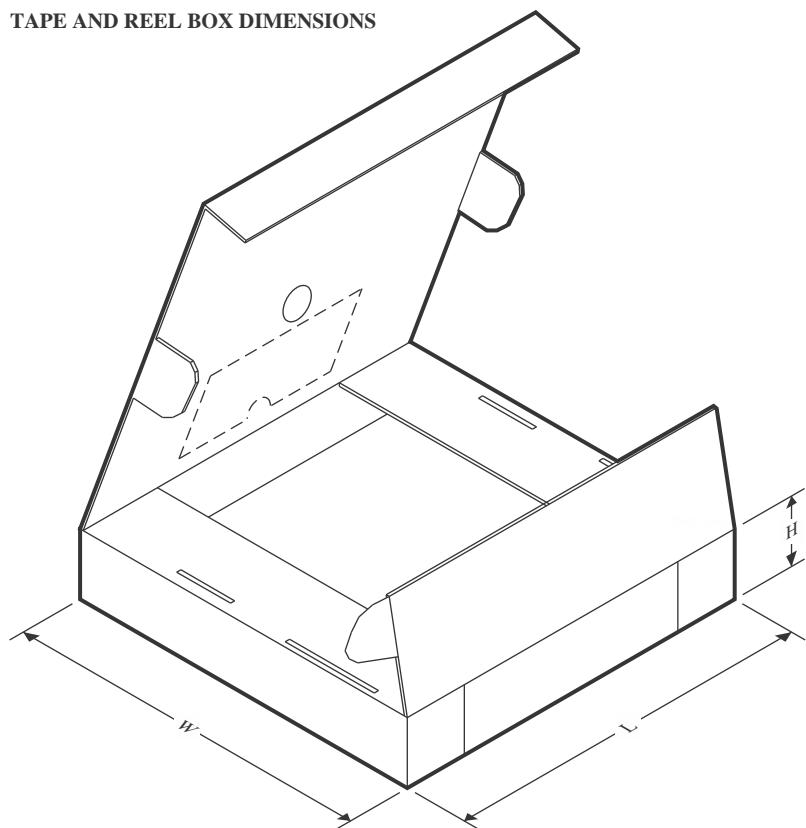
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74HCS157DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74HCS157DR	SOIC	D	16	2500	330.0	16.4	6.6	9.3	2.1	8.0	16.0	Q1
SN74HCS157PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74HCS157PWR	TSSOP	PW	16	2000	330.0	12.4	6.85	5.45	1.6	8.0	12.0	Q1

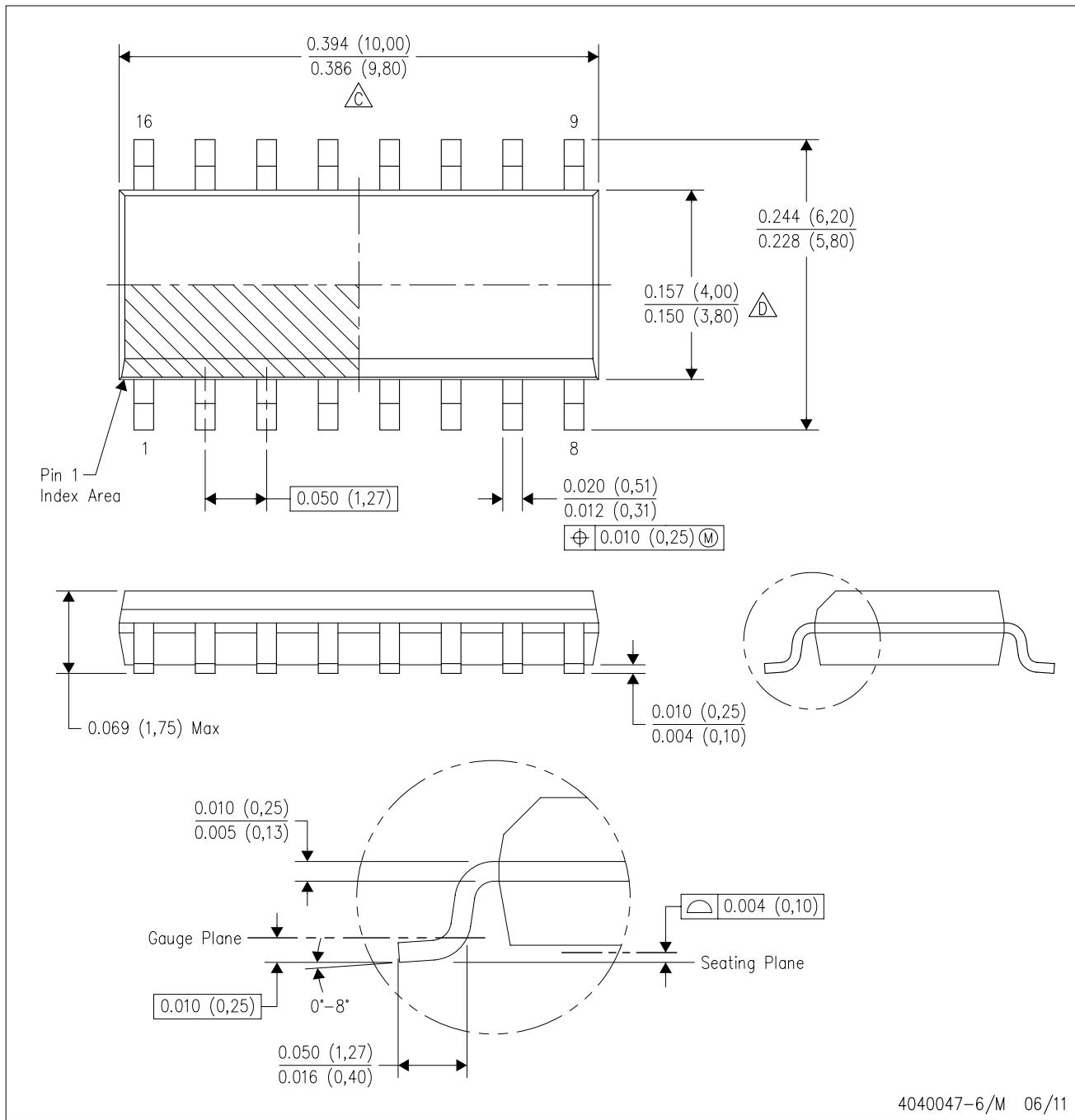
TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74HCS157DR	SOIC	D	16	2500	356.0	356.0	35.0
SN74HCS157DR	SOIC	D	16	2500	366.0	364.0	50.0
SN74HCS157PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74HCS157PWR	TSSOP	PW	16	2000	366.0	364.0	50.0

D (R-PDSO-G16)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

B. This drawing is subject to change without notice.

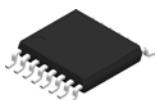
C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.

E. Reference JEDEC MS-012 variation AC.

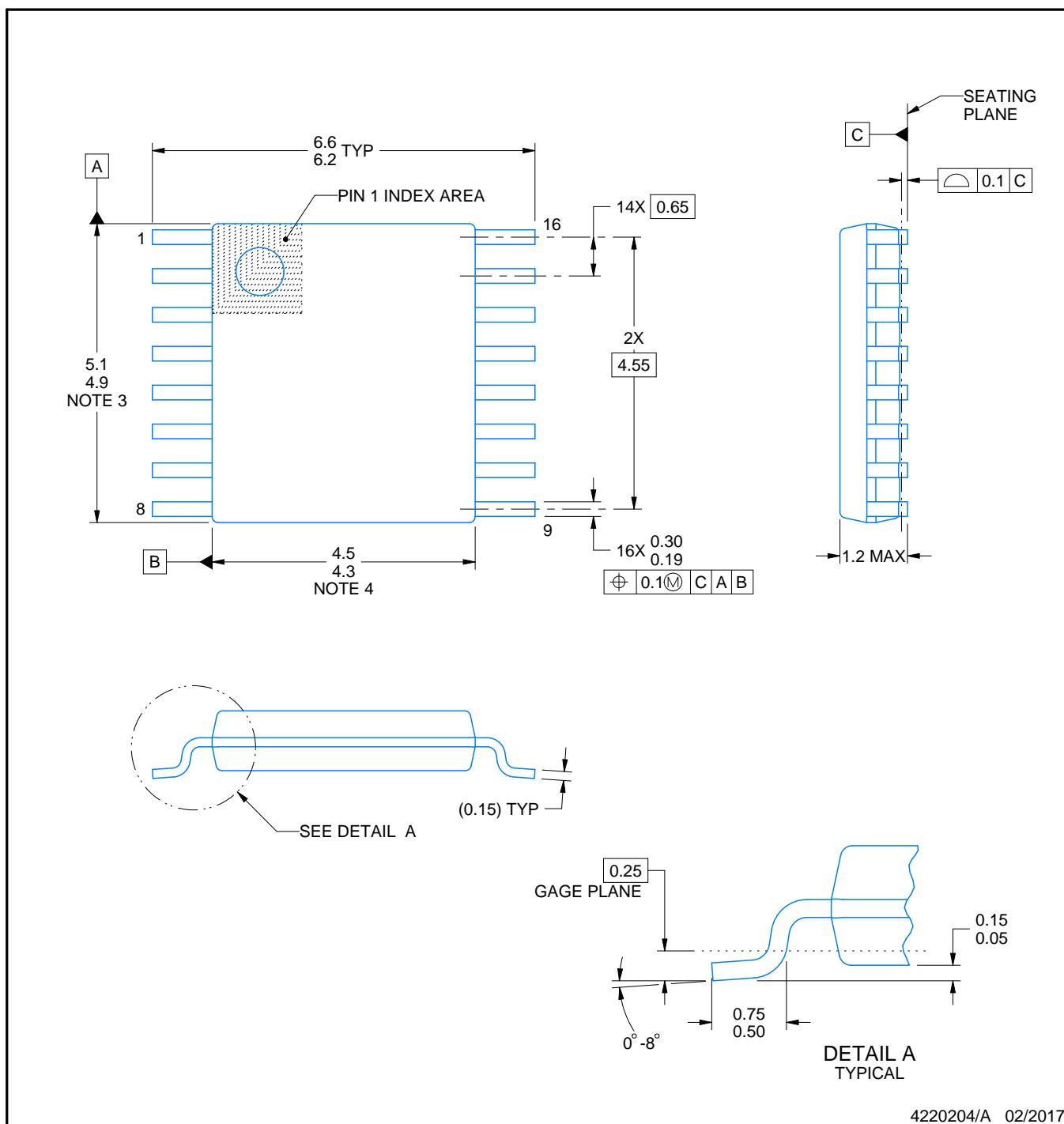
PACKAGE OUTLINE

PW0016A



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

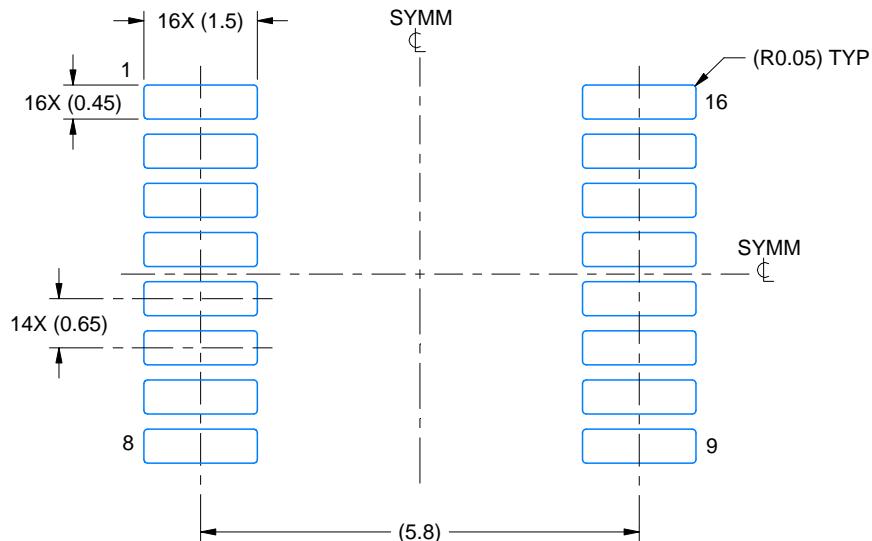
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

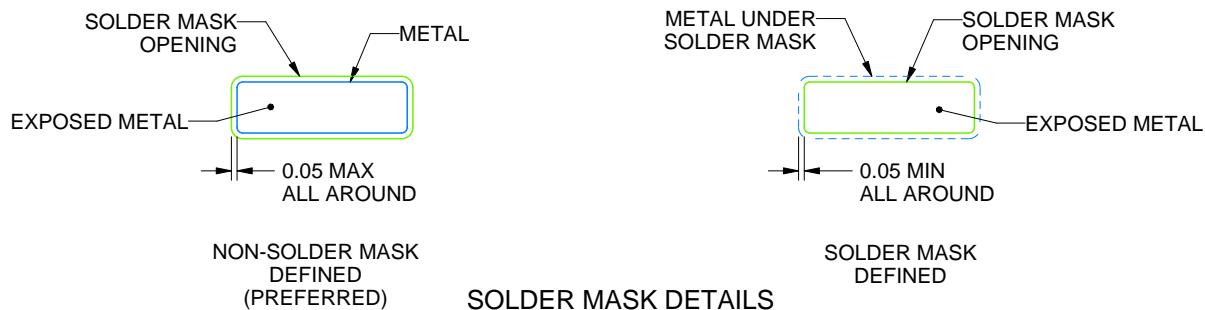
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

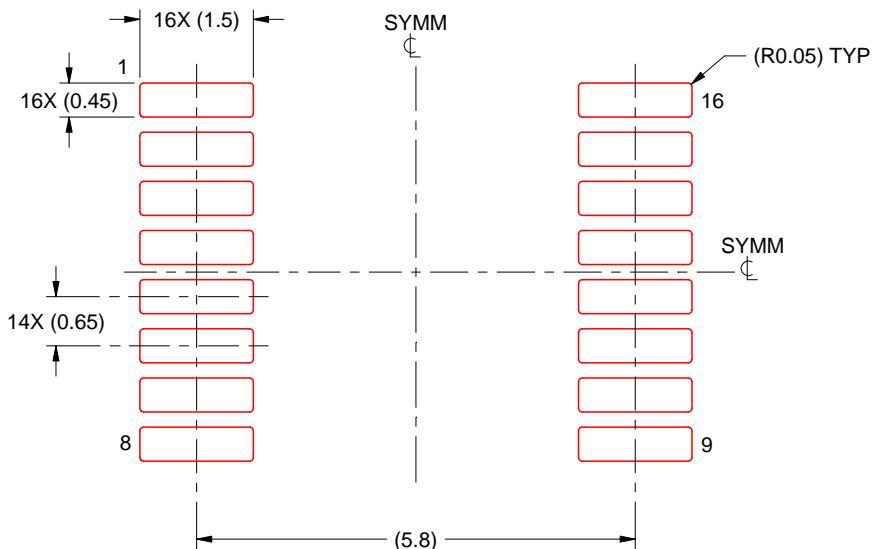
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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SNx4LV74A Dual Positive-Edge-Triggered D-Type Flip-Flops

1 Features

- 2-V to 5.5-V V_{CC} Operation
- Maximum t_{pd} of 8.5 ns at 5 V
- Typical V_{OLP} (Output Ground Bounce) < 0.8 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Typical V_{OHV} (Output V_{OH} Undershoot) > 2.3 V at $V_{CC} = 3.3$ V, $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-up Performance Exceeds 250 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 500-V Charged-Device Model (C101)

2 Applications

- Programmable Logic Controller (PLC)
- DCS and PAC: Analog Input Module
- AV Receiver
- Server PSU
- STB, DVR, and Streaming Media (Withdraw)
- Server Motherboard

3 Description

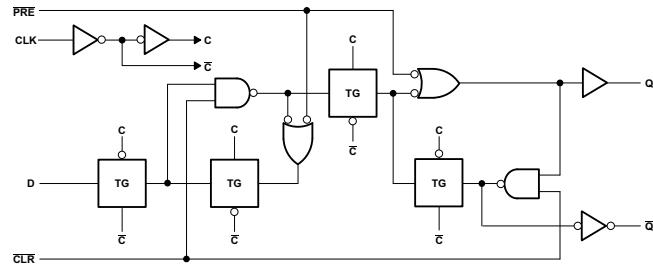
These dual positive-edge-triggered D-type flip-flops are designed for 2-V to 5.5-V V_{CC} operation.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
SN74LV74A	VQFN (14)	3.50 mm × 3.50 mm
	SOIC (14)	8.65 mm × 3.91 mm
	SOP (14)	10.30 mm × 5.30 mm
	SSOP (14)	6.20 mm × 5.30 mm
	TSSOP (14)	5.00 mm × 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Logic Diagram, Each Flip-Flop (Positive Logic)



An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. UNLESS OTHERWISE NOTED, this document contains PRODUCTION DATA.

Table of Contents

1 Features	1	7 Parameter Measurement Information	9
2 Applications	1	8 Detailed Description	10
3 Description	1	8.1 Overview	10
4 Revision History.....	2	8.2 Functional Block Diagram.....	10
5 Pin Configuration and Functions	3	8.3 Feature Description.....	10
6 Specifications.....	4	8.4 Device Functional Modes.....	11
6.1 Absolute Maximum Ratings	4	9 Application and Implementation	12
6.2 ESD Ratings.....	4	9.1 Application Information.....	12
6.3 Recommended Operating Conditions	5	9.2 Typical Application	12
6.4 Electrical Characteristics.....	5	10 Power Supply Recommendations	14
6.5 Switching Characteristics: $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	6	11 Layout.....	14
6.6 Switching Characteristics: $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	6	11.1 Layout Guidelines	14
6.7 Switching Characteristics: $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	6	11.2 Layout Example	14
6.8 Timing Requirements: $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$	6	12 Device and Documentation Support	15
6.9 Timing Requirements: $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$	7	12.1 Documentation Support	15
6.10 Timing Requirements: $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$	7	12.2 Trademarks	15
6.11 Noise Characteristics	7	12.3 Electrostatic Discharge Caution	15
6.12 Operating Characteristics.....	7	12.4 Glossary	15
6.13 Typical Characteristics	8	13 Mechanical, Packaging, and Orderable Information	15

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

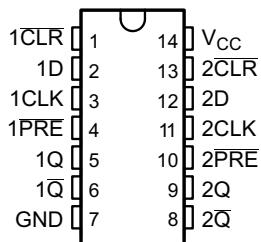
Changes from Revision L (April 2005) to Revision M

Page

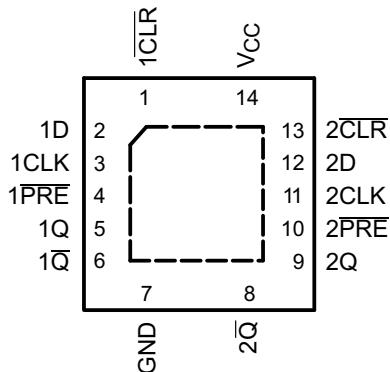
- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section 1
- Removed Ordering Information table. 1

5 Pin Configuration and Functions

**D, DGV, NS, or PW Package
14-PIN SOIC, SOP, SSOP, or TSSOP
Top View**



**RGY Package
14-PIN VQFN
Top View**



Pin Functions

PIN NO.	NAME	I/O	DESCRIPTION
1	1CLR	I	1 clear
2	1D	I	1D input
3	1CLK	I	1 clock
4	1PRE	I	1 preset
5	1Q	O	1Q output
6	1Q-bar	O	1Q-bar output
7	GND	–	GND
8	2Q-bar	O	2Q-bar output
9	2Q	O	2Q output
10	2PRE	I	2 preset
11	2CLK	I	2 clock
12	2D	I	2D input
13	2CLR	I	2 clear
14	Vcc	–	Supply voltage input

6 Specifications

6.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	-0.5	7	V
V_I	Input voltage ⁽²⁾	-0.5	7	V
V_O	Voltage applied to any output in the high-impedance or power-off state ⁽²⁾	-0.5	7	V
V_O	Output voltage ⁽²⁾⁽³⁾	-0.5	$V_{CC} + 0.5$	V
I_{IK}	Input clamp current	$V_I < 0$	-20	mA
I_{OK}	Output clamp current	$V_O < 0$	-50	mA
I_O	Continuous output current	$V_O = 0$ to V_{CC}	± 25	mA
	Continuous current through V_{CC} or GND		± 50	mA
θ_{JA}	Package thermal impedance	D package ⁽⁴⁾	86	°C/W
		DB package ⁽⁴⁾	96	
		DGV package ⁽⁴⁾	127	
		NS package ⁽⁴⁾	76	
		PW package ⁽⁴⁾	113	
		RGY package ⁽⁵⁾	47	
T_{STG}	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5 V maximum.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.
- (5) The package thermal impedance is calculated in accordance with JESD 51-5.

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	2000
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	500

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			SN54LV74A⁽²⁾		SN74LV74A		UNIT
			MIN	MAX	MIN	MAX	
V _{CC}	Supply voltage		2	5.5	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5				V
		V _{CC} = 2.3 V to 2.7 V	V _{CC} × 0.7	V _{CC} × 0.7			
		V _{CC} = 3 V to 3.6 V	V _{CC} × 0.7	V _{CC} × 0.7			
		V _{CC} = 4.5 V to 5.5 V	V _{CC} × 0.7	V _{CC} × 0.7			
V _{IL}	Low-level input voltage	V _{CC} = 2 V		0.5	0.5		V
		V _{CC} = 2.3 V to 2.7 V		V _{CC} × 0.3	V _{CC} × 0.3		
		V _{CC} = 3 V to 3.6 V		V _{CC} × 0.3	V _{CC} × 0.3		
		V _{CC} = 4.5 V to 5.5 V		V _{CC} × 0.3	V _{CC} × 0.3		
V _I	Input voltage		0	5.5	0	5.5	V
V _O	Output voltage		0	V _{CC}	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V		-50	-50	μA	mA
		V _{CC} = 2.3 V to 2.7 V		-2	-2		
		V _{CC} = 3 V to 3.6 V		-6	-6		
		V _{CC} = 4.5 V to 5.5 V		-12	-12		
I _{OL}	Low-level output current	V _{CC} = 2 V		50	50	μA	mA
		V _{CC} = 2.3 V to 2.7 V		2	2		
		V _{CC} = 3 V to 3.6 V		6	6		
		V _{CC} = 4.5 V to 5.5 V		12	12		
Δt/Δv	Input transition rise or fall rate	V _{CC} = 2.3 V to 2.7 V		200	200		ns/V
		V _{CC} = 3 V to 3.6 V		100	100		
		V _{CC} = 4.5 V to 5.5 V		20	20		
T _A	Operating free-air temperature		-55	125	-40	125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

(2) Product Preview

6.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	SN54LV74A⁽¹⁾			SN74LV74A -40°C to 85°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V _{OH}	I _{OH} = -50 μA	2 V to 5.5 V	V _{CC} –0.1			V _{CC} –0.1			V
	I _{OH} = -2 mA	2.3 V	2			2			
	I _{OH} = -6 mA	3 V	2.48			2.48			
	I _{OH} = -12 mA	4.5 V	3.8			3.8			
V _{OL}	I _{OL} = 50 μA	2 V to 5.5 V		0.1		0.1		0.1	V
	I _{OL} = 2 mA	2.3 V		0.4		0.4		0.4	
	I _{OL} = 6 mA	3 V		0.44		0.44		0.44	
	I _{OL} = 12 mA	4.5 V		0.55		0.55		0.55	
I _I	V _I = 5.5 V or GND	0 to 5.5 V		±1		±1		±1	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V		20		20		20	μA
I _{off}	V _I or V _O = 5.5 V	0		5		5		5	μA
C _I	V _I = V _{CC} or GND	3.3 V		2		2		2	pF
		5 V		2		2		2	

(1) Product Preview

SN54LV74A, SN74LV74A

SCLS381M – AUGUST 1997 – REVISED MARCH 2015

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6.5 Switching Characteristics: $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV74A ⁽¹⁾		SN74LV74A $-40^\circ\text{C} \text{ to } 85^\circ\text{C}$		SN74LV74A $-40^\circ\text{C} \text{ to } 125^\circ\text{C}$		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15 \text{ pF}$	50 ⁽²⁾	100 ⁽²⁾		40 ⁽²⁾		40		40	MHz	
				$C_L = 50 \text{ pF}$	30	70	25		25		25		
t_{pd}	$\overline{\text{PRE}} \text{ or } \overline{\text{CLR}}$	Q or \overline{Q}	$C_L = 15 \text{ pF}$	9.8 ⁽²⁾	14.8 ⁽²⁾		1 ⁽²⁾	17 ⁽²⁾	1	17	1	18	ns
				CLK	11.1 ⁽²⁾	16.4 ⁽²⁾	1 ⁽²⁾	19 ⁽²⁾	1	19	1	20	
t_{pd}	$\overline{\text{PRE}} \text{ or } \overline{\text{CLR}}$	Q or \overline{Q}	$C_L = 50 \text{ pF}$	13	17.4		1	20	1	20	1	21	ns
				CLK	14.2	20	1	23	1	23	1	24	

(1) Product Preview

(2) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.6 Switching Characteristics: $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV74A ⁽¹⁾		SN74LV74A $-40^\circ\text{C} \text{ to } 85^\circ\text{C}$		SN74LV74A $-40^\circ\text{C} \text{ to } 125^\circ\text{C}$		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15 \text{ pF}$	80 ⁽²⁾	140 ⁽²⁾		70 ⁽²⁾		70		70	MHz	
				$C_L = 50 \text{ pF}$	50	90	45		45		45		
t_{pd}	$\overline{\text{PRE}} \text{ or } \overline{\text{CLR}}$	Q or \overline{Q}	$C_L = 15 \text{ pF}$	6.9 ⁽²⁾	12.3 ⁽²⁾		1 ⁽²⁾	14.5 ⁽²⁾	1	14.5	1	15.5	ns
				CLK	7.9 ⁽²⁾	11.9 ⁽²⁾	1 ⁽²⁾	14 ⁽²⁾	1	14	1	15	
t_{pd}	$\overline{\text{PRE}} \text{ or } \overline{\text{CLR}}$	Q or \overline{Q}	$C_L = 50 \text{ pF}$	9.2	15.8		1	18	1	18	1	19	ns
				CLK	10.2	15.4	1	17.5	1	17.5	1	18.5	

(1) Product Preview

(2) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.7 Switching Characteristics: $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see [Figure 3](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54LV74A ⁽¹⁾		SN74LV74A $-40^\circ\text{C} \text{ to } 85^\circ\text{C}$		SN74LV74A $-40^\circ\text{C} \text{ to } 125^\circ\text{C}$		
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15 \text{ pF}$	130 ⁽²⁾	180 ⁽²⁾		110 ⁽²⁾		110		110	MHz	
				$C_L = 50 \text{ pF}$	90	140	75		75		75		
t_{pd}	$\overline{\text{PRE}} \text{ or } \overline{\text{CLR}}$	Q or \overline{Q}	$C_L = 15 \text{ pF}$	5 ⁽²⁾	7.7 ⁽²⁾		1 ⁽²⁾	9 ⁽²⁾	1	9	1	10	ns
				CLK	5.6 ⁽²⁾	7.3 ⁽²⁾	1 ⁽²⁾	8.5 ⁽²⁾	1	8.5	1	9.5	
t_{pd}	$\overline{\text{PRE}} \text{ or } \overline{\text{CLR}}$	Q or \overline{Q}	$C_L = 50 \text{ pF}$	6.6	9.7		1	11	1	11	1	12	ns
				CLK	7.2	9.3	1	10.5	1	10.5	1	11.5	

(1) Product Preview

(2) On products compliant to MIL-PRF-38535, this parameter is not production tested.

6.8 Timing Requirements: $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 2.5 \text{ V} \pm 0.2 \text{ V}$ (unless otherwise noted) (see [Figure 3](#))

				$T_A = 25^\circ\text{C}$		SN54LV74A ⁽¹⁾		SN74LV74A $-40^\circ\text{C} \text{ to } 85^\circ\text{C}$		SN74LV74A $-40^\circ\text{C} \text{ to } 125^\circ\text{C}$		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration		$\overline{\text{PRE}} \text{ or } \overline{\text{CLR}}$ low	8		9		9		9		ns
				CLK	8		9		9		9	
t_{su}	Setup time before CLK↑		Data	8		9		9		9		ns
			$\overline{\text{PRE}} \text{ or } \overline{\text{CLR}}$ inactive	7		7		7		7		
t_h	Hold time, data after CLK↑			0.5		0.5		0.5		0.5		ns

(1) Product Preview

6.9 Timing Requirements: $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 3.3 \text{ V} \pm 0.3 \text{ V}$ (unless otherwise noted) (see [Figure 3](#))

		$T_A = 25^\circ\text{C}$		SN54LV74A ⁽¹⁾		SN74LV74A $-40^\circ\text{C} \text{ to } 85^\circ\text{C}$		SN74LV74A $-40^\circ\text{C} \text{ to } 125^\circ\text{C}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	PRE or CLR low	6	7	7	7	7	7	7	ns
	CLK	CLK	6	7	7	7	7	7	7	
t_{su}	Setup time before CLK↑	Data	6	7	7	7	7	7	7	ns
		PRE or CLR inactive	5	5	5	5	5	5	5	
t_h	Hold time, data after CLK↑		0.5	0.5	0.5	0.5	0.5	0.5	0.5	ns

(1) Product Preview

6.10 Timing Requirements: $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$

over recommended operating free-air temperature range, $V_{CC} = 5 \text{ V} \pm 0.5 \text{ V}$ (unless otherwise noted) (see [Figure 3](#))

		$T_A = 25^\circ\text{C}$		SN54LV74A ⁽¹⁾		SN74LV74A $-40^\circ\text{C} \text{ to } 85^\circ\text{C}$		SN74LV74A $-40^\circ\text{C} \text{ to } 125^\circ\text{C}$		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	PRE or CLR low	5	5	5	5	5	5	5	ns
	CLK	CLK	5	5	5	5	5	5	5	
t_{su}	Setup time before CLK↑	Data	5	5	5	5	5	5	5	ns
		PRE or CLR inactive	3	3	3	3	3	3	3	
t_h	Hold time, data after CLK↑		0.5	0.5	0.5	0.5	0.5	0.5	0.5	ns

(1) Product Preview

6.11 Noise Characteristics⁽¹⁾

$V_{CC} = 3.3 \text{ V}$, $C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$

PARAMETER	SN74LV74A			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}	0.1	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}	0	-0.8	V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	3.2		V
$V_{IH(D)}$	High-level dynamic input voltage	2.31		V
$V_{IL(D)}$	Low-level dynamic input voltage	0.99		V

(1) Characteristics are for surface-mount packages only.

6.12 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	V_{CC}	TYP	UNIT
C_{pd}	$C_L = 50 \text{ pF}$	$f = 10 \text{ MHz}$	3.3 V	21
			5 V	23

6.13 Typical Characteristics

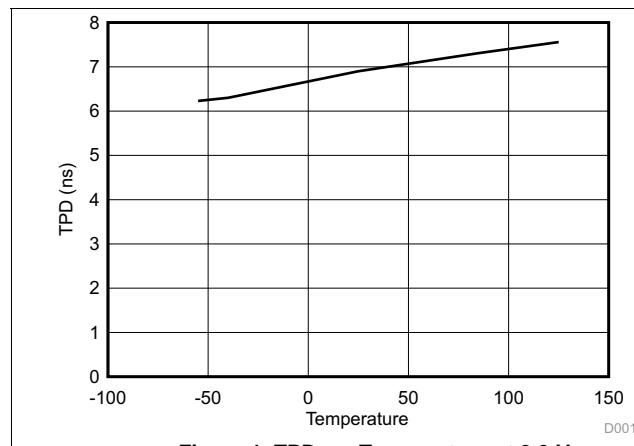


Figure 1. TPD vs. Temperature at 3.3 V

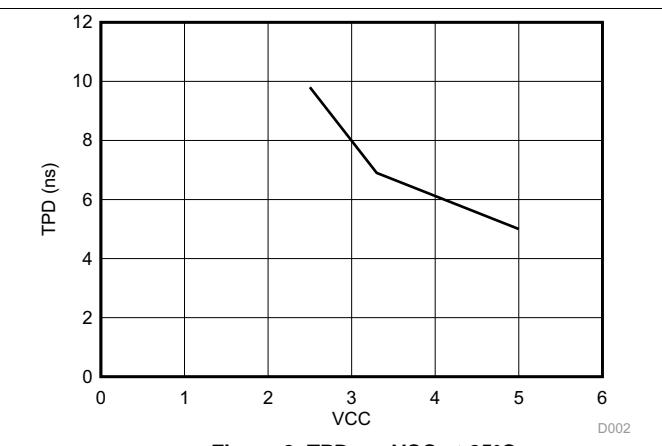
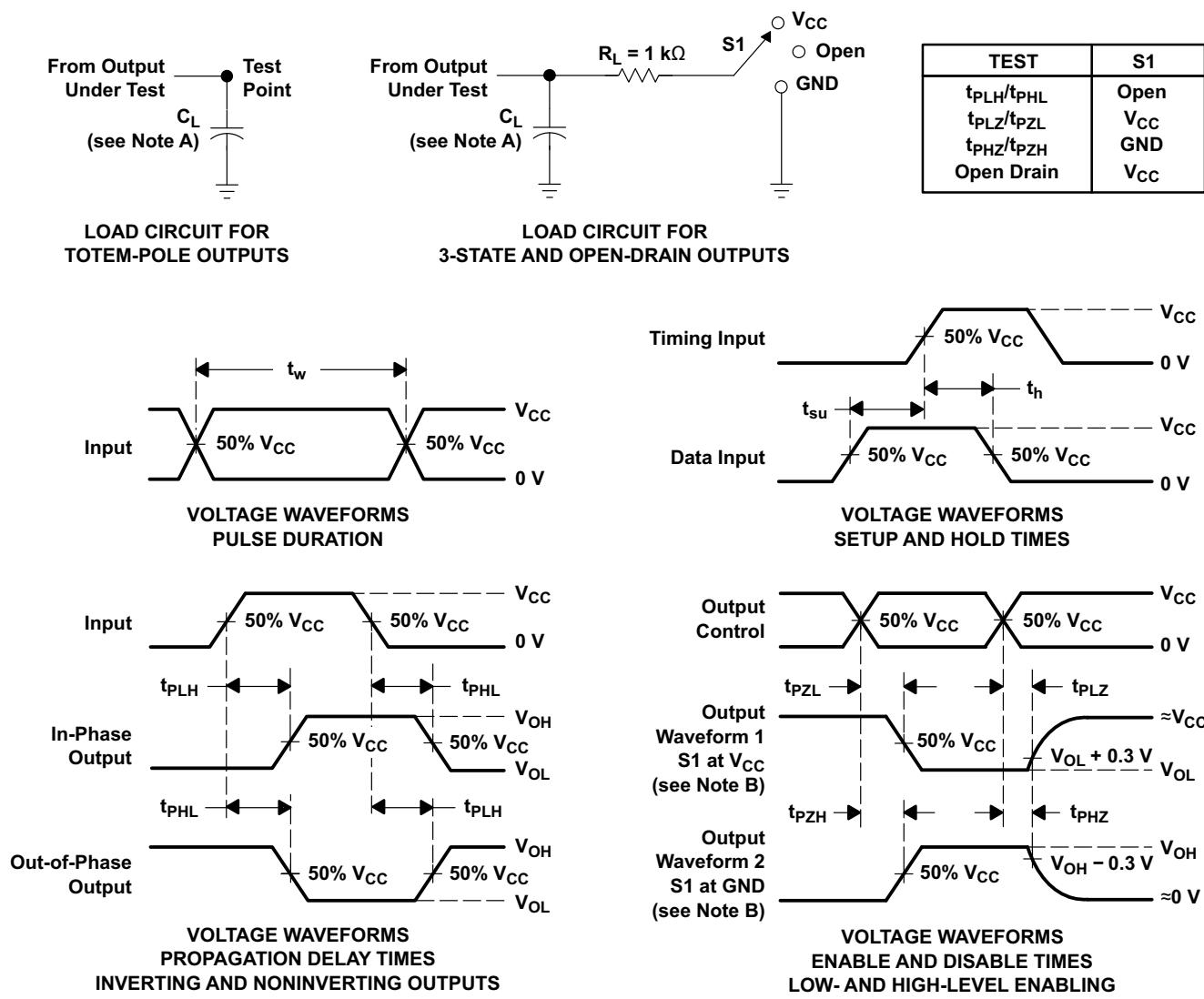


Figure 2. TPD vs. VCC at 25°C

7 Parameter Measurement Information



- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 3 \text{ ns}$, $t_f \leq 3 \text{ ns}$.
 - The outputs are measured one at a time, with one input transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PHL} and t_{PLH} are the same as t_{pd} .
 - All parameters and waveforms are not applicable to all devices.

Figure 3. Load Circuit and Voltage Waveforms

8 Detailed Description

8.1 Overview

These dual positive-edge-triggered D-type flip-flops are designed for 2-V to 5.5-V V_{CC} operation.

A low level at the preset (\overline{PRE}) or clear (\overline{CLR}) inputs sets or resets the outputs, regardless of the levels of the other inputs. When \overline{PRE} and \overline{CLR} are inactive (high), data at the data (D) inputs meeting the setup-time requirements is transferred to the outputs on the positive-going edge of the clock pulse. Clock triggering occurs at a voltage level and is not directly related to the rise time of the clock pulse. Following the hold-time interval, data at the D input can be changed without affecting the levels at the outputs. The state of the output upon power-up is not known until the first valid clock edge has occurred while V_{CC} is within *Recommended Operating Conditions*.

These devices are fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down.

8.2 Functional Block Diagram

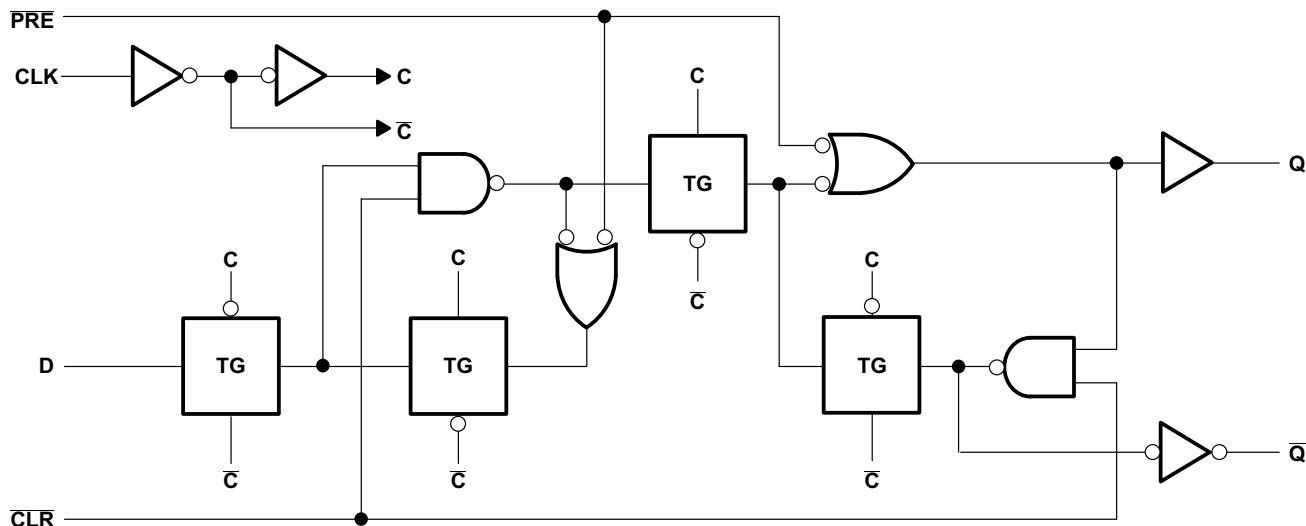


Figure 4. Logic Diagram, Each Flip-Flop (Positive Logic)

8.3 Feature Description

The device's wide operating range allows it to be used in a variety of systems that use different logic levels. The low propagation delay allows fast switching and higher speeds of operation. In addition, the low ground bounce stabilizes the performance of non-switching outputs while another output is switching.

8.4 Device Functional Modes

Table 1. Function Table

INPUTS				OUTPUTS	
PRE	CLR	CLK	D	Q	Q̄
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H ⁽¹⁾	H ⁽¹⁾
H	H	↑	H	H	L
H	H	↑	L	L	H
H	H	L	X	Q ₀	Q̄ ₀

- (1) This configuration is nonstable; that is, it does not persist when **PRE** or **CLR** returns to its inactive (high) level.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The SN74LV74A is a Low drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs can accept voltages to 5.5 V at any valid V_{CC} making it Ideal for down translation.

9.2 Typical Application

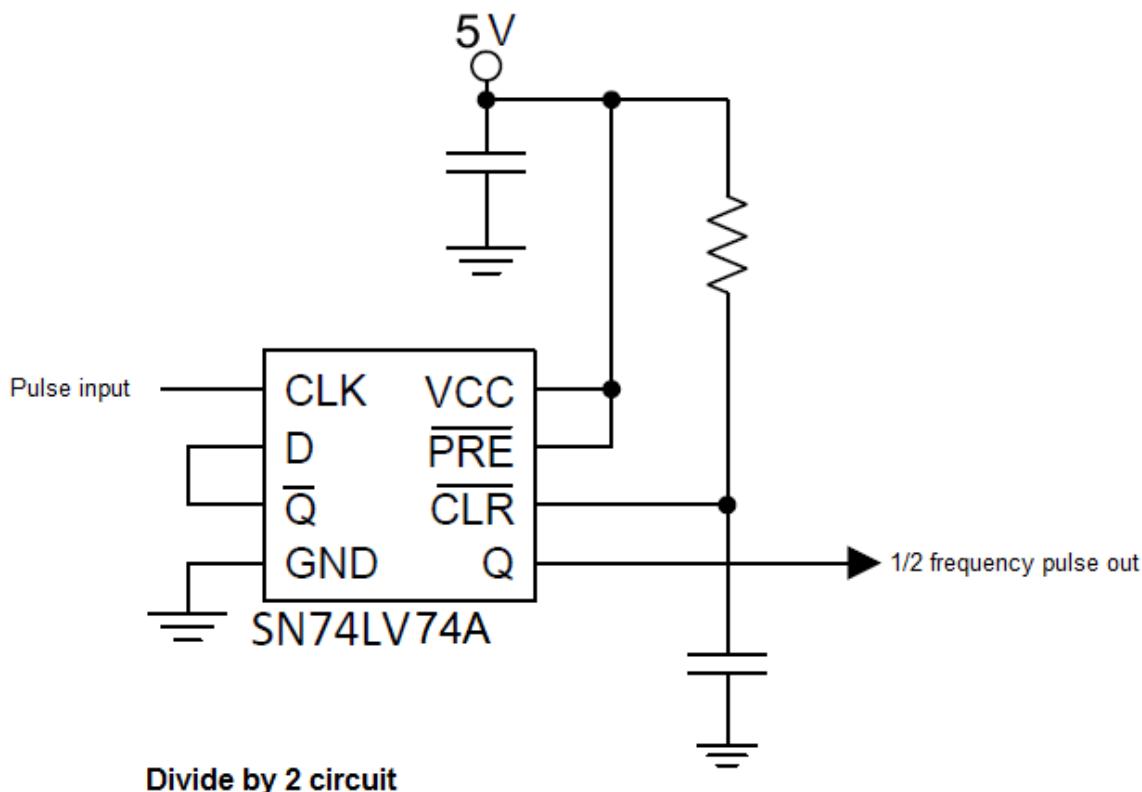


Figure 5. Typical Application Schematic

9.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Take care to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so consider routing and load conditions to prevent ringing.

Typical Application (continued)

9.2.2 Detailed Design Procedure

- Recommended input conditions:
 - Specified High and low levels. See (V_{IH} and V_{IL}) in *Recommended Operating Conditions*.
 - Inputs are overvoltage tolerant allowing them to go as high as 5.5 V at any valid V_{CC} .
- Recommended output conditions:
 - Load currents should not exceed 25 mA per output and 50 mA total for the part.
 - Outputs should not be pulled above V_{CC} .

9.2.3 Application Curves

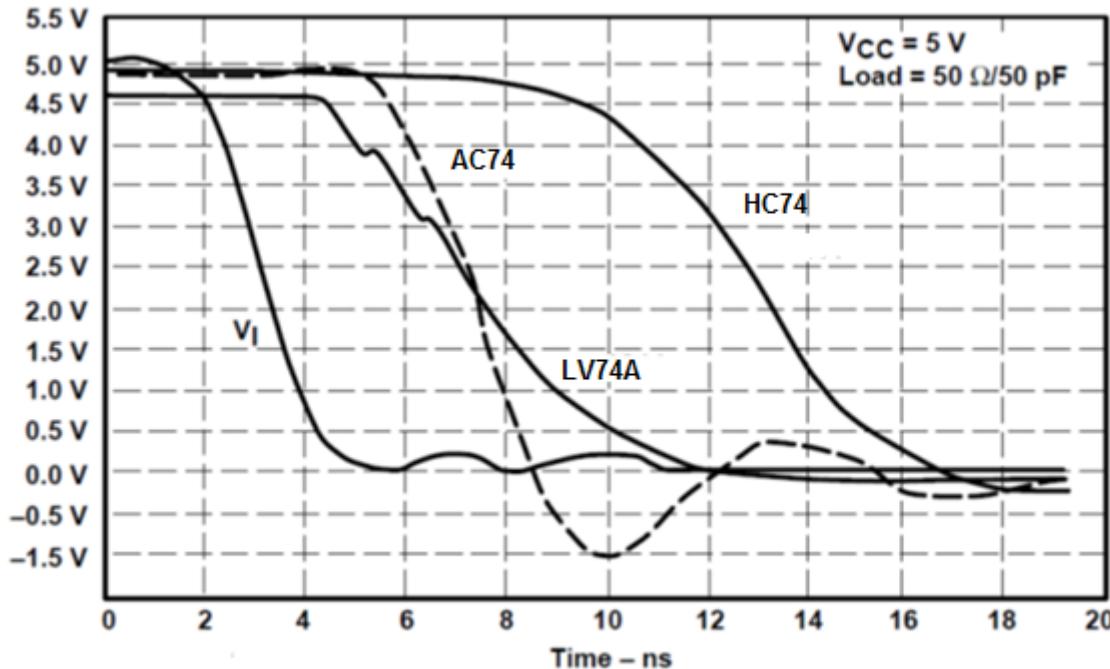


Figure 6. Switching Characteristics Comparison

10 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*.

Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends a 0.1- μF capacitor and if there are multiple V_{CC} terminals then TI recommends a 0.01- μF or 0.022- μF capacitor for each power terminal. Multiple bypass capacitors can be paralleled to reject different frequencies of noise. Frequencies of 0.1 μF and 1 μF are commonly used in parallel. The bypass capacitor should be installed as close as possible to the power terminal for best results.

11 Layout

11.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only three of the four buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or V_{CC} whichever make more sense or is more convenient. Floating outputs is generally acceptable, unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the I.O's so they also cannot float when disabled.

11.2 Layout Example

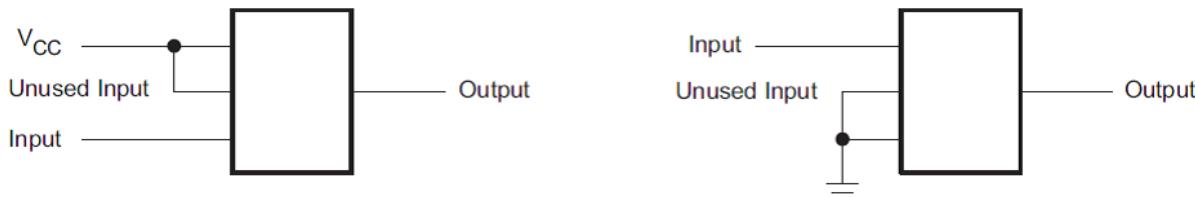


Figure 7. Layout Recommendation

12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation see the following:

Implications of Slow or Floating CMOS Inputs, SCBA004

12.2 Trademarks

All trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

[SLY022 — TI Glossary](#).

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.



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PACKAGE OPTION ADDENDUM

10-Dec-2020

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV74AD	ACTIVE	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV74A	Samples
SN74LV74ADBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV74A	Samples
SN74LV74ADGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV74A	Samples
SN74LV74ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV74A	Samples
SN74LV74ANSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV74A	Samples
SN74LV74APW	ACTIVE	TSSOP	PW	14	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV74A	Samples
SN74LV74APWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	LV74A	Samples
SN74LV74APWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV74A	Samples
SN74LV74APWT	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV74A	Samples
SN74LV74ARGYR	ACTIVE	VQFN	RGY	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	LV74A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.



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PACKAGE OPTION ADDENDUM

10-Dec-2020

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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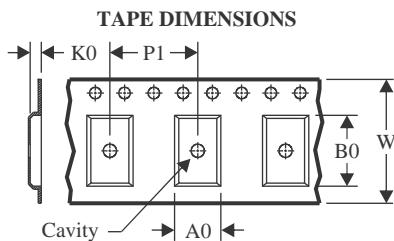
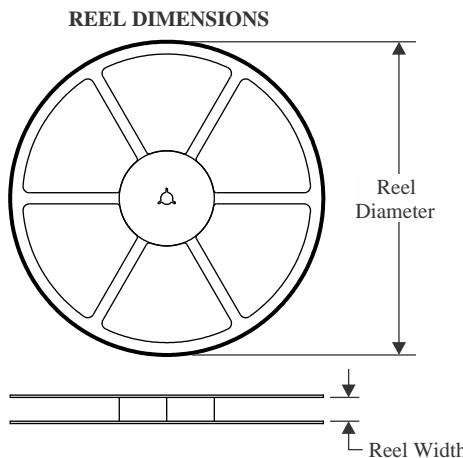
OTHER QUALIFIED VERSIONS OF SN74LV74A :

- Automotive: [SN74LV74A-Q1](#)
- Enhanced Product: [SN74LV74A-EP](#)

NOTE: Qualified Version Definitions:

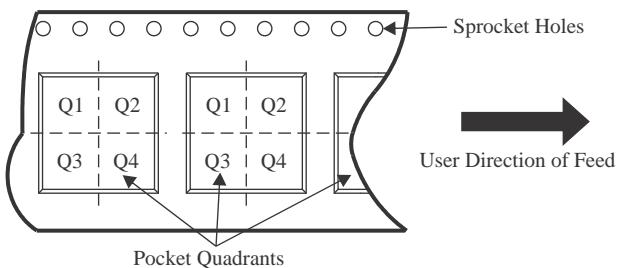
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION



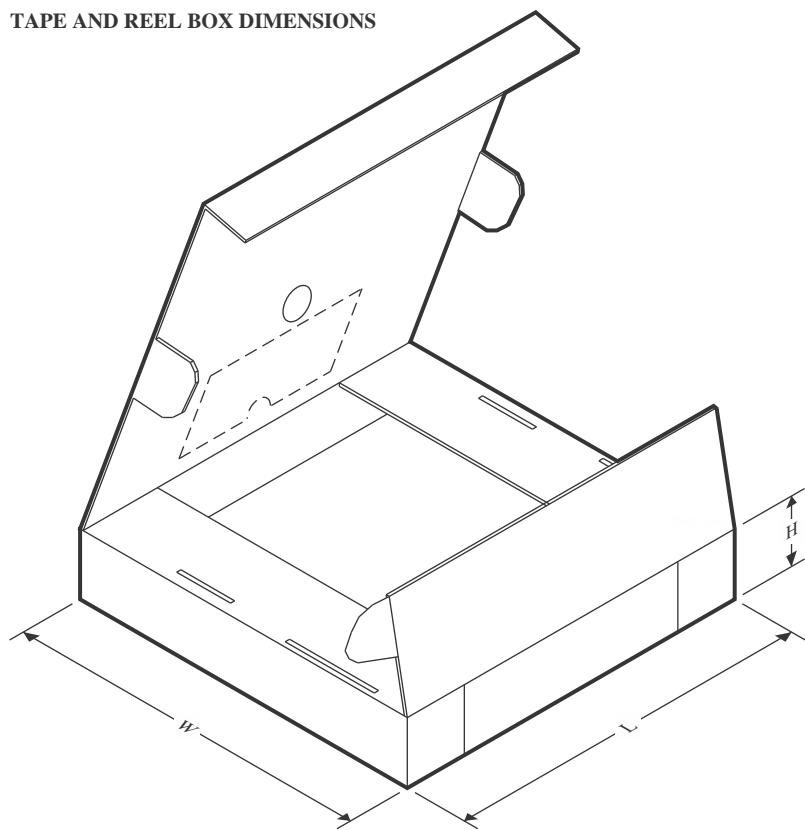
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



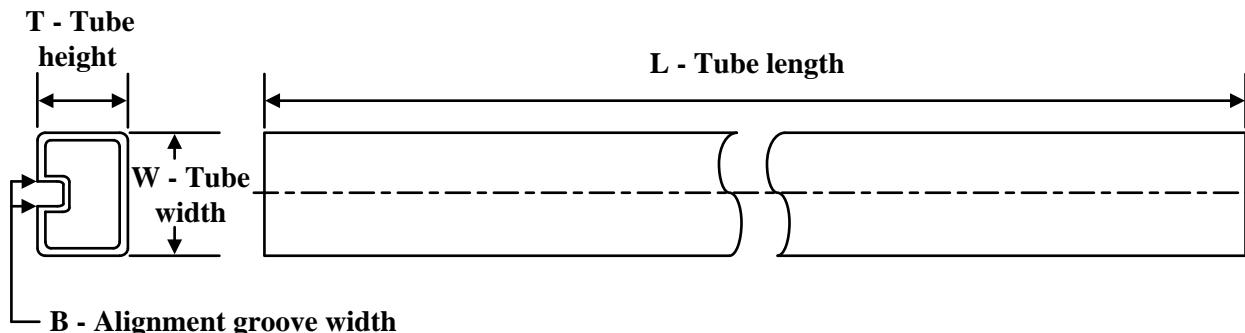
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV74ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV74ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV74ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV74ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV74APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV74APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV74APWRG4	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV74APWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74LV74ARGYR	VQFN	RGY	14	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV74ADBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LV74ADGVR	TVSOP	DGV	14	2000	356.0	356.0	35.0
SN74LV74ADR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LV74ANSR	SO	NS	14	2000	367.0	367.0	38.0
SN74LV74APWR	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LV74APWR	TSSOP	PW	14	2000	364.0	364.0	27.0
SN74LV74APWRG4	TSSOP	PW	14	2000	356.0	356.0	35.0
SN74LV74APWT	TSSOP	PW	14	250	356.0	356.0	35.0
SN74LV74ARGYR	VQFN	RGY	14	3000	356.0	356.0	35.0

TUBE


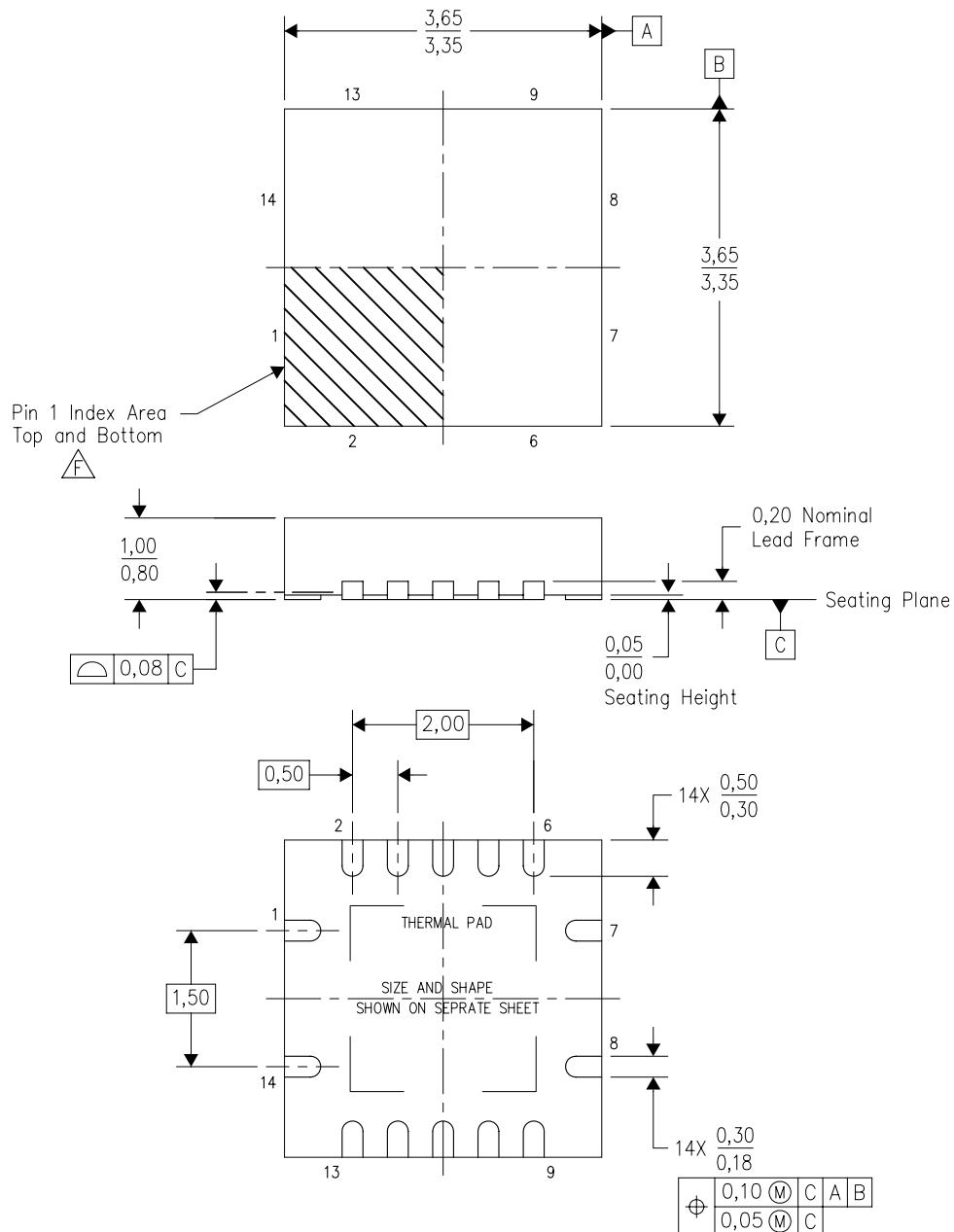
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μ m)	B (mm)
SN74LV74AD	D	SOIC	14	50	506.6	8	3940	4.32
SN74LV74APW	PW	TSSOP	14	90	530	10.2	3600	3.5

MECHANICAL DATA

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



Bottom View

4203539-2/l 06/2011

- NOTES:
- All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - This drawing is subject to change without notice.
 - QFN (Quad Flatpack No-Lead) package configuration.
 - The package thermal pad must be soldered to the board for thermal and mechanical performance.
 - See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
 - Package complies to JEDEC M0-241 variation BA.

THERMAL PAD MECHANICAL DATA

RGY (S-PVQFN-N14)

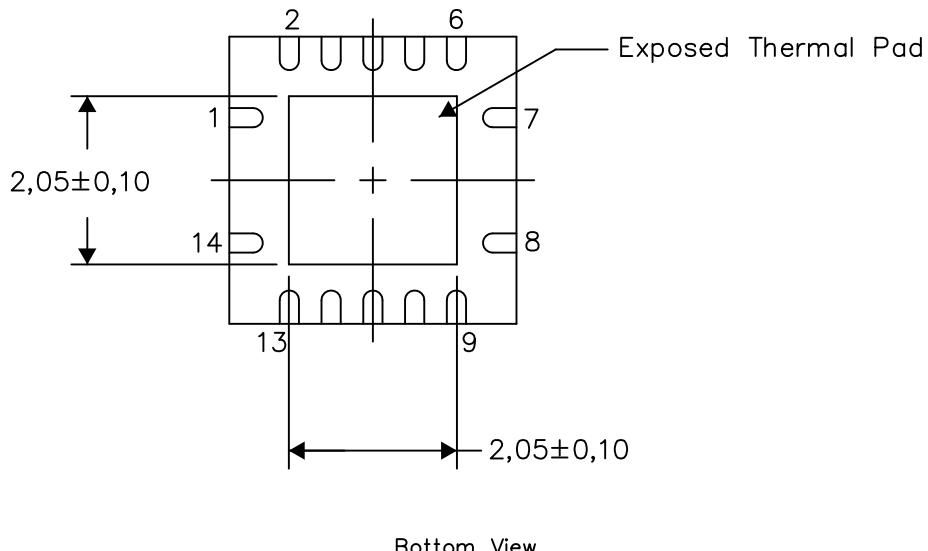
PLASTIC QUAD FLATPACK NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

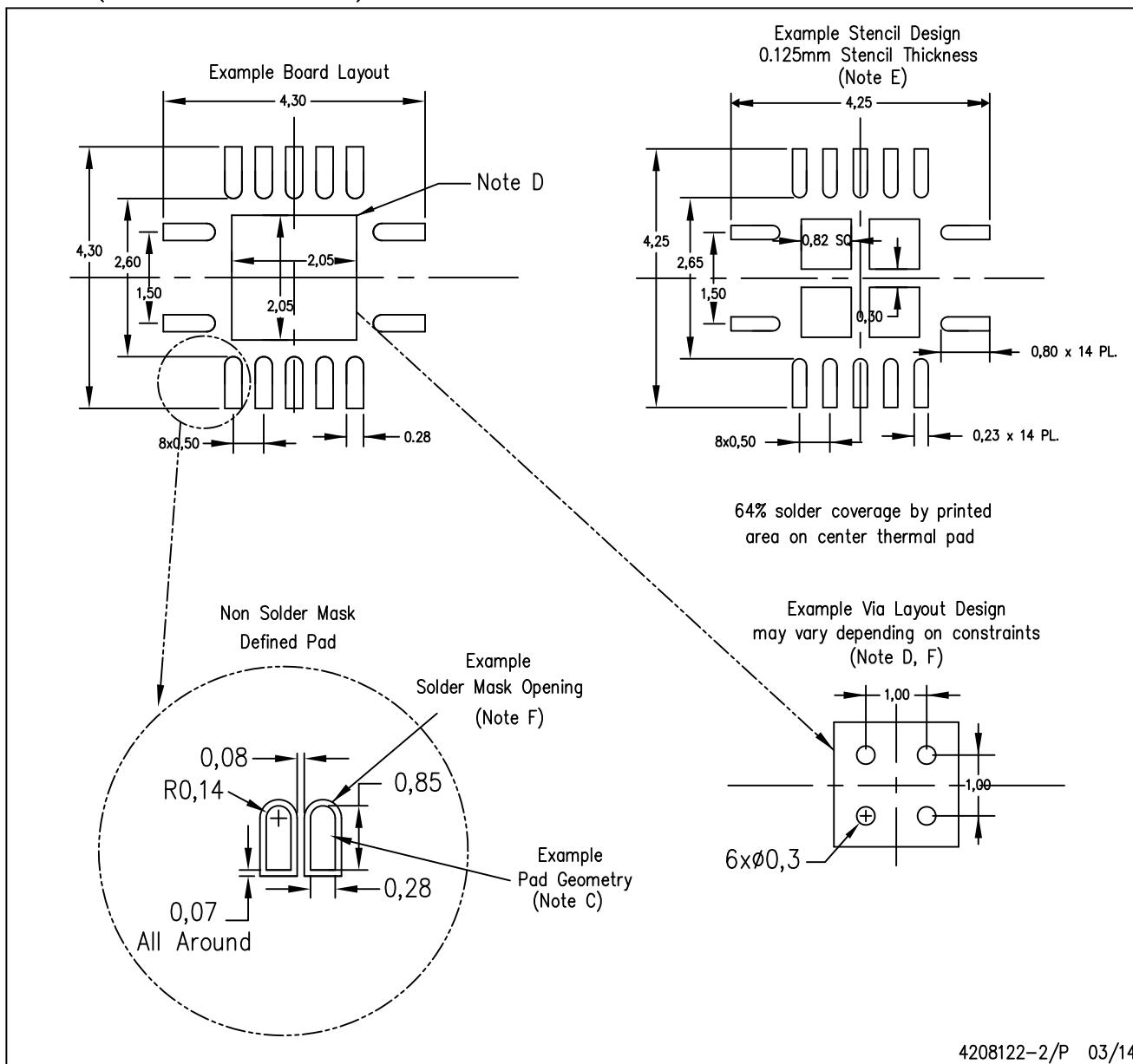
4206353-2/P 03/14

NOTE: All linear dimensions are in millimeters

LAND PATTERN DATA

RGY (S-PVQFN-N14)

PLASTIC QUAD FLATPACK NO-LEAD



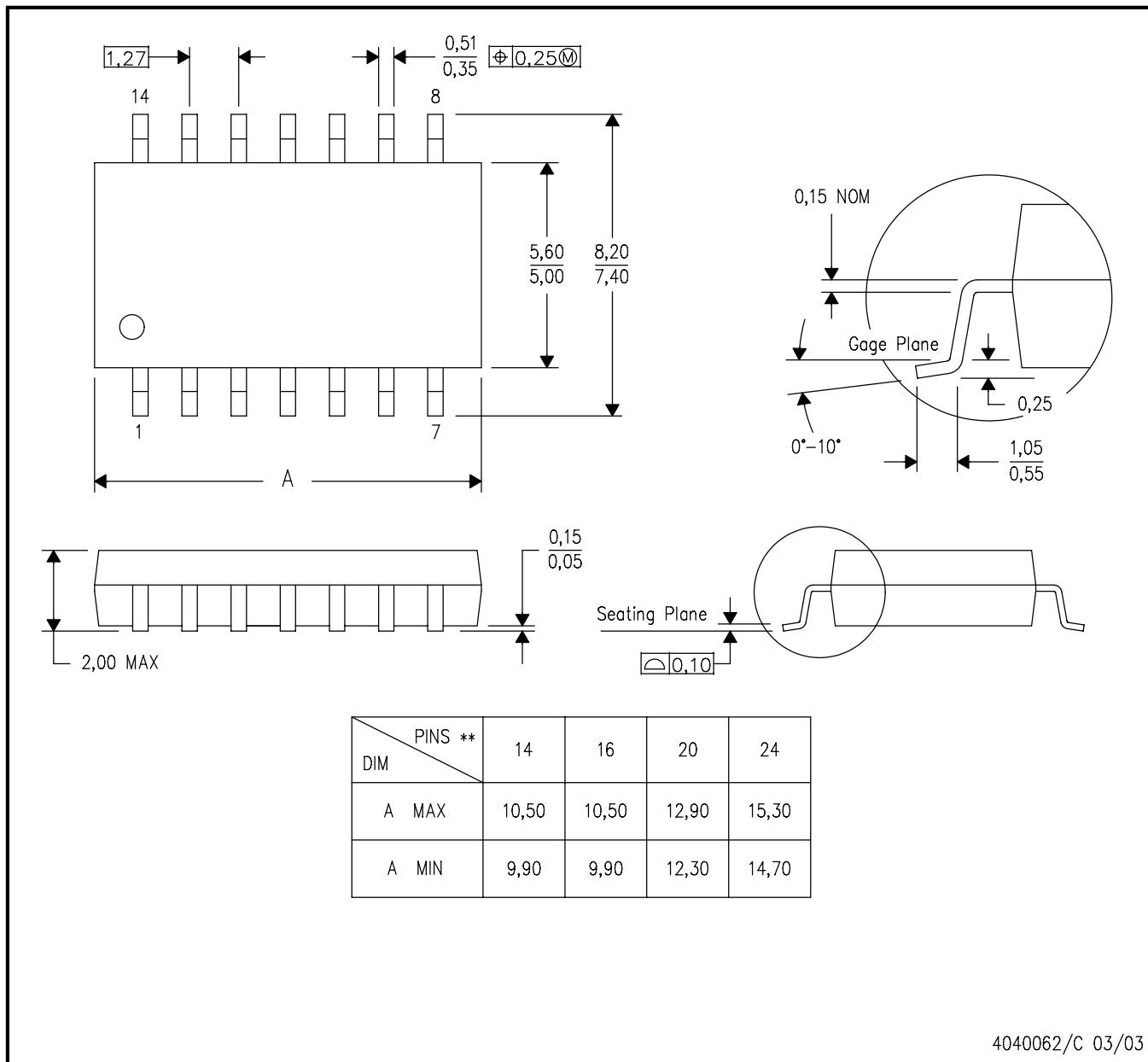
- NOTES:**
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat-Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
 - Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

MECHANICAL DATA

NS (R-PDSO-G)**

14-PINS SHOWN

PLASTIC SMALL-OUTLINE PACKAGE



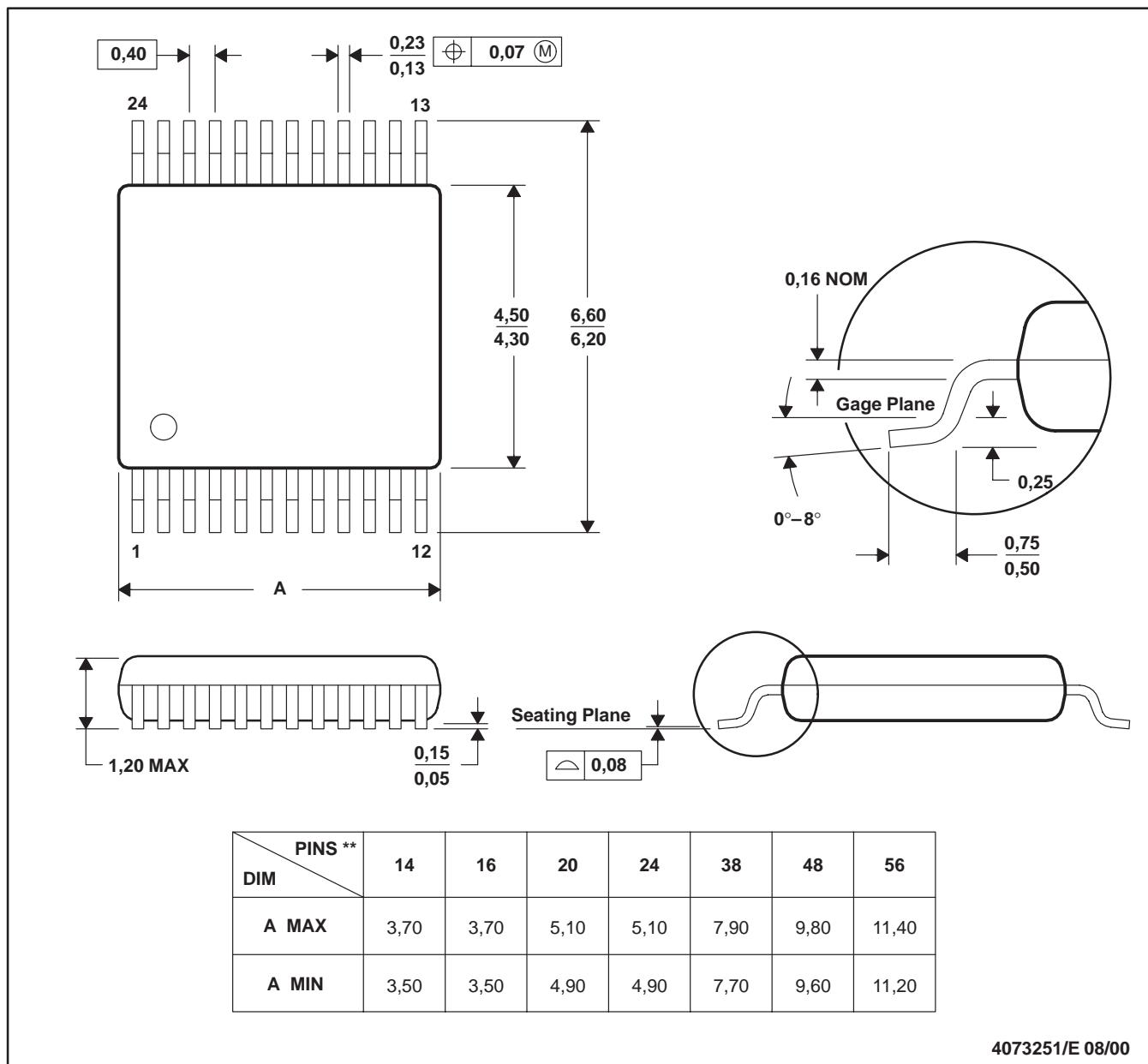
4040062/C 03/03

- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

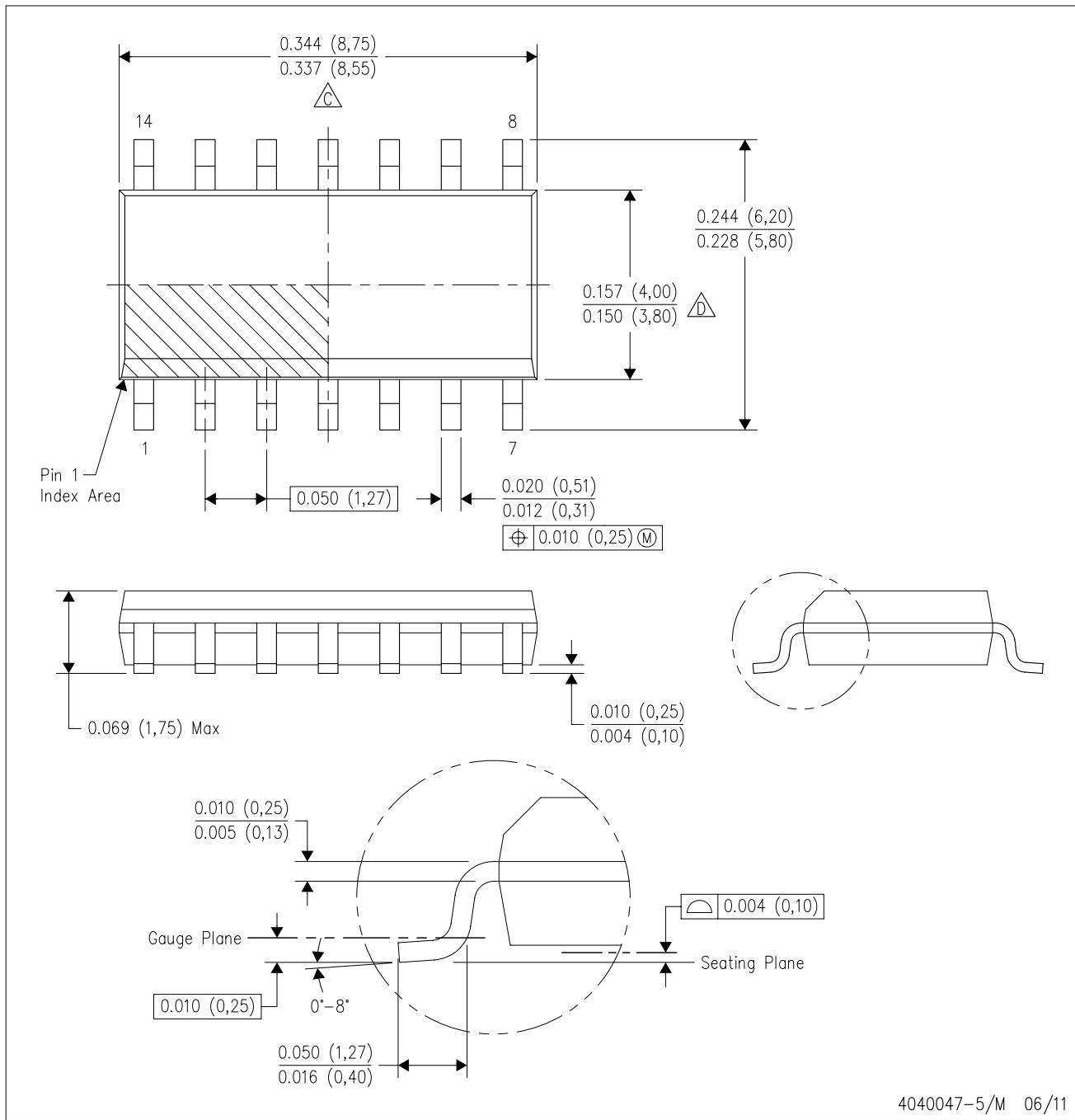
24 PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0.15 per side.
 - D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



NOTES: A. All linear dimensions are in inches (millimeters).

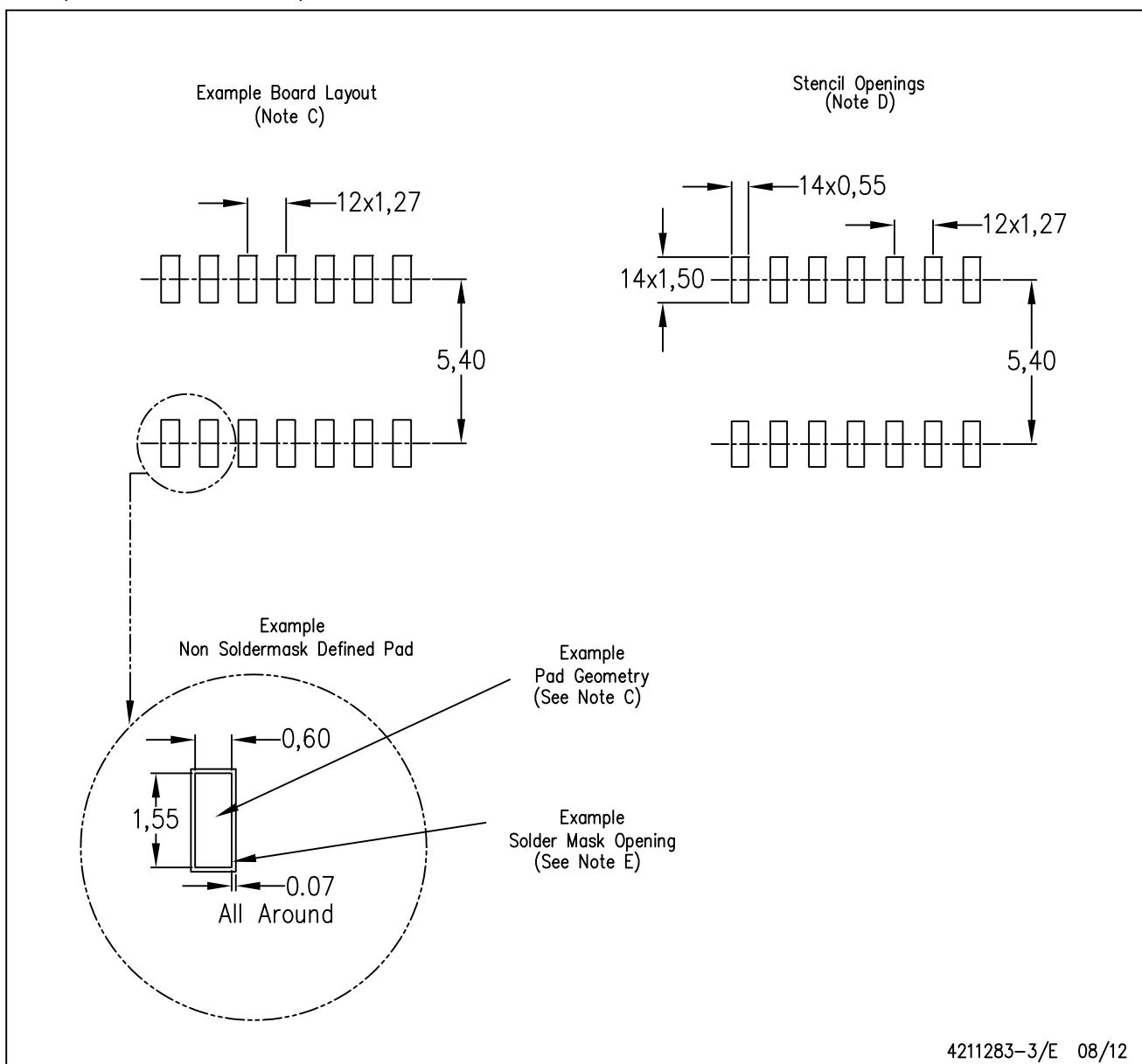
B. This drawing is subject to change without notice.

C Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.

D Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



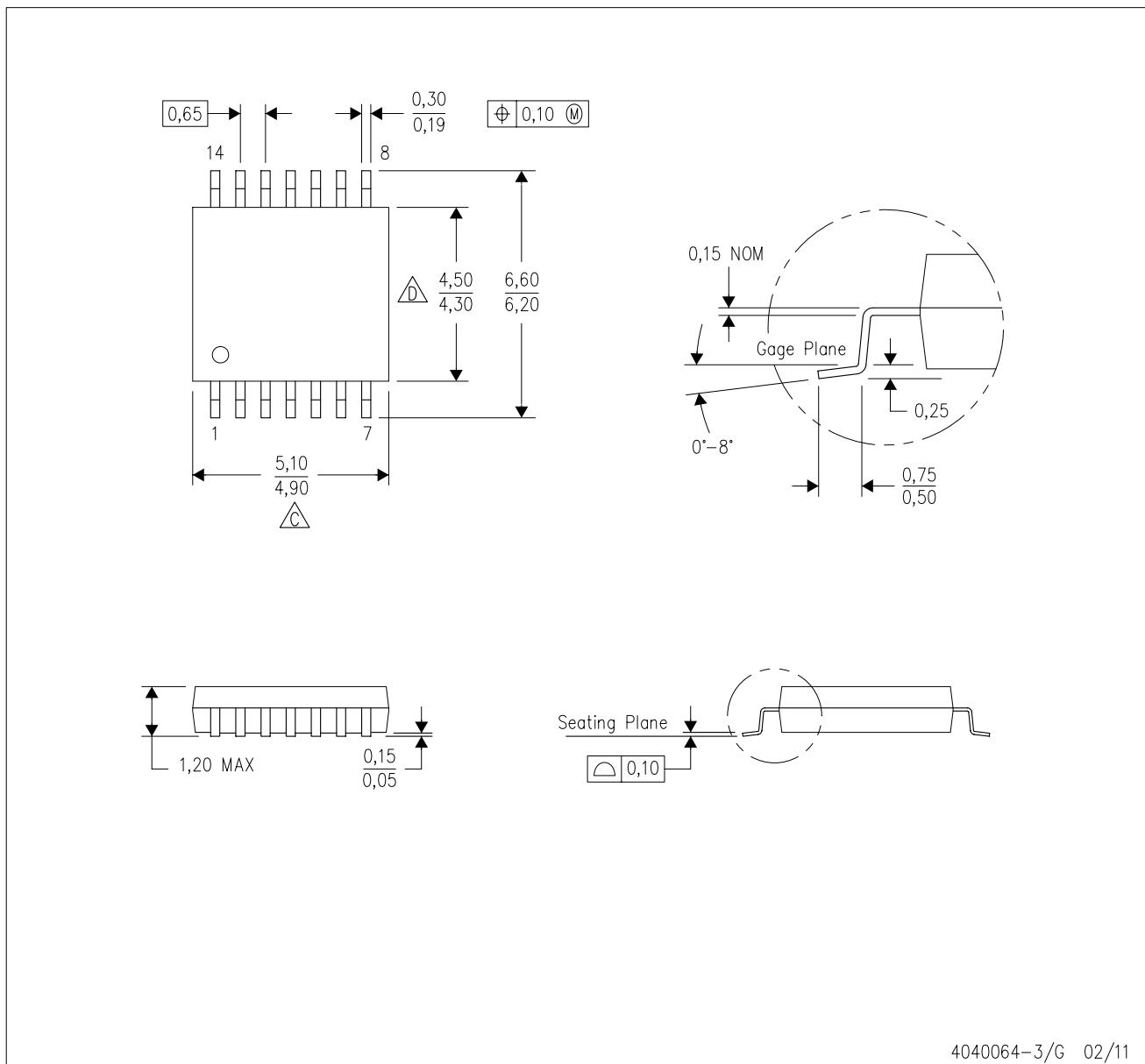
4211283-3/E 08/12

- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

MECHANICAL DATA

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.

B. This drawing is subject to change without notice.

C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.

D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.

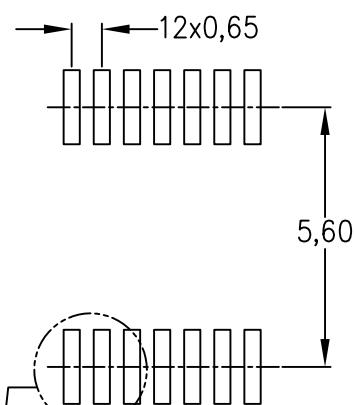
E. Falls within JEDEC MO-153

LAND PATTERN DATA

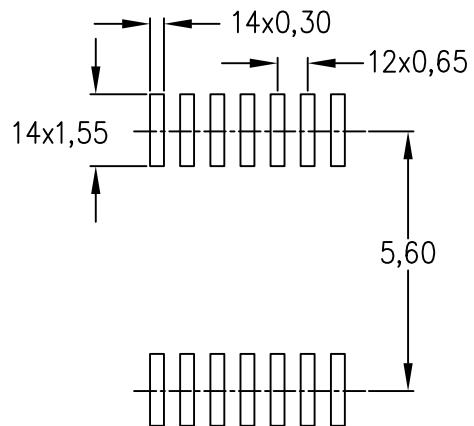
PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

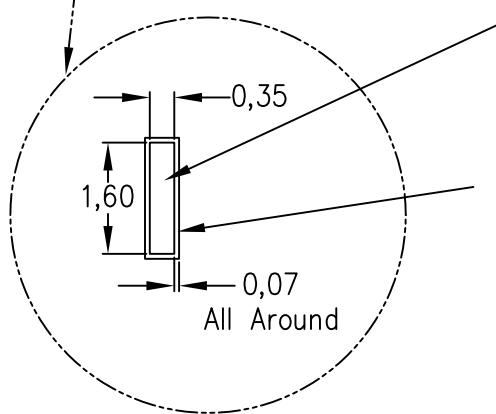
Example Board Layout
(Note C)



Stencil Openings
(Note D)



Example
Non Soldermask Defined Pad



Example
Pad Geometry
(See Note C)

Example
Solder Mask Opening
(See Note E)

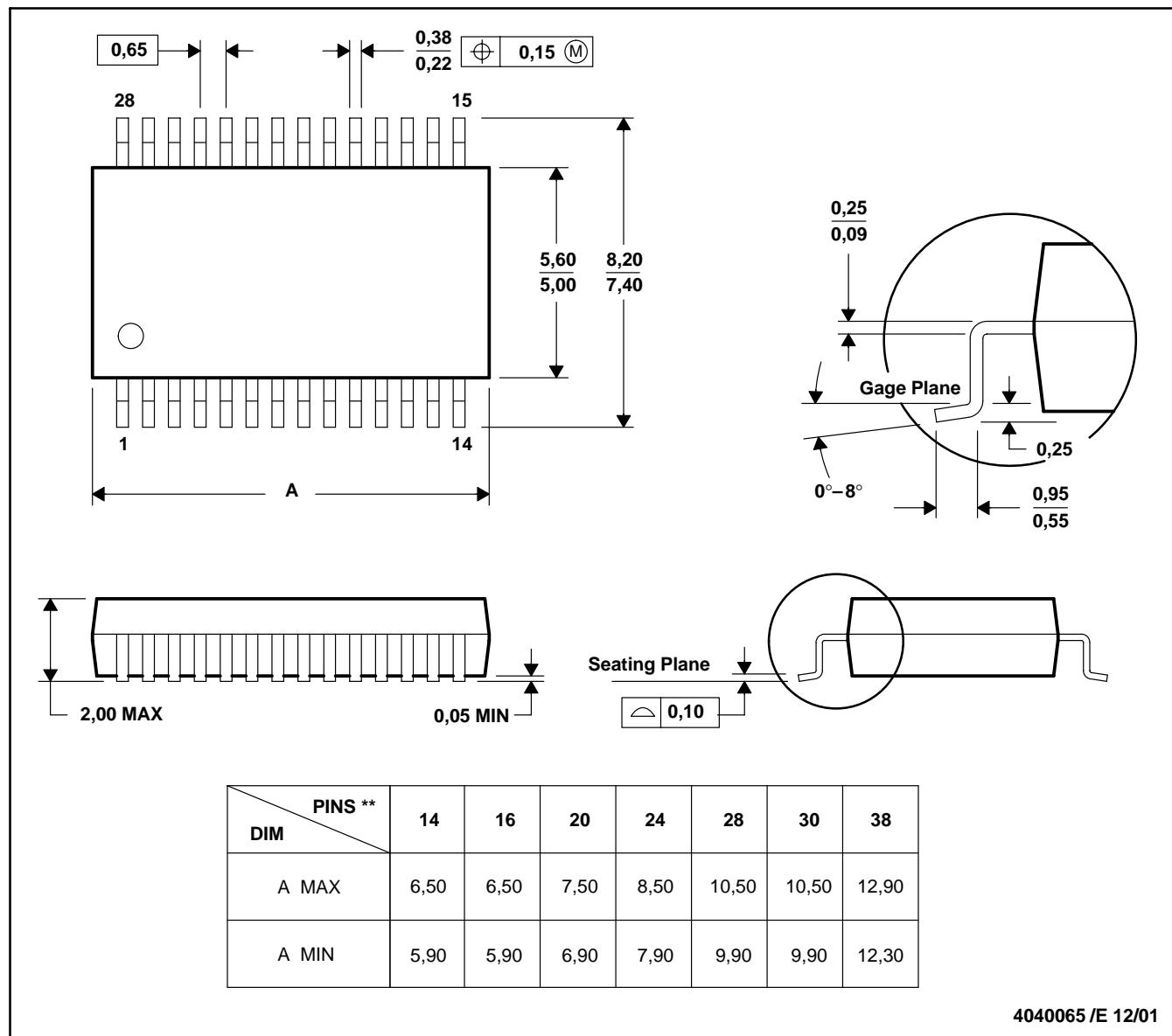
4211284-2/G 08/15

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - D. Falls within JEDEC MO-150

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ICL7135C, TLC7135C
4 1/2-DIGIT PRECISION
ANALOG-TO-DIGITAL CONVERTERS

SLAS074D – DECEMBER 1986 – REVISED SEPTEMBER 2003

- Zero Reading for 0-V Input
- Precision Null Detection With True Polarity at Zero
- 1-pA Typical Input Current
- True Differential Input
- Multiplexed Binary-Coded-Decimal (BCD) Output
- Low Rollover Error: ± 1 Count Max
- Control Signals Allow Interfacing With UARTs or Microprocessors
- Autoranging Capability With Over-and Under-Range Signals
- TTL-Compatible Outputs
- Second Source to Teledyne TSC7135, Intersil ICL7135, Maxim ICL7135, and Siliconix Si7135
- CMOS Technology

**DW OR N PACKAGE
(TOP VIEW)**

V _{CC} -	1	28	UNDER RANGE
REF	2	27	OVER RANGE
ANLG COMMON	3	26	STROBE
INT OUT	4	25	RUN/HOLD
AUTO ZERO	5	24	DGTL GND
BUFF OUT	6	23	POLARITY
C _{ref} -	7	22	CLK
C _{ref} +	8	21	BUSY
IN-	9	20	D1
IN+	10	19	D2
V _{CC} +	11	18	D3
D5	12	17	D4
B1	13	16	B8
B2	14	15	B4

DESCRIPTION

The ICL7135C and TLC7135C converters are manufactured with Texas Instruments highly efficient CMOS technology. These 4 1/2-digit, dual-slope-integrating, analog-to-digital converters (ADCs) are designed to provide interfaces to both a microprocessor and a visual display. The digit-drive outputs D1 through D4 and multiplexed binary-coded-decimal outputs B1, B2, B4, and B8 provide an interface for LED or LCD decoder/drivers as well as microprocessors.

The ICL7135C and TLC7135C offer 50-ppm (one part in 20,000) resolution with a maximum linearity error of one count. The zero error is less than 10 μ V and zero drift is less than 0.5 μ V/ $^{\circ}$ C. Source-impedance errors are minimized by low input current (less than 10 pA). Rollover error is limited to ± 1 count.

The BUSY, STROBE, RUN/HOLD, OVER RANGE, and UNDER RANGE control signals support microprocessor-based measurement systems. The control signals also can support remote data acquisition systems with data transfer through universal asynchronous receiver transmitters (UARTs).

The ICL7135C and TLC7135C are characterized for operation from 0 $^{\circ}$ C to 70 $^{\circ}$ C.

AVAILABLE OPTIONS

TA	PACKAGE	
	PLASTIC DIP (N)	SMALL OUTLINE (DW)
0°C to 70°C	ICL7135CN	
	TLC7135CN	TLC7135CDW



Caution. These devices have limited built-in protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

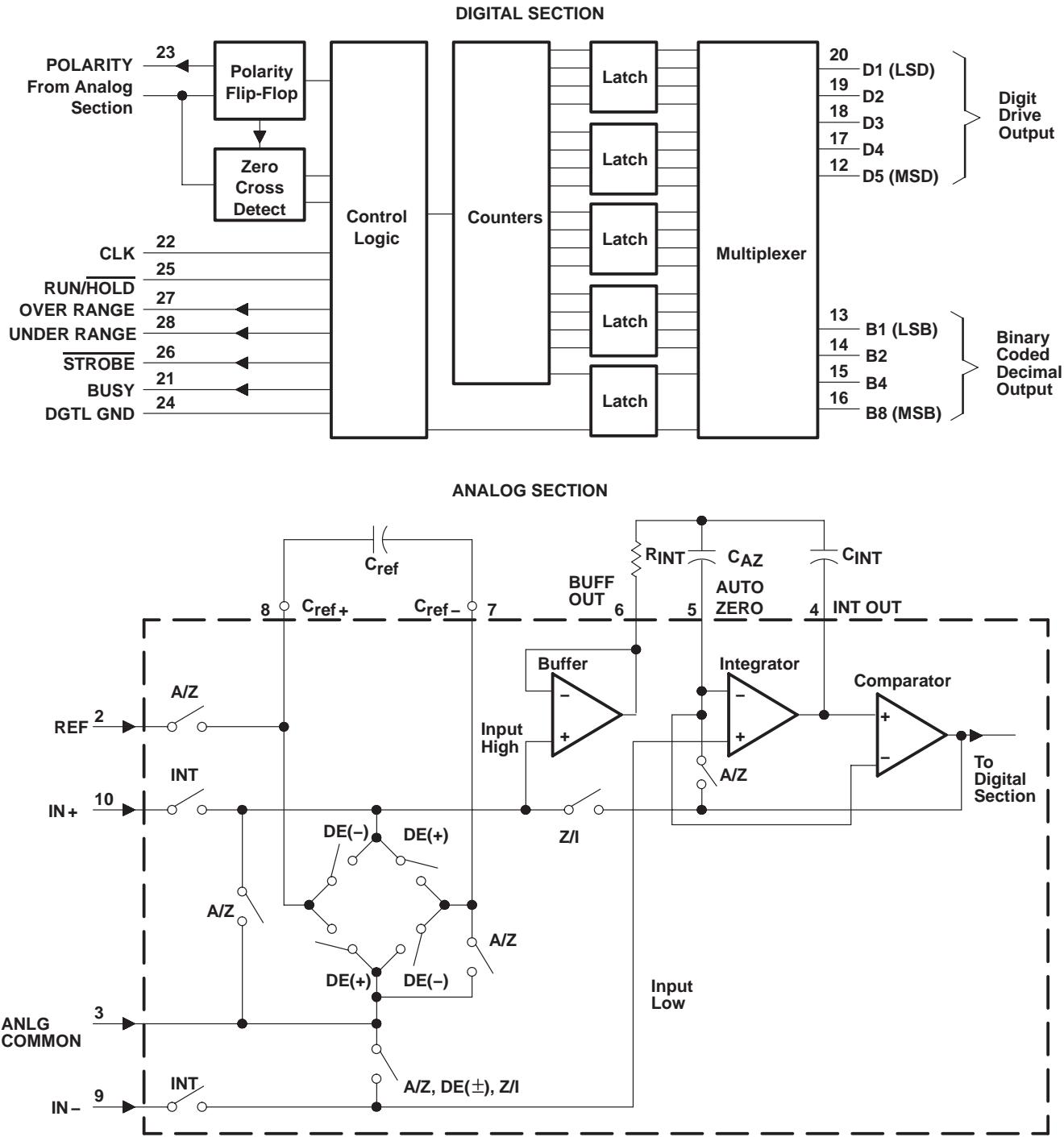


Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ICL7135C, TLC7135C
4 1/2-DIGIT PRECISION
ANALOG-TO-DIGITAL CONVERTERS

SLAS074D – DECEMBER 1986 – REVISED SEPTEMBER 2003

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	UNIT
Supply voltage (V_{CC+} with respect to V_{CC-})	15 V
Analog input voltage (IN– or IN+)	V_{CC-} to V_{CC+}
Reference voltage range	V_{CC-} to V_{CC+}
Clock input voltage range	0 V to V_{CC+}
Operating free-air temperature range, T_A	0°C to 70°C
Storage temperature range, T_{Stg}	−65°C to 150°C
Lead temperature 1.6 mm (1/16 inch) from case for 10 seconds: N package	260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage, V_{CC+}	4	5	6	V
Supply voltage, V_{CC-}	−3	−5	−8	V
Reference voltage, V_{ref}		1		V
High-level input voltage, CLK, RUN/HOLD, V_{IH}		2.8		V
Low-level input voltage, CLK, RUN/HOLD, V_{IL}		0.8		V
Differential input voltage, V_{ID}	$V_{CC-} + 1$	$V_{CC+} - 0.5$		V
Maximum operating frequency, f_{clock} (see Note 1)	1.2	2		MHz
Operating free-air temperature range, T_A	0	70		°C

NOTE 1: Clock frequency range extends down to 0 Hz.

ELECTRICAL CHARACTERISTICS

$V_{CC+} = 5$ V, $V_{CC-} = 5$ V, $V_{ref} = 1$ V, $f_{clock} = 120$ kHz, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OH}	D1-D5, B1, B2, B4, B8	$I_O = -1$ mA	2.4	5		V
	Other outputs	$I_O = -10$ μ A	4.9	5		
V_{OL} Low-level output voltage		$I_O = 1.6$ mA		0.4		V
$V_{ON(PP)}$ Peak-to-peak output noise voltage (see Note 1)		$V_{ID} = 0$, Full scale = 2 V		15		μ V
α_{VO} Zero-reading temperature coefficient of output voltage		$V_{ID} = 0$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	0.5	2		μ V/°C
I_{IH} High-level input current		$V_I = 5$ V, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	0.1	10		μ A
I_{IL} Low-level input current		$V_I = 0$ V, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	−0.02	−0.1		mA
I_I Input leakage current, IN– and IN+		$V_{ID} = 0$	TA = 25°C	1	10	pA
			0°C ≤ TA ≤ 70°C		250	
I_{CC+} Positive supply current		$f_{clock} = 0$	TA = 25°C	1	2	mA
			0°C ≤ TA ≤ 70°C		3	
I_{CC-} Negative supply current		$f_{clock} = 0$	TA = 25°C	−0.8	−2	mA
			0°C ≤ TA ≤ 70°C		−3	
C_{pd} Power dissipation capacitance		See Note 2		40		pF

NOTES: 1. This is the peak-to-peak value that is not exceeded 95% of the time.

2. Factor-relating clock frequency to increase in supply current. At $V_{CC+} = 5$ V, $I_{CC+} = I_{CC+}(f_{clock} = 0) + C_{pd} \times 5 \text{ V} \times f_{clock}$

ICL7135C, TLC7135C
4 1/2-DIGIT PRECISION
ANALOG-TO-DIGITAL CONVERTERS

SLAS074D – DECEMBER 1986 – REVISED SEPTEMBER 2003

OPERATING CHARACTERISTICS

$V_{CC+} = 5 \text{ V}$, $V_{CC-} = 5 \text{ V}$, $V_{ref} = 1 \text{ V}$, $f_{clock} = 120 \text{ kHz}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted)

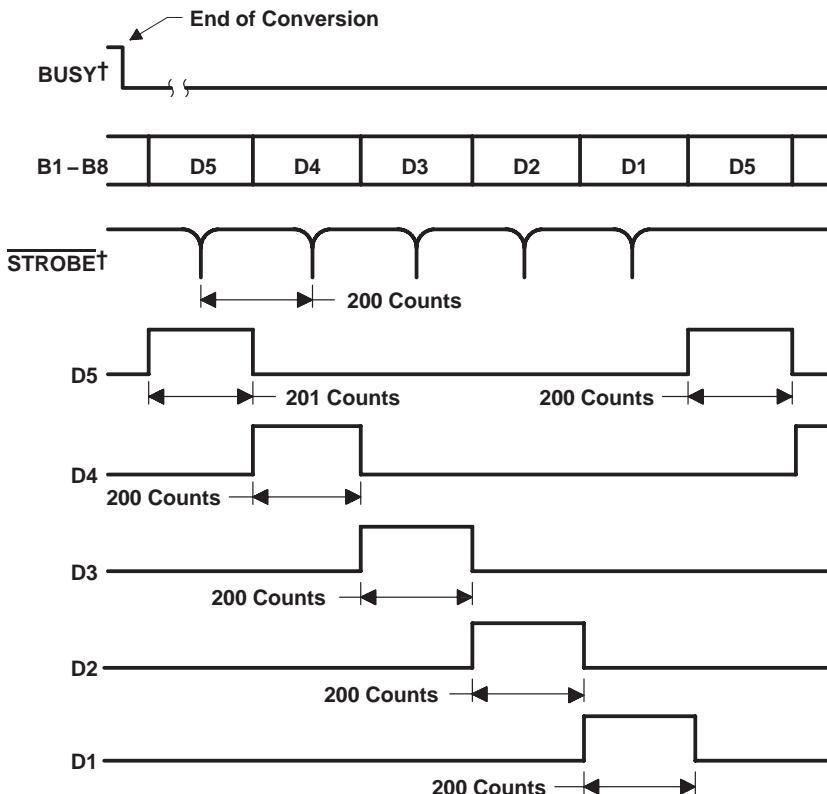
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
α_{FS} Full-scale temperature coefficient (see Note 1)	$V_{ID} = 2 \text{ V}$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$		5		ppm/ $^\circ\text{C}$
E_L Linearity error	$-2 \text{ V} \leq V_{ID} \leq 2 \text{ V}$		0.5		count
E_D Differential linearity error (see Note 2)	$-2 \text{ V} \leq V_{ID} \leq 2 \text{ V}$		0.01		LSB
E_{FS} \pm Full-scale symmetry error (rollover error) (see Note 3)	$V_{ID} = \pm 2 \text{ V}$		0.5	1	count
Display reading with 0-V input	$V_{ID} = 0$, $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	-0.0000	± 0.0000	0.0000	Digital Reading
Display reading in ratiometric operation	$V_{ID} = V_{ref}$, $T_A = 25^\circ\text{C}$ $0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$	0.9998 0.9995	0.9999 0.9999	1.0000 1.0005	Digital Reading

NOTES: 1. This parameter is measured with an external reference having a temperature coefficient of less than 0.01 ppm/ $^\circ\text{C}$.

2. The magnitude of the difference between the worst case step of adjacent counts and the ideal step.

3. Rollover error is the difference between the absolute values of the conversion for 2 V and -2 V.

TIMING DIAGRAMS



† Delay between BUSY going low and the first **STROBE** pulse is dependent upon the analog input.

Figure 1

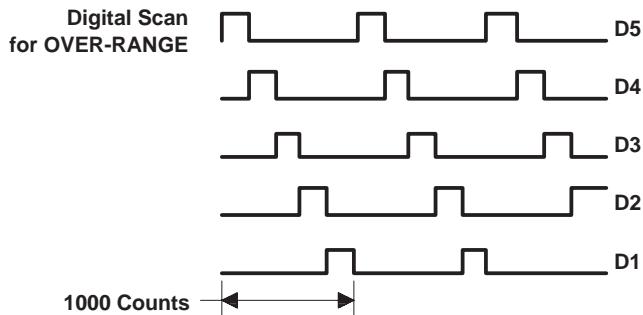


Figure 2

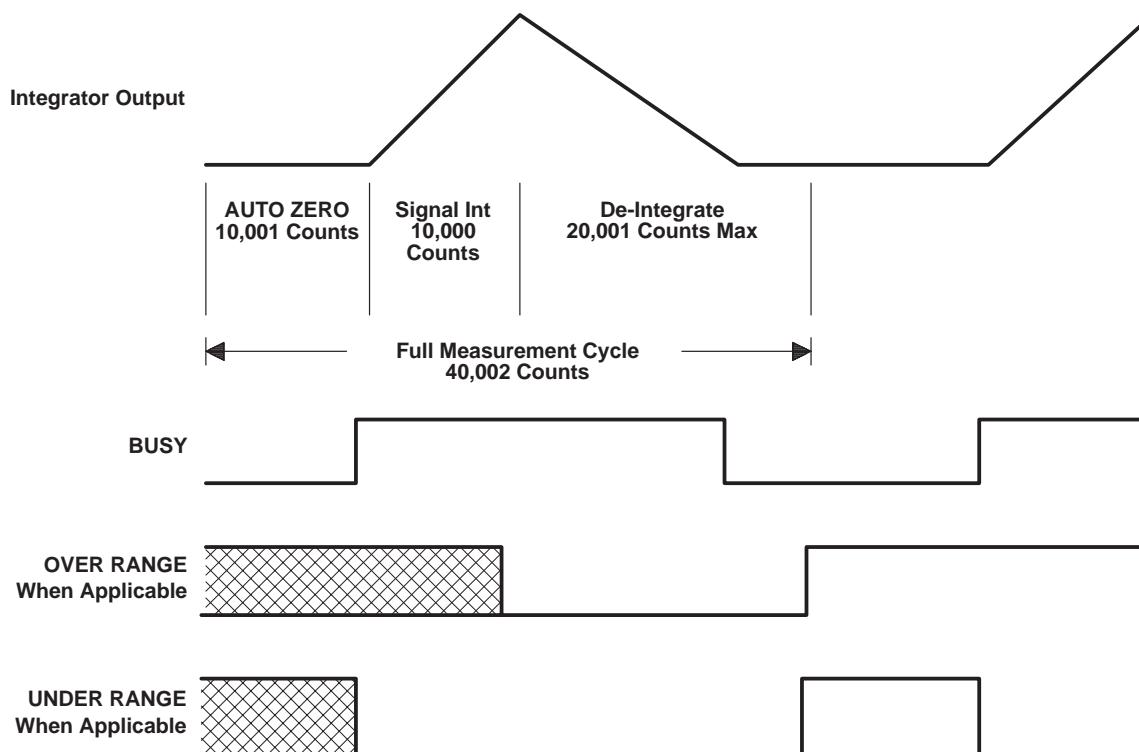
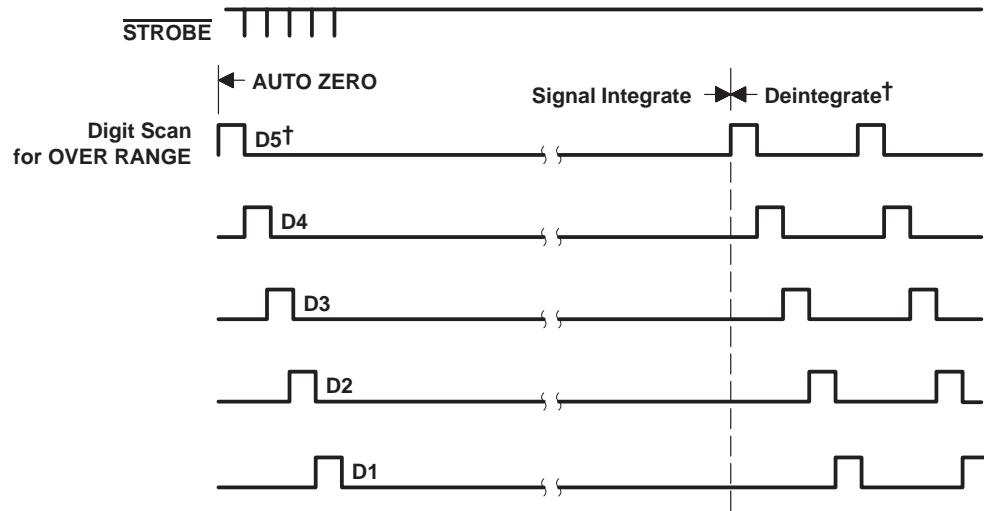


Figure 3

ICL7135C, TLC7135C 4 1/2-DIGIT PRECISION ANALOG-TO-DIGITAL CONVERTERS

SLAS074D – DECEMBER 1986 – REVISED SEPTEMBER 2003



† First D5 of AUTO ZERO and deintegrate is one count longer.

Figure 4

PRINCIPLES OF OPERATION

A measurement cycle for the ICL7135C and TLC7135C consists of the following four phases.

1. Auto-Zero Phase. The internal IN+ and IN– inputs are disconnected from the terminals and internally connected to ANLG COMMON. The reference capacitor is charged to the reference voltage. The system is configured in a closed loop and the auto-zero capacitor is charged to compensate for offset voltages in the buffer amplifier, integrator, and comparator. The auto-zero accuracy is limited only by the system noise, and the overall offset, as referred to the input, is less than 10 μ V.
2. Signal Integrate Phase. The auto-zero loop is opened and the internal IN+ and IN– inputs are connected to the external terminals. The differential voltage between these inputs is integrated for a fixed period of time. When the input signal has no return with respect to the converter power supply, IN– can be tied to ANLG COMMON to establish the correct common-mode voltage. Upon completion of this phase, the polarity of the input signal is recorded.
3. Deintegrate Phase. The reference is used to perform the deintegrate task. The internal IN– is internally connected to ANLG COMMON and IN+ is connected across the previously charged reference capacitor. The recorded polarity of the input signal ensures that the capacitor is connected with the correct polarity so that the integrator output polarity returns to zero. The time required for the output to return to zero is proportional to the amplitude of the input signal. The return time is displayed as a digital reading and is determined by the equation $10,000 \times (V_{ID}/V_{ref})$. The maximum or full-scale conversion occurs when V_{ID} is two times V_{ref} .
4. Zero Integrator Phase. The internal IN– is connected to ANLG COMMON. The system is configured in a closed loop to cause the integrator output to return to zero. Typically, this phase requires 100 to 200 clock pulses. However, after an over-range conversion, 6200 pulses are required.

DESCRIPTION OF ANALOG CIRCUITS

Input Signal Range

The common mode range of the input amplifier extends from 1 V above the negative supply to 1 V below the positive supply. Within this range, the common-mode rejection ratio (CMRR) is typically 86 dB. Both differential and common-mode voltages cause the integrator output to swing. Therefore, care must be exercised to ensure that the integrator output does not become saturated.

Analog Common

Analog common (ANLG COMMON) is connected to the internal IN– during the auto-zero, deintegrate, and zero integrator phases. When IN– is connected to a voltage that is different from analog common during the signal integrate phase, the resulting common-mode voltage is rejected by the amplifier. However, in most applications, IN– is set at a known fixed voltage (i.e., power supply common for instance). In this application, analog common should be tied to the same point, thus removing the common-mode voltage from the converter. Removing the common-mode voltage in this manner slightly increases conversion accuracy.

Reference

The reference voltage is positive with respect to analog common. The accuracy of the conversion result is dependent upon the quality of the reference. Therefore, to obtain a high accuracy conversion, a high quality reference should be used.

DESCRIPTION OF DIGITAL CIRCUITS

RUN/HOLD Input

When RUN/HOLD is high or open, the device continuously performs measurement cycles every 40,002 clock pulses. When this input is taken low, the integrated circuit continues to perform the ongoing measurement cycle and then hold the conversion reading for as long as the terminal is held low. When the terminal is held low after completion of a measurement cycle, a short positive pulse (greater than 300 ns) initiates a new measurement cycle. When this positive pulse occurs before the completion of a measurement cycle, it will not be recognized. The first STROBE pulse, which occurs 101 counts after the end of a measurement cycle, is an indication of the completion of a measurement cycle. Thus, the positive pulse could be used to trigger the start of a new measurement after the first STROBE pulse.

STROBE Input

Negative going pulses from this input transfer the BCD conversion data to external latches, UARTs, or microprocessors. At the end of the measurement cycle, STROBE goes high and remains high for 201 counts. The most significant digit (MSD) BCD bits are placed on the BCD terminals. After the first 101 counts, halfway through the duration of output D1–D5 going high, the STROBE terminal goes low for 1/2 clock pulse width. The placement of the STROBE pulse at the midpoint of the D5 high pulse allows the information to be latched into an external device on either a low-level or an edge. Such placement of the STROBE pulse also ensures that the BCD bits for the second MSD are not yet competing for the BCD lines and latching of the correct bits is ensured. The above process is repeated for the second MSD and the D4 output. Similarly, the process is repeated through the least significant digit (LSD). Subsequently, inputs D5 through D1 and the BCD lines continue scanning without the inclusion of STROBE pulses. This subsequent continuous scanning causes the conversion results to be continuously displayed. Such subsequent scanning does not occur when an over-range condition occurs.

ICL7135C, TLC7135C 4 1/2-DIGIT PRECISION ANALOG-TO-DIGITAL CONVERTERS

SLAS074D – DECEMBER 1986 – REVISED SEPTEMBER 2003

BUSY Output

The BUSY output goes high at the beginning of the signal integrate phase. BUSY remains high until the first clock pulse after zero crossing or at the end of the measurement cycle when an over-range condition occurs. It is possible to use the BUSY terminal to serially transmit the conversion result. Serial transmission can be accomplished by ANDing the BUSY and CLOCK signals and transmitting the ANDed output. The transmitted output consists of 10,001 clock pulses, which occur during the signal integrate phase, and the number of clock pulses that occur during the deintegrate phase. The conversion result can be obtained by subtracting 10,001 from the total number of clock pulses.

OVER-RANGE Output

When an over-range condition occurs, this terminal goes high after the BUSY signal goes low at the end of the measurement cycle. As previously noted, the BUSY signal remains high until the end of the measurement cycle when an over-range condition occurs. The OVER RANGE output goes high at the end of BUSY and goes low at the beginning of the deintegrate phase in the next measurement cycle.

UNDER-RANGE Output

At the end of the BUSY signal, this terminal goes high when the conversion result is less than or equal to 9% (count of 1800) of the full-scale range. The UNDER-RANGE output is brought low at the beginning of the signal integrate phase of the next measurement cycle.

POLARITY Output

The POLARITY output is high for a positive input signal and updates at the beginning of each deintegrate phase. The polarity output is valid for all inputs including ± 0 and OVER RANGE signals.

Digit-Drive (D1, D2, D4 and D5) Outputs

Each digit-drive output (D1 through D5) sequentially goes high for 200 clock pulses. This sequential process is continuous unless an over-range occurs. When an over-range occurs, all of the digit-drive outputs are blanked from the end of the strobe sequence until the beginning of the deintegrate phase (when the sequential digit-drive activation begins again). The blanking activity during an over-range condition can cause the display to flash and indicate the over-range condition.

BCD Outputs

The BCD bits (B1, B2, B4 and B8) for a given digit are sequentially activated on these outputs. Simultaneously, the appropriate digit-drive line for the given digit is activated.

System Aspects

Integrating Resistor

The value of the integrating resistor (R_{INT}) is determined by the full-scale input voltage and the output current of the integrating amplifier. The integrating amplifier can supply 20 μA of current with negligible nonlinearity. The equation for determining the value of this resistor is:

$$R_{INT} = \frac{\text{Full Scale Voltage}}{I_{INT}}$$

Integrating amplifier current, I_{INT} , from 5 to 40 μA yields good results. However, the nominal and recommended current is 20 μA .



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Integrating Capacitor

The product of the integrating resistor and capacitor should be selected to give the maximum voltage swing without causing the integrating amplifier output to saturate and get too close to the power supply voltages. When the amplifier output is within 0.3 V of either supply, saturation occurs. With ± 5 -V supplies and ANLG COMMON connected to ground, the designer should design for a ± 3.5 -V to ± 4 -V integrating amplifier swing. A nominal capacitor value is 0.47 μF . The equation for determining the value of the integrating capacitor (C_{INT}) is:

$$C_{\text{INT}} = \frac{10,000 \times \text{Clock Period} \times I_{\text{INT}}}{\text{Integrator Output Voltage Swing}}$$

where

I_{INT} is nominally 20 μA .

Capacitors with large tolerances and high dielectric absorption can induce conversion inaccuracies. A capacitor that is too small could cause the integrating amplifier to saturate. High dielectric absorption causes the effective capacitor value to be different during the signal integrate and deintegrate phases. Polypropylene capacitors have very low dielectric absorption. Polystyrene and polycarbonate capacitors have higher dielectric absorption, but also work well.

Auto-Zero and Reference Capacitor

Large capacitors tend to reduce noise in the system. Dielectric absorption is unimportant except during power up or overload recovery. Typical values are 1 μF .

Reference Voltage

For high-accuracy absolute measurements, a high quality reference should be used.

Rollover Resistor and Diode

The ICL7135C and TLC7135C have a small rollover error; however, it can be corrected. The correction is to connect the cathode of any silicon diode to INT OUT and the anode to a resistor. The other end of the resistor is connected to ANLG COMMON or ground. For the recommended operating conditions, the resistor value is 100 $\text{k}\Omega$. This value may be changed to correct any rollover error that has not been corrected. In many noncritical applications the resistor and diode are not needed.

Maximum Clock Frequency

For most dual-slope A/D converters, the maximum conversion rate is limited by the frequency response of the comparator. In this circuit, the comparator follows the integrator ramp with a 3- μs delay. Therefore, with a 160-kHz clock frequency (6- μs period), half of the first reference integrate clock period is lost in delay. Hence, the meter reading changes from 0 to 1 with a 50- μV input, 1 to 2 with a 150- μV input, 2 to 3 with a 250- μV input, etc. This transition at midpoint is desirable; however, when the clock frequency is increased appreciably above 160 kHz, the instrument flashes 1 on noise peaks even when the input is shorted. The above transition points assume a 2-V input range is equivalent to 20,000 clock cycles.

When the input signal is always of one polarity, comparator delay need not be a limitation. Clock rates of 1 MHz are possible since nonlinearity and noise do not increase substantially with frequency. For a fixed clock frequency, the extra count or counts caused by comparator delay are a constant and can be subtracted out digitally.

For signals with both polarities, the clock frequency can be extended above 160 kHz without error by using a low value resistor in series with the integrating capacitor. This resistor causes the integrator to jump slightly towards the zero-crossing level at the beginning of the deintegrate phase, and thus compensates for the comparator delay. This series resistor should be 10 Ω to 50 Ω . This approach allows clock frequencies up to 480 kHz.

ICL7135C, TLC7135C

4 1/2-DIGIT PRECISION

ANALOG-TO-DIGITAL CONVERTERS

SLAS074D – DECEMBER 1986 – REVISED SEPTEMBER 2003

Minimum Clock Frequency

The minimum clock frequency limitations result from capacitor leakage from the auto-zero and reference capacitors. Measurement cycles as high as 10 μ s are not influenced by leakage error.

Rejection of 50-Hz or 60-Hz Pickup

To maximize the rejection of 50-Hz or 60-Hz pickup, the clock frequency should be chosen so that an integral multiple of 50-Hz or 60-Hz periods occur during the signal integrate phase. To achieve rejection of these signals, some clock frequencies that can be used are:

50 Hz: 250, 166.66, 125, 100 kHz, etc.

60 Hz: 300, 200, 150, 120, 100, 40, 33.33 kHz, etc.

Zero-Crossing Flip-Flop

This flip-flop interrogates the comparator's zero-crossing status. The interrogation is performed after the previous clock cycle and the positive half of the ongoing clock cycle has occurred, so any comparator transients that result from the clock pulses do not affect the detection of a zero-crossing. This procedure delays the zero-crossing detection by one clock cycle. To eliminate the inaccuracy, which is caused by this delay, the counter is disabled for one clock cycle at the beginning of the deintegrate phase. Therefore, when the zero-crossing is detected one clock cycle later than the zero-crossing actually occurs, the correct number of counts is displayed.

Noise

The peak-to-peak noise around zero is approximately 15 μ V (peak-to-peak value not exceeded 95% of the time). Near full scale, this value increases to approximately 30 μ V. Much of the noise originates in the auto-zero loop, and is proportional to the ratio of the input signal to the reference.

Analog and Digital Grounds

For high-accuracy applications, ground loops must be avoided. Return currents from digital circuits must not be sent to the analog ground line.

Power Supplies

The ICL7135C and TLC7135C are designed to work with ± 5 -V power supplies. However, 5-V operation is possible when the input signal does not vary more than ± 1.5 V from midsupply.



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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLC7135CDW	ACTIVE	SOIC	DW	28	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	TLC7135C	Samples
TLC7135CDWR	ACTIVE	SOIC	DW	28	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM		TLC7135C	Samples
TLC7135CDWRG4	ACTIVE	SOIC	DW	28	1000	TBD	Call TI	Call TI			Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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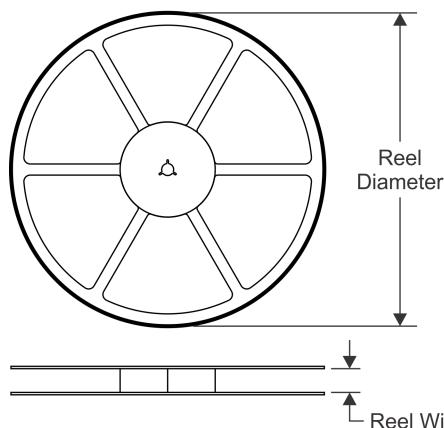
PACKAGE OPTION ADDENDUM

13-Jul-2022

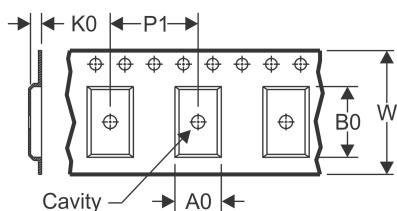
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

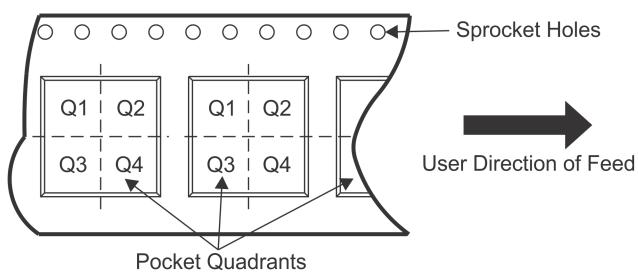


TAPE DIMENSIONS



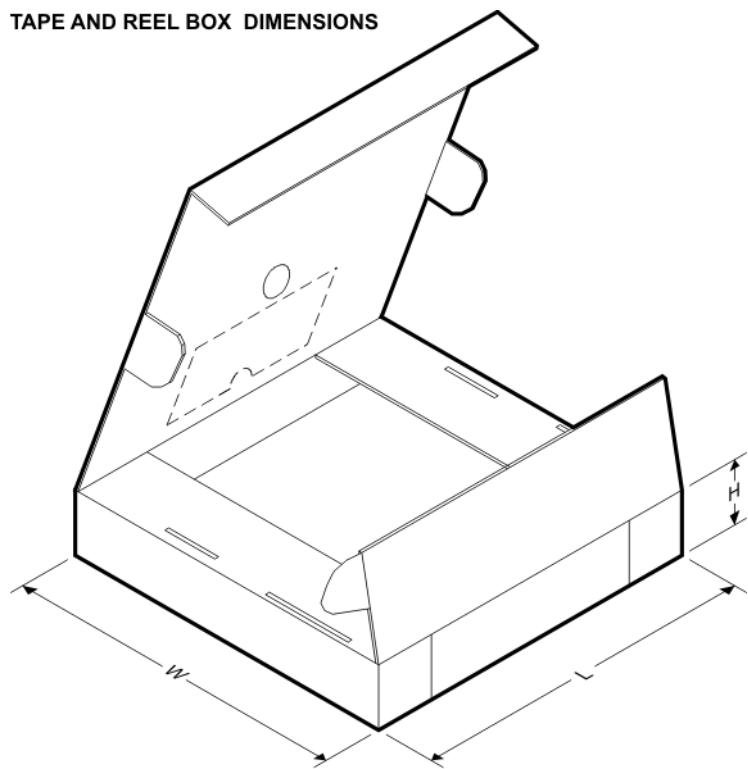
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



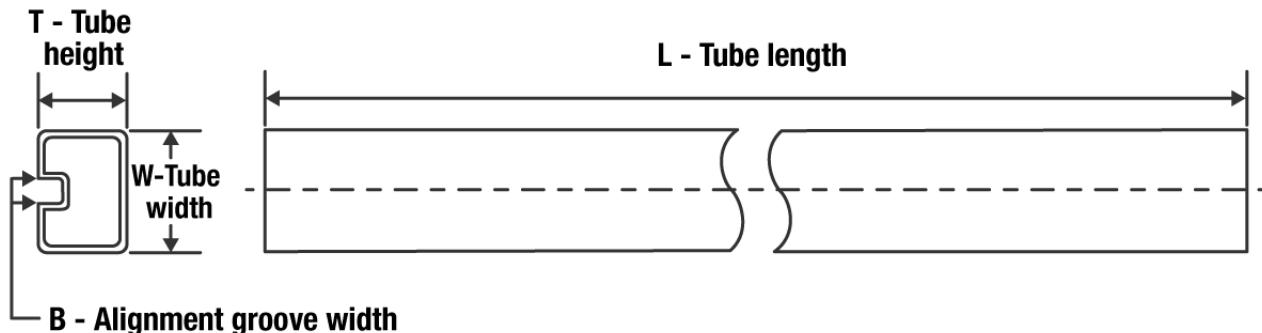
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLC7135CDWR	SOIC	DW	28	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLC7135CDWR	SOIC	DW	28	1000	350.0	350.0	66.0

TUBE

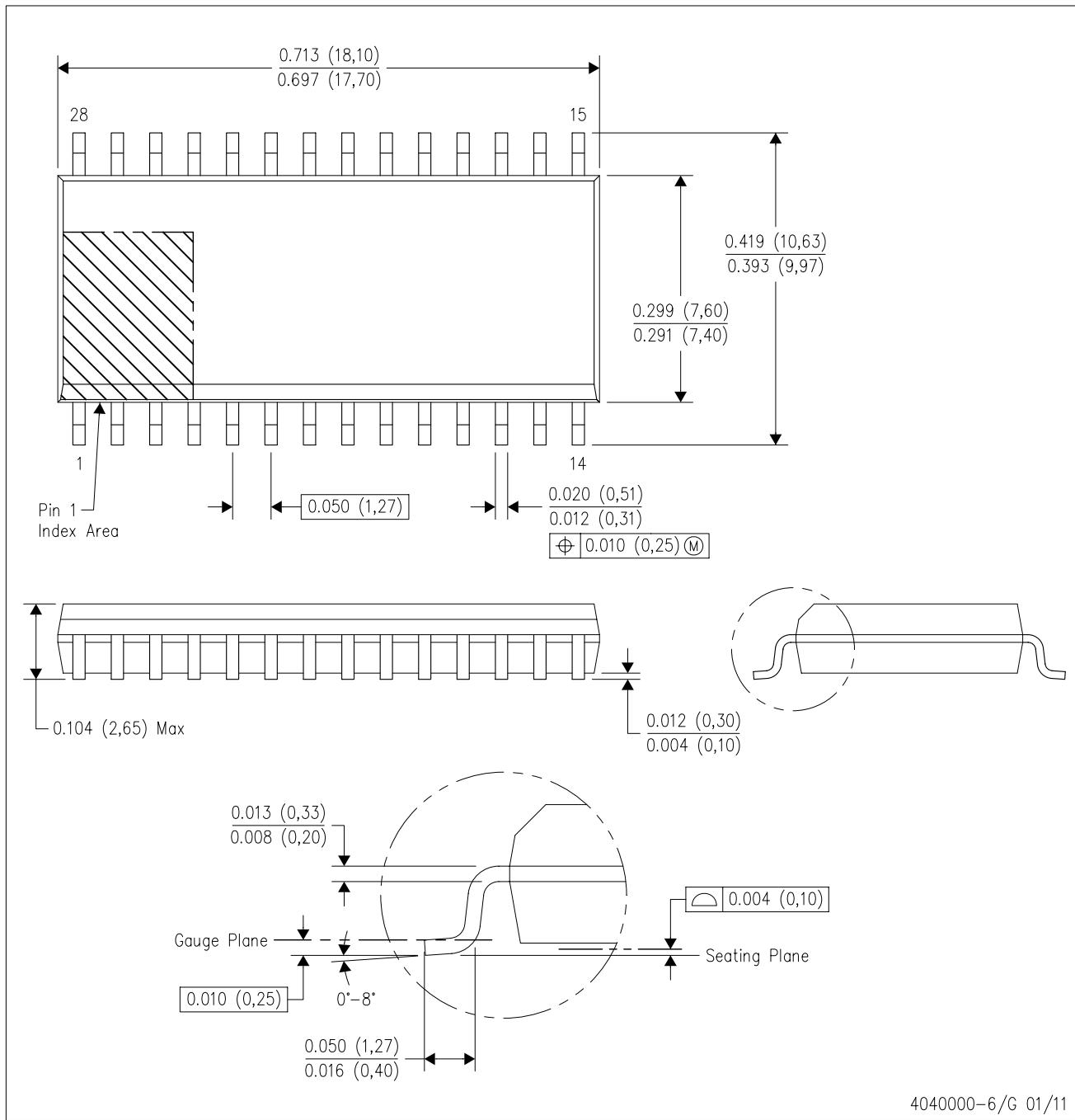
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μ m)	B (mm)
TLC7135CDW	DW	SOIC	28	20	506.98	12.7	4826	6.6

MECHANICAL DATA

DW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



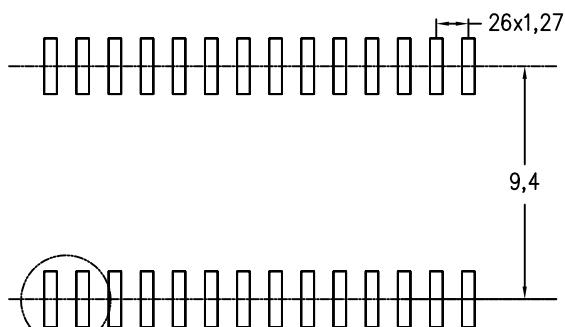
- NOTES:
- A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - D. Falls within JEDEC MS-013 variation AE.

LAND PATTERN DATA

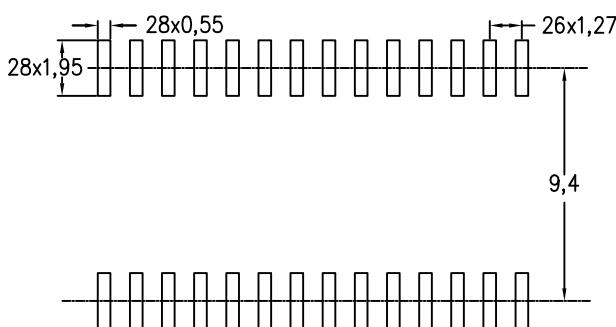
DW (R-PDSO-G28)

PLASTIC SMALL OUTLINE

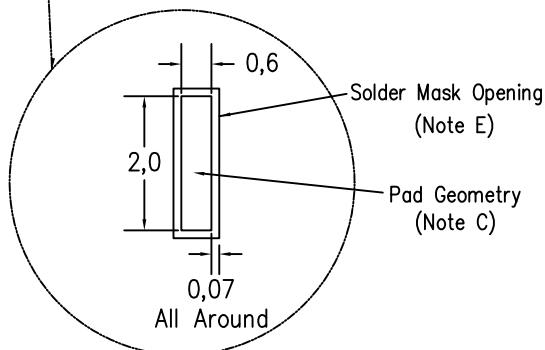
Example Board Layout
(Note C)



Stencil Openings
(Note D)



Non Solder Mask Define Pad



4209202-6/F 08/13

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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DAC0808

DAC0808 8-Bit D/A Converter



Literature Number: SNAS539A

DAC0808 8-Bit D/A Converter

General Description

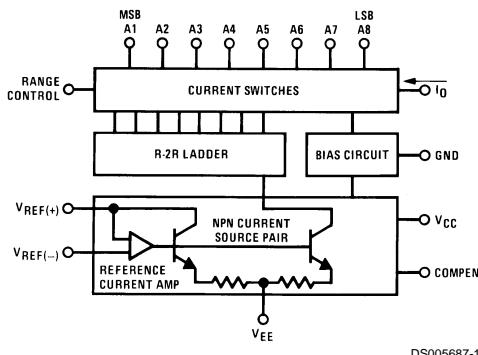
The DAC0808 is an 8-bit monolithic digital-to-analog converter (DAC) featuring a full scale output current settling time of 150 ns while dissipating only 33 mW with $\pm 5V$ supplies. No reference current (I_{REF}) trimming is required for most applications since the full scale output current is typically ± 1 LSB of $255 I_{REF}/256$. Relative accuracies of better than $\pm 0.19\%$ assure 8-bit monotonicity and linearity while zero level output current of less than 4 μA provides 8-bit zero accuracy for $I_{REF} \geq 2$ mA. The power supply currents of the DAC0808 are independent of bit codes, and exhibits essentially constant device characteristics over the entire supply voltage range.

The DAC0808 will interface directly with popular TTL, DTL or CMOS logic levels, and is a direct replacement for the MC1508/MC1408. For higher speed applications, see DAC0800 data sheet.

Features

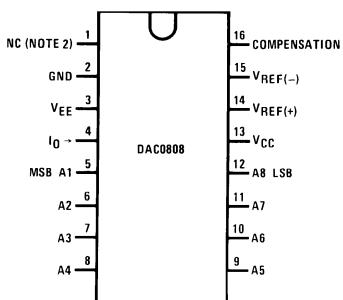
- Relative accuracy: $\pm 0.19\%$ error maximum
- Full scale current match: ± 1 LSB typ
- Fast settling time: 150 ns typ
- Noninverting digital inputs are TTL and CMOS compatible
- High speed multiplying input slew rate: 8 mA/ μs
- Power supply voltage range: $\pm 4.5V$ to $\pm 18V$
- Low power consumption: 33 mW @ $\pm 5V$

Block and Connection Diagrams



DS005687-1

Dual-In-Line Package



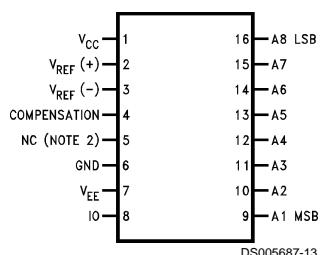
DS005687-2

Top View

Order Number DAC0808
See NS Package M16A or N16A

Block and Connection Diagrams (Continued)

Small-Outline Package



Ordering Information

ACCURACY	OPERATING TEMPERATURE RANGE	N PACKAGE (N16A) (Note 1)		SO PACKAGE (M16A)
		DAC0808LCN	MC1408P8	DAC0808LCM
8-bit	0°C ≤ TA ≤ +75°C			

Note 1: Devices may be ordered by using either order number.

Absolute Maximum Ratings (Note 2)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Power Supply Voltage	
V_{CC}	+18 V _{DC}
V_{EE}	-18 V _{DC}
Digital Input Voltage, V5–V12	-10 V _{DC} to +18 V _{DC}
Applied Output Voltage, V_O	-11 V _{DC} to +18 V _{DC}
Reference Current, I_{14}	5 mA
Reference Amplifier Inputs, V14, V15	V_{CC}, V_{EE}
Power Dissipation (Note 4)	1000 mW
ESD Susceptibility (Note 5)	TBD

Storage Temperature Range	-65°C to +150°C
Lead Temp. (Soldering, 10 seconds)	
Dual-In-Line Package (Plastic)	260°C
Dual-In-Line Package (Ceramic)	300°C
Surface Mount Package	
Vapor Phase (60 seconds)	215°C
Infrared (15 seconds)	220°C

Operating Ratings

Temperature Range	$T_{MIN} \leq T_A \leq T_{MAX}$
DAC0808	$0 \leq T_A \leq +75^\circ C$

Electrical Characteristics

($V_{CC} = 5V$, $V_{EE} = -15 V_{DC}$, $V_{REF}/R14 = 2$ mA, and all digital inputs at high logic level unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
E_r	Relative Accuracy (Error Relative to Full Scale I_O) DAC0808LC (LM1408-8) Settling Time to Within ½ LSB (Includes t_{PLH})	(Figure 4) $T_A=25^\circ C$ (Note 7), (Figure 5)			±0.19	% ns
t_{PLH}, t_{PHL}	Propagation Delay Time	$T_A = 25^\circ C$, (Figure 5)		30	100	ns
TCl_O	Output Full Scale Current Drift			± 20		ppm/ $^\circ C$
MSB	Digital Input Logic Levels High Level, Logic "1" Low Level, Logic "0"	(Figure 3)	2			V _{DC} V _{DC}
V_{IH}					0.8	
V_{IL}						
MSB	Digital Input Current High Level Low Level	(Figure 3) $V_{IH} = 5V$ $V_{IL} = 0.8V$		0 -0.003	0.040 -0.8	mA mA
I_{15}	Reference Input Bias Current	(Figure 3)		-1	-3	μA
	Output Current Range	(Figure 3) $V_{EE} = -5V$ $V_{EE} = -15V, T_A = 25^\circ C$	0 0	2.0 2.0	2.1 4.2	mA mA
I_O	Output Current Output Current, All Bits Low	$V_{REF} = 2.000V,$ $R14 = 1000\Omega,$ (Figure 3) (Figure 3)	1.9	1.99 0	2.1 4	mA μA
	Output Voltage Compliance (Note 3) $V_{EE} = -5V, I_{REF} = 1$ mA V_{EE} Below -10V	$E_r \leq 0.19\%, T_A = 25^\circ C$			-0.55, +0.4 -5.0, +0.4	V _{DC} V _{DC}
SRI _{REF}	Reference Current Slew Rate	(Figure 6)	4	8		mA/ μs
	Output Current Power Supply Sensitivity	$-5V \leq V_{EE} \leq -16.5V$		0.05	2.7	$\mu A/V$
I_{CC} I_{EE}	Power Supply Current (All Bits Low)	(Figure 3)		2.3 -4.3	22 -13	mA mA
V_{CC} V_{EE}	Power Supply Voltage Range	$T_A = 25^\circ C$, (Figure 3)	4.5 -4.5	5.0 -15	5.5 -16.5	V _{DC} V _{DC}
	Power Dissipation					

Electrical Characteristics (Continued)

($V_{CC} = 5V$, $V_{EE} = -15V$, $V_{REF}/R14 = 2\text{ mA}$, and all digital inputs at high logic level unless otherwise noted.)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
	All Bits Low	$V_{CC} = 5V$, $V_{EE} = -5V$		33	170	mW
	All Bits High	$V_{CC} = 5V$, $V_{EE} = -15V$ $V_{CC} = 15V$, $V_{EE} = -5V$ $V_{CC} = 15V$, $V_{EE} = -15V$		106 90 160	305	mW

Note 2: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.

Note 3: Range control is not required.

Note 4: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX} , θ_{JA} , and the ambient temperature, T_A . The maximum allowable power dissipation at any temperature is $P_D = (T_{JMAX} - T_A)/\theta_{JA}$ or the number given in the Absolute Maximum Ratings, whichever is lower. For this device, $T_{JMAX} = 125^\circ\text{C}$, and the typical junction-to-ambient thermal resistance of the dual-in-line J package when the board mounted is 100°C/W . For the dual-in-line N package, this number increases to 175°C/W and for the small outline M package this number is 100°C/W .

Note 5: Human body model, 100 pF discharged through a 1.5 k Ω resistor.

Note 6: All current switches are tested to guarantee at least 50% of rated current.

Note 7: All bits switched.

Note 8: Pin-out numbers for the DAL080X represent the dual-in-line package. The small outline package pinout differs from the dual-in-line package.

Typical Application

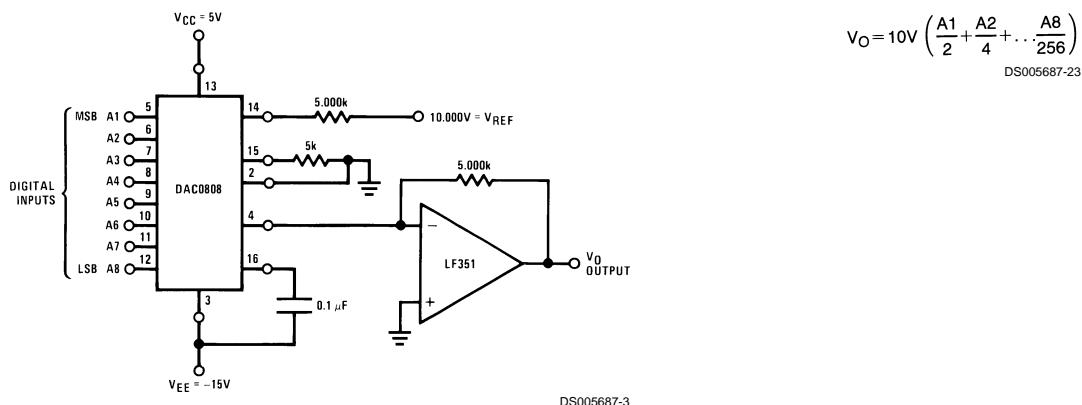
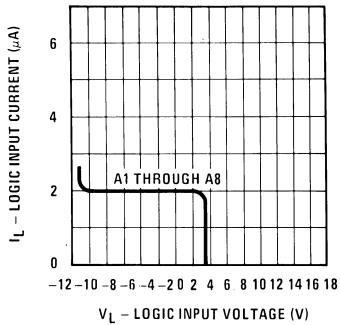


FIGURE 1. +10V Output Digital to Analog Converter (Note 8)

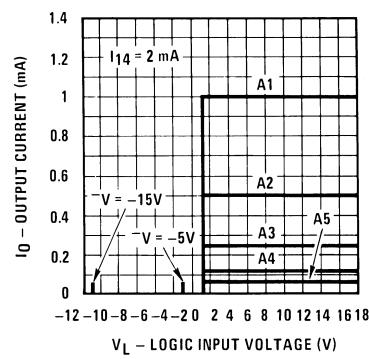
Typical Performance Characteristics

$V_{CC} = 5V$, $V_{EE} = -15V$, $T_A = 25^\circ\text{C}$, unless otherwise noted

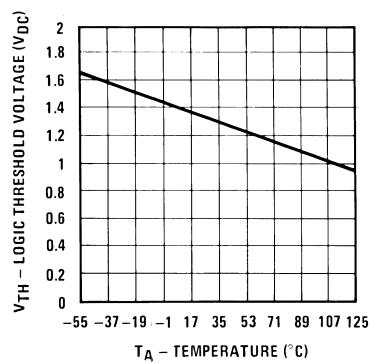
Logic Input Current vs Input Voltage



Bit Transfer Characteristics



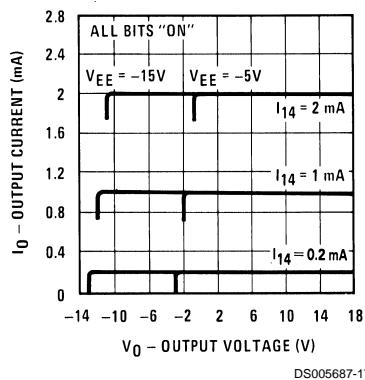
Logic Threshold Voltage vs Temperature



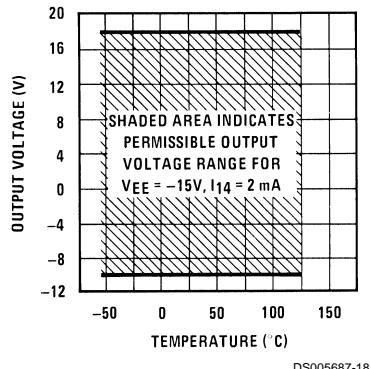
Typical Performance Characteristics

$V_{CC} = 5V$, $V_{EE} = -15V$, $T_A = 25^\circ C$, unless otherwise noted (Continued)

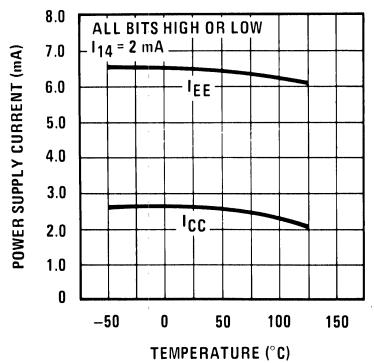
Output Current vs Output Voltage (Output Voltage Compliance)



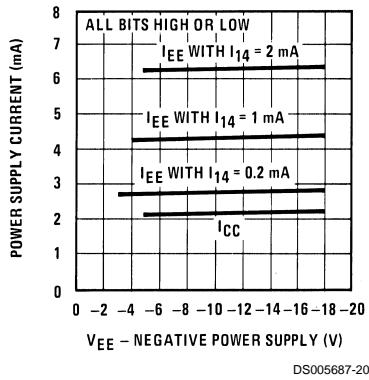
Output Voltage Compliance vs Temperature



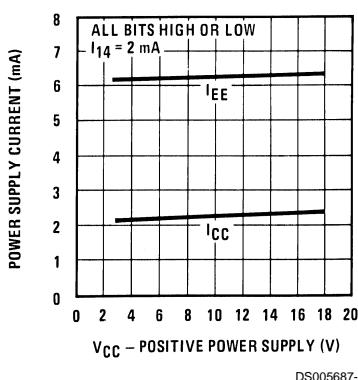
Typical Power Supply Current vs Temperature



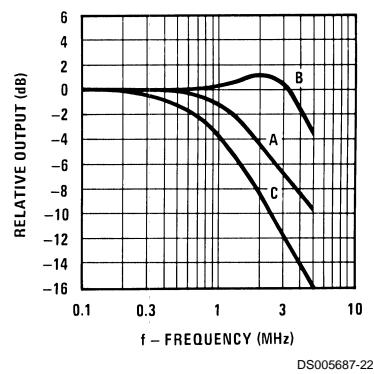
Typical Power Supply Current vs V_{EE}



Typical Power Supply Current vs V_{CC}



Reference Input Frequency Response

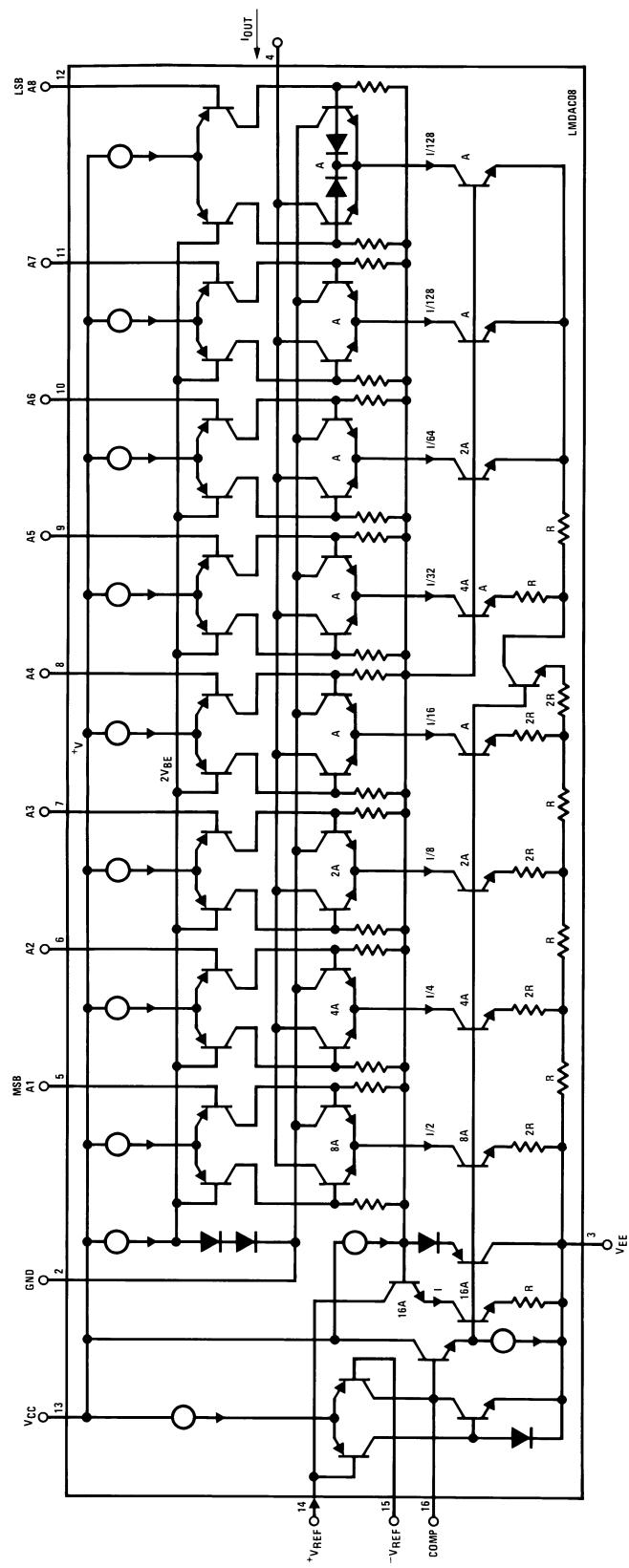


Unless otherwise specified: $R_{14} = R_{15} = 1\text{ k}\Omega$, $C = 15\text{ pF}$, pin 16 to V_{EE} ; $R_L = 50\Omega$, pin 4 to ground.

Curve A: Large Signal Bandwidth Method of Figure 7, $V_{REF} = 2\text{ Vp-p}$ offset 1V above ground.

Curve B: Small Signal Bandwidth Method of Figure 7, $R_L = 250\Omega$, $V_{REF} = 50\text{ mVp-p}$ offset 200 mV above ground.

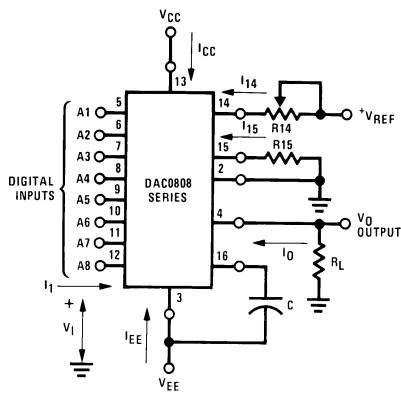
Curve C: Large and Small Signal Bandwidth Method of Figure 9 (no op amp, $R_L = 50\Omega$), $R_S = 50\Omega$, $V_{REF} = 2V$, $V_S = 100\text{ mVp-p}$ centered at 0V.



DS005687-4

FIGURE 2. Equivalent Circuit of the DAC0808 Series (Note 8)

Test Circuits



V_I and I_1 apply to inputs A1–A8.

The resistor tied to pin 15 is to temperature compensate the bias current and may not be necessary for all applications.

$$I_O = K \left(\frac{A_1}{2} + \frac{A_2}{4} + \frac{A_3}{8} + \frac{A_4}{16} + \frac{A_5}{32} + \frac{A_6}{64} + \frac{A_7}{128} + \frac{A_8}{256} \right)$$

$$\text{where } K \cong \frac{V_{\text{REF}}}{R_{14}}$$

and $A_N = "1"$ if A_N is at high level

$A_N = "0"$ if A_N is at low level

FIGURE 3. Notation Definitions Test Circuit (Note 8)

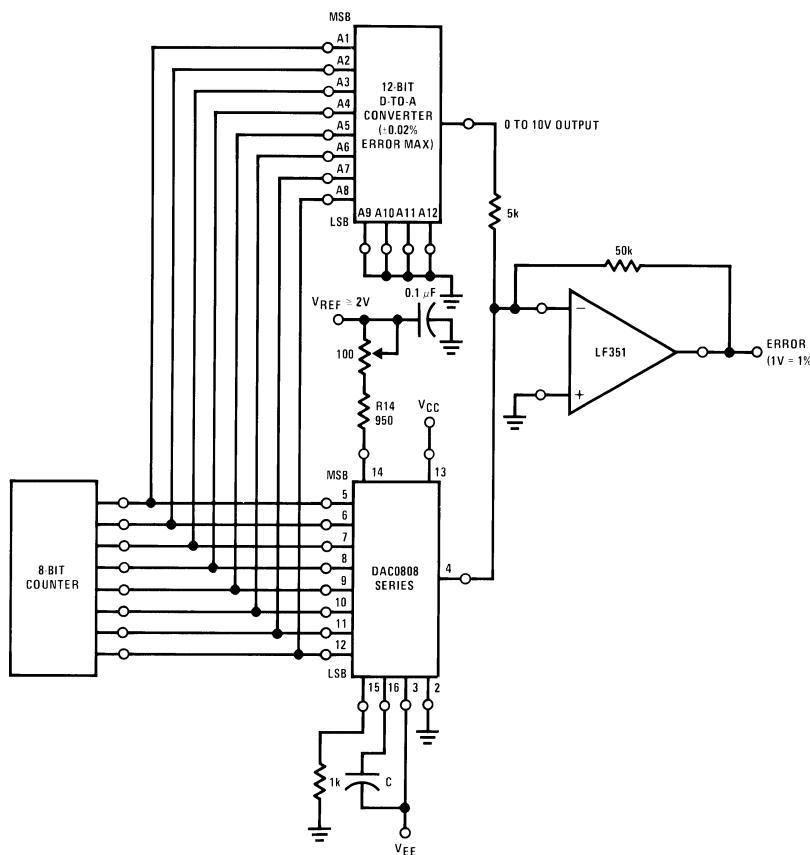


FIGURE 4. Relative Accuracy Test Circuit (Note 8)

Test Circuits (Continued)

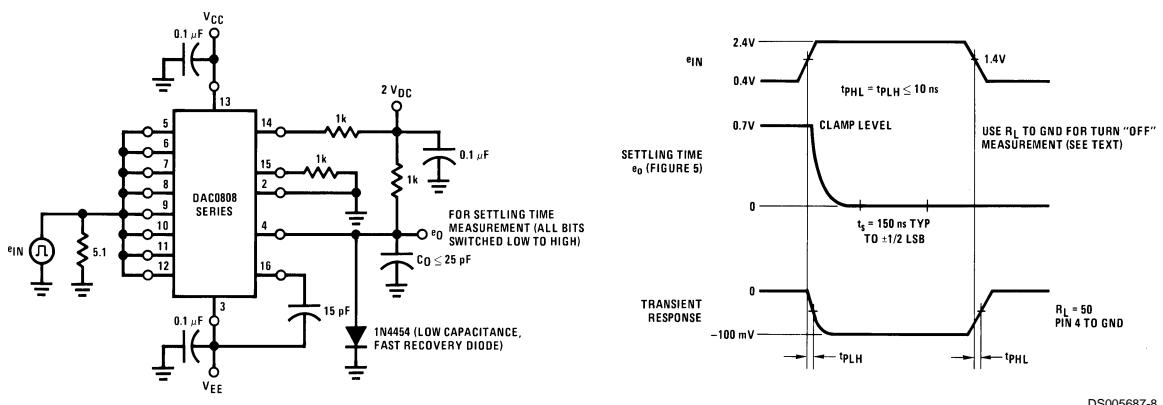


FIGURE 5. Transient Response and Settling Time (Note 8)

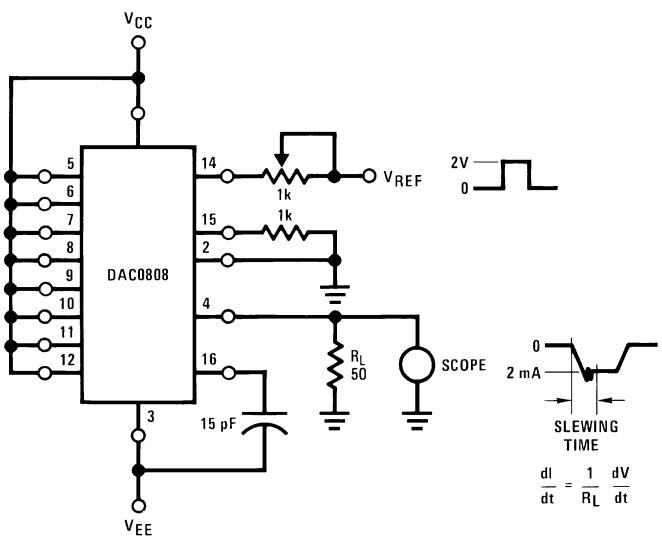
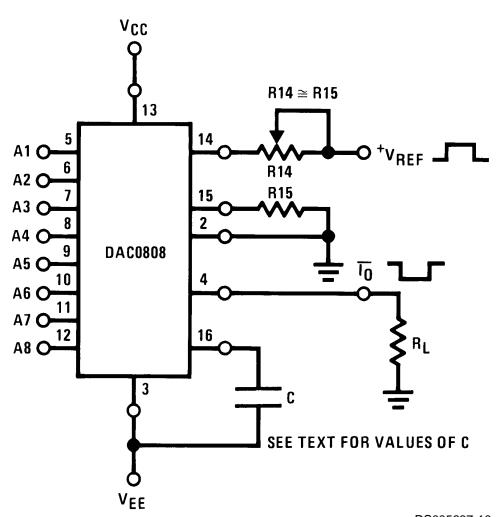


FIGURE 6. Reference Current Slew Rate Measurement (Note 8)

FIGURE 7. Positive V_{REF} (Note 8)

Test Circuits (Continued)

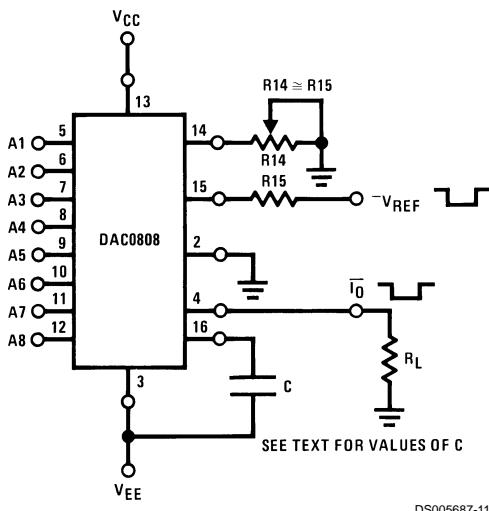


FIGURE 8. Negative V_{REF} (Note 8)

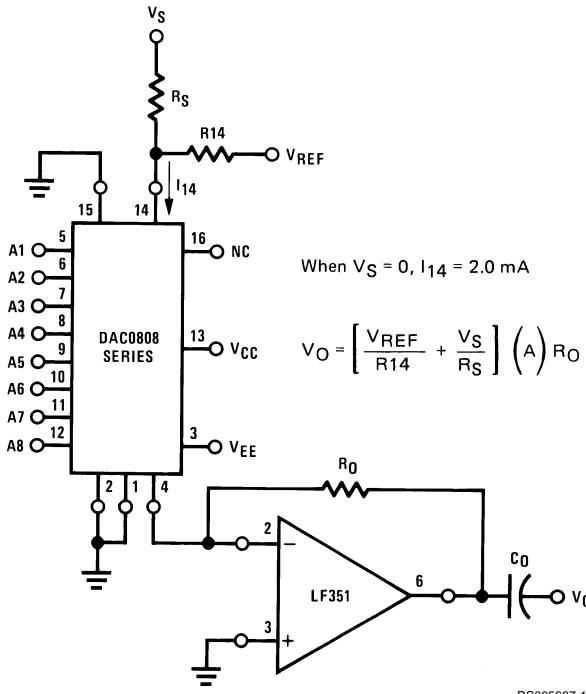


FIGURE 9. Programmable Gain Amplifier or Digital Attenuator Circuit (Note 8)

Application Hints

REFERENCE AMPLIFIER DRIVE AND COMPENSATION

The reference amplifier provides a voltage at pin 14 for converting the reference voltage to a current, and a turn-around circuit or current mirror for feeding the ladder. The reference amplifier input current, I_{14} , must always flow into pin 14, regardless of the set-up method or reference voltage polarity.

Connections for a positive voltage are shown in *Figure 7*. The reference voltage source supplies the full current I_{14} .

For bipolar reference signals, as in the multiplying mode, R15 can be tied to a negative voltage corresponding to the minimum input level. It is possible to eliminate R15 with only a small sacrifice in accuracy and temperature drift.

The compensation capacitor value must be increased with increases in R14 to maintain proper phase margin; for R14 values of 1, 2.5 and 5 k Ω , minimum capacitor values are 15, 37 and 75 pF. The capacitor may be tied to either V_{EE} or ground, but using V_{EE} increases negative supply rejection.

A negative reference voltage may be used if R14 is grounded and the reference voltage is applied to R15 as shown in *Figure 8*. A high input impedance is the main

Application Hints (Continued)

advantage of this method. Compensation involves a capacitor to V_{EE} on pin 16, using the values of the previous paragraph. The negative reference voltage must be at least 4V above the V_{EE} supply. Bipolar input signals may be handled by connecting R14 to a positive reference voltage equal to the peak positive input level at pin 15.

When a DC reference voltage is used, capacitive bypass to ground is recommended. The 5V logic supply is not recommended as a reference voltage. If a well regulated 5V supply which drives logic is to be used as the reference, R14 should be decoupled by connecting it to 5V through another resistor and bypassing the junction of the 2 resistors with 0.1 μ F to ground. For reference voltages greater than 5V, a clamp diode is recommended between pin 14 and ground.

If pin 14 is driven by a high impedance such as a transistor current source, none of the above compensation methods apply and the amplifier must be heavily compensated, decreasing the overall bandwidth.

OUTPUT VOLTAGE RANGE

The voltage on pin 4 is restricted to a range of -0.55 to 0.4V when $V_{EE} = -5V$ due to the current switching methods employed in the DAC0808.

The negative output voltage compliance of the DAC0808 is extended to -5V where the negative supply voltage is more negative than -10V. Using a full-scale current of 1.992 mA and load resistor of 2.5 k Ω between pin 4 and ground will yield a voltage output of 256 levels between 0 and -4.980V. Floating pin 1 does not affect the converter speed or power dissipation. However, the value of the load resistor determines the switching time due to increased voltage swing. Values of R_L up to 500 Ω do not significantly affect performance, but a 2.5 k Ω load increases worst-case settling time to 1.2 μ s (when all bits are switched ON). Refer to the subsequent text section on Settling Time for more details on output loading.

OUTPUT CURRENT RANGE

The output current maximum rating of 4.2 mA may be used only for negative supply voltages more negative than -8V, due to the increased voltage drop across the resistors in the reference current amplifier.

ACCURACY

Absolute accuracy is the measure of each output current level with respect to its intended value, and is dependent upon relative accuracy and full-scale current drift. Relative accuracy is the measure of each output current level as a fraction of the full-scale current. The relative accuracy of the DAC0808 is essentially constant with temperature due to the excellent temperature tracking of the monolithic resistor ladder.

The reference current may drift with temperature, causing a change in the absolute accuracy of output current. However, the DAC0808 has a very low full-scale current drift with temperature.

The DAC0808 series is guaranteed accurate to within $\pm 1/2$ LSB at a full-scale output current of 1.992 mA. This corresponds to a reference amplifier output current drive to the ladder network of 2 mA, with the loss of 1 LSB (8 μ A) which is the ladder remainder shunted to ground. The input current to pin 14 has a guaranteed value of between 1.9 and 2.1 mA, allowing some mismatch in the NPN current source pair. The accuracy test circuit is shown in Figure 4. The 12-bit converter is calibrated for a full-scale output current of 1.992 mA. This is an optional step since the DAC0808 accuracy is essentially the same between 1.5 and 2.5 mA. Then the DAC0808 circuits' full-scale current is trimmed to the same value with R14 so that a zero value appears at the error amplifier output. The counter is activated and the error band may be displayed on an oscilloscope, detected by comparators, or stored in a peak detector.

Two 8-bit D-to-A converters may not be used to construct a 16-bit accuracy D-to-A converter. 16-bit accuracy implies a total error of $\pm 1/2$ of one part in 65,536 or $\pm 0.00076\%$, which is much more accurate than the $\pm 0.019\%$ specification provided by the DAC0808.

MULTIPLYING ACCURACY

The DAC0808 may be used in the multiplying mode with 8-bit accuracy when the reference current is varied over a range of 256:1. If the reference current in the multiplying mode ranges from 16 μ A to 4 mA, the additional error contributions are less than 1.6 μ A. This is well within 8-bit accuracy when referred to full-scale.

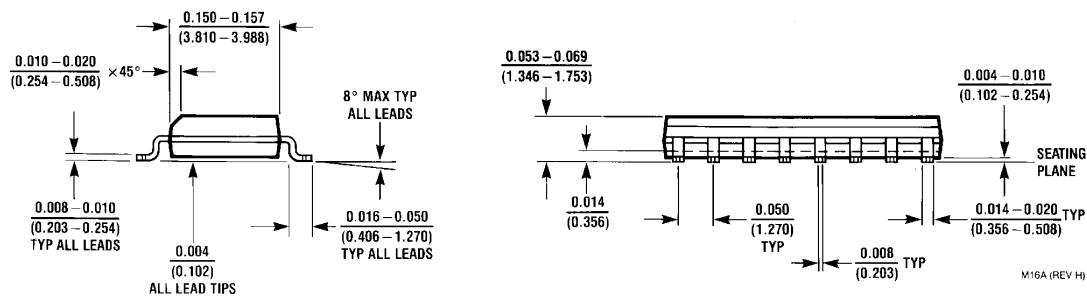
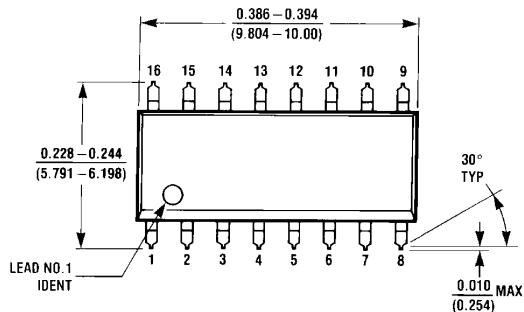
A monotonic converter is one which supplies an increase in current for each increment in the binary word. Typically, the DAC0808 is monotonic for all values of reference current above 0.5 mA. The recommended range for operation with a DC reference current is 0.5 to 4 mA.

SETTLING TIME

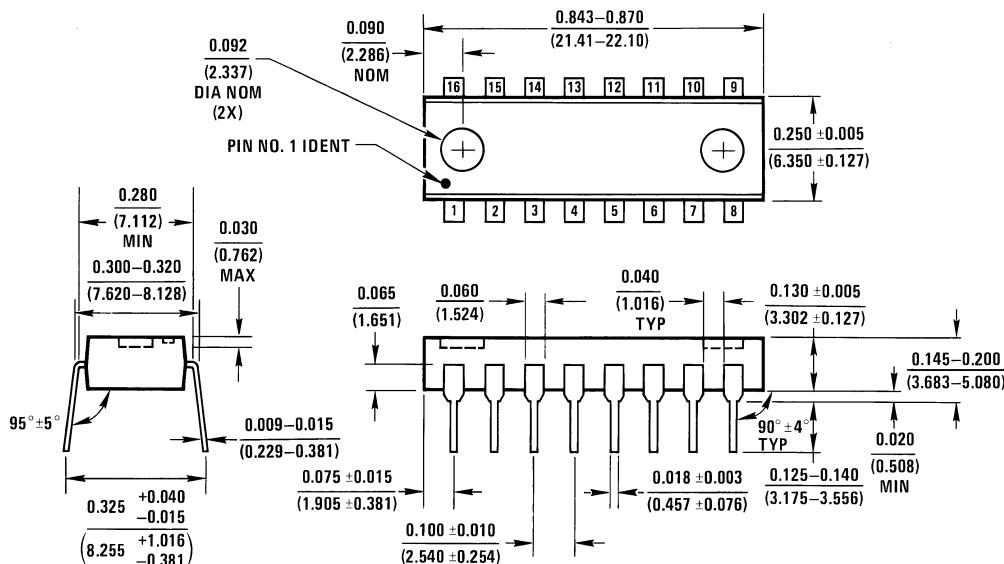
The worst-case switching condition occurs when all bits are switched ON, which corresponds to a low-to-high transition for all bits. This time is typically 150 ns for settling to within $\pm 1/2$ LSB, for 8-bit accuracy, and 100 ns to $1/2$ LSB for 7 and 6-bit accuracy. The turn OFF is typically under 100 ns. These times apply when $R_L \leq 500\Omega$ and $C_O \leq 25 \text{ pF}$.

Extra care must be taken in board layout since this is usually the dominant factor in satisfactory test results when measuring settling time. Short leads, 100 μ F supply bypassing for low frequencies, and minimum scope lead length are all mandatory.

Physical Dimensions inches (millimeters) unless otherwise noted



**Small Outline Package
Order Number DAC0808LCM
NS Package Number M16A**



**Dual-In-Line Package
Order Number DAC0808
NS Package Number N16A**

Notes

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