

Universidad de Costa Rica
Escuela de Ingeniería Eléctrica
IE0624 - Laboratorio de Microcontroladores

Laboratorio 4

STM32: GPIO, ADC, comunicaciones, Iot

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Introducción

En este documento se presenta la solución realizada para el Laboratorio 4 del curso Laboratorio de Microcontroladores. El laboratorio consiste en el desarrollo de un sismógrafo digital utilizado para el estudio y el registro de las oscilaciones que pueden ocurrir en el edificio de la escuela de Ingeniería Eléctrica. En caso de que haya un corte en el suministro de electricidad, el sismógrafo será alimentado por baterías cargadas por paneles solares y tendrá poco ancho de banda para la transmisión de datos.

Para llevar a cabo este sismógrafo se hizo uso del microcontrolador STM32F429 Discovery kit y la biblioteca libopencm3. El sismógrafo hace una lectura de los ejes del giroscopio (X, Y, Z) incorporado en el microcontrolador y cuenta con un botón que permite habilitar o deshabilitar la comunicación USART/USB y con un LED que parpadea para indicar si la de transmisión de datos está habilitada o no. En la práctica el sismógrafo funcionaría con baterías por lo que el microcontrolador es capaz de leer la tensión de las mismas y enciende un LED de alarma en caso de aproximarse al límite mínimo de operación para estas. Tanto el nivel de batería como la habilitación de la comunicación se muestran en la LCD. Por último, se utiliza un script de python para recibir los datos transmitidos desde el puerto serial del microcontrolador y este posteriormente envía la información del giroscopio y el nivel de batería para desplegarlas en un dashboard de la plataforma de thingsboard mediante el uso de widgets.

Los resultados fueron exitosos pues se lograron obtener todas las mediciones requeridas y transmitir la información de manera correcta hacia la plataforma *Thingsboard*.

Todos los recursos asociados a la solución desarrollada se encuentran en el repositorio a continuación: https://github.com/yennergonzalez/Laboratorio_Microcontroladores_4

Nota teórica

Microcontrolador STM32F429 Discovery kit

El STM32F429 Discovery es un kit de desarrollo producido por STMicroelectronics. Aprovecha las capacidades de los microcontroladores de alto rendimiento para permitir a los usuarios desarrollar aplicaciones de manera sencilla con interfaces gráficas de usuario avanzadas. La serie STM32F429 de microcontroladores pertenecen a la línea Advanced que utilizan instrucciones DSP y FPU. Se basa en la tecnología ARM Cortex-M4 y ofrece hasta 180MHz. Contiene un chip integrado que se suministra en un encapsulado LQFP de 144 contactos. Este incluye una herramienta que funciona como interfaz de depuración integrada ST-LINK/V2, una pantalla LCD TFT de 2,4 pulgadas, una SDRAM de 64 Mbits, un sensor giroscopio ST MEMS, LEDs, pulsadores y un conector USB OTG micro-B [3] [4].



Figura 1: Microcontrolador STM32F429 Discovery kit

Características generales del microcontrolador

Dentro de sus características destacan las siguientes:

- Memoria flash de 2 MB, 256 KB de memoria RAM en un empaquetado LQFP144.
- Alimentación de la placa a través del bus USB o desde una tensión de alimentación externa de 3 V o 5 V.
- Sensor de movimiento ST MEMS, giroscopio de salida digital de 3 ejes (L3GD20).
- Pantalla TFT LCD (Thin-film-transistor liquid-crystal display) de 2,4 pulgadas, 262 000 colores RGB, 240 x 320 puntos.

- SDRAM 64 Mbits (1 Mbit x 16-bit x 4-bank) que incluye un modo de actualización automática y un modo de ahorro de energía.
- LED1 (rojo o verde) para la comunicación USB.
- LED2 (rojo) para los 3.3 V de encendido.
- LED3 y LED4 para usuarios.
- USB OTG LEDs, LED5 VBUS (verde) LED6 Over-Current (rojo).
- Dos pulsadores (usuario y reset).
- USB OTG con un conector micro-AB.
- Encabezado de extensión para E/S LQFP144 para una conexión rápida a la placa de creación de prototipos.

Características eléctricas del microcontrolador

La fuente de alimentación de la placa la proporciona la computadora a través del cable USB o también se puede utilizar una fuente de alimentación externa de 5 V. La placa posee dos diodos, el D1 y D2, que protegen los pines de 5 V y 3 V de las fuentes de alimentación externas. Para el diseño del circuito que soluciona el problema propuesto para el laboratorio es necesario considerar las características eléctricas de la plataforma a utilizar: Si no se especifica lo contrario, los valores mínimos y máximos están establecidos en las peores condiciones de temperatura ambiente, tensión de alimentación y frecuencias mediante pruebas en producción en el 100 % de los dispositivos. Los datos típicos se basan en $TA = 25^{\circ}\text{C}$, $VDD = 3,3\text{ V}$ (para el rango de voltajes entre 1,7 V y 3,6 V).

Symbol	Ratings	Min	Max	Unit
V_{DD-VSS}	External main supply voltage (including V_{DDA} , V_{DD} and V_{BAT}) ⁽¹⁾	- 0.3	4.0	
V_{IN}	Input voltage on FT pins ⁽²⁾	$V_{SS} - 0.3$	$V_{DD} + 4.0$	V
	Input voltage on TTa pins	$V_{SS} - 0.3$	4.0	
	Input voltage on any other pin	$V_{SS} - 0.3$	4.0	
	Input voltage on BOOT0 pin	V_{SS}	9.0	
$ \Delta V_{DDx} $	Variations between different V_{DD} power pins	-	50	mV
$ \Delta V_{SSx} $	Variations between all the different ground pins including V_{REF-}	-	50	
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see Section 6.3.15: Absolute maximum ratings (electrical sensitivity)		

Figura 2: Características eléctricas del microcontrolador

Symbol	Ratings	Max.	Unit
ΣI_{VDD}	Total current into sum of all V_{DD_X} power lines (source) ⁽¹⁾	270	
ΣI_{VSS}	Total current out of sum of all V_{SS_X} ground lines (sink) ⁽¹⁾	- 270	
I_{VDD}	Maximum current into each V_{DD_X} power line (source) ⁽¹⁾	100	
I_{VSS}	Maximum current out of each V_{SS_X} ground line (sink) ⁽¹⁾	- 100	
I_{IO}	Output current sunk by any I/O and control pin	25	
	Output current sourced by any I/Os and control pin	- 25	
ΣI_{IO}	Total output current sunk by sum of all I/O and control pins ⁽²⁾	120	
	Total output current sourced by sum of all I/Os and control pins ⁽²⁾	- 120	
$I_{INJ(PIN)}$ ⁽³⁾	Injected current on FT pins ⁽⁴⁾		mA
	Injected current on NRST and BOOT0 pins ⁽⁴⁾		
	Injected current on TTa pins ⁽⁵⁾	±5	
$\Sigma I_{INJ(PIN)}$ ⁽⁵⁾	Total injected current (sum of all I/O and control pins) ⁽⁶⁾	±25	

Figura 3: Características eléctricas del microcontrolador

Diagrama de pines del microcontrolador

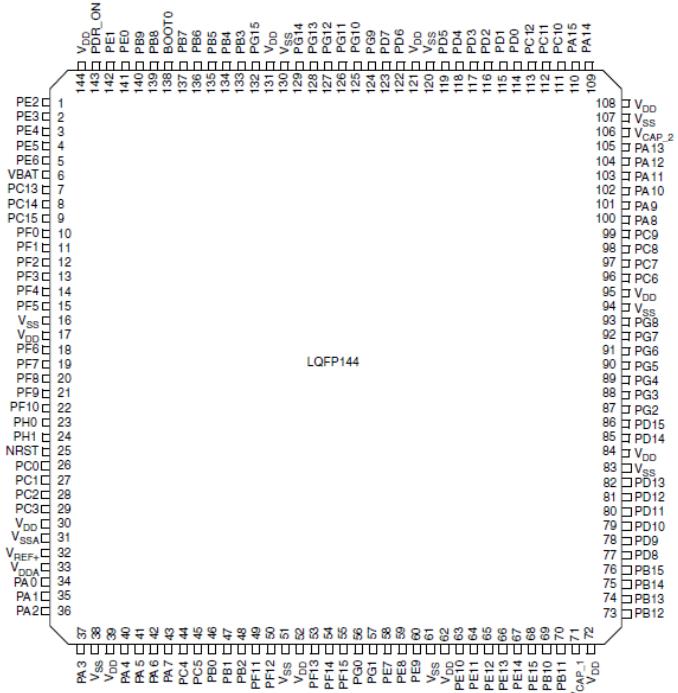


Figura 4: Diagrama de pines del microcontrolador

Diagrama de bloques del microcontrolador

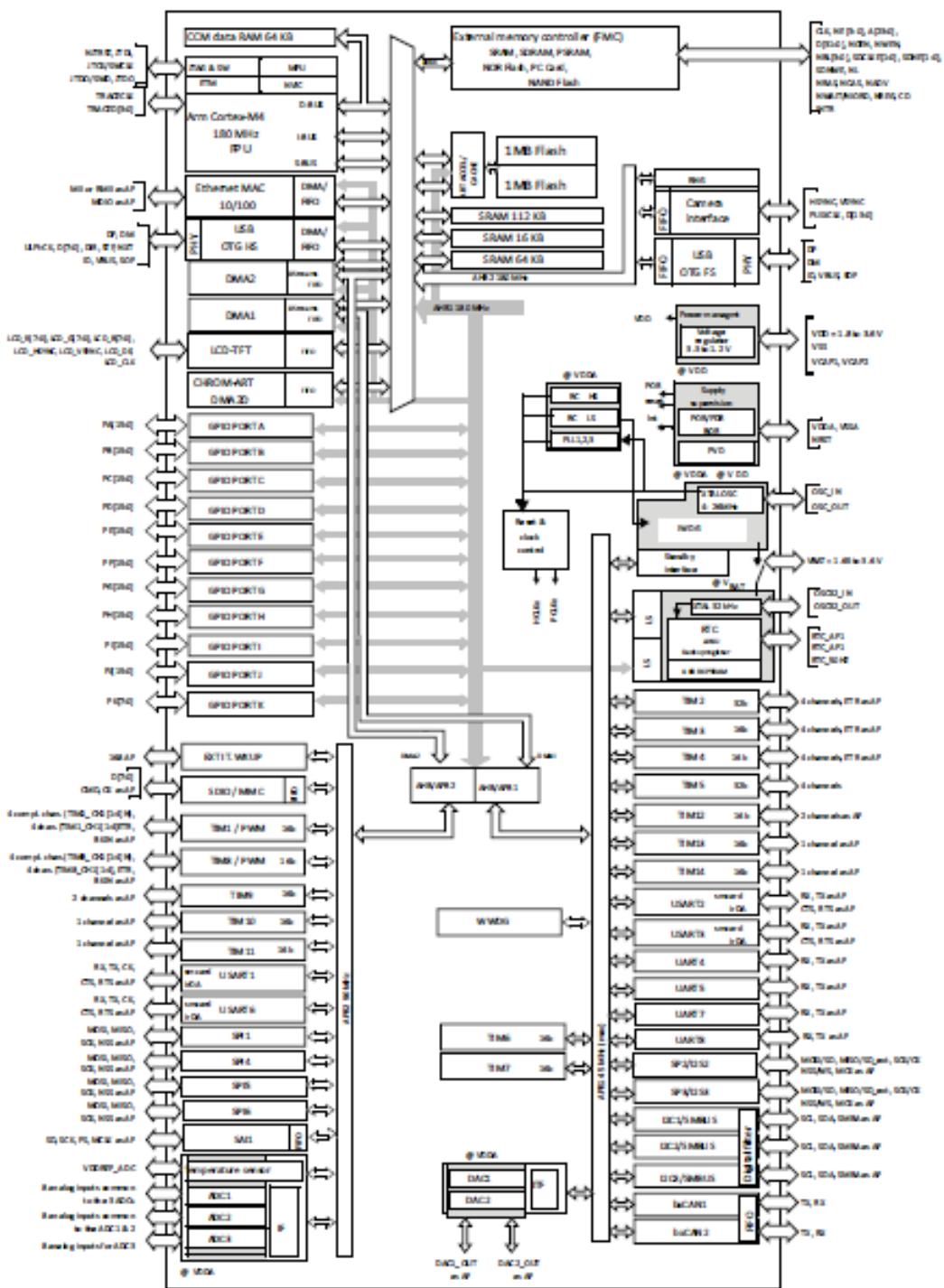


Figura 5: Diagrama de bloques del microcontrolador

Periféricos

LG3D20

El LG3D20 es un sensor angular de tres ejes de bajo consumo. Incluye un elemento de censado y una interfaz IC que posee la capacidad de brindar la medición angular a través de la interfaz digital conocida como I2C/SPI. Esta interfaz se fabrica mediante un proceso CMOS que permite un alto nivel de integración para diseñar un circuito dedicado que se adapta mejor a las características de detección. Además, es capaz de medir velocidades con un ancho de banda ajustada por el usuario.

Este sensor es utilizado en dispositivos de realidad virtual y videojuegos, en robótica, en el control de movimiento hombre-máquina-interfaz, en sistemas de navegación con GPS y algunos electrodomésticos. Se caracteriza por poseer filtros paso alto y paso bajo integrados con ancho de banda seleccionable por el usuario, además tiene un modo de apagado y de suspensión integrados, tiene una alta capacidad de supervivencia a impactos, tiene un sensor de temperatura y un protocolo FIFO.

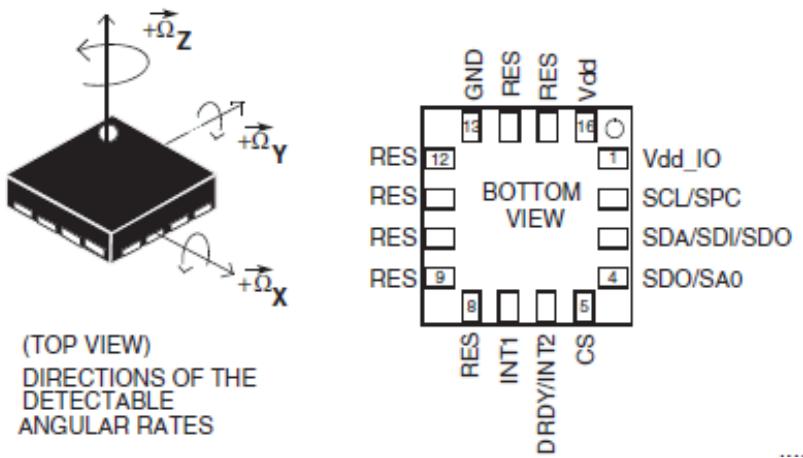


Figura 6: Sensor MEMS L3GD20

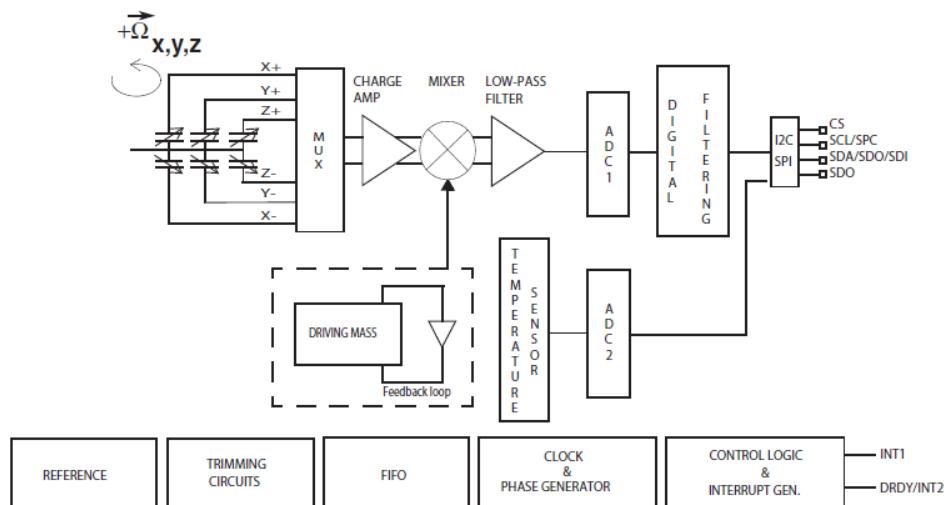


Figura 7: Diagrama de bloques del Sensor MEMS L3GD20

ILI9341

El ILI9341 es un controlador SOC (System On Chip) para una pantalla táctil de cristal líquido TFT con una resolución RGB de 240x320 píxeles. Permite una interfaz de bus de datos paralelo de 8/9/16/18 bits, una de RGB de bus de datos de 6/16/18 bits y un periférica serial (SPI) de 3/4 líneas. Puede funcionar con un voltaje de entrada y salida de entre 1,65 V y 3,3 V y posee un circuito seguidor de voltaje incorporado para generar niveles de voltaje que controlan la pantalla LCD. Es compatible con el modo de visualización a todo color de 8 colores y el modo de suspensión para un control de energía preciso por software.

Estas características hacen que el ILI9341 sea un controlador de LCD ideal para productos portátiles de tamaño mediano o pequeño, como teléfonos celulares digitales, teléfonos inteligentes donde la duración de la batería es un aspecto a tomar en cuenta.



Figura 8: Pantalla LCD

Diseño del circuito

Para este laboratorio prácticamente todo es implementado a través de la placa de desarrollo, el único circuito adicional corresponde a un divisor de tensión para obtener una señal de entre 0 y 5 V que es proporcional a una de entre 0 y 9 V, correspondiente a la tensión de la batería.

Lista de componentes y costos

Cantidad	Componente	Costo unitario
1	STM32F429 Discovery kit	\$29.9
2	Resistores	\$0.50 (10 unidades)

Tabla 1: Costos de los componentes utilizados.

Costo total

De acuerdo con los precios listados, el costo total de los componentes utilizados sería de **\$31**. Este es un precio relativamente accesible.

Conceptos/temas de laboratorio

Librería LibOpenCM3

Libopencm3 (anteriormente conocido como libopenstm32) es un proyecto (librería de hardware) cuyo objetivo es el de crear una biblioteca de firmware libre o de código abierto (LGPL v3 o posterior) para varios microcontroladores de la familia ARM Cortex-M3 (pero también se admiten M0, M4 y más por venir), incluidos ST STM32, Toshiba TX03, Atmel SAM3U, NXP LPC1000, EFM32 y otros [2].

Tecnología IOT y Thingsboard

El IoT (Internet de las cosas) corresponde a todos aquellos objetos que son de uso cotidiano que se pueden conectar a internet de manera autónoma sin la necesidad de la intervención humana. Para llevar a cabo el IoT en numerosos objetos es necesario contar con ciertos módulos, o incluso microcontroladores que ya traen incorporada esta función, que pueden brindar la capacidad de comunicación y conexión a la red, que normalmente es inalámbrica. Uno de los microcontroladores más famosos para este tipo de aplicación es el ESP8266 [1].

Uno de los protocolos de datos utilizados para IoT es el MQTT (Message Queuing Telemetry Transport) el es de gran utilidad para establecer conexiones en ubicaciones remotas donde es necesario usar poca memoria y/o ancho de banda. Para el laboratorio, también se utilizará Thingsboard, que es una plataforma de IoT Open source se encarga de recolectar, procesar, visualizar datos y administrar dispositivos. Tiene la capacidad de habilitar alarmas por eventos de telemetría, actualizaciones de atributos y acciones de usuarios. Se accede mediante iot.eie.ucr.ac.cr.

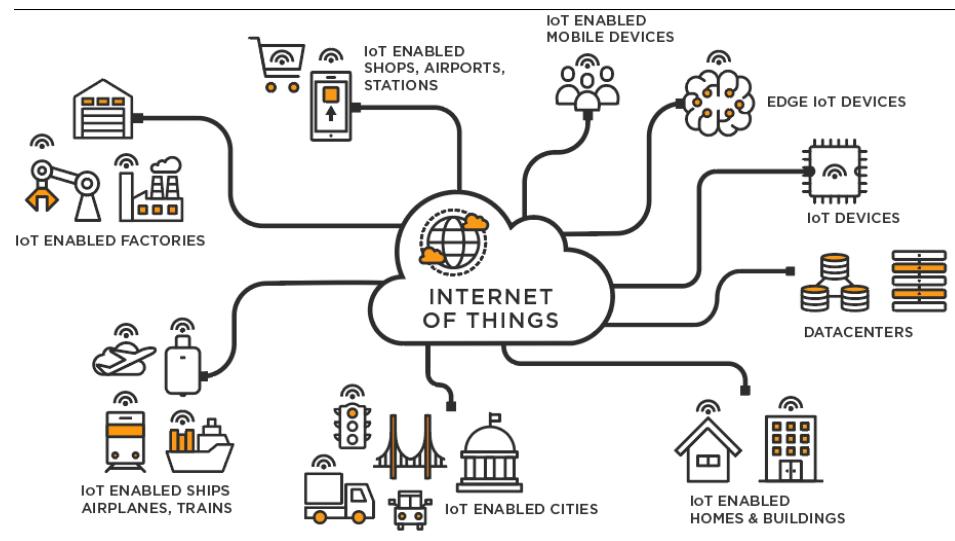


Figura 9: Esquema de IoT

Comunicación USART

Los microcontroladores normalmente poseen puertos serie destinados a comunicaciones llamado USART (Universal Synchronous Asynchronous Receiver Transmitter) los cuales se configuran para realizar una comunicación asincrónica bidireccional simultánea (full duplex) o sincrónica (con transmisión de la señal de reloj) en ambas direcciones de manera no simultánea (half duplex). Para llevar a cabo esta comunicación, el Arduino utiliza los pines señalados con 0 y 1 que corresponden a RX y TX respectivamente. En el modo asíncrono, TX corresponde a la terminal por la cual sale la señal de datos y RX es la terminal por donde entran los datos enviados [5]. USART permite la comunicación del Arduino con la computadora y posee la característica de poder enviar paquetes de datos mayores que una UART.

Desarrollo

Análisis del programa

El programa es relativamente sencillo pues este se implementa utilizando las funciones de la biblioteca `libopencm3` que permiten abstraer significativamente la configuración del microcontrolador. A grandes rasgos el *firmware* consiste de tres partes: la declaración de funciones, la configuración inicial y el funcionamiento continuo, donde las últimas dos corresponden específicamente a la parte que se ejecuta. La secuencia de ejecución se muestra en el siguiente diagrama de flujo:

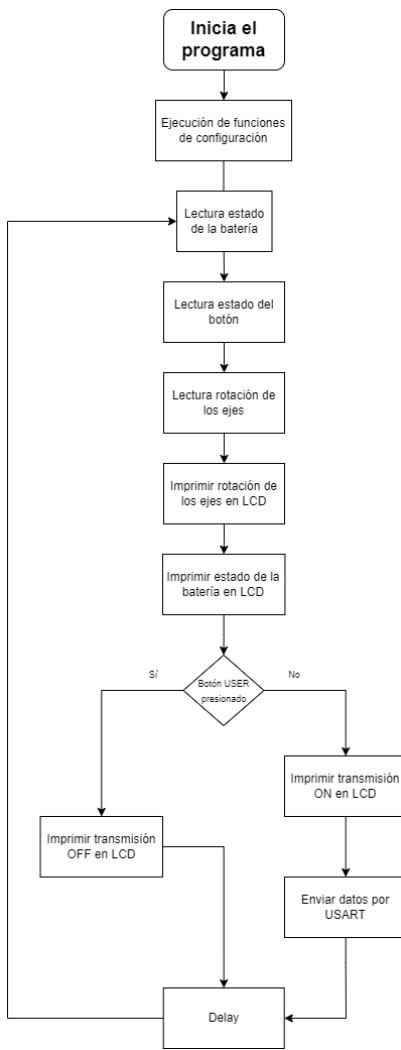


Figura 10: Diagrama de flujo del *firmware* desarrollado para el sismógrafo.

A continuación también se detalla lo que se realiza en cada una de las partes del programa:

Declaración de funciones

En la declaración de funciones se listan las funciones que se utilizarán en el programa y los parámetros que estas recibirán. En esta sección se tienen las funciones que se utilizarán para configurar los pines y puertos junto con su modo de funcionamiento (entrada, salida, entrada analógica, función alternativa ...) y algunas funciones para obtener datos. Dentro de las primeras figuran las funciones `clock_setup`, `batt_setup`, `USART_setup`, `spi_setup`, `button_setup`, `adc_setup` y `gpio_setup`.

Las funciones utilizadas para obtener datos corresponden a `read_xyz` y `read_adc_naiive` que obtienen la aceleración en los tres ejes y la tensión de entrada en el pin PA1 (para medir la tensión de la batería), respectivamente.

Configuración inicial - set up

La parte de configuración del programa consiste en ejecutar las funciones de configuración declaradas en la parte anterior de manera que el microcontrolador quede listo para operar de la manera deseada.

Funcionamiento continuo - while

Después de las dos partes anteriores se entra en el funcionamiento cíclico del programa, este consiste en leer las aceleraciones en los tres ejes mediante el giroscopio, imprimir estos valores en la pantalla, leer el estado del botón **USER** del microcontrolador para determinar si la comunicación está habilitada o deshabilitada, leer la tensión de la batería e imprimir su porcentaje de carga en la pantalla y encender los LEDs correspondientes si la comunicación está habilitada y si la batería es baja. Después de esto se entra a un ciclo **for** para hacer que el microcontrolador espere un tiempo y después se repite el procedimiento recién enunciado de manera indefinida.

De acuerdo a si la comunicación está habilitada o no, los datos medidos por el microcontrolador se envían hacia la plataforma Thingsboard .

Para la impresión en pantalla se utiliza la función **gfx_puts** y para transmitir los datos por USART se utiliza la función **uart_send_blocking** mientras que para la interacción con giroscopio se utilizan las funciones **spi_read** y **spi_send** pues estas permiten leer y escribir a este para indicarle la operación que se desea realizar y su configuración.

Lectura giroscopio: Para la lectura del giroscopio se utilizan tres variables para cada eje: **axis_data**, **past_axis_data** y **print_axis_data**. El valor actual leído corresponde a **axis_data** mientras que **past_axis_data** corresponde al valor medido del ciclo anterior, finalmente, **print_axis_data** se define como la resta de las dos variables anteriores y es esta variable la que se imprime en la pantalla y la que se transmite. Esto se hace porque inicialmente se estaban obteniendo valores extraños (aceleraciones en todos los ejes a pesar de que la placa estaba inmóvil), y simplemente consiste en tomar el cambio entre dos mediciones consecutivas, eliminando cualquier sesgo o error de calibración que pueda tener el giroscopio y que produzca dichos errores.

Registro de datos y transmisión a Thingsboard

Una vez creada la cuenta en Thingsboard, el primer paso para empezar a trabajar en la plataforma es crear un device que va a ser la representación del microcontrolador y se configuran los credenciales, en este caso se utilizó un token.

La información a transmitir (estado de la batería y la rotación de los ejes) se está obteniendo continuamente y si la transmisión USART está activada esta llega al script de python que la *parsea* y la transmite hacia Thingsboard.

```
broker='iot.eie.ucr.ac.cr'
topic_pub='v1/devices/me/telemetry'
```

Además, se debe configurar el **client.username_pw_set** que sería el token del device de Thingsboard y por último se realiza la conexión al broker con **client.connect**.

```
client.username_pw_set("14gy9675")
client.connect(broker)
```

Una vez hecho esto, se procede con la parte del código que se encarga de la extracción de datos transmitidos de manera serial. Se toma una línea a la vez y del formato decidido en el firmware se sabe que cada medición está separada de la siguiente por un carácter ',' (coma), por que utilizando el comando **split** se puede obtener fácilmente una lista con los elementos a reportar:

```
getData=ser.readline()
dataString = getData.decode('utf-8')
data=dataString[0:-2]
splitdata = data.split(',')
```

A continuación se indica el elemento de la lista que contiene cada una de las magnitudes medidas:

- `splitdata[0]` : Aceleración en X
- `splitdata[1]`: Aceleración en Y
- `splitdata[2]`: Aceleración en Z
- `splitdata[3]`: porcentaje de la batería

Por último, para que la transmisión de datos se haga efectiva, se configuran los siguientes comandos que lo que hacen es publicar a un broker/servidor desde un cliente:

```
client.publish(topic_pub, msgx) para la aceleración en X
client.publish(topic_pub, msgy) para la aceleración en Y
client.publish(topic_pub, msgz) para la aceleración en Z
client.publish(topic_pub, msgbatterys) para el nivel de batería
client.publish(topic_pub, msgbatteryp) para el porcentaje de batería
```

El script está configurado para enviar conjuntos de datos cada medio segundo. Para revisar que todo esté funcionando de manera correcta basta con revisar el apartado últimas telemetrías.

Análisis del circuito

Para este laboratorio prácticamente todos los requerimientos son implementados mediante la placa de desarrollo por lo que el circuito externo al microcontrolador es mínimo.

Dimensionamiento de los componentes

En esta sección se presentan los cálculos realizados para determinar los valores requeridos para los distintos componentes utilizados.

Para este laboratorio el único dimensionamiento requerido fue el de un divisor de tensión para la batería de 9 V pues la entrada del microcontrolador puede ser como máximo de 5 V. Para esto se propuso que la corriente que debería circular a través del divisor debe ser baja (para evitar que la batería se descarga rápidamente) y se eligió para esta un valor de $500 \mu A$, por lo tanto, despejando la resistencia total requerida:

$$R = \frac{V}{I} = \frac{9 \text{ V}}{500 \mu\text{A}} = 18 \text{ k}\Omega$$

Luego, se quiere que la primera resistencia del divisor genere una caída de 4 V, de manera que la tensión entre el nodo intermedio del divisor (que será el valor medido por el microcontrolador) y tierra sea una señal de máximo 5 V, por lo tanto, los resistores deberían tener los siguientes valores con tal de tener las caídas deseadas:

$$R_1 = \frac{V}{I} = \frac{4 \text{ V}}{500 \mu\text{A}} = 8 \text{ k}\Omega$$

$$R_2 = \frac{V}{I} = \frac{4 \text{ V}}{500 \mu\text{A}} = 10 \text{ k}\Omega$$

Comercialmente no existen resistencias de $8 \text{ k}\Omega$ por lo que en su lugar se utilizará una de $8,2 \text{ k}\Omega$ mientras que las de $10 \text{ k}\Omega$ sí están disponibles comercialmente.

Capturas del funcionamiento del microcontrolador

En esta sección se muestran fotografías y capturas de los resultados obtenidos durante el desarrollo del laboratorio:

LED Comunicación En estas fotografías se puede observar que el LED LD3 (verde, derecha) está encendido cuando no se presionada el botón USER y correspondientemente se tiene el texto “Transmitting: ON” en la pantalla. Por otra parte, cuando se presiona el botón, el LED deja de parpadear y se despliega en la pantalla “Transmitting: OFF”.



Figura 11: Microcontrolador sin el botón presionado, comunicación habilitada.



Figura 12: Microcontrolador con el botón presionado, comunicación deshabilitada.

LED Batería Baja Para las fotografías a continuación se puede observar que cuando la batería tiene por entrada 5 V, el LED LD4 (rojo, izquierda) permanece apagado y se tiene en la pantalla el texto “Batería: 93 %” mientras que cuando se conecta a 0 V, el LED empieza a parpadear y se muestra en la pantalla el texto “Batería: 0 %”. (Para esta parte como no se contaba con una batería de 9 V se utilizaron las salidas de 5 V y GND de un Arduino UNO)

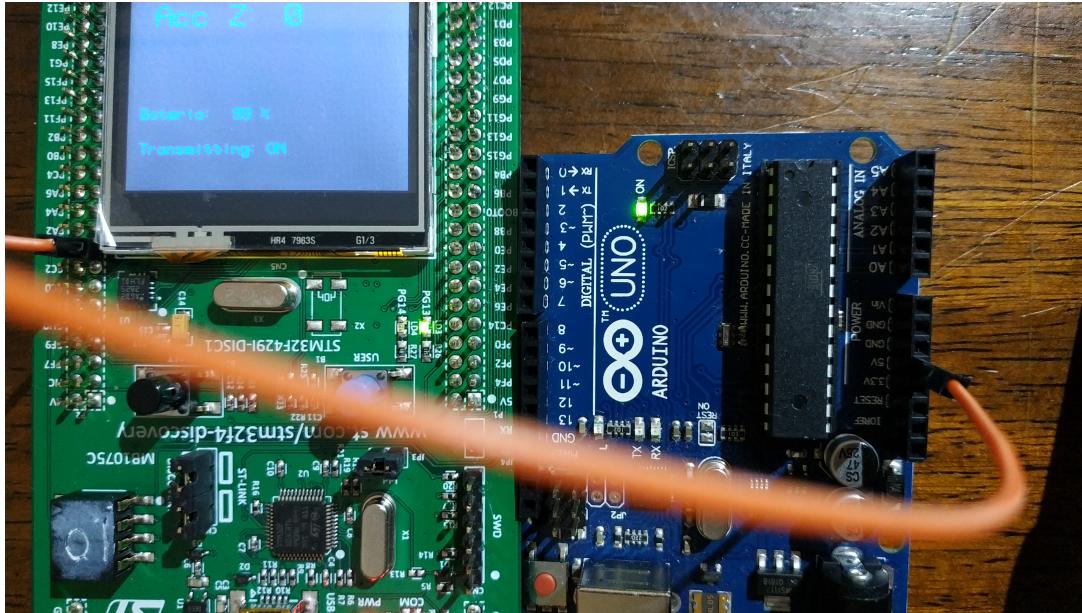


Figura 13: Microcontrolador con una fuente de aproximadamente 5 V en la entrada medida, batería alta.

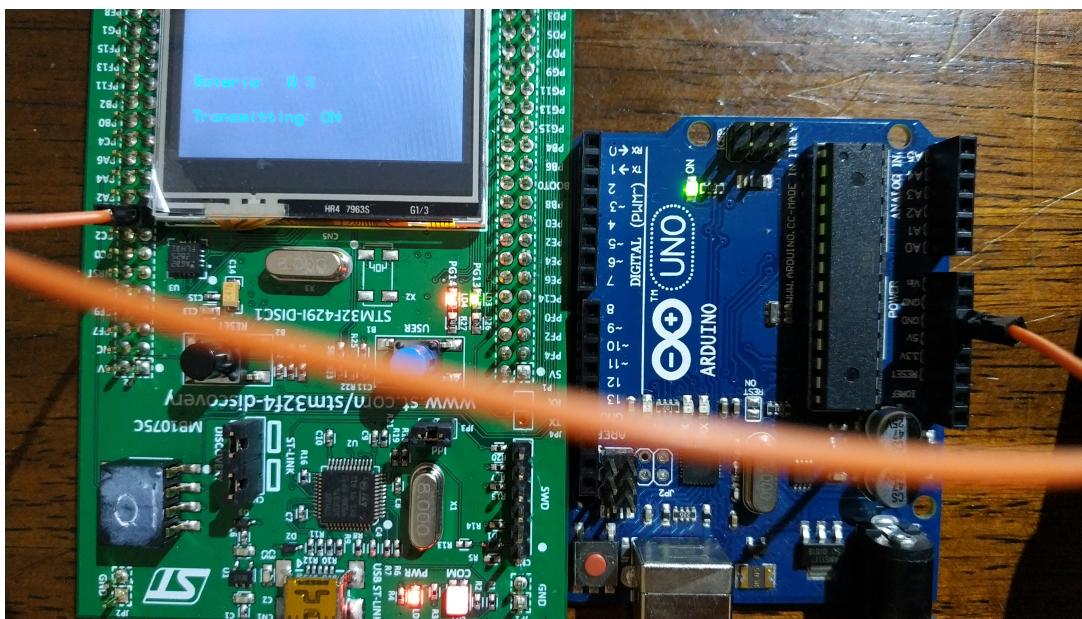


Figura 14: Microcontrolador sin tensión de alimentación en la entrada medida, batería baja.

Display En la figura a continuación se muestra la pantalla desplegando todos los datos indicados en el enunciado:



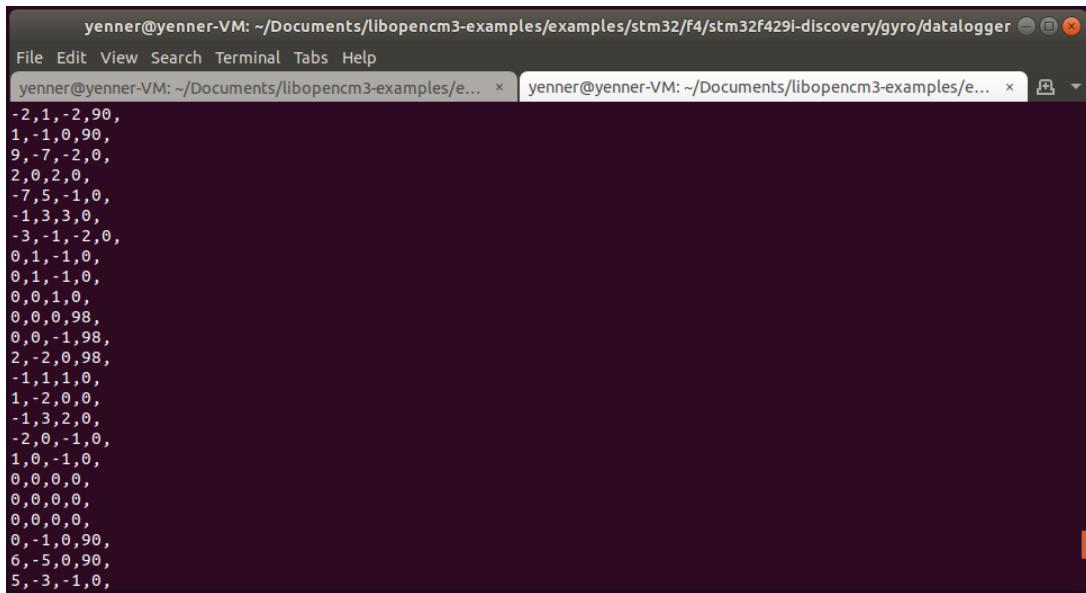
Figura 15: Pantalla LCD del microcontrolador mostrando los valores requeridos.

Giroscopio En la siguiente figura se muestra una fotografía tomada de los valores reportados por el giroscopio en la pantalla LCD.



Figura 16: Pantalla LCD reportando los valores medidos mediante el giroscopio

Comunicación USART En la figura siguiente se muestra la captura de una terminal donde se está ejecutando el *script* de *python* donde se almacenan los datos transmitidos mediante USART. Los valores son, respectivamente, la rotación en el eje x, la rotación en el eje y, la rotación en el eje z y el porcentaje de batería sensado.



A screenshot of a terminal window titled "yenner@yenner-VM: ~/Documents/libopencm3-examples/examples/stm32/f4/stm32f429i-discovery/gyro/datalogger". The window contains two tabs. The left tab shows the command "python" being run. The right tab displays a continuous stream of data. The data consists of three columns of values separated by commas: rotation in X, rotation in Y, rotation in Z, and battery percentage. The data starts with "-2,1,-2,90," and continues with many other entries, indicating periodic USART transmissions.

```
-2,1,-2,90,
1,-1,0,90,
9,-7,-2,0,
2,0,2,0,
-7,5,-1,0,
-1,3,3,0,
-3,-1,-2,0,
0,1,-1,0,
0,1,-1,0,
0,0,1,0,
0,0,0,98,
0,0,-1,98,
2,-2,0,98,
-1,1,1,0,
1,-2,0,0,
-1,3,2,0,
-2,0,-1,0,
1,0,-1,0,
0,0,0,0,
0,0,0,0,
0,0,0,0,
0,-1,0,90,
0,-5,0,90,
5,-3,-1,0,
```

Figura 17: Valores de rotación en los ejes y porcentaje de batería enviados mediante USART.

Thingsboard Como se muestra en la figura 18, se utilizaron 2 widgets, el primero es de categoría card que permite visualizar una tabla con los datos enviados por el microcontrolador. El segundo widget es de categoría chart, este es una gráfica temporal que muestra el cambio de la información a través del tiempo.

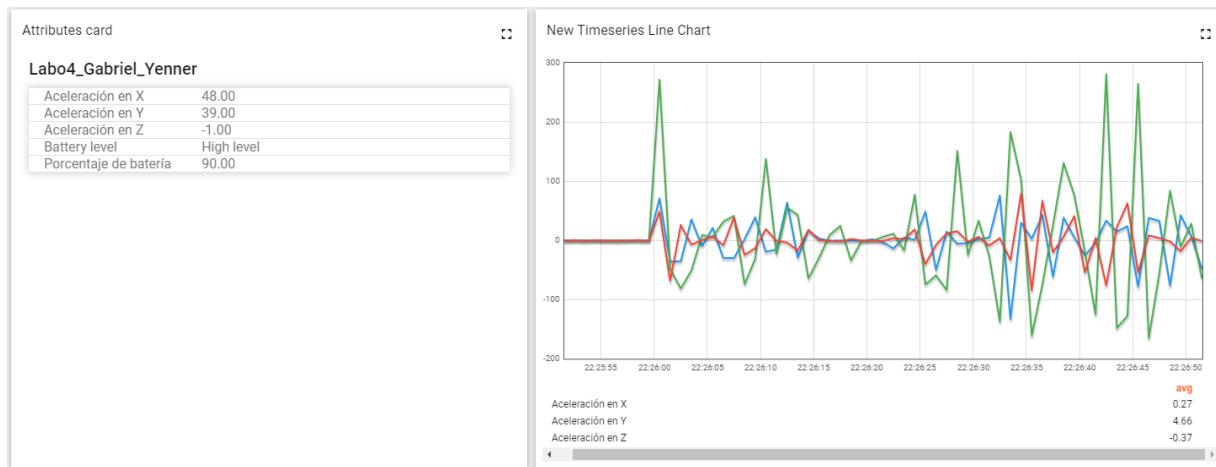


Figura 18: Transmisión de la información a Thingsboard

Conclusiones y recomendaciones

- Se logró implementar un sismógrafo, que lee los valores reoprtados por su giroscopio y los reporta en su pantalla LCD junto con su estado actual de batería.
- Se transmitieron los datos medidos por el microcontrolador mediante USART y fue posible habilitar o deshabilitar esta comunicación mediante el uso del botón de usuario del microcontrolador.
- Mediante un script de Python, se logró enviar la información generada por el microcontrolador a la plataforma Thingsboard de manera correcta.
- Se recomienda revisar cuidadosamente cada parte del diseño antes de pasar a la siguiente pues tuvimos dificultades con incorporar el giroscopio al resto del programa, sin embargo partiendo de un programa nuevo e implementando primero el giroscopio y luego incluyendo las demás partes ya desarrolladas el programa funcionó correctamente.
- Se recomienda leer tanto la hoja del fabricante como la documentación de las bibliotecas a utilizar para comprender como se relacionan entre sí las funciones con el modo de operación deseado para los componentes.
- Otra recomendación es revisar que los datos transmitidos desde el microcontrolador tengan un formato correcto para que el script de Python no genere errores en el momento de su ejecución y con ello garantizar que los datos transmitidos hacia Thingsboard sean correctos.

Referencias

- [1] Pizarro Peláez, J. (2020). Internet de las cosas (IOT) con ESP manual práctico. Ediciones Paraninfo. https://books.google.co.cr/books?id=B2oHEAAQBAJ&pg=PA42&dq=sensor+BMP180&hl=es&sa=X&ved=2ahUKEwixg_63kpX4AhWynWoFHY-PDAAQ6AF6BAGIEAI#v=onepage&q=sensor%20BMP180&f=false
- [2] LibOpenCM3. <https://libopencm3.org/>
- [3] RS. Kit de desarrollo Discovery de STMicroelectronics, con núcleo ARM Cortex M4F. <https://es.rs-online.com/web/p/kits-de-desarrollo-de-microcontroladores/9093660>
- [4] STMicroelectronics. Discovery kit with STM32F429ZI MCU * New order code STM32F429I-DISC1. <https://www.st.com/en/evaluation-tools/32f429idiscovery.html>
- [5] Valdés, F. Pallas, R. (2007). *Microcontroladores: Fundamentos y aplicaciones con PIC*. https://books.google.co.cr/books?id=ODenKG0HMRkC&pg=PA258&dq=comunicacion+USART&hl=es&sa=X&ved=2ahUKEwif7vWG0dn6AhVbRjABHQ_HB0cQ6AF6BAGEEAI#v=onepage&q=comunicacion%20USART&f=false.

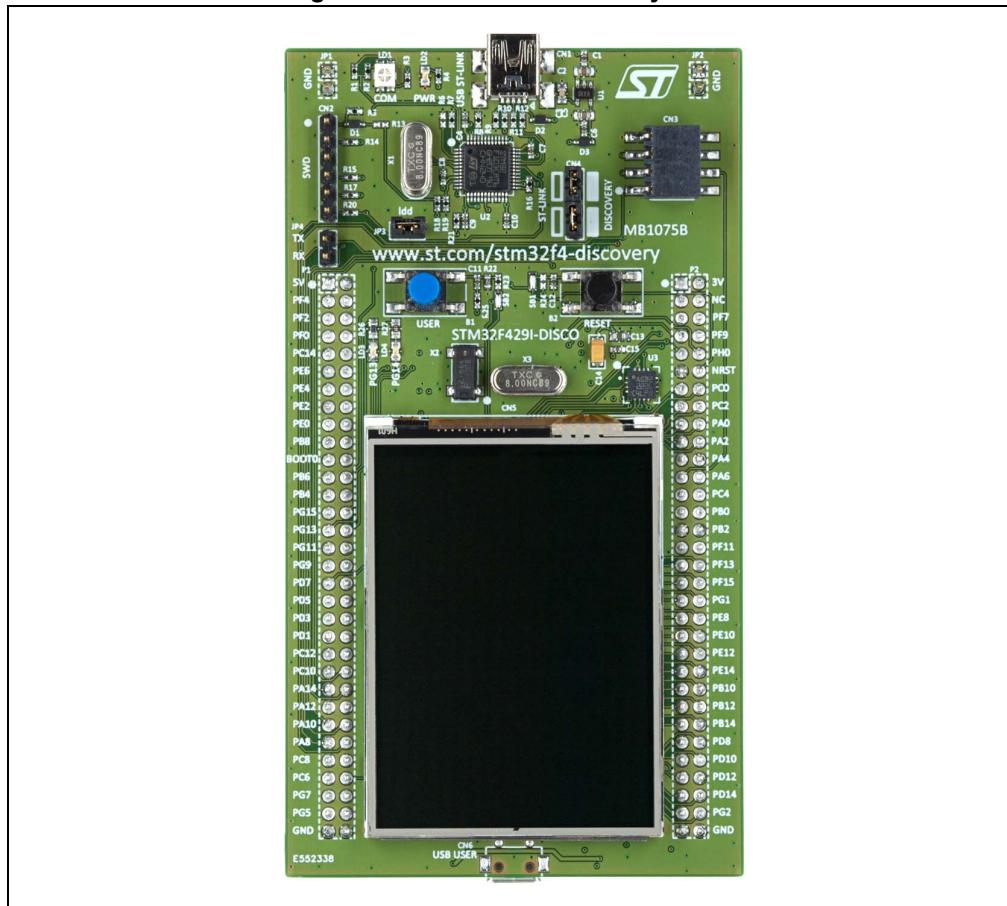
Apéndices

En esta sección se presentan las hojas del fabricante de los componentes utilizados.

Introduction

The STM32F429 Discovery kit (32F429IDISCOVERY) helps you to discover the high performance of the STM32F4 series and to develop your applications. It is based on an STM32F429ZIT6 and includes an ST-LINK/V2 embedded debug tool interface, 2.4" TFT LCD, SDRAM 64 Mbits, Gyroscope ST MEMS, LEDs, pushbuttons and a USB OTG micro-B connector.

Figure 1. STM32F429 Discovery board



2 Quick start

The STM32F429 Discovery is a low-cost and easy-to-use development kit to quickly evaluate and start a development with an STM32F4 series microcontroller.

Before installing and using the product, please accept the Evaluation Product License Agreement from www.st.com/stm32f4-discovery.

For more information on the STM32F429 Discovery board and for demonstration software, visit www.st.com/stm32f4-discovery.

2.1 Getting started

Follow the sequence below to configure the STM32F429 Discovery board and launch the DISCOVER application:

1. Ensure that the jumpers JP3 and CN4 are set to "on" (Discovery mode).
2. Connect the STM32F429 Discovery board to a PC using a USB cable type A/mini-B through the USB ST-LINK connector CN1, to power the board. The LEDs LD2 (PWR) and LD1 (COM).
3. The following applications are available on the screen:
 - Clock/Calendar and Game
 - Video Player and Image Browser (play videos and view images from the USB mass storage connected to CN6)
 - Performance monitor (watch the CPU load and run a graphical benchmark)
 - System Info
4. The demo software, as well as other software examples that allow you to discover the STM32 F4 series features, are available on www.st.com/stm32f4-discovery.
5. Develop your own applications starting from the examples.

2.2 System requirements

- Windows PC (XP, Vista, 7)
- USB type A to mini-B cable

2.3 Development toolchain supporting the STM32F429 Discovery kit

- Altium: TASKING™ VX-Toolset
- Atollic: TrueSTUDIO
- IAR: EWARM
- Keil™: MDK-ARM

2.4 Order code

To order the STM32F429 Discovery kit, use the STM32F429I-DISCO order code.

3 Features

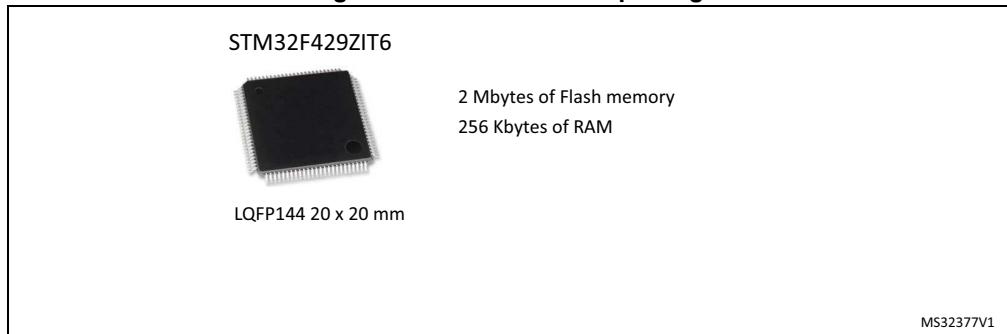
The STM32F429 Discovery board offers the following features:

- STM32F429ZIT6 microcontroller featuring 2 MB of Flash memory, 256 KB of RAM in an LQFP144 package
- On-board ST-LINK/V2 with selection mode switch to use the kit as a standalone ST-LINK/V2 (with SWD connector for programming and debugging)
- Board power supply: through the USB bus or from an external 3 V or 5 V supply voltage
- L3GD20, ST MEMS motion sensor, 3-axis digital output gyroscope
- TFT LCD (Thin-film-transistor liquid-crystal display) 2.4", 262K colors RGB, 240 x 320 dots
- SDRAM 64 Mbits (1 Mbit x 16-bit x 4-bank) including an AUTO REFRESH MODE, and a power-saving
- Six LEDs:
 - LD1 (red/green) for USB communication
 - LD2 (red) for 3.3 V power-on
 - Two user LEDs:
LD3 (green), LD4 (red)
 - Two USB OTG LEDs:
LD5 (green) VBUS and LD6 (red) OC (over-current)
- Two pushbuttons (user and reset)
- USB OTG with micro-AB connector
- Extension header for LQFP144 I/Os for a quick connection to the prototyping board and an easy probing

4.1 STM32F429ZIT6 microcontroller

This ARM Cortex-M4 32-bit MCU with FPU has 225 DMIPS, up to 2 MB Flash/256 + 4 KB RAM, USB OTG HS/FS, Ethernet, 17 TIMs, 3 ADCs, 20 comm. interfaces, a camera and an LCD-TFT, 1.7-3.6 V operation.

Figure 4. STM32F429ZIT6 package



This device provides the following benefits (see [Table 2](#)).

Table 2. Features and benefits

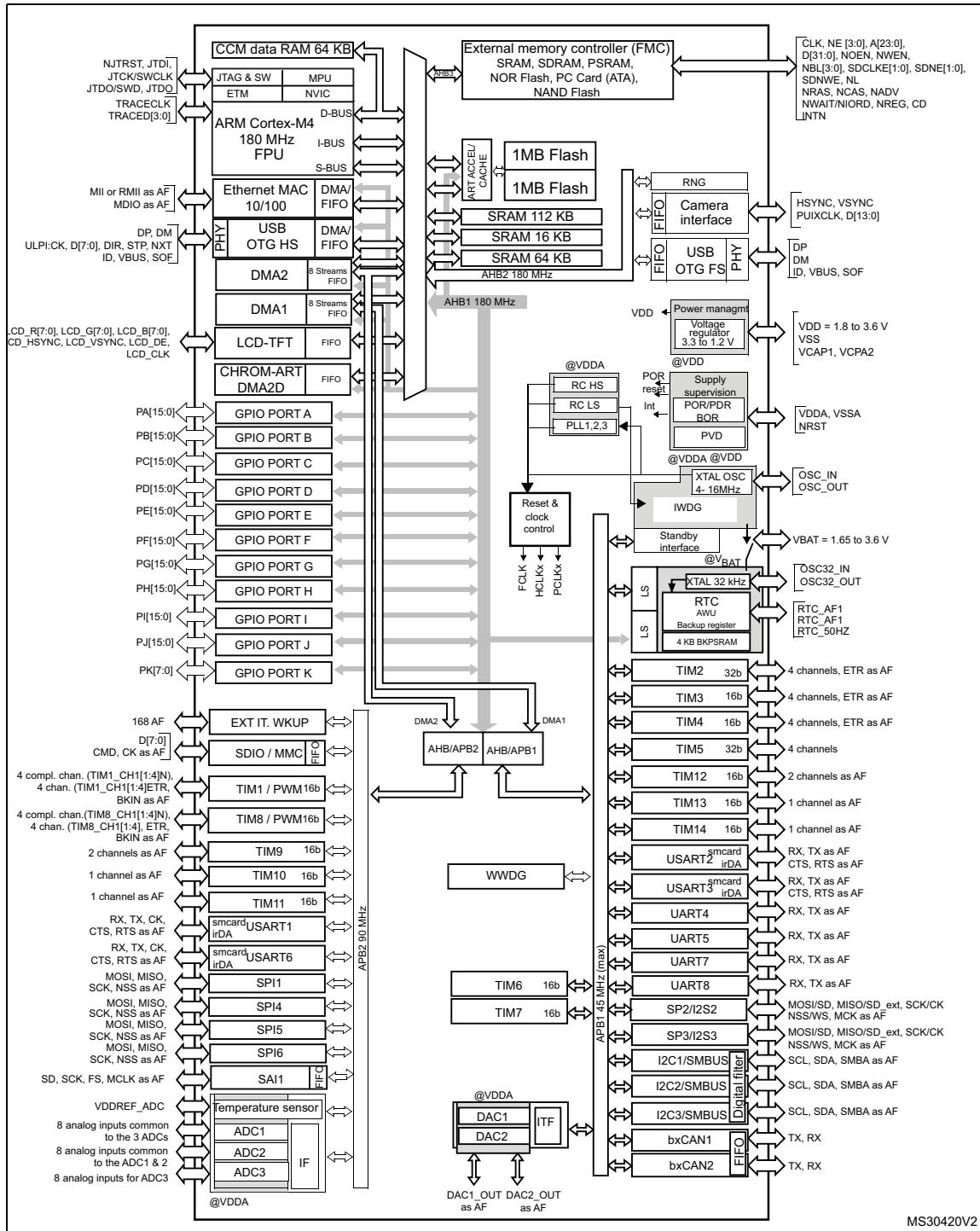
Features	Benefits
High performance <ul style="list-style-type: none"> – Up to 180 MHz/225 DMIPS Cortex-M4 with single cycle DSP MAC and floating point unit – CoreMark score: 608 at 180 MHz – CoreMark/MHz: 3.37 	<ul style="list-style-type: none"> – Boosted execution of control algorithms – More features for your applications – Ease of use – Better code efficiency – Faster time to market – Elimination of scaling and saturation – Easier support for meta-language tools
Maximum integration <ul style="list-style-type: none"> – Up to 2 Mbytes of on-chip dual bank Flash memory, up to 256 Kbytes of SRAM, reset circuit, internal RCs, PLLs, ultra-small packages (WLCSP) 	<ul style="list-style-type: none"> – Read while write operations support – More features in space-constrained applications – Use of high-level languages: Java, .Net
Designed for high performance and ultra-fast data transfers <ul style="list-style-type: none"> – ART Accelerator™: memory accelerator – Chrom-ART Accelerator™: graphic accelerator (rectangle filling, rectangle copy with pixel format conversion and blending) 	<ul style="list-style-type: none"> – Performance equivalent to zero-wait execution from Flash – Graphic content is created twice as fast and independently from the CPU
<ul style="list-style-type: none"> – 32-bit, 7-layer AHB bus matrix with up to 10 masters and 8 slaves including 3 blocks of SRAM – Multi DMA controllers: 2 general-purpose, 1 for USB HS, one for Ethernet 	Concurrent execution and data transfer
<ul style="list-style-type: none"> – One 4th SRAM block dedicated to the core 	Simplified resource allocation
<ul style="list-style-type: none"> – Flexible memory interface with SDRAM support: up to 90 MHz, 32-bit parallel 	<ul style="list-style-type: none"> – High bandwidth for external memories – Cost-effective external RAM

Table 2. Features and benefits (continued)

Features	Benefits
Outstanding power efficiency <ul style="list-style-type: none"> – Ultra-low dynamic power in Run mode: 260 μA/MHz at 180 MHz running CoreMark benchmark from Flash memory (peripherals off) – RTC <1 μA typ in V_{BAT} mode – Down to 100 μA typ in Stop mode – 3.6 V down to 1.7 V V_{DD} – 1.2 V voltage regulator with power scaling capability 	Extra flexibility to reduce power consumption for applications requiring both high-processing and low-power performance when running at low voltage or on a rechargeable battery
Superior and innovative peripherals and connectivity <ul style="list-style-type: none"> – Connectivity: camera interface, crypto/hash HW processor with AES GCM and CCM support, and SHA-256 – Ethernet MAC10/100 with IEEE 1588 v2 support, 2 USB OTG (one with HS support) – Up to 20 communication interfaces (including 4x USART + 4x UART, 6x SPI, 3x I²C with digital filter, 2x CAN, SDIO) – USART at 11.25 Mbit/s; SPI at 45 Mbit/s 	New possibilities to connect and communicate high-speed data
Audio: <ul style="list-style-type: none"> – dedicated audio PLL, 2x I²S and 1x SAI with TDM⁽¹⁾ support 	High-quality multi-channel audio support
<ul style="list-style-type: none"> – LCD TFT controller – Up to SVGA format (800 x 600) – Up to 24-bit RGB parallel pixel output – 2-layer support with blending 	Support for cost-effective standard displays
Analog: <ul style="list-style-type: none"> – 2x 12-bit DACs, 3x 12-bit ADCs reaching 7.2 MSPS in interleaved mode – Up to 17 timers: 16 and 32 bits running up to 180 MHz 	More precision thanks to high resolution
High integration <ul style="list-style-type: none"> – WLCSP143 4.5 x 5.5 mm, 2-Mbyte Flash/256-Kbyte SRAM) 	Smaller board space allowing for smaller applications
Extensive tools and software solutions <ul style="list-style-type: none"> – Hardware sector protection with execute only access – Various IDE, starter kits, libraries, RTOS and stacks, either open source or provided by ST or 3rd parties, including the ARM CMSIS DSP library optimized for Cortex-M4 instructions 	<ul style="list-style-type: none"> – Software IP protection – A wide choice within the STM32 ecosystem to develop your applications

1. TDM: time division multiplex

Figure 5. STM32F429ZIT6 block diagram



4.3 Power supply and power selection

The power supply is provided either by the host PC through the USB cable, or by an external 5 V power supply.

The D1 and D2 diodes protect the 5 V and 3 V pins from external power supplies:

- 5 V and 3 V can be used as output power supplies when another application board is connected to pins P1 and P2.
In this case, the 5 V and 3 V pins deliver a 5 V or 3 V power supply and the power consumption must be lower than 100 mA.
- 5 V and 3 V can also be used as input power supplies, e.g. when the USB connectors are not connected to the PC.
In this case, the STM32F429 Discovery board must be powered by a power supply unit or by an auxiliary equipment complying with standard EN-60950-1: 2006+A11/2009, and must be Safety Extra Low Voltage (SELV) with limited power capability.

Note: *The board can also be powered through the USB USER connector and is protected by D4 and D5 diodes when both USBs are connected (in which case, the 5 V power is around 4.4 volts).*

4.4 LEDs

- LD1 COM:
LD1 default status is red. LD1 turns to green to indicate that communications are in progress between the PC and the ST-LINK/V2.
- LD2 PWR:
The red LED indicates that the board is powered.
- User LD3:
The green LED is a user LED connected to the I/O PG13 of the STM32F429ZIT6.
- User LD4:
The red LED is a user LED connected to the I/O PG14 of the STM32F429ZIT6.
- User LD5:
The green LED indicates when VBUS is present on CN6 and is connected to PB13 of the STM32F429ZIT6.
- User LD6:
The red LED indicates an overcurrent from VBUS of CN6 and is connected to the I/O PC5 of the STM32F429ZIT6.

4.5 Pushbuttons

- B1 USER:
User and Wake-Up button connected to the I/O PA0 of the STM32F429ZIT6.
- B2 RESET:
The pushbutton connected to NRST is used to RESET the STM32F429ZIT6.

4.6 USB OTG supported

The STM32F429ZIT6 is used to drive only USB OTG full speed on this board. The USB micro-AB connector (CN6) allows the user to connect a host or device component, such as a USB key, mouse, and so on.

Two LEDs are dedicated to this module:

- LD5 (green LED) indicates when VBUS is active
- LD6 (red LED) indicates an overcurrent from a connected device.

4.7 Gyroscope MEMS (ST MEMS L3GD20)

The L3GD20 is an ultra-compact, low-power, three-axis angular rate sensor. It includes a sensing element and an IC interface able to provide the measured angular rate to the external world through the I2C/SPI serial interface.

The L3GD20 has dynamically user-selectable full scales of ± 250 dps/ 500 dps/ ± 2000 dps and is capable of measuring rates.

The STM32F429ZIT6 MCU controls this motion sensor through the SPI interface.

4.8 TFT LCD (Thin-film-transistor liquid-crystal display)

The TFT LCD is a 2.41" display of 262 K colors. Its definition is QVGA (240 x 320 dots) and is directly driven by the STM32F429ZIT6 using the RGB protocol. It includes the ILI9341 LCD controller and can operate with a 2.8 ± 0.3 V voltage.

The STM32F429ZIT6 MCU controls this motion sensor through the SPI interface.

4.9 64-Mbit SDRAM (1Mbit x 16-bit x 4-bank)

The 64-Mbit SDRAM is a high speed CMOS, dynamic random-access memory designed to operate in 3.3 V memory systems containing 67,108,864 bits. It is internally configured as a quad-bank DRAM with a synchronous interface. Each 16,777,216-bit bank is organized as 4,096 rows by 256 columns by 16 bits. The 64-Mbit SDRAM includes an AUTO REFRESH MODE, and a power-saving, power-down mode. All signals are registered on the positive edge of the clock signal, CLK.

The STM32F429ZIT6 MCU reads and writes data at 80 MHz.

4.10 JP3 (Idd)

Jumper JP3, labeled Idd, allows the consumption of STM32F429ZIT6 to be measured by removing the jumper and connecting an ammeter.

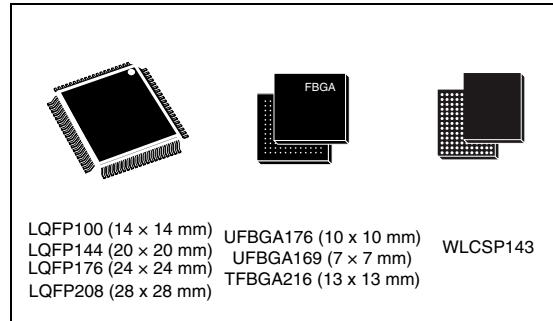
- Jumper on: STM32F429ZIT6 is powered (default).
- Jumper off: an ammeter must be connected to measure the STM32F429ZIT6 current, (if there is no ammeter, the STM32F429ZIT6 is not powered).

32b Arm® Cortex®-M4 MCU+FPU, 225DMIPS, up to 2MB Flash/256+4KB RAM, USB OTG HS/FS, Ethernet, 17 TIMs, 3 ADCs, 20 com. interfaces, camera & LCD-TFT

Datasheet - production data

Features

- Core: Arm® 32-bit Cortex®-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait state execution from Flash memory, frequency up to 180 MHz, MPU, 225 DMIPS/1.25 DMIPS/MHz (Dhrystone 2.1), and DSP instructions
- Memories
 - Up to 2 MB of Flash memory organized into two banks allowing read-while-write
 - Up to 256+4 KB of SRAM including 64-KB of CCM (core coupled memory) data RAM
 - Flexible external memory controller with up to 32-bit data bus: SRAM, PSRAM, SDRAM/LPSDR SDRAM, Compact Flash/NOR/NAND memories
- LCD parallel interface, 8080/6800 modes
- LCD-TFT controller with fully programmable resolution (total width up to 4096 pixels, total height up to 2048 lines and pixel clock up to 83 MHz)
- Chrom-ART Accelerator™ for enhanced graphic content creation (DMA2D)
- Clock, reset and supply management
 - 1.7 V to 3.6 V application supply and I/Os
 - POR, PDR, PVD and BOR
 - 4-to-26 MHz crystal oscillator
 - Internal 16 MHz factory-trimmed RC (1% accuracy)
 - 32 kHz oscillator for RTC with calibration
 - Internal 32 kHz RC with calibration
- Low power
 - Sleep, Stop and Standby modes
 - V_{BAT} supply for RTC, 20×32 bit backup registers + optional 4 KB backup SRAM
- 3×12-bit, 2.4 MSPS ADC: up to 24 channels and 7.2 MSPS in triple interleaved mode
- 2×12-bit D/A converters
- General-purpose DMA: 16-stream DMA controller with FIFOs and burst support
- Up to 17 timers: up to twelve 16-bit and two 32-bit timers up to 180 MHz, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input



- Debug mode
 - SWD & JTAG interfaces
 - Cortex-M4 Trace Macrocell™
- Up to 168 I/O ports with interrupt capability
 - Up to 164 fast I/Os up to 90 MHz
 - Up to 166 5 V-tolerant I/Os
- Up to 21 communication interfaces
 - Up to 3 × I²C interfaces (SMBus/PMBus)
 - Up to 4 USARTs/4 UARTs (11.25 Mbit/s, ISO7816 interface, LIN, IrDA, modem control)
 - Up to 6 SPIs (45 Mbit/s), 2 with muxed full-duplex I²S for audio class accuracy via internal audio PLL or external clock
 - 1 x SAI (serial audio interface)
 - 2 × CAN (2.0B Active) and SDIO interface
- Advanced connectivity
 - USB 2.0 full-speed device/host/OTG controller with on-chip PHY
 - USB 2.0 high-speed/full-speed device/host/OTG controller with dedicated DMA, on-chip full-speed PHY and ULPI
 - 10/100 Ethernet MAC with dedicated DMA: supports IEEE 1588v2 hardware, MII/RMII
- 8- to 14-bit parallel camera interface up to 54 Mbytes/s
- True random number generator
- CRC calculation unit
- RTC: subsecond accuracy, hardware calendar
- 96-bit unique ID

2 Description

The STM32F427xx and STM32F429xx devices are based on the high-performance Arm® Cortex®-M4 32-bit RISC core operating at a frequency of up to 180 MHz. The Cortex-M4 core features a Floating point unit (FPU) single precision which supports all Arm® single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

The STM32F427xx and STM32F429xx devices incorporate high-speed embedded memories (Flash memory up to 2 Mbyte, up to 256 Kbytes of SRAM), up to 4 Kbytes of backup SRAM, and an extensive range of enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

All devices offer three 12-bit ADCs, two DACs, a low-power RTC, twelve general-purpose 16-bit timers including two PWM timers for motor control, two general-purpose 32-bit timers. They also feature standard and advanced communication interfaces.

- Up to three I²Cs
- Six SPIs, two I²Ss full duplex. To achieve audio class accuracy, the I²S peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
- Four USARTs plus four UARTs
- An USB OTG full-speed and a USB OTG high-speed with full-speed capability (with the ULPI),
- Two CANs
- One SAI serial audio interface
- An SDIO/MMC interface
- Ethernet and camera interface
- LCD-TFT display controller
- Chrom-ART Accelerator™.

Advanced peripherals include an SDIO, a flexible memory control (FMC) interface, a camera interface for CMOS sensors. Refer to [Table 2: STM32F427xx and STM32F429xx features and peripheral counts](#) for the list of peripherals available on each part number.

The STM32F427xx and STM32F429xx devices operate in the –40 to +105 °C temperature range from a 1.7 to 3.6 V power supply.

The supply voltage can drop to 1.7 V with the use of an external power supply supervisor (refer to [Section 3.17.2: Internal reset OFF](#)). A comprehensive set of power-saving mode allows the design of low-power applications.

The STM32F427xx and STM32F429xx devices offer devices in 8 packages ranging from 100 pins to 216 pins. The set of included peripherals changes with the device chosen.

3 Functional overview

3.1 Arm® Cortex®-M4 with FPU and embedded Flash and SRAM

The Arm® Cortex®-M4 with FPU processor is the latest generation of Arm processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The Arm® Cortex®-M4 with FPU core is a 32-bit RISC processor that features exceptional code-efficiency, delivering the high-performance expected from an Arm core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

The STM32F42x family is compatible with all Arm tools and software.

Figure 4 shows the general block diagram of the STM32F42x family.

Note: Cortex-M4 with FPU core is binary compatible with the Cortex-M3 core.

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard Arm® Cortex®-M4 with FPU processors. It balances the inherent performance advantage of the Arm® Cortex®-M4 with FPU over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor full 225 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 128-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART Accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 180 MHz.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.4 Embedded Flash memory

The devices embed a Flash memory of up to 2 Mbytes available for storing programs and data.

3.5 CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.6 Embedded SRAM

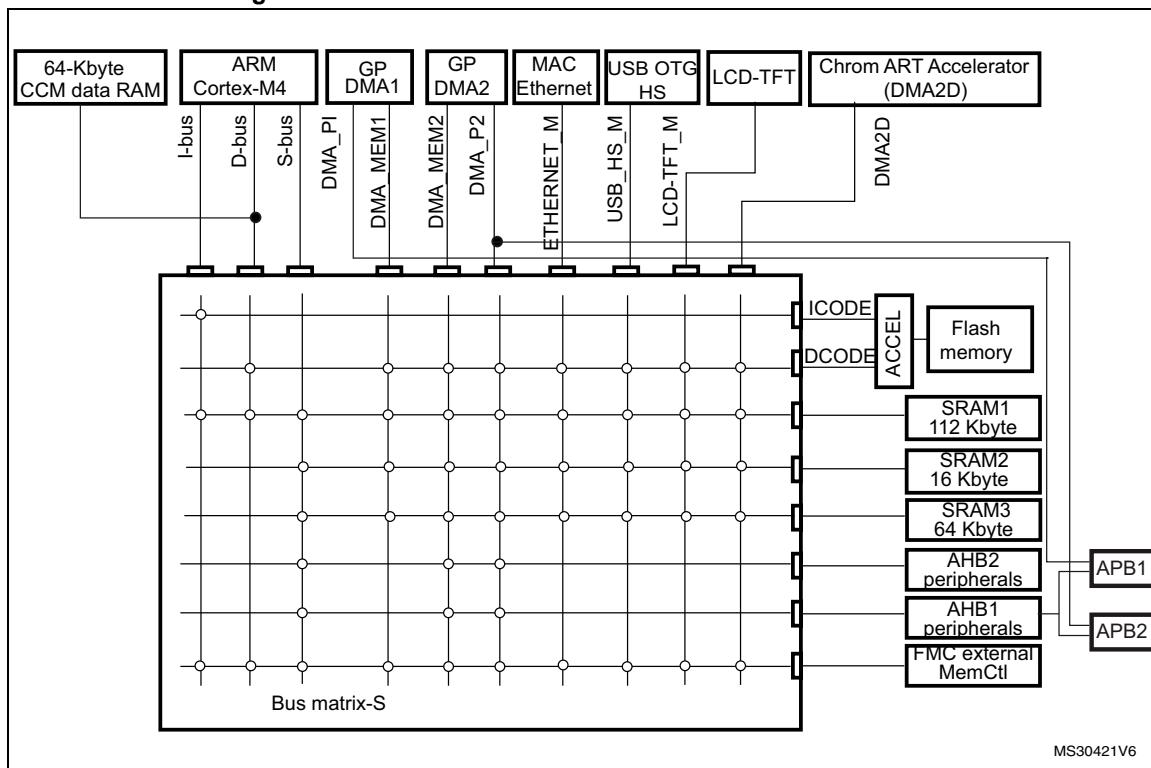
All devices embed:

- Up to 256Kbytes of system SRAM including 64 Kbytes of CCM (core coupled memory) data RAM
RAM memory is accessed (read/write) at CPU clock speed with 0 wait states.
- 4 Kbytes of backup SRAM
This area is accessible only from the CPU. Its content is protected against possible unwanted write accesses, and is retained in Standby or VBAT mode.

3.7 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs, Ethernet, USB HS, LCD-TFT, and DMA2D) and the slaves (Flash memory, RAM, FMC, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 5. STM32F427xx and STM32F429xx Multi-AHB matrix



3.8 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals:

- SPI and I²S
- I²C
- USART
- General-purpose, basic and advanced-control timers TIMx
- DAC
- SDIO
- Camera interface (DCMI)
- ADC
- SAI1.

3.9 Flexible memory controller (FMC)

All devices embed an FMC. It has four Chip Select outputs supporting the following modes: PCCard/Compact Flash, SDRAM/LPSDR SDRAM, SRAM, PSRAM, NOR Flash and NAND Flash.

Functionality overview:

- 8-,16-, 32-bit data bus width
- Read FIFO for SDRAM controller
- Write FIFO
- Maximum FMC_CLK/FMC_SDCLK frequency for synchronous accesses is 90 MHz.

LCD parallel interface

The FMC can be configured to interface seamlessly with most graphic LCD controllers. It supports the Intel 8080 and Motorola 6800 modes, and is flexible enough to adapt to specific LCD interfaces. This LCD parallel interface capability makes it easy to build cost-effective graphic applications using LCD modules with embedded controllers or high performance solutions using external controllers with dedicated acceleration.

3.10 LCD-TFT controller (available only on STM32F429xx)

The LCD-TFT display controller provides a 24-bit parallel digital RGB (Red, Green, Blue) and delivers all signals to interface directly to a broad range of LCD and TFT panels up to XGA (1024x768) resolution with the following features:

- 2 displays layers with dedicated FIFO (64x32-bit)
- Color Look-Up table (CLUT) up to 256 colors (256x24-bit) per layer
- Up to 8 Input color formats selectable per layer
- Flexible blending between two layers using alpha value (per pixel or constant)
- Flexible programmable parameters for each layer
- Color keying (transparency color)
- Up to 4 programmable interrupt events.

3.11 Chrom-ART Accelerator™ (DMA2D)

The Chrom-Art Accelerator™ (DMA2D) is a graphic accelerator which offers advanced bit blitting, row data copy and pixel format conversion. It supports the following functions:

- Rectangle filling with a fixed color
- Rectangle copy
- Rectangle copy with pixel format conversion
- Rectangle composition with blending and pixel format conversion.

Various image format coding are supported, from indirect 4bpp color mode up to 32bpp direct color. It embeds dedicated memory to store color lookup tables.

An interrupt can be generated when an operation is complete or at a programmed watermark.

All the operations are fully automatized and are running independently from the CPU or the DMAs.

3.12 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 91 maskable interrupt channels plus the 16 interrupt lines of the Cortex®-M4 with FPU core.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

3.13 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 23 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 168 GPIOs can be connected to the 16 external interrupt lines.

3.14 Clocks and startup

On reset the 16 MHz internal RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy over the full temperature range. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock can be monitored for failure. If a failure is

6 Electrical characteristics

6.1 Parameter conditions

Unless otherwise specified, all voltages are referenced to V_{SS}.

6.1.1 Minimum and maximum values

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by tests in production on 100% of the devices with an ambient temperature at T_A = 25 °C and T_A = T_{Amax} (given by the selected temperature range).

Data based on characterization results, design simulation and/or technology characteristics are indicated in the table footnotes and are not tested in production. Based on characterization, the minimum and maximum values refer to sample tests and represent the mean value plus or minus three times the standard deviation (mean±3σ).

6.1.2 Typical values

Unless otherwise specified, typical data are based on T_A = 25 °C, V_{DD} = 3.3 V (for the 1.7 V ≤ V_{DD} ≤ 3.6 V voltage range). They are given only as design guidelines and are not tested.

Typical ADC accuracy values are determined by characterization of a batch of samples from a standard diffusion lot over the full temperature range, where 95% of the devices have an error less than or equal to the value indicated (mean±2σ).

6.1.3 Typical curves

Unless otherwise specified, all typical curves are given only as design guidelines and are not tested.

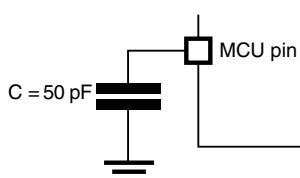
6.1.4 Loading capacitor

The loading conditions used for pin parameter measurement are shown in [Figure 20](#).

6.1.5 Pin input voltage

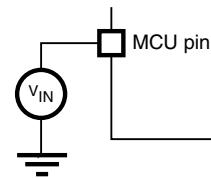
The input voltage measurement on a pin of the device is described in [Figure 21](#).

Figure 20. Pin loading conditions



MS19011V2

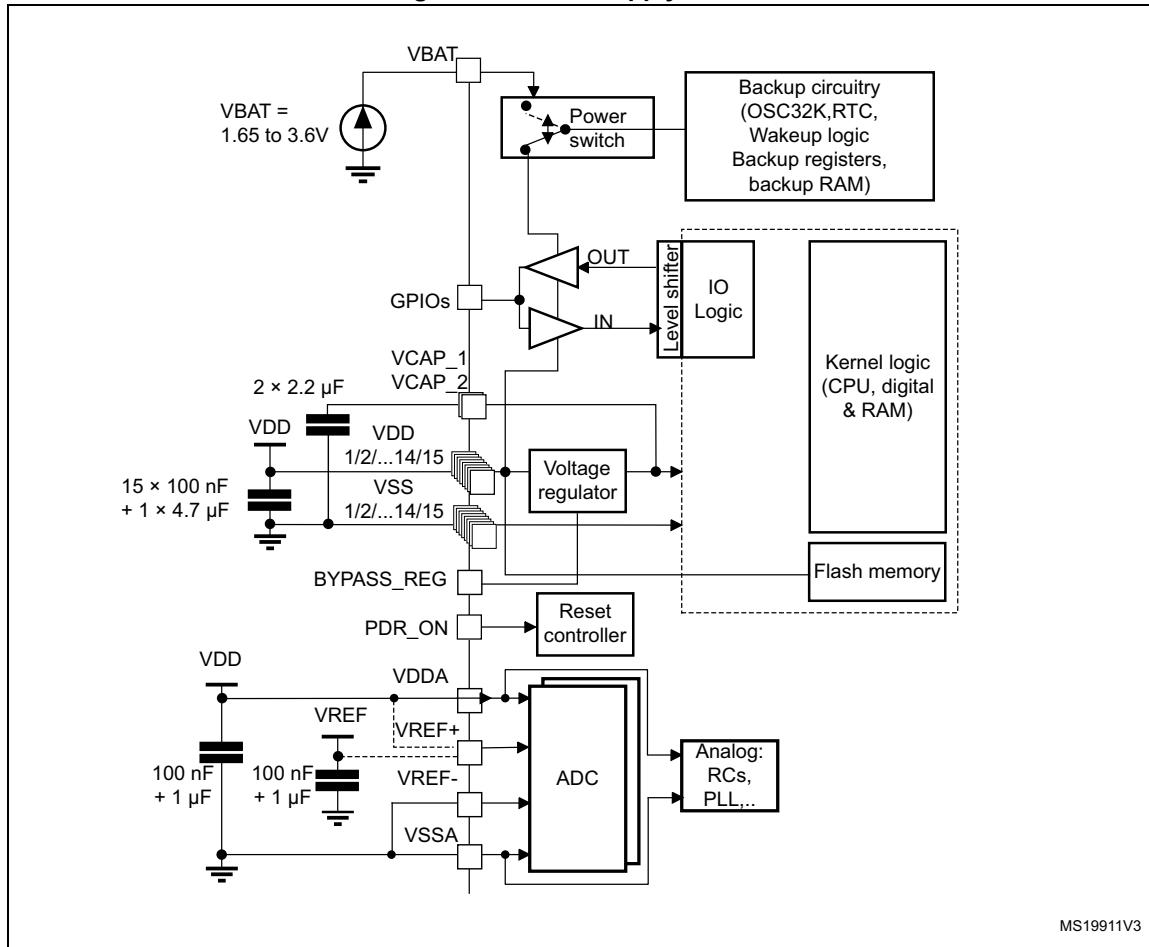
Figure 21. Pin input voltage



MS19010V2

6.1.6 Power supply scheme

Figure 22. Power supply scheme

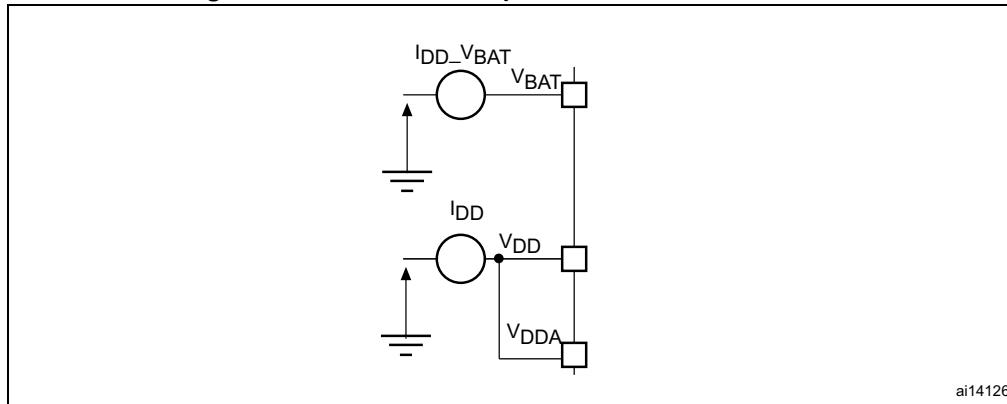


1. To connect BYPASS_REG and PDR_ON pins, refer to [Section 3.17: Power supply supervisor](#) and [Section 3.18: Voltage regulator](#)
2. The two 2.2 μ F ceramic capacitors should be replaced by two 100 nF decoupling capacitors when the voltage regulator is OFF.
3. The 4.7 μ F ceramic capacitor must be connected to one of the V_{DD} pin.
4. V_{DDA}=V_{DD} and V_{SSA}=V_{SS}.

Caution: Each power supply pair (V_{DD}/V_{SS}, V_{DDA}/V_{SSA} ...) must be decoupled with filtering ceramic capacitors as shown above. These capacitors must be placed as close as possible to, or below, the appropriate pins on the underside of the PCB to ensure good operation of the device. It is not recommended to remove filtering capacitors to reduce PCB size or cost. This might cause incorrect operation of the device.

6.1.7 Current consumption measurement

Figure 23. Current consumption measurement scheme



6.2 Absolute maximum ratings

Stresses above the absolute maximum ratings listed in [Table 14: Voltage characteristics](#), [Table 15: Current characteristics](#), and [Table 16: Thermal characteristics](#) may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these conditions is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

Device mission profile (application conditions) is compliant with JEDEC JESD47 Qualification Standard, extended mission profiles are available on demand.

Table 14. Voltage characteristics

Symbol	Ratings	Min	Max	Unit
$V_{DD}-V_{SS}$	External main supply voltage (including V_{DDA} , V_{DD} and V_{BAT}) ⁽¹⁾	- 0.3	4.0	
V_{IN}	Input voltage on FT pins ⁽²⁾	$V_{SS} - 0.3$	$V_{DD} + 4.0$	V
	Input voltage on TTa pins	$V_{SS} - 0.3$	4.0	
	Input voltage on any other pin	$V_{SS} - 0.3$	4.0	
	Input voltage on BOOT0 pin	V_{SS}	9.0	
$ \Delta V_{DDx} $	Variations between different V_{DD} power pins	-	50	
$ V_{SSx} - V_{SSL} $	Variations between all the different ground pins including V_{REF-}	-	50	mV
$V_{ESD(HBM)}$	Electrostatic discharge voltage (human body model)	see Section 6.3.15: Absolute maximum ratings (electrical sensitivity)		

1. All main power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. V_{IN} maximum value must always be respected. Refer to [Table 15](#) for the values of the maximum allowed injected current.

Table 15. Current characteristics

Symbol	Ratings	Max.	Unit	
ΣI_{VDD}	Total current into sum of all V_{DD_x} power lines (source) ⁽¹⁾	270	mA	
ΣI_{VSS}	Total current out of sum of all V_{SS_x} ground lines (sink) ⁽¹⁾	- 270		
I_{VDD}	Maximum current into each V_{DD_x} power line (source) ⁽¹⁾	100		
I_{VSS}	Maximum current out of each V_{SS_x} ground line (sink) ⁽¹⁾	- 100		
I_{IO}	Output current sunk by any I/O and control pin	25		
	Output current sourced by any I/Os and control pin	- 25		
ΣI_{IO}	Total output current sunk by sum of all I/O and control pins ⁽²⁾	120		
	Total output current sourced by sum of all I/Os and control pins ⁽²⁾	- 120		
$I_{INJ(PIN)}$ ⁽³⁾	Injected current on FT pins ⁽⁴⁾	- 5/+0		
	Injected current on NRST and BOOT0 pins ⁽⁴⁾			
	Injected current on TTa pins ⁽⁵⁾	±5		
$\Sigma I_{INJ(PIN)}$ ⁽⁵⁾	Total injected current (sum of all I/O and control pins) ⁽⁶⁾	±25		

1. All main power (V_{DD} , V_{DDA}) and ground (V_{SS} , V_{SSA}) pins must always be connected to the external power supply, in the permitted range.
2. This current consumption must be correctly distributed over all I/Os and control pins. The total output current must not be sunk/sourced between two consecutive power supply pins referring to high pin count LQFP packages.
3. Negative injection disturbs the analog performance of the device. See note in [Section 6.3.21: 12-bit ADC characteristics](#).
4. Positive injection is not possible on these I/Os and does not occur for input voltages lower than the specified maximum value.
5. A positive injection is induced by $V_{IN} > V_{DDA}$ while a negative injection is induced by $V_{IN} < V_{SS}$. $I_{INJ(PIN)}$ must never be exceeded. Refer to [Table 14](#) for the values of the maximum allowed input voltage.
6. When several inputs are submitted to a current injection, the maximum $\Sigma I_{INJ(PIN)}$ is the absolute sum of the positive and negative injected currents (instantaneous values).

Table 16. Thermal characteristics

Symbol	Ratings	Value	Unit
T_{STG}	Storage temperature range	- 65 to +150	°C
T_J	Maximum junction temperature	125	°C

**a-Si TFT LCD Single Chip Driver
240RGBx320 Resolution and 262K color**

Specification

Version: V1.11
Document No.: ILI9341_DS_V1.11.pdf

ILI TECHNOLOGY CORP.

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Hsinchu Country 302 Taiwan R.O.C.
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1. Introduction

ILI9341 is a 262,144-color single-chip SOC driver for a-TFT liquid crystal display with resolution of 240RGBx320 dots, comprising a 720-channel source driver, a 320-channel gate driver, 172,800 bytes GRAM for graphic display data of 240RGBx320 dots, and power supply circuit.

ILI9341 supports parallel 8-/9-/16-/18-bit data bus MCU interface, 6-/16-/18-bit data bus RGB interface and 3-/4-line serial peripheral interface (SPI). The moving picture area can be specified in internal GRAM by window address function. The specified window area can be updated selectively, so that moving picture can be displayed simultaneously independent of still picture area.

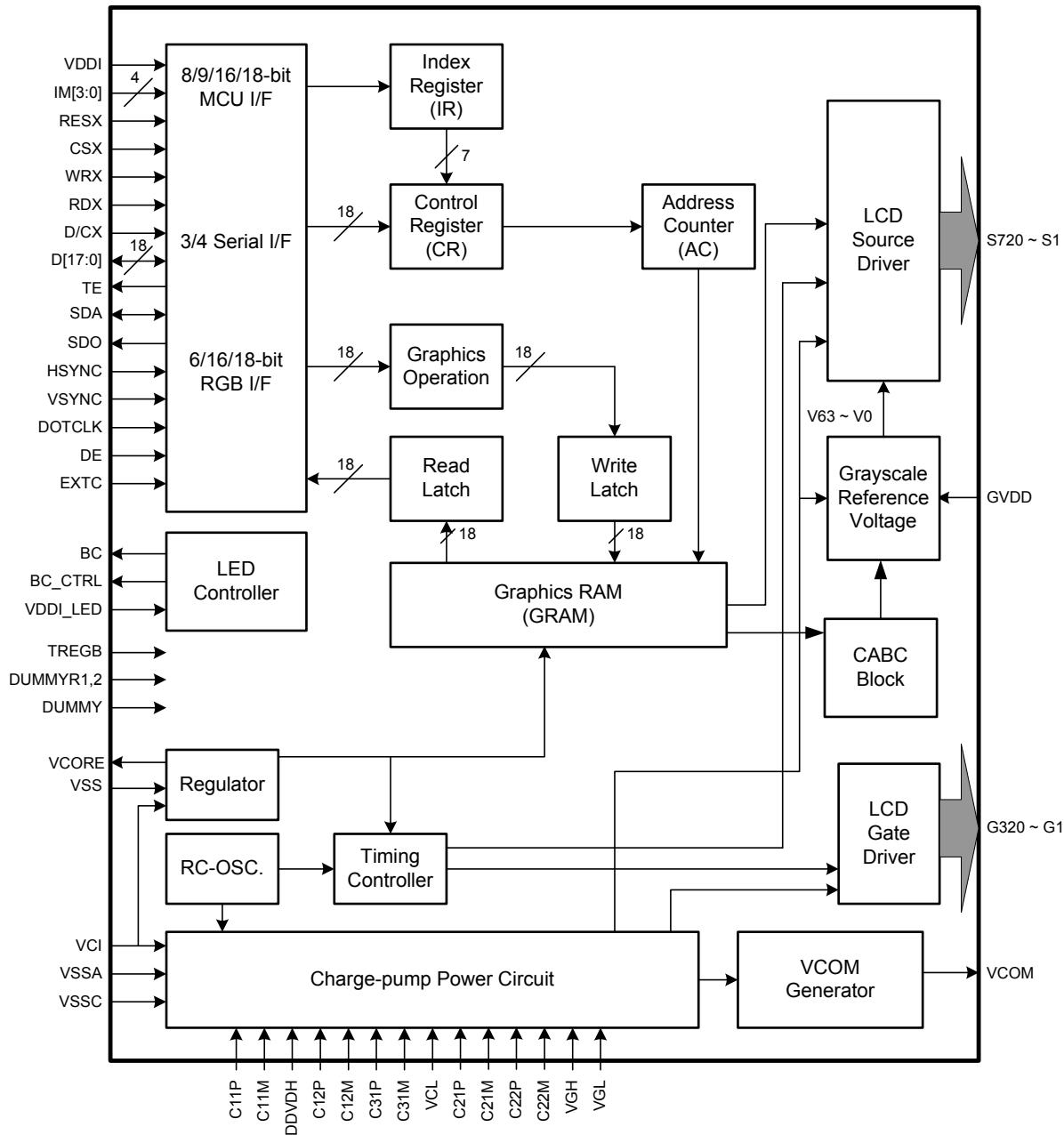
ILI9341 can operate with 1.65V ~ 3.3V I/O interface voltage and an incorporated voltage follower circuit to generate voltage levels for driving an LCD. ILI9341 supports full color, 8-color display mode and sleep mode for precise power control by software and these features make the ILI9341 an ideal LCD driver for medium or small size portable products such as digital cellular phones, smart phone, MP3 and PMP where long battery life is a major concern.

2. Features

- ◆ Display resolution: [240xRGB](H) x 320(V)
- ◆ Output:
 - 720 source outputs
 - 320 gate outputs
 - Common electrode output (VCOM)
- ◆ a-TFT LCD driver with on-chip full display RAM: 172,800 bytes
- ◆ System Interface
 - 8-bits, 9-bits, 16-bits, 18-bits interface with 8080- I /8080- II series MCU
 - 6-bits, 16-bits, 18-bits RGB interface with graphic controller
 - 3-line / 4-line serial interface
- ◆ Display mode:
 - Full color mode (Idle mode OFF): 262K-color (selectable color depth mode by software)
 - Reduce color mode (Idle mode ON): 8-color
- ◆ Power saving mode:
 - Sleep mode
- ◆ On chip functions:
 - VCOM generator and adjustment
 - Timing generator
 - Oscillator
 - DC/DC converter
 - Line/frame inversion
 - 1 preset Gamma curve with separate RGB Gamma correction
- ◆ Content Adaptive Brightness Control
- ◆ MTP (3 times):
 - 8-bits for ID1, ID2, ID3
 - 7-bits for VCOM adjustment

- ◆ Low -power consumption architecture
 - Low operating power supplies:
 - VDDI = 1.65V ~ 3.3V (logic)
 - **VCI = 2.5V ~ 3.3V** (analog)
 - LCD Voltage drive:
 - Source/VCOM power supply voltage
 - DDVDH - GND = 4.5V ~ 5.8V
 - VCL - GND = -1.5V ~ -2.5V
 - Gate driver output voltage
 - VGH - GND = 10.0V ~ 18.0V
 - VGL - GND = -5.0V ~ -10.0V
 - VGH - VGL \leq 28V
 - VCOM driver output voltage
 - VCOMH = 3.0V ~ (DDVDH – 0.2)V
 - VCOML = (VCL+0.2)V ~ 0V
 - VCOMH - VCOML \leq 6.0V
 - Operate temperature range: -40°C to 85°C
 - a-Si TFT LCD storage capacitor : Cst on Common structure only

3. Block Diagram



4. Pin Descriptions

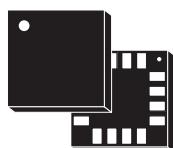
Power Supply Pins			
Pin Name	I/O	Type	Descriptions
VDDI	I	P	Low voltage power supply for interface logic circuits (1.65 ~ 3.3 V)
VDDI_LED	I		Power supply for LED driver interface. (1.65 ~ 3.3 V) If LED driver is not used, fix this pin at VDDI.
VCI	I	Analog Power	High voltage power supply for analog circuit blocks (2.5 ~ 3.3 V)
Vcore	O	Digital Power	Regulated Low voltage level for interface circuits Connect a capacitor for stabilization. Don't apply any external power to this pad
VSS3	I	I/O Ground	System ground level for I/O circuits.
VSS	I	Digital Ground	System ground level for logic blocks
VSSA	I	Analog Ground	System ground level for analog circuit blocks Connect to VSS on the FPC to prevent noise.
VSSC	I	Analog Ground	System ground level for analog circuit blocks Connect to VSS on the FPC to prevent noise

Interface Logic Signals																																																																																																		
Pin Name	I/O	Type	Descriptions																																																																																															
IM[3:0]	I	(VDDI/VSS)	Select the MCU interface mode																																																																																															
			<table border="1"> <thead> <tr> <th>IM3</th><th>IM2</th><th>IM1</th><th>IM0</th><th>MCU-Interface Mode</th><th>DB Pin in use</th><th></th></tr> <tr> <th>Register/Content</th><th></th><th></th><th></th><th></th><th>Register/Content</th><th>GRAM</th></tr> </thead> <tbody> <tr> <td>0</td><td>0</td><td>0</td><td>0</td><td>80 MCU 8-bit bus interface I</td><td>D[7:0]</td><td>D[7:0]</td></tr> <tr> <td>0</td><td>0</td><td>0</td><td>1</td><td>80 MCU 16-bit bus interface I</td><td>D[7:0]</td><td>D[15:0]</td></tr> <tr> <td>0</td><td>0</td><td>1</td><td>0</td><td>80 MCU 9-bit bus interface I</td><td>D[7:0]</td><td>D[8:0]</td></tr> <tr> <td>0</td><td>0</td><td>1</td><td>1</td><td>80 MCU 18-bit bus interface I</td><td>D[7:0]</td><td>D[17:0]</td></tr> <tr> <td>0</td><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data serial interface I</td><td colspan="2">SDA: In/OUT</td></tr> <tr> <td>0</td><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data serial interface I</td><td colspan="2">SDA: In/OUT</td></tr> <tr> <td>1</td><td>0</td><td>0</td><td>0</td><td>80 MCU 16-bit bus interface II</td><td>D[8:1]</td><td>D[17:10], D[8:1]</td></tr> <tr> <td>1</td><td>0</td><td>0</td><td>1</td><td>80 MCU 8-bit bus interface II</td><td>D[17:10]</td><td>D[17:10]</td></tr> <tr> <td>1</td><td>0</td><td>1</td><td>0</td><td>80 MCU 18-bit bus interface II</td><td>D[8:1]</td><td>D[17:0]</td></tr> <tr> <td>1</td><td>0</td><td>1</td><td>1</td><td>80 MCU 9-bit bus interface II</td><td>D[17:10]</td><td>D[17:9]</td></tr> <tr> <td>1</td><td>1</td><td>0</td><td>1</td><td>3-wire 9-bit data serial interface II</td><td colspan="2">SDI: In SDO: Out</td></tr> <tr> <td>1</td><td>1</td><td>1</td><td>0</td><td>4-wire 8-bit data serial interface II</td><td colspan="2">SDI: In SDO: Out</td></tr> </tbody> </table>	IM3	IM2	IM1	IM0	MCU-Interface Mode	DB Pin in use		Register/Content					Register/Content	GRAM	0	0	0	0	80 MCU 8-bit bus interface I	D[7:0]	D[7:0]	0	0	0	1	80 MCU 16-bit bus interface I	D[7:0]	D[15:0]	0	0	1	0	80 MCU 9-bit bus interface I	D[7:0]	D[8:0]	0	0	1	1	80 MCU 18-bit bus interface I	D[7:0]	D[17:0]	0	1	0	1	3-wire 9-bit data serial interface I	SDA: In/OUT		0	1	1	0	4-wire 8-bit data serial interface I	SDA: In/OUT		1	0	0	0	80 MCU 16-bit bus interface II	D[8:1]	D[17:10], D[8:1]	1	0	0	1	80 MCU 8-bit bus interface II	D[17:10]	D[17:10]	1	0	1	0	80 MCU 18-bit bus interface II	D[8:1]	D[17:0]	1	0	1	1	80 MCU 9-bit bus interface II	D[17:10]	D[17:9]	1	1	0	1	3-wire 9-bit data serial interface II	SDI: In SDO: Out		1	1	1	0
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MPU Parallel interface bus and serial interface select																																																																																																		
If use RGB Interface must select serial interface.																																																																																																		
* : Fix this pin at VDDI or VSS.																																																																																																		

RESX	I	MCU (VDDI/VSS)	This signal will reset the device and must be applied to properly initialize the chip. Signal is active low.
EXTC	I	MCU (VDDI/VSS)	Extended command set enable. Low: extended command set is discarded. High: extended command set is accepted. Please connect EXTC to VDDI to read/write extended registers (RB0h~RCFh, RE0h~RFFh)
CSX	I	MCU (VDDI/VSS)	Chip select input pin ("Low" enable). This pin can be permanently fixed "Low" in MPU interface mode only. * note1,2
D/CX (SCL)	I	MCU (VDDI/VSS)	This pin is used to select "Data or Command" in the parallel interface or 4-wire 8-bit serial data interface. When DCX = '1', data is selected. When DCX = '0', command is selected. This pin is used serial interface clock in 3-wire 9-bit / 4-wire 8-bit serial data interface. If not used, this pin should be connected to VDDI or VSS.
RDX	I	MCU (VDDI/VSS)	8080- I /8080- II system (RDX): Serves as a read signal and MCU read data at the rising edge. Fix to VDDI level when not in use.
WRX (D/CX)	I	MCU (VDDI/VSS)	- 8080- I /8080- II system (WRX): Serves as a write signal and writes data at the rising edge. - 4-line system (D/CX): Serves as command or parameter select. Fix to VDDI level when not in use.
D[17:0]	I/O	MCU (VDDI/VSS)	18-bit parallel bi-directional data bus for MCU system and RGB interface mode Fix to VSS level when not in use
SDI/SDA	I/O	MCU (VDDI/VSS)	When IM[3] : Low, Serial in/out signal. When IM[3] : High, Serial input signal. The data is applied on the rising edge of the SCL signal. If not used, fix this pin at VDDI or VSS.
SDO	O	MCU (VDDI/VSS)	Serial output signal. The data is outputted on the falling edge of the SCL signal. If not used, open this pin
TE	O	MCU (VDDI/VSS)	Tearing effect output pin to synchronize MPU to frame writing, activated by S/W command. When this pin is not activated, this pin is low. If not used, open this pin.
DOTCLK	I	MCU (VDDI/VSS)	Dot clock signal for RGB interface operation. Fix to VDDI or VSS level when not in use.
VSYNC	I	MCU (VDDI/VSS)	Frame synchronizing signal for RGB interface operation. Fix to VDDI or VSS level when not in use.
HSYNC	I	MCU (VDDI/VSS)	Line synchronizing signal for RGB interface operation. Fix to VDDI or VSS level when not in use.
DE	I	MCU (VDDI/VSS)	Data enable signal for RGB interface operation. Fix to VDDI or VSS level when not in use.

MEMS motion sensor: three-axis digital output gyroscope

Datasheet - production data



LGA-16 (4x4x1 mm)

Features

- Three selectable full scales (250/500/2000 dps)
- I²C/SPI digital output interface
- 16 bit-rate value data output
- 8-bit temperature data output
- Two digital output lines (interrupt and data ready)
- Integrated low- and high-pass filters with user-selectable bandwidth
- Wide supply voltage: 2.4 V to 3.6 V
- Low voltage-compatible IOs (1.8 V)
- Embedded power-down and sleep mode
- Embedded temperature sensor
- Embedded FIFO
- High shock survivability
- Extended operating temperature range (-40 °C to +85 °C)
- ECOPACK® RoHS and “Green” compliant

Applications

- Gaming and virtual reality input devices
- Motion control with MMI (man-machine interface)
- GPS navigation systems
- Appliances and robotics

Description

The L3GD20 is a low-power three-axis angular rate sensor.

It includes a sensing element and an IC interface capable of providing the measured angular rate to the external world through a digital interface (I²C/SPI).

The sensing element is manufactured using a dedicated micro-machining process developed by STMicroelectronics to produce inertial sensors and actuators on silicon wafers.

The IC interface is manufactured using a CMOS process that allows a high level of integration to design a dedicated circuit which is trimmed to better match the sensing element characteristics. The L3GD20 has a full scale of ±250/±500/ ±2000 dps and is capable of measuring rates with a user-selectable bandwidth.

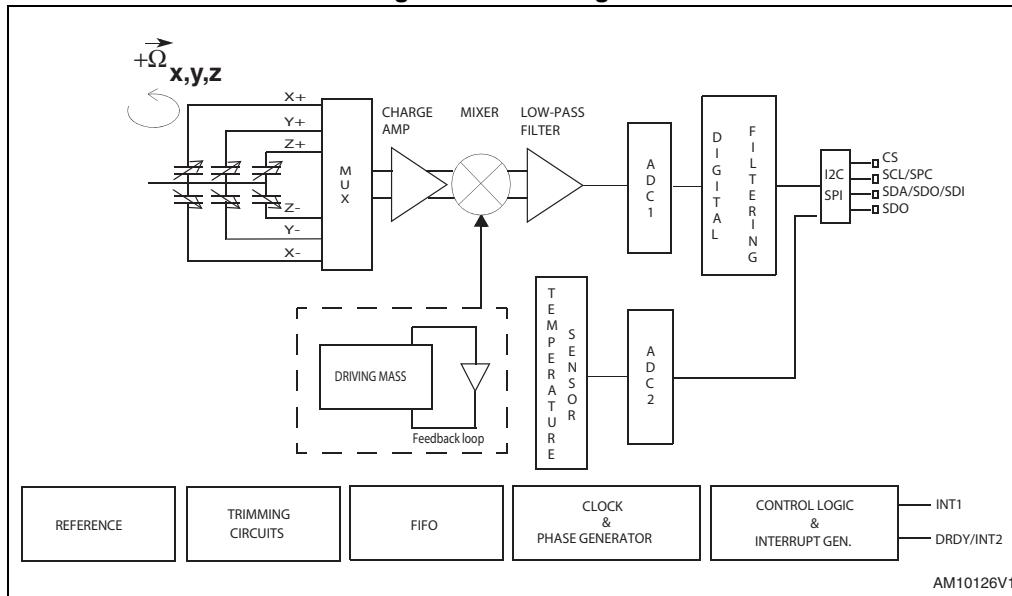
The L3GD20 is available in a plastic land grid array (LGA) package and can operate within a temperature range of -40 °C to +85 °C.

Table 1. Device summary

Order code	Temperature range (°C)	Package	Packing
L3GD20	-40 to +85	LGA-16 (4x4x1 mm)	Tray
L3GD20TR	-40 to +85	LGA-16 (4x4x1 mm)	Tape and reel

1 Block diagram and pin description

Figure 1. Block diagram



Note: The vibration of the structure is maintained by drive circuitry in a feedback loop. The sensing signal is filtered and appears as a digital signal at the output.

1.1 Pin description

Figure 2. Pin connection

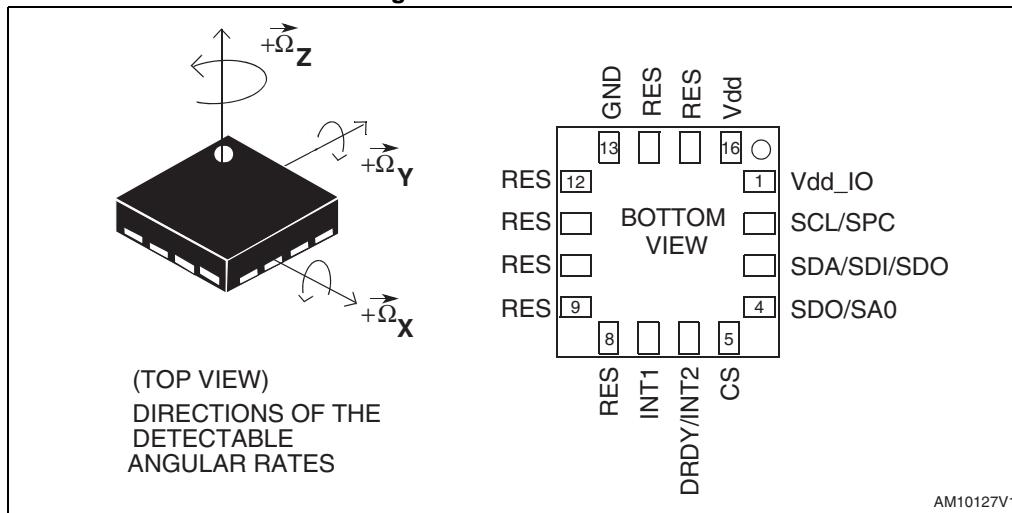


Table 2. Pin description**Table 3.**

Pin#	Name	Function
1	Vdd_IO ⁽¹⁾	Power supply for I/O pins
2	SCL SPC	I ² C serial clock (SCL) SPI serial port clock (SPC)
3	SDA SDI SDO	I ² C serial data (SDA) SPI serial data input (SDI) 3-wire interface serial data output (SDO)
4	SDO SA0	SPI serial data output (SDO) I ² C less significant bit of the device address (SA0)
5	CS	I ² C/SPI mode selection (1: SPI idle mode / I ² C communication enabled; 0: SPI communication mode / I ² C disabled)
6	DRDY/INT2	Data ready/FIFO interrupt (Watermark/Overrun/Empty)
7	INT1	Programmable interrupt
8	Reserved	Connect to GND
9	Reserved	Connect to GND
10	Reserved	Connect to GND
11	Reserved	Connect to GND
12	Reserved	Connect to GND
13	GND	0 V supply
14	Reserved	Connect to GND with ceramic capacitor ⁽²⁾
15	Reserved	Connect to Vdd
16	Vdd ⁽³⁾	Power supply

1. 100 nF filter capacitor recommended.
2. 1 nF min value must be guaranteed under 11 V bias condition.
3. 100 nF plus 10 μ F capacitors recommended.

2.2 Electrical characteristics

@ Vdd =3.0 V, T=25 °C unless otherwise noted.

Table 5. Electrical characteristics (1)

Symbol	Parameter	Test condition	Min.	Typ. ⁽²⁾	Max.	Unit
Vdd	Supply voltage		2.4	3.0	3.6	V
Vdd_IO	I/O pins supply voltage ⁽³⁾		1.71		Vdd+0.1	V
Idd	Supply current			6.1		mA
IddSL	Supply current in sleep mode ⁽⁴⁾	Selectable by digital interface		2		mA
IddPdn	Supply current in power-down mode	Selectable by digital interface		5		µA
VIH	Digital high level input voltage		0.8*Vdd_I_O			V
VIL	Digital low level input voltage				0.2*Vdd_I_O	V
Top	Operating temperature range		-40		+85	°C

1. The product is factory calibrated at 3.0 V.
2. Typical specifications are not guaranteed.
3. It is possible to remove Vdd maintaining Vdd_IO without blocking the communication busses; in this condition the measurement chain is powered off.
4. Sleep mode introduces a faster turn-on time relative to power-down mode.

2.3 Temperature sensor characteristics

@ Vdd =3.0 V, T=25 °C unless otherwise noted.

Table 6. Electrical characteristics (1)

Symbol	Parameter	Test condition	Min.	Typ. ⁽²⁾	Max.	Unit
TSDr	Temperature sensor output change vs. temperature	-		-1		°C/digit
TODR	Temperature refresh rate			1		Hz
Top	Operating temperature range		-40		+85	°C

1. The product is factory calibrated at 3.0 V.
2. Typical specifications are not guaranteed.

7 Register description

The device contains a set of registers which are used to control its behavior and to retrieve angular rate data. The register address, consisting of 7 bits, is used to identify them and to write the data through the serial interface.

7.1 WHO_AM_I (0Fh)

Table 18. WHO_AM_I register

1	1	0	1	0	1	0	0
---	---	---	---	---	---	---	---

Device identification register.

7.2 CTRL_REG1 (20h)

Table 19. CTRL_REG1 register

DR1	DR0	BW1	BW0	PD	Zen	Xen	Yen
-----	-----	-----	-----	----	-----	-----	-----

Table 20. CTRL_REG1 description

DR1-DR0	Output data rate selection. Refer to Table 21
BW1-BW0	Bandwidth selection. Refer to Table 21
PD	Power-down mode enable. Default value: 0 (0: power-down mode, 1: normal mode or sleep mode)
Zen	Z axis enable. Default value: 1 (0: Z axis disabled; 1: Z axis enabled)
Yen	Y axis enable. Default value: 1 (0: Y axis disabled; 1: Y axis enabled)
Xen	X axis enable. Default value: 1 (0: X axis disabled; 1: X axis enabled)

DR<1:0> is used for ODR selection. **BW <1:0>** is used for Bandwidth selection.

In the [Table 21](#) all frequencies resulting in combinations of DR / BW bits are reported.

Table 21. DR and BW configuration setting

DR <1:0>	BW <1:0>	ODR [Hz]	Cut-Off
00	00	95	12.5
00	01	95	25
00	10	95	25

Table 21. DR and BW configuration setting (continued)

DR <1:0>	BW <1:0>	ODR [Hz]	Cut-Off
00	11	95	25
01	00	190	12.5
01	01	190	25
01	10	190	50
01	11	190	70
10	00	380	20
10	01	380	25
10	10	380	50
10	11	380	100
11	00	760	30
11	01	760	35
11	10	760	50
11	11	760	100

A combination of **PD**, **Zen**, **Yen**, **Xen** is used to set device to different modes (power-down / normal / sleep mode) in accordance with [Table 22](#) below.

Table 22. Power mode selection configuration

Mode	PD	Zen	Yen	Xen
Power-down	0	-	-	-
Sleep	1	0	0	0
Normal	1	-	-	-

7.3 CTRL_REG2 (21h)

Table 23. CTRL_REG2 register

0 ⁽¹⁾	0 ⁽¹⁾	HPM1	HPM0	HPCF3	HPCF2	HPCF1	HPCF0
------------------	------------------	------	------	-------	-------	-------	-------

- These bits must be set to '0' to ensure proper operation of the device

Table 24. CTRL_REG2 description

HPM1- HPM0	High-pass filter mode selection. Default value: 00 Refer to Table 25
HPCF3- HPCF0	High-pass filter cutoff frequency selection Refer to Table 26

Table 25. High-pass filter mode configuration

HPM1	HPM0	High-pass filter mode
0	0	Normal mode (reset reading HP_RESET_FILTER)
0	1	Reference signal for filtering
1	0	Normal mode
1	1	Autoreset on interrupt event

Table 26. High-pass filter cut off frequency configuration [Hz]

HPCF3-0	ODR=95 Hz	ODR=190 Hz	ODR=380 Hz	ODR=760 Hz
0000	7.2	13.5	27	51.4
0001	3.5	7.2	13.5	27
0010	1.8	3.5	7.2	13.5
0011	0.9	1.8	3.5	7.2
0100	0.45	0.9	1.8	3.5
0101	0.18	0.45	0.9	1.8
0110	0.09	0.18	0.45	0.9
0111	0.045	0.09	0.18	0.45
1000	0.018	0.045	0.09	0.18
1001	0.009	0.018	0.045	0.09

7.4 CTRL_REG3 (22h)

Table 27. CTRL_REG1 register

I1_Int1	I1_Boot	H_Lactive	PP_OD	I2_DRDY	I2_WTM	I2_ORun	I2_Empty
---------	---------	-----------	-------	---------	--------	---------	----------

Table 28. CTRL_REG3 description

I1_Int1	Interrupt enable on INT1 pin. Default value 0. (0: disable; 1: enable)
I1_Boot	Boot status available on INT1. Default value 0. (0: disable; 1: enable)
H_Lactive	Interrupt active configuration on INT1. Default value 0. (0: high; 1:low)
PP_OD	Push-pull / Open drain. Default value: 0. (0: push-pull; 1: open drain)
I2_DRDY	Date-ready on DRDY/INT2. Default value 0. (0: disable; 1: enable)
I2_WTM	FIFO watermark interrupt on DRDY/INT2. Default value: 0. (0: disable; 1: enable)
I2_ORun	FIFO overrun interrupt on DRDY/INT2. Default value: 0. (0: disable; 1: enable)
I2_Empty	FIFO empty interrupt on DRDY/INT2. Default value: 0. (0: disable; 1: enable)

7.5 CTRL_REG4 (23h)

Table 29. CTRL_REG4 register

BDU	BLE	FS1	FS0	-	0 ⁽¹⁾	0 ⁽¹⁾	SIM
-----	-----	-----	-----	---	------------------	------------------	-----

1. This value must not be changed.

Table 30. CTRL_REG4 description

BDU	Block data update. Default value: 0 (0: continuos update; 1: output registers not updated until MSb and LSb reading)
BLE	Big/little endian data selection. Default value 0. (0: Data LSb @ lower address; 1: Data MSb @ lower address)
FS1-FS0	Full scale selection. Default value: 00 (00: 250 dps; 01: 500 dps; 10: 2000 dps; 11: 2000 dps)
SIM	SPI serial interface mode selection. Default value: 0 (0: 4-wire interface; 1: 3-wire interface).

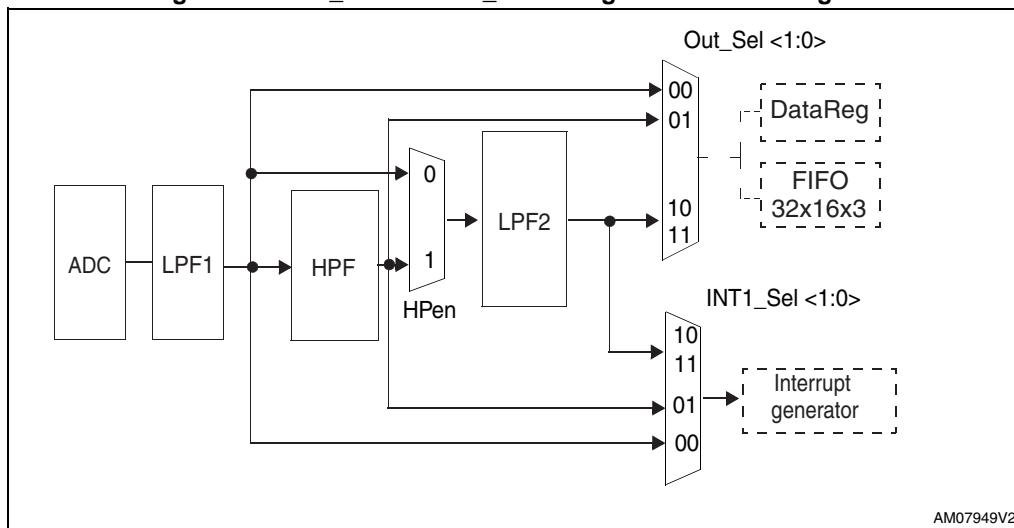
7.6 CTRL_REG5 (24h)

Table 31. CTRL_REG5 register

BOOT	FIFO_EN	--	HPen	INT1_Sel1	INT1_Sel0	Out_Sel1	Out_Sel0
------	---------	----	------	-----------	-----------	----------	----------

Table 32. CTRL_REG5 description

BOOT	Reboot memory content. Default value: 0 (0: normal mode; 1: reboot memory content)
FIFO_EN	FIFO enable. Default value: 0 (0: FIFO disable; 1: FIFO Enable)
HPen	High-pass filter enable. Default value: 0 (0: HPF disabled; 1: HPF enabled See Figure 20)
INT1_Sel1-INT1_Sel0	INT1 selection configuration. Default value: 0 (See Figure 20)
Out_Sel1-Out_Sel0	Out selection configuration. Default value: 0 (See Figure 20)

Figure 18. INT1_Sel and Out_Sel configuration block diagram

7.7 REFERENCE/DATACAPTURE (25h)

Table 33. REFERENCE register

Ref7	Ref6	Ref5	Ref4	Ref3	Ref2	Ref1	Ref0
------	------	------	------	------	------	------	------

Table 34. REFERENCE register description

Ref 7-Ref0	Reference value for interrupt generation. Default value: 0
------------	--

7.8 OUT_TEMP (26h)

Table 35. OUT_TEMP register

Temp7	Temp6	Temp5	Temp4	Temp3	Temp2	Temp1	Temp0
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Table 36. OUT_TEMP register description

Temp7-Temp0	Temperature data
-------------	------------------

Temperature data (1LSB/deg - 8-bit resolution). The value is expressed as two's complement.

7.9 STATUS_REG (27h)

Table 37. STATUS_REG register

ZYXOR	ZOR	YOR	XOR	ZYXDA	ZDA	YDA	XDA
-------	-----	-----	-----	-------	-----	-----	-----

Table 38. STATUS_REG description

ZYXOR	X, Y, Z -axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data has overwritten the previous data before it was read)
ZOR	Z axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Z-axis has overwritten the previous data)
YOR	Y axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the Y-axis has overwritten the previous data)
XOR	X axis data overrun. Default value: 0 (0: no overrun has occurred; 1: new data for the X-axis has overwritten the previous data)
ZYXDA	X, Y, Z -axis new data available. Default value: 0 (0: a new set of data is not yet available; 1: a new set of data is available)
ZDA	Z axis new data available. Default value: 0 (0: new data for the Z-axis is not yet available; 1: new data for the Z-axis is available)
YDA	Y axis new data available. Default value: 0 (0: new data for the Y-axis is not yet available; 1: new data for the Y-axis is available)
XDA	X axis new data available. Default value: 0 (0: new data for the X-axis is not yet available; 1: new data for the X-axis is available)

7.10 OUT_X_L (28h), OUT_X_H (29h)

X-axis angular rate data. The value is expressed as two's complement.

7.11 OUT_Y_L (2Ah), OUT_Y_H (2Bh)

Y-axis angular rate data. The value is expressed as two's complement.

7.12 OUT_Z_L (2Ch), OUT_Z_H (2Dh)

Z-axis angular rate data. The value is expressed as two's complement.

7.13 FIFO_CTRL_REG (2Eh)

Table 39. REFERENCE register

FM2	FM1	FM0	WTM4	WTM3	WTM2	WTM1	WTM0
-----	-----	-----	------	------	------	------	------

Table 40. REFERENCE register description

FM2-FM0	FIFO mode selection. Default value: 00 (see Table 41)
WTM4-WTM0	FIFO threshold. Watermark level setting

Table 41. FIFO mode configuration

FM2	FM1	FM0	FIFO mode
0	0	0	Bypass mode
0	0	1	FIFO mode
0	1	0	Stream mode
0	1	1	Stream-to-FIFO mode
1	0	0	Bypass-to-Stream mode

7.14 FIFO_SRC_REG (2Fh)

Table 42. FIFO_SRC register

WTM	OVRN	EMPTY	FSS4	FSS3	FSS2	FSS1	FSS0
-----	------	-------	------	------	------	------	------

Table 43. FIFO_SRC register description

WTM	Watermark status. (0: FIFO filling is lower than WTM level; 1: FIFO filling is equal or higher than WTM level)
OVRN	Overrun bit status. (0: FIFO is not completely filled; 1:FIFO is completely filled)
EMPTY	FIFO empty bit. (0: FIFO not empty; 1: FIFO empty)
FSS4-FSS1	FIFO stored data level

7.15 INT1_CFG (30h)

Table 44. INT1_CFG register

AND/OR	LIR	ZHIE	ZLIE	YHIE	YLIE	XHIE	XLIE
--------	-----	------	------	------	------	------	------

Table 45. INT1_CFG description

AND/OR	AND/OR combination of interrupt events. Default value: 0 (0: OR combination of interrupt events 1: AND combination of interrupt events)
LIR	Latch interrupt request. Default value: 0 (0: interrupt request not latched; 1: interrupt request latched) Cleared by reading INT1_SRC reg.
ZHIE	Enable interrupt generation on Z high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value higher than preset threshold)
ZLIE	Enable interrupt generation on Z low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value lower than preset threshold)
YHIE	Enable interrupt generation on Y high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value higher than preset threshold)
YLIE	Enable interrupt generation on Y low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value lower than preset threshold)
XHIE	Enable interrupt generation on X high event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value higher than preset threshold)
XLIE	Enable interrupt generation on X low event. Default value: 0 (0: disable interrupt request; 1: enable interrupt request on measured value lower than preset threshold)

7.16 INT1_SRC (31h)

Interrupt source register. Read only register.

Table 46. INT1_SRC register

0	IA	ZH	ZL	YH	YL	XH	XL
---	----	----	----	----	----	----	----

Table 47. INT1_SRC description

IA	Interrupt active. Default value: 0 (0: no interrupt has been generated; 1: one or more interrupts have been generated)
ZH	Z high. Default value: 0 (0: no interrupt, 1: Z high event has occurred)
ZL	Z low. Default value: 0 (0: no interrupt; 1: Z low event has occurred)
YH	Y high. Default value: 0 (0: no interrupt, 1: Y high event has occurred)
YL	Y low. Default value: 0 (0: no interrupt, 1: Y low event has occurred)
XH	X high. Default value: 0 (0: no interrupt, 1: X High event has occurred)
XL	X low. Default value: 0 (0: no interrupt, 1: X Low event has occurred)

Reading at this address clears INT1_SRC IA bit (and eventually the interrupt signal on the INT1 pin) and allows the refresh of data in the INT1_SRC register if the latched option was chosen.

7.17 INT1_THS_XH (32h)

Table 48. INT1_THS_XH register

-	THSX14	THSX13	THSX12	THSX11	THSX10	THSX9	THSX8
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Table 49. INT1_THS_XH description

THSX14 - THSX9	Interrupt threshold. Default value: 0000 0000
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7.18 INT1_THS_XL (33h)

Table 50. INT1_THS_XL register

THSX7	THSX6	THSX5	THSX4	THSX3	THSX2	THSX1	THSX0
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Table 51. INT1_THS_XL description

THSX7 - THSX0	Interrupt threshold. Default value: 0000 0000
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7.19 INT1_THS_YH (34h)

Table 52. INT1_THS_YH register

-	THSY14	THSY13	THSY12	THSY11	THSY10	THSY9	THSY8
---	--------	--------	--------	--------	--------	-------	-------

Table 53. INT1_THS_YH description

THSY14 - THSY9	Interrupt threshold. Default value: 0000 0000
----------------	---

7.20 INT1_THS_YL (35h)

Table 54. INT1_THS_YL register

THSY7	THSY6	THSY5	THSY4	THSY3	THSY2	THSY1	THSY0
-------	-------	-------	-------	-------	-------	-------	-------

Table 55. INT1_THS_YL description

THSY7 - THSY0	Interrupt threshold. Default value: 0000 0000
---------------	---

7.21 INT1_THS_ZH (36h)

Table 56. INT1_THS_ZH register

-	THSZ14	THSZ13	THSZ12	THSZ11	THSZ10	THSZ9	THSZ8
---	--------	--------	--------	--------	--------	-------	-------

Table 57. INT1_THS_ZH description

THSZ14 - THSZ9	Interrupt threshold. Default value: 0000 0000
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7.22 INT1_THS_ZL (37h)

Table 58. INT1_THS_ZL register

THSZ7	THSZ6	THSZ5	THSZ4	THSZ3	THSZ2	THSZ1	THSZ0
-------	-------	-------	-------	-------	-------	-------	-------

Table 59. INT1_THS_ZL description

THSZ7 - THSZ0	Interrupt threshold. Default value: 0000 0000
---------------	---

7.23 INT1_DURATION (38h)

Table 60. INT1_DURATION register

WAIT	D6	D5	D4	D3	D2	D1	D0
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Table 61. INT1_DURATION description

WAIT	WAIT enable. Default value: 0 (0: disable; 1: enable)
D6 - D0	Duration value. Default value: 000 0000

The **D6 - D0** bits set the minimum duration of the interrupt event to be recognized. Duration steps and maximum values depend on the ODR chosen.

The **WAIT** bit has the following definitions:

Wait = '0': the interrupt falls immediately if the signal crosses the selected threshold

Wait = '1': if the signal crosses the selected threshold, the interrupt falls only after the duration has counted the number of samples at the selected data rate, written into the duration counter register.