NYCU-EE IC LAB – Fall 2023

Lab011 Exercise

Design: Matrix Multiplication with Systolic Array

Data Preparation

1. Extract files from TA's directory:
   % tar xvf ~iclabta01/Lab11.tar
2. The extracted LAB directory contains:
   a. Exercise/
   b. Practice/

Design Description

For this LAB, you just run the APR flow for LBP.

Input

| Input	Bit Width	Definition and Description
clk	1	Clock.
rst_n	1	Asynchronous active-low reset.
in_valid	1	High when input signals are valid.
in_valid2	1	High when input signals are valid.
matrix	1	Elements of input matrix and weight matrix.
matrix_size	2	The signal will determine the dimension of input matrix, weight matrix and output matrix.
i_mat_idx	1	Input matrix index, this signal will be given when **in_valid2** is high.
w_mat_idx	1	Weight matrix index, this signal will be given when **in_valid2** is high.

Output

Output	Bit Width	Definition and Description
out_valid	1	High when out_value is valid. It cannot be overlapped with **in_valid** and **in_valid2** signal.
out_value	1	It will output the length and value of the summation along **antidiagonal** direction of output matrix in sequence serially.

Specifications

1. Top module name: CHIP

2. The clock period is 10.0ns for RTL to gate-sim.

3. You can adjust your clock period by yourself, but the maximum period is **40 ns** (post sim).

4. The input delay is set to **0.5*(clock period)**.

5. The output delay is set to **0.5*(clock period)**, and the output loading is set to **0.05**.

6. The gate level simulation cannot include any timing violations without the *notimingcheck* command.

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7. Don't use any wire/reg/submodule/parameter name called *error*, *congratulation*, *latch* or *fail* otherwise you will fail the lab. Note: * means any char in front of or behind the word. e.g: error_note is forbidden.

8. Don't write Chinese comments or other language comments in the file you turned in.

Block Diagram
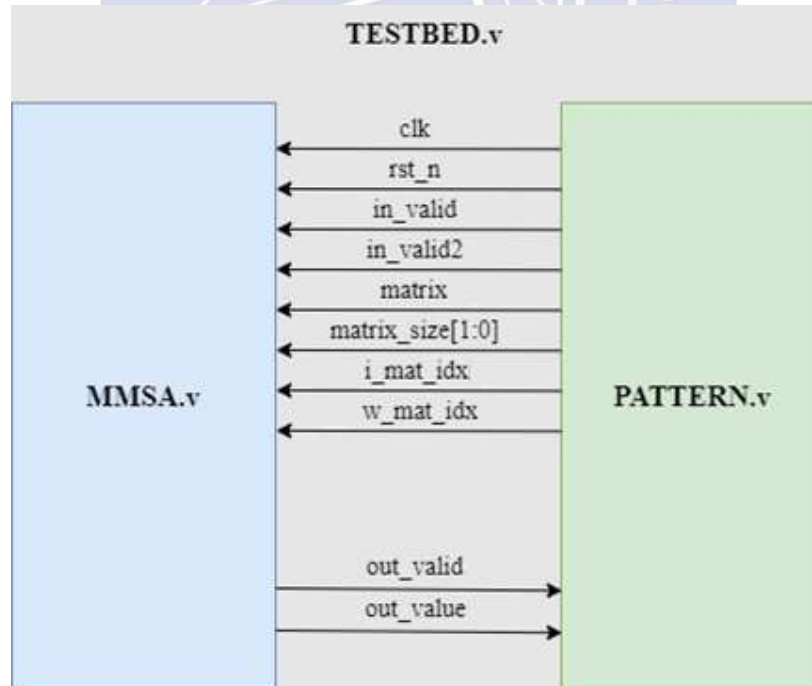
Constraints of the design in APR flow

1. Floorplaning
   a. Core size
      Define by user
   b. Core to IO boundary
      Each side must be more than 250
   c. Hard Macro placement
      All hard macro should be in CORE

2. Power planning
   a. Core Ring
      (i)   Top & Bottom: metal layer must be odd (1,3,…) and width is 9.
      (ii)   Left & Right: metal layer must be even (2,4,…) and width is 9.
      (iii) Each side must be wire group, interleaving, and at least 10 pairs.
   b. Stripes
      (i)   Vertical: metal layer must be even (2,4,…) and width is at least 2. 4
      (ii)   Horizontal: metal layer is must be odd (1,3,…) and width is at least 2. 4
      (iii) The maximum distance between two stripes or the stripe and edge should be less than 200.

3. Timing analysis results
   a. Timing Slack
      NO negative slacks after setup/hold time analysis (include SI).
   b. Design Rule Violation (DRV)
      The DRV of (fanout, cap, tran) should be all 0 after post-Route setup/hold time

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analysis (including SI)

4. Design verification results
   a. Layout vs. Schematic (LVS)
      NO LVS violations after "verify Connectivity".
   b. Design Rule Check (DRC)
      NO DRC violations after "verify DRC".

Grading Policy

1. Synthesis, RTL & Gate Level Simulation Correctness, APR and Post Level Simulation Correctness (70%)
2. Performance (30%)
   a. _Chip area_$^{1.5}$ * Clock_Period (post sim)
   b. You will only get performance score with correct APR and Post Simulation Result1st
   c. Demo (100%), 2nd Demo (70% of total)

Note

Please submit your files under 09_SUBMIT before **12:00 noon**.
Due Day: 1st Demo: MAY 22th 2nd Demo: MAY 24th

➢ If uploaded files violate the naming rule, you will get 5 deduct point.
➢ In this lab, you can adjust your clock cycle time. Consequently, make sure to key in post-layout clock cycle time after the command like the figure below. It's means that the TA will demo your APR Level design with post-layout clock cycle time.
   After that, you should check the following files under **09_SUBMIT/Lab11_iclabXXX/**

   RTL design : clock_cycle_iclabXXX.txt (XXX is your account no.)
   Memory file : 04_MEM_iclabXXX
                 (with all your memory files .v / .db / .vclef / .lib)
                 file_list_iclabXXX.f
   APR file :   CHIP_iclabXXX.sdc
                 CHIP_iclabXXX.inn
                 CHIP_iclabXXX.io
                 CHIP_iclabXXX.v
                 CHIP_iclabXXX.sdf
                 CHIP_iclabXXX.inn.dat

   If you miss any files on the list, you will fail this lab.
   If any error occurs when restoring your design, you will FAIL the lab
   Then use the command like the figure below to check the files are uploaded or not.
   `[Exercise/09_SUBMIT]% ./02_check 1st_demo`

1. **Template folders and reference commands:**
   00_TESTBED
   04_MEM/   (Memory location)
   05_APR/   (Automatic Place & Route Folder)   **./00_combine**
                 (Gate-level simulation with pads)   **./01_run**
   06_POST/   (Post Layout Simulation)   **./01_run**
   09_SUBMIT/   (submit your files)   **./01_submit ./02_check**
   `Exercise/09_SUBMIT]$ ./01_submit 40.0`

   40.0 is your cycle time
   ➢ You can key in **./09_clean_up** to clear all log files and dump files in each folder

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