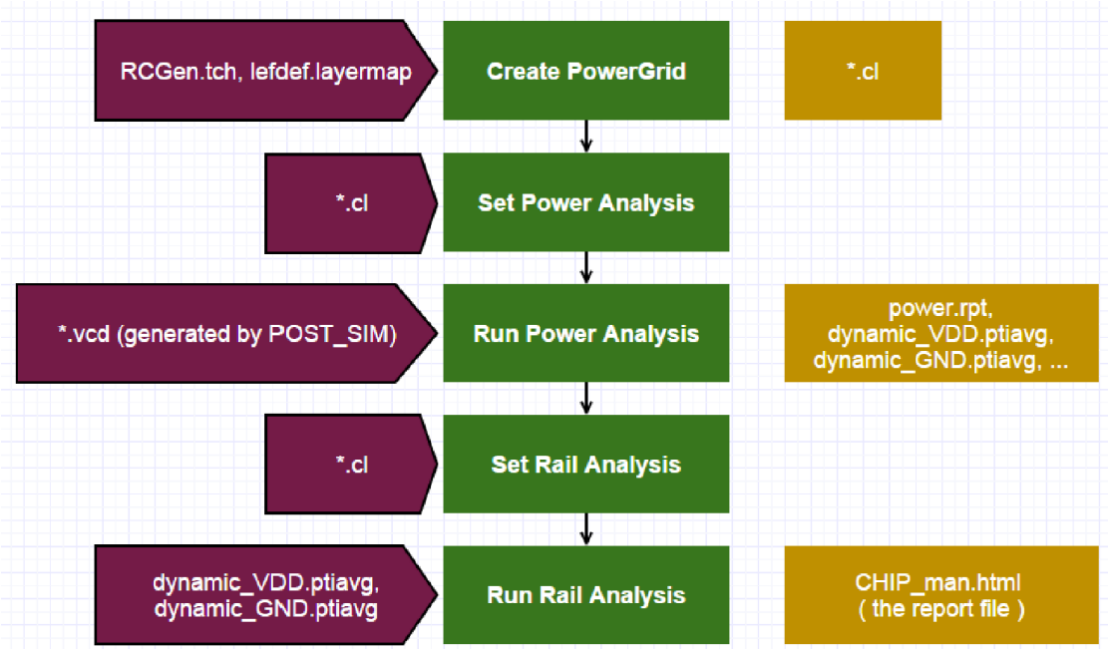
NYCU-EE ICLAB - Spring 2023

Lab12 Power Rail Analysis Practice Tutorial

1. Flow overview

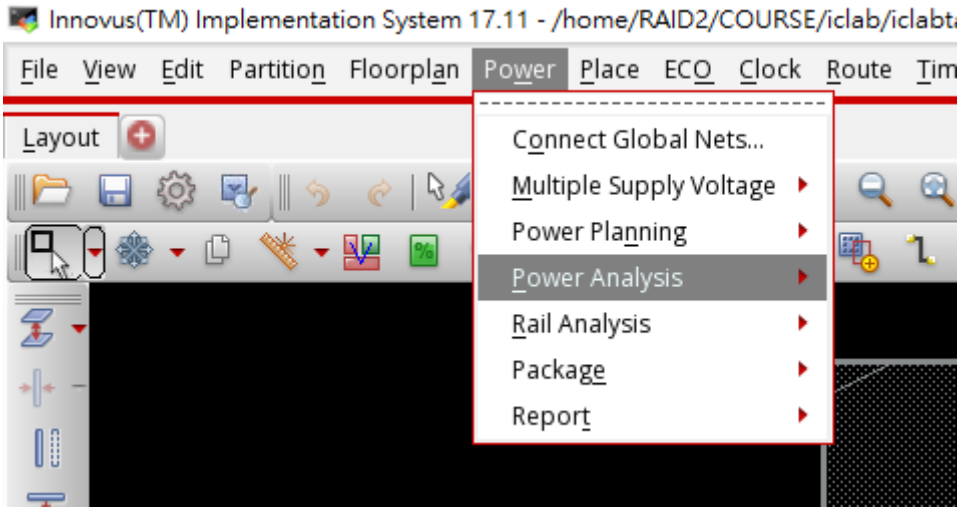


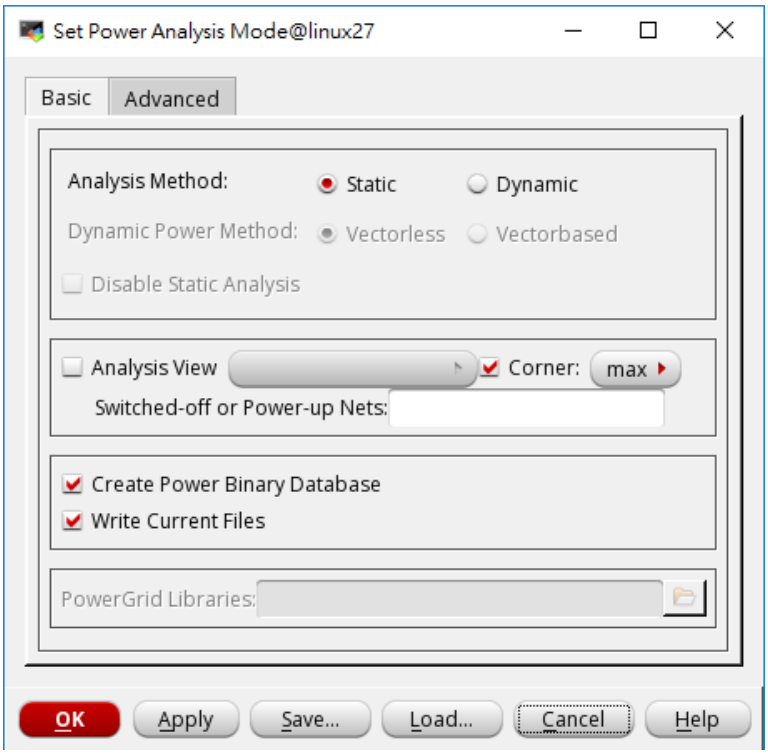
2. Set environment

- `unix% tar -xvf ~iclabta01/Lab12.tar`
- `unix% cd Lab12/Practice/05_APR`
- `unix% mkdir power_log` (You will save all the things here)
- `unix% innovus`
- Restore the design **DBS/CHIP.inn**

3. Static Power Analysis

1. Save CHIP.v
2. Write CHIP.sdf
3. Run post simulation at 06_POST, the generated waveform CHIP_POST.fsdb will be used for power rail analysis.
4. In the innovus menu, open ***Power*** -> ***Power Analysis*** -> ***Setup***





i. Click OK.

5. In the innovus menu, open ***Power*** -> ***Power Analysis*** -> ***Run***

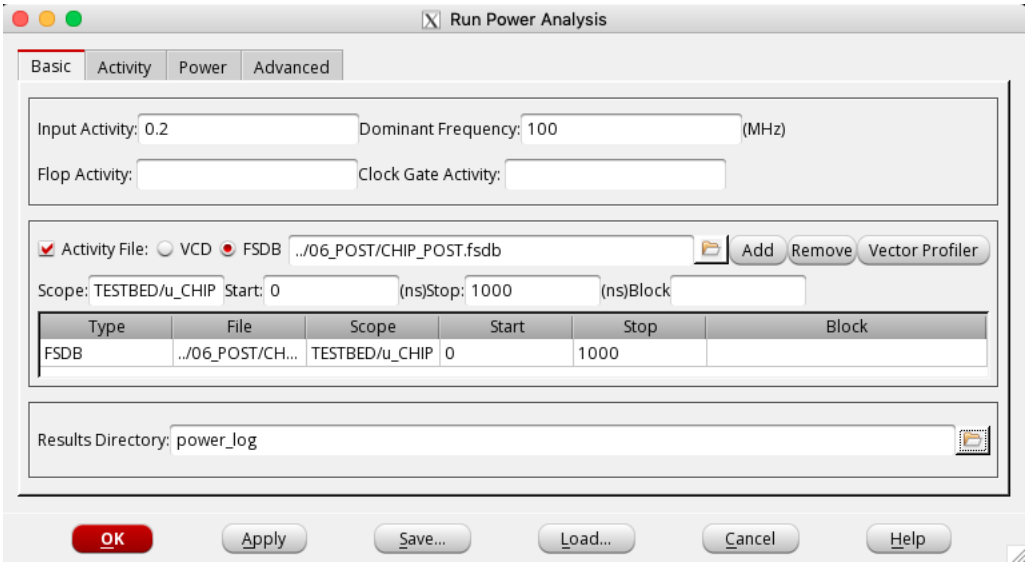
i. ◆Activity FILE ◆FSDB

ii. Fill the information:

- Select CHIP_POST.fsdb (from 06_POST)
- Scope: TESTBED/u_CHIP
- Start: 0; Stop: 1000
- Press Add

iii. Results Directory: power_log

iv. Click OK.

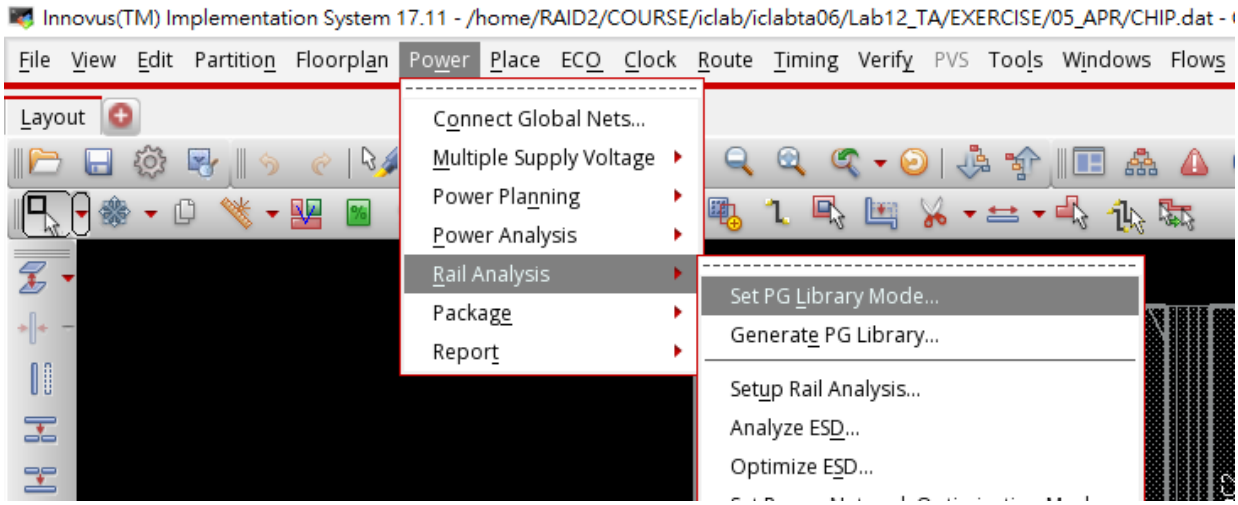


v. Results appear at terminal

```
Total Power
--------------------------------------------------------------------------------
Total Internal Power:       56.34742919           89.3507%
Total Switching Power:       6.69368832           10.6142%
Total Leakage Power:         0.02211333            0.0351%
Total Power:                63.06323143
--------------------------------------------------------------------------------
```

4. Create Power Grid Library

1. In the innovus menu, open ***Power*** -> ***Rail Analysis*** -> ***Set PG Library Mode***



i. Cell type: ◆Tech Only

ii. Filler Cell Names: **FILL1 FILL16 FILL2 FILL32 FILL4 FILL64 FILL8**

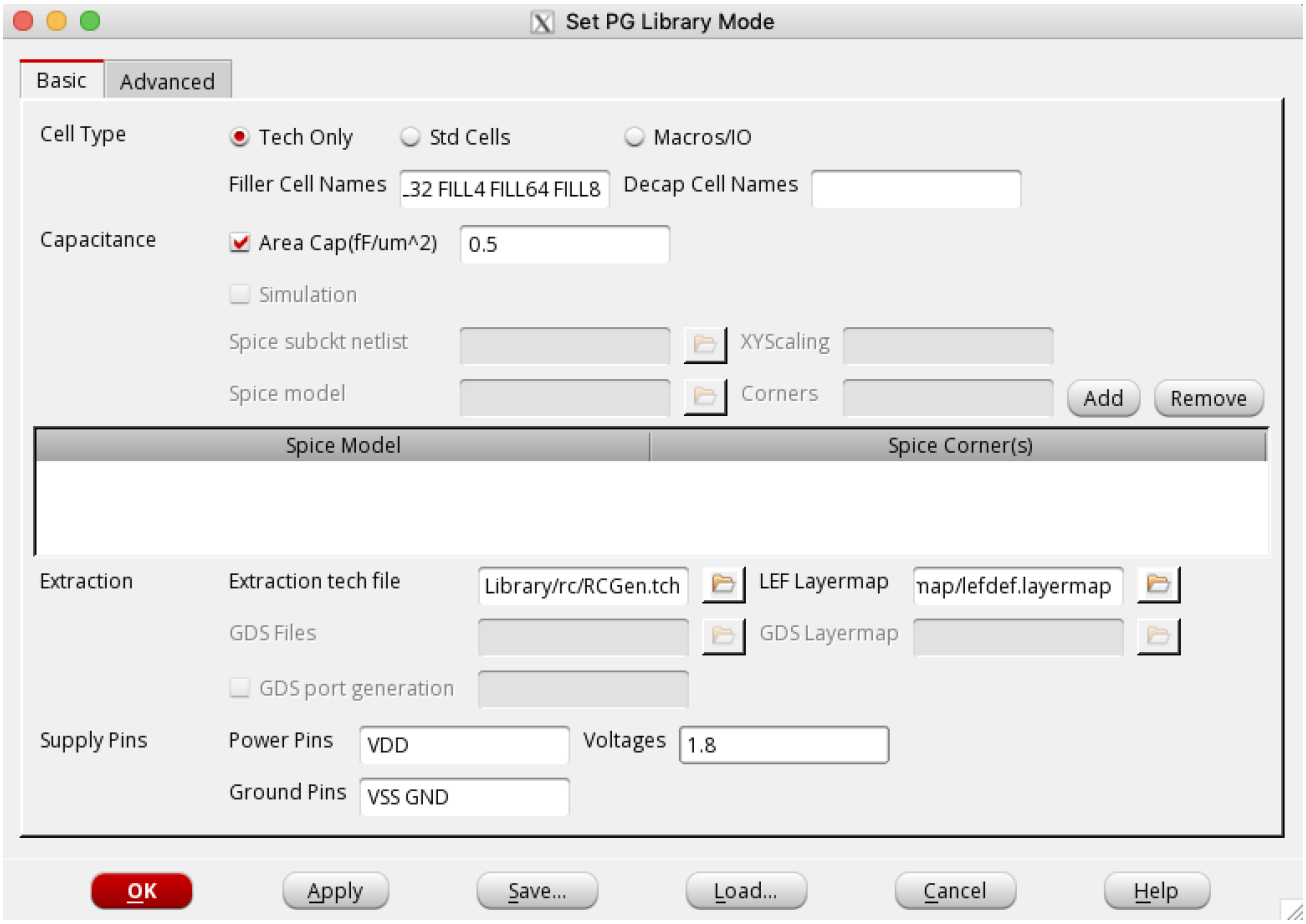
iii. Extraction

- Extraction tech file: **Library/rc/RCGen.tch** (File of type: All files(*))
- LEF Layermap: **Library/layermap/lefdef.layermap**

iv. Supply Pins

- Voltages: **1.8**
- Power pin: **VDD**
- Ground pin: **VSS GND**

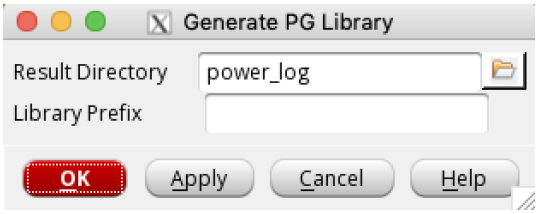
v. Click OK



2. In the innovus menu, open ***Power -> Rail Analysis -> Generate PG Library***

i. Choose power_log

ii. Click OK



iii. Check if the directory **techonly.cl** exists (under power_log/)

3. In the innovus menu, open ***Power -> Rail Analysis -> Set PG Library Mode***

   i. Cell type: ◆Std Cells

   ii. Filler Cell Names: **FILL1 FILL16 FILL2 FILL32 FILL4 FILL64 FILL8**

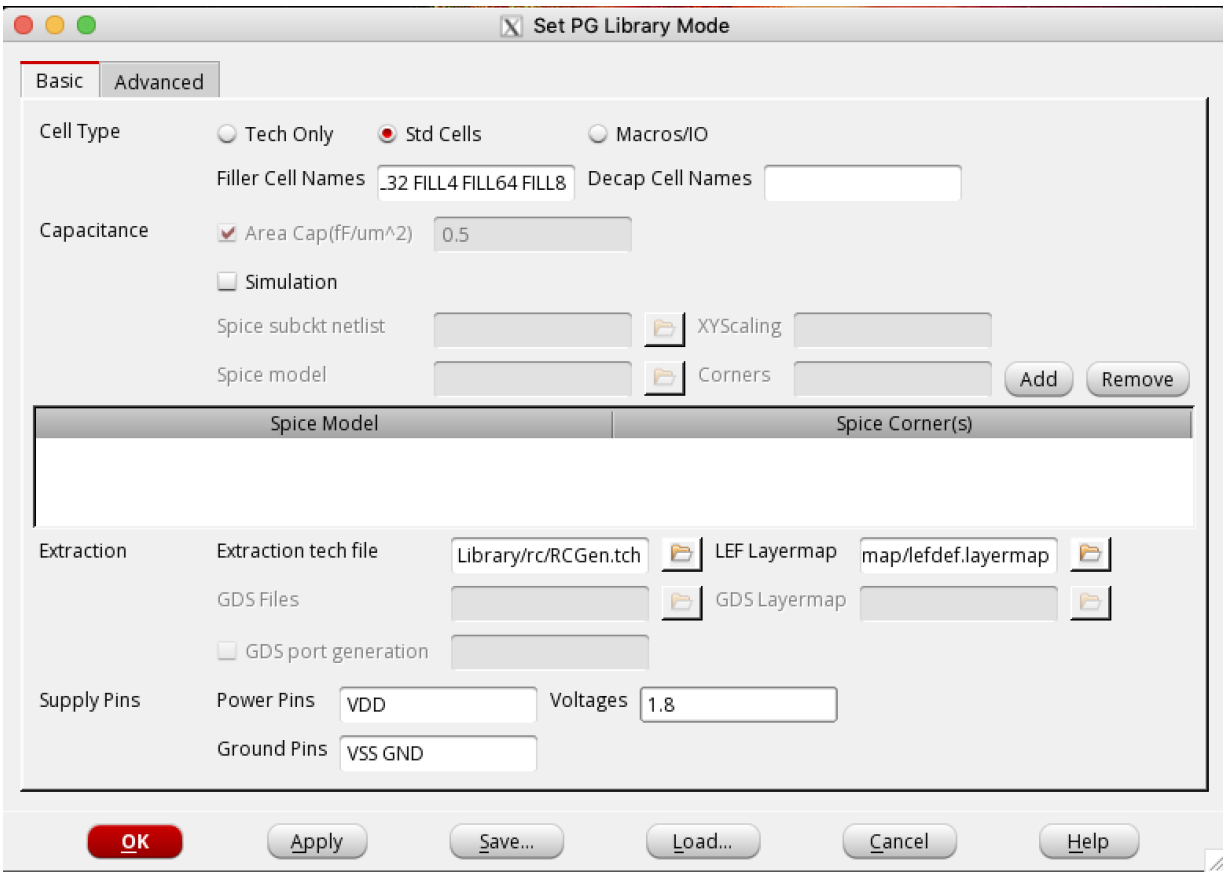
   iii. Extraction

   - Extraction tech file: **Library/rc/RCGen.tch**
   - LEF Layermap: **Library/layermap/lefdef.layermap**

   iv. Supply Pins

   - Voltage: **1.8**
   - Power pin: **VDD**
   - Ground pin: **VSS GND**

   v. Click **OK**.



4. In the innovus menu, open ***Power -> Rail Analysis -> Generate PG Library***

   i. Click OK

   ii. Check if the directory **stdcells.cl** exists (under power_log/)

5. Rail Analysis

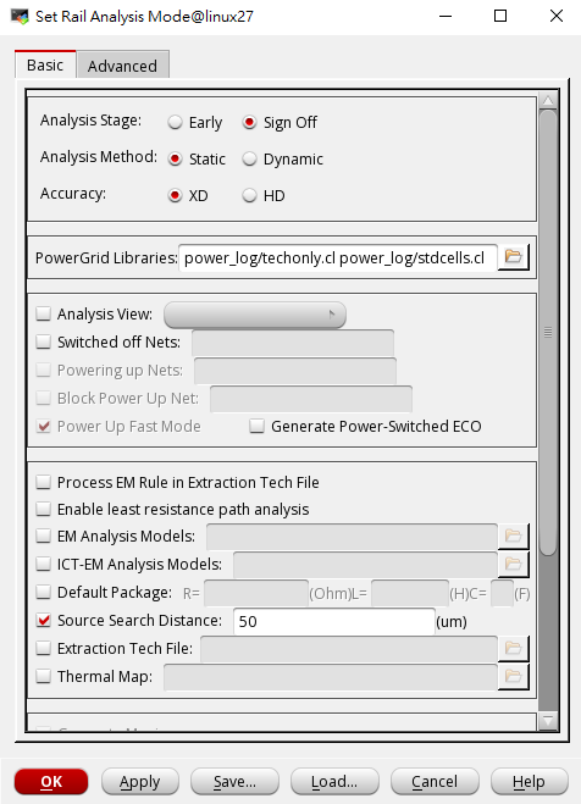
1. In the innovus menu, open ***Power -> Rail Analysis -> Setup Rail Analysis***

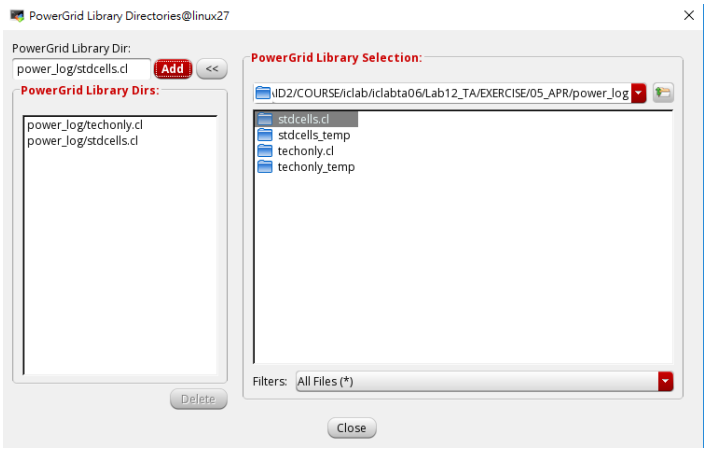
   i. Analysis Method: ◆ **Static**

   ii. PowerGrid Libraries:

   power_log/**techonly.cl** (should be added first)
   power_log/**stdcells.cl**

   iii. Click **OK**





2. In the innovus menu, open ***Power -> Rail Analysis -> Run Rail Analysis***

   i. ◆ Domain Based Domain Name: PD

   ii. Power Net(s): VDD Voltage(s): 1.8 Threshold:1.7 (Press ADD)

   Power Net(s): GND Voltage(s): 0 Threshold:0.1 (Press ADD)

   *(1.8v * 5% ≈ 0.1v)*

   iii. Power/Current Files(s):

   power_log/static_VDD.ptiavg

   power_log/static_GND.ptiavg

   iv. Power Pads: ◆ XY File

   v. Click **Create**

   - Net Name: VDD
   - Click **Fetch**
   - Save as **power_log/CHIP_VDD.pp**

   vi. Click **Create** again

   - Net Name: GND
   - Click **Fetch**
   - Save as **power_log/CHIP_GND.pp**

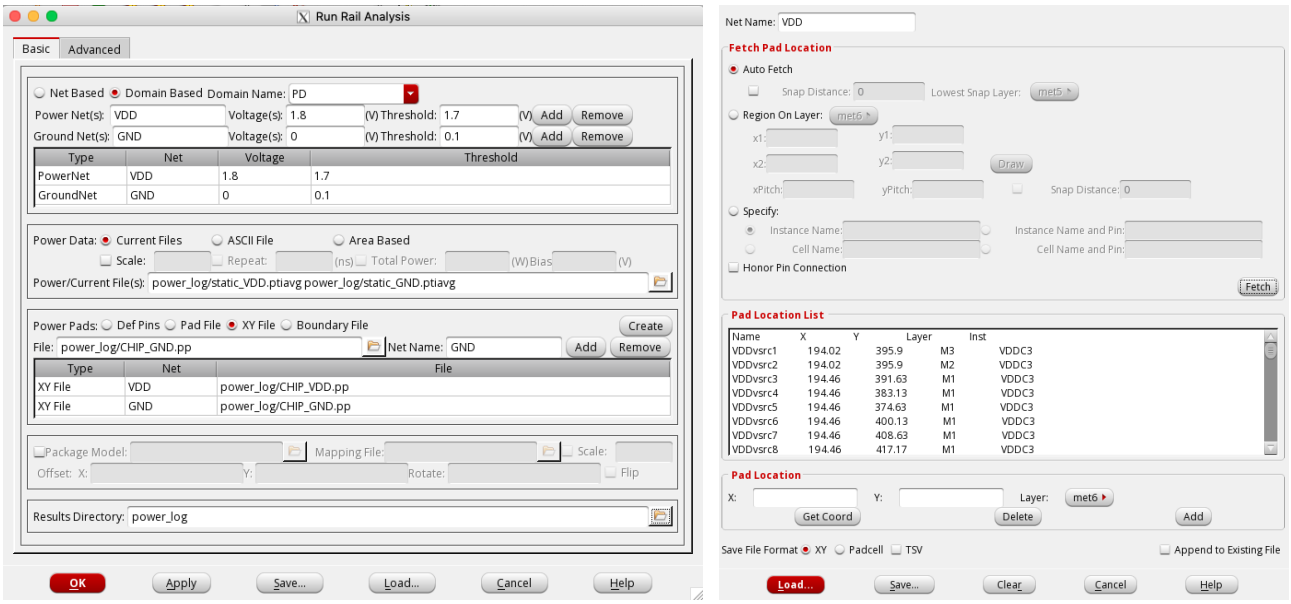
   vii. Click **Cancel**

   viii. File: **power_log/CHIP_VDD.pp** Net Name: VDD (press ADD)

   ix. File: **power_log/CHIP_GND.pp** Net Name: GND (press ADD)

   x. Results Directory: **power_log**

   xi. Click **OK**



6. Power & IR Drop Results

1. In the innovus menu, open ***Power -> Report -> Power & Rail Result***

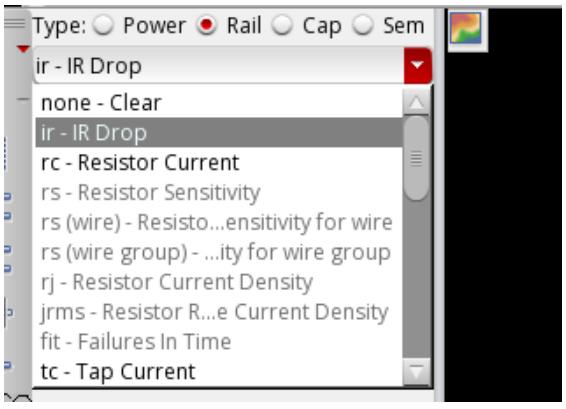
   i. ◆Auto Apply for Color Scale

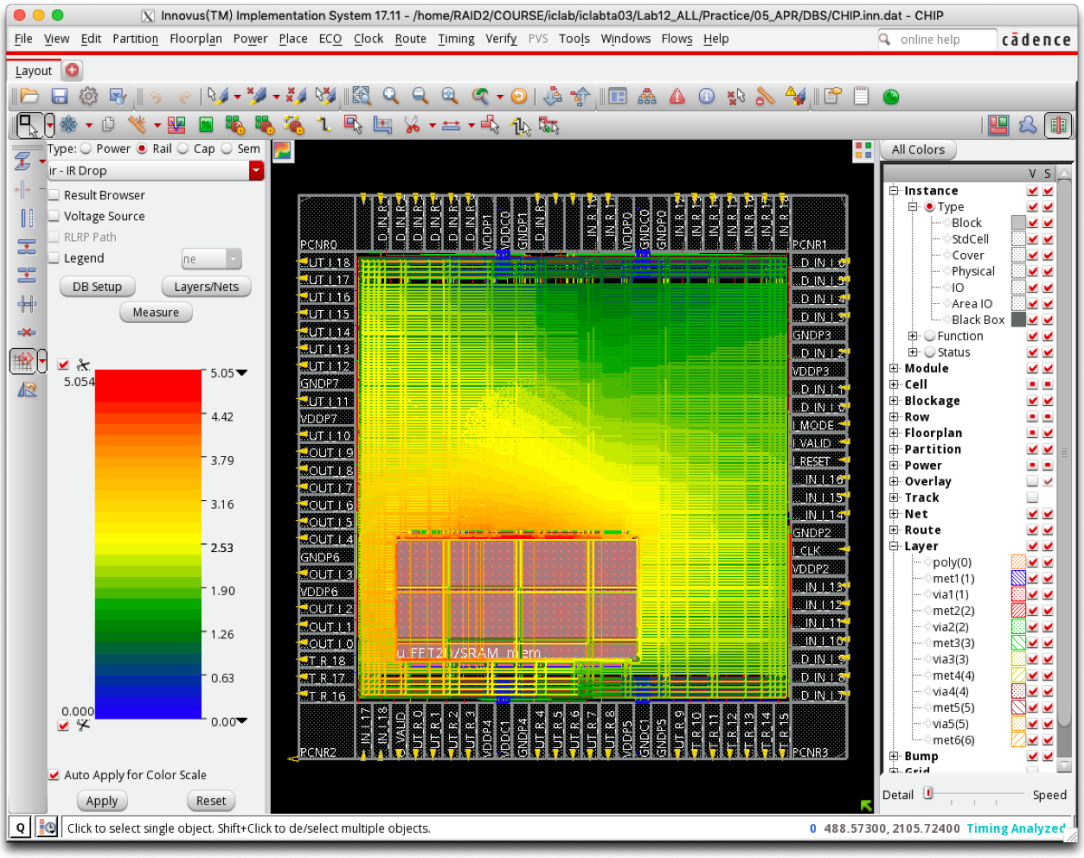
   ii. Click DB Setup

   - Power Databas: power_log/power.db
   - Rail Database: power_log/PD_25C_avg_1
   - Click OK

   iii. Type: ◆Rail

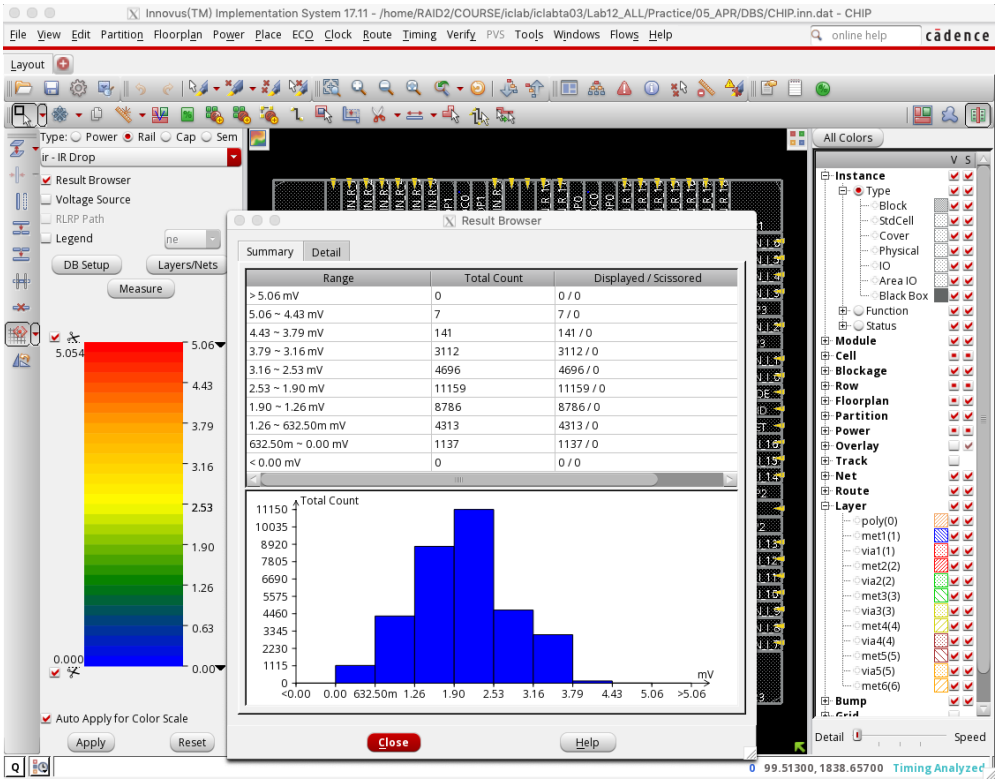
   iv. Choose ir – IR Drop





i. ◆Result Browser

The following shows the distribution of IR Drop (they should in the range **0.1V**)



Appendix - Provided library files

- Timing libraries

Directory	Contain
/05_APR/Library/lib/	slow.lib
	fast.lib
	umc18io3v5v_slow.lib
	umc18io3v5v_fast.lib

- Physical libraries

Directory	Contain
/05_APR/Library/lef/	umc18_6lm.lef
	umc18_6lm_antenna.lef
	umc18io3v5v_6lm.lef

- RC extraction table/files

Directory	Contain
/05_APR/Library/rc/	umc18_1p6m.captbl
	RCGen.tch

- CeltIC libraries

Directory	Contain
/05_APR/Library/cdb/	slow.cdb
	fast.cdb

- Layermap

Directory	Contain
/05_APR/Library/layermap/	lefdef.layermap
	qrc_lefdef.layermap