

# NYCU-EE IC LAB – Spring 2023

## Lab12 Exercise

### Design: Train Tour APRII

#### Data Preparation

1. Extract test data from TA's directory:

```
% tar xvf ~iclabta01/Lab12.tar
```

2. The extracted LAB directory contains:

a. 00\_TESTBED

b. 01\_RTL

c. 02\_SYN

d. 03\_GATE

e. 04\_MEM

f. 05\_APR

g. 06\_POST

h. 09\_SUBMIT

#### Description

In this lab you will finish the **backend flow (APR)** for Lab2(TA provided netlist files) and use the **IR drop and Power Analysis** tool for your layout.

#### Inputs and Outputs

Input Signals	Bit Width	Definition
clk	1	Clock.
rst_n	1	Asynchronous active-low reset.
in_valid	1	High when col and row signals are valid.
in_valid_num	1	High when in_num signals are valid.
col, row	4	(col, row) is queen's location
in_num	3	number of inputs

Output Signals	Bit Width	Definition
out_valid	1	High when output is valid
out	4	Row positions of 12 queens column by column

#### Layout Specifications

1. CHIP.sdc period is **fixed to 10ns** input/output delay is **fixed to 5ns**
2. Core power pad and io power pad
  - a. At least one pair at each side.
3. Floorplanning
  - a. Core size:
    - ✓ Defined by you
  - b. Core to IO boundary:
    - ✓ Each side must be larger than **100**
4. Power Planning

- a. Core Ring
  - ✓ Top & Bottom: metal layer must be odd and width is **fixed to 9**.
  - ✓ Left & Right: metal layer must be even and width is **fixed to 9**.
  - ✓ Each side must be **wire group**, **interleaving**, and **at least 4 pairs**.
- b. Stripes
  - ✓ Vertical: metal layer must be even and width is defined by you.
  - ✓ Horizontal: metal layer must be odd and width is defined by you.
  - ✓ Number of pairs is defined by you
- c. Timing Analysis
  - ✓ Timing Slack:
    - NO negative slacks** after setup/hold time analysis (Post-Route stage)
  - ✓ Design Rule Violation (DRV)
    - The DRV of (fanout, cap, tran) should be all **0** after setup/hold time analysis
- d. Design Verification Result
  - ✓ LVS : **No LVS violations** after “verify connectivity”
  - ✓ DRC : **No DRC violations** after “verify DRC”
  - ✓ **Note: Remember to check DRC / LVS again after placing the fillers.**  
 Although in normal cases, if DRC and LVS are verified after nanoRoute, no more DRC / LVS will be produced during postRoute optimization and adding core filler. However some special cases produce the further DRC and LVS. For example: inserting a filler that is isolated from all other cells and power lines, then open LVS occurs. Thus, be sure to verify all the specs above after performing all APR steps.
- e. Rail Analysis:
  - ✓ VDD Threshold set to **1.7**
  - ✓ GND Threshold set to **0.1**
  - ✓ No IR drop is allowed larger than **3mV**

#### Note

1. Complete **CHIP.io** and **CHIP\_SHELL.v**
2. Do all the flow as in APRI (Lab11) with Layout Specification above
3. Run Power Analysis (Setup & Run)
4. Run Rail Analysis
  - Set PG Library Mode
  - Generate PG Library
  - Setup Rail Analysis
  - Run Rail Analysis
5. Observe the IR Drop to analyze whether IR drop is within **3mV**.
6. Please submit your files under 09\_SUBMIT before 12:00 at noon on May. 29:
  - If uploaded files **violate the naming rule**, you will get **5 deduct point**.

**[Exercise/09\_SUBMIT]% ./01\_submit**

After that, you should check the following files under 09\_SUBMIT/Lab12\_iclabXXX/

- i. **CHIP\_iclabXXX.inn**
- ii. **CHIP\_iclabXXX.inn.dat** (this one is a directory)
- iii. **CHIP\_SHELL\_iclabXXX.v**
- iv. **CHIP\_iclabXXX.io**

If you miss any files on the list, you will fail this lab.

Then use the command like the figure below to check the files are uploaded or not

**[Exercise/09\_SUBMIT]% ./02\_check 1st\_demo**

7. **Self-Verify** APR Result!!! Remember to **restore** and check the **checklist**.

- **You should meet all the Layout Specification and File Specification above, pass post simulation without any timing violation, and within tolerable IR drop to pass the demo.**
- **Post simulation correctness & Within Tolerable IR Drop: 100 points**
- **2de pass grade: 70 points**

