1. **Verilog coding rules**

    a. **Verify whether your implementation is at least synthesizable. In short,**
        i. Use only input, output, and output reg for the port declarations of the module.
        ii. Use only reg and wire type for the variable declarations in the module.
        iii. Do not use the initial statement (e.g., initial begin end).
        iv. Do not use the delay (e.g., # 5).
        v. Do not submit your own test bench files
        vi. You can use keyword to define constants (e.g., parameter, …)
        vii. Others are not needed.

    b. **Non-blocking and blocking assignments**
        i. Use only non-blocking assignments for the synchronous logic.
        ii. Use only blocking assignments for the asynchronous logic.
        iii. Do not mix both assignments in the single always block.
        iv. For more details, please refer to documents in Google.

    c. **Avoid unexpected behaviors**
        i. High impedance (z) and unknown value (x) causes unexpected behaviors for the simulation. Do not allow them and assign the explicit values.

    d. **Sensitivity list**
        i. Use asterisk (*) for the asynchronous logic in the always block. There are no reasons to specify variables in the sensitivity list. If you encounter the problem due to asterisk (*), you first have to think whether you correctly implemented logics.

    e. **Output reg vs output**
        i. The output reg is reg and thus, it acts as reg. For this reason, output reg is only available for the asynchronous logic and synchronous logic in the always block. In other words, the continuous assignment is impossible.
        Unlike the output reg, the output is wire. It only works for the continuous assignments and the asynchronous logic in the always block.
        ii. While some simulators do not catch and report errors for the incorrect usage, this is explicitly wrong implementation. TAs' simulator fails to compile your files if these errors occur.

2. **Submission guide**

    a. **Do not ignore the submission guide written in .pdf.**
        i. Filename
        ii. Contents inside .zip
        iii. Files you have to submit or not
        iv. Others notified in .pdf

    b. **We do not accept submissions if files are not correctly submitted.**

- **You must follow the rules described in red words or sentences**