Lab 4-2a. Pipelined CPU
(w/ control flow instrs.)

CSED 311

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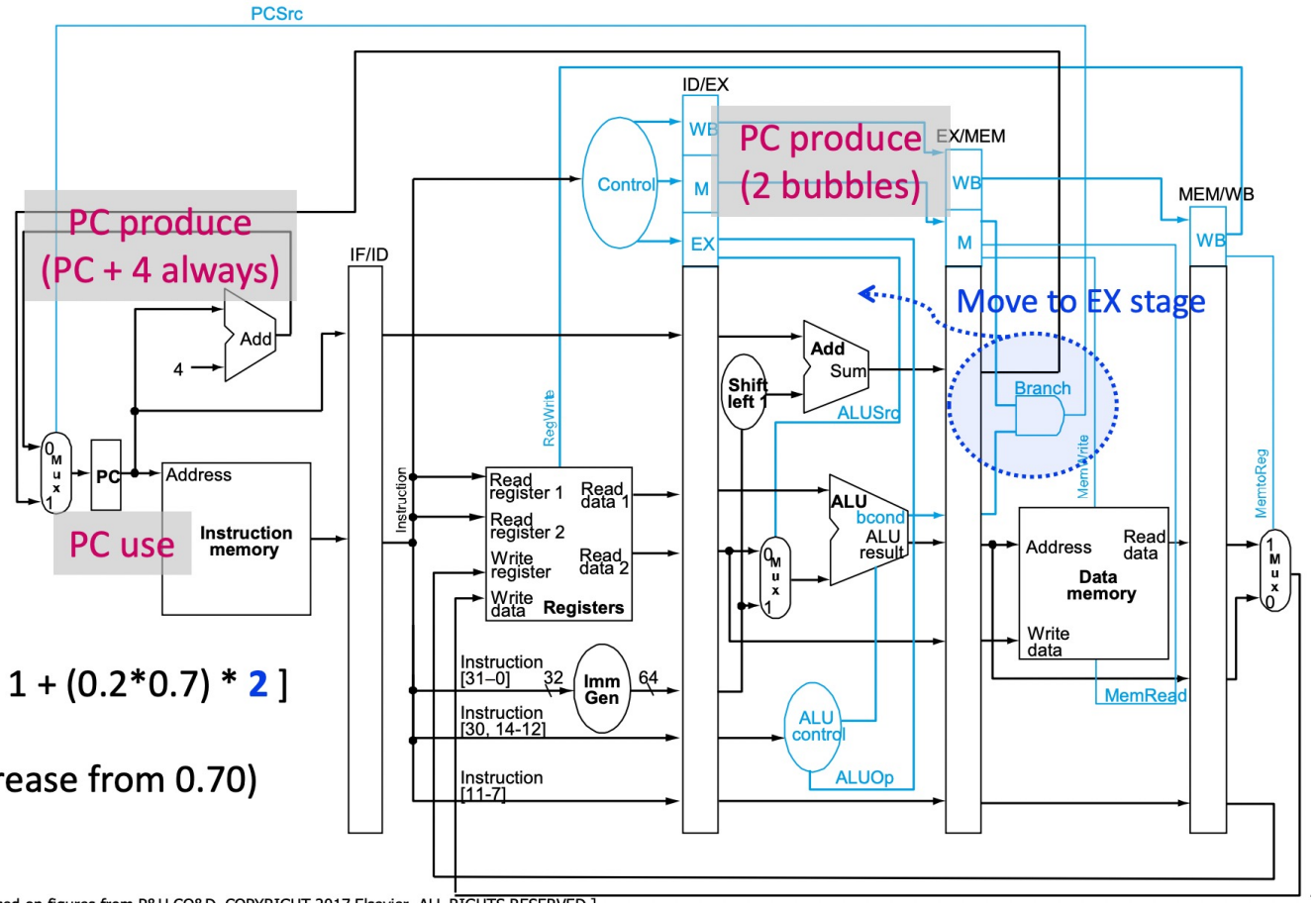
Datapath (w/ control flow instrs.)

- Resolve at EXE stage (BEQ, BNE, BLT, BGE, JAL, JALR)
  - Miss prediction causes two bubbles



Submission

- Implementation (Deadline: 5/17 9:00 am)
  - 5-stage pipelined CPU w/ control flow instructions
    - Implement your design over lab4-1 implementation
    - Control hazard
      - Branch prediction (need to flush on misprediction)
        - Always not taken (no extra credit) – Does not require BTB
        - Always taken (partial extra credit +3) – Require BTB (32 entries)
        - 2-bit global prediction (partial extra credit +5) – Require BTB (32 entries)
        - Gshare (full extra credit +7) – Require BTB (32 entries)
        - Entries in BTB must be initialized as empty
  - You need to follow the rules described in lab_guide.pdf

- Report (Deadline: 5/17 23:59)
  - How to handle branch prediction?
  - Describe your design of branch predictor
  - If you implement 2-bit global prediction
    - Compare total cycles of 2-bit global prediction with that of always-taken and always-not-taken
  - If you implement always-taken
    - Compare total cycles of always-taken with that of always-not-taken

Submission

- Implementation file format
  - .zip file name: Lab4-2a_{team_num}_{student1_id}_{student2_id}.zip
  - Contents of the zip file (only *.v):
    - cpu.v
    - …
    - Do not include top.v, Memory.v, and RegisterFile.v
- Report file format
  - Lab4-2a_{team_num}_{student1_id}_{student2_id}.pdf