Vivado simulation guide

CSED 311

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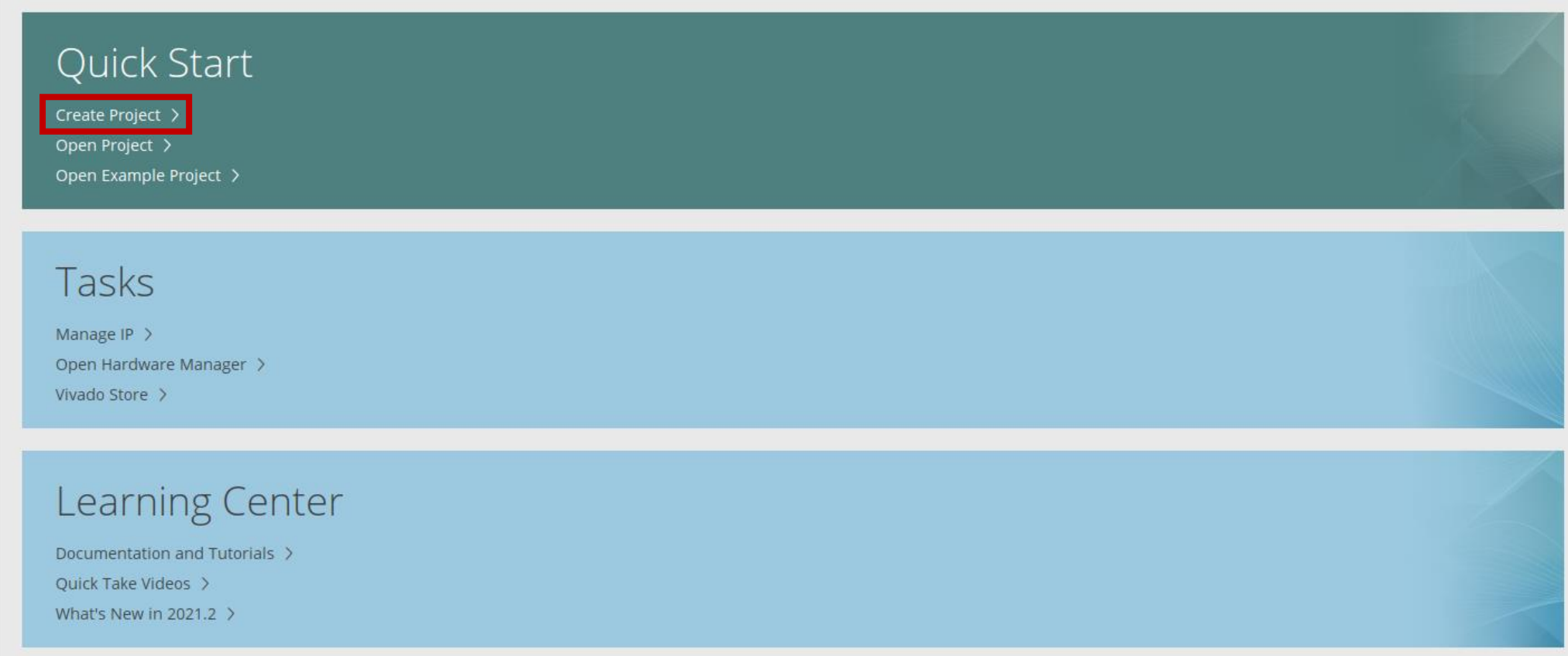
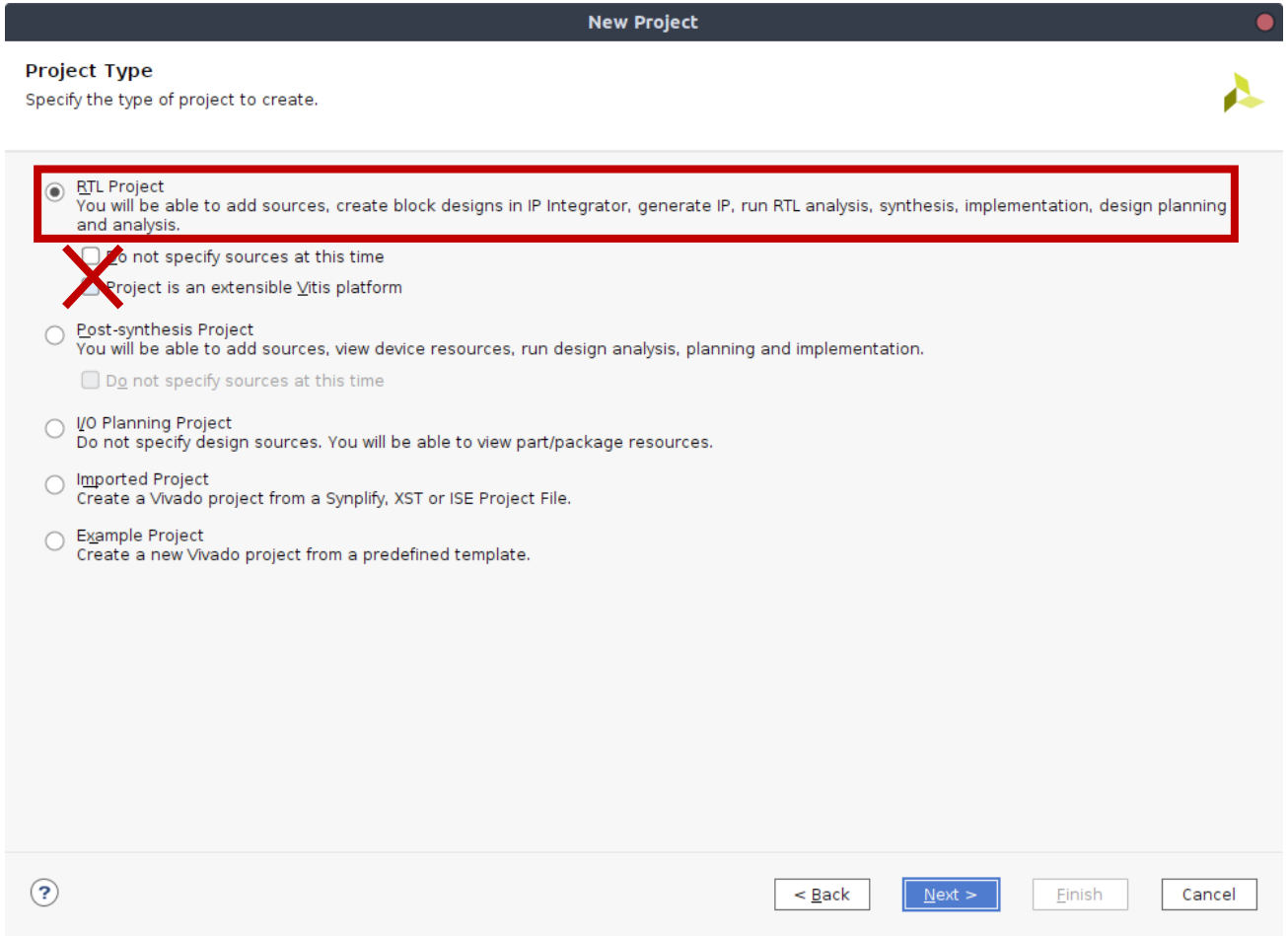
Project setup

- **Create project**



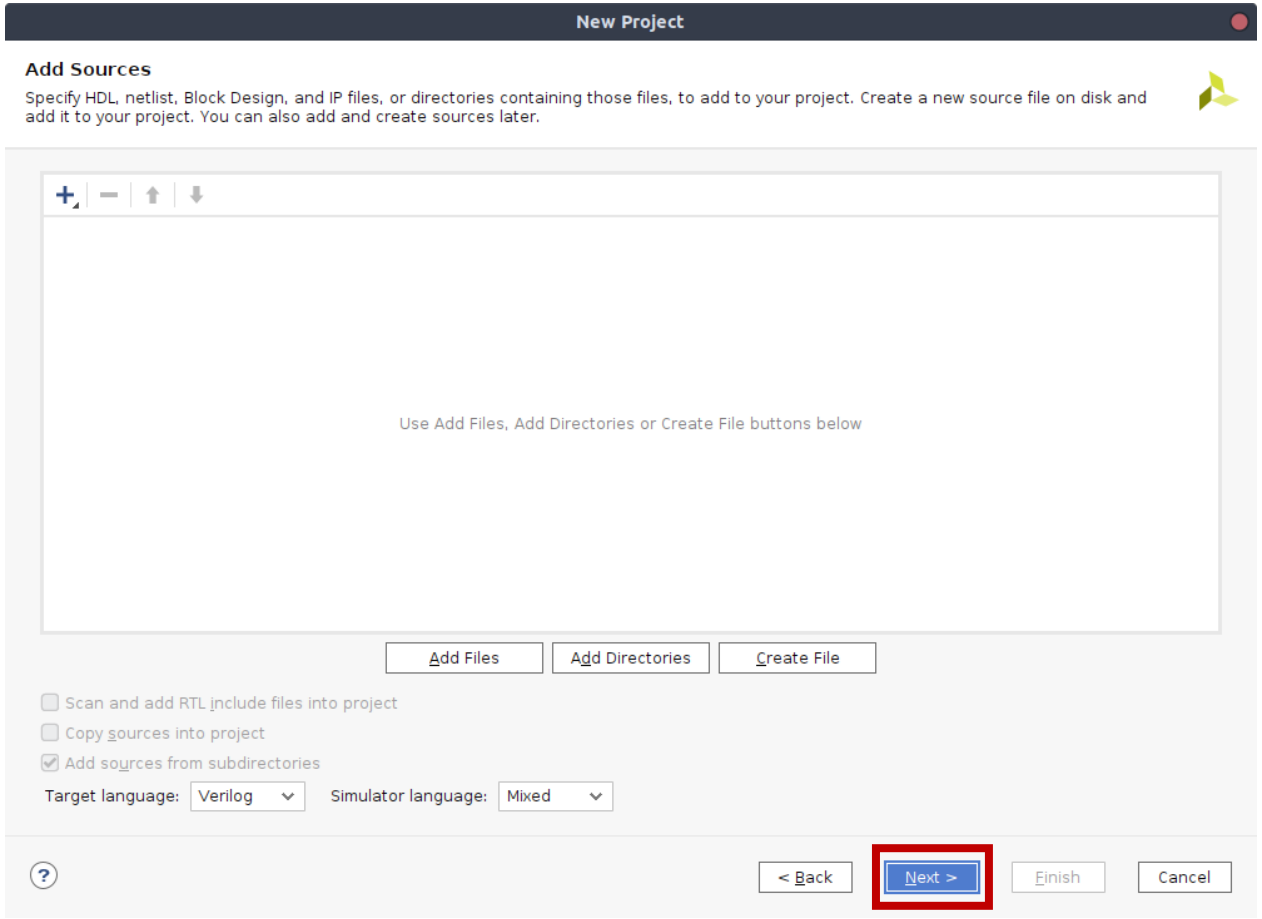
Project setup

- **Choose RTL Project**
  - Uncheck all check boxes under “RTL Project”



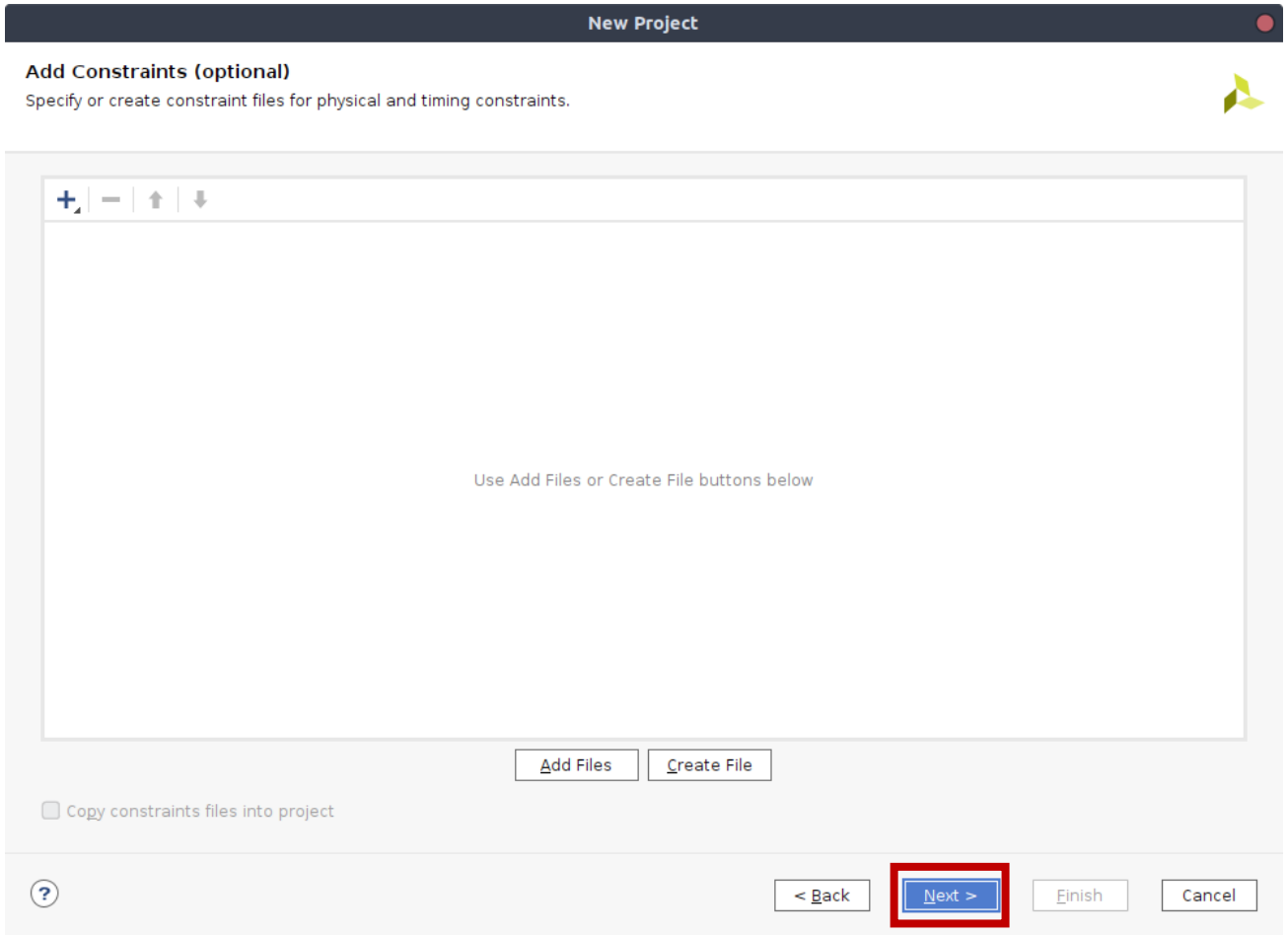
Project setup

- **Do nothing** and go to Next



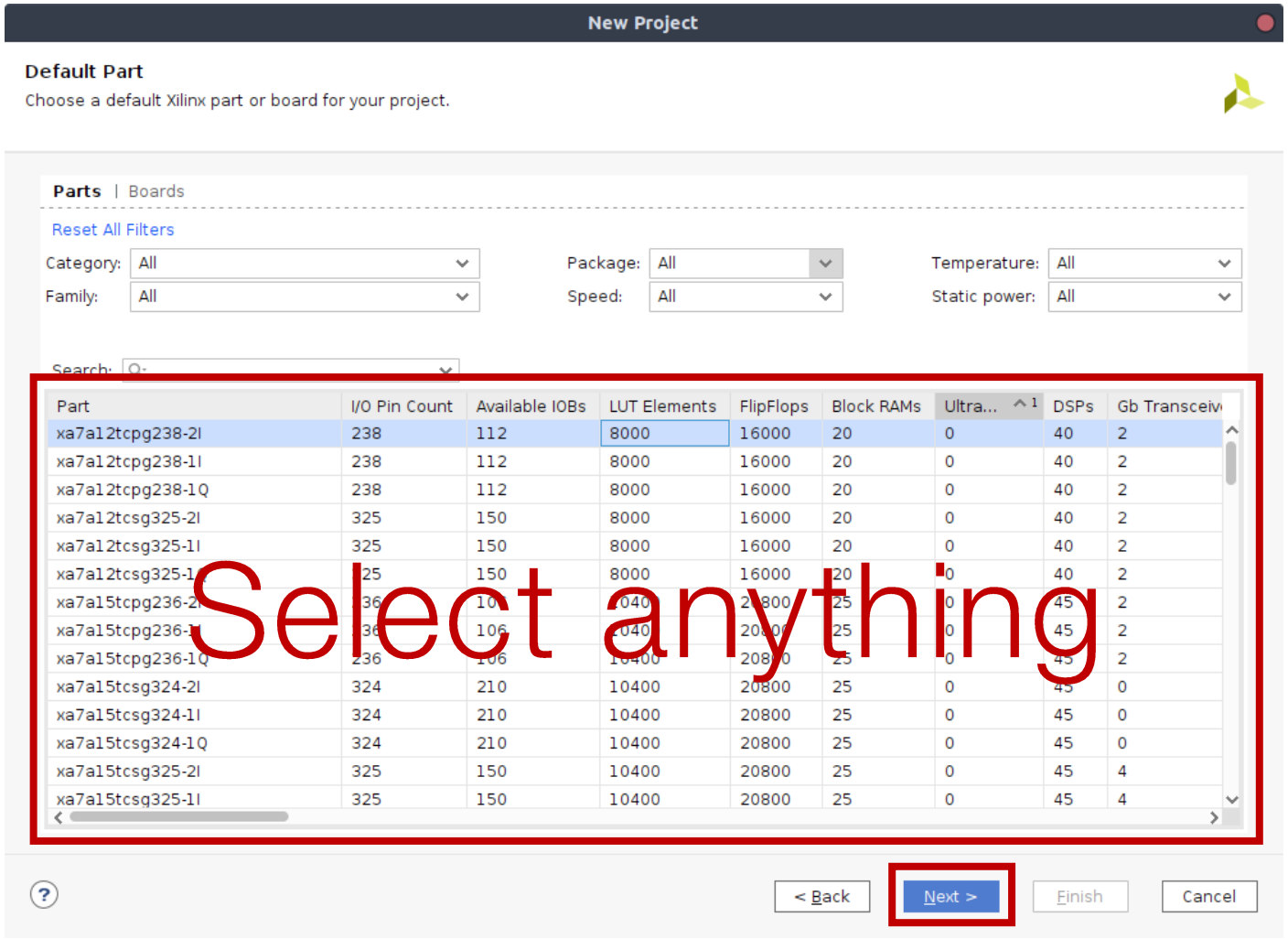
Project setup

- **Do nothing** and go to Next



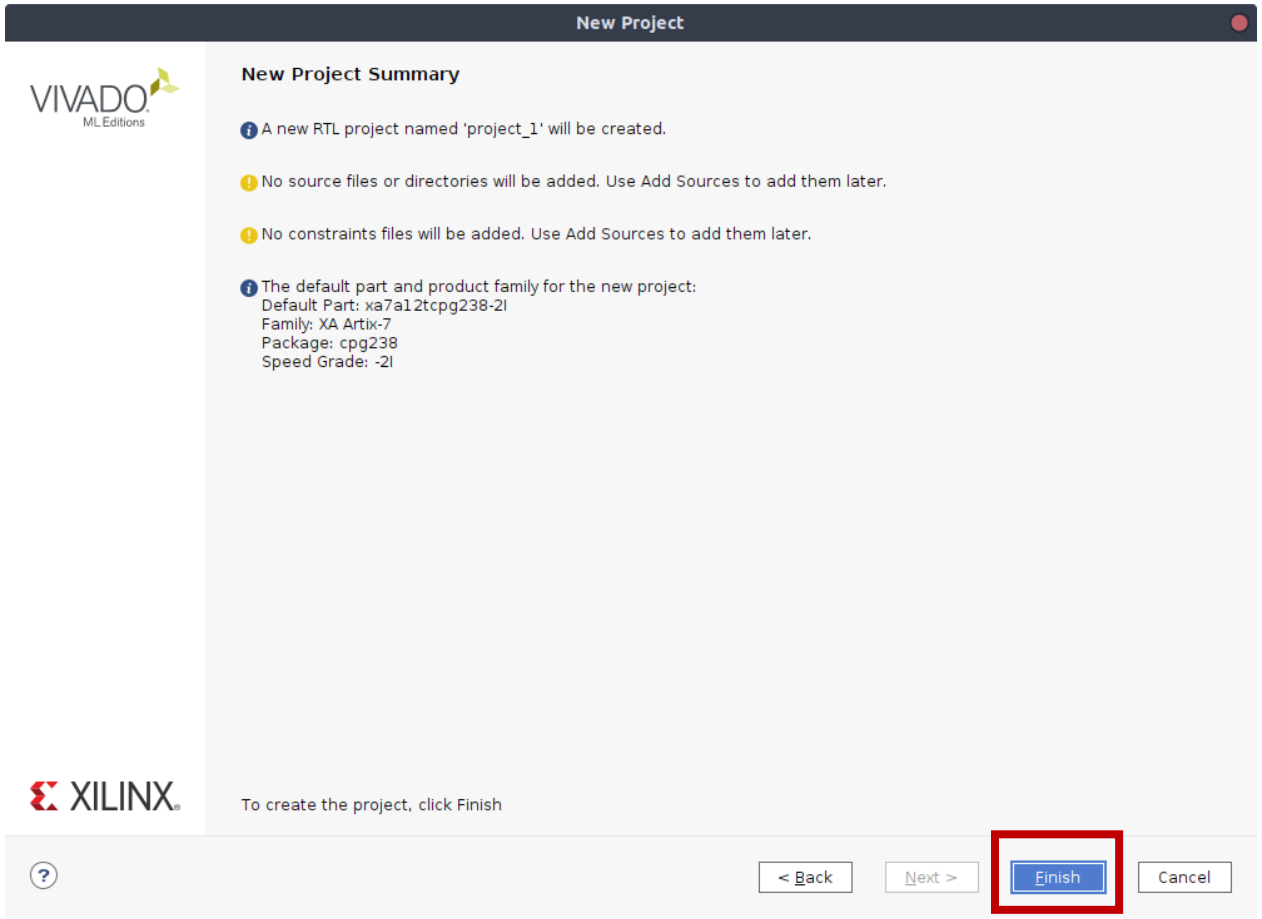
Project setup

- **Select anything you want and go to next**
  - This section is required for FPGA. However, because we do not use FPGA, we ignore this section



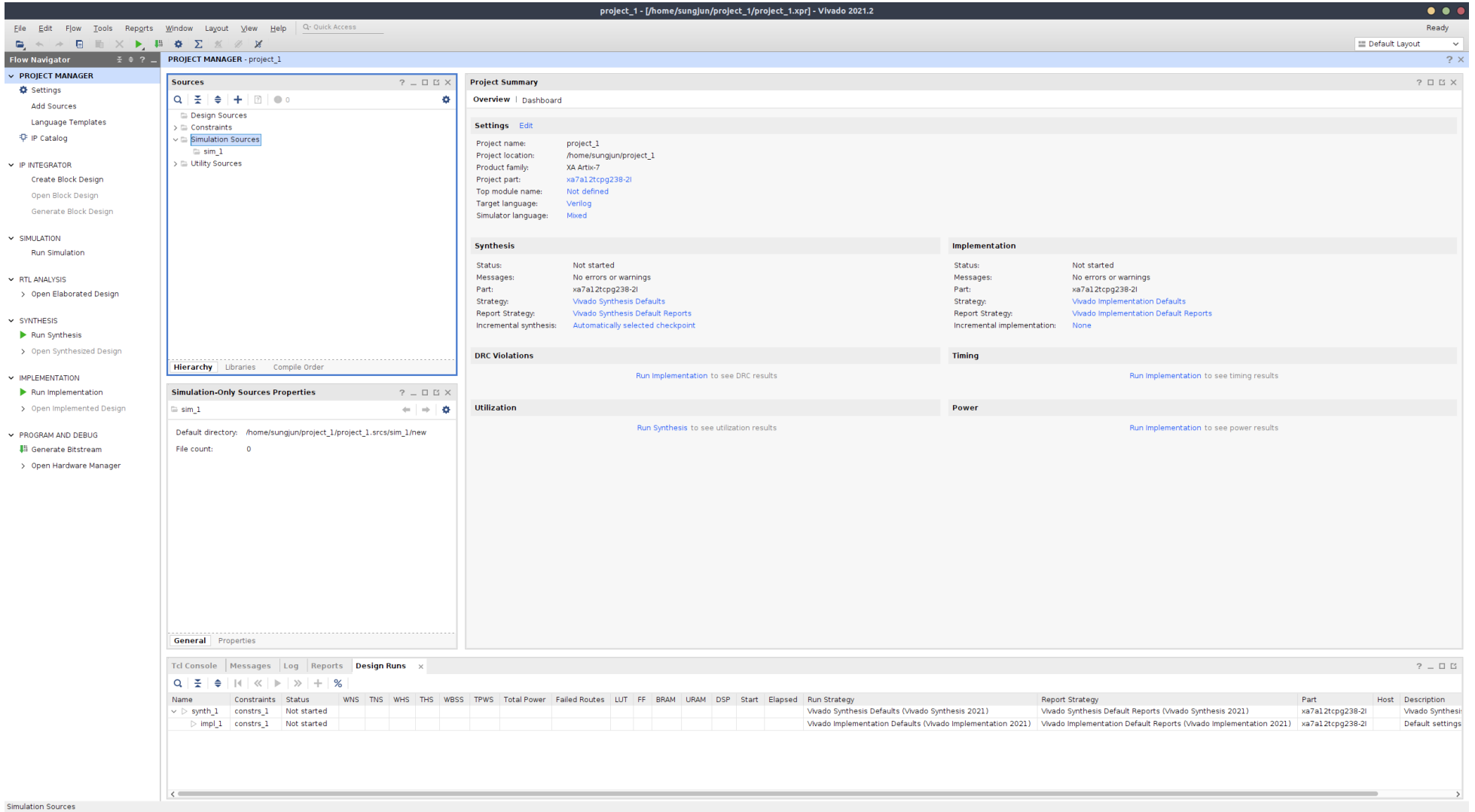
Project setup

- **Finish project setup**



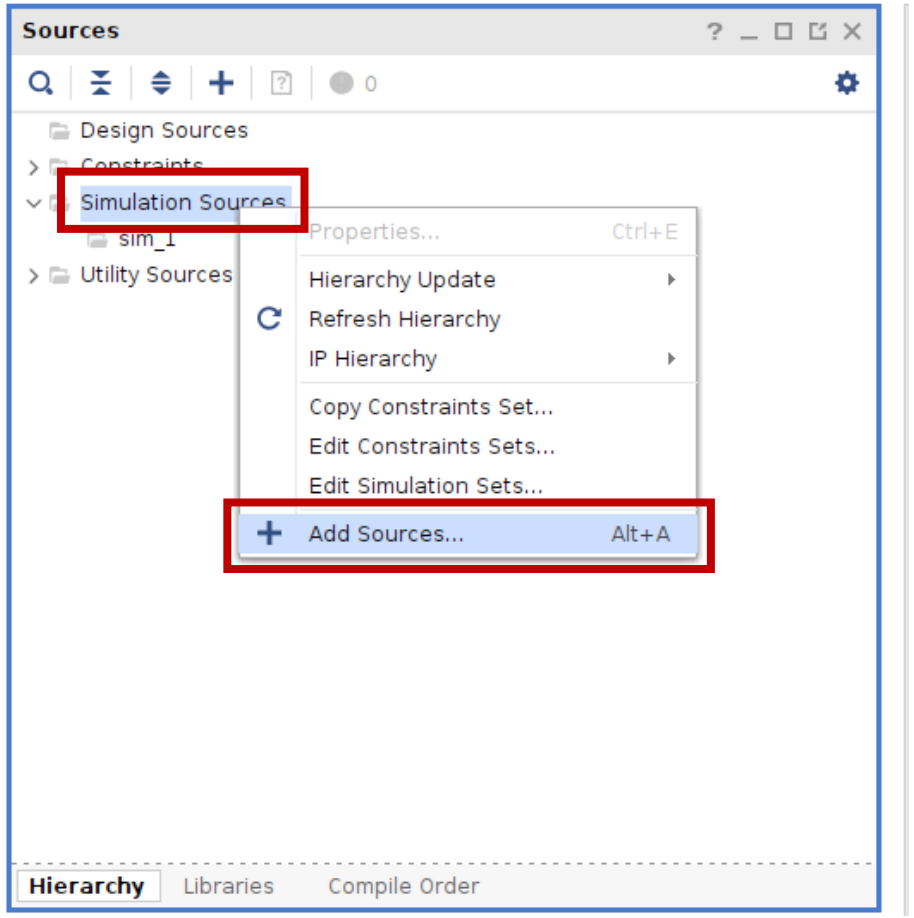
Import simulation files

- This is the project main page



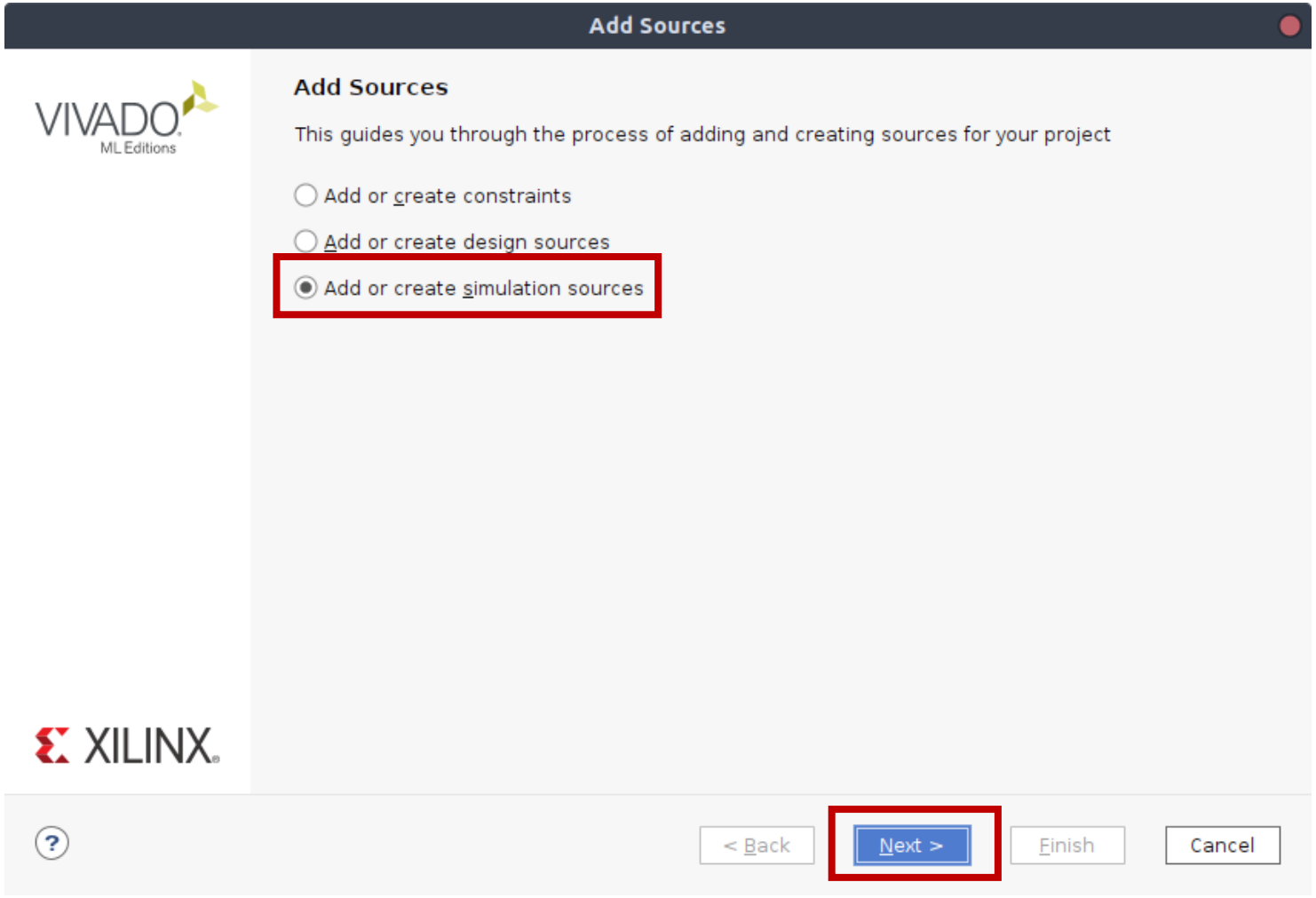
Import simulation files

- Click ‘Add sources’ from ‘Simulation Sources’



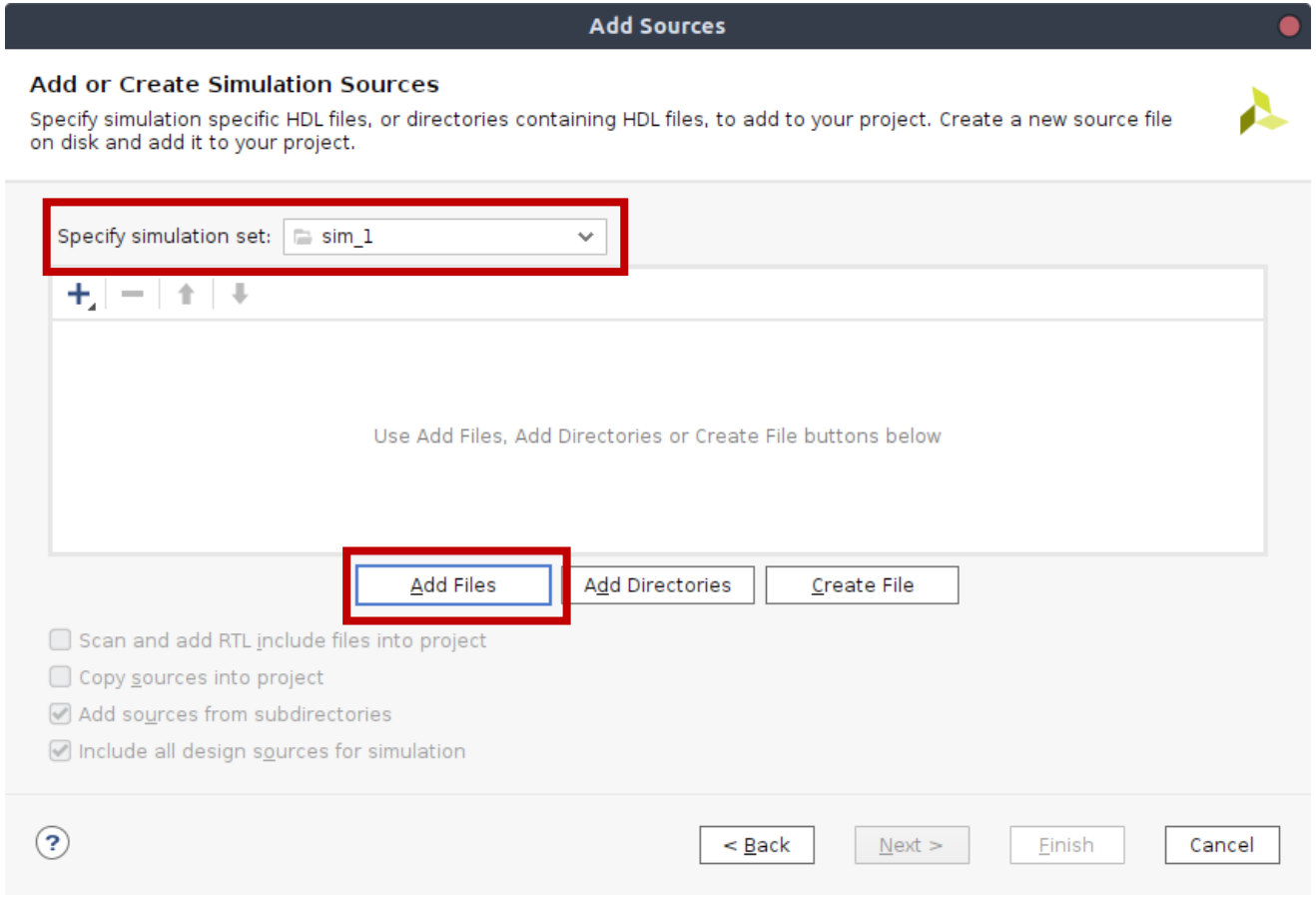
Import simulation files

- **Choose ‘Add or create simulation sources’**



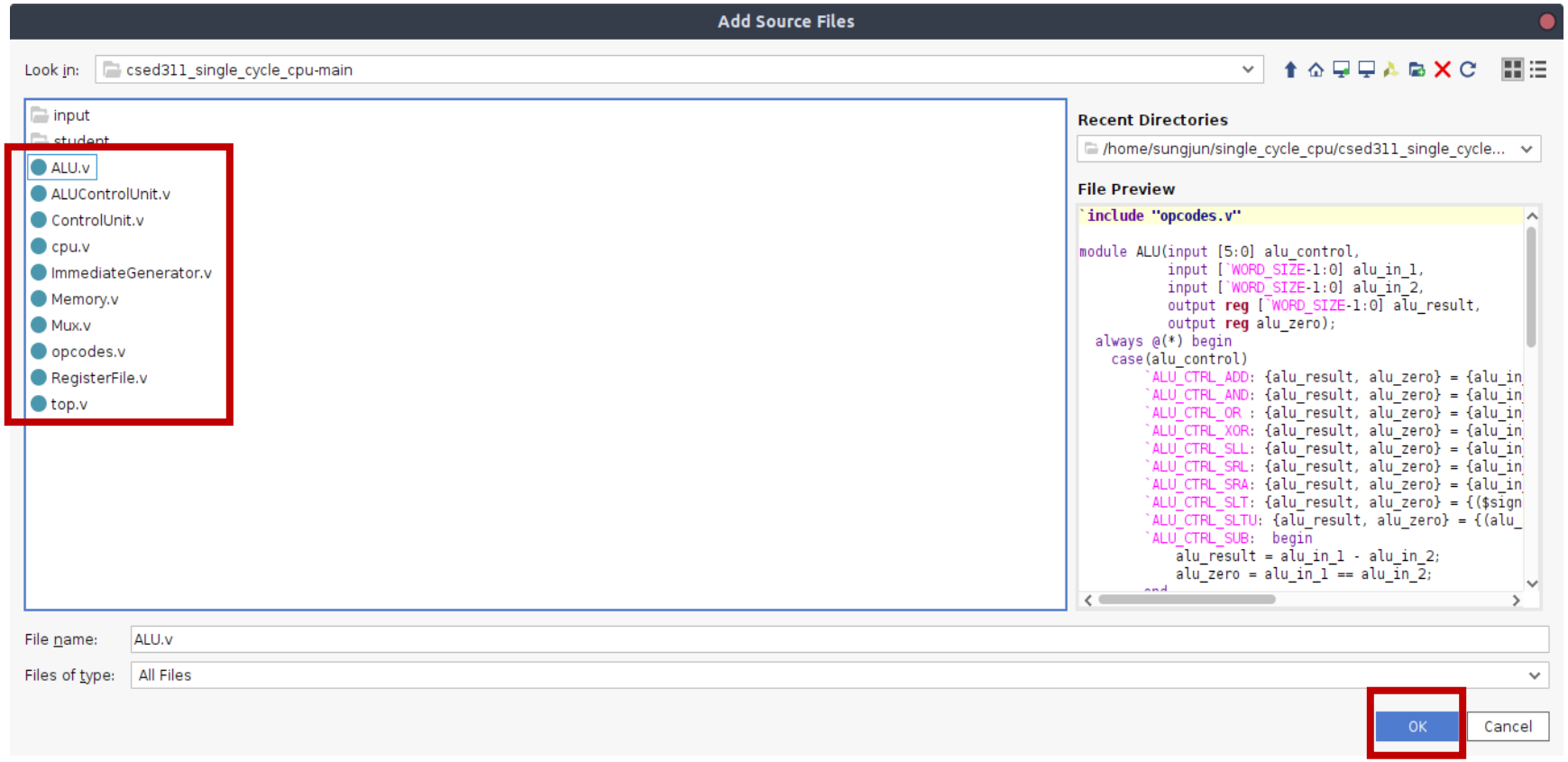
Import simulation files

- **Select default simulation set (sim_1) and click ‘Add Files’**



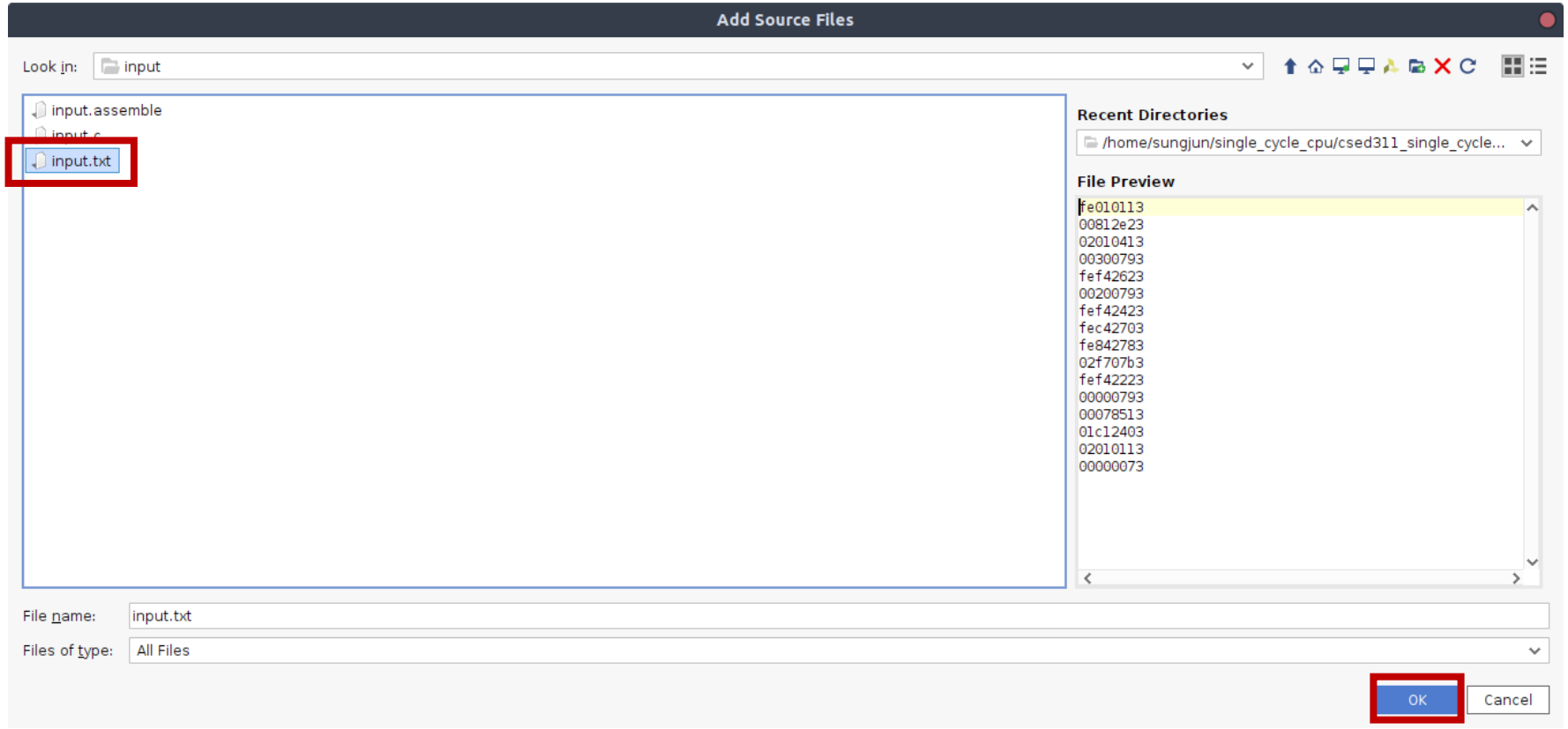
Import simulation files

- Select not only Verilog files (*.v) but also simulation input file (binary instructions)



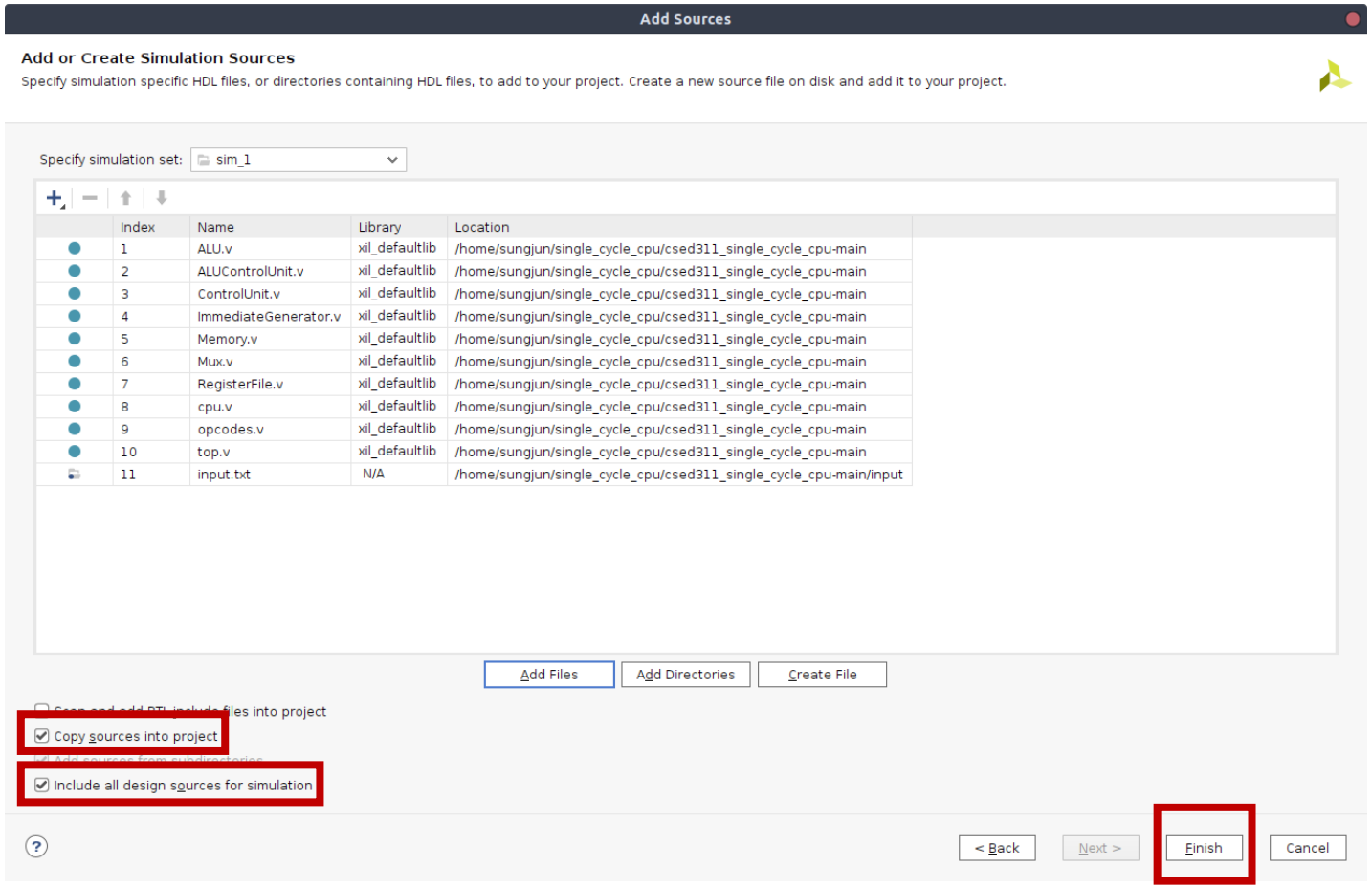
Import simulation files

- **Select not only Verilog files (*.v) but also simulation input file (binary instructions)**



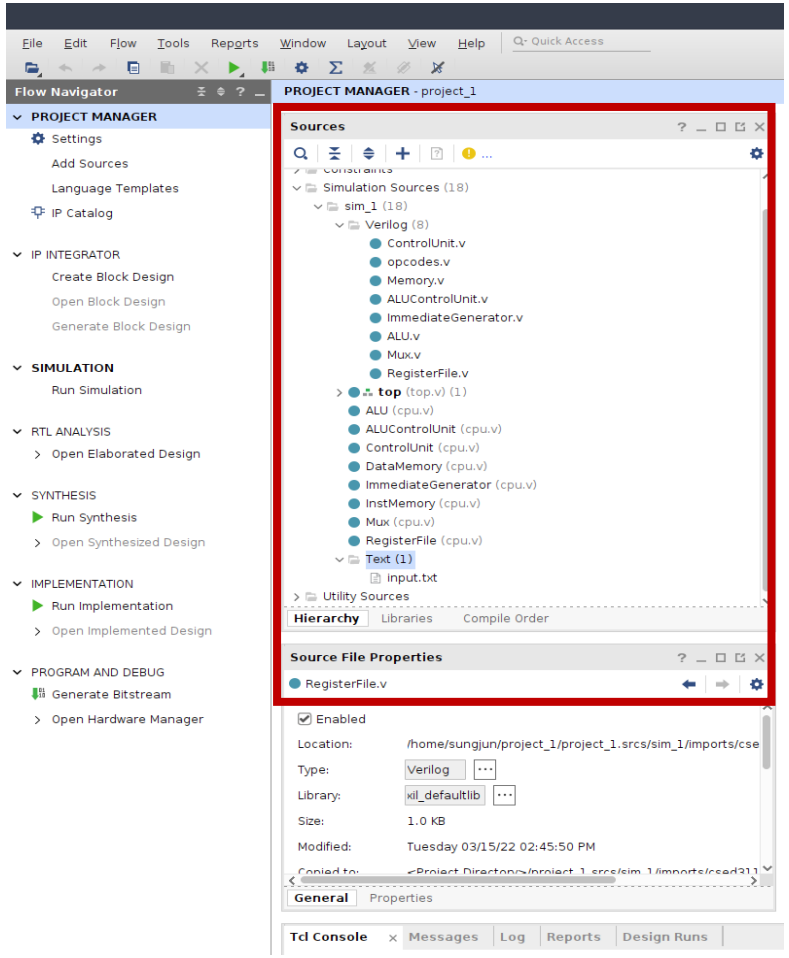
Import simulation files

- **Choose ‘Copy sources into project’ and ‘Include all design sources for simulation’**
  - The former copies (imports) your sources files into the project directory.
  - As a result, although you modify your files in Vivado project, the original source files will not be reflected.



Import simulation files

- **Import results**
- **You must verify whether both Verilog files and simulation input file are correctly imported**



Run simulation

- **From simulation, select ‘Run Simulation’ and ‘Run Behavioral Simulation’**