

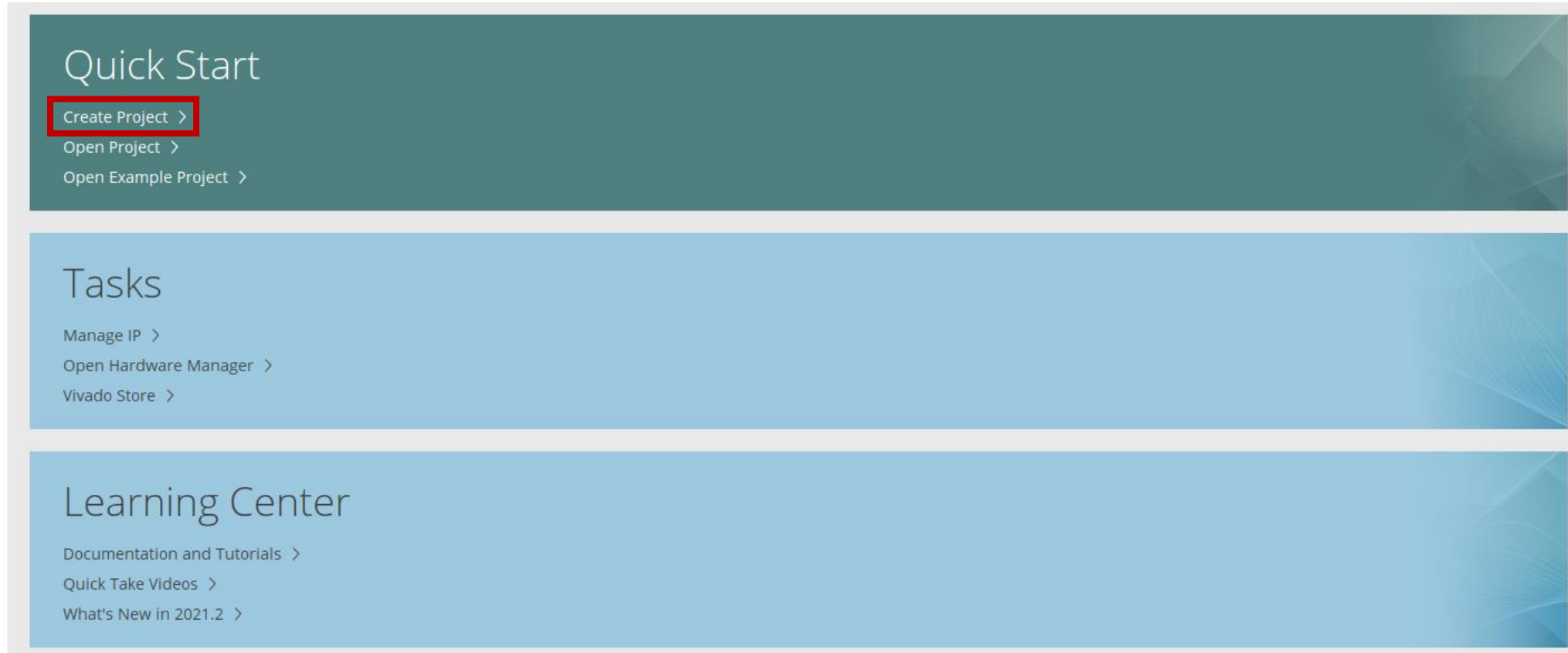
# Vivado simulation guide

CSED 311

Sungjun Cho

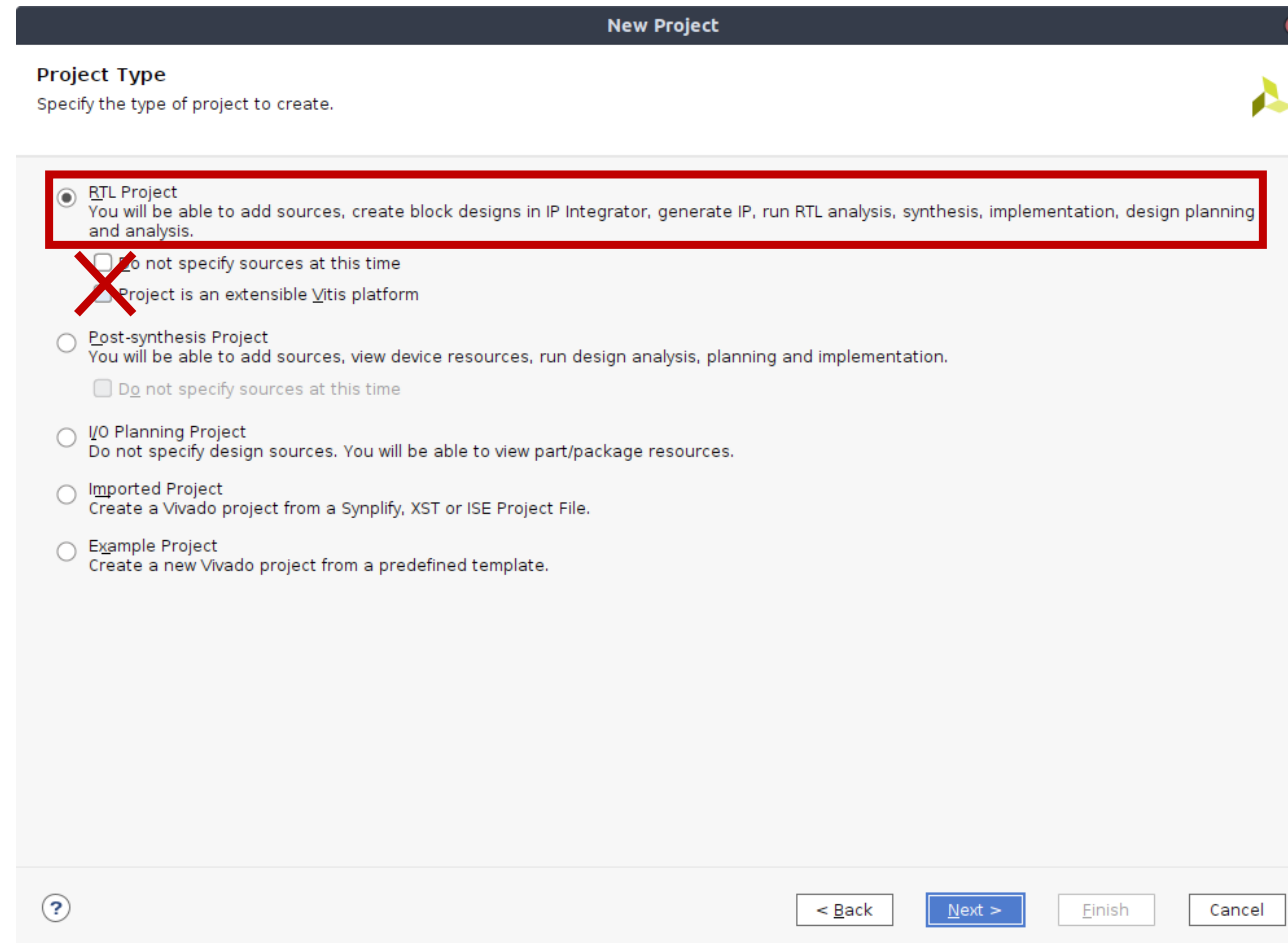
# Project setup

- Create project



# Project setup

- Choose RTL Project
  - Uncheck all check boxes under “RTL Project”



**New Project**

**Project Type**  
Specify the type of project to create.

☒ **RTL Project**  
You will be able to add sources, create block designs in IP Integrator, generate IP, run RTL analysis, synthesis, implementation, design planning and analysis.

☒ Do not specify sources at this time

☒ Project is an extensible Vitis platform






☐ **Post-synthesis Project**  
You will be able to add sources, view device resources, run design analysis, planning and implementation.

☐ Do not specify sources at this time

☐ **I/O Planning Project**  
Do not specify design sources. You will be able to view part/package resources.

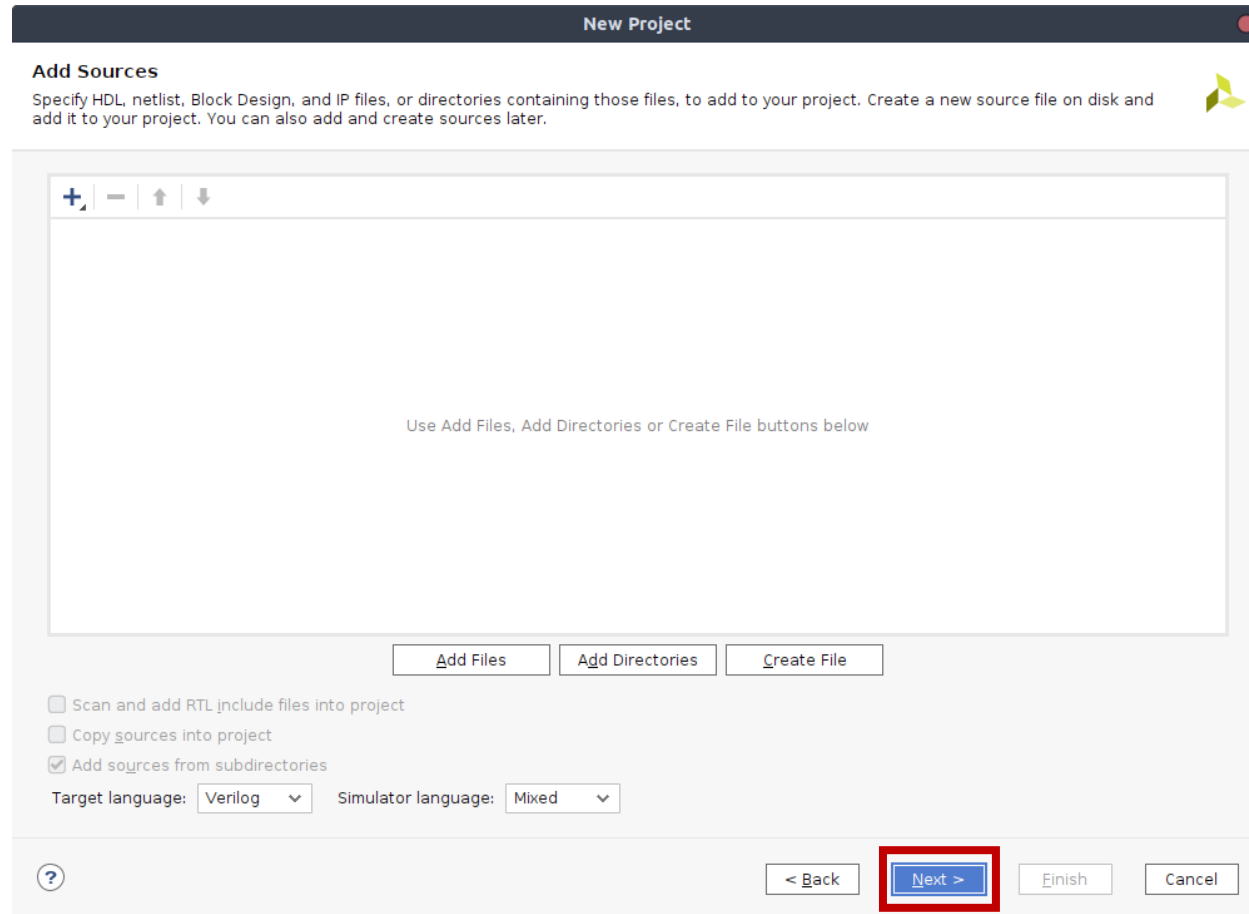
☐ **Imported Project**  
Create a Vivado project from a Synplify, XST or ISE Project File.

☐ **Example Project**  
Create a new Vivado project from a predefined template.

# Project setup

- **Do nothing** and go to Next



New Project

**Add Sources**

Specify HDL, netlist, Block Design, and IP files, or directories containing those files, to add to your project. Create a new source file on disk and add it to your project. You can also add and create sources later.

Use Add Files, Add Directories or Create File buttons below

Add Files Add Directories Create File

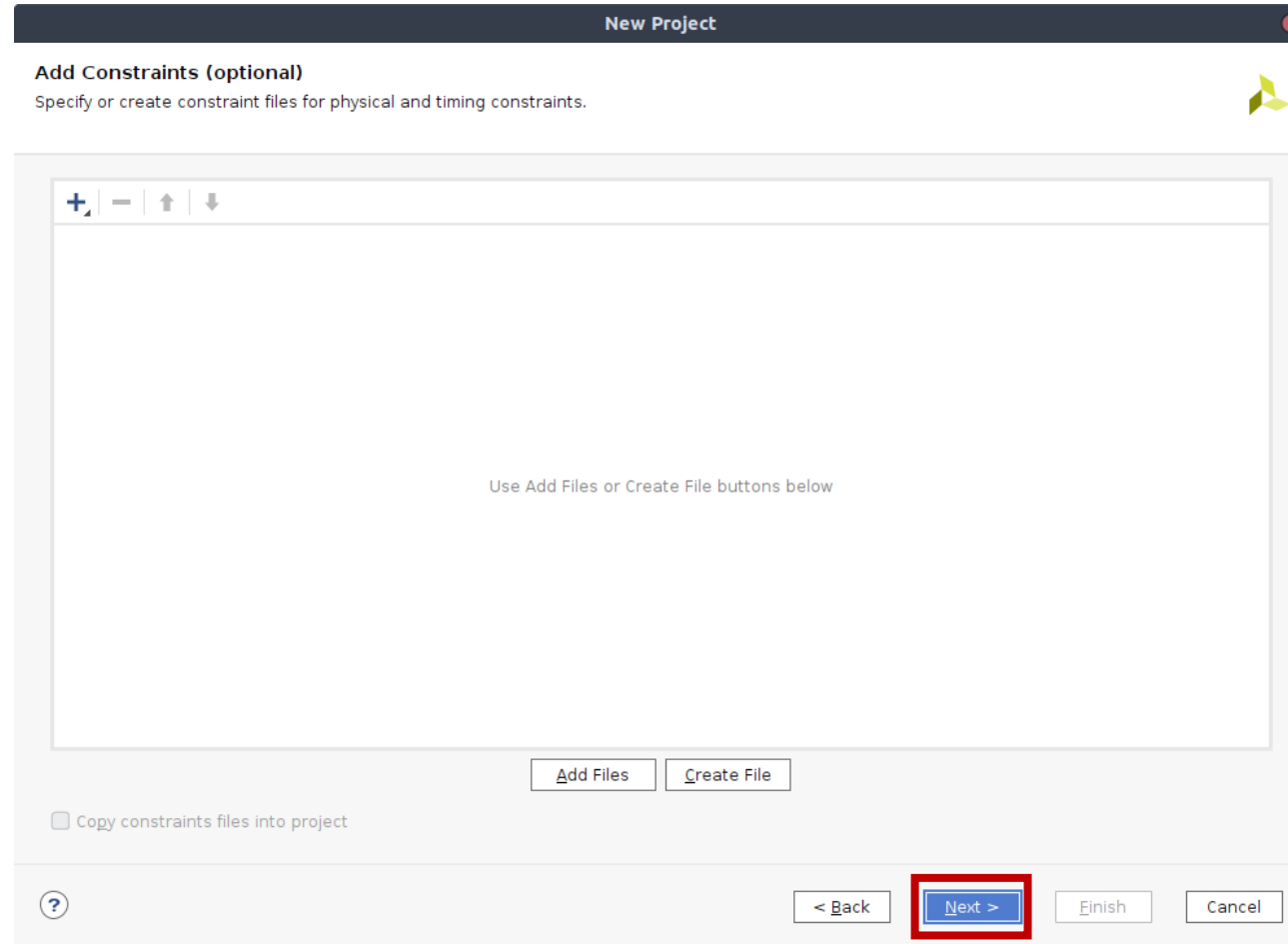
☐ Scan and add RTL include files into project  
☐ Copy sources into project  
☒ Add sources from subdirectories

Target language: Verilog Simulator language: Mixed

? < Back Next > Finish Cancel

# Project setup

- **Do nothing** and go to Next



# Project setup

- Select anything you want and go to next
  - This section is required for FPGA. However, because we do not use FPGA, we ignore this section

New Project

Default Part

Choose a default Xilinx part or board for your project.

Parts | Boards

[Reset All Filters](#)

Category: All

Package: All

Temperature: All

Family: All

Speed: All

Static power: All

Search: Q:

| Part             | I/O Pin Count | Available IOBs | LUT Elements | FlipFlops | Block RAMs | Ultra... ^1 | DSPs | Gb Transceiv |
|------------------|---------------|----------------|--------------|-----------|------------|-------------|------|--------------|
| xa7a12tcbg238-2I | 238           | 112            | 8000         | 16000     | 20         | 0           | 40   | 2            |
| xa7a12tcbg238-1I | 238           | 112            | 8000         | 16000     | 20         | 0           | 40   | 2            |
| xa7a12tcbg238-1Q | 238           | 112            | 8000         | 16000     | 20         | 0           | 40   | 2            |
| xa7a12tcbg325-2I | 325           | 150            | 8000         | 16000     | 20         | 0           | 40   | 2            |
| xa7a12tcbg325-1I | 325           | 150            | 8000         | 16000     | 20         | 0           | 40   | 2            |
| xa7a12tcbg325-1Q | 25            | 150            | 8000         | 16000     | 20         | 0           | 40   | 2            |
| xa7a15tcbg236-2I | 36            | 106            | 10400        | 20800     | 25         | 0           | 45   | 2            |
| xa7a15tcbg236-1I | 36            | 106            | 10400        | 20800     | 25         | 0           | 45   | 2            |
| xa7a15tcbg236-1Q | 236           | 106            | 10400        | 20800     | 25         | 0           | 45   | 2            |
| xa7a15tcbg324-2I | 324           | 210            | 10400        | 20800     | 25         | 0           | 45   | 0            |
| xa7a15tcbg324-1I | 324           | 210            | 10400        | 20800     | 25         | 0           | 45   | 0            |
| xa7a15tcbg324-1Q | 324           | 210            | 10400        | 20800     | 25         | 0           | 45   | 0            |
| xa7a15tcbg325-2I | 325           | 150            | 10400        | 20800     | 25         | 0           | 45   | 4            |
| xa7a15tcbg325-1I | 325           | 150            | 10400        | 20800     | 25         | 0           | 45   | 4            |

?

< Back

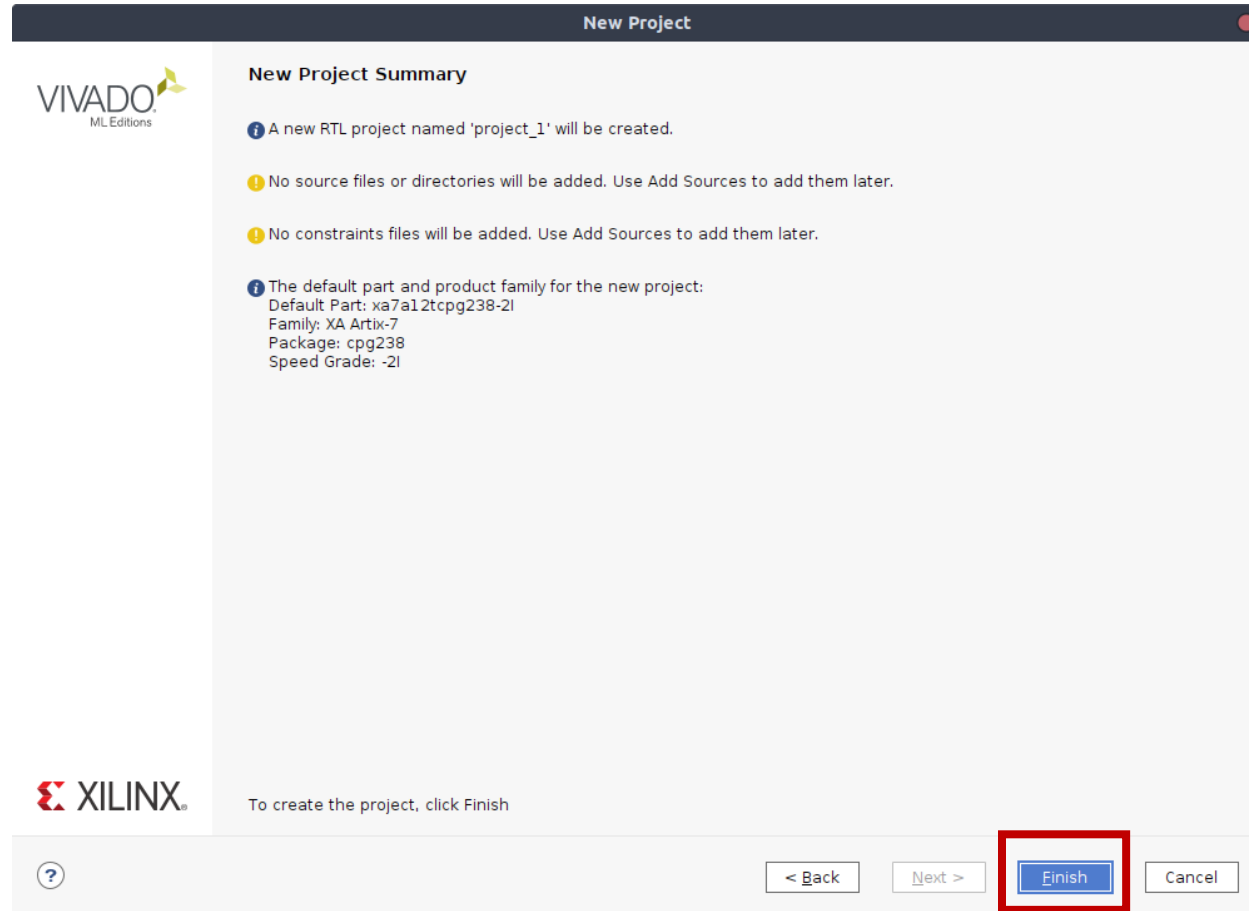
Next >

Finish

Cancel

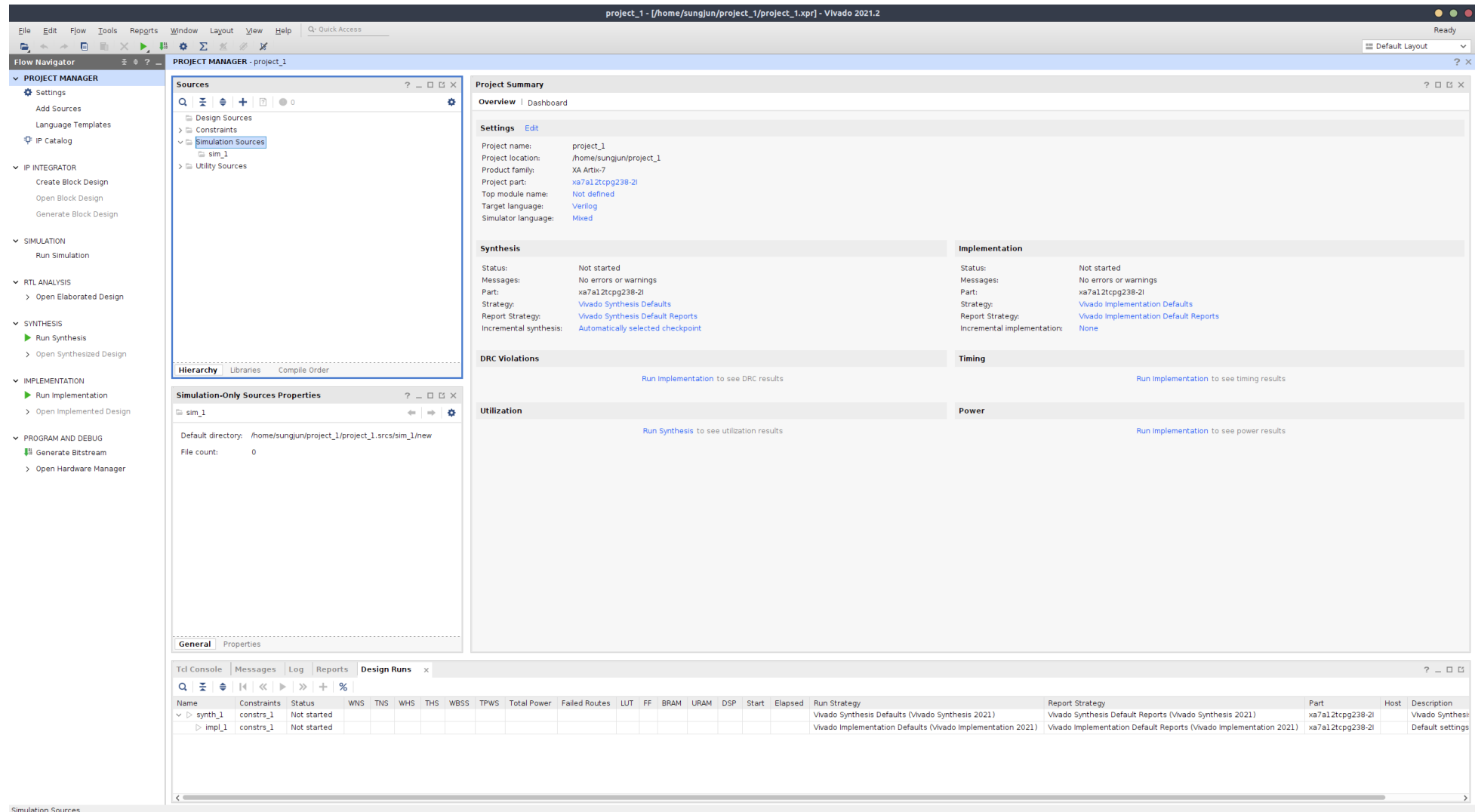
# Project setup

- Finish project setup



# Import simulation files

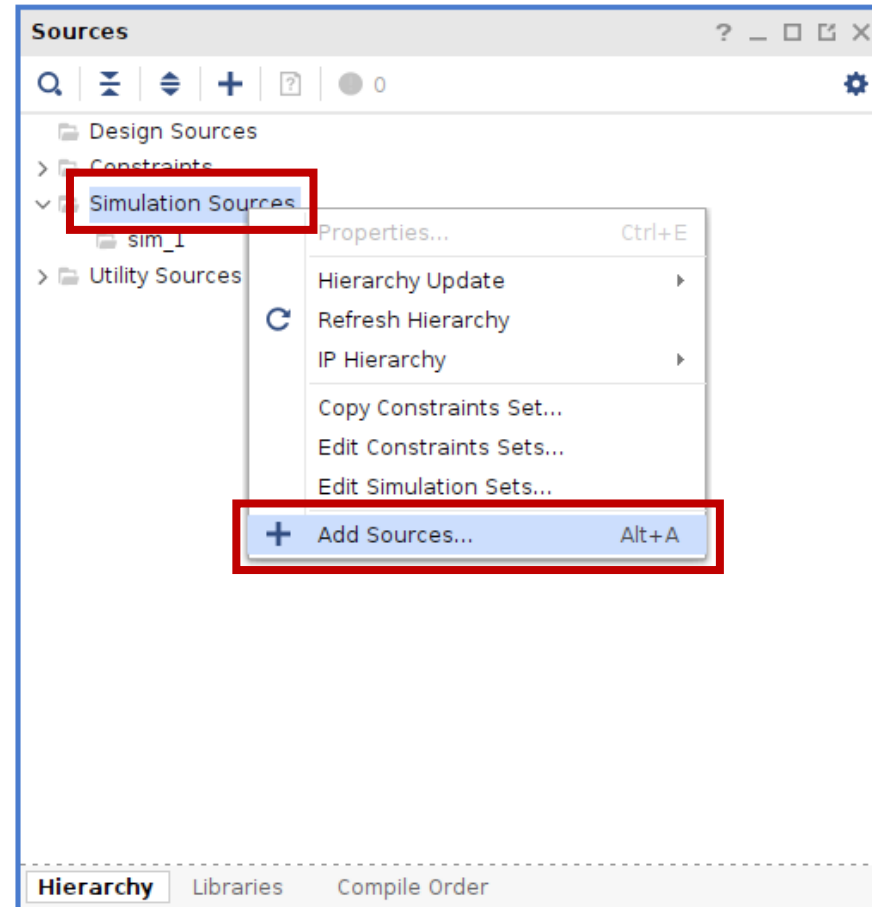
- This is the project main page





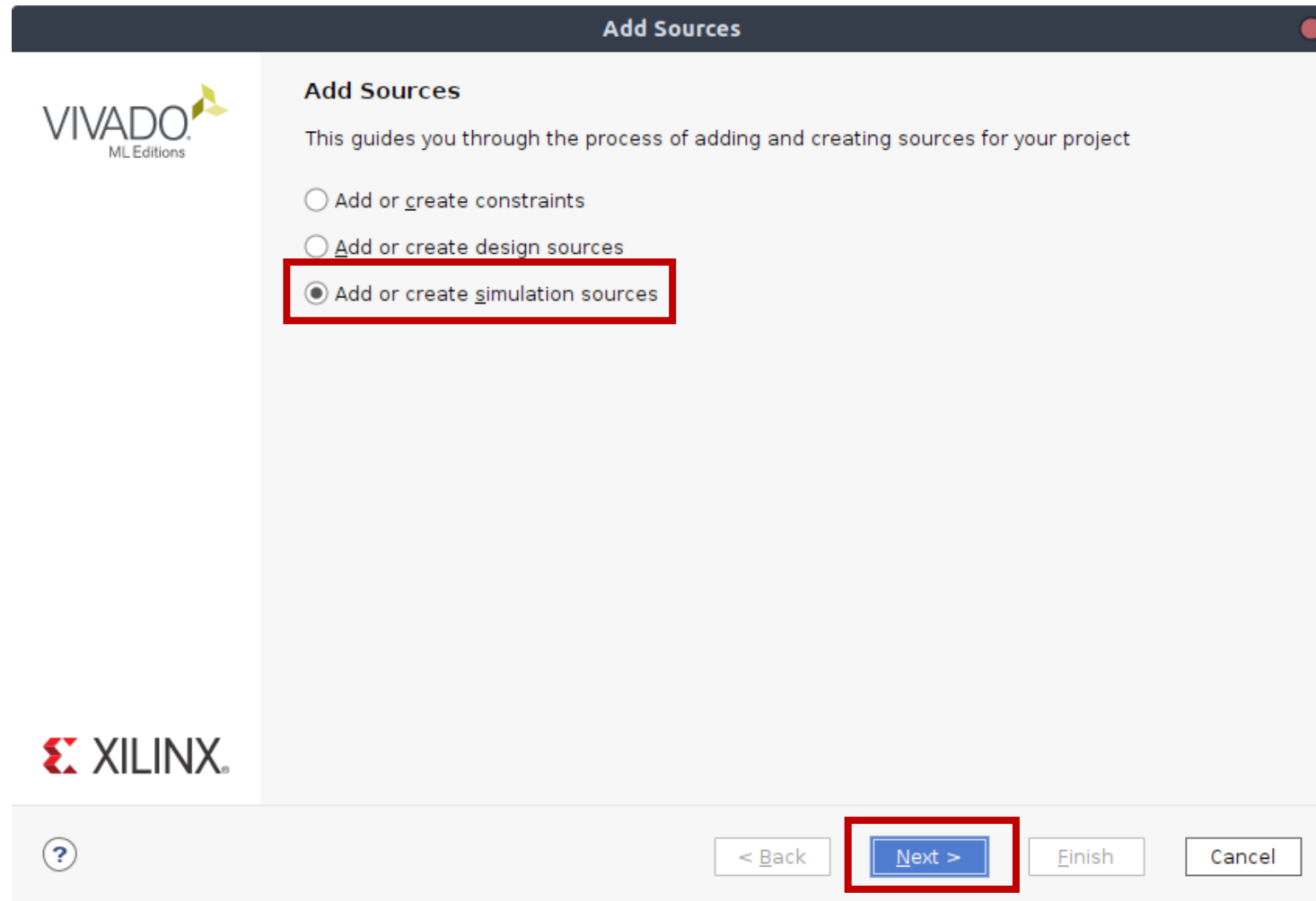
# Import simulation files

- Click 'Add sources' from 'Simulation Sources'



# Import simulation files

- Choose 'Add or create simulation sources'



# Import simulation files

- Select default simulation set (sim\_1) and click 'Add Files'

**Add Sources**

**Add or Create Simulation Sources**

Specify simulation specific HDL files, or directories containing HDL files, to add to your project. Create a new source file on disk and add it to your project.

Specify simulation set: sim\_1

Use Add Files, Add Directories or Create File buttons below

Add Files Add Directories Create File

☐ Scan and add RTL include files into project

☐ Copy sources into project

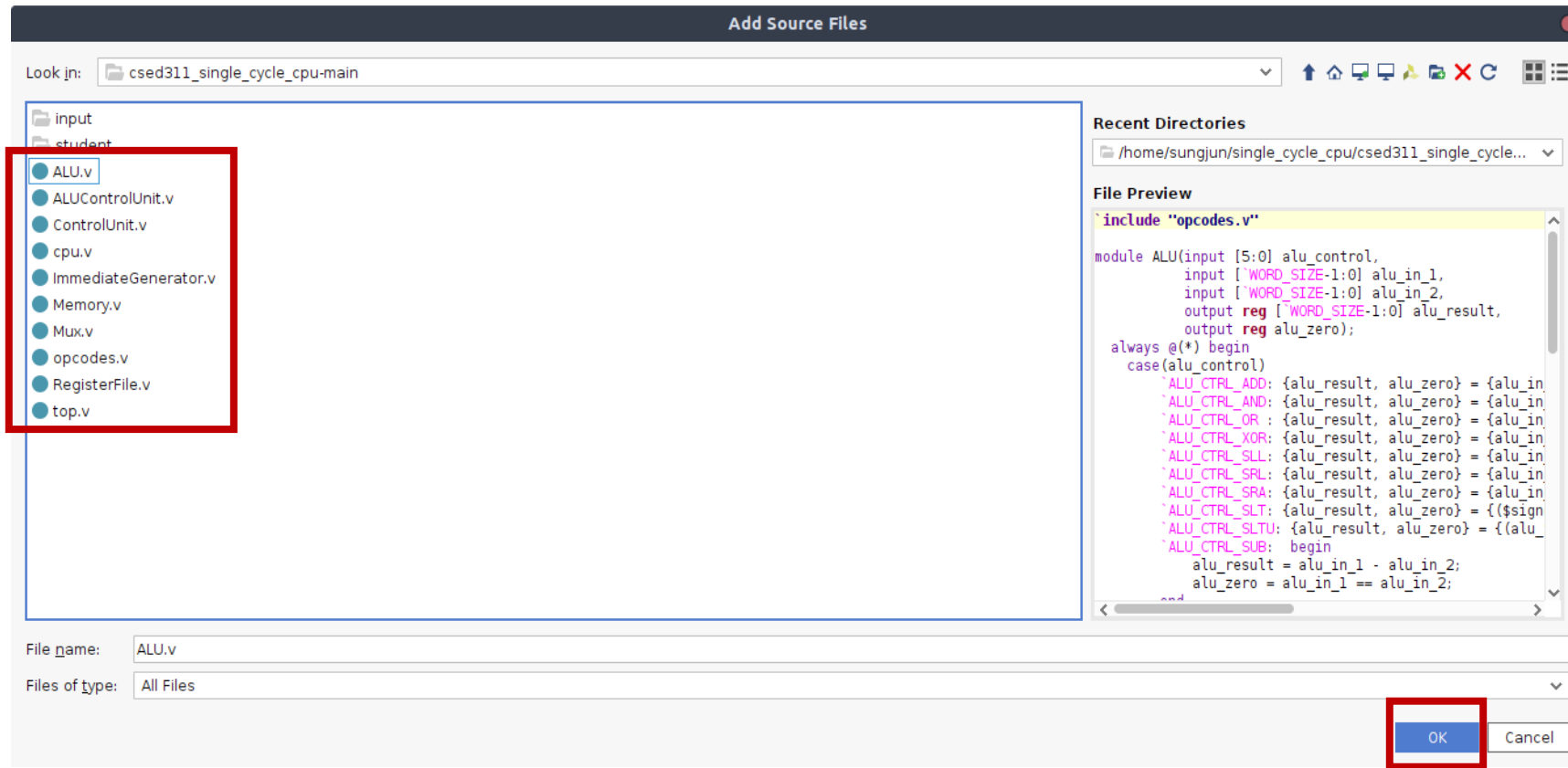
☒ Add sources from subdirectories

☒ Include all design sources for simulation

? < Back Next > Finish Cancel

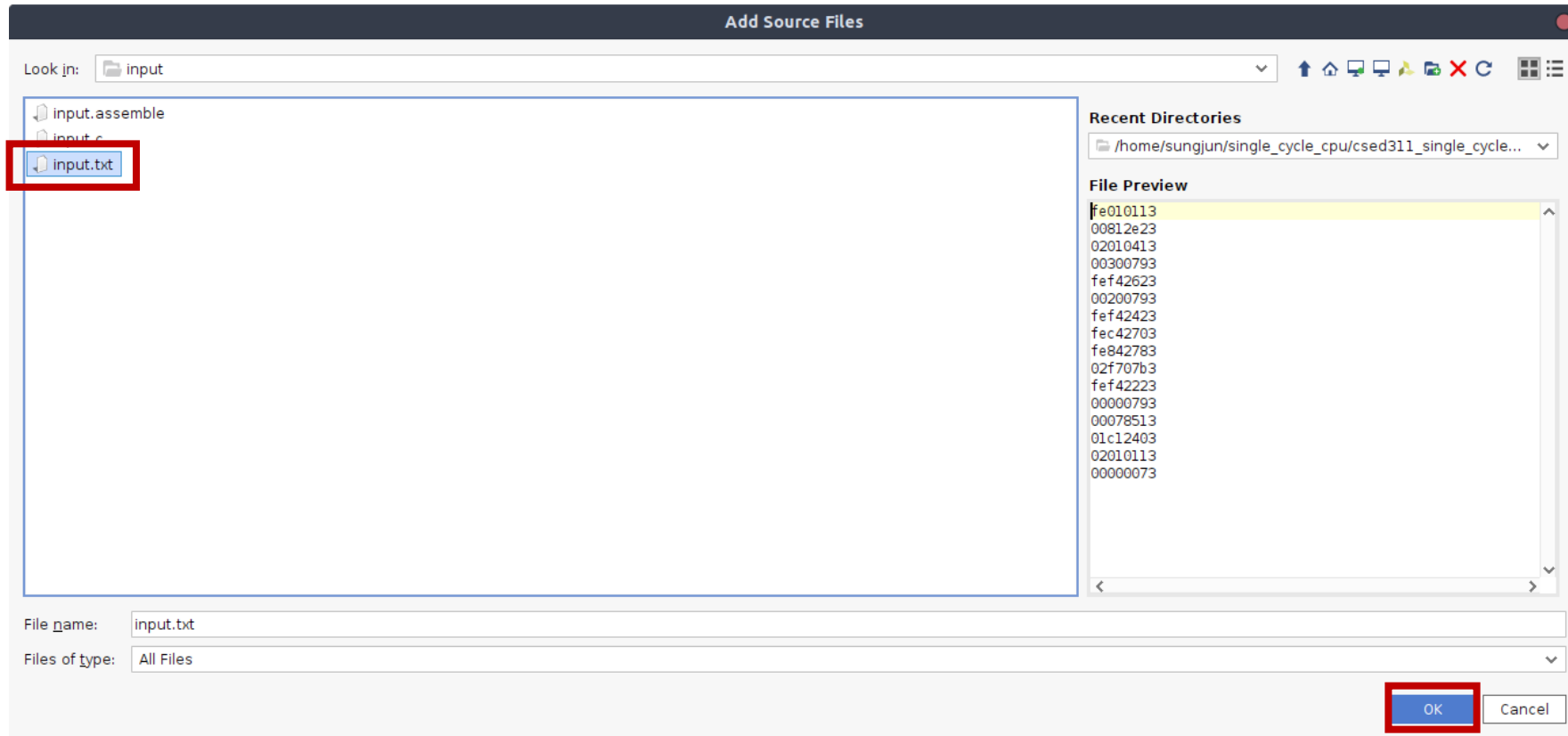
# Import simulation files

- Select not only Verilog files (\*.v) but also simulation input file (binary instructions)



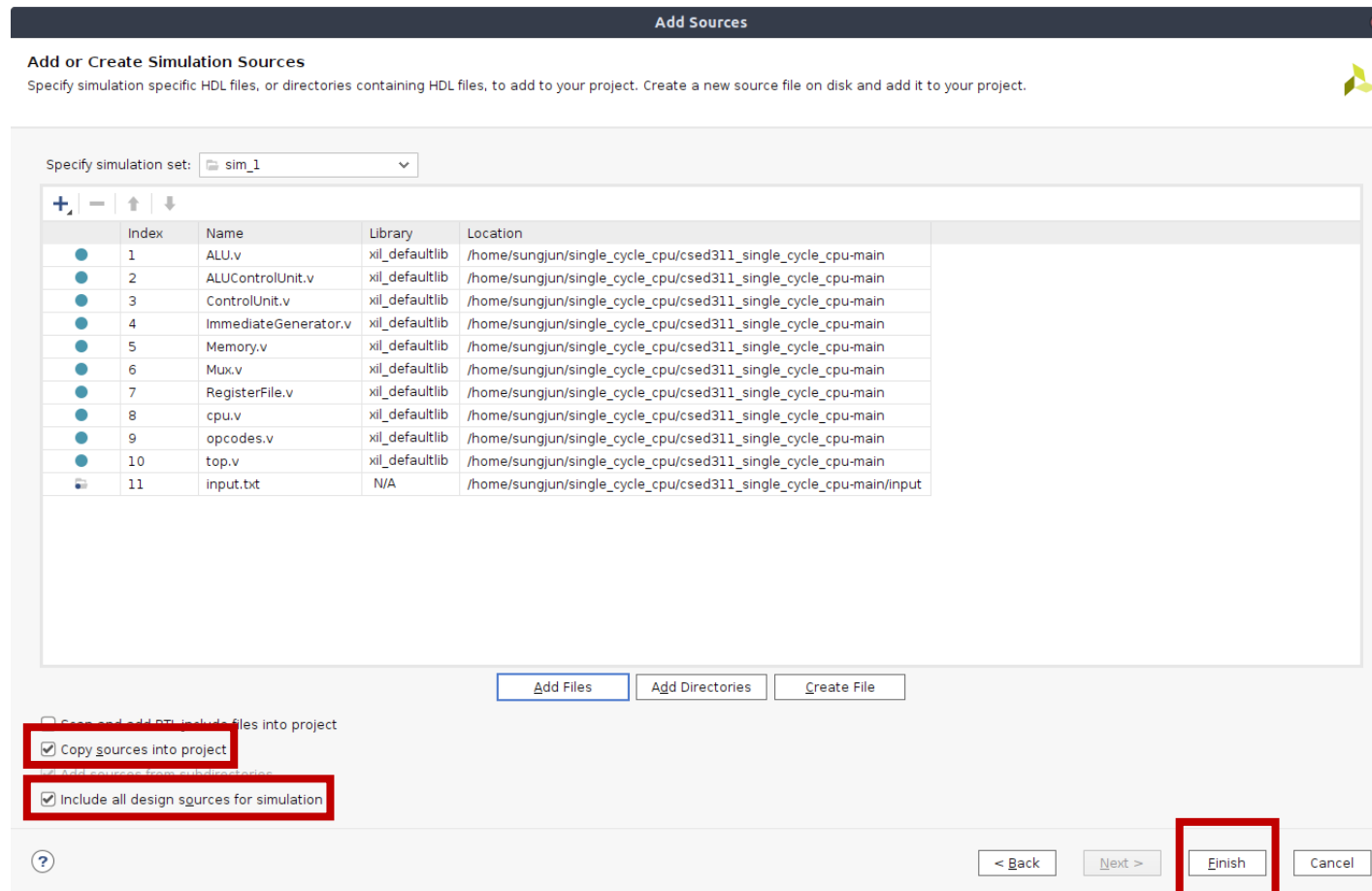
# Import simulation files

- Select not only Verilog files (\*.v) but also simulation input file (binary instructions)



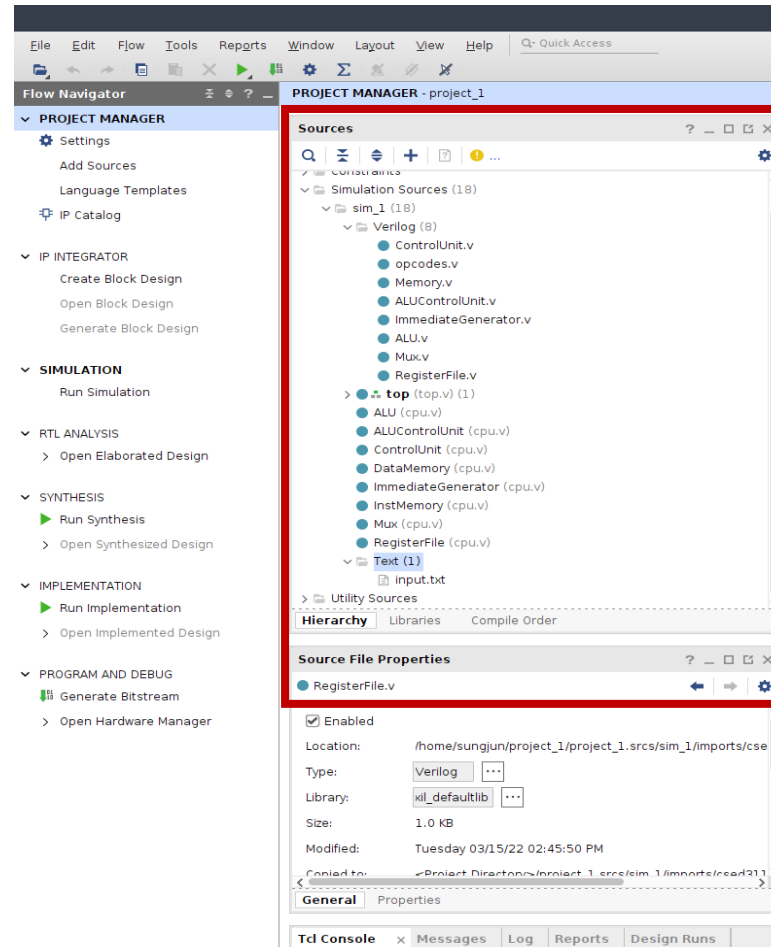
# Import simulation files

- Choose 'Copy sources into project' and 'Include all design sources for simulation'
  - The former copies (imports) your sources files into the project directory.
  - As a result, although you modify your files in Vivado project, the original source files will not be reflected.



# Import simulation files

- Import results
- You must verify whether both Verilog files and simulation input file are correctly imported



# Run simulation

- From simulation, select 'Run Simulation' and 'Run Behavioral Simulation'

