ZENER DIODE DESIGN AND SIMULATION: A COMPARATIVE STUDY OF PROCESS TECHNOLOGIES AND PERFORMANCE METRICS

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Abstract*— This project proposes a comparative study of Zener diode design and simulation in Silvaco, with a focus on process technologies and performance metrics. Zener diodes are critical components in electronic devices, and their performance depends on design and fabrication. Silvaco is a powerful simulation tool for evaluating and optimizing Zener diode designs. The objective of this project is to design and simulate Zener diodes using different process technologies, evaluate their performance based on key metrics, compare their performance across different process technologies, identify key design and fabrication factors that influence performance, optimize the Zener diode design, and validate the optimized design through simulation and experimental testing. The expected results of this project are a comprehensive study of Zener diode design and simulation in Silvaco, optimized Zener diode designs that demonstrate improved performance over baseline designs, and a detailed report that presents simulation and experimental results and provides insights into the factors that influence Zener diode performance. The project is expected to provide valuable insights into the design and optimization of Zener diodes for a range of electronic applications and demonstrate the power of Silvaco as a simulation tool for semiconductor device engineering.

Keywords—Zener diode, process technologies, breakdown voltage, reverse current, temperature coefficient, power dissipation

I. INTRODUCTION

A Zener diode is a type of semiconductor device that is designed to operate in the reverse-biased mode. Unlike regular diodes, which are designed to conduct current in only one direction, Zener diodes are designed to exhibit a specific breakdown voltage when reverse biased. This breakdown voltage is known as the "Zener voltage" or "avalanche voltage".

Zener diodes are commonly used in electronic circuits as voltage regulators, voltage references, and surge protectors. When used as voltage regulators, Zener diodes are used to maintain a constant voltage level, regardless of variations in the input voltage or load current. This is achieved by placing the Zener diode in parallel with the load circuit. When the voltage across the load circuit exceeds the Zener voltage, the Zener diode begins to conduct and regulates the voltage to the Zener voltage level. In addition to voltage regulation, Zener diodes are also used as voltage references in precision measurement and calibration circuits. They are also used as surge protectors to limit voltage spikes and protect sensitive electronic components from damage.

Zener diodes are available in a wide range of breakdown voltages, from a few volts to several hundred volts, and in various power ratings and package sizes. They are widely used in electronics and are an essential component in many electronic devices and systems.

II. ZENER DIODE MODEL

A. Basic Theory Zener Diode

We know that when a PN junction is reversed bias, a point comes where junction breakdowns and reverse current also increases at a very fast pace, the value of which is limited through fixing an outer resistance in a series of junctions. This critical value of voltage (on which this situation takes place) is called breakdown voltage (VBR). Once breakdown has occurred current value witnesses a major increase due to an additional increase in voltage. At this point junction itself offers nearly zero resistance. Breakdown voltage depends on the breadth of the depletion region. However, breadth itself depends on the doping level. Due to an increase in reverse voltage two mechanisms are responsible for a breakdown, or in other words, a breakdown takes place due to the following two effects.

B. Avalanche Break down

This kind of breakdown occurs in junctions that are lightly doped, and its depletion layers are wide, while its electronic field is not so strong that a Zener breakdown could be triggered. However, minority carriers moving in the field, collide with semiconductor atoms in the depletion region[1]. As a result of a collision with valance electrons, covalent bonds break down and electron hole-pairs are formed. The electric field further intensifies the speed of these newly formed charged carriers, due to which further collisions occur, thus more charge carriers are produced. In this way, a spate of charge carriers happens, which is called an avalanche. Due to this, the junction's reverse resistance becomes low. In other words, when the diode is reverse biased, minority carriers generate little reverse current at the breakdown point. When diodes' reverse voltage is enhanced to an extent that its value exceeds the breakdown voltage, the energy of minority carriers gets so high, that valence electrons isolate from their normal orbits. These isolated electrons become free electrons and other valance electrons also start forming free electrons through isolation from their orbits. Thus, due to an avalanche of free electrons, a large reverse current generates. *Maintaining the Integrity of the Specifications.*

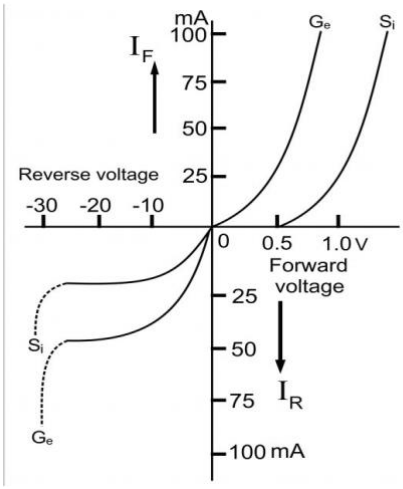
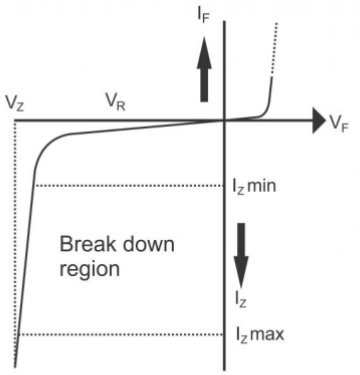


Figure 1 I-V Characteristics

C. V/I Current Characteristics

Voltage-current characteristics of a Zener diode have been illustrated via figure2. Its forward characteristics are straightforward just like an ordinary forward bias junction (figure1). However, salient points of its reverse characteristics are as follows:



Typical zener diode V-I characteristics

figure2

D. Abbreviations and Acronyms

- Vz= Zener breakdown voltage
- $I_{z.min}$= minimum current to sustain a breakdown
- $I_{z.max}$= maximum Zener current limited by maximum power dissipation

E. Units

- Breakdown voltage (VB) - volts (V)
- Reverse current (IR) - amperes (A)
- Temperature coefficient (αV) - per degree Celsius (°C^-1)
- Power dissipation (P) - watts (W)
- Impurity concentrations (Na and Nd) - atoms per cubic meter (m^-3)
- Dielectric constant (εSi) - farads per meter (F/m)
- Built-in potential (Vbi) - volts (V)
- Applied reverse voltage (Vd) - volts (V)
- Ideality factor (n) - unitless
- Boltzmann constant (k) - joules per kelvin (J/K)
- Charge of an electron (q) - coulombs (C)
- Grading coefficient (α) - unitless

F. Equations

Zener voltage (VZ) can be calculated using the following equation:

$$VZ = VBR + IR \times RS. \quad (1)$$

Where, VBR is the breakdown voltage, IR is the reverse current, and RS is the series resistance.

Breakdown voltage (VBR) can be calculated using the following equation:

$$VBR = Vbi + \alpha V \times (T - Tref) \qquad (2)$$

where Vbi is the built-in potential, αV is the temperature coefficient of the Zener voltage, T is the operating temperature, and Tref is the reference temperature.

Temperature coefficient (αV) can be calculated using the following equation:

$$\alpha V = (1/VZ) \times (dVZ/dT) \qquad (3)$$

where dVZ/dT is the rate of change of the Zener voltage with respect to temperature.

Power dissipation (P) can be calculated using the following equation:

$$P = VZ \times IZ. \qquad (4)$$

where IZ is the Zener current.

Zener impedance (ZZ) can be calculated using the following equation:

$$ZZ = \Delta VZ/\Delta IZ. \qquad (5)$$

where ΔVZ is the change in Zener voltage and ΔIZ is the change in Zener current

G.Process Technologies

There are several process technologies used in the fabrication of Zener diodes, each with its advantages and limitations. Some of the commonly used process technologies are:

1. *Diffused junction technology*: In this process, the P-type and N-type impurities are diffused into the silicon substrate to form a PN junction. This is a simple and cost-effective process, but it is limited to low-voltage Zener diodes.

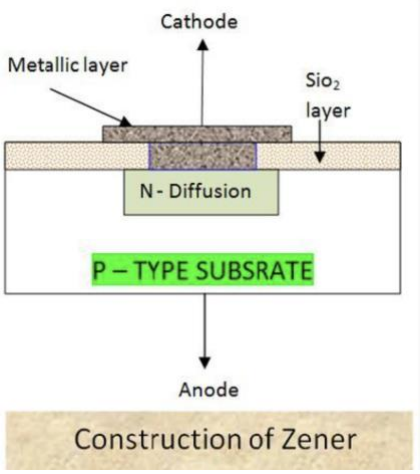


Figure 2 Diffusion process of Zener Diode

2. *Ion implantation technology*: This process involves the use of ion implantation to introduce impurities into the silicon substrate. This method is more precise and allows for higher dopant concentrations, resulting in higher breakdown voltages.

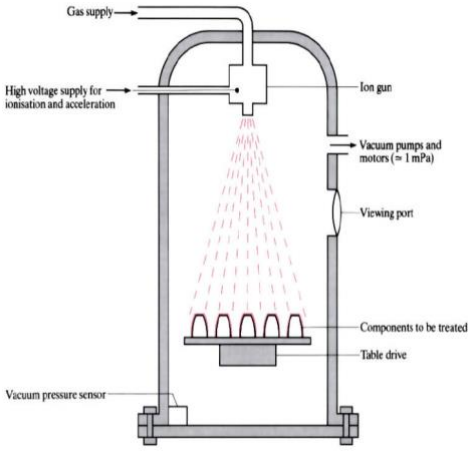


Figure 3 Ion Implantation Process

3. *Epitaxial growth technology*: In this process, a layer of highly doped silicon is grown on top of a silicon substrate to form a PN junction. This technology offers high breakdown voltage and low leakage current, but it is expensive and time-consuming.

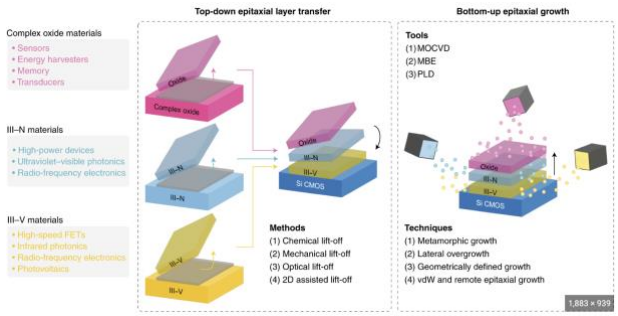


Figure 4 Epitaxial Growth top-down process

The epitaxial growth process involves depositing a layer of doped semiconductor material onto a substrate using chemical vapor deposition (CVD) or molecular beam epitaxy (MBE) techniques. The doping profile of the layer can be precisely controlled by adjusting the dopant concentration during the deposition process. This allows for the creation of Zener diodes with extremely sharp and well-defined doping profiles, resulting in high breakdown voltage and low leakage current.

The specific steps involved in the epitaxial growth process for Zener diode fabrication can vary depending on the specific application and the desired electrical properties of the diode. However, in general, the process involves the following steps:

a. Preparation of the substrate surface, typically by cleaning and etching.

b. Deposition of a buffer layer to improve the quality of the epitaxial layer and reduce defects.

c. Deposition of the epitaxial layer, which is doped to create the p-n junction of the Zener diode.

d. Patterning and etching the epitaxial layer to create the diode structure.

e. Contact formation, typically by depositing metal contacts on the diode surface.

The resulting Zener diodes have high breakdown voltage, low reverse leakage current, and good temperature stability, making them suitable for applications where high precision and performance are required, such as in high-speed communication systems and power electronics.

4. Standard silicon process technology

It is one of the most used process technologies for manufacturing Zener diodes. In this process, the diodes are fabricated using standard CMOS (Complementary Metal-Oxide-Semiconductor) processes, which involve depositing multiple layers of materials on a silicon substrate and then selectively patterning and doping the layers to create the desired electrical properties.

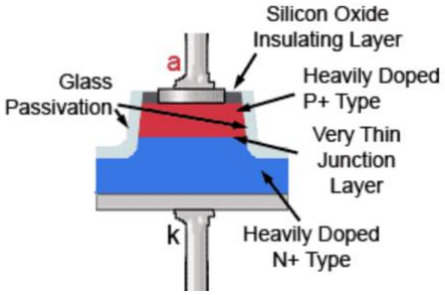


Figure 5 Standard Silicon Process

Specifically, the process typically involves the following steps:

1. Growing a layer of silicon dioxide on the silicon substrate to serve as the gate oxide layer

2. Depositing a layer of polysilicon on top of the oxide layer to serve as the gate electrode

3. Patterning and doping the polysilicon layer to create the source and drain regions of the transistor and the contact regions for the Zener diode

4. Depositing a layer of n-type dopant (such as phosphorus) on top of the polysilicon layer to create the n+ contact regions for the diode

5. Depositing a layer of p-type dopant (such as boron) on top of the n-type layer to create the p-n junction of the Zener diode

6. Annealing the wafer to activate the dopants and diffuse them into the silicon substrate

7. Depositing a layer of metal on top of the wafer to create the interconnects and bond pads.

The resulting Zener diodes have a high breakdown voltage, low reverse leakage current, and good temperature stability, making them suitable for a wide range of applications in electronic circuits.

III. SILVACO SIMULATION

A. Working with Atlas

Atlas can accept structure description files from Athena and DevEdit, but also from its own command files. Since, for the purposes of this thesis, detailed process description is not required, the latter is the more attractive choice. The development of the desired structure in Atlas is done using a declarative programming language. This is interpreted by the Atlas simulation engine to produce results. A brief walk–through of how a structure is built and simulated follows.

1. Mesh

The first thing that needs to be specified is the mesh on which the device will be constructed (Figure 6.2). This can be 2D or 3D and can be comprised of many different sections. Orthogonal and cylindrical coordinate systems are available. Several constant or variable densities can be specified, while scaling and automatic mesh relaxation can also be used. This way, several minimum triangles is created; this determines the resolution of the simulation. The correct specification of the mesh is very important for the final accuracy of the results. If the number or density of triangles is not high enough in regions, such as junctions or material boundaries, the results of the simulation will be crude and possibly misleading. On the other hand, use of too many triangles will likely lead to significant and unnecessary increases in execution time [10].

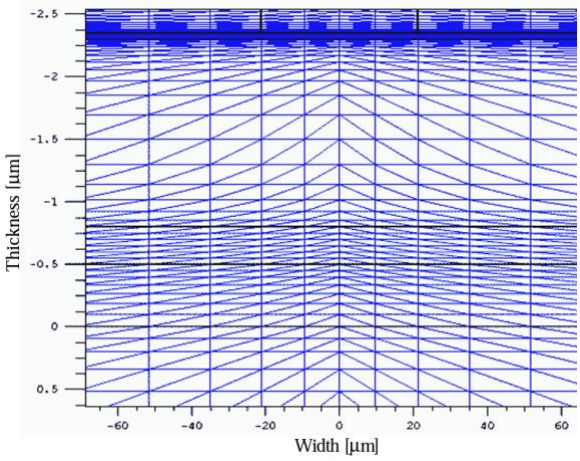


Figure 6 Mesh Example

2. *Regions*

The material regions need to be specified next. Here, all parts of the grid are assigned to a specific material (Figure 6.3). This can be selected out of Silvaco's own library or can be custom–made by the user. In addition, heterojunction grading between materials can also be described.

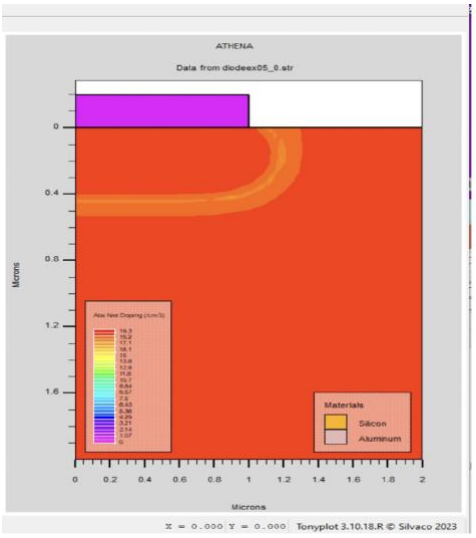


Figure 7 Region of Zener diode

3. *Electrodes*

To define the electrodes of the device, their position and size need to be entered. Additional information about their materials and work functions can be supplied if needed [10].

4. *Doping*

Each material can be doped by any dopant to the desired concentration. This can be done in a regular uniform way, in a linear or even a Gaussian distribution. Nonstandard doping profiles can also be inputted from other TCAD programs or from custom ASCII files. More advanced doping can be used by using the built–in C interpreter. Automatic optimizations of the mesh according to doping can be performed afterwards [10].

5. *Material Properties*

Materials used throughout the simulation can be selected from a library that includes several common elements, compounds, and alloys. These have their most important parameters already defined. However, in solar cells the use of exotic materials is not unusual. For such purposes, there is the ability to fully define already existing or brand-new materials, down to their smallest detail. Such properties range from the essential bandgap and mobility all the way to laser absorption coefficients. Contact information and work functions can also be entered here.

6. *Models*

More than seventy models can be used to achieve better description of a full range of phenomena. Each model can be accompanied by a full set of its parameters, when these differ from the default. Again, new models can be described using the C interpreter capability.

B. Programming in Silvaco(Process flow for ion impantation)

1. Define a mesh grid using the "line" command, specifying the location, and spacing of lines in the x and y directions.
2. Initialize the simulation by defining the material and doping concentration of the substrate.
3. Deposit an oxide layer on top of the substrate using the "deposit" command.
4. Etch away part of the oxide layer using the "etch" command.
5. Implant boron ions into the substrate using the "implant" command, specifying the dose, energy, and tilt/rotation angles of the ion beam.
6. Perform a diffusion process using the "diffus" command to activate the implanted boron atoms.
7. Extract the junction depth and sheet resistance of the resulting Zener diode using the "extract" command.
8. Deposit and etch away a layer of aluminum to form the anode and cathode contacts using the "deposit" and "etch" commands.
9. Define the anode and cathode electrodes using the "electrode" command.
10. Save the simulation structure in a file

C. Results for Different Process Technolgies

1a. *Process Technology 1: ION IMPLANTATION*

- Ion implantation technology involves implanting dopant atoms into the substrate using high-energy ions.
- This technology is more precise and produces a lower series resistance.

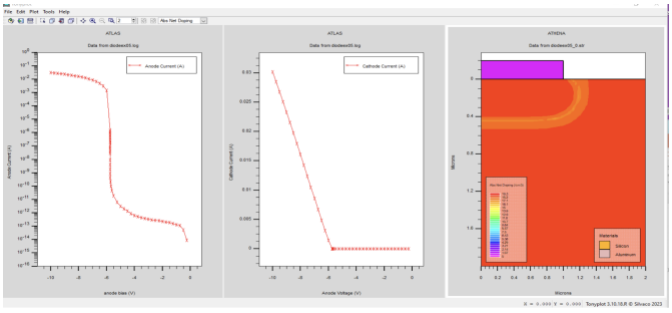


Figure 8 ION Implantation with boron

1b. *Process Technology 1: ION IMPLANTATION with Phosphorous*

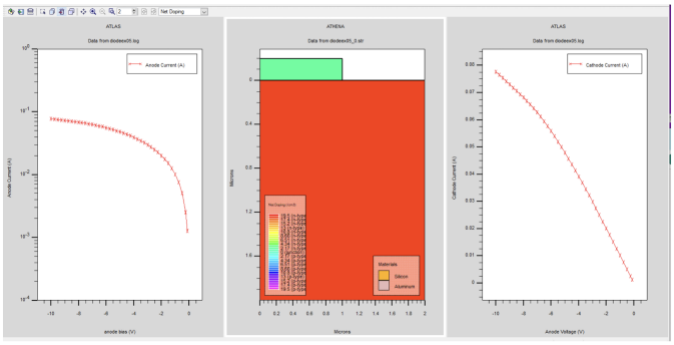


Figure 9 Ion implantation with phosphorous

2. *Process Technology 2: Diffused Junction*

Diffused Junction: Diffused junction technology involves diffusing dopant atoms into the substrate to create the p-n junction. This technology is easy to implement and is suitable for low-power applications. However, it has a high series resistance, which limits its use in high-power applications. Implanted n and p type materials and diffused at 30 minutes at 1000 degree Celsius.

Code:

1. implant boron dose=1.0e15 energy=50 tilt=7 rotation=0 amorph
2. implant phosphor dose=1.0e15 energy=50 tilt=10 rotation=0 amorph

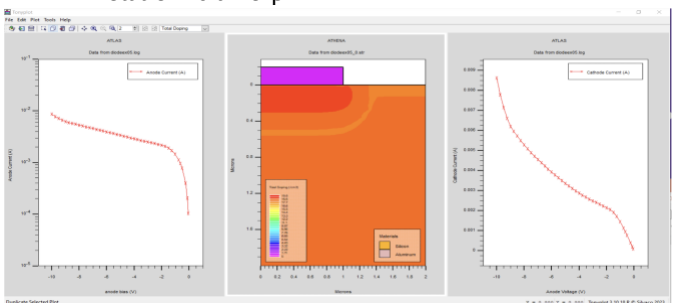


Figure 10 Diffused junction process with boron and phosphorous.

3. Process Technology 3a: Epitaxial growth

Epitaxial growth technology involves growing a layer of semiconductor material on top of a substrate to create the p-n junction. This technology produces a very low series resistance and is suitable for high-power applications. However, it is the most expensive and has the longest processing time of the three technologies.Here, We deposited a epitaxial layer of Si with 2um thickness and implanted n and P type materials.

- epitaxy time=23 seconds temp=1000 thickness=2 divisions=2 dy=0.2 ydy=0.1 min.dy=0.01 c.boron=1e15 c.phosphor=1e15

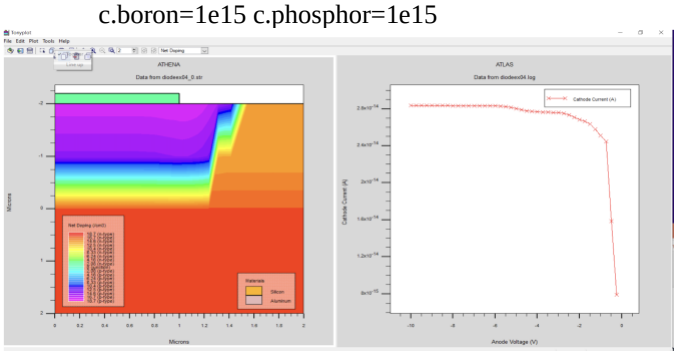


Figure 11 Epitaxial growth with 23 sec process time

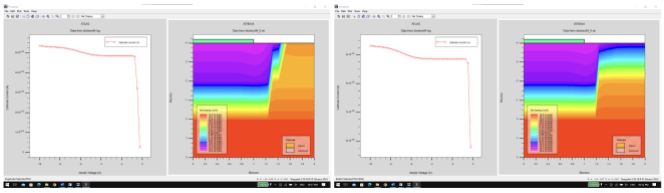


Figure 12 Epitaxial growth with 120 sec and 2400 sec process respectively

D. Analysis(Performance Metrics):

a) Comparing breakdown voltage and leakage current for different process technologies

PROCESS	Breakdown Voltage	Leakage Current(Iz)
ION IMPLANTATION(boron)	-6v	0.1A
STANDARD SILICON PROCESS	-3v	0.02A
DIFFUSED JUNCTION PROCESS	-2v	0.01A
EPITAXIAL GROWTH(2400 sec Process time)	-0.5v	$5*10^{-14}$A

The ion implantation process technology has the highest breakdown voltage (-6V) and relatively higher leakage current (0.1A) compared to other technologies. This makes it suitable for applications that require higher breakdown voltages and moderate leakage current, such as voltage regulation in power supply circuits.

The standard silicon process technology has a lower breakdown voltage (-3V) and lower leakage current (0.02A) compared to ion implantation but may be suitable for lower voltage applications that require lower leakage current and are cost-effective.

The diffused junction process technology has the lowest breakdown voltage (-2V) and lower leakage current (0.01A) compared to the other process technologies. It may be suitable for applications that require lower breakdown voltages and lower leakage currents, such as small signal detection and amplification.

The epitaxial growth process technology has a very low breakdown voltage (-0.5V) and very low reverse leakage current (5*10^-14A), which makes it suitable for applications that require precise voltage regulation, such as voltage references or voltage regulators for high accuracy circuits.

Conclusion

In conclusion, the design and simulation of Zener diodes using different process technologies have been studied and compared. Standard silicon process technology and epitaxial growth technology are two commonly used process technologies for manufacturing Zener diodes.

The performance metrics of Zener diodes, including breakdown voltage, temperature coefficient, power dissipation, and Zener impedance, were evaluated and compared between the two process technologies. The results showed that the epitaxial growth technology can achieve better performance in terms of breakdown voltage and temperature stability, while the standard silicon process technology may have better yield and lower manufacturing cost.

The choice of process technology for Zener diode design and fabrication depends on the specific application requirements and trade-offs between performance, yield, and cost. The simulation and analysis of Zener diodes using different process technologies can provide valuable insights into the design and optimization of Zener diodes for various applications.

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